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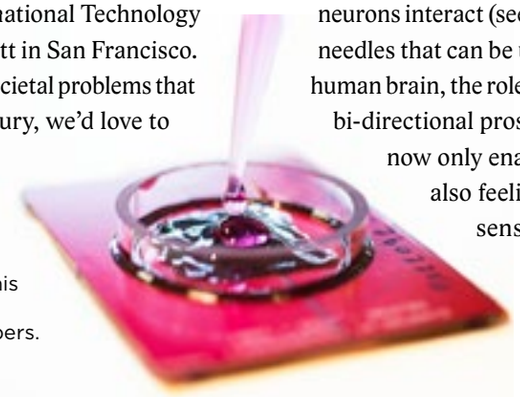
JULY 9, 2019
TUESDAY

Can Silicon Technology Help Transform Healthcare?

BY PETE SINGER, EDITOR-IN-CHIEF

The semiconductor industry has delivered breakthrough innovations in computer processing power and miniaturization over the last 70 years. Could it deliver similar results in the field of healthcare? That was the question addressed by Paru Deshpande, VP Life Sciences & Imaging at imec during a talk on Monday during imec's International Technology Forum at the Grand Hyatt in San Francisco. "When we think of the societal problems that we face in the 21st century, we'd love to see that same revolution happen in healthcare.



Petridish with in-vitro cell culture on a chip. This technology allows testing of cells in high numbers. Source: imec.

For us at imec and I think for many of you from the silicon technology side, there is a question of what role can silicon technology play in driving this revolution," he said.

He spoke of work at imec, where researchers have developed technologies where cells can be grown on a chip to analyze how neurons interact (see photo), chips with needles that can be used to analyze the human brain, the role chips could play in bi-directional prosthetics that would now only enable movement but also feeling, and the role of sensors, optical solutions and microfluidics. "We are

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DON'T MISS

9:15 am -2:30 pm
AI Design Forum
Blue Shield of California Theater at YBCA

2:00 pm – 4:00 pm
Applied AI in Design-to-Manufacturing
TechTALKS Theater North

2:30 pm -3:30 pm
Bulls and Bears
Blue Shield of California Theater at YBCA

3:30 pm – 4:00 pm
Beyond the Hype: The Journey of Big Data and IIOT from scratch to production deployment
Manufacturing Pavillion: Meet the Experts Stage

3:30 pm – 4:45 pm
Panel: Driving Growth in New Industry Inflections
Blue Shield of California Theater at YBCA

5:30 pm – 10:00 pm
Heart of Technology – HOT PARTY
John Collins Lounge

Intel Unveils New Tools in Its Advanced Chip Packaging Toolbox

This week at SEMICON West, Intel engineering leaders provided an update on Intel's advanced packaging capabilities and unveiled new building blocks, including innovative uses of EMIB and Foveros together and a new Omni-Directional Interconnect (ODI) technology.

- **Co-EMIB:** Intel's EMIB and Foveros technologies leverage high-density interconnects to enable high bandwidth at low power, with I/O density on par with or better than competitive approaches. The company's new Co-EMIB technology enables the linkage of even more computing performance and capability together.
- **ODI:** Intel's new Omni-Directional Interconnect provides even greater flexibility for communication among chiplets in a package. The top chip can communicate hori-

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EDWARDS

Rare, All-Electric Chinese SUV and Newest Chevy Autonomous Test Vehicle to be Previewed This Week

China's Xpeng Motors will display and dissect an automotive unicorn – a rare, all-electric sports utility vehicle – at SEMICON West this week. Also available for a look under the hood is General Motors' self-driving Chevrolet Bolt Cruise AV Autonomous Test Vehicle, featuring no more steering wheel to clutter the cockpit.

Xpeng Motors' G3 Smart SUV

Xpeng's G3 Smart SUV rolled its 10,000th vehicle off the company's Zhengzhou production line this month, while attaining top customer delivery numbers among new EV makers in China for 2019.

Loaded with microelectronics, including from among suppliers who will attend SEMICON West, the G3 comes equipped with smart autonomous driving and connectivity features, many of them first of their kind. Fully electric and seating five, the G3 features a voice-activated artificial intelligent assistant, driverless auto parking, heartbeat monitoring, facial recognition, a fatigue alert system and other utilization of new capabilities that rely on sophisticated electronics.

Like its future production model, the Chevy Bolt Cruise AV test vehicle to be displayed won't have a steering wheel. As a replacement for that old-fashioned guiding mechanism, the vehicle is equipped with an advanced sensor program capable of reacting to its surrounding environment 360 degrees, day or night. Central to the vehicle's command are computers using a combination of systems, including machine learning, dispatch and routing, remote assistance, simulation, planning and networking. It has been tested in one of the most complex driving environments in the U.S. – San Francisco.

The G3 and autonomous Bolt will be on display in the Smart Transportation Pavilion, which during SEMICON West's three days also will feature Meet the Experts sessions for:

- Government Regulatory Impact on Automotive Electronics
- Autonomous Driving: 2025 and Beyond
- Future Trends in Vehicle Electrification
- Advancements in Automotive Sensors
- Role of 5G for Smart Transportation

Platinum Sponsors for SEMICON West are Applied Materials, KLA, Lam Research and TEL. Other top sponsors are AEM Singapore, ASE, Burr & Forman LLP, Edwards, eSilicon Corporation, SAP and Silvaco.

Chevy Bolt Cruise AV test vehicle on display this week doesn't have a steering wheel

Show Daily Staff

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GOLD FLAG MEDIA LLC

Kerry Hoffman
Publisher
kerryh@semiconductordigest.com

Ed Korczynski
Senior Technical Editor
edk@semiconductordigest.com

Pete Singer
Editor-in-Chief
psinger@semiconductordigest.com

Dave Lammers
Contributing Editor
dplammers@att.net

Shannon Davis
Web Editor
sdavis@semiconductordigest.com

Dick James
Contributing Editor
dickjames@siliconics.ca

TRADESHOW MEDIA PARTNERS

Mark Larson
Production and Printing
mark@tsmpartners.com

Kevin Clarke
Layout and Design
kevin@tsmpartners.com

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70% water and you cannot dismiss that fact when you're thinking about healthcare solutions," he said.

He also spoke about the need for a manufacturing platform that – like semiconductor manufacturing -- can bring new technologies to the world. "There are more than 7 billion people out there. If you're going to come up with a healthcare solution, especially one with sophisticated technology, you need to do that with a platform that can actually address the entire community of the world," he said.

At last year's ITF, imec announced a novel organ-on-chip platform for pharmacological studies with unprecedented signal quality. It fuses imec's high-density multi-electrode array (MEA)-chip with a microfluidic well plate, developed in collaboration with Micronit Microtechnologies, in which cells can be cultured, providing an environment that mimics human physiology. Capable of performing multiple tests in parallel, the new device aims to be a

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More Stringent IPCC Guidelines Impact Semiconductor Manufacturing

The Intergovernmental Panel on Climate Change (IPCC), the United Nations' body for assessing the science related to climate change, recently released the latest refinement to its 2006 Guidelines. As part of an effort to tackle climate change, the refined regulations tighten control on new greenhouse gases used in semiconductor manufacturing and increase requirements for reporting and accountability for manufacturers.

"The IPCC has recognised that there is a gap between the amount of greenhouse gas measured in the atmosphere and the amount calculated from the inventory of known sources of emission," said Prof. Mike Czerniak, Visiting Industrial Professor, Bristol University, and Environmental Solutions Business Development Manager, Edwards. "The gap is of particular concern for gases such as perfluoro compounds (PFCs), which not only have extraordinarily high global warming potentials (GWP) but also extremely long lifetimes in the atmosphere, as long as 50,000 years."

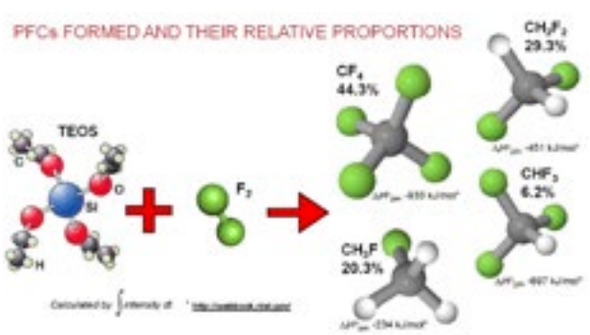

Figure 1. CF_4 formation during TEOS chamber clean.

The IPCC is the scientific organization supporting the United Nations Framework Convention on Climate Change (UNFCCC). Organized by the United Nations and the World Meteorological Organization, the IPCC's reports provide the scientific underpinnings for the international climate negotiations that led to the 1997 Kyoto Protocol and the 2015 Paris Agreement on climate change. The IPCC reviews the state of the science of climate change every 10-13 years.

"The reason that these refined guidelines have been upgraded was that there was a growing realization that there's a mismatch between what you measure in the atmosphere, which we refer to as top down and what's reportedly emitted by humanity which is termed bottom up," said Prof. Czerniak.

Two new mechanisms for PFC formation during semiconductor manufacturing have been identified and emission factors have been added to the latest IPCC refinement:

1. CF_4 formation by reaction of fluorine with hydrocarbon fuel in combustion-based abatement in systems that mix the fuel and process chamber effluent.
2. CF_4 formation when cleaning chemical vapor deposition (CVD) chamber deposits.

CF_4 is of particular concern because it has an atmospheric life of 50,000 years. "For all intents and purposes, that's forever," Czerniak said.

The semiconductor industry took a major step in reducing its carbon footprint years ago by largely replacing perfluorinated gases (PFCs) with less impactful gases, particularly NF_3 for processes such as CVD chamber cleaning. "That has massively reduced the carbon footprint of the industry and that was the main way that the industry was able to reach the World Semiconductor Council targets set for 2010," Prof. Czerniak said.

With the new IPCC guidelines, semiconductor manufacturers must consider how the NF_3 is treated with gas abatement systems, since it's possible to create CF_4 if the NF_3 is exposed to the fuel gas. "If you don't do your abatement in an optimal way, the fluorine that the NF_3 is converted into can react with methane or propane fuel gas," Prof. Czerniak said. "If you do mix the two together and you can actually create some new CF_4 that didn't exist before. For the first time ever, direct accountability required in the form of a data-backed certification from the equipment manufacturer that the reaction is minimized."

Edwards' inward-fired combustor avoids the mixing of chamber exhaust and fuel that, in other designs, can lead to the production of PFCs where they did not exist in the original exhaust stream. The lower, more uniform temperature profile of the inward-fired combustor ensures a high destruction removal efficiency (DRE), with low NOx generation. Inward-fired combustors have been standard on Edwards' abatement systems since the company started developing them in the 1990s. "What we do is we burn the fuel on the combustor pad inside our equipment, so what comes off from the pad and meets up with the fluorine is very, very hot nitrogen and Carbon Dioxide and water vapor," Prof. Czerniak explained. "It's the hydrogen in the water vapor that reacts with the fluorine and forms hydrogen fluoride (HF), which is very dilute acid. That's exactly what we want to happen." The dilute HF is treated in the fab's water treatment system, or in some cases repurposed for other industrial applications. In Japan, for example, it is used as part of ceramic making processes.

The new IPCC guidelines also point to the possible formation of CF_4 during certain semiconductor processes, such as CVD chamber cleaning. "Say you've been growing silicon dioxide using TEOS as your precursor gas," Prof. Czerniak said. "Each molecule of TEOS has four carbon atoms in it, and that carbon can get left on the walls of the chamber when you've done a processing run (Figure 1). When you're cleaning it with fluorine, it would react with that carbon and start making some CF_4. Customers are going to have to start accounting for that and hopefully abating it," he said.

The semiconductor industry has been relatively proactive with green initiatives such as PFC reduction, but it could potentially be pushed harder in that direction due to the rapid growth of automotive electronics. Consumers purchasing electric cars in an effort to reduce their carbon footprint, for example, may consider the environmental impact of the automotive manufacturing process, including the electronics supply chain.

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Applied Materials Introduces Two New Systems for Emerging Memories

Applied Materials, Inc. today unveiled innovative, high-volume manufacturing solutions aimed at accelerating industry adoption of new memory technologies targeting the Internet of Things (IoT) and cloud computing.

Today's high-volume memory technologies including DRAM, SRAM and flash were invented decades ago and have become ubiquitous in digital devices and systems. New memories – notably MRAM, ReRAM and PCRAM – promise unique benefits, but they are based on new materials that have been too challenging for high-volume manufacturing. Today, Applied Materials is introducing new manufacturing systems that allow novel materials – the key to these new memories – to be deposited with atomic-level precision. The company is delivering the most advanced systems it has ever developed to enable these promising new memories to be reliably produced at an industrial scale.

"The new Endura® platforms we are introducing today are the most sophisticated chip-making systems our company has ever created," said Dr. Prabu Raja, senior vice president and general manager of Applied's Semiconductor Products Group. "Our broad portfolio gives us the unique ability to integrate multiple materials engineering technologies along with on-board metrology to create new films and structures that were not possible until now. These integrated platforms illustrate the critical role that new materials and 3D architectures can play in giving the computing industry entirely new ways to improve performance, power and cost."

"IBM has been spearheading R&D of new memories for many years, and we see the need for these technologies increasing as the AI era demands improvements in chip performance and efficiency," said Mukesh Khare, vice president, Semiconductors, AI Hardware and Systems, IBM Research. "New materials and device types can play an important role in enabling high-performance, low-power embedded memory for IoT, Cloud and AI products. Applied Materials' high-volume manufacturing solutions can help accelerate the availability of these new memories across the industry."

"Improving the efficiency of data centers is a key priority for cloud service provider and enterprise customers," said Sung Gon Jin of SK hynix, head of the Advanced Technology Thin Film Group. "In addition to providing continued innovations in DRAM and NAND, SK hynix is pioneering the development of next-generation memories that can help boost performance and reduce power consumption. We value the work of Applied Materials in collaborating with us to speed the development of new materials and high-volume production techniques for promising emerging memories."

MRAM for the IoT

The computer industry is building the Internet of Things whereby sensors, computing and communications are incorporated into tens of billions of devices that will monitor their environments, make decisions and send critical information to cloud data centers. MRAM (magnetic random access memory) is a leading candidate to be the memory of choice for storing IoT device software and AI algorithms.

MRAM incorporates delicate magnetic materials commonly found in hard disk drives. MRAM is inherently fast and also nonvolatile, allowing software and data to be retained even when power is removed. Due to its fast performance and high endurance, MRAM may eventually be used as an alternative to SRAM in level 3 cache memory. MRAM can be incorporated into the back-end interconnect layers of IoT chip designs, thereby enabling smaller die sizes and lower costs.

Applied's new Endura® Clover™ MRAM PVD platform is made up of nine unique wafer processing chambers all integrated in pristine, high-vacuum conditions (Figure 1). It is the industry's first 300-millimeter MRAM system for high-volume manufacturing capable of individually depositing up to five different materials per chamber. MRAM memories require precise deposition of at least 30 different layers of material, some of which are 500,000 times thinner than a human hair. Process variations of just a fraction of the diameter of an atom can greatly affect device performance and reliability. The Clover MRAM PVD platform includes on-board metrology that measures and monitors thickness of the MRAM layers with sub-angstrom sensitivity as they are created, to ensure atomic-level uniformity without risking exposure to the outside environment.

Figure 1. The Endura® Clover™ MRAM PVD platform is made up of nine unique wafer processing chambers all integrated in pristine, high-vacuum conditions.

"As an extremely fast, high-endurance nonvolatile memory, MRAM is poised to displace embedded flash and level 3 cache SRAM in both IoT and AI applications," said Tom Sparkman, CEO of Spin Memory. "The availability of a high-volume manufacturing system from Applied Materials is a huge boost to the ecosystem, and we are thrilled to be working with Applied to deliver MRAM solutions and accelerate its adoption."

ReRAM and PCRAM in the cloud

As data generation grows exponentially, cloud data centers require order-of-magnitude improvements in the speed and power consumption of the data pathways linking servers and storage systems. ReRAM (resistive RAM) and

PCRAM (phase change RAM) are fast, non-volatile, low-power, high-density memories that can be used as "storage class memory" to fill the widening price-performance gap between server DRAM and storage.

ReRAM is made using new materials that act like a fuse, allowing filaments to be selectively formed within the billions of storage cells to represent data. In contrast, PCRAM incorporates the phase change material found in DVD disks, and bits are programmed by changing the state of the material from amorphous to crystalline. Similar to 3D NAND memories, ReRAM and PCRAM are arranged in 3D structures, and memory makers can steadily reduce the cost of storage by adding more layers with each product generation. ReRAM and PCRAM also offer the possibility of intermediate stages of programming and resistivity to allow multiple bits of data to be stored in each memory cell.

ReRAM and PCRAM both promise significantly lower cost than DRAM along with substantially faster read performance than NAND and hard disk drives. ReRAM is also a leading candidate for future in-memory computing architectures whereby computing elements are integrated into the memory arrays to help overcome the data movement bottleneck associated with AI computing.

Applied's Endura® Impulse™ PVD platform for PCRAM and ReRAM includes up to nine process chambers integrated under vacuum along with on-board metrology to allow the precise deposition and control of the multi-component materials used in these emerging memories (Figure 2).

Figure 2. The Endura® Impulse™ PVD platform for PCRAM and ReRAM includes up to nine process chambers integrated under vacuum along with on-board metrology.

"Uniform deposition of the new materials used in ReRAM memories is critical to achieving the highest possible device performance, reliability and endurance," said George Minassian, CEO and co-founder of Crossbar, Inc. "We specify the Applied Materials Endura Impulse PVD system with onboard metrology in our ReRAM technology engagements with memory and logic customers because it enables a breakthrough in these critical metrics."


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BISTel Launches New AI Powered Equipment Health Monitoring and Predictive Maintenance Solution for Smart Manufacturing

BISTel, a leading supplier of adaptive intelligence (AI) applications and equipment engineering solutions (EES) for smart manufacturing introduced a next-generation, AI powered equipment health monitoring and predictive maintenance (HMP) solution for smart manufacturing. HMP provides manufacturers with real-time, actionable insights into the health of their equipment and allows them to optimize performance, resulting in higher equipment utilization, better uptime, and substantially improved factory productivity. BISTel will demonstrate the new HMP in the Semicon West Smart Pavilion, Moscone Center.


W.K. Choi, CEO of BISTel

HMP is a fully integrated solution that addresses a myriad of manufacturing problems and bottlenecks that are a drag on production and engineering productivity. Today, manufacturers face three common threats to maintaining high quality, high productivity plants and equipment - Unscheduled production stoppages due to lack of asset monitoring, lack of plant-wide insights into the health of equipment caused by data fragmentation across the factory and highly inefficient equipment maintenance programs that increase production costs and increase the replacement cost of critical parts. HMP addresses these challenges.

Industry leading data visualization

Whether you are an operator, engineer or executive, HMP integrates seamlessly with all other factory data management systems to provide the ultimate data visualization experience by providing each user with factory insights they need when they need it resulting in better and more meaningful decision making.

"Our new HMP solution integrates A.I. based advanced machine learning technologies to help customers detect and classify faults real-time, then uses predictive analytics to determine when faults might occur in the future or when maintenance should be done. As a result, downtime is vastly reduced, and productivity is greatly increased," noted W.K. Choi, CEO of BISTel.

About HMP

HMP's fab wide, real-time monitoring maintains the health of equipment and web-based visualization improves decision making. For example, HMP collects, contextualizes, and analyzes data to enable role-based dashboarding for all users across the factory. Other benefits include:

- New AI enabled smart applications offer deeper manufacturing intelligence and better factory insights. For instance, fault detection enables an early warning equipment failure system to help eliminates downtime and real-time notifications allow speedy corrective responses.
- Fault classification applications provides timely, actionable insights on equipment failures which helps to reduce troubleshooting, repair time, and downtime.
- New, powerful A.I. predictive analytics enable data driven predictive maintenance which increases equipment utilization and eliminates downtime due to RUL failure.

HMP is available on Siemens' MindSphere cloud-based open IIoT operating system platform. It also is available on SK Telecom's Metatron cloud-based, asset performance management platform helping to provide powerful data analytics and manufacturing intelligence to customers globally.

Silicon Technology cont'd from p 3

game-changer for the pharmaceutical industry, offering high quality data in the drug development process.

Imec's solution packs 16,384 electrodes, distributed over 16 wells, and offers multiparametric analysis. Each of the 1,024 electrodes in a well can detect intracellular action potentials, aside from the traditional extracellular signals.

While great progress has been made, however, Deshpande cautioned that there is much more to be done. He said the work at imec and elsewhere show how far researchers can go in moving from conventional technologies to something that is working with the human body. "I think that will go only further as we look into the future because the reality is we are a full electrical system. There's more and more research and development being done to try and interface with that electrical system. People are looking at devices to control disorders of the brain, to control signals in the heart, but also disorders like rheumatoid arthritis, gastrointestinal disorders, and even things like diabetes," he said. "So perhaps it's too optimistic to say we will go from pills to chips, but I think there is a role for silicon in this and as more research is done to understand us as an electrical system, we will see more and more opportunity for devices that actually interface with that system."

Intel cont'd from p 3

zontally with other chiplets, similar to EMIB. It can also communicate vertically with through-silicon vias (TSVs) in the base die below, similar to Foveros.

- **MDIO:** Building upon its Advanced Interface Bus (AIB) PHY level interconnect, Intel disclosed a new die-to-die interface called MDIO. The technology enables a modular approach to system design with a library of chiplet intellectual property blocks.

Collectively, these technologies are complementary tools in a powerful toolbox.

HEIDENHAIN and ETEL to Share Expertise at SEMICON West

Visitors to this July's SEMICON West 2019 trade show will have the rare opportunity to learn about "Where Accuracy Meets Throughput" at the HEIDENHAIN and ETEL joint show booth #831. Here, daily presentations will be given by HEIDENHAIN and ETEL experts highlighting this year's application focus of Fan-Out Wafer-Level Packaging. This trend demands both a high accuracy and high throughput motion system, especially at the wafer reconstitution process step.

Many state-of-the-art products will also be on display at the HEIDENHAIN/ETEL booth, including but not limited to HEIDENHAIN brands:

1. ETEL's TELICA motion system – TELICA (Figure 1) is ETEL's newly developed positioning platform dedicated to semiconductor back-end processes, as well as the electronics market. Soon to be available, this new system allows users to handle the requirements of next generation advanced packages with a placement accuracy in the µm range, over a working space of up to 870 x 800 mm (therefore compatible with large panels 720x 650), allowing very high duty cycles and throughput.

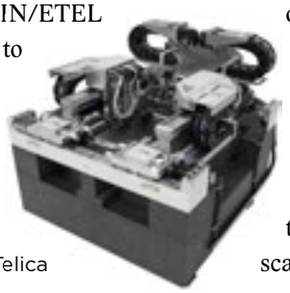


Figure 1. ETEL Telica

2. NUMERIK JENA LIKgo linear encoder – The LIKgo (Figure 2) is a newly designed low-cost linear install with generous mounting tolerances thanks to a new scanning technology that provides significantly improved signal quality. Measuring steps down to 78.125 nm are possible. Other advantages and benefits of this new LIKgo include a very small scanning head that weighs only 5 g.

Figure 2. NUMERIK JENA LIKgo

3. RSF MCR 15 encoder series – Another new product in the HEIDENHAIN corporate group product portfolio is the MCR 15 absolute modular angle encoder from RSF. Developed for dynamic applications in the semiconductor and electronics industries, this new angle encoder consists of a scanning head and a graduation flange. The MCR scanning heads are designed specifically for the available interfaces as well as for the graduation-flange outside diameters.

The short presentations will be given three times during each day (11 a.m., 1 p.m. and 3 p.m.) at their show booth #851 in the Moscone Center. You discuss these topics directly with the experts after each presentation.

Changes in the Advanced Packaging Supply Chain: Opportunity or Misfortune?

BY SANTOSH KUMAR AND MARIO IBRAHIM, YOLE DÉVELOPPEMENT

Amidst a dynamic ecosystem, the semiconductor supply chain is undergoing change at various levels (Figure 1). Some players have successfully managed to expand into a new business model and significantly impact the IC manufacturing chain, while others have failed to take off.

Different players have different motivations to move or expand into new businesses. Yole Développement (Yole) identified, for example, software players like Google, Microsoft, Facebook, and Alibaba. Such companies are designing their own processors in order to have system-level integration/ customization and control of the supply chain up to assembly level.

The biggest change is marked by foundries expanding into the advanced packaging business. Though they are relative newcomers, their impact has been significant.

TSMC leads for innovation in the fan-out and 3D advanced packaging platforms, with various offerings such as InFO (and its variants), CoWoS, WoW, 3D SoIC, and more. For TSMC, advanced packaging has become a full-fledged business, and the company expects US$3 billion revenue from its advanced packaging activities in 2019, which would put place them fourth among OSATs.

Figure 2. The top 25 OSATs in terms of revenue.

Elsewhere, UMC is a key supplier of Si interposers for 2.5D packaging, and recently partnered with Xperi to optimize and commercialize ZiBond and DBI technologies for a wide range of semiconductor devices. Meanwhile, XMC provides 3D IC TSV packaging for image sensors and high-performance applications. Overall, these players are instrumental in moving packaging from substrate to a silicon platform.

IC substrate and PCB manufacturers like SEMCO, Unimicron, AT&S, and Shinko are entering the advanced packaging arena with panel-level fan-out packages and embedded dies (and passives) in organic substrates, and are eating the lunch of OSATs – especially those involved in the advanced packaging business. EMS companies such as Foxconn, Jabil are developing assembly / packaging capabilities and are expanding into the OSAT's business domain to improve their profit margin and move up the value chain. Foxconn provide the RF SiP packaging services for Avago FEM and module assembly for various OEMs. Jabil acquired Kasalis which is the manufacturing system for the active alignment, assembly, and test of compact optoelectronic devices.

To remain competitive, lots of M&A will take place in the OSAT sector in the coming years, at various levels: consolidation amongst big players, the merger or acquisition of two midsize players with complementary services offerings (i.e. between pure packaging and testing players), and small OSATs (or WLP houses) being acquired by big players. Niche WLP players like Deca Technologies and LB Semicon are strong candidates for acquisition. Figure 2 shows the top 25 OSATs.

In addition, the trade tension between the U.S. and China could potentially disrupt semiconductor growth and cast uncertainty over the supply chain. The picture is still unclear and there is lots of confusion, intermingled with many "ifs" and "buts". Multiple scenarios are today possible depending on whether there is an all-out trade war or if a new trade deal is reached, either with concessions from each side or the status quo being maintained. It is also possible that this trade war will see assembly supply chains shifting from China to Taiwan, Korea, and Southeast Asia.

Figure 1. Amidst a dynamic ecosystem, the semiconductor supply chain is undergoing change at various levels.

Once the traditional domain of OSATs and IDMs, a paradigm shift is occurring today in the packaging/ assembly sphere. Players from different business models including foundries, substrate/PCB suppliers, EMS/DMs, are arriving and cannibalizing OSATs' share.

All in all, there is a lot of moves within the advanced packaging industry. Yole and its advanced packaging team, in collaboration with System Plus Consulting, specialized in reverse engineering & costing, will definitely keep a close eye on this industry and its impressive changes...

Santosh Kumar, Principal Analyst & Director, Packaging, Assembly & Substrates, Yole Korea, Mario Ibrahim, Technology & Market Analyst, Yole Développement, and Favier Shoo, Technology & Market Analyst, Yole Développement

EV Group Unveils New Maskless Exposure Technology

EV Group (EVG), a leading supplier of wafer bonding and lithography equipment for the MEMS, nanotechnology and semiconductor markets, recently unveiled MLE™ (Maskless Exposure), a revolutionary next-generation lithography technology developed to address future back-end lithography needs for advanced packaging, MEMS, biomedical and high-density printed circuit board (PCB) applications. The world's first highly scalable maskless lithography technology for high-volume manufacturing (HVM), MLE combines high-resolution patterning with high throughput and yield, while eliminating the significant overhead costs associated with photomasks, including mask management and maintenance infrastructure. Furthermore, MLE delivers unsurpassed flexibility to enable extremely short development cycles for new devices.

MLE technology accommodates any wafer size up to panels and supports all commercially available resists through a tightly integrated clustered write-head configuration and multi-wavelength high-power UV source. Throughput is independent of layout complexity and resolution, and MLE achieves the same patterning performance regardless of photoresist. MLE complements EVG's existing lithography systems, targeting new and emerging use cases where other approaches face scalability, cost-of-ownership (CoO) and other limitations.

EVG is now offering demonstrations of its MLE technology at the company's headquarters. MLE will be incorporated into a new line of EVG systems, which are currently in development and will be announced in due course.

"Our new MLE technology excels in back-end lithography applications, where other patterning technologies, such as steppers, have to compromise on performance or cost. No longer will customers need to choose between resolution, speed, flexibility or cost of ownership for their back-end patterning needs," stated Paul Lindner, executive technology director at EV Group. "Early development work with an exclusive range of customers has shown that the applications benefiting from MLE are wide ranging and growing in number. As we ramp up the development of this unique exposure technology into first products, we look forward to partnering with more companies across the industry to support new devices and applications that will benefit from MLE."

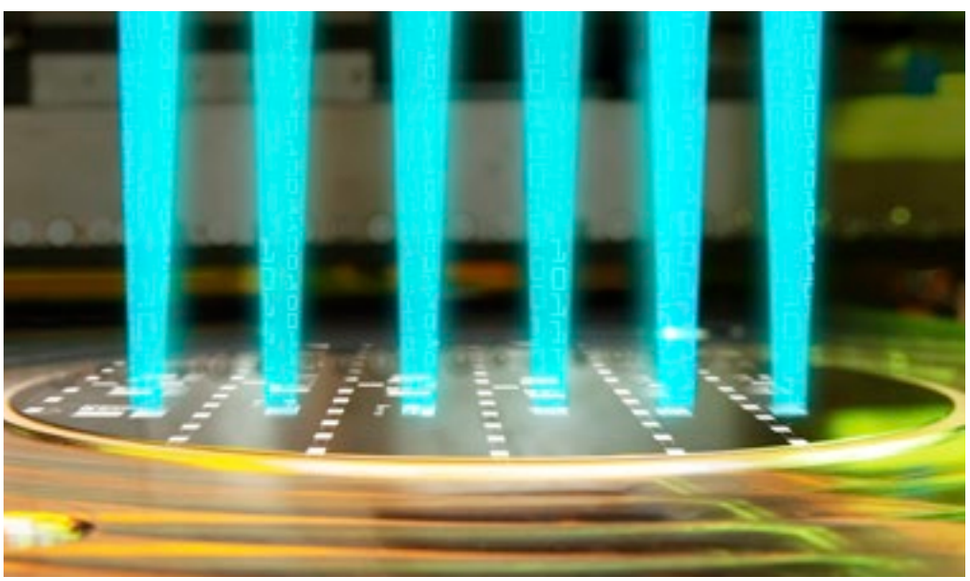
Back-end lithography faces new challenges

As heterogeneous integration becomes an increasing driving force in semiconductor development and innovation, impacting the advanced packaging, MEMS and PCB markets, backend lithography requirements are growing. In advanced packaging, for example, the minimum resolution requirements for redistribution layers (RDL) and interposers with their continuously denser lines/spaces (L/S) are becoming increasingly stringent. In some cases, they are approaching or exceeding two microns, while die placement variation and the use of cost-efficient organic substrates require more flexibility in patterning. The requirements for higher overlay accuracy as well as high depth of field in vertical sidewall patterning are also growing. New requirements, such as minimizing pattern distortion and die shift due to wafer distortion in fan-out wafer level packaging (FoWLP) and support for thick and thin resists, are just some of the criteria for existing and future advanced packaging lithography systems.

In MEMS manufacturing – with its complex product mix – mask/reticle overhead costs have a growing impact on CoO, while excellent focus control is critical for patterning in trenches. In the PCB and biomedical markets, demand is growing for a higher degree of pattern flexibility to address a wide range of both feature sizes and substrate sizes.

MLE technology detail

EVG's MLE technology enables high-resolution (<2 microns L/S), stitch-free maskless exposure of the entire substrate surface with high throughput and low CoO. The system scales according to user needs by adding or removing UV exposure heads – for facilitating rapid transition from R&D to HVM mode, for throughput optimization, or for adaptation to different substrate sizes and materials – and is ideal for processing a range of substrates from small silicon or compound semiconductor wafers up to panel sizes. MLE achieves the same patterning performance regardless of photoresist thanks to a flexible and scalable high-power UV laser source, which provides multiple wavelength exposure options.



EVG's new MLE™ technology provides unsurpassed flexibility, scalability and cost-of-ownership benefits compared to existing high-volume-manufacturing lithography methods.

Finding Marginal Semiconductor Wafer Defects

Final electrical test remains one of the best ways to assess a circuit's ultimate viability. But we know, unfortunately, that even 100% end-of-line electrical testing of semiconductor wafers will not guarantee that chips will not fail in the field. Certain non-killer but marginal wafer defects can still slip through electrical testing if they have sufficient electrical connectivity, even though it may be less than optimal. And over the longer term, chips like these can become reliability "time-bombs." In the end products, repeated thermal and electrical overstress can cause electromigration and push such circuits into failure.

Fortunately, there's another tool that can catch many of these latent defects. It's a way that can provide additional defect information, earlier in the process — using high-speed in-line macro defect inspection.

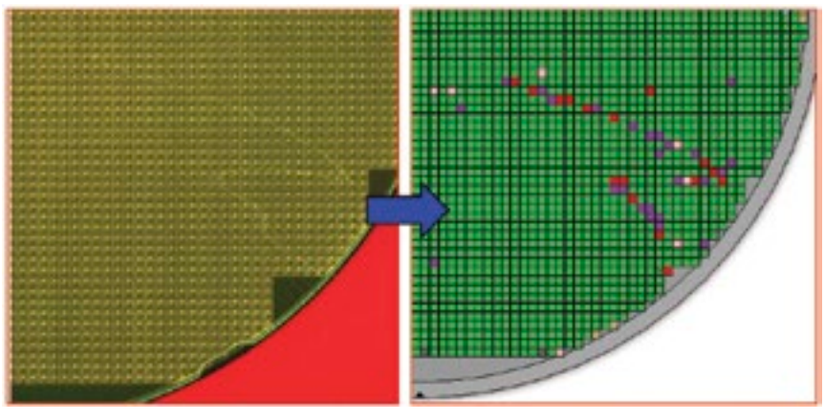


Figure 1. (L) This in-line semiconductor macro wafer inspection picture shows a common surface scratch – in a "Z" shape – on a wafer.

Figure 2. (R) The final electrical test result for the wafer shown in Fig. 1. Note that not all the die within the Z area failed

Good die may not all be equally good

Figure 1 is an in-line semiconductor macro wafer inspection picture showing a common surface scratch – in a "Z" shape – on a wafer. Now compare that with Figure 2, which shows the final electrical test result for the same wafer. You will notice that not all the die within the Z area failed. The electrical test seems to indicate that there are still a number of "good" (green) die within the Z pattern — even though we might reasonably suspect that additional die within that area could actually have been adversely affected by the scratch.

In Figures 3 and 4 we can see another example: Figure 3, from in-line semiconductor macro wafer inspection, clearly reveals a problem of inadequate photoresist coverage at the edge of the wafer. However, final electrical testing of the same wafer, shown in Figure 4, again reports fewer failed (non-green) die than might have been expected, given the extent of the photoresist issue.

So, as before, we might well suspect that at least some of those "good" die at the periphery of the failed areas may actually be compromised, at least to some degree.

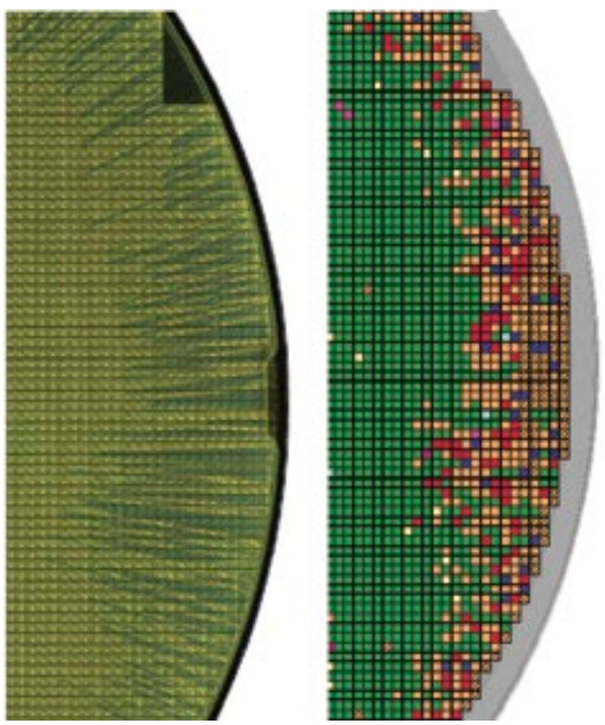


Figure 3. (L) This in-line semiconductor macro wafer inspection clearly reveals a problem of inadequate photoresist coverage at the edge of the wafer.

Figure 4. (R) Final electrical testing of the wafer shown in Figure 3 again reports fewer failed (non-green) die than might have been expected, given the extent of the photoresist issue.

More complete wafer defect information = improved yields and better inspections

Those are just two of the many "gray area" scenarios that allow marginal devices to get past electrical test and into customers' hands. In the examples shown above, final electrical testing did not have the benefit of the earlier macro wafer inspection information. Fortunately, however, today's ultra high-speed automated macro defect wafer inspection systems can automatically provide a wealth of additional defect data – to inform and improve every subsequent processing step and inspection. We'll talk more about that in a forthcoming issue of *Macro Intelligence*.

Ultra-fast full-wafer macro defect inspection – to complement micro sampling

Because of their ultra-high speed, today's macro defect inspection systems have become an essential complement to micro inspection. For example, the EagleView from Microtronic can provide fabs with full-wafer semiconductor macro inspection of all the wafers in the lot, without recipes – in just a few minutes! So there's no need for macro sampling.

This allows macro defect inspection to be used after many more process steps, to catch more problems earlier. Which means that fabs can take more specific corrective actions much sooner – to minimize scrap, increase yields, and reduce costs.

SEMI Americas and Semiconductor Digest Announce 2019 "Best of West" Award Finalists

Each year at SEMICON West, the "Best of West" awards are presented by SEMI and Semiconductor Digest. The award recognizes innovative new products or services that are significantly advancing the electronics manufacturing supply chain or a particular manufacturing capability.

Selected from over 500 exhibitors, Semiconductor Digest and SEMI announced that the following Best of West 2019 Finalists will be displaying their products on the show floor during Semicon West, July 8-10, 2019:

CyberOptics: NanoResolution MRS Sensor

Proprietary MRS sensor technology, deemed best-in-class, enables metrology grade accuracy by inhibiting optical measurement distortions and reflections. CyberOptics' unique sensor architecture simultaneously captures and transmits multiple images in parallel while proprietary 3D fusing algorithms merge the images together. The result is ultra-high quality 3D images and high-speed inspection.

Advantest: V93000 Wave Scale Millimeter Solution

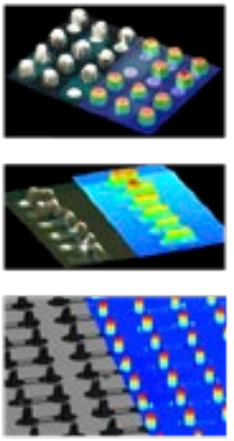
The dawning of 5G and 5G-NR (new radio) ICs requires test equipment to handle millimeter-wave (mmWave) frequencies. Advantest's scalable V93000 Wave Scale™ RF solution has been extended to support multi-band testing at the fast interface speeds used by 5G devices, making it the industry's first fully integrated, multi-site mmWave ATE test solution.

Edwards: Atlas System

Edwards' innovative porous head/slot nozzle technology, combined with its unique inward fired combustor, is designed to manage PFC abatement and high flow flammable process gas in the pump exhausts. In addition, when embedded into Edwards' sub-fab integrated solution it reduces customer risk and improves customers' uptime.

Congratulations to each of the Finalists. The Best of West Award winner will be announced during SEMICON West on Wednesday, July 10, 2019.

Advantest's V9300 Wave Scale Millimeter Solution



CyberOptics' Nanoresolution MRS Sensor

Edwards' Atlas PFC abatement system

IMPROVING YOUR YIELD

AIRBORNE PARTICLE COUNTERS

Yield

Cost
Waste
Risk

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