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JULY 10, 2019
WEDNESDAY

CEO Panel Tackles the Future of Moore's Law Question

BY PETE SINGER

CEO panel, left to right: Aart de Geus, Synopsys; Victor Peng, Xilinx; Lisa Su, AMD; Sanjay Mehrotra, Micron, Gary Dickerson, Applied Materials, and moderator/journalist John Markoff.

On Tuesday morning, Applied Materials hosted a CEO panel discussion with Aart de Geus, PhD, Chairman and co-Chief Executive Officer, Synopsys; Victor Peng, President and CEO, Xilinx; Lisa Su, PhD, President and CEO, AMD; Sanjay Mehrotra, President and CEO, Micron; and Gary Dickerson, President and CEO, Applied Materials. John Markoff, author and former technology writer with The New York Times acted as moderator.

Markoff had some great questions for the panel related to cost per transistor, new materials, life after CMOS, potential surprise technologies, quantum computing, AI and new architectures – but his first question was perhaps the most controversial: "Is Moore's Law dead or alive?" The panel's mixed response was illuminating:

Art de Geus, Synopsys: It's completely alive. The discussion on Moore's Law invariably goes

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DON'T MISS

9:05 am -9:35 am
Ten Global Trends Shaping the Future of Media and Technology
Blue Shield of California Theater at YBCA

9:35 am – 10:05 am
The Future of Computing: Bits + Neurons + Qbits
Blue Shield of California Theater at YBCA

9:50 am -10:50 am
Advanced Packaging – It's Changing the World of Wafer Test
Moscone North, Hall E, Room 21

10:20 am – 10:50 am
KEYNOTE: The Need for a Quantum Leap in Human Organ Biofabrication
Blue Shield of California Theater at YBCA

12:05 pm – 12:35 pm
Heterogeneous Integration Roadmap Update
TechTALK North

1:30 pm – 4:30 pm
Advanced Processing Tools and Manufacturing
Meet the Experts Theater, SMART MedTech

SEMI Releases 2019 Mid-Year Total Equipment Forecast

Global sales of semiconductor manufacturing equipment by original equipment manufacturers are projected to drop 18.4 percent to $52.7 billion in 2019 from last year's historic high of $64.5 billion, SEMI, the global industry association representing the electronics manufacturing and design supply chain, reported today in its Mid-Year Total Equipment Forecast. However, it is still the industry's third best year ever, said SEMI Americas President Dave Anderson during a press conference yesterday.

Released this week at SEMICON West, the forecast shows growth in equipment sales resuming in 2020, with an 11.6 percent jump to $58.8 billion. The current forecast reflects recent downward adjustments in capital expenditures and rising market uncertainty due in part to geopolitical tensions.

The SEMI Mid-Year Forecast shows wafer processing equipment sales falling 19.1 per-

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CEO Panel cont'd from p 1

back to the '65 document and then people will exactly track where are the economics, where's the technology? That's not the way to think about it. I think the way to think about it is Moore's Law is the behavior of an exponential that had taken economic feedback on the exponential that drove a revolution of what mankind can do. And the reason I'm saying is completely alive is because right now we're facing another decade or two of amazing opportunities that themselves economically will drive the push for technology. Maybe it's not exactly the same kind of curve that Moore actually drew, it doesn't matter. The impact is what matters of the exponential.

Victor Peng, Xilinx: Of course, I have to say the opposite. It's mostly dead. 'Not quite dead yet' as the saying goes. I'm not saying that there won't be still quite significant improvements in computing, but it's going to take a very different form. I'll talk about Moore's law in a general sense, where if you take any processor and in every two years you move move it to the next node and you don't change the architecture, the performance, power and the area will get, we could get better, which is sort of good for cost. Today, you can get definitely you get one, you can get to pick which one you want.., but it's really hard to get all three. In that more traditional sense of Moore's law, I think that's not going to be working. On top of that, it's been said for a long time, this happens every two

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Show Daily Staff

Published by Semiconductor Digest, a property of Gold Flag Media LLC, Andover, MA.

GOLD FLAG MEDIA LLC

Kerry Hoffman
Publisher
kerryh@semiconductordigest.com

Ed Korczynski
Senior Technical Editor
edk@semiconductordigest.com

Pete Singer
Editor-in-Chief
psinger@semiconductordigest.com

Dave Lammers
Contributing Editor
dplammers@att.net

Shannon Davis
Web Editor
sdavis@semiconductordigest.com

Dick James
Contributing Editor
dickjames@siliconics.ca

TRADESHOW MEDIA PARTNERS

Mark Larson
Production and Printing
mark@tsmpartners.com

Kevin Clarke
Layout and Design
kevin@tsmpartners.com

SEMI Smart Manufacturing Initiative Releases New Industry Benchmark Survey

The SEMI Smart Manufacturing Initiative today released the semiconductor industry's first Benchmark Survey to assess the current implementation level of automation and control measures aimed at increasing productivity and efficiency in front-end semiconductor fabs. Also designed to gauge the readiness of respondents to implement further smart manufacturing measures, the survey was distributed to more than 5,000 contacts across 200 companies that manage device fabrication facilities. The deadline for completing and returning the survey is July 26.

The Benchmark Survey will help participating members assess where their facilities fall on the smart manufacturing implementation curve using methodologies defined in the Overall Equipment Efficiency (OEE) SEMI Standard as a guide. Fab implementation of the technologies will be categorized by speed, output and quality – all top-level metrics of factory efficiency.

The team SEMI assembled to develop this groundbreaking Benchmark Survey consists of major industry players with deep expertise in factory automation

ARIEL MEYUHAS,
COO OF MAX INTERNATIONAL ENGINEERING GROUP

The benchmark project

The survey was created by subject matter experts from the Americas Chapter of the SEMI Smart Manufacturing Technology Community. Member companies include Intel, Applied Materials, EMD Performance Materials, MAX International Engineering Group, Cimetrix, Jabil and SUNY Polytechnic Institute. The group collaborated with Advanced Focus, a provider of services to improve manufacturing performance. Focusing on front-end semiconductor processing, the benchmark will later be extended to include the assembly, test, surface-mount and printed circuit board assembling sectors of the electronics industry.

"This survey benchmarks the current level of adoption and implementation of smart manufacturing technologies in the fab and how it affects manufacturing efficiency," said Zsolt Marcet, supply chain engineer at Intel and current co-chair of the Benchmark Survey team. "It will give valuable insights into the industry as a whole in understanding the role of smart manufacturing."

"OEE provides an effective metric of how a fab is performing in the transition to smart manufacturing," said Dinesh Saigal, senior manager at Applied Materials and also co-chair of the Benchmark Survey team.

"This study is unprecedented in demonstrating how smart manufacturing is a differentiator in factory performance," said Ariel Meyuhas, COO of MAX International Engineering Group and a Benchmark Survey team member. "It will give participants an excellent view of what peers are doing to improve fab efficiency and competitiveness using smart manufacturing metrics."

"The team SEMI assembled to develop this groundbreaking Benchmark Survey consists of major industry players with deep expertise in factory automation," said Tom Salmon, vice president of Collaborative Technology Platforms at SEMI and leader of the Smart Manufacturing Initiative. "We look forward to leveraging the survey results to design best practices and guidelines across the electronics manufacturing supply chain and drive the adoption of AI, ML and predictive analytic solutions that fulfill the promise of smart manufacturing."

IDMs or foundries interested in completing the survey can click here to request a link.

The Smart Manufacturing Pavilion is among the theme pavilions featured at SEMICON West, July 9-11 at the Moscone Center in San Francisco.

Particle Counts Increasing in Importance

As geometries shrink and chips move into taller 3D structures, both semiconductor process reactant flows and by-products are increasing. This poses several new challenges that the tool's vacuum system must handle, one of these being the management of increased particle generation rates. Furthermore, as critical dimensions shrink, the impact of particles on the wafer becomes more significant and detrimental. As a result, acceptable particle size and counts per wafer are becoming smaller and smaller.

"Particle counts are affecting both the wafer yield and tool uptime more today than ever," claimed Dawn Stephenson, Business Development Manager – Chamber Solutions at Edwards Vacuum. "What we find is that tool maintenance cycles now are no longer determined by component failures. They are really determined by particle counts. Particle contamination is becoming much more important to both the tool manufacturer and the end user."

There are multiple sources of chamber particles, including:

1. particles formed in the process chamber and either removed by the turbomolecular pump (TMP) or recoiled from the TMP back into the chamber,
2. by-product deposition formed or collected on the throttling gate valve (TGV) and potentially vibrated back into the chamber or transported into the TMP,
3. by-product deposition formed in the TMP and back-streamed into the chamber.

To prevent deposition from forming in the TMP and becoming a potential particle source, any condensable by-products (such as NH_4Cl, $AlCl_3$) must be kept in the vapor phase by reducing the partial pressure or increasing the temperature of the gas path.

"We've looked at different ways you can optimize the thermal platform of the pump to maintain temperatures all through the gas path above 150°C to help minimize deposition, which typically occurs in the higher-pressure regions of the pump," Stephenson said. "That's been successful in improving tool uptime and now we're looking into different materials of construction that can withstand 200°C or even higher."

Tool maintenance cycles now are no longer determined by component failures. They are really determined by particle counts. Particle contamination is becoming much more important to both the tool manufacturer and the end user.
DAWN STEPHENSON, EDWARDS VACUUM

When it comes to particles formed in the chamber or on the TGV, Stephenson notes, "As a company, we've done a lot of work in simulating particle movement from the chamber into the turbo pump and understanding what percentage of these particles are recoiled back." Their modeling showed that a significant percentage of particles do deflect back from the first or second blade stages of the turbo pump depending on where they strike the blade. "The particles that hit on the blade edges are much more likely to be recoiled back into the chamber, than pumped all the way through the turbo," Stephenson said. This is shown in Figure 1.

Edwards have tested alternative turbopump designs to determine if particle recoil rate back to the chamber can be reduced. The testing is done by dropping individual particles onto a spinning TMP and collecting the amount that recoiled. "We've done our own in-house testing to validate our simulation and modeling by sprinkling particles into the turbo pump and measuring those that are returned back into the chamber," Stephenson. Field tests are also underway at leading semiconductor and display manufacturers on tools from leading suppliers.

The result: A new approach that Edwards has dubbed ART, or Anti-Recoil Technology, reduces the number of particles deflected back into the process chamber, without compromising the effective pumping speed.

"There are a lot of different factors that would affect this and we understand that it is very process dependent, but have shown that, with modification to the turbopumps, you can reduce the particles that are recoiled back by up to 65%, depending on the gas flow," Stephenson said. See "Innovative Approaches to Vacuum Enable High-Volume Atomic Layer Processing," in the July issue of Semiconductor Digest, pg. 26, for more information.

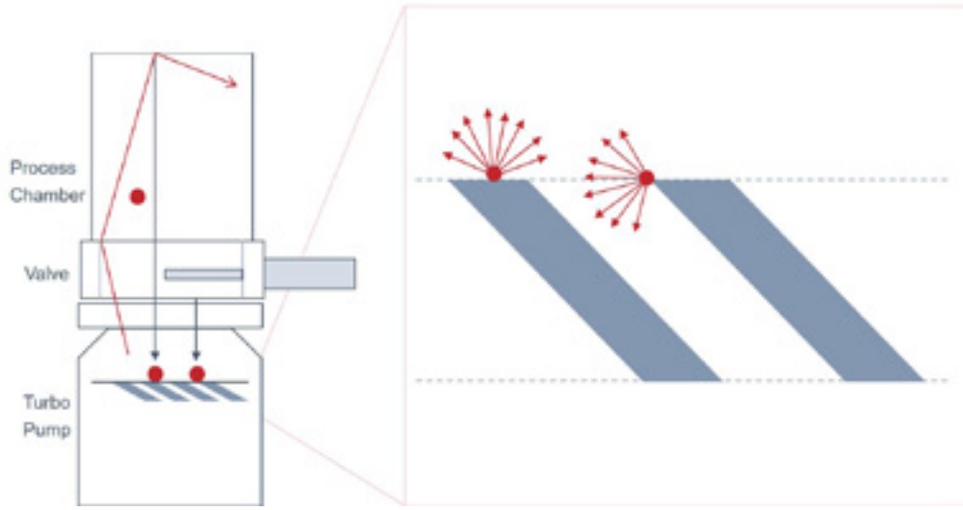

Figure 1. Particle recoil in a vacuum process chamber.

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No recipes required. Just load and go.

EagleView accepts four cassettes, with 100mm to 300mm wafers. And no recipes are needed. It's totally plug-and-play. So you can eliminate all the time, hassle and special staff to generate and maintain recipes. With full automation, virtually anyone in your fab can use it anytime.

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Because it sees every wafer, EagleView can catch a lot more defects. And, it gives you smarter ways to track down root causes. At the start of each run, the fab's host automation system sends the lot's tool history to EagleView, where that gets integrated with the wafer image data. So when you spot a defect you can easily drill down to see which particular process tool was the likely culprit.

Spot onesie-twosies. Stop excursions.

EagleView's 100% inspection catches even those elusive one-time problems. Spotting them sooner often lets you rework wafers rather than having to scrap them later on. And correcting excursion problems earlier helps improve fab performance overall. Plus, EagleView's special guardbanding capability can clearly ink-off problem areas on wafers so they won't cause surprises down the line.

Wafer randomization for free.

While EagleView is inspecting wafers it can also randomize or sort them. Automatically. While maintaining full speed. So, if you want to do slot position analysis you won't need to buy extra sorters. And you won't need special IT efforts to create usable databases.

Machine vision: better, more consistent data.

EagleView removes all the variables of human optical inspection. Its defect data recording is consistent and complete. Every shift. Every day.

Information for all.

There are no licenses restricting how many stations can use EagleView wafer data. Everyone can access it. Throughout your fab or enterprise, around the world. No extra charge.

Higher yields. Lowest CoO.

EagleView needs no consumables, and maintenance is so minimal, customers can do it themselves. Plus, you can save all those resources you used to spend on recipes. And get guardbanding ink-off virtually free. Bottom-line: EagleView has the lowest CoO of any tool in its class.

Have it your way. We do customization.

Maybe you work with silicon carbide or other transparent wafers. Or you need OCR to convert vendor scribes to lot IDs. Or wafers split to double-spaced cassettes. Or custom slot positions. Just tell us what you need!

EagleView: popular and proven.

These powerful tools have already inspected over 300 million wafers and they're boosting yields around the world. Perhaps EagleView could be helping <u>your</u> fab. Why not set up a demo and see for yourself!

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2019 Rare Earths Rarely So Strategic

BY TERRY A. FRANCIS, DIRECTOR OF TECHNOLOGY & SENIOR ANALYST, TECHCET

Global supply-chains are being disrupted by the U.S./China trade wars, driving increased awareness of the strategic importance of rare-earth elements (REE). China currently controls the global market for these critical materials with over 79% share of the world's mined production, and currently holding approximately 37% of the world's REE reserves. China has recently reduced rare-earth oxide (REO) production by 30%. REEs are vital building-blocks for batteries, catalysts, lasers, magnets, emerging memory devices, and other high-value components of the modern world. In the recent past, U.S. companies were happy to pay reduced prices for REE from China such that U.S. production shut down, and the remaining mining in the U.S. now ships ore concentrate to China for refining.

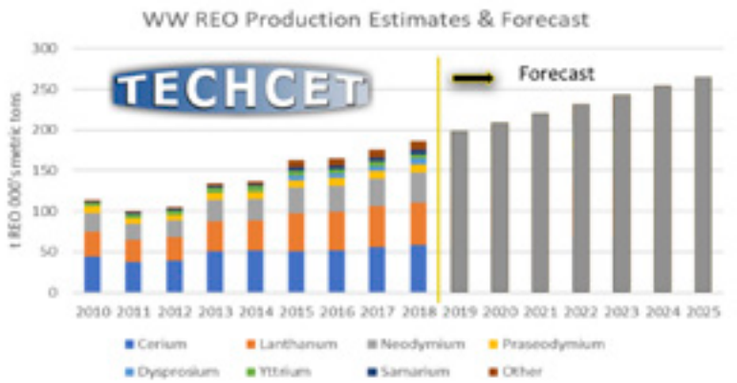

Figure 1. Rare-Earth Oxide (REO) production estimates and forecasts of critical elements needed to meet world-wide demand over the period 2010-2025. (Source: TECHCET).

REE are heavy metals distributed in moderate quantities around the world. The name is really a misnomer because REE are not very rare in the earth, and are found in over 300 known mineral rocks at an average concentration of 150-220 ppm (compared to copper at 55 ppm). Finding and mining of REE is not difficult, but their chemical properties make them extremely difficult to separate into individual elements. A mix of dilute REO must be concentrated, and then reacted with acids and bases to separate out the individual pure oxides under strict process and EHS controls.

Research into REE alternatives has so far found no other materials capable of providing equal performance, despite government funding in Japan, Europe, and the US (DARPA's "React"). Demand for batteries for electric vehicles and other products that use REE soared to 130 million tons last year. TECHCET sees strong global demand growth for several REE, such as neodymium, praseodymium, dysprosium, and lanthanum (Figure 1).

Weak consumption lowered prices of rare earth in the third quarter of 2018, and prices fell for praseodymium, neodymium, terbium, and dysprosium. We anticipate prices of most rare earth products will rise over the next few years. This will help the supply-chain reach pricing levels that will sustain the profitability and growth of the dominant producers, while also incentivizing continued global investments in exploration and resource development.

Global supply

China dominates REE production, and so has direct and indirect control over pricing. China has a majority ownership of mines inside the country and has made direct investments in external mines or in the outtake of these mines. TECHCET has identified 62 global REE mining locations, but after thorough analysis considers only 28 mines as having shown activity or potential of producing REO in the next 3-5 years (2021-2026). Outside of China, the largest sources of REO mining and production are located in Australia, Russia, Vietnam, and India. Canada has a large potential reserve with multiple companies, but the capacity has not been developed, and many companies still ship ore to china for refining and purification.

The challenges in securing a fair, binding purchase agreement for REE is not unique to REO sales. Potential purchasers continue to buy predominantly from China and, whilst they are interested in establishing a non-Chinese supply-chain to diversify their supply risk, they also expect new entrants to supply at a substantial discount to the established Chinese suppliers (Figure 2). Companies need to be well positioned with a low-risk, permitted and "development ready" project, and not bound to an inferior pricing position for many years.

Tariff strategies likely ineffective

Since REE production in the U.S. is not at industrial quantities, a tariff on raw REE would increase the cost in the U.S. with the intent to create profitable local production. This action has two issues: the cost of building capacity, and the low market prices. An existing mine, like Mountain Pass in California, required a half-billion dollars to begin operations. Russia recently invested one billion dollars to start a new REE mine.

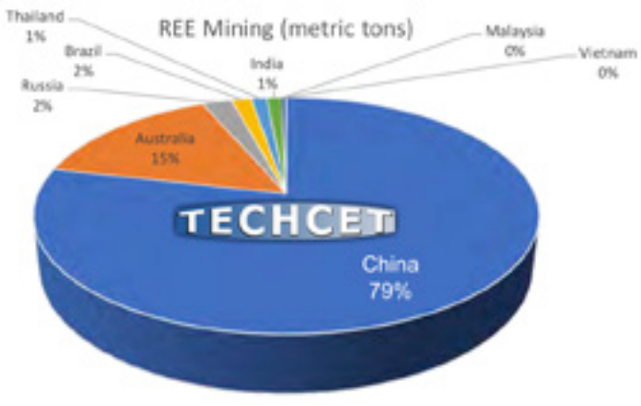

Figure 2: 2018 Estimated mining supply of Rare Earth Elements (REE) by country, showing that China currently dominates the supply-chain with 79% share of the market. (Source: TECHCET).

The second issue of low market prices is connected to China's strategic investments over the last 20 years in refining and separation technologies. Chinese companies are now more efficient than international competitors and can make profits while offering low prices.

CEO Panel cont'd from p 3

years, I think clearly the cadence for when the next node comes, it's taking longer than two years for a variety of reasons, as much economic as technical.

Lisa Su, AMD: John and I were talking this morning about we all used to do. I grew up as a process technologist, so I can't say Moore's law is dead, right? It just can't be (laughter). I think Moore's law is slowing, but it's something that we all strive to in terms of how do we get more performance for our products. There are lots of things that you can do in addition to process technology to keep that performance trend going. That's what we're all trying to do, whether it's in hardware or software or systems. That's the key: how do we keep that performance trend for our industry that's driving all of the applications going and there's a tremendous amount of effort to augment Moore's law

Sanjay Mehrotra, Micron: For almost a decade, Moore's law has slowed down significantly and actually has been less relevant. A lot of innovations have been living in memory and technology, for example, going from 2D NAND to 3D NAND. That has given capability to bring down costs as well as gain more gigabits per wafer. However, in DRAM, certainly a lot of innovation is happening with high bandwidth memory, stacking of vertical chips and TSV technologies to gain performance and to get the benefit of higher capacities. But there is no question that Moore's Law is significantly challenged in memory and storage. If you just look at 10 years ago versus today, what's happening in NAND as well as in DRAM, year-over-year, year bit growth that you could get from one technology transition to the next technology transition has more than halved now. Certainly, there are challenges. However, engineers are always finding new innovative ways to address memory and technology challenges better from a process point of view or design point of view and architecture point.

The challenges are significant, but there's tremendous opportunity not looking backwards, at classic Moore's law 2D scaling, but looking forward with these five year drivers in this new playbook.

GARY DICKERSON, APPLIED MATERIALS

Gary Dickerson, Applied Materials: With classic Moore's law, when you think about shrinking in two dimensions, Victor is cor-

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KLA Announces New Defect Inspection and Review Portfolio

On Tuesday, KLA Corp. announced the 392x and 295x optical defect inspection systems and the eDR7380™ e-beam defect review system. The new inspection systems are extensions of the company's flagship patterned wafer platforms, featuring advancements in the speed and sensitivity that define optical inspection. The new e-beam review system introduces innovations that cement its value as the essential link between defect and source. This portfolio is designed to accelerate time-to-market for leading-edge 3D NAND, DRAM and logic integrated circuits (ICs) throughout their product lifecycle.

KLA's new 392x and 295x optical inspection systems and eDR7380 e-beam review system support detection, identification and sourcing of critical defects for advanced logic, DRAM and 3D NAND devices.

"Manufacturing the next generation of memory and logic chips profitably requires unprecedented process control," said Ahmad Khan, executive vice president of the Global Products Group at KLA. "Device structures are smaller, narrower, taller and deeper, with more complex shapes and new materials. Discriminating defects from benign physical variations—signal from noise—has become an incredibly difficult problem. I'm excited to announce that our optical and e-beam engineering teams have developed a family of innovative, connected defect inspection and review systems, designed to enable our industry to continue to move forward."

The 392x and 295x optical patterned wafer defect inspection systems achieve unparalleled levels of sensitivity, throughput and yield-relevant binning by leveraging substantial advances in broadband plasma illumination technology, sensor architecture and integration of chip design information. As a result, the new systems provide faster defect discovery, accelerated yield learning, and more comprehensive inline monitoring than their industry-leading predecessors. The 392x and 295x systems use different wavelength ranges to cover inspection applications for all layers, from shallow trench isolation through metallization, including EUV lithography quality control.

With best-in-class image quality and the unique ability to deliver a complete defect pareto in one test, the eDR7380 e-beam wafer defect review system provides faster defect sourcing in development, faster excursion detection, and more accurate, actionable data during production. The system is equipped to support review of fragile EUV lithography process layers. Unique linkage to KLA inspectors reduces time to results, enables access to a broad range of KLA-specific applications, and improves inspection sensitivity through smart sampling and efficient exchange of defect data.

The 392x, 295x and eDR7380 systems are available as new systems or as upgrades from previous-generation 39xx, 29xx or eDR7xxx systems. These systems are designed for future extendibility to protect a fab's capital investment.

All of the new systems are in operation at leading IC manufacturers worldwide, where they work together to make innovative electronic devices manufacturable. To maintain the high performance and productivity demanded by chip manufacturers, the 392x, 295x and eDR7380 systems are backed by KLA's global comprehensive service network.

KLA's new 392x and 295x optical inspection systems and eDR7380 e-beam review system support detection, identification and sourcing of critical defects for advanced logic, DRAM and 3D NAND devices.

Mid-Year Forecast cont'd from p 1

cent in 2019 to $42.2 billion. The other front-end segment, consisting of fab facilities equipment, wafer manufacturing, and mask/reticle equipment, is expected to slide 4.2 percent to $2.6 billion this year. The assembly and packaging equipment segment is on track to decline 22.6 percent to $3.1 billion in 2019, while semiconductor test equipment is forecast to decrease 16.4 percent to $4.7 billion this year.

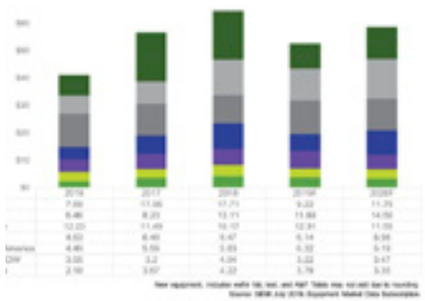

Figure 1. The SEMI Mid-Year Forecast shows wafer processing equipment sales falling 19.1 percent in 2019 to $42.2 billion, but it will still be the industry's third best year ever. Results are in terms of the market size in billions of U.S. dollars.

Taiwan will dethrone Korea as the largest equipment market and lead the world with 21.1 percent growth this year, followed by North America with an 8.4 percent uptick. China will maintain the second spot for the second consecutive year, and Korea will fall to third after throttling back capital expenditures. All regions tracked except Taiwan and North America will contract this year.

SEMI forecasts that, in 2020, the equipment market is expected to recover on the strength of memory spending and new projects in China. Equipment sales in Japan will surge 46.4 percent to $9.0 billion. China, Korea, and Taiwan are forecast to remain the top three markets next year, with China rising to the top for the first time. Korea is forecast to become the second largest market at $11.7 billion, while Taiwan is expected to reach $11.5 billion in equipment sales. More upside is likely if the macroeconomy improves and trade tensions subside in 2020.

ULVAC Names New Senior Management for North American subsidiary, ULVAC Technologies, Inc.

ULVAC Technologies, Inc. has announced that Dr. Koukou Suu, of ULVAC Japan, will serve as the new CEO of ULVAC's North American subsidiary, ULVAC Technologies, Inc., based in Methuen, MA. Dr. Suu, will replace incumbent President/CEO, Wayne Anderson, who will serve as Senior Advisor, to assist in the senior executive and operations transition. Dr. Suu, joined ULVAC, Inc. in 1993 and since then has been leading and engaging with developments of numerous semiconductor and electronics emerging technologies. He was the General Manager of ULVAC's Institute of Semiconductor and Electronics Technologies (2008-2014) and prior to assuming the role of CEO of ULVAC Technologies, was named an ULVAC Fellow and General Manager of Global Market & Technology Strategy for the company.

ULVAC Technologies, Inc. is also pleased to announce that also effective this date, Dave Sackett has been promoted to the position of CFO. Dave began his career with ULVAC in 1999, and has been responsible for the Finance, HR, IT and Materials departments, and now has the responsibility to manage Corporate Governance.

Dr. Koukou Suu, CEO of ULVAC

Dave Sackett, CFO of ULVAC

ULVAC, Inc. is an international corporation, which has been in business for 67 years. ULVAC designs and manufactures systems, equipment and materials for the industrial and research applications of vacuum technology. UVAC's systems cover a very broad spectrum of markets. In North America, ULVAC Technologies, Inc. has been long-established in Methuen, MA. This facility houses: sales & business development, customer service support, engineering, domestic manufacturing, a fully equipped applications lab, and an etch foundry services, operation.

Increasing Semiconductor Device Reliability Requires Adding More Wafer Inspection

Some industry sectors such as automotive and medical continue to push for higher and higher reliability levels; however, many fabs are having difficulties achieving them. Current inspection regimes still allow too many defects to pass through and escape to the field – primarily because of time and expense issues.

One fundamental problem is the amount of wafer real estate that is currently going uninspected. Even though much inspection is being done, still, the total inspected area remains small compared to the cumulative wafer surface passing through production (see comparison chart in Figure 1).

Today, fabs employ several different types of inspections, each playing a special role in the overall defect management program. But now, if additional wafer inspection is needed, what specific types of inspection should be increased, and where? And can this be accomplished without dramatically impacting budgets and production schedules?

Automated micro inspection

These are the "big guns" in many fabs' defect inspection arsenal today. The automated, highly advanced micro inspection tools are able to detect extremely small defects, below

1µm, and they are essential for catching today's ever-shrinking killer defects. However, these tools are costly, require device-dependent recipes and are comparatively slow, with throughputs of ~175 wafers per day.

Automated micro inspection tools are used in line, but only to limited degree – at a handful of key production steps, typically sampling two wafers from the lot. Though it might be desirable to add more automated micro inspections at many more steps, that is generally not feasible either from a cost or production time standpoint.

Comparison of Cumulative Wafer Surface Inspected

	Manual Microscope	Automated Micro Insp.	Automated Mid-Micro Insp.	Automated Macro Insp.
Number of Tools	5	2	2	1
Insertion Points	30	6	1	6
Throughput	~720 wafers/day	~175 wafers/day	~600 wafers/day	>3000 wafers/day
Standardized Defect Reporting	No	Yes	Yes	Yes
% of Cumulative Wafer Surface Inspected	0.32%	6.40%	13.33%	79.96%

Figure 1. The total inspected area remains small compared to the cumulative wafer surface passing through production.

Automated mid-micro inspection

These tools are similar to the micro inspection tools, except with lower magnification. The mid-micro tools also require device-dependent recipes to perform die-to-die inspection, and they will detect defects down to ~10µm. They provide higher throughput (~600 wafers per day) and are lower in price, but they are still expensive enough for fabs to limit their use to the end of line. These tools are frequently used for outgoing inspection of bond pads, probe marks, etc.

Manual microscope inspection

Optical microscopes are used for post photo or post CMP inspection. A typical fab might employ microscopes to sample five wafers from a lot – looking at five sites on each of the five wafers.

Optical microscopes are used for many types of defects very effectively and provide much useful information. These instruments can be applied to study features and defects

smaller than 1µm. However, the quality of this inspection can vary substantially with the experience and alertness of human operators. Also, these inherently subjective inspections do not generate standardized or comprehensive reporting that can be used fab-wide. And fundamentally, microscope inspection remains a sampling method, not well suited to covering the substantial amount of additional wafer surface we need to inspect.

Naked-Eye and bright-light inspection

It should be noted that some fabs still use some form of human-eye inspection, using it to look at every wafer in every lot. This method serves a useful purpose in spotting gross or obvious problems on wafer surfaces. Like microscope inspection, however, it is inherently subjective, and its value can vary greatly with the knowledge and experience of the viewer. It, too, does not generate any standardized reporting or record-keeping for the fab.

So, what additional wafer inspection can be added?

Automated macro inspection – opening new possibilities

This is a newer generation of automated wafer inspection tools that fits between the automated micro and mid-micro tools and the non-automated human inspection methods

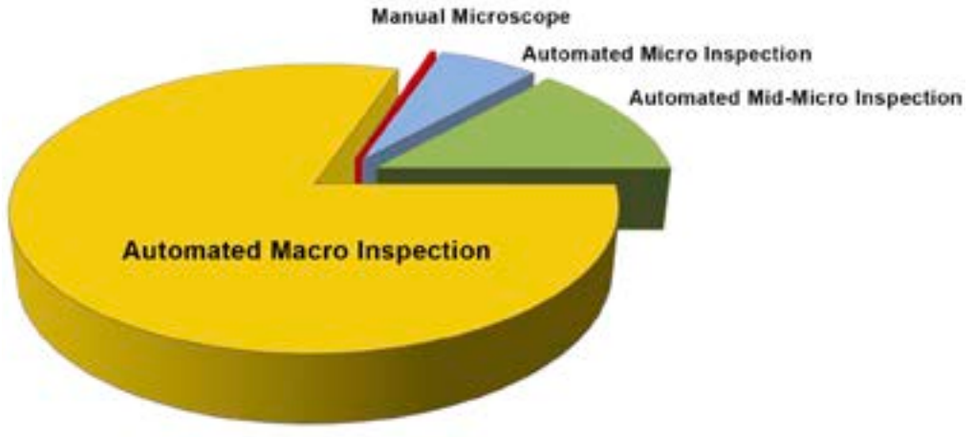

Figure 2. Automated wafer inspection tools fit between the automated micro and mid-micro tools and the non-automated human inspection methods

(Figure 2). These automated macro defect inspection tools, such as the EagleView from Microtronic, do not require recipes, and they are extremely fast – capable of throughputs of over 3000 wafers per day. Plus, they create a unique, high-resolution color image of the entire surface of every wafer in the lot.

This accomplishes three things: First, it substantially increases the total wafer surface area inspected during production. Second, it allows fabs to precisely identify types and

locations of a wide range of macro surface defects. Third, it provides a consistent, detailed and permanent record of every wafer in the lot at many important steps in processing. Plus, the macro information provided by these automated tools can be combined with micro defect data to create a powerful, comprehensive defectivity database for use by the entire fab at any time, now and in the future.

Covering much more wafer surface at many more steps

Specifically designed to cover a great deal of wafer real estate rapidly and cost-effectively, these new tools can be used to look at all the wafers at many more in-line production steps. A single automated macro inspection tool, for example, could be used for 100% inspection at many photo and/or CMP levels.

The net result of adding automated macro inspection can be a huge increase in wafer surface coverage compared with what was possible with previous tools alone – which can enhance defect detection levels and reliability overall.

The chart below compares typical amounts of wafer surface that might be seen by different defect inspection tools in a fab running 200mm wafers, 500 wafer starts per day, 300 process steps, and 30 mask levels.

Improving inline performance, as well

Adding 100% macro defect inspection in-line can alert fabs to process excursions and intermittent problems (onesie-twosie's) immediately, allowing faster, more accurate, and much more cost-effective corrective actions to be taken – without waiting for backend inspection or electrical probe results, which can be much more costly and ineffective for correcting in-line problems.

Bottom line, for many fabs automated macro inspection tools can be useful, comparatively easy to implement, and a cost-efficient way to look at much more wafer surface that has been going uninspected.

Applied Materials to Acquire Kokusai Electric

Applied Materials, Inc. announced a definitive agreement under which Applied will acquire all outstanding shares of Kokusai Electric Corporation for $2.2 billion in cash from global investment firm KKR.

Kokusai Electric is a leading company in providing high-productivity batch processing systems and services for memory, foundry and logic customers. These systems complement Applied's leadership portfolio in single-wafer processing systems. Kokusai Electric has strong customer relationships, world-class supply chain and manufacturing capabilities in Japan and Asia, and a talented team of employees.

Following the close of the transaction, Kokusai Electric will operate as a business unit of Applied's Semiconductor Products Group and continue to be based in Tokyo, with technology and manufacturing centers in Toyama, Japan and Cheonan, Korea. The acquisition is expected to be immediately accretive to Applied's non-GAAP earnings per share at close.

The transaction has been approved by the Applied Materials Board of Directors. The transaction is expected to close within approximately 12 months and is subject to regulatory approvals and other customary closing conditions.

"Kokusai Electric has a strong culture of innovation along with excellent customer relationships and serves fast-growing areas of the wafer fab equipment market," said Gary Dickerson, president and CEO of Applied Materials. "By bringing Kokusai Electric's talented team into Applied, we believe we will accelerate innovation for customers and create significant value for our shareholders."

"The opportunity to combine with Applied Materials will be very attractive for Kokusai Electric's customers and employees alike," said Fumiyuki Kanai, president and CEO of Kokusai Electric. "We are excited about the opportunity to integrate Kokusai Electric's experienced team with Applied's global development, customer support and services capabilities. We believe the combination will accelerate our ability to bring exciting new technologies to customers."

How the MEMS Market Is Holding Up in a Gloomy Economy

BY ERIC MOUNIER, PHD. AND DIMITRIOS DAMIANOS, YOLE DÉVELOPPEMENT

The semiconductor market had its best year in 2018, reaching almost US$470 billion. However, growth was slower than anticipated due to sluggish smartphone and automotive sales.

MEMS, which follows the semiconductor market, also had a good year, but with a slower growth rate than anticipated. However, Yole Développement (Yole) expects the MEMS market to experience significant growth between 2019 and 2024 (Figure 1).

The market research & strategy consulting company estimates the market will exhibit +8.3% growth in value and +11.9% growth in units, with consumer still having the biggest share. Yole's analysts announce, more than 60%.

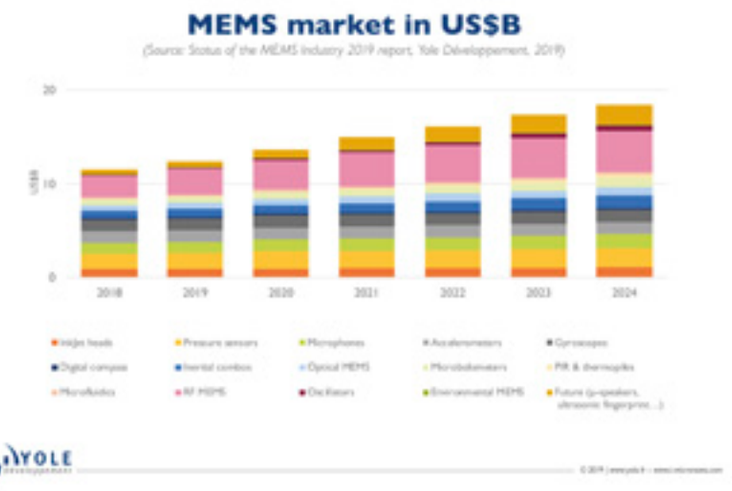

Figure 1. The MEMS market is expected to experience significant growth between 2019 and 2024.

Some devices will benefit from new usage: for example, MEMS printheads for high-resolution printing, and microphones for more widespread adoption of voice interface. Also, regulation will favor pressure sensor growth due to the implementation of TPMS regulations in China.

For inertial MEMS, automotive and consumer will continue to be a major part of the demand, focusing mostly on combos which provide better form factors and easier integration/higher functionality.

Moreover, new applications are coming, such as medical (especially wearables) and industrial (for example, machine health monitoring) for stand-alone inertial MEMS. Also, IMU growth will be driven by automotive (i.e. robotic vehicles). Future cars could integrate MEMS mirrors, which could find new usage in solid-state LIDAR, as well as microbolometers for night vision capabilities and situational awareness in ADAS.

Yole believes smart buildings and retail will also be the impetus for infrared sensor market prosperity. On the medical side, Si continues to be adopted by microfluidics companies that develop CMOS-based biochips. Despite a slowdown in the smartphone market, 5G will drive the demand for new chips: this is the case for RF MEMS and MEMS oscillators, which will be needed in the deployments of new base stations and for the ever-growing edge computing.

Under its Status of the MEMS Industry annual report, 2019 edition, Yole has revamped its RF MEMS forecast due to a delay in the adoption of the 8 x 8 MIMO. Despite this, Yole's analysts believes BAW filters will grow from US$2.3 billion to US$4.4 billion, from 2019 to 2024.

Last but not least, emerging MEMS like environmental MEMS, micro speakers, fingerprints, and auto-focus will fuel future market growth. This will be linked to new applications for more mature MEMS devices, such as key fob signal-blocking (accelerometer), gunshot localization (microphones), AI speakers, etc. Moreover, sensor fusion coupled with AI (and eventually edge computing) could stimulate new use cases and rejuvenate the MEMS market.

MEMS & sensors are an historic activity at Yole. For more than 20 years, analysts are following this industry and exchange with leading companies to identify the changes and understand technical disruptions. This year again, they provide a relevant technology & market analysis of this market with a comprehensive understanding of the technical challenges and business issues.

Authors: Eric Mounier, PhD. Fellow Analyst, Photonics, Sensing & Display, Yole Développement (Yole) - Dimitrios Damianos, Technology & Market Analyst, MEMS Sensors Photonics Imaging, Yole Développement (Yole)

CEO Panel cont'd from p 7

rect, it doesn't deliver it today simultaneous improvements in power, performance area and cost. Over the last few years, that classic approach has really run out of gas. But we've talked about five different drivers in this new playbook. One is architecture innovation. Especially with AI and big data and with workload-specific types of applications, in the edge cloud, training and inference, architecture innovation is a huge focus for many different companies. The innovation around new structures – Sanjay talked about 2D and 3D NAND – the playbook in NAND for decades was to shrink in two dimensions and then now we go vertical. It's a different driver. You hit a physical limit and you hit a cost limit. Now it's about new structure and new materials. Also, how you connect the chips together in packaging, heterogeneous integration. That's another driver. There's now question that classic 2D scaling has run out of gas, but there are all of these new opportunities in structure innovation, materials innovation architectures and packages. The challenges are significant, but there's tremendous opportunity not looking backwards, at classic Moore's law 2D scaling, but looking forward with these five year drivers in this new playbook.

Nanometrics and Rudolph Announce Merger

Michael Plisinski, CEO of Rudolph

Pierre-Yves Lesaicherre, President and CEO of Nanometrics

Nanometrics Inc., a leading provider of advanced process control metrology and software analytics, and Rudolph Technologies, Inc., a leading provider of semiconductor process control systems, lithography equipment, and software for wafer fabs and advanced packaging facilities, announced that they have agreed to combine in an all-stock merger of equals transaction. The merged company will be a premier end-to-end metrology, inspection, process control software, and lithography equipment provider for the semiconductor industry and other advanced markets.

Under the terms of the agreement, which was unanimously approved by the Boards of Directors of both companies, Rudolph stockholders will receive 0.8042 shares of Nanometrics common stock for each Rudolph share. Upon completion of the merger, current Nanometrics stockholders will own approximately 50% and current Rudolph stockholders will own approximately 50% of the combined company.

Rudolph CEO Michael Plisinski will serve as Chief Executive Officer and Rudolph CFO Steven Roth will serve as Chief Financial Officer of the combined company, alongside a highly experienced leadership team comprised of executives from both companies. The Board of Directors will be led by Nanometrics director Christopher Seams and will have 12 directors, consisting of six from each existing Board. The combined company will be headquartered in Wilmington, Massachusetts and will maintain a strong presence at Nanometrics' headquarters in Milpitas, California.

Nanometrics President and Chief Executive Officer, Pierre-Yves Lesaicherre said, "Nanometrics has a long history of innovation in the field of optical metrology, pioneering the use of scatterometry for semiconductor process control. In recent years, we have established a strong position in optical critical dimension metrology, enabling the ramp of advanced technology nodes by each of the major semiconductor manufacturers worldwide. Our merger announced today with Rudolph marks the culmination of our respective businesses' growth, diversification, and increased scale."

Rudolph Chief Executive Officer, Michael Plisinski added, "This strategic transaction brings together two successful and complementary teams and product portfolios. Nanometrics' metrology portfolio is a strong strategic fit with Rudolph's current diversified product lines including software, inspection, metrology, and lithography. Our current set of products has already created integrated solutions for the advanced packaging market, and we expect to develop new integrated solutions for customers as we are able to draw from an even larger set of products in the future.

1,000th SEMI Industry Standard Marks 40+ Years of Microelectronics Innovation

SEMI announced yesterday at SEMICON West the publication of the 1,000th SEMI international Standard since the launch of the program in 1973. A linchpin of innovation for electronics manufacturing, SEMI Standards make possible smaller, faster and smarter electronics that have transformed the way we live and work.

"SEMI Standards are the oxygen of the electronics industry, speeding product development, boosting product reliability, driving down manufacturing costs, and increasing factory efficiency while improving worker safety," said Ajit Manocha, SEMI president and CEO. "Electronics have evolved to deliver greater social good across automotive, healthcare, agriculture and countless other industries that touch our daily lives. These innovations all start with SEMI Standards."

SEMI Standards are as pervasive as their impact is profound. They have enabled the production of more than 2.2 billion wafers, 1.8 trillion IC devices. A purchase order for a piece of semiconductor processing equipment typically cites an average of 25 SEMI Standards. The 1,000 SEMI Standards include protocols for hardware and software communication, traceability, 3D-IC, compound semiconductors, facilities, MEMS, metrics, silicon wafer, carriers and automation systems. The Standards are used in many segments including display, photovoltaic, printed circuit board manufacturing and high-brightness LEDs.

The 1,000th SEMI Standard – SEMI S30 – defines the safe use and handling of energetic materials, the potentially hazardous process chemicals used increasingly in semiconductor manufacturing to spur advances in materials purity, integrity and quality. SEMI S30 is titled EHS Guideline for Use of Energetic Materials in Semiconductor R&D and Manufacturing Processes.

Volunteer SEMI members lend their specialized expertise to develop SEMI Standards for the benefit of the global electronics industry.

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