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JULY 11, 2019
THURSDAY

Jeffrey Welser, Ph.D
Vice President/Lab Director
IBM Research-Almaden

The Future of Computing: Moore's Law on Steroids

BY SHANNON DAVIS, WEB EDITOR

In his keynote address at SEMICON West on Wednesday morning, Jeffrey Welser, Ph.D. described a future of computing that looks fundamentally different than what we experience now. Dr. Welser, the Vice President and Lab Director of IBM Research-Almaden, discussed ways in which hardware and software engineers alike are looking to fuse neuroscience with computer science to drive new opportunities to the next level.

Dr. Welser described what IBM Research is learning from how our brains process information to begin to build networks more like neural networks.

In this case, it would be just layers of very simple computations, that would take inputs from the layer ahead of it, sum them up to a certain computation, and pass them on to the next layer," Welser explained to his audience. "And all you could really do was sort of adjust the weights of connections."

Welser says this is very much like we think the brain works; however, up until recent years, there hadn't been enough data in existence or adequate computing power to make it an efficient or useful processing method. But starting

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DON'T MISS

10:29 am -12:39 pm
Role of 5G for Smart Transportation
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10:30 am – 12:40 pm
Advanced Lithography: Delays and Pivots Along the Way to 5nm and Beyond
TechTALK Stage North

10:30 am -12:40 pm
MEMS Manufacturing for 2020 and Beyond
TechTALK Stage South

1:30 pm – 5:30 pm
Advanced Applications
Meet the Experts Theater, SMART Transportation Pavillion

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Supply Chain Integration
TechTALK State North

1:30 pm – 3:35 pm
Traditional and Not So Traditional "More Moore" Scaling
TechTALK State North

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Moore's Law cont'd from p 1

in the earlier 2010s, error rates of experimental neural networks began to go down and by 2015, Welser said IBM actually surpassed the ability of humans' image recognition.

"It's really quite interesting now that it's becoming something you can utilize," said Welser.

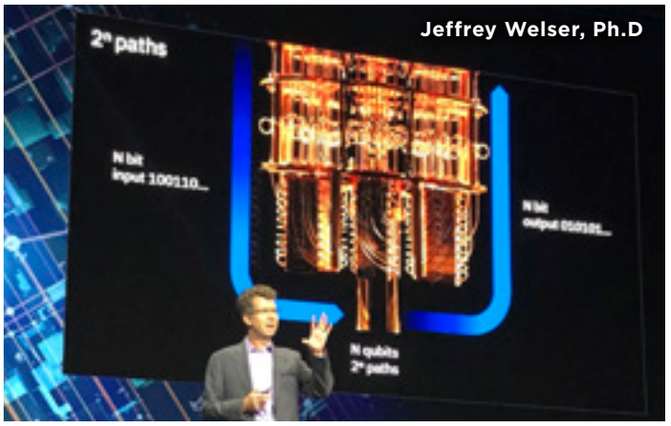
Welser said IBM is making more advances toward continuing to improve GPUs and algorithms for neural networking and its uses in AI, which, he said, is just an extension of what we use to call "big data" in the past. AI analyzes much less structured data in ways similar to how CPUs run big data analytics, except AI doesn't just analyze databases of numbers and texts, but also things like images or audio or natural language.

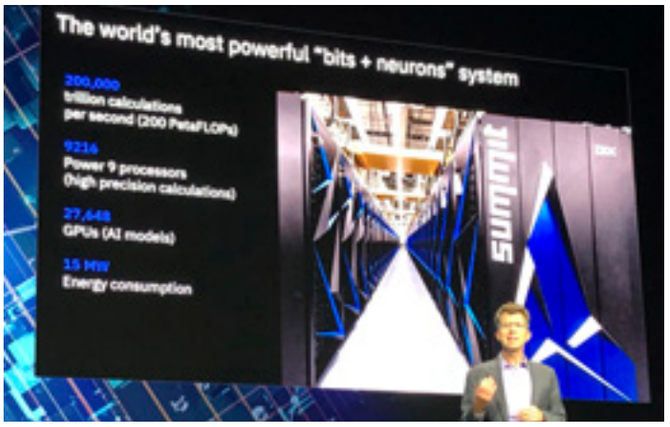
"Our big data analytics pretty much solely ran on CPUs," said Welser. "If you look at why AI works today on deep learning, it is because we use things like FPJs and GPUs, which can do massive parallelization of these fairly simple calculations necessary to make a neural net work. And so they've become very efficient as I've said, they can actually better than us at actually making decisions in image recognition."

GPUs and beyond, into the realm of quantum computing.

The basic difference, Welser described, between a quantum system and a traditional system is the bits of information, which, in a traditional system, is always a one or a zero. In quantum computing, qubits, or quantum bits, are used – which is a quantum state that can be a one or a zero or it can be a superposition of both.

"The two key attributes you need to take advantage of if you're going to use quantum computing, one is super position," said Welser. "The ability of that qubit to be some proportion of one and zero in a linear superposition between them. But also it's the idea that you can entangle two qubits, so you can actually set the two qubits so that they both are in a probability state between one and zero. But once you measure one or manipulate one, it actually changes what the other ones are doing. And in fact you can do that among a huge number of qubits, and no matter how far apart they are, as soon as you do make a manipulation to one, it manipulates all of them simultaneously."





This is a great time to be in the hardware business, because it's getting fun and interesting again to use the materials and device exploration.

JEFFREY WELSER, PH.D
VICE PRESIDENT AND LAB DIRECTOR, IBM RESEARCH-ALMADEN

If you're a quantum physicist, this new type of computing could give you a massive parallelization in terms of the kinds of calculations you can do and the number of different states you could test at the same time.

"And it's this exponential increase in the number of states you can represent and manipulate once that really gives the power behind the quantum computer, if you can map the problem appropriately," said Welser.

IBM put out the world's first quantum computer in May 2016, which was a five-qubit system. There's now a 16-qubit system in existence as well. However, "there are certain calculations that you literally cannot do on a classical system, no matter how big you intend to build the system," said Wesler. "But if you had a quantum system, and they were good, noise-free, perfect quantum bits, you could do with about 160 qubits. We're wrestling with 50 qubits today, so that's not that far in the future.

"So, this is kind of like Moore's Law on steroids, right?" he said.

"I think this is a great time to be in the hardware business, because it's getting fun and interesting again to use the materials and device exploration," Wesler concluded. "There are going to be a lot of challenges to do it to get to these next levels of computing, but at the same time, I think they're going to offer some really interesting tools to advance how quickly we can do those sorts of experiments."

Welser told his audience that IBM is going to find more efficient ways of connecting the

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Maximizing EUVL System Availability

The innovative process of extreme ultraviolet lithography, known in its short form as EUVL or EUV, is the next generation lithography technology that leading semiconductor chipmakers plan to use in the manufacturing of the most advanced semiconductor components. This technology has an historic importance, as it is enabling the continued extension of Moore's Law. The immediate challenge for EUV is the tool uptime.

Figure 1. Edwards has established a platform on its EUV Zenith system that enables system health monitoring via remote connectivity to equipment parameters.

AS EUVL enters high volume production, there is a strong need to optimize system availability, and one of the most important factors in doing so is tied to the availability and performance of the EUVL tool sub fab vacuum and exhaust gas management sub-system. "Never at any other time in the history of Moore's Law has it been so acute for the sub fab to understand the critical importance of the EUV lithography platform," said Niall Walsh, Program Development Manager at Edwards.

Although vacuum and abatement equipment is common place in semiconductor fabs, the vacuum and abatement sub-system for an EUVL tool presents a subtly different challenge to the conventional philosophy in the sub-fab. On one hand, the required availability on other process tools (such as CVD and etch) is restricted by the necessity to perform scheduled maintenance activities on those tools as well as the sub-fab equipment due to harshness of those processes. On the other hand, for EUVL 100% availability of the vacuum and abatement subsystem would ultimately be required so as not to restrict wafer throughput. Consequently, the ability of this vacuum and abatement sub-system to manage the process tool gases continuously and safely in all tool states is integral to delivering maximum availability of the process tool.

To address the new requirements, Edwards has established a platform on its EUV Zenith system (Figure 1) that enables system health monitoring via remote connectivity to equipment parameters. This enables rapid response time by immediate access to in house subject matter experts for the predictive and corrective maintenance activities for improving tool operation and overall availability. "With over 10 years of enabling EUV from a sub fab perspective, our innovative leading technology solutions and systemization capabilities continue to strive to enable maximum EUV process up-time and yield within a managed safe environment," Walsh said.

The ASML EUVL Process and Tool environment is driven around availability and productivity performance where reliability and process stability stands high in the requirements ranking for product and equipment needs. Defining that very need, from a sub fab perspective, is captured in the SEMI E10 standard, which establishes a generic way of measuring equipment performance and productivity through the definition of six basic equipment states (Figure 2).

Here are a number of key initiatives and processes to maximize the EUV Zenith availability:

- An Availability Matrix to understand reliability and availability loss of system components during design phase and field operation resulting in identified availability projects
- A known issues management process which actively addresses faults if and when they arise driven by our global installed base (ISB), of over 100 dedicated EUV sub systems enabling lessons learned for further improving both scheduled and unscheduled activities
- As a result, a continuous improvement program can be designed to ensure the sub fab vacuum and exhaust gas management subsystem delivers the maximum EUVL Tool uptime possible
- In addition, the process of continuous feedback of existing PM schedules and timings ensures a continuous focus on improving overall availability

"We have an availability matrix and known issues monitoring process. We have a continuous improvement program. We have a really close collaboration and partnerships and with end customers and OEMs. All these coupled together drive our availability program and our improvement," said Walsh.

Walsh said they have also initiated projects to drive towards the "golden number" of 99.9% availability. "The ASML system continues to evolve as does ours," Walsh explained. "The global installed base that we support is more than 100 systems dedicated to EUV. It's quite an installed base and with the onset of high volume manufacturing now at different customer locations that figure could double in the coming years."

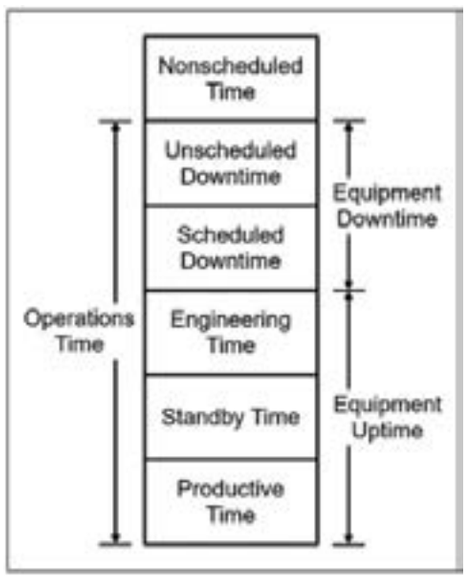

Figure 2. The SEMI E10 standard establishes a generic way of measuring equipment performance and productivity through the definition of six basic equipment states.

The Industry's Most Yield-Enhancing Macro Defect Inspection System

Nothing else gives you as <u>much</u> information on as <u>many</u> wafers...

Inspect <u>all</u> wafers. Super fast. No sampling.

EagleView 5 automatically macro-inspects every single wafer in every single lot. Edge to edge. At ultra high speed: 3000+ wafers/day. This unique tool delivers an actual high-res full-wafer color image, not a digital construct. And it creates a complete, trackable "waferbase" that also includes each wafer's OCR number and slot position. This data hub provides a unique wholistic picture of every wafer at every step. And it can even integrate data from microscope and micro defect inspection.

No recipes required. Just load and go.

EagleView accepts four cassettes, with 100mm to 300mm wafers. And no recipes are needed. It's totally plug-and-play. So you can eliminate all the time, hassle and special staff to generate and maintain recipes. With full automation, virtually anyone in your fab can use it anytime.

Catch more defects. And more root causes.

Because it sees every wafer, EagleView can catch a lot more defects. And, it gives you smarter ways to track down root causes. At the start of each run, the fab's host automation system sends the lot's tool history to EagleView, where that gets integrated with the wafer image data. So when you spot a defect you can easily drill down to see which particular process tool was the likely culprit.

Spot onesie-twosies. Stop excursions.

EagleView's 100% inspection catches even those elusive one-time problems. Spotting them sooner often lets you rework wafers rather than having to scrap them later on. And correcting excursion problems earlier helps improve fab performance overall. Plus, EagleView's special guardbanding capability can clearly ink-off problem areas on wafers so they won't cause surprises down the line.

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While EagleView is inspecting wafers it can also randomize or sort them. Automatically. While maintaining full speed. So, if you want to do slot position analysis you won't need to buy extra sorters. And you won't need special IT efforts to create usable databases.

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EagleView removes all the variables of human optical inspection. Its defect data recording is consistent and complete. Every shift. Every day.

Information for all.

There are no licenses restricting how many stations can use EagleView wafer data. Everyone can access it. Throughout your fab or enterprise, around the world. No extra charge.

Higher yields. Lowest CoO.

EagleView needs no consumables, and maintenance is so minimal, customers can do it themselves. Plus, you can save all those resources you used to spend on recipes. And get guardbanding ink-off virtually free. Bottom-line: EagleView has the lowest CoO of any tool in its class.

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Maybe you work with silicon carbide or other transparent wafers. Or you need OCR to convert vendor scribes to lot IDs. Or wafers split to double-spaced cassettes. Or custom slot positions. Just tell us what you need!

EagleView: popular and proven.

These powerful tools have already inspected over 300 million wafers and they're boosting yields around the world. Perhaps EagleView could be helping <u>your</u> fab. Why not set up a demo and see for yourself!

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Memory Industry: A New Phase of Consolidation Due to The Entrance of Chinese Players

Simone Bertolazzi, Technology & Market Analyst, Memory, Mike Howard, VP of DRAM & Memory Research, and Walt Coon, VP of NAND & Memory Research at Yole Développement (Yole)

Despite some cyclicality and seasonality, the stand-alone memory market has experienced extraordinary growth over the past decade. This has been driven by important megatrends, such as mobility, cloud computing, artificial intelligence (AI), and the Internet of Things (IoT). NAND and DRAM account together for around 97% of the overall stand-alone memory market. Their revenues hit a record high of around US$160 billion in 2018, registering an impressive compound annual growth rate (CAGR) of 32% between 2016 and 2018.

At the end of 2018, both NAND and DRAM markets started experiencing oversupply caused by unseasonably weak demand, including lower than- expected smartphone sales and a slowdown in datacenter demand. DRAM prices are projected to decline by around 40% this year and likely will not increase again until 2020. For NAND, the outlook is more positive with potential for improving market conditions in the second half of 2019.

In the long-term, NAND and DRAM revenues are forecast to grow with CAGR2018-2024 of 4% and 1% respectively

Market concentration has accelerated dramatically in the last decade and is now very high, with three dominant NAND and DRAM players, namely Samsung, Micron, and SK Hynix, and two pure NAND players, namely Toshiba and SanDisk/Western Digital, holding a combined 95% market share.

Nowadays, it is unlikely that the memory market could consolidate further. No significant mergers or acquisitions were recorded in 2018 in the DRAM industry. The major event in the NAND business was the sale of Toshiba's memory unit to an investment group led by Bain Capital and including Apple, SK Hynix, Dell, Kingston and Seagate.

Meanwhile, Chinese players could become a threat and might trigger a new phase of market consolidation in the long term (Figure 1). In China, central and local governments, in partnership with a number of private players, are investing billions of dollars to develop a local semiconductor memory ecosystem. Objectives are to:

- Bridge the gap between domestic production and consumption,
- Reduce dependency on the supply of global memory companies,
- Fulfill huge memory chip demand in strong growth segments like mobile/ wireless, consumer, servers, AI, IoT, and automotive.

Figure 1.A map of the key memory players in China.

In the NAND business, Yangtze Memory Technologies Co. (YMTC) is the most likely to succeed out of all the publicly-known Chinese memory players, thanks to significant financial backing from government investment funds and a head start on R&D and manufacturing. The company's volume production of 64-layer 3D NAND devices based on the newly-developed XtackingTM technology is expected to take off in the second half of 2019.

On the other hand, DRAM in China is still in the technology-development phase. DRAM manufacturing is incredibly difficult and it will likely take a while longer for China to achieve competitive parity with the rest of the industry.

Yole Développement (Yole) expects that significant output from Chinese vendors could reach the market in 2020 for NAND, likely later for DRAM. Meanwhile, stand-alone NOR will remain the most solid memory business in China thanks to a well-developed local supply-chain system. In coming years, a possible relaxation of the China-US trade tension might open up new opportunities for China to acquire key companies across the memory supply chain, which could reinforce China's position in the semiconductor memory industry.

Memory activities at Yole Group are supported by a dedicated team including PhD and MBA qualified industry veterans from Yole Développement, System Plus Consulting and KnowMade. They daily collect information, identify trends, challenges, emerging markets, and competitive environments. They turn that information into results and give their customer a complete picture of the memory industry's landscape.

With this strong market positioning within the memory industry, the Group proposes for the 1st time, an Executives Breakfast, prior the Flash Memory Summit on August 6, from 7:00 AM to 9:30 AM. Titled "Executives Breakfast – Memory industry: What could happen in the future?" ,this event is a great opportunity to get a comprehensive picture of the memory industry and debate with analysts and industrial experts. Program & registration are now available on i-micronews.com.

SEMI Announces Election and Re-Election of Board Members

SEMI today yesterday at SEMICON West 2019 the election of Kazuo Ushida, Chairman of the Board, Representative Director, Nikon Corporation, as a new member of the SEMI International Board. In addition, SEMI confirmed the re-election of six current members to the SEMI International Board of Directors in accordance with the association's by-laws.

The following six Board members were re-elected for two-year terms:

- **Michael Allison,** CEO, VAT
- **Bertrand Loy,** president and CEO, Entegris
- **Daisuke Murata,** president and CEO, Murata Machinery
- **Stephen Schwartz,** president and CEO, Brooks Automation
- **Kyu Dong (KD) Sung,** CEO, EO Technics
- **Xinchao Wang,** Honorary Chairman, JCET

The SEMI Executive Committee confirmed Bertrand Loy, president and CEO of Entegris, as chairman of the SEMI Executive Committee. SEMI also confirmed Kevin Crofton, president of SPTS and corporate vice president at Orbotech, as vice-chairman.

The leadership appointments and the elected board members' tenure become effective at the annual SEMI membership meeting on July 10, during SEMICON West 2019 in San Francisco, California.

"The SEMI Board of Directors is comprised of global business leaders who represent SEMI members and the industry, ensuring that SEMI develops and delivers member value in all regions," said SEMI president and CEO Ajit Manocha. "We congratulate the newly elected and re-elected members and greatly appreciate all of our board members' contributions to the industry."

Nikon's Kazuo Ushida

SEMI's 17 voting directors and 11 emeritus directors represent companies from Europe, China, Japan, Korea, North America, and Taiwan, reflecting the global scope of the association's activities. SEMI directors are elected by the general membership as voting members of the board and can serve a total of five two-year terms.


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CMOS Image Sensors: Expect a 10.1% Year-on-Year Growth Rate for 2019

"CIS has become a key market segment in the semiconductor industry, reaching US$15.5 billion in 2018", asserts Chenmeijing Liang, Technology & Market Analyst, Photonics, Sensing and Display at Yole Développement (Yole). And Yole's analyst adds: "And it should exceed 3% of the total semiconductor sales".

This segment has seen Sony become a significant semiconductor player, alongside other CIS players such as Samsung, OVT, and ON Semiconductor. Innovative approaches like wafer stacking technologies have emerged specifically for CIS, and have become key developments for the semiconductor market in general. In the context of a fierce rivalry in the technology sector, imaging has become a key focal point of OEMs and the entire semiconductor supply chain (Figure 1).

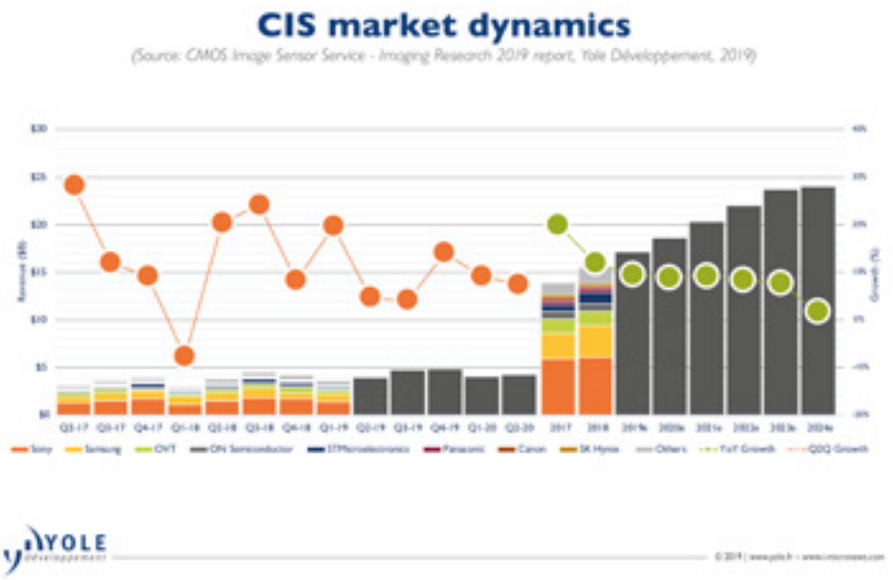


Figure 1. The CIS segment has seen Sony become a significant semiconductor player, alongside other CIS players such as Samsung, OVT, and ON Semiconductor

The market research & strategy consulting company announces today a new product, published in quarterly instalments. Titled CIS Service – Imaging Research, this monitor contains world-class research, data, and insights pertaining to the imaging markets. With a full package including an Excel database with quarterly update on historical and forecast data, a PDF slide deck with graphs and analysis covering the expected evolution and a direct access to Yole's analysts for one year. The new product powered by Yole, proposes a detailed description of the CIS markets' evolution in terms of revenue, shipments, capex, and near-term price evolution, as well as demand per market segment and CIS technology evolution. NIR (near infrared) sensing is also included in this quarterly imaging monitor, as well as detailed profiles of main suppliers.

In 2007, smartphones began disrupting the imaging market and its corresponding technology. Just five years later, the production peak for digital still-cameras was reached, and phones became the primary imaging device for consumers. "New use-cases linked to social media began fueling the need for high-quality rear (world-facing) cameras for photography, quickly followed by front (selfie) cameras for videos and top-grade photography", details Pierre Cambou, Principal Analyst, Imaging at Yole.

2015 – 2017 saw additional cameras attached, either to extend the zoom capability on the rear or to provide 3D biometric interaction on the front. Pierre Cambou adds: "In 2019, 3D rear cameras are pushing the trend further to the back, improving the photographic experience and making inroads into AR (augmented reality) applications."

In 2019, the overall attachment rate for CIS cameras per phone is moving towards in average of 2.5 units per phone, and the growth rate for CIS attachment will rise from 6.5% to 7.8% from 2019 to 2021. Amidst stagnant smartphone volume, CIS attachment rate is a central, successful strategy for main smartphone OEMs like Apple, Huawei, and Samsung.

Alongside mobile, which is the main application market with 70% of all CIS sales, security and automotive are experiencing double-digit growth and have grown into billion-dollar CIS segments.

So what do the upcoming quarters hold? 2019 looks slightly different than 2018, confirm Yole's analysts with the new tool, CIS Service – Imaging Research. With a low Q1, the CIS market faces a slowly eroding ASP (average selling price) since most players can now match Sony's proposition. Nevertheless, the market remains constrained in terms of capacity, with capex the main limiting factor since customers always want more CIS cameras. The outlook though remains very positive. Yole announce a range of 10% year-on-year in 2019 and 8% over the long-term. In 2024, CIS is heading for US$24 billion. Without doubt, the CIS industry is still showing a bright future...

These results will be presented in Shenzhen, China beginning of September. Therefore, Yole is proud to collaborate once more with the China International Optoelectronic Expo (CIOE) to organize a new edition of the Executive Forums on Photonics, from September 4 to 6, 2019 in Shenzhen, alongside the 21th CIOE.

4 dedicated sessions have been planned: IR imaging – Si photonics – LiDAR – 3D sensing. List of speakers is impressive: HIK Vision, HP Electronics, Innoviz, Intel, LGE, Oxford Instruments, Sicoya, System Plus Consulting, Teem Photonics, ULIS, Valeo, Yole Développement and more... Program & registration on i-micronews.com.

New Mobile Leak Detectors

Pfeiffer Vacuum's ASM 390 and ASM 392 are leak detection solutions adapted to the semiconductor and display industries as well as to other demanding applications where rapid pump down and high sensitivity is key. Both models are Semi S2 compliant. The leak detectors are fitted with a dry frictionless backing pump and a powerful high vacuum pump, making them the ideal tools for leak testing of various components in clean environments.

Equipped with an additional turbopump, the ASM 392 will speed up the leak detection process to reduce the downtime of the production equipment. The ASM 390 and ASM 392 have been developed to provide full confidence in leak testing regardless of operator knowledge. They deliver accurate results in minimal time, making them highly efficient in the field.

ASM 390 and ASM 392 are uniquely ergonomic with a convenient size and height, a secondary handle in the front, a fully rotatable, removable display, an inlet in the front for easy connection to test ports and maneuverability for access to all testing areas, even in tight spaces.

Thanks to a wide, clear color touch panel display, an integrated toolbox with modular compartments and storage space for vacuum bellows, leak detection can be very easy.

Pfeiffer Vacuum mobile leak detectors ASM 390 and ASM 392 for rapid pump down and short response times on large test objects.

How "Guardbanding" of Inline Wafer Defects Can Improve Chip Reliability Insurance

In previous bulletins we discussed the problem of partially-defective, marginal die that are still functional enough to pass final electrical test. Some of these "walking wounded" chips get past final testing, but in the customer's end product, under ongoing stress, they may fail. This is a particularly serious issue with automotive, medical and other customers who demand maximum long-term device reliability.

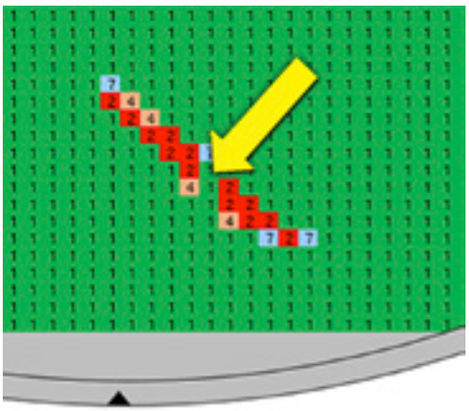


Figure 1. Guardbanding can remove these questionable mid-scratch die.

The semiconductor industry has long used a process known as digital guardbanding to ink-off suspect die. This updates the die coordinates on the wafer map preventing shipment of suspect die. Guardbanding removes marginal die and also takes out additional die around the edges of clearly identified defective die, this added insurance is known as a "buffer."

To accomplish this, neighboring-die algorithms may be used to automatically search wafer maps and apply guardbanding based upon proximity to known bad die. For example, in Figure 1, guardbanding might have been used to remove the questionable "good" area (indicated by arrow) within the scratch zone.

Putting guardbanding to work earlier

To date, guardbanding has been used primarily at end-of-line testing — but it can also play a critical role during in-line inspection. That's because final inspections can still miss a variety of defects that occur earlier in line. For example, certain in-line problems can get covered over by subsequent processing steps and become very difficult to detect later. For this reason, in-line macro defect inspection and in-line guardbanding have become essential complements to traditional micro inspections and electrical testing.

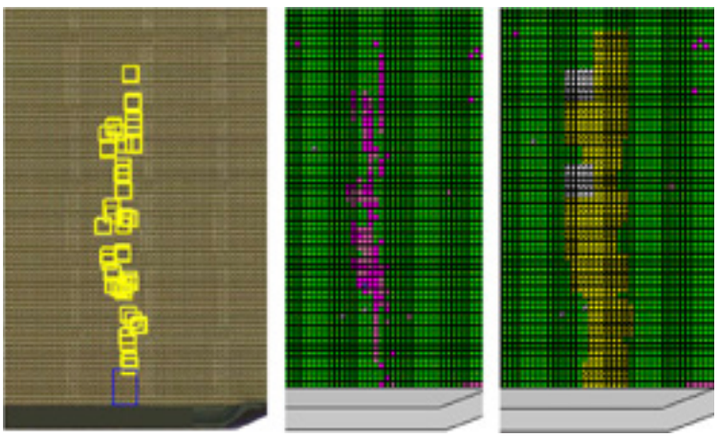


Figure2a. Scratch defect detected by macro inspection.
Figure 2b. Same defect at wafer probe
Figure 2c. Wafer probe with guardbanding.

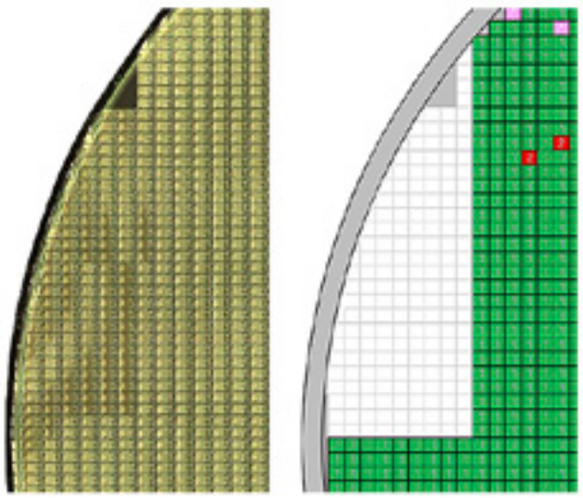


Figure 3a. A photo hotspot detected by macro inspection.
Figure 3b. At wafer probe with stepper shot guardbanded.

In-line macro defect inspection and guardbanding — at high speed

With today's generation of ultra-high speed automated macro inspection tools, such as the EagleView from Microtronic, fabs can now inspect every wafer in the lot — without need for sampling or recipes. This allows fabs to inspect many more wafers at many more processing steps — to correct process and equipment issues sooner, and to save more wafers from being scrapped or affected in an excursion. And in addition to identifying in-line macro defects, EagleView also makes it easier to guardband those defects...

Some fabs still use a hand-drawn paper tracing system to enable guardbanding, which is time consuming and inaccurate. With the EagleView platform, guardbanding is performed directly on a high-resolution wafer image, for maximum precision and ease.

The tool may be set to automatically add guardbanding to some defects, or an operator may add guardbanding selectively to specific defects. Some types of scratches, for example, may scatter particles onto surrounding die. Figure 2a shows a scratch detected by macro inspection. Figure 2b shows the same wafer at wafer probe, and Figure 2c shows the scratch with guardbanding added.

Integrating defect data from more sources

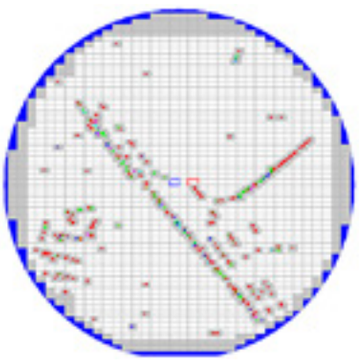
The macro inspection tool produces a true high-resolution, permanent-record image of every wafer, which builds a powerful, comprehensive database of defect information for the fab (Figure 3). These files provide a rich and valuable data resource for end-of-line testing, for root cause analysis of current in-line

problems or to refer to at any time in the future.

Importantly, the EagleView system can also import KLARF files from micro-inspection tools (Figure 4a) and overlay them onto the EagleView image (Figure 4b) where a user-defined buffer can be applied real-time. The wafer probe map is displayed in Figure 4c, and Figure 4d shows the resulting guardbanded wafer probe map. EagleView can use SEMI standard G85 wafer maps or apply a translator for legacy probe map systems.

Doing more to enhance chip quality

Today, there are still many ways for defects to slip through final testing and get shipped to customers. However, in-line macro defect inspection and guardbanding are important and powerful tools that can help fabs to catch more problems earlier — to improve chip reliability, reduce returns and keep customers happier.



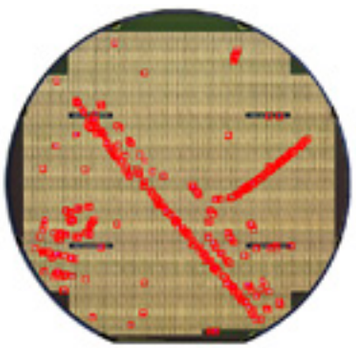
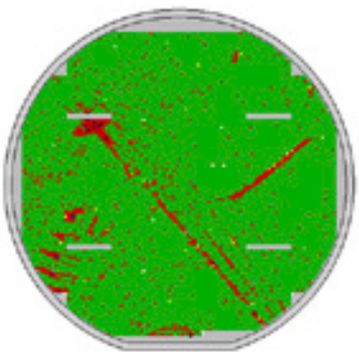


Figure 4a. KLARF file from micro inspection.
Figure 4b. KLARF file overlaying EagleView wafer image.



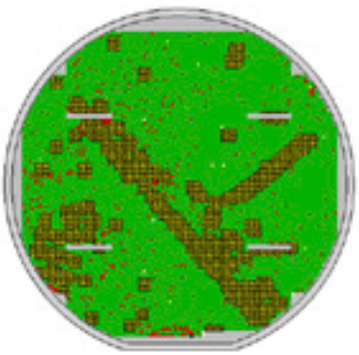


Figure 4c. Probe map of the same wafer.
Figure 4d. Wafer probe map with guardbanding.

DuPont Introduces Three New Cleaning Chemistries

DuPont Electronics & Imaging announced three new chemistries to support advanced semiconductor fabrication: DuPont™ EKC™ PCMP2110 cleaner, EKC™ PCMP3210 cleaner and EKC™ 590 CuSolve™ remover.

DuPont's EKC Technology group develops materials for precision cleaning and surface preparation in semiconductor fabrication processes including front- and back-end-of-line wafer processes, packaging and assembly. These new expansions to the EKC cleans portfolio address a number of complex challenges associated with advanced technology node processes, where the number of process steps has increased. EKC™ PCMP2110 and EKC™ PCMP3210 are new chemistries for post-chemical mechanical planarization (CMP) cleaning, whereas EKC™ 590 CuSolve™ is a new offering for post-etch residue removal.

The most recent of the three new innovations, EKC™ PCMP2110 is formulated for emerging logic and memory CMP processes that use ceria-based slurries. At advanced nodes, cleaning after ceria CMP is challenging due to increasingly higher removal rate requirements and the small ceria particle size. EKC™ PCMP2110 provides better post-CMP (PCMP) cleaning performance than specialized cleans used in the marketplace today, while also making it possible to eliminate post wet bench commodity clean steps such as sulfuric peroxide mixture (SPM) or sulfuric acid.

EKC™ PCMP3210 is DuPont's first offering for tungsten PCMP, designed for sub 14nm FinFet logic. Compatible with tungsten in an alkaline formulation, EKC™ PCMP3210 effectively cleans dielectric layers after CMP (such as silicon nitride and TEOS), preventing corrosion within very tight specifications. EKC™ PCMP3210 has already been adopted by a number of manufacturers at advanced nodes.

"As customers move to advanced node processes for both memory and logic, the number of CMP steps increases and it becomes even more critical to have efficient in-line cleaning," said Douglas Holmes, EKC Business Director, DuPont Electronics & Imaging. "With the introduction of our two newest PCMP products, we can help our customers reduce overall process complexity and protect wafer yields."

Augmenting DuPont's post-etch removal chemistry portfolio, EKC™ 590 CuSolve™ is the first commercial post-etch cleaning product designed for use in creating copper interconnects at the 7nm node and beyond. DuPont's removal chemistry eliminates reactive ion etch (RIE) residues and residues from the titanium nitride masks used in the etch process, while also etching aluminum nitride for subsequent copper metal filling, all in a single efficient step. EKC™ 590 is compatible with both copper and cobalt and is also backward compatible with mature technology nodes.

"With EKC™ 590, customers can remove titanium nitride hard mask and post-RIE residues, etch aluminum nitride and complete in-situ cleaning in a single quick step," said Robert Auger, Ph.D., Removal Chemistry R&D Director, DuPont Electronics & Imaging. "We're pleased to bring our customers a first-to-market cleaning solution for sub 7nm nodes that enables them to create highly reliable copper interconnects."

All three new products are available globally for sampling.

CEA-Leti and UnitySC Announce Further Collaboration

Leti, a research institute of CEA Tech, and UnitySC, a wholly owned subsidiary of FOGALE Nanotech Group and a leader in inspection and metrology solutions for advanced semiconductor packaging, today announced a four-year extension of their collaboration to further advance metrology-inspection capabilities per tool, while reducing the tools' footprint and cost of ownership.

CEA-Leti and UnitySC have been working on the development of a metrology-inspection platform for the past four years. The initial targeted applications were 3D integration modules, specialty bonding, and CMP. So far, the collaboration has helped advance UnitySC's system from a table-top tool to a fully automated 200-300 mm Swiss Army knife-like platform that has shown very good performance during the validation phase. Today, UnitySC and CEA-Leti extend this collaboration to finalize the improvement of the platform and enhance its application space.

The extended collaboration also will address smarter tools for Industry 4.0. CEA-Leti and UnitySC will specifically work towards improving the platform's ease of use and reliability, enhancing the multi-sensor approach of today tools, and bringing intelligence to the platform by adding innovative artificial intelligence (AI) approaches.

This new generation of the platform, announced during SEMICON West, will allow users to tackle several control problems on different applications. These include buried interface defects on Si and GaN, and SiC edge defectivity control, as well as etch and roughness, bonded wafers and chip-to-wafer alignment, among others.

ZEISS Launches High-resolution 3D X-ray Imaging Solutions

ZEISS recently unveiled a new suite of high-resolution 3D X-ray imaging solutions for failure analysis (FA) of advanced semiconductor packages, including 2.5/3D and fan-out wafer-level packages. The new ZEISS systems include the Xradia 600-series Versa and Xradia 800 Ultra X-ray microscopes (XRM) for submicron and nanoscale package FA, respectively, as well as the new Xradia Context microCT. With the addition of these new systems to its existing family of products, ZEISS now provides the broadest portfolio of 3D X-ray imaging technologies serving the semiconductor industry.

As the semiconductor industry approaches the limits of CMOS scaling, semiconductor packaging needs to help bridge the performance gap. To continue producing ever-smaller and faster devices with lower power requirements, the semiconductor industry is turning to package innovation through 3D stacking of chips and other novel packaging formats. This drives increasingly complex package architectures and new manufacturing challenges, along with increased risk of package failures. Furthermore, since the physical location of failures is often buried within these complex 3D structures, conventional methods for visualizing failure locations are becoming less effective. New techniques are required to efficiently isolate and determine the root cause of failures in these advanced packages.

To address these needs, ZEISS has developed a new suite of 3D X-ray imaging solutions that provides submicron and nanoscale 3D images of features and defects buried within intact structures in advanced package 3D architectures. This is enabled by rotating a sample and capturing a series of 2D X-ray images from different perspectives, followed by reconstruction of 3D volumes using sophisticated mathematical models and algorithms. An unlimited number of virtual cross-sections of the 3D volume may be viewed from any angle – providing valuable insight of failure locations prior to physical failure analysis (PFA). The combination of submicron and nanoscale XRM solutions from ZEISS provides a unique FA workflow that can significantly enhance FA success rates. ZEISS's new Xradia Context microCT offers high contrast and resolution in a large field of view, using projection-based geometric magnification, and is fully upgradable to Xradia Versa.

Xradia 600-series Versa is the next generation of 3D XRM for non-destructive imaging of localized defects within intact advanced semiconductor packages. It excels in structural and FA applications for process development, yield improvement and construction analysis. Based on the award-winning Versa platform with Resolution at a Distance (RaaD) capability, Xradia 600-series Versa offers unsurpassed performance for high-resolution imaging of larger samples at long working distances to determine root causes of defects and failures in packages, circuit boards and 300 mm wafers. It can easily visualize defects associated with package-level failures, such as cracks in bumps or microbumps, solder wetting problems or through silicon via (TSV) voids. The 3D visualization of defects prior to PFA reduces artifacts and guides cross-section orientations, leading to improved FA success rates.

Xradia 800 Ultra brings 3D XRM to the nanoscale realm, producing images of buried features with nanoscale spatial resolution while preserving the volume integrity of the region of interest. Applications include process analysis, construction analysis and defect analysis of ultra-fine-pitch flip chip and bump connections – enabling process improvement for ultra-fine-pitch package and back-end-of-line (BEOL) interconnects. Xradia 800 Ultra enables visualization of the texture and volume of solder consumed by intermetallic compounds in fine-pitch copper pillar microbumps. Defect sites are preserved during imaging, enabling targeted follow-up analysis by a variety of techniques.

Xradia Context microCT is a new submicron-resolution 3D X-ray microCT system based on the Versa platform. It is designed for high-resolution imaging of packages at short working distances with high throughput.

How to Catch More "Disappearing" Latent Defects

By 2020 electronic devices will account for over 35% of the manufacturing cost of an automobile, and by 2030, that number is expected to rise to 50%. Tens of thousands of cars are manufactured each day, with each car using thousands of chips — and if even one of those chips fails in the field it may have disastrous consequences: loss of life, vehicle recalls, major litigation, loss of company reputation and market share and more — potentially totaling billions of dollars.

As a result, carmakers are demanding greater assurances of chip reliability from their suppliers. Now, instead of parts-per-million failure rates they are demanding parts-per-billion levels. And they are insisting that Zero Defect strategies be implemented. So, how do you accomplish that?

Macro defects can become invisible

Fabs have long understood the correlation between wafer yields and chip reliability, so they have used baseline yield improvement as the primary means and metric for increasing chip reliability. But that has not been enough. Certain defects need to be detected earlier in line because some of them are evading end-of-line inspection — and becoming reliability "time bombs" that may go off later in the field!

Part of the challenge has been limited wafer sampling. Because of time and cost constraints, micro defect inspection is usually only used to sample one or two wafers per lot, and only after certain steps. This sampling aims to monitor baseline defectivity, and it assumes that all other significant defects will be caught at end-of-line defect inspection and electrical testing.

However, many types of defects, including many macro defects, only occur intermittently. These are frequently missed by sampling. And when they are not flagged in time they can be covered over by subsequent process steps, often becoming invisible to later inspection. See the "disappearing" macro defect in Figure 1. Because Microtronic's EagleView is an exceptionally fast macro defect inspection system, it enables fabs to macro-inspect all of the wafers in a lot, without recipes, in just a few minutes. So there is no need for sampling. Consequently, EagleView can be used after many more process steps, to catch more problems much earlier in line. So fabs can take more effective corrective actions much sooner... To rework wafers rather than scrapping them later. Or to take problem tools off-line for repair before they cause further damage.

Net result: 100% macro inspection can increase yields while also reducing costs. And, very importantly, it can catch many more time-bomb reliability defects and keep them from becoming disasters later on in the field.

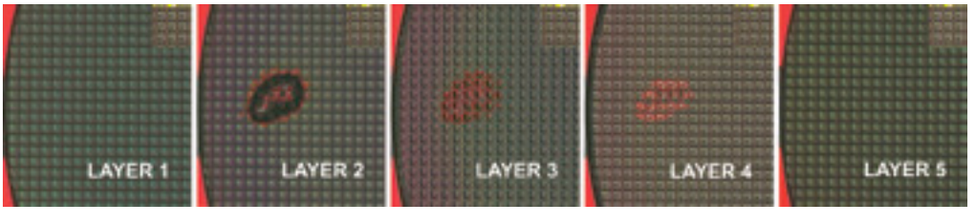


Figure 1. When defects are not flagged in time they can be covered over by subsequent process steps, often becoming invisible to later inspection.

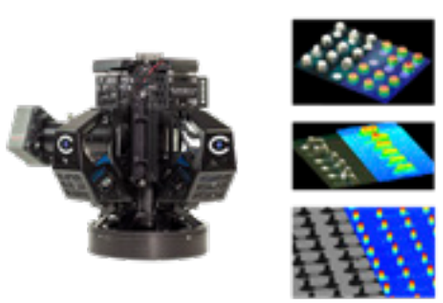
Semiconductor Digest and SEMI Announce the 2019 Best of West Award Winner

SEMI and Semiconductor Digest today announced the recipient of the 2019 "Best of West" Award. The award recognizes important product and technology developments in the electronics manufacturing supply chain. Held in conjunction with SEMICON West, the largest and most influential electronics manufacturing exposition in North America, the Best of West finalists were selected based on their financial impact on the industry, engineering or scientific achievement, and/or societal impact.

The winner is the CyberOptics NanoResolution MRS Sensor. The proprietary MRS sensor technology, deemed best-in-class, enables metrology-grade accuracy by inhibiting optical measurement distortions and reflections. CyberOptics' unique sensor architecture simultaneously captures and transmits multiple images in parallel while proprietary 3D fusing algorithms merge the images. The result is ultra-high quality 3D images and high-speed inspection.

"There's a big emphasis on metrology at this year's SEMICON West," said Pete Singer, Editor-in-Chief of Semiconductor Digest. "The CyberOptics MRS Sensor is a great example of a fantastic new tool now available to semiconductor manufacturers."

Congratulations to CyberOptics on their winning entry. The award will be presented during SEMICON West on Wednesday, July 10, 2019.



CyberOptics' Nanoresolution MRS Sensor

More than 23,000 professionals from the electronics manufacturing supply chain are expected to attend SEMICON West, the flagship event for the U.S. semiconductor industry. Learn more at www.semiconwest.org.

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