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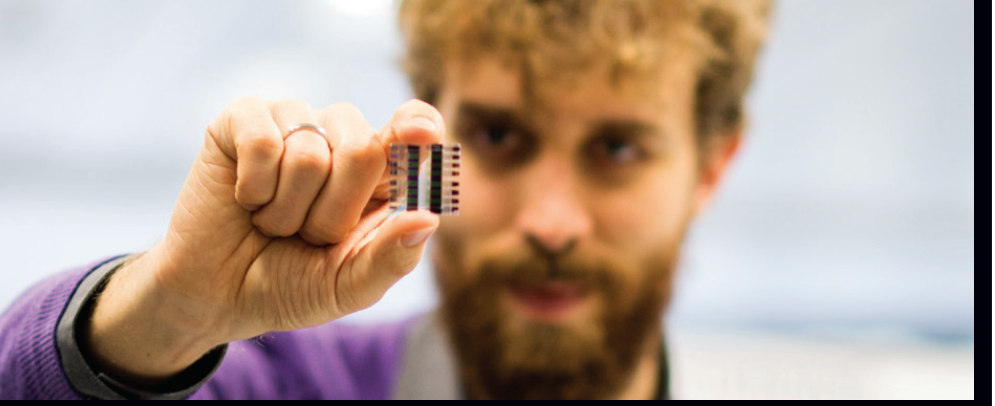

Solid State TECHNOLOGY®

APRIL/MAY 2018 VOL. 61 NO. 3

Caption: This month's cover story author Pawel Malinowski holds a test device used for investigation of high resolution patterning of OLEDs.

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editorial

Five reasons to attend The ConFab, May 20-23

The ConFab 2018 Conference and Networking Event will be held May 20-23 at The COSMOPOLITAN of Las Vegas. Presented by Solid State Technology, the event is designed exclusively for execs in the semiconductor industry. The focus of this year's event is the new wave of growth that is sweeping through the semiconductor industry, propelled by a vast array of new applications, including artificial intelligence, virtual and augmented reality, automotive, 5G, the IoT, cloud computing and healthcare, among others.

Here are five reasons to attend.

1. The Presentations: You'll hear from **IBM**'s Rama Divakaruni on A.I., **Google**'s John Martinis on quantum computing, **GlobalFoundries**' George Gomba on EUV, **Nvidia**'s John Hu on top industry drivers, **HERE**'s Rajeev Rajan on driving autonomous, **Qualcomm**'s Bill von Novack on wireless power in medical implants, and **Qorvo**'s Howard Witham on the use of A.I. in semiconductor manufacturing, to name a few.

2. The Panels. Our panel on Heterogeneous Integration, organized by **ASE**'s Bill Chen and **Cisco**'s Li Li will feature great panelists: David McCann, VP Packaging and Test, Dev. & Operations, **GlobalFoundries**; Xin Wu, Vice President – Silicon Technology, **Xilinx**; Dr. Meyya Meyyappan, Chief Scientist, **NASA** Ames Research Center, Rozalia Beica, Global Director, **Dow DuPont** and Bill Bottoms, Chairman, **3MTS**. For the first time, we'll also have two late afternoon panels, one focused on A.I., led by **BISTel**'s Tom Ho and another on trends in automotive electronics, led by **KLA-Tencor**'s Rob Cappel.

3. Dynamic networking. A big part of The ConFab is the networking. There are plenty of opportunities to get together at breakfast, lunch and for evening receptions. Wouldn't it be nice to get out and talk to old friends and meet some new ones, and find out what your peers are doing?

4. Strategic business meetings. We arrange strategic meetings between interested parties throughout the supply chain, focusing on bringing together IDMs, foundries, OSATs and fabless companies with suppliers of equipment and materials, components and services.

5. Las Vegas! The ConFab 2018 will take place at The COSMOPOLITAN of Las Vegas, a swanky, modern, upscale hotel in downtown Las Vegas with tons to offer.

The need for real collaboration has never been greater. Come to The ConFab 2018 and make it happen!

Register now by contacting Sally Bixby at sbixby@extensionmedia.com. Complimentary passes are available to qualified VIPs. You can also check out The ConFab website, www.theconfab.com. I hope to see you there!

—Pete Singer, Editor-in-Chief

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- Agenda: How AI is Driving the New Semiconductor Era, Quantum Supremacy: Checking a Quantum Computer with a Classical Supercomputer, Advances in Semiconductor Manufacturing, Deep Learning IC Industry Driven by AI, Internet of Things, Autonomous Driving and Virtual Reality, Enabling a Startup Ecosystem for Semiconductors, AI Potential in the Semiconductor Fab, Rise of the Technology Foundry, Wireless Power in Medical Implants, EUV in High-Volume Manufacturing, Heterogeneous Integration, Automotive Electronics, Emerging Tech Markets Fueling IC Growth, and more.
- The ConFab 2018 connects key decision-makers, clients, colleagues, partners, suppliers and analysts in conference sessions and multiple networking breakfasts, lunches, cocktail receptions and private meetings. Don't miss a valuable opportunity to meet face-to-face.

Presented by:

Solid State TECHNOLOGY®

The ConFab 2018
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Web Exclusives

Insights from the Leading Edge: IBM/DARPA IceCOOL program

As part of the DARPA ICECool program, seeking to develop appropriate cooling technologies for 3D chip stacks, IBM developed a new chip-embedded cooling approach, utilizing a nonconductive fluid, doing away with the need for a barrier between the chip electrical signals and the fluid.

https://bit.ly/2HpLQ6t

AI and MEMS sensors: A critical pairing

How can consumer-product manufacturers tap the built-in capabilities of MEMS inertial sensors -- which are already ubiquitous in end-user devices -- to make the most of AI?

https://bit.ly/2uWkrH5

Black swans unmasked and other stories from my days in San Jose – Further thoughts on 2018 SPIE AL EUVL conference

Stochastics effects, which are random and local variables, were in focus during the EUVL Conference this year.

https://bit.ly/2GMChS4

U.S. federal government R&D spending for 2018 finalized

Although many months past due, Congress on March 23 finalized the federal spending for the remainder of fiscal year (FY) 2018, only hours before a what would have been the third government shutdown of the year. Congressional spending has been allocated in fits and starts since the end of FY 2017 last September, with patchwork deals keeping things running amid pervasive uncertainty.

https://bit.ly/2H8B8nk

n&b news and blogs

What's next for smart speakers? Smart microphones

What's behind the smart speakers? Even smarter microphones. There are two different kinds of tiny microphones in our smart devices, including smartphones, smart home products and smart speakers – capacitive and piezoelectric MEMS (microelectro-mechanical systems) microphones.

https://bit.ly/2HcNOK0

2018 SPIE Advanced Lithography – EUVL Conference update

The 2018 SPIE Advanced Lithography meeting was held from February 25 to March 1, 2018 in San Jose, CA.

https://bit.ly/2EBY1u6

The ConFab 2018 announces conference agenda and speakers

In the 2018 program, we will take a close look at the new applications driving the semiconductor industry, the technology that will be required at the device and process level to meet new demands, and the kind of strategic collaboration that will be required. It is this combination of business, technology and social interactions that make the conference so unique and so valuable. Browse this slideshow for a look at this year's speakers, keynotes, panel discussions, and special guests.

https://bit.ly/2H9pJUp

SEMI reports record semiconductor photomask sales of $3.7B

SEMI announced that after several years of incremental increases the worldwide semiconductor photomask market surged 13 percent to a record high $3.75 billion in 2017 and is forecast to exceed $4.0 billion in 2019.

https://bit.ly/2HuiS5P

China now world's largest consumer of semiconductor packaging equipment and materials

Fueled by heavy government investment, IC packaging and testing in China generated $29 billion in revenue in 2017, making China the world's largest consumer of packaging equipment and materials.

https://bit.ly/2JCkc75

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BI02 The Future of Materials Science Academia—Preparing for a Career in Higher Education

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BM01 3D Printing of Passive and Active Medical Devices
BM02 Electronic and Coupled Transport in Biology
BM03 Multiscale Modeling of Soft Materials and Interfaces
BM04 Biomaterials for Regenerative Engineering
BM05 Advanced Manufacturing Technologies for Emulating Biological Tissues
BM06 Plasma Processing and Monitoring for Bioengineering and Biomedical Engineering
BM07 Bioelectronics—Fundamentals, Materials and Devices
BM08 Materials-to-Devices for Integrated Wearable Systems—Energy Harvesting and Storage, Sensors/Actuators and Integration
BM09 Bioinspired Macromolecular Assembly and Inorganic Crystallization—From Tissue Scaffolds to Nanostructured Materials

CHARACTERIZATION, MECHANICAL PROPERTIES AND STRUCTURE–PROPERTY RELATIONSHIPS

CM01 Solid-State Chemistry of Inorganic Materials
CM02 Structure–Property Relations in Non-Crystalline Materials
CM03 *In Situ/Operando* Analysis of Electrochemical Materials and Interfaces
CM04 Ultrafast Optical Probes for Advanced Materials Characterization and Development
CM05 Fundamentals of Materials Property Changes Under Irradiation

ELECTRONIC, PHOTONIC AND MAGNETIC MATERIALS

EP01 New Materials and Applications of Piezoelectric, Pyroelectric and Ferroelectric Materials
EP02 Materials for Manipulating and Controlling Magnetic Skyrmions
EP03 Beyond-Graphene 2D Materials—Synthesis, Properties and Device Applications
EP04 Novel Photonic and Plasmonic Materials Enabling New Functionalities
EP05 Excitons, Electrons and Ions in Organic Materials
EP06 Coherent Electronic Spin Dynamics in Materials and Devices
EP07 Tailored Disorder—Novel Materials for Advanced Optics and Photonics
EP08 Ultra-Wide-Bandgap Materials and Devices
EP09 Diamond Electronics, Sensors and Biotechnology—Fundamentals to Applications

ENERGY—TRANSFER, STORAGE AND CONVERSION

ET01 Solid-State Batteries—Materials, Interfaces and Performance
ET02 Silicon for Photovoltaics
ET03 Application of Nanoscale Phenomena and Materials to Practical Electrochemical Energy Storage and Conversion
ET04 Perovskite Solar Cells—Challenges and Opportunities
ET05 Fundamental Aspects of Halide Perovskite (Opto)electronics and Beyond
ET06 Advanced Materials and Chemistries for High-Energy and Safe Rechargeable Batteries
ET07 Advanced Processing and Manufacturing for Energy Conversion, Storage and Harvesting Devices
ET08 Emerging Materials and Characterization for Selective Catalysis
ET09 Materials for Chalcogen Electrochemistry in Energy Conversion and Storage
ET10 Redox Active Materials and Flow Cells for Energy Applications
ET11 Emerging Materials and Device Concepts for Flexible, Low-Cost Photovoltaic Technologies
ET12 Harvesting Functional Defects in Energy Materials
ET13 Materials for Multifunctional Windows
ET14 Materials Science Facing Global Warming—Practical Solutions for Our Future
ET15 Scientific Basis for Nuclear Waste Management

GENERAL INTEREST

GI01 Machine Learning and Data-Driven Materials Development and Design
GI02 Materials for Next-Generation Robotics

NANOMATERIALS

NM01 Carbon Nanotubes, Graphenes and Related Nanostructures
NM02 Nanometal—Synthesis, Properties and Applications
NM03 Nanowires and Related 1D Nanostructures—New Opportunities and Grand Challenges
NM04 Nanomaterials and Nanomanufacturing for Sustainability

PROCESSING AND MANUFACTURING

PM01 Architected Materials—Synthesis, Characterization, Modeling and Optimal Design
PM02 Conductive Materials Reliability in Flexible Electronics
PM03 Hierarchical, Hybrid and Roll-to-Roll Manufacturing for Device Applications
PM04 High-Entropy Alloys
PM05 Electromagnetic Fields in Materials Synthesis—Far from Equilibrium Effects
PM06 Advances in Intermetallic-Based Alloys for Structural and Functional Applications
PM07 Plasma-Based Synthesis, Processing and Characterization of Novel Materials for Advanced Applications

THERMAL PROPERTIES AND THERMOELECTRIC MATERIALS

TP01 Caloric Materials for Highly Efficient Cooling Applications
TP02 Thermal Analysis—Materials, Measurements and Devices
TP03 Emerging Low-Temperature Thermal Energy Conversion Technologies

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EUROPE – **imec** and **Qromis** presented high performance p-GaN HEMTs on 200mm CTE-matched substrates.

USA - **ON Semiconductor** announced its 2017 Supplier Award winners.

EUROPE – **Plasma-Therm** announced that it has acquired **KOBUS**, a plasma deposition company.

ASIA - **Samsung Electronics** diversified its 8-inch foundry offerings with new RF/IoT and fingerprint technology solutions.

USA - **Broadcom** withdrew its offer to acquire Qualcomm, after the Trump administration sent an Order to block the merger.

EUROPE - **UnitySC** acquired **HSEB Dresden GMBH**.

USA - **Veeco** achieved a milestone with 100 automated MBE systems installed worldwide.

EUROPE - **Leti** announced its silicon photonics process design kit (PDK) for photonic circuits is available in the Synopsys PhoeniX OptoDesigner suite.

USA - **Synopsys** acquired **Silicon and Beyond Private Limited**.

EUROPE - **EV Group** and **IBM** signed a license agreement on laser debonding technology.

With its highest growth rate in 14 years, the global semiconductor industry topped $429B in 2017

The semiconductor industry closed out 2017 in blockbuster fashion, posting the highest year-over-year growth in 14 years. Global semiconductor revenue grew 21.7 percent, reaching $429.1 billion in 2017, according to IHS Markit (Nasdaq: INFO).

Recording year-over-year growth of 53.6 percent, and its highest semiconductor revenue ever, Samsung replaced Intel as the new market leader of the semiconductor industry in 2017. Intel was followed by SK Hynix, in third position.

"2017 was quite a memorable year," said Shaun Teevens, semiconductor supply chain analyst, IHS Markit. "Alongside record industry growth, Intel, which had led the market for 25 years, was supplanted by Samsung as the leading semiconductor supplier in the world."

Among the top 20 semiconductor suppliers, SK Hynix and Micron enjoyed the largest year-over-year revenue growth, growing 81.2 percent and 79.7 percent, respectively. "A very favorable memory market with strong demand and high prices was mainly responsible for the strong growth of these companies," Teevens said.

Qualcomm remained the top fabless company in 2017, followed by nVidia, which moved into the second position, after growing 42.3 percent over the previous year. Among the top 20 fabless companies, MLS enjoyed the highest market share gain, moving from number 20 to number 15 in the IHS Markit revenue ranking.

Memory was the strongest industry category

Memory integrated circuits proved to be the strongest industry category, growing 60.8 percent in 2017 compared to the previous year. Within the category, DRAM grew 76.7 percent and NAND grew 46.6 percent — the highest growth rate for both memory subcategories in 10 years. Much of the revenue increase was based on higher prices and increased demand for memory chips, relative to tight supply.

"The technology transition from planar 2D NAND to 3D NAND drove the market into an unbalanced supply-demand environment in 2017, driving prices higher throughout the year," said Craig Stice, senior director, memory and storage, IHS Markit. "Entering 2018, the 3D NAND transition is now almost three-quarters of the total bit percent of production, and it is projected to provide supply relief for the strong demand coming from the SSD and mobile markets. Prices are expected to begin to decline aggressively, but 2018 could still be a record revenue year for the NAND market."

Excluding memory, the remainder of the semiconductor industry grew 9.9 percent last year, largely due to solid unit-sales growth and strong demand across all applications, regions and technologies. Notably, semiconductors used for data processing applications expanded 33.4 percent by year-end. Intel remained the market leader in this category, with sales almost two times larger than second-ranked Samsung.

Worldwide Ranking of the Top-10 Suppliers of Semiconductors in 2017
(Ranking by Revenue in Millions of U.S. Dollars)

2016 Rank	2017 Rank	Company Name	2016 Revenue($)	2017 Revenue($)	Revenue Percent Change	Revenue Percent of Total	Revenue Cumulative Percent
2	1	Samsung Electronics	40,389	62,031	53.6%	14.5%	14.5%
1	2	Intel	54,980	61,406	11.7%	14.3%	28.8%
5	3	SK Hynix	14,699	26,638	81.2%	6.2%	35.0%
7	4	Micron Technology	12,710	22,843	79.7%	5.3%	40.3%
4	5	Broadcom Limited	14,979	17,375	16.0%	4.0%	44.3%
3	6	Qualcomm	15,405	16,872	9.5%	3.9%	48.3%
6	7	Texas Instruments	12,836	14,525	13.2%	3.4%	51.7%
8	8	Toshiba	9,904	11,864	19.8%	2.8%	54.4%
9	9	NXP	9,306	8,864	-4.7%	2.1%	56.5%
13	10	nVidia	6,030	8,578	42.3%	2.0%	58.5%
		Top 10 Companies	**191,238**	**250,996**	**31.2%**	**58.5%**	
		All Others	**161,356**	**178,112**	**10.4%**	**41.5%**	
		Total Semiconductor	**352,594**	**429,108**	**21.7%**	**100.0%**	

Source: IHS Markit Q1 2018 Competitive Landscaping Tool

U.S. companies maintain largest share of fabless company IC sales

Research included in the March Update to the 2018 edition of IC Insights' McClean Report shows that fabless IC suppliers accounted for 27% of the world's IC sales in 2017—an increase from 18% ten years earlier in 2007. As the name implies, fabless IC companies do not operate an IC fabrication facility of their own.

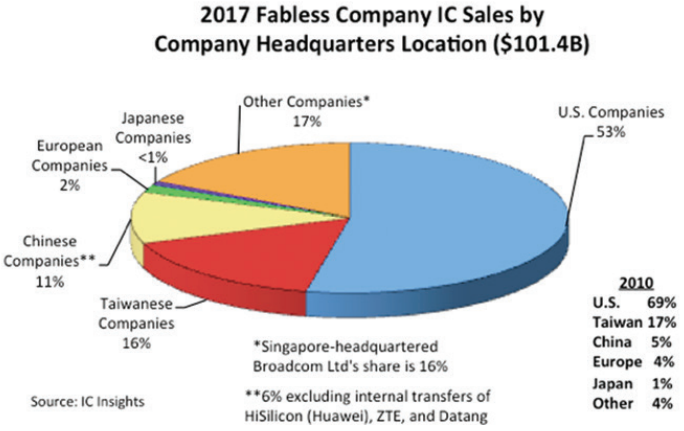


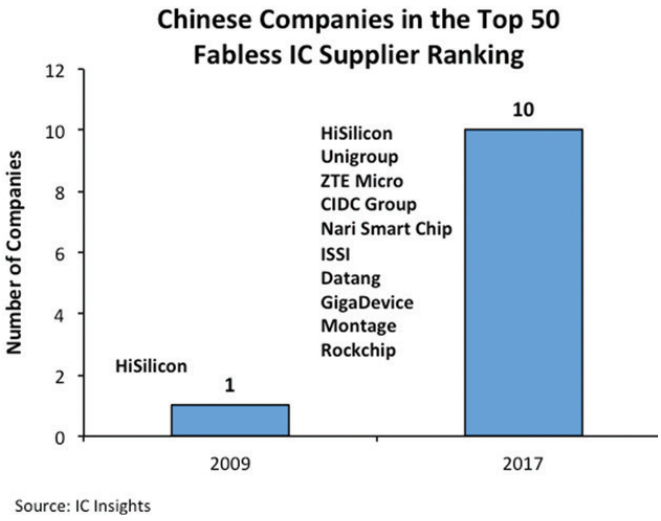
Figure 1 shows the 2017 fabless company share of IC sales by company headquarters location. At 53%, U.S. companies accounted for the greatest share of fabless IC sales last year, although this share was down from 69% in 2010 (due in part to the acquisition of U.S.-based Broadcom by Singapore-based Avago). Broadcom Limited currently describes itself as a "co-headquartered" company with its headquarters in San Jose, California and Singapore, but it is in the process of establishing its headquarters entirely in the U.S. Once this takes place, the U.S. share of the fabless companies IC sales will again be about 69%.

Taiwan captured 16% share of total fabless company IC sales in 2017, about the same percentage that it held in 2010. MediaTek, Novatek, and Realtek each had more than $1.0 billion in IC sales last year and each was ranked among the top-20 largest fabless IC companies.

China is playing a bigger role in the fabless IC market. Since 2010, the largest fabless IC marketshare increase has come from the Chinese suppliers, which captured 5% share in 2010 but represented 11% of total fabless IC sales in 2017. Figure 2 shows that 10 Chinese fabless companies were included in the top-50 fabless IC supplier list in 2017 compared to only one company in 2009. Unigroup was the largest Chinese fabless IC supplier (and ninth-largest global fabless supplier) in 2017 with sales of $2.1 billion. It is worth noting that when excluding the internal transfers of HiSilicon (over 90% of its sales go to its parent company Huawei), ZTE, and Datang, the Chinese share of the fabless market drops to about 6%.

Continued on page 8

U.S. companies ... , *Continued from page 7*



Source: IC Insights

European companies held only 2% of the fabless IC company marketshare in 2017 as compared to 4% in 2010. The loss of share was due to the acquisition of U.K.-based CSR, the second-largest European fabless IC supplier, by U.S.-based Qualcomm in 1Q15 and the purchase of Germany-based Lantiq, the third-largest European fabless IC supplier, by Intel in 2Q15. These acquisitions left U.K.-based Dialog ($1.4 billion in sales in 2017) and Norway-based Nordic ($236 million in sales in 2017) as the only two European-based fabless IC suppliers to make the list of top-50 fabless IC suppliers last year.

The fabless IC business model is not so prominent in Japan or in South Korea. Megachips, which saw its 2017 sales jump by 40% to $640 million, was the largest Japan-based fabless IC supplier. The lone South Korean company among the top-50 largest fabless suppliers was Silicon Works, which had a 15% increase in sales last year to $605 million.

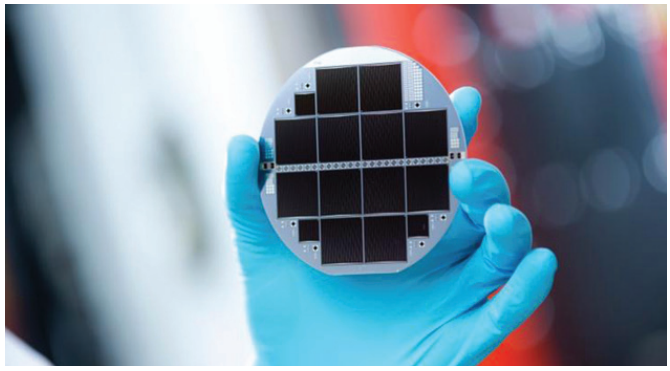
Fraunhofer ISE and EV Group achieve 33.3% efficiency with silicon-based multi-junction solar cell

Silicon solar cells dominate the global photovoltaic market today with a share of 90 percent. With ever new technological developments, research and industry are nearing the theoretical efficiency limit for semiconductor silicon. At the same time, they are forging new paths to develop a new generation of even more efficient solar cells.

The Fraunhofer researchers achieved the high conversion efficiency of the silicon-based multi-junction solar cell with extremely thin 0.002 mm semiconductor layers of III-V compound semiconductors, bonding them to a silicon solar cell. To compare, the thickness of these layers is less than one twentieth the thickness of a human hair. The visible sunlight is absorbed in a gallium-indium-phosphide (GaInP) top cell, the near infrared light in gallium-arsenide (GaAs) and the longer wavelengths in the silicon subcell. In this way, the efficiency of silicon solar cells can be significantly increased.

"Photovoltaics is a key pillar for the energy transformation," says Dr. Andreas Bett, Institute Director of Fraunhofer ISE. "Meanwhile, the costs have decreased to such an extent that photovoltaics has become an economically viable competitor to conventional energy sources. This development, however, is not over yet. The new result shows how material consumption can be reduced through higher efficiencies, so that not only the costs of photovoltaics can be further optimized but also its manufacture can be carried out in a resource-friendly manner.

Already in November 2016, the solar researchers in Freiburg together with their industry partner EVG demonstrated an efficiency of 30.2 percent, increasing it to 31.3 percent in March 2017. Now they have succeeded once again in greatly improving the light absorption and the charge separation in silicon, thus achieving a new record of 33.3 percent efficiency. The technology also convinced the jury of the GreenTec Awards 2018 and has been nominated among the top three in the category "Energy."



Silicon-based multi-junction solar cell consisting of III-V semiconductors and silicon. The record cell converts 33.3 percent of the incident sunlight into electricity.
© Fraunhofer ISE/Photo: Dirk Mahler

The Technology

For this achievement, the researchers used a well-known process from the microelectronics industry called "direct wafer bonding" to transfer III-V semiconductor layers, of only 1.9 micrometers thick, to silicon. The surfaces were deoxidized in a EVG580® ComBond® chamber under high vacuum with a ion beam and subsequently

bonded together under pressure. The atoms on the surface of the III-V subcell form bonds with the silicon atoms, creating a monolithic device. The complexity of its inner structure is not evident from its outer appearance: the cell has a simple front and rear contact just as a conventional silicon solar cell and therefore can be integrated into photovoltaic modules in the same manner.

The III-V / Si multi-junction solar cell consists of a sequence of subcells stacked on top of each other. So-called "tunnel diodes" internally connect the three subcells made of gallium-indium-phosphide (GaInP), gallium-arsenide (GaAs) and silicon (Si), which span the absorption range of the sun's spectrum. The GaInP top cell absorbs radiation between 300 and 670 nm. The middle GaAs subcell absorbs radiation between 500 and 890 nm and the bottom Si subcell between 650 and 1180 nm, respectively. The III-V layers are first epitaxially deposited on a GaAs substrate and then bonded to a silicon solar cell structure. Here a tunnel oxide passivated contact (TOPCon) is applied to the front and back surfaces of the silicon. Subsequently the GaAs substrate is removed, a nanostructured backside contact is implemented to prolong the path length of light. A front side contact grid and antireflection coating are also applied.

On the way to the industrial manufacturing of III-V / Si multi-junction solar cells, the costs of the III-V epitaxy and the connecting technology with silicon must be reduced. There are still great challenges to overcome in this area, which the Fraunhofer ISE researchers intend to solve through future investigations. Fraunhofer ISE's new Center for High Efficiency Solar Cells, presently being constructed in Freiburg, will provide them with the perfect setting for developing next-generation III-V and silicon solar cell technologies. The ultimate objective is to make high efficiency solar PV modules with efficiencies of over 30 percent possible in the future.

Project Financing

Dr. Roman Cariou, the young scientist and first author, was supported through the European Union with a Marie Curie Stipendium (HISTORIC, 655272). The work was also supported by the European Union within the NanoTandem project (641023) as well as by the German Federal Ministry for Economic Affairs and Energy BMWi in the PoTaSi project (FKZ 0324247).

AI vs IoT

PHIL GARROU,
Contributing Editor

AI and IoT both buzz words that are predicted to drive the electronics industry over the next decade. I am bullish on AI, not so much on IoT. As I have explained before my opinion is formed from a packaging perspective and while I think AI will need all the latest high end packaging solutions, I still perceive that most IoT will require the absolute lowest cost, stripped down packaging available. AI platforms are an intimate combination of hardware and software but certainly will be requiring the latest that we have to offer in high end packaging solutions.

AI processing will go into home control devices, autos, surveillance systems, airplanes, wearables and things we have yet to think of. AI processing is unique in that traditional customers Amazon, Google and Apple, have begun to design their own AI chips, in hopes of differentiating their products from those of rivals. This has major ramifications for companies like Intel and Nvidia, which will now be competing with their customers.

While I certainly am not an AI expert, we all must quickly up our knowledge in this area which I see leading advanced packaging into the next decade.

While cloud companies like Google appear to be favoring custom chips to augment CPUs and GPUs, semiconductor and IP companies are designing chips to enable efficient hardware and neural net systems and Intel is proposing an open platform ecosystem based on Xeon, FPGAs, and specialized processors like Nervana and Saffron.

Google's Tensor Processing Unit (TPU), was introduced last year. Their initial beta customer Lyft, is using AI to recognize surroundings, locations, street signs etc. The cloud-based TPU features 180 teraflops of floating-point performance through four ASICS with 64 GB of high bandwidth memory. These modules can be used alone or connected together via a dedicated network to form multi-petaflop ML supercomputers that they call TPU pods.

The best known mobile AI processor is included in the Apple iPhone X. Apple's A11 is a 64-bit ARM 6 core CPU with two high performance 2.39 GHz cores called Monsoon, and four energy efficient cores, call Mistral. The A11's performance controller gives the chip access to all six cores simultaneously. The A11 has three-core GPU by Apple, the M11 motion coprocessor, an image processor supporting computational photography, and the new Neural Engine that comes into play for Face ID and other machine learning tasks.

Amazon is reportedly developing a chip designed for artificial intelligence to work with the Echo and other hardware powered by Amazon's Alexa virtual assistant. The chip should allow Alexa-powered devices to respond more quickly to commands, by allowing more data processing to be handled on the device vs the cloud.

Nvidia has announced its new Volta GPU with 640 tensor cores, which delivers over 100 Teraflops. It has been adopted by leading cloud suppliers including Amazon, Microsoft, Google, Oracle , and others. On the OEM side, Dell EMC, HP, Huawei, IBM and Lenovo have all announced Volta-based offerings for their customers.

Microsoft has teamed with Intel and is offering their Stratix 10 FPGAS for AI processing on Microsoft Azure (see below) codename "Brainwave." Intel is proposing FPGAs + processors for AI work. Intel is reportedly focusing on the Stratix X FPGA as a AI companion to Intel's Xeon processors.

Intel's 14 nm Stratix 10 FPGAs accelerate Microsoft's Azure deep learning platform using FPGAs with "soft" Deep Neural Network (DNN) units synthesized onto the FPGAs instead of hardwired Processing Units (DPUs). Brainwave is designed for live data streams including video, sensor feeds, and search queries.

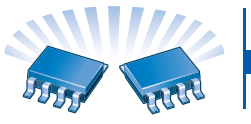
Intel is making a major play in AI. Intel has multiple processor options for AI, including Xeon, FPGAs, Nervana, Movidius, and Saffron.

Saffron Technology was acquired by Intel in 2015. It develops "..cognitive computing systems that use incremental learning to understand and unify by entity (person, place or thing) the connections between an entity and other "things" in data, along with the context of their connections and their raw frequency counts.... Saffron learns from all sources of data including structured and unstructured data to support knowledge-based decision making." It is being used extensively in the financial services industry.

In 2016, Intel announced acquired Nervana, a startup developing AI software and hardware for machine learning. In 2017, Intel revealed the Nervana Neural Network Processor (NNP) designed expressly for AI and deep learning.

It will be interesting to see hope the packaging community develops solutions that will be compatible with these advanced high speed HPC applications.

Packaging



Novel chip enables disease detection

A novel invention by a team of researchers from the National University of Singapore (NUS) holds promise for a faster and cheaper way to diagnose diseases with high accuracy. Professor Zhang Yong from the Department of Biomedical Engineering at the NUS Faculty of Engineering and his team have developed a tiny microfluidic chip that could effectively detect minute amounts of biomolecules without the need for complex lab equipment.

Diseases diagnostics involves detection and quantification of nano-sized bio-particles such as DNA, proteins, viruses, and exosomes (extracellular vesicles). Typically, detection of biomolecules such as proteins are performed using colorimetric assays or fluorescent labelling with a secondary antibody for detection, and requires complex optical detection equipment such as fluorescent microscopy or spectrophotometry.

One alternative to reduce cost and complexity of disease detection is the adoption of label-free techniques, which are gaining traction in recent times. However, this approach requires precision engineering of nano-features (in a detection chip), complex optical setups, novel nano-probes (such as graphene oxide, carbon nanotubes, and gold nanorods) or additional amplification steps such as aggregation of nanoparticles to achieve sensitive detection of biomarkers.

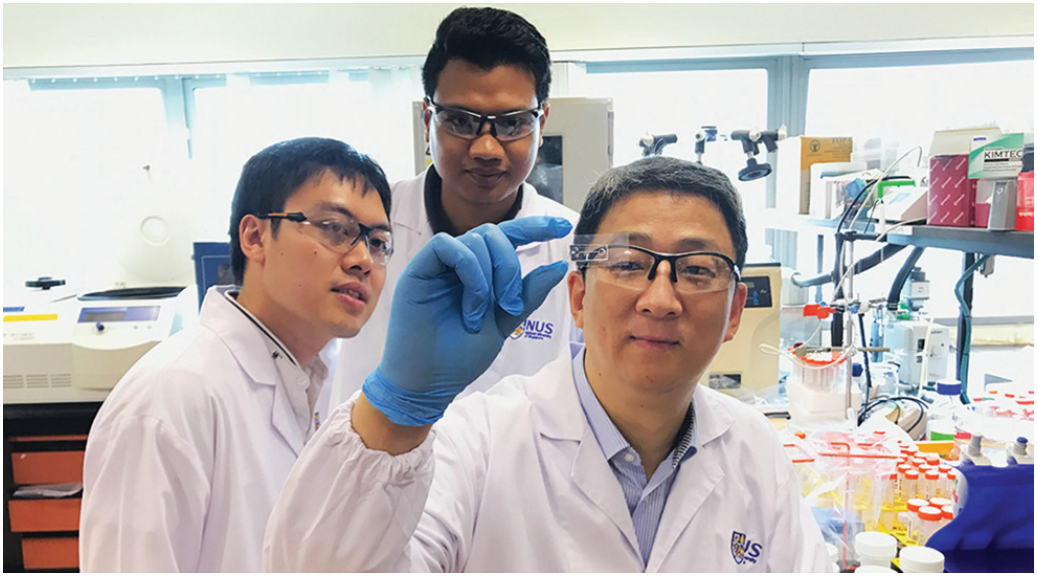
"Our invention is an example of disruptive diagnostics. This tiny biochip can sensitively detect proteins and nano-sized polymer vesicles with a concentration as low as 10ng/mL (150 pM) and 3.75µg/mL respectively. It also has a very small footprint, weighing only 500 mg and is 6mm^3 in size. Detection can be performed using standard laboratory microscopes, making this approach highly attractive for use in point-of-care diagnostics," explained Prof Zhang.

His team, comprising Dr Kerwin Kwek Zeming and two NUS PhD students Mr Thoriq Salafi and Ms Swati Shikha, published their findings in scientific journal Nature Communications on 28 March 2018.

Novel approach for disease diagnosis

This novel fluorescent label-free approach uses the lateral shifts in the position of the microbead substrate in pillar arrays, for quantifying the biomolecules, based on the change in surface forces and size, without the need of any external equipment. Due to the usage of lateral displacement, the nano-biomolecules can be detected in real-time and the detection is significantly faster in comparison to fluorescent label based detection.

"These techniques can also be extended to many other types of nano-biomolecules, including nucleic acid and virus detection. To complement this chip technology, we are also developing a portable smartphone-based accessory and microfluidic pump to make the whole detection platform portable for outside laboratory disease diagnostics. We hope to further develop this technology for commercialization," said Prof Zhang.



Semiconductors

NUS Engineering researchers have developed a low-cost microfluidic chip that can quickly and accurately detect and quantify nano-bioparticles using only a standard laboratory microscope without any fluorescent labels.

Photolithography for high resolution OLED displays

PAWEL MALINOWSKI *and* **TUNGHUEI KE**, *imec, Leuven, Belgium*

Photolithography of organic semiconductors is an emerging technology that can enable high resolution OLED displays.

Modern society has grown accustomed to an overflow of visual information, with displays in the center of most user interfaces. The pace of introducing new technologies and of reducing cost of manufacturing has been impressive and does not seem to slow down. The most prominent examples are OLED displays (based on organic light emitting diodes), evolving from a curiosity only some years ago to a technology that is dominating the market position today. 2017 has seen major increase in both shipments (more than 400 million units) and revenue (around $25 billion) for AMOLED display panels (according to UBI Research and DSCC).

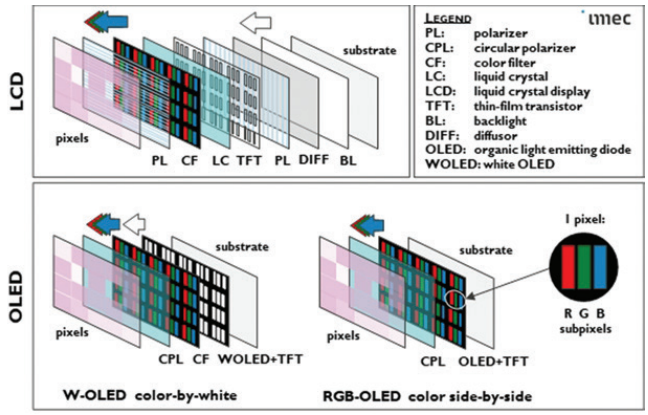


FIGURE 1. LCD vs. OLED displays.

From the very beginning of OLED history, it was crucial to find a way to maintain efficient emission in stacks composed of very fragile materials. As most of the materials used in an OLED structure are highly sensitive to a lot of elements (e.g., air, moisture, solvents, temperature, radiation), protecting the device has always been crucial, both during fabrication and during operation. This has evolved into several research tracks. Firstly, great effort by material companies to synthesize new molecules and polymers resulted in many OLED families, both for thermal evaporation and solution processing. Secondly, equipment advances made it possible to uniformly deposit stacks on large substrates with industrial takt time. Thirdly, different encapsulations were developed to protect the OLED stack during usage to ensure enough lifetime for consumer applications. All of the above required years of research and significant investments, which makes it challenging to introduce new OLED manufacturing techniques and change the existing process flows.

At the same time, current manufacturing methods have their limitations. Two main approaches are color-by-white (WOLED) and side-by-side red-green-blue (RGB OLED), differing by the way that the colors are realized in subpixels (**FIGURE 1**). In WOLED, the light source is a continuous layer of a broadband (white) OLED emitter and the three basic colors are selected by passing the light through color filters (CF). The advantage is that the pixel density is limited only by the backplane resolution and the CF resolution, which is why this is the main concept used for OLED microdisplays with CMOS circuitry. The disadvantage is that significant portion of the light is lost due to CF absorption, which impacts the display power efficiency. In RGB OLED, each subpixel is a different material stack, so each subpixel is a separate light emitter. This is typically realized by depositing each stack by thermal evaporation through a fine metal mask (FMM) and is used for most smartphone OLED displays. The advantage is that each color is optimized, so the display efficiency is much higher. At the same time, it is difficult to scale the FMM technique both in substrate size (masks tend to bend under their own weight, so the motherglass has to be cut for OLED deposition) and in resolution (standard masks are not suitable for resolutions above several hundred ppi and the cross-fading area limits the aperture ratio).

An alternative way to realize side-by-side RGB pixels is to use photolithography techniques known very well from the semiconductor industry (and used in displays for the TFT backplane fabrication). In such case, after depositing a blanket OLED stack, photoresists could be

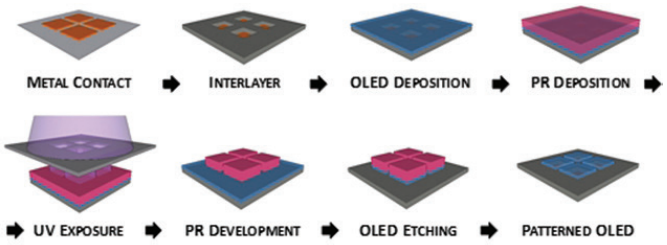


FIGURE 2. Patterning with photolithography process.

used to transfer the pattern and remove the unnecessary material by etching (**FIGURE 2**). The challenge here is, again, susceptibility of OLED materials to solvents – using standard (semiconductor) photoresist chemistry results in dissolution/removal of the stack. Still, the gains are definitely worth the extra effort, as litho can provide both very high pixel density (submicron pixel pitch) and, at the same time, very high aperture ratio (emitting area maximized thanks to minimizing pixel spacing). Over the years, some new approaches for photolithography have been proposed. One way, followed by Orthogonal Inc, is to use fluorinated materials which should not have any chemical interaction with the organic stacks (thus, orthogonal to OLED). The other approach, followed by imec together with Fujifilm, is to pattern organic stacks using a non-fluorinated, chemically amplified photoresist system.

For imec, R&D hub with long traditions of developing new photolithography nodes, organic photolithography is a way to address the challenges of next-generation high resolution displays. In virtual and augmented reality (VR/AR) applications, the display is very near to the eye of the user. This results in very aggressive requirements in terms of pixel density in order to avoid annoying "pixilation." The same goes for required minimum pixel spacing, to avoid "screen door effect". With photolithography, these two challenges can be addressed simultaneously. The OSR photoresist system from Fujifilm can deliver lines and spaces with 1 µm pitch, which fits in the roadmap towards several thousand ppi resolution for the OLED frontplane. We have realized a dot pattern transfer to OLED emission layer with 3 µm pitch, which corresponds to 8400 ppi resolution in a monochrome array. After stripping off the photoresist, the EML remains on the substrate, as verified by photoluminescence (**FIGURE 3**).

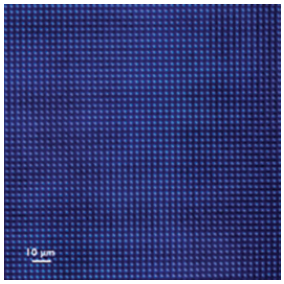


FIGURE 3. 3 µm pixel pitch (photoluminescence).

On the device level, we have fabricated OLED arrays with 10 µm pixel pitch (**FIGURE 4**), corresponding to 2500 ppi. In this case, an important parameter is the alignment accuracy, which

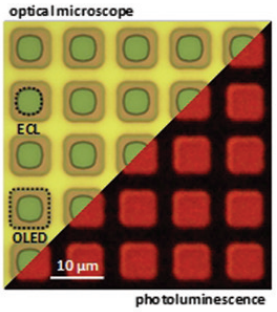


FIGURE 4. OLED arrays with single color and 10 um subpixel pitch.

defines how much of the total display area can be used for emission. Another limitation is the resolution of the PDL (pixel definition layer), a dielectric layer separating the OLED stack from the bottom contact level. The resolution of this layer limits the maximum opening that can be achieved, which translates to the aperture ratio of the pixel – or the percentage of the area that is used for OLED emission. In this example, the "photoluminescence aperture ratio", or the relation of the OLED island to the pixel area is around 50%, which is enabled by small spacing (<3 µm). However, the "electroluminescence aperture ratio", of the relation of the area emitting light, is 25% because of the PDL area and the necessary overlap of the OLED island. Assuming minimum line spacing of 1 µm, one can envision PL ratio of 81% (9 x 9 µm) and EL ratio of 64% (8 x 8 µm) for a subpixel of 10 x 10 µm. With such scaling, the usable area of the array can be enlarged, which results in longer device lifetime (since we can reduce the driving current density) and in reduction or elimination of the screen-door effects.

Obviously, interrupting the optimum deposition process in ultra-high vacuum and exposing the OLED stack to photolithography materials has an impact on the device performance. Just breaking the vacuum results in a hit on lifetime performance. Additionally, our initial process flow includes exposure of the stack to ambient atmosphere (air and humidity), as we have been using standard cleanroom equipment. In the beginning, such "worst case scenario" resulted in proof-of-concept of emitting OLEDs after patterning, but, unsurprisingly, with device lifetime of only few minutes. In the course of the development, we have introduced improvements on three fronts. Firstly, there have been continuous upgrades of the photoresist system to make it more compatible with the organic stack. Secondly, the process flow has been optimized to reduce the impact of process parameters on device performance. Thirdly, the OLED stacks have been tuned for robustness, for example by introducing additional protection layers for the most critical interfaces. All these actions resulted in device lifetimes of several hundred hours at 1000 nit luminance. As the lifetime is the major concern when it comes to the readiness of this technology, this is an ongoing effort to bring all the parameters to a level acceptable by the industry.

In parallel to performance improvement, we have been developing a route for patterning of multicolor arrays with photolithography. The main challenge in this case is to protect the previous "color" (OLED stack) while patterning the next one. Once this condition is satisfied, side-by-side arrays with several stacks can be realized – and, this is not limited to light emitters. Next to red-green-blue OLEDs, for example an organic photodetector subpixel could be fabricated to add functionality to the display. In terms of manufacturing, each "color" of the frontplane would be fabricated in a similar way as it is done for each layer of the backplane.

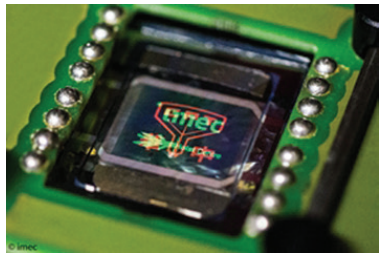


FIGURE 5. Prototype passive OLED display with pixels patterned by photolithography.

In our recent work, we fabricated a 2-color passive OLED display and this prototype was demonstrated at the Touch Taiwan 2017 exhibition (**FIGURE 5**). The 1400 x 1400 pixel array has a subpixel pitch of 10 µm, resulting in a resolution of 1250 ppi. The stacks are phosphorescent red and green small molecule OLEDs, deposited by thermal evaporation. The display is designed for top emission and uses glass encapsulation. Thanks to the separate driving of two groups of subpixels, the two colors can be displayed independently. The prototype has been in operation for tens of hours with all pixels turned on, with no visible degradation. This indicates that the process flow for multicolor patterning proves basic functionality and already ensures stability for reasonable working time. A similar frontplane can be integrated with a TFT or CMOS backplane, enabling then video mode of operation, with individual driving of each subpixel. In a separate demonstration, we have also verified that the fabrication process is compatible with a FPD backplane process using IGZO TFT and flexible substrate.

Taking everything into account, photolithography of organic semiconductors is an emerging technology that can enable high resolution OLED displays. Many technology milestones have been already cleared – we know that we can achieve patterns of few microns, realize side-by-side multicolor pixels, integrate the pixelated frontplane on different backplanes, and get encouraging efficiency and lifetime performance. Currently, optimization of OLED performance after patterning is still the top priority. At the same time, we are addressing the complete integration flow and manufacturability aspects. To have this technology fully incorporated in a fab process flow, material and equipment developments are required. Still, the prospect of ultra-high resolution with simultaneous high aperture ratio in a process flow based on standard semiconductor techniques remains very attractive and justifies going the extra mile to tackle the pending engineering challenges. ◆

Gases: Essential materials for display manufacturing

EDDIE LEE, *Linde Electronics, Hsinchu, Taiwan*

Technology trends in backplane technology are driving higher gas demand in display manufacturing. Specific gas requirements of process blocks are discussed, and various supply modes are reviewed.

Since its initial communalization in the 1990s, active matrix thin-film-transistor (TFT) displays have become an essential and indispensable part of modern living. They are much more than just televisions and smartphones; they are the primary communication and information portals for our day-to-day life: watches (wearables), appliances, advertising, signage, automobiles and more.

There are many similarities in the display TFT manufacturing and semiconductor device manufacturing such as the process steps (deposition, etch, cleaning, and doping), the type of gases used in these steps, and the fact that both display and semiconductor manufacturing both heavily use gases.

However, there are technology drivers and manufacturing challenges that differentiate the two. For semiconductor device manufacturing, there are technology limitations in making the device increasingly smaller. For display manufacturing, the challenge is primarily maintaining the uniformity of glass as consumers drive the demand for larger and thinner displays.

While semiconductor wafer size has maxed because of the challenges of making smaller features uniformly across the surface of the wafer, the size of the display mother glass has grown from 0.1m x 0.1m with 1.1mm thickness to 3m x 3m with 0.5mm thickness over the past 20 years due to consumer demands for larger, lighter, and more cost-effective devices.

As the display mother glass area gets bigger and bigger, so does the equipment used in the display manufacturing process and the volume of gases required. In addition, the consumer's desire for a better viewing experience such as more vivid color, higher resolution, and lower power consumption has also driven display manufacturers to develop and commercialize active matrix organic light emitting displays (AMOLED).

Technology

Layers of display device

In general, there are two types of displays in the market today: active matrix liquid crystal display (AMLCD) and AMOLED. In its simplicity, the fundamental components required to make up the display are the same for AMLCD and AMOLED. There are four layers of a display device (**FIGURE 1**): a light source, switches that are the thin-film-transistor and where the gases are mainly used, a shutter to control the color selection, and the RGB (red, green, blue) color filter.

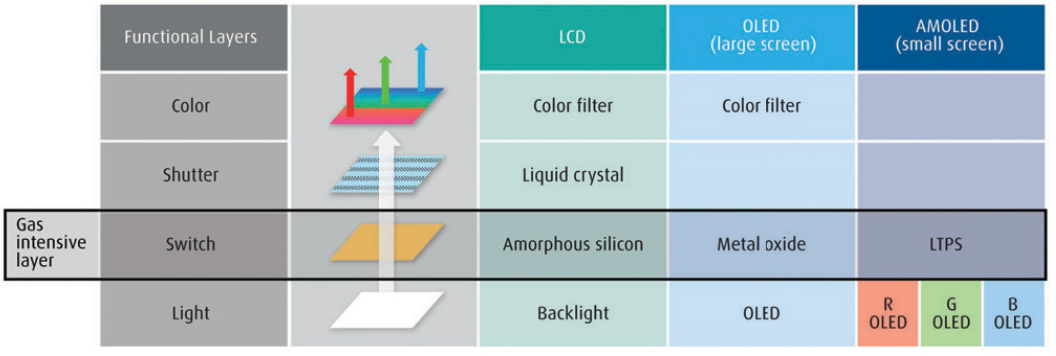


FIGURE 1. Function and composition of thin-film display devices

About backplane/TFT

The thin-film-transistors used for display are 2D transitional transistors, which are similar to bulk CMOS before FinFET. For the active matrix display, there is one transistor for each pixel to drive the individual RGB within the pixel. As the resolution of the display grows, the transistor size also reduces, but not to the sub-micron scale of semiconductor devices. For example, the transistor size for a smart watch with 325 PPI pixel density is 2mm^2; for a 4K TV with 80 PPI pixel density, it is 8mm^2.

	a-Si	Metal Oxide	LTPS
Electron mobility (m^2/Vs)	<1	1 – 50 (typically 5 – 10)	50 – 300
Cost	Low	Low	High
Manufacturing challenges	Low	High	Medium

FIGURE 2. Mobility comparison of a-Si, MO, and LTPS devices

	a-Si	Metal Oxide	LTPS
TFT uniformity (Gen8)	Good	Good	Poor
Manufacturing yield	High (>95%)	Low (≈85%)	Low (≈85%)
Mask #	4 ~ 5	4 ~ 7	5 ~ 7
Cost	Low	Low	High
Scalable to large panels	Yes	Yes	?
Primary TFT process	PECVD	PVD	PECVD
Process temperature (C)	>300	~40	>400

FIGURE 3. Comparison of display processes

Technology trends

TFT-LCD (thin-film-transistor liquid-crystal display) is the baseline technology. MO / White OLED (organic light emitting diode) is used for larger screens. LTPS / AMOLED is used for small / medium screens. The challenges for OLED are the effect of < 1 micron particles on yield, much higher cost compared to a-Si due to increased mask steps, and moisture impact to yield for the OLED step.

Mobility limitation (**FIGURE 2**) is one of the key reasons for the shift to MO and LTPS to enable better viewing experience from higher resolution, etc.

The challenge to MO is the oxidation after IGZO metallization / moisture prevention after OLED step, which decreases yield. A large volume of N_2O (nitrous oxide) is required for manufacturing, which means a shift in the traditional supply mode might need to be considered.

Although AMLCD displays are still dominant in the market today, AMOLED displays are growing quickly. Currently about 25% of smartphones are made with AMOLED displays and this is expected to grow to ~40% by 2021. OLED televisions are also growing rapidly, enjoying double digit growth rate year over year. Based on IHS data, the revenue for display panels with AMOLED technologies is expected to have a CAGR of 18.9% in the next five years while the AMLCD display revenue will have a -2.8% CAGR for the same period with the total display panel revenue CAGR of 2.5%. With the rapid growth of AMOLED display panels, the panel makers have accelerated their investment in the equipment to produce AMOLED panels.

Types of backplanes

There are three types of thin-film-transistor devices for display: amorphous silicon (a-Si), low temperature polysilicon (LTPS), and metal oxide (MO), also known as transparent amorphous oxide semiconductor (TAOS). AMLCD panels typically use a-Si for lower-resolution displays and TVs while high-resolution displays use LTPS transistors, but this use is mainly limited to small and medium displays due to its higher costs and scalability limitations. AMOLED panels use LTPS and MO transistors where MO devices are typically used for TV and large displays (**FIGURE 3**).

How gases are used

This shift in technology also requires a change in the gases used in production of AMOLED panels as compared with the AMLCD panels. As shown in **FIGURE 4**, display manufacturing today uses a wide variety of gases.

These gases can be categorized into two types: Electronic Specialty gases (ESGs) and Electronic Bulk gases (EBGs) (**FIGURE 5**). Electronic Specialty gases such as silane, nitrogen trifluoride, fluorine (on-site generation), sulfur hexafluoride, ammonia, and phosphine mixtures make up 52% of the gases used in the manufacture of the displays while the Electronic Bulk gases–nitrogen, hydrogen, helium, oxygen, carbon dioxide, and argon – make up the remaining 48% of the gases used in the display manufacturing.

Key usage drivers

The key gas usage driver in the manufacturing of displays is PECVD (plasma-enhanced chemical vapor deposition),

which accounts for 75% of the ESG spending, while dry etch is driving helium usage. LTPS and MO transistor production is driving nitrous oxide usage. The ESG usage for MO transistor production differs from what is shown in **FIGURE 4**: nitrous oxide makes up 63% of gas spend, nitrogen trifluoride 26%, silane 7%, and sulfur hexafluoride and ammonia together around 4%. Laser gases are used not only for lithography, but also for excimer laser annealing application in LTPS.

		a-Si	LTPS	Metal Oxide	Process	Delivery Method
Deposition	SiH_4	●	●	●	Si, SiN, SiO	Gas cylinders & large forms
	NH_3	●	●	●	SiN	
	N_2O		●	●	SiO	
	TEOS		●		SiO	Bubbler
Doping	1% B_2H_6/H_2		●		in-situ	Gas cylinders
	15% B_2H_6/H_2		●		implanter	
	1% PH_3/H_2	●			in-situ	Gas cylinders & large forms
	20% PH_3/H_2		●		implanter	Gas cylinders
	1% PH_3/SiH_4	●			in-situ	
Clean	NF_3	●	●	●	CVD	Gas cylinders & large forms
	F_2	●	●	●	CVD	on-site
Etch	CF_4		●		Si, SiN, SiO	Gas cylinders
	C_2HF_5		●		SiO	
	SF_6	●	●	●	SiN, SiO	
	Cl_2	●	●		Si	
	BCl_3	●			Al	
Laser	4.5% HCl/1% H_2/Ne		●		XeCl 308	Gas cylinders
	Xe		●		XeCl 308	
	Ne		●		Balance	
	5% F_2/He		●		KrF 248	
	Kr		●		KrF 248	
Others	H_2	●	●	●	CVD	Compressed gas truck
	O_2	●	●	●	SiO, ITO, Etch	Cryogenic liquid truck
	N_2	●	●	●	SiN	On-site & Cryogenic liquid truck
	CO_2	●	●	●		Cryogenic liquid truck
	He	●	●	●	Cooling	Compressed gas truck
	Ar	●	●	●	PVD	Cryogenic liquid truck

FIGURE 4. Primary gases used in display manufacturing

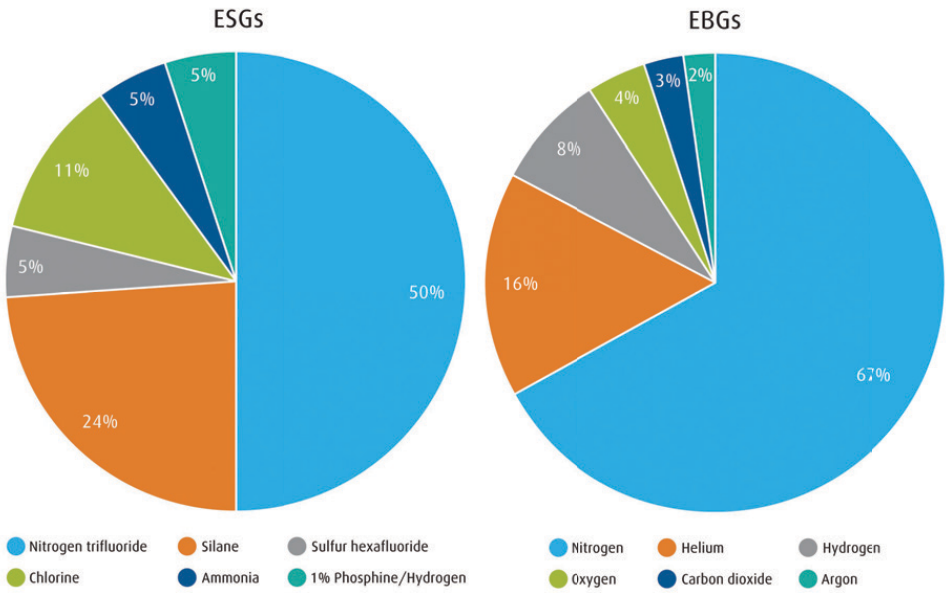


FIGURE 5. Gas usage in display manufacturing by type for a-Si devices

Silane: SiH_4 is one of the most critical molecules in display manufacturing. It is used in conjunction with ammonia (NH_3) to create the silicon nitride layer for a-Si transistor, with nitrogen (N_2) to form the pre excimer laser anneal a-Si for the LTPS transistor, or with nitrous oxide (N_2O) to form the silicon oxide layer of MO transistor.

Nitrogen trifluoride: NF_3 is the single largest electronic material from spend and volume standpoint for a-Si and LTPS display production while being surpassed by N_2O for MO production. NF_3 is used for cleaning the PECVD chambers. This gas requires scalability to get the cost advantage necessary for the highly competitive market.

Nitrous oxide: Used in both LTPS and MO display production, N_2O has surpassed NF_3 to become the largest electronic material from spend and volume standpoint for MO production. N_2O is a regional and localized product due to its low cost, making long supply chains with high logistic costs unfeasible. Averaging approximately 2 kg per 5.5 m^2 of mother glass area, it requires around 240 tons per month for a typical 120K per month capacity generation 8.5 MO display production. The largest N_2O compressed gas trailer can only deliver six tons of N_2O each time and thus it becomes both costly and risky for MO production.

Nitrogen: For a typical large display fab, N_2 demand can be as high as 50,000 Nm3/hour, so an on-site generator, such as the Linde SPECTRA-N® 50,000, is a cost-effective solution that has the added benefit of an 8% reduction in CO_2 (carbon dioxide) footprint over conventional nitrogen plants.

Helium: H_2 is used for cooling the glass during and after processing. Manufacturers are looking at ways to decrease the usage of helium because of cost and availability issues due it being a non-renewable gas.

Gas distribution at the fab

N_2 On-site generators: Nitrogen is the largest consumed gas at the fab, and is required to be available before the first tools are brought to the fab. Like major semiconductor fabs, large display fabs require very large amounts of nitrogen, which can only be economically supplied by on-site plants.

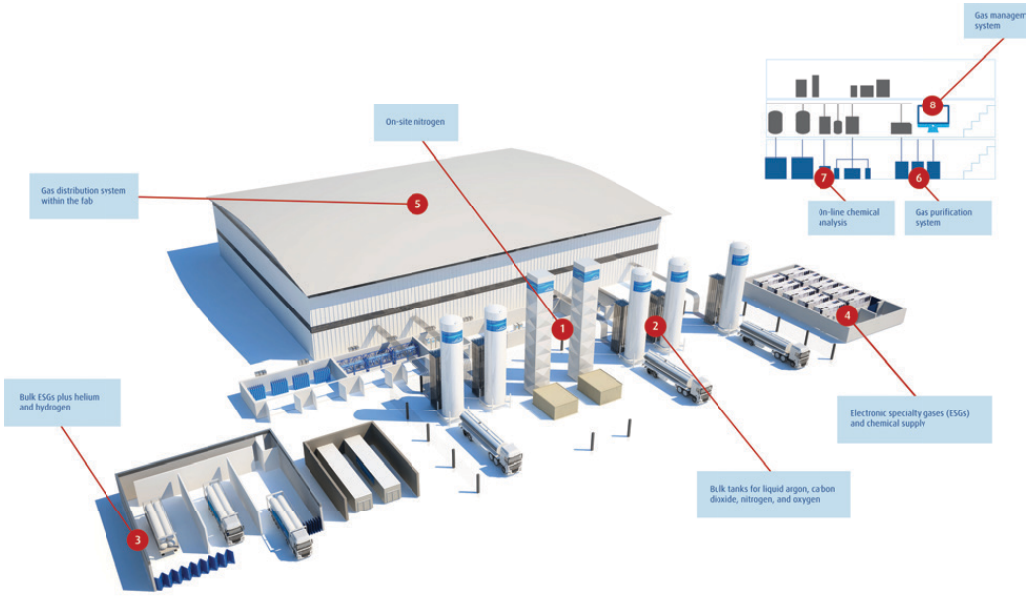


FIGURE 6. Where gases are used in the display fab

Cryogenic liquid truck trailers: Oxygen, argon, and carbon dioxide are produced at off-site plants and trucked short distances as cryogenic liquids in specialty vacuum-insulated tankers.

Compressed gas truck trailers: Other large volume gases like hydrogen and helium are supplied over longer distances in truck or ISO-sized tanks as compressed gases.

Individual packages: Specialty gases are supplied in individual packages. For higher volume materials like silane and nitrogen trifluoride, these can be supplied in large ISO packages holding up to 10 tons. Materials with smaller requirements are packaged in standard gas cylinders.

Blended gases: Laser gases and dopants are supplied as blends of several different gases. Both the accuracy and precision of the blended products are important to maintain the display device fabrication operating within acceptable parameters.

In-fab distribution: Gas supply does not end with the delivery or production of the material of the fab. Rather, the materials are further regulated with additional filtration, purification, and on-line analysis before delivery to individual production tools.

Conclusion

The consumer demand for displays that offer increasingly vivid color, higher resolution, and lower power consumption will challenge display makers to step up the technologies they employ and to develop newer displays such as flexible and transparent displays. The transistors to support these new displays will either be LTPS and / or MO, which means the gases currently being used in these processes will continue to grow. Considering the current a-Si display production, the gas consumption per area of the glass will increase by 25% for LTPS and ~ 50% for MO productions.

To facilitate these increasing demands, display manufacturers must partner with gas suppliers to identify which can meet their technology needs, globally source electronic materials to provide customers with stable and cost-effective gas solutions, develop local sources of electronic materials, improve productivity, reduce carbon footprint, and increase energy efficiency through on-site gas plants. This is particularly true for the burgeoning China display manufacturing market, which will benefit from investing in on-site bulk gas plants and collaboration with global materials suppliers with local production facilities for high-purity gas and chemical manufacturing. ◆

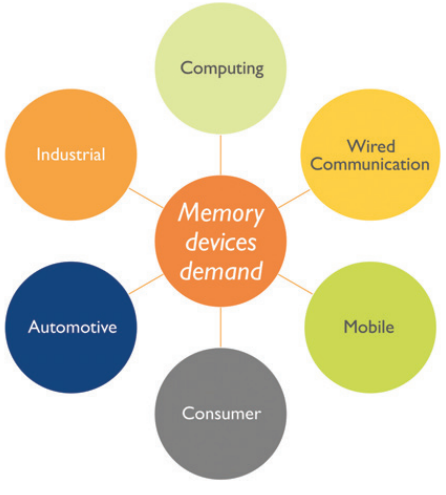
Memory device packaging: From leadframe to TSV

SANTOSH KUMAR, *Yole Développement, Lyon-Villeurbanne, France*

Memory devices employ a wide range of packaging technology from wire-bond leadframe and BGA to TSV.

The memory market is going through a strong growth phase. The total memory market grew by >50% YoY to more than US$125 billion in 2017 from US$79.4 billion in 2016. [1] RAM and NAND dominate the market, representing almost 95 % of standalone memory sales. There is a supply/demand mismatch in the market which is impacting on the ASP of memory devices, and as a result the large memory IDMs are reaping record profits. The memory industry has consolidated with the top five players - Samsung, SKHynix, Micron, Toshiba and Western Digital - accounting for 90% of the market.

The demand for memory is coming from all sectors but the mobile and computing (mainly servers) market is showing particularly strong growth. On average, the DRAM memory capacity per smartphone will rise more than threefold to reach around 6GB by 2022. DRAM cost per smartphone represents >10% of the bill of materials of the phone and is expected to increase further. The NAND capacity per smartphone will increase more than fivefold to reach >150GB by 2022. For servers, the DRAM capacity per unit will increase to a whopping 0.5TB by 2022, and the NAND capacity per SSD for the enterprise market will be in excess of 5TB by 2022. The growth in these markets is led by applications like deep learning, big-data, networking, AR/VR, and autonomous driving. The automotive market, which traditionally used low density (low-MB) memory, will see the adoption of DRAM memory led by the emerging trend of autonomous driving and in-vehicle infotainment. The NOR flash memory market also saw a resurgence and is expected to grow at an impressive 16% CAGR to reach ~US$4.4 billion by 2022, due to its application in new areas such as AMOLED displays, touch display driver ICs and industrial IoTs.

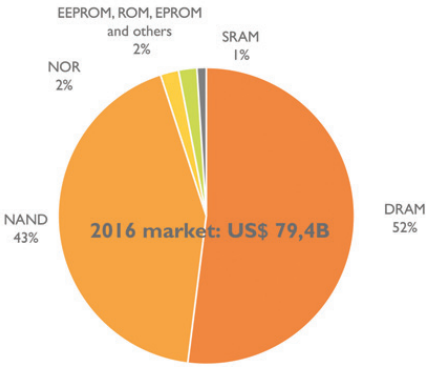


On the supply side, the consolidation of players, the difficulty in migrating to advanced nodes due to technical challenges, and the need for higher investment to migrate from 2D to 3D NAND, has led to shortfall in both DRAM & NAND flash supply. DRAM players want to retain high ASPs (& high profitability) to justify the huge capex investment for advanced node migration and as such are not inclined to increase capacity. Entry of Chinese memory players will ease the supply side constraint, but it'll not happen before 2020.

Memory device packaging

There are many variations of memory device packaging. This implies a wide range of packaging technology from the low pin count SOP package to the high pin-count TSV, all depending upon the specific product requirements such as density, performance, cost, etc. We have broadly identified five packaging platforms for memory devices: *viz* lead frame, wire-bond BGA, flip-chip BGA, WLCSP and TSV, even though in each platform there are many variations and different nomenclature in industry.

The total memory package market is expected to grow at 4.6% $CAGR_{2016\text{-}2022}$ to reach ~US$26 billion by 2022. [1] Wire-bond BGA accounted for more than 80% of the packaging market in dollar terms in 2016. Flip-chips, however, started making inroads in the DRAM memory packaging market and is expected to grow at ~20% CAGR in the next five years to account for more than 10% of the memory packaging market. Currently the flip-chip market



is only around 6% of the total memory packaging market. Flip-chip growth is led by its increased adoption in the DRAM PC/server segment fueled by a high bandwidth requirement.

Currently Samsung has already converted >90% of its DRAM packaging line. SK Hynix have started the conversion and other players will also adopt it in future. At Yole Développement (Yole), we believe that all DDR5 memory for PC/servers will move to flip-chip.

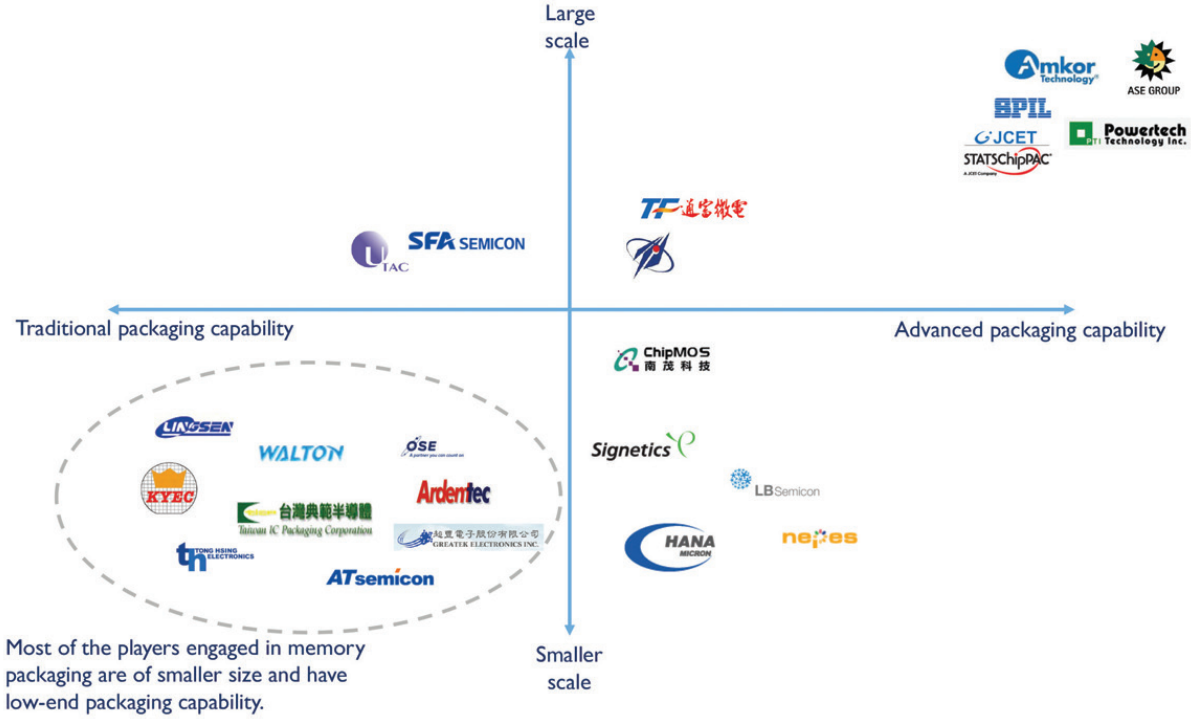
TSV is employed in high bandwidth memory devices requiring high bandwidth with low latency memory chips for high performance computing in various applications. In 2016 the TSV market was <1% of the total memory market. However, it is expected to grow by >30% CAGR to reach ~8% of memory packaging in dollar terms. WLSCP packaging is used in NOR flash and niche memory devices (EEPROMs/EPROM/ROM). It is expected to grow at >10% CAGR, but in terms of value will remain <1% of the market by 2022.

In mobile applications, memory packaging will mainly remain on the wire-bond BGA platform but will start to move into the multi-chip package (ePoP) for high end smartphones.

The main requirement of NAND flash devices is high storage density at low cost. NANDs are stacked using wire bonding to provide high density in a single package. The NAND packaging market is expected to reach ~ US$ 10 billion by 2022. NAND flash packaging will remain on the wire bond BGA platform and will not migrate to flip-chip. Toshiba, however, will start using TSV packaging in NAND devices to increase the data transfer rate for high end applications. Following Toshiba, we believe Samsung and SKHynix will also bring TSV packaged NAND devices into the market.

OSATs account for <20% of the memory packaging business

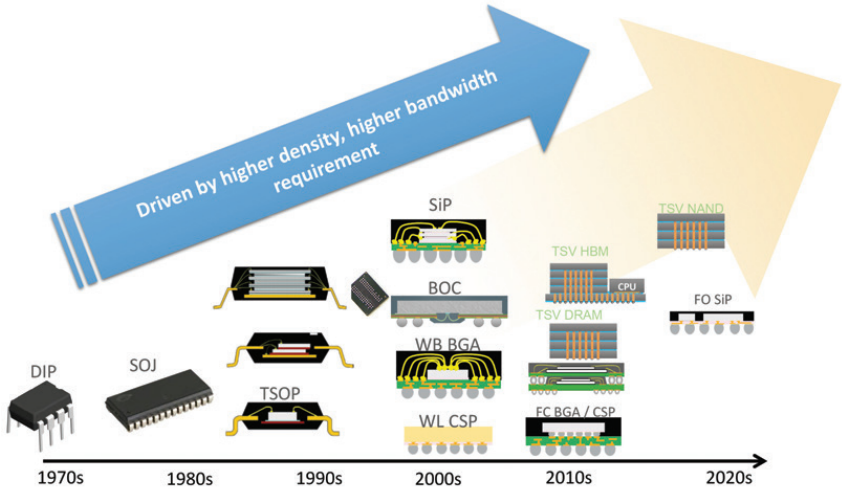
The total memory packaging market is estimated to have been ~US$20 billion in 2016. There are many OSATs involved in the memory packaging business, and >80% of the packaging (by value) is still done internally by OSATs. The majority of these are small OSATs and have only low-end packaging capability. Global memory IDMs have much experience in packaging, accumulated over years, and have their own internal large capacity. Therefore, there is limited opportunity for OSATs to make inroads into the packaging activity of IDMs. Many Chinese players, however, are entering the memory market with more than US$50 billion investment committed. [1] These new entrants do not have experience in memory assembly / packaging, unlike global IDMs, and they will outsource major packaging activities to OSATs. The flip-chip business for memory packaging will increase to 13% of the total market to reach US$3.5 billion in 2022. This



is an opportunity for low-end memory OSATs to invest in flip-chip bumping and assembly capacity. Otherwise they will lose business to the big OSATs with advanced packaging capability.

Conclusion

The memory industry is going through a golden phase with strong demand coming from all sectors, particularly from the mobile and computing (mainly servers) markets. Memory devices employ a wide range of packaging technology from wire-bond leadframe and BGA to TSV. Wire-bond BGA still accounts for the bulk of the memory packaging market. However, flip-chip technology will start making inroads in DRAM memory packaging and will grow at 20% CAGR (by revenue) over the next five years, accounting for ~13% of the total memory packaging market by 2022. The memory packaging market is mainly controlled by IDMs. OSATs have limited opportunity to impact IDM packaging activity. Many Chinese players, however, are entering the memory business and, unlike global IDMs, these new players lack experience in memory assembly/packaging and they outsource most of their packaging activity to OSATs.



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Baseline yield predicts baseline reliability

DAVID W. PRICE, **DOUGLAS G. SUTHERLAND** *and* **JAY RATHERT**, *KLA-Tencor, Milpitas, CA*

The Process Watch series explores key concepts about process control—defect inspection, metrology and data analysis—for the semiconductor industry. This article is the second in a five-part series on semiconductors in the automotive industry. In the first article, we introduced some of the challenges involved in the automotive supply chain and showed that the same defects that cause yield loss are also responsible for reliability issues. In this article, we discuss the connection between baseline yield and baseline reliability and present ways that both can be improved.

The strong correlation between semiconductor IC yield and reliability has been well studied and documented. The data shown in **FIGURE 1** demonstrates this relationship. Similar outcomes have been shown at the lot, wafer and die location level. Simply put, when yield is high, reliability follows suit. As discussed in the first article of the Process Watch Automotive series, this yield-reliability correlation is not unexpected, since the defect types that cause die failures are the same as those that cause early reliability problems. Yield and reliability defects differ primarily by their size and where they occur on the device pattern in the die.

It follows that reducing the number of yield-killing defects in the IC manufacturing process will increase baseline yield and simultaneously increase device reliability in the field. Recognizing this fact, fabs serving the automotive market are faced with two critical questions. The first is economic in nature: what is the appropriate level of investment of time, money and resources in yield improvement to create the needed reliability gains? The second question is technical: what are the best defect reduction methodologies for boosting the baseline yield to the necessary levels?

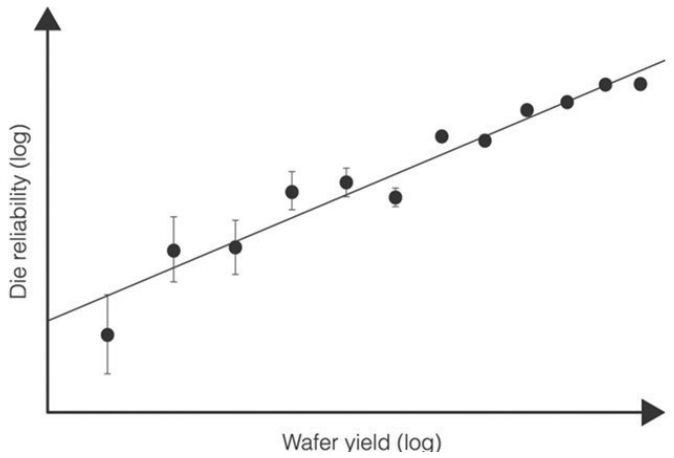

FIGURE 1. Data demonstrating the strong correlation between IC device reliability and yield. [1]

For fabs that make consumer devices (ICs for mobile phones, tablets, etc.), "mature yield" is defined as the point where further improvements in yield no longer warrant the investment of time and resources. As a product matures, yield tends to stabilize at some high value, but usually well below 100%. Instead of pursuing higher yield, it makes more economic sense for the consumer fab to reallocate resources to developing the next design node's processes and devices, or to reducing costs to improve the profitability of their legacy node.

For automotive fabs, the economic decision on whether to invest more to increase yield extends beyond the typical marginal revenue determination. When there is a reliability issue, the automotive IC manufacturer will likely bear the cost of expensive and time-consuming failure analysis, and will be held financially liable for field warranty failures, recalls and potential legal liabilities. Given that automotive IC reliability requirements are as much as two to three orders of magnitude higher than consumer IC requirements, automotive fabs must achieve higher baseline yield levels. This requires a new way of thinking about what constitutes "mature yield."

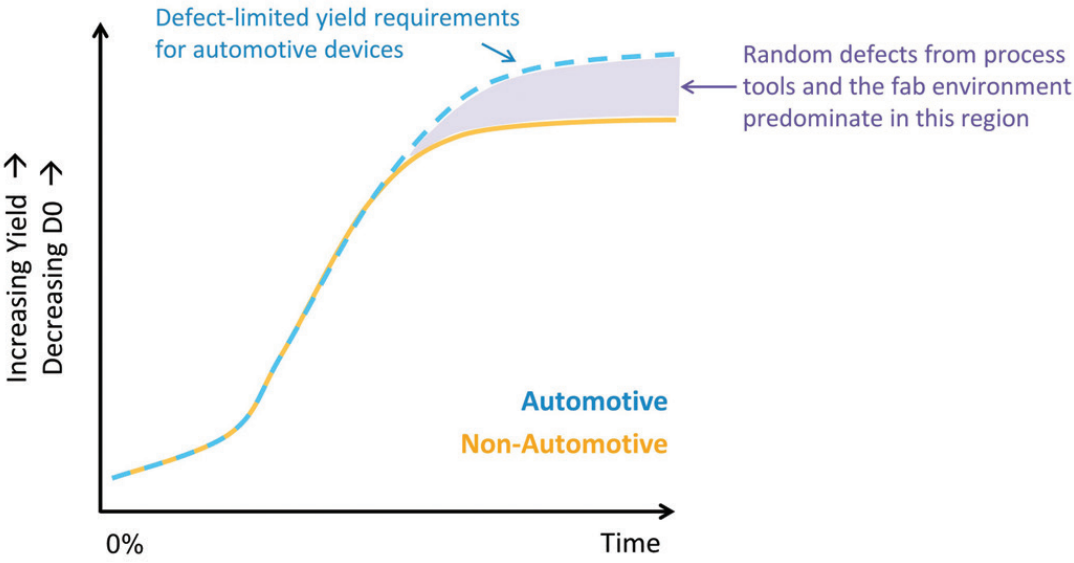

FIGURE 2. In a consumer device fab (yellow line), the top of the yield curve (Yield versus Time) is limited by diminishing returns to profitability for increased investment in defect reduction. The automotive fab yield curve, shown by the blue dashed line, also factors in reliability. Additional improvement to baseline yield must be made by automotive fabs to meet the parts per billion quality requirements. The purple shaded area highlights the difference in yield between consumer and automotive fabs – a difference that's primarily related to process tool defectivity.

FIGURE 2 highlights the difference in mature yield between consumer and automotive fabs. As either type of fab moves up the yield curve, almost all systematic sources of yield loss have been resolved. The remaining yield loss is primarily due to random defectivity, contributed by either the process tools or the environment. A consumer fab may adopt a "good enough" approach to yield and reliability at this point. However, in the automotive industry, fabs employ a continuous improvement strategy to push the yield curve even higher. By driving down the incidence of yield-limiting defects, automotive fabs also reduce latent reliability defects, thereby optimizing their profits and mitigating risk.

The automotive supply chain – from OEMs to Tier 1 suppliers to IC manufacturers – is adopting a mindset that "every defect matters" in pursuit of a Zero Defect strategy. They recognize that when latent defects escape the fab, the cost of discovery and mitigation increases as much as 10x at every additional level of the supply chain. As such, the existing over-reliance on electrical test needs to be replaced by a strategy where latent failures are stopped in the fab where the cost is lowest. Only by implementing a methodical defect reduction program will a fab move towards the Zero Defect goal and be able to pass the stringent audits required by automobile manufacturers.

In addition to robust inline defect control capability, some of the defect reduction methods that automotive purchasing managers look for include:

- Continuous Improvement Program (CIP) for baseline defect reduction
- Golden Tool Work Flow
- Dog Tool Programs

Continuous improvement in baseline defect reduction

The foundation of any rigorous baseline defect reduction plan is the inline defect strategy. To successfully detect the defects that affect yield and reliability of their design rules and device types, a fab's inline defect strategy must include both an appropriate process control toolset and an adequate sample plan. The defect inspection systems utilized must produce the required defect sensitivity, be maintained to specifications and utilize well-tuned inspection recipes. The sample plan must be set for the right process steps at sufficient frequency to quickly flag process or tool excursions. Additionally, there should be sufficient inspection capacity to support a control plan that expedites excursion detection, root cause isolation and WIP-at-risk traceability. With these elements, an automotive fab should achieve a successful baseline defect reduction plan that can demonstrate positive yield trends over time, provide goals for further improvement, and equal industry best practices.

Within a baseline defect reduction plan, one of the biggest challenges is answering the question: where did this defect come from? The answer is often not straightforward. Sometimes the defect is detected many process steps away from the defect source. Sometimes the defect becomes apparent only after the wafer has gone through several other process steps that "decorate" it – i.e., make it more visible to inspection systems. A Tool Monitoring strategy helps resolve the question surrounding a defect's origin.

In Tool Monitoring / Tool Qualification (TMTQ) applications, a bare wafer is inspected, run through a specific process tool (or chamber) and then inspected again (**FIGURE 3**). Any new defects found on the wafer with the second inspection must have been added by that specific process tool. The results are unequivocal; there is no question about the defect's origin. Automotive fabs pursuing a Zero Defect standard recognize the benefit of a Tool Monitoring strategy: with sensitive inspection recipes, appropriate control limits and out-of-control action plans (OCAP), the sources of random yield loss contributed by each process tool can be revealed and addressed.

Furthermore, when a process tool's contribution of adder defects is plotted over time, as in **FIGURE 4**, it provides a record of continuous improvement that can be audited and used to set future defect reduction goals. The defects

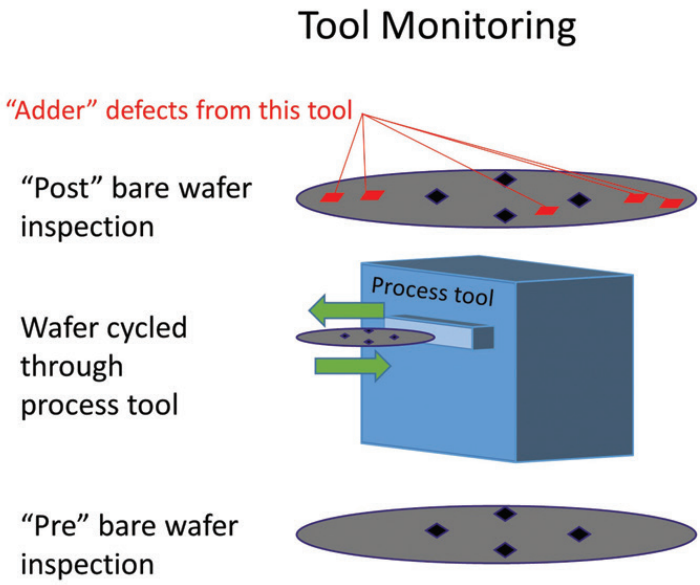

FIGURE 3. After baselining the bare wafer with a "pre" inspection, it can be cycled through some or all process tool steps. The "post" inspection reveals defects added by the process tool.

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from every tool in the fab can be classified to generate a defect library that can be referenced for failure analysis of field returns. This approach requires very frequent tool qualification – at least once per day – and is usually used in conjunction with a Golden Tool Work Flow or Dog Tool Programs, discussed below.

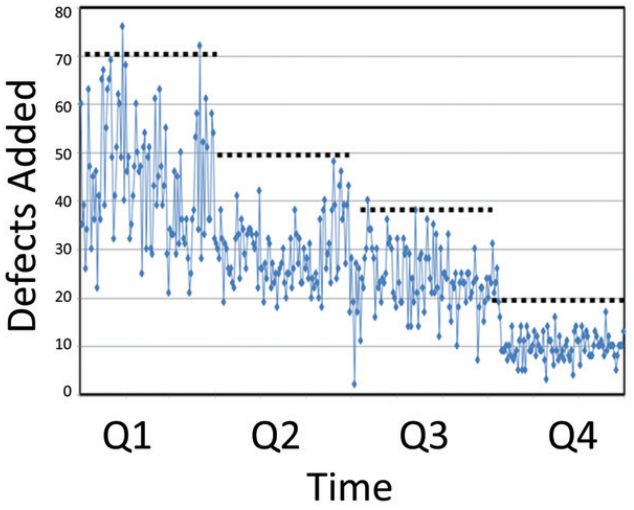

FIGURE 4. Continuous improvement in tool cleanliness over time. The source of the problem is unambiguous and objective defect reduction targets can be set on a quarterly or monthly basis. In addition, comparing the defectivity of two process tools can show which tool is cleaner. This helps guide tool maintenance activities to pinpoint the cause of the differences between the tools.

Golden Tool Work Flow

A Golden Tool Work Flow is another strategy used by fabs to reach the Zero Defect standard required by the automotive industry. With a Golden Tool Work Flow or Automotive Work Flow (AWF), the wafers for automotive ICs only go through the best process tools in the fab, requiring that the fab knows the best tool for any given process step. To reliability determine which tool is best, fabs leverage data from inline and tool monitoring inspections, and then only use those tools for the Automotive Work Flow. Restricting automotive wafers to a single tool at each process step can lead to longer cycle times. However, this is usually preferable to sending automotive wafers through process flows that suffer from higher defect levels that can lead to reliability issues. When coupled with a methodical continuous improvement program, most fabs can usually get multiple tools qualified for AWF at each step by setting quarterly targets for defect reduction.

Because it is a difficult method the scale up, the Golden Tool Work Flow is best suited for fabs where only a small percentage of WIP is automotive. For fabs in high volume automotive production, a more methodical continuous improvement program, such as the Dog Tool approach described below, is preferred.

Dog Tool Programs

A Dog Tool Program is the opposite of a Golden Tool Work Flow as it proactively addresses the worst process tool – the dog tool – at any given process step. Fabs that have been most successful in driving down baseline defectivity often have done so by adopting a Dog Tool Program. They first take down the dog tool at every process step and work on that tool until it is better than the average of the remaining tools in that set. They repeat this process over and over until all tools in the set meet some minimum standard. An effective Dog Tool program requires that the fab has a methodical Tool Monitoring strategy to qualify each process tool at each step. At a minimum, this qualification procedure should be done daily on each tool to ensure there is sufficient data so that an ANOVA or Kruskal-Wallis analysis can identify the best and worst tools in each set. A Dog Tool Program, with planned process tool downtime, is the one of the fastest ways known to bring an entire fab up to automotive standards. By increasing yield and reliability, this strategy ultimately improves an automotive fab's effective capacity and profitability.

Summary

Automotive manufacturers who demand high reliability often require the fab to change their mindset about what really defines mature yield. In this article we have discussed several ways that fabs can reduce their baseline defectivity and improve reliability and yield. In the next article in this series we will discuss some of the technical considerations regarding the sensitivity of defect inspection tools and how that helps ensure chip reliability.

DR. DAVID W. PRICE and JAY RATHERT are Senior Directors at KLA-Tencor Corp. DR. DOUGLAS SUTHERLAND is a Principal Scientist at KLA-Tencor Corp., Milpitas, CA.

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Next generation dopant gas delivery system for ion implant applications

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A new class of adsorbent materials offer high capacity storage and safe delivery of dopant gases

Metal-Organic Framework (MOF) materials are a new class of crystalline adsorbents with broad applicability in electronics materials storage, delivery, purification, and abatement. The adsorbents have unprecedented surface areas and uniform pore sizes that can be precisely customized to the specific properties of electronic gases. ION-X® is a sub-atmospheric dopant gas delivery system designed for ion implantation, and the first commercial product that uses MOFs (ION-X® is commercially available through an agreement between NuMat Technologies and Versum Materials). The performance of ION-X delivering arsine (AsH_3), phosphine (PH_3), and boron trifluoride (BF_3) was evaluated in high current implanters at the Axcelis Advanced Technology Center and compared to the incumbent delivery systems. In-process and on-wafer results of the MOF-based dopant gases compared positively to conventional source gases. Flow, pressure, and beam stability were undistinguishable from conventional gas sources throughout the lifetime of the cylinder. Beam and wafer contamination levels (both surface and energetic) were below specification limits, matching the performance of the reference qualified products.

Dopant gas safety challenges

The storage and delivery of hazardous gases creates significant environmental, health, and safety challenges. Their usage requires implementation of stringent safety control systems to minimize the risks of exposure to humans and the environment. The dangers associated with handling toxic gases are the result of both the inherent chemical hazard of the molecule and the kinetic energy stored in the vessel in the form of compression. In essence, the lethality of a toxic release is magnified exponentially by the energetic force of the high-pressure storage. Historically, one way to mitigate these risks was to dilute the hazardous material with inert gases in an effort to attenuate the toxicity effects. Depending on the concentration, this solution provides a safety factor improvement of 10 or 100 by virtue of reducing the molecular density of the hazardous gas to 10% or 1% mixtures, respectively. This approach is commonly used in the electronics manufacturing industry for gases that are known to have extreme toxicity. Hydride gases (i.e. arsine, phosphine, germane, or diborane) are examples of such highly toxic gases used as source materials in a number of electronic manufacturing processes. While this dilution method is effective at reducing the toxicity levels, these mixtures

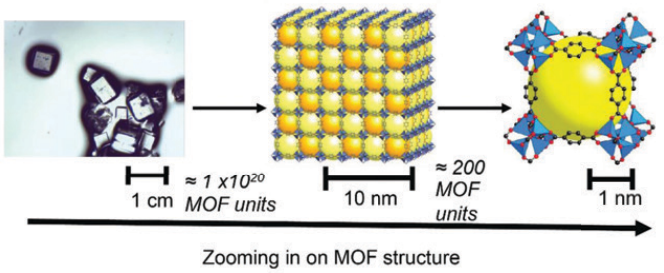

FIGURE 1. Structure of a representative MOF material at different scales.

are typically produced at cylinder pressures significantly higher than the pressures of the pure toxic gases. In a release event, this solution reduces the lethality of the dose at the expense of a higher release rate.

In 1993, ATMI (now an Entegris company) introduced a different approach to reduce the toxic gas storage hazards [1]. The technology involves using nano-porous adsorbents to condense the gas molecules onto their surfaces. This process effectively reduces the kinetic energy of the gas, thus reducing the pressure in the gas cylinder. The large available surface areas within these materials result in gas storage capacities comparable to the high-pressure cylinders. The intrinsic safety advantages of adsorbed gas cylinders are derived from the reduction in pressure within the cylinder. Typically, these vessels are filled to sub-atmospheric pressures (measured at room temperature) in order to inhibit an outward gas release in the event of a leak.

The first sub-atmospheric dopant gas delivery systems used zeolites (SDS® 1) while the second and third generations (SDS® 2 and SDS® 3) evolved to activated carbon adsorbent materials. These gas cylinders store and deliver dopant precursor gases (primarily arsine, phosphine, and boron trifuoride) predominantly for ion implantation processes. In its third generation, and in order to further improve gas storage capacities, SDS 3 evolved by creating a highly dense monolithic adsorbent that nearly eliminated void volumes in the cylinder.

In this paper, we describe a new sub-atmospheric gas delivery system (ION-X ®) that uses a novel ultra-high surface area class of materials called metal-organic frameworks (MOFs). In addition, the implant process performance using the new product delivering arsine, phosphine, and boron trifluoride was evaluated in a major ion implant OEM facility will be described.

MOF overview: The next generation in nano-porous adsorbents

MOF are three-dimensional crystalline structures assembled with metal-containing nodes connected by organic links (**FIGURE 1**). The resulting highly organized molecular structures generate nano-pores with record surface areas [2-4]. In addition, the large number of available metal nodes and organic linkers provide unparalleled molecular design flexibility to tailor the chemical and physical properties of the adsorbent material to fit the application. Since their discovery in the early 1990's, MOFs have evolved from an academic curiosity to a widely recognized new class of materials with practical applications in energy, specialty chemicals, military, medical, pharmaceutical, and electronics industries. MOFs are one of the fastest growing classes of materials, with thousands of experimental structures now being reported.

For gas storage and delivery applications, MOFs' design flexibility provides advantages over traditional adsorbents (**FIGURE 2**). Pore size, surface area, and chemical stability can be tailored to the specific properties of the adsorbed gases. Compared to zeolites and activated carbon adsorbents, MOFs have significantly larger surface areas (up to 7,000 m^2/g has been reported [5]. This property, combined with bulk density, is critical in gas storage applications where capacity is measured in terms of vessel volume rather than adsorbent mass. Pore size tunability is also an important parameter in efforts to match the dimensions of the MOF cavities to the molecular sizes of the target adsorbates. This parameter impacts adsorption capacities (how much gas can be loaded) and desorption characteristics (how much can be delivered as a function of pressure). Unlike the broad pore size distributions found in activated carbon adsorbents, MOFs' crystallinity results in more "usable" pores. This pore size uniformity also results in higher gas quality, as impurities are selectively size excluded.

	Zeolites	Carbons	Metal Organic Frameworks
Surface Area	~500 m^2/g	~1500 m^2/g	Up to 7500 m^2/g
Structure	Crystalline	Amorphous	Crystalline
Pore Size	0.3-1 nm	0.3-5 nm	0.3-10 nm
Pore Size Distribution	Narrow	Broad	Narrow
Molecular Tunability	Low	Very Low	Large

FIGURE 2. Properties of selected adsorbents.

FIGURE 3. ION-X 2.4 L dopant gas cylinder.

Preventing reactions between the adsorbent and the target gas is extremely important in electronics applications. Adsorbent/gas interactions will contribute to gas decomposition, leading to impurities and unwanted dopant gas composition changes that could affect the process. The molecular composition of zeolites and carbon adsorbents are limited to a few elements (typically carbon, aluminum, and silicon) and their oxides. MOFs, on the other hand, can be synthetized from a large range of organic and inorganic constituents, offering more options for creating stable gas/adsorbent interactions.

MOF-based gas delivery system for ion implant gases

ION-X (**FIGURE 3**) is a sub-atmospheric dopant gas storage and delivery system designed for ion implantation [6]. ION-X uses individual MOF structures with tailored pore sizes to effectively and reversibly adsorb arsine, phosphine, and boron trifluoride gases. The pressure in filled ION-X cylinders is below one atmosphere, significantly reducing the health and environmental impact of an accidental gas release. Furthermore, MOFs' ultra-high surface areas and uniform structures provide capacity and deliverable advantages compared to existing carbon adsorbent-based products (**FIGURE 4**). It is important to note that the first-generation ION-X cylinders utilize granulated MOFs with similar adsorbent bulk density to the first-generation carbon product: for the same mass of adsorbent, MOFs provide 40% to 55% higher gas delivery by virtue of their superior surface area and pose size uniformity. Analogous to the evolution of SDS® 2, MOF densification inside the cylinder will further increase the gas capacity in next-generation ION-X products.

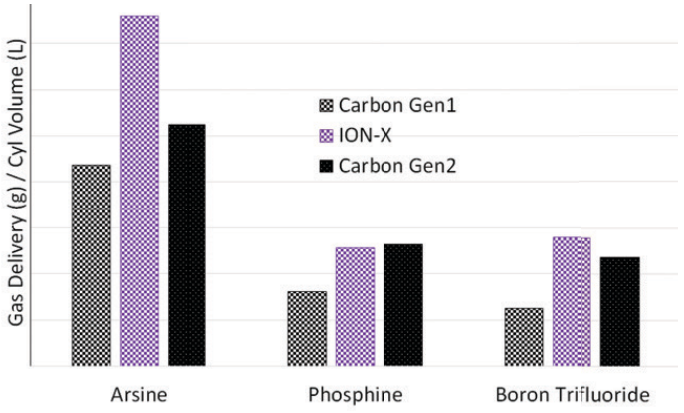

FIGURE 4. Dopant gas delivery comparison (down to 20 torr) between carbon-based incumbent products and ION-X.

Implant performance characterization

The performances of ION-X dopant delivery systems were recently evaluated using a PurionH 300 mm high current ion implanter at Axcelis' Advanced Technology Center (Beverly, MA, USA). The test plan included flow, mass spectral, and metal contamination analyses (both at the surface and at implanted depth). The experiments were repeated using commercially available and well-established sub-atmospheric dopant gas sources in order to provide a basis for comparison.

Cylinder installation and setup was seamless, requiring no modifications to the existing gas box hardware or software. Flow rate stability for all three gases (AsH_3, PH_3, and BF_3) was demonstrated in the 3.5 to 8 sccm ranges down to cylinder pressures of 20 torr (spec limit). For arsine, the flow experiment continued through a full cylinder depletion, showing a stable flow rate down to cylinder pressure below 3 torr.

The beam energy, purity, and stability were evaluated by analyzing the mass spectra generated during the implantation processes. In all cases, the target dose was 5×10^{15} at/cm^2 with beam energies of 40 keV, 20 keV and 15 keV for As^+, P^+, and BF_2^+ ion implants respectively. The stability and purity of the target doping ion beams were within specifications and very similar to the ones produced by the reference gas sources. Based on the mass spectra, ION-X did not generate any impurities derived from either gas or MOF decomposition.

Neutral and energetic metal contamination levels were thoroughly investigated in this study. All metal analyses were performed by sampling wafers produced using the recipes described in the previous paragraph. Vapor Phase Decomposition-inductively coupled Plasma-Mass Spectrometry (VPD-ICP-MS) was used to monitor the contamination from key trace metals at the wafer surface. Particular attention was placed on monitoring zinc and iron, metals used in the hydride and BF_3 ION-X MOF adsorbents respectively. Results show that all metal levels were within specification limits and compared well to the levels detected in control wafers. In all cases, zinc and iron surface contamination levels were below their corresponding detection limits of 0.03 and 0.05 x 10^{10} atoms/cm^2.

Energetic metal contamination is of special interest in ion implantation as even low levels of impurities could affect the performance of the electronic devices. The depth

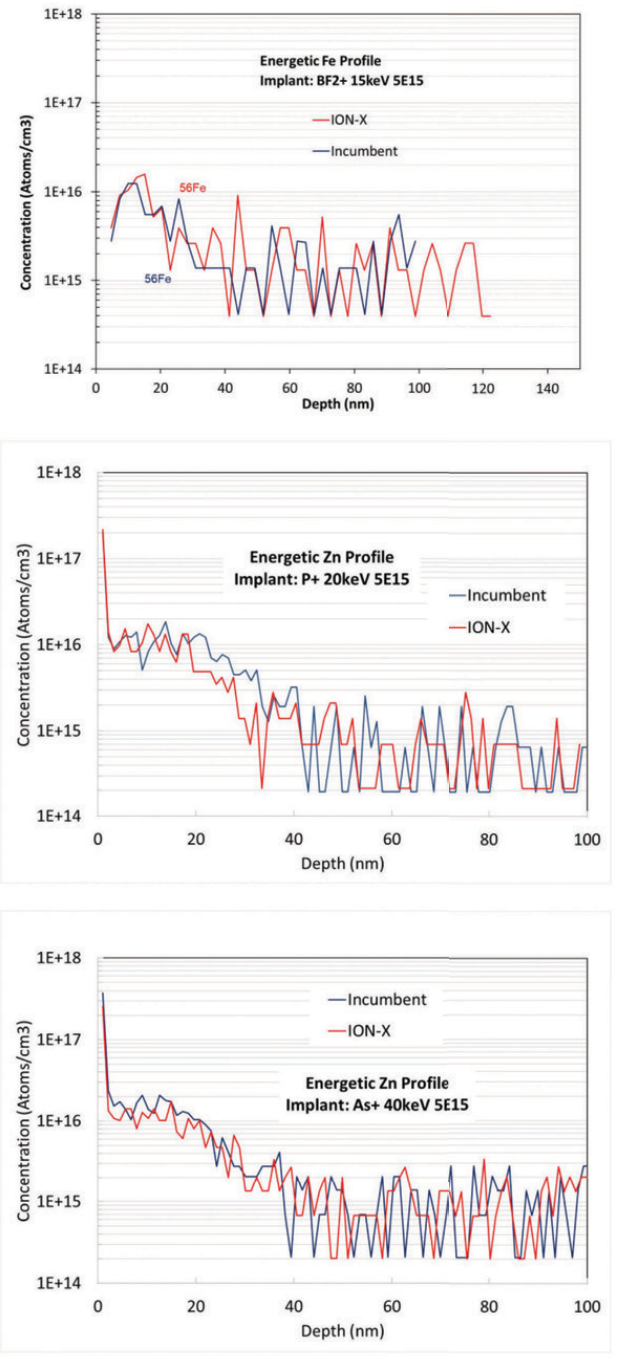

FIGURE 5. Comparison of energetic Zn (hydrides) and Fe (BF3) levels using incumbent and ION-X gas sources.

profile of the metals used in ION-X's MOFs composition were measured using Secondary Ion Mass Spectrometry (SIMS). Wafers used for SIMs analyses were doped using both ION-X and incumbent gas sources using the same ion implant tool and previously stated recipes. The zinc and iron metal concentration profiles for the hydride and boron implants were well within specifications and show no discernable differences between the incumbent and the MOF-based gas sources (**FIGURE 5**). These results, combined with the previous surface contamination tests, conclusively establish the gas and ion purity of the dopant species extracted from ION-X adsorbents. Moreover, the results are consistent with extensive gas analyses performed at NuMat after subjecting the MOF adsorbent materials to accelerated aging, vibration, and cycle testing.

Summary

This article provides process and on-wafer performance of ION-X, a new MOF-based dopant gas delivery system. The adsorbents used in these cylinders have surface areas, stability, purity, and pore sizes ideal for the storage and delivery of ion implant dopant gases. In-process and on-wafer performance of boron trifluoride, arsine, and phosphine dopant sources compared positively to conventional source gas cylinders. The issue of contamination was investigated in detail, demonstrating that the new adsorbents do not contribute to surface or energetic metal impurities. The results published in this article provide independent evaluation of the new product, supporting the safe use of this product in mainstream ion implant applications. To that end, ION-X is already qualified and being used at an electronics manufacturing site with confirmed high stability and purity performance.

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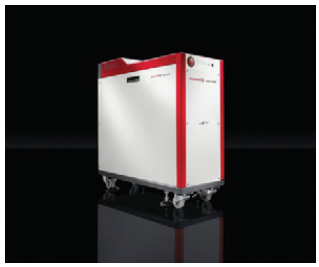

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Cloud computing: the power to optimize manufacturing

DAVID W. JIMENEZ, *CEO, Wright Williams & Kelly, Inc.*

For 27 years Wright Williams & Kelly, Inc. (WWK) has developed strategies and operational products and services proven to produce significant results. Over the course of nearly three decades WWK has saved its clients over $10 billion and led the way in cost modeling, capacity planning, and operational efficiency; however, sometimes a company gets ahead of its markets. It has been 15 years since WWK launched its first online subscription-based product…and 13 years since it stopped offering it. Today, WWK returns to the cloud.

The cloud is an innovation fueled by advanced chip technology, but it has also been a model the industry hesitated to embrace. Much of this had to do with limited data protection schemes. Intellectual property (IP) is at the core of a successful integrated circuit business and letting key information leave the confines of the organization has traditionally been a forbidden proposition.

Fast forward a decade and a half and cloud-based services are now the norm. Fears over IP theft remain, but the protections have greatly improved. Further, the offerings that add value to cloud-based solutions have also greatly expanded. The move to the cloud now has less to do with a reduction in paranoia and more to do with the advantages of cloud computing. IBM breaks down the advantages into three areas; flexibility; efficiency; and strategic value.

Flexibility allows the scaling of computing power to the task at hand regardless of the local machine used to connect. Efficiency is accessing the needed applications from anywhere in the world from any connected device. Strategic value comes from being able to move faster than competitors by not being tied to existing infrastructure and the hesitancy to obsolete major IT investments. Michael Wright and Walter Ferguson in their 2005 treatise "The New Business Normal" predicted strategic advantage would accrue to those who could access, collate, analyze, and act on information faster than the competition, anywhere in the world and at any time.

WWK has leveraged these advantages by moving its complete suite of manufacturing optimization applications to the cloud. In addition to the advantages inherent in cloud computing, this move provides WWK's clients substantial cost advantages by lowering up front licensing costs and shifting from capital budgeting to more flexible expense accounting.

Cloud-based solutions: Developed with DARPA/SEMATECH, TWO COOL® is a cost of ownership (COO) and overall equipment efficiency (OEE) modeling platform designed to help equipment and process engineers as well as suppliers understand process step level impacts of changes in operating parameters.

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Advantages put into practice: One advantage in moving these applications to the cloud is users benefit from a state-of-the art computing system. Modeling and simulation apps are computing power intensive. Instead of each user requiring a high-end workstation, the cloud allows users to share a virtual machine(s) (VM). When needs increase, upgrading the VM is quick and low-cost. This keeps the total cost of ownership (TCO) for IT infrastructure at a minimum.

Another advantage is updates happen behind the scenes and for all users at the same time. Traditional software maintenance costs disappear. No more scenarios where users are operating on different revision levels nor lose data due to forgotten backups.

Remote computing has always been a better solution, but there were reasons behind the slow acceptance. Even before the term cloud computing came to the fore, WWK understood this. It offered a remote server-based product before anyone knew what the cloud was. WWK was early to market, but the understanding it gained pointed it in the right direction. Like most market windows you can be early but never late. The arrival of the breadth of solutions needed to offer cloud-based applications has enabled WWK to scrap client-side software licensing and provide a robust, low cost manufacturing optimization software suite with all the advantages it envisioned 15 years ago. I guess we are back to the future. ◆

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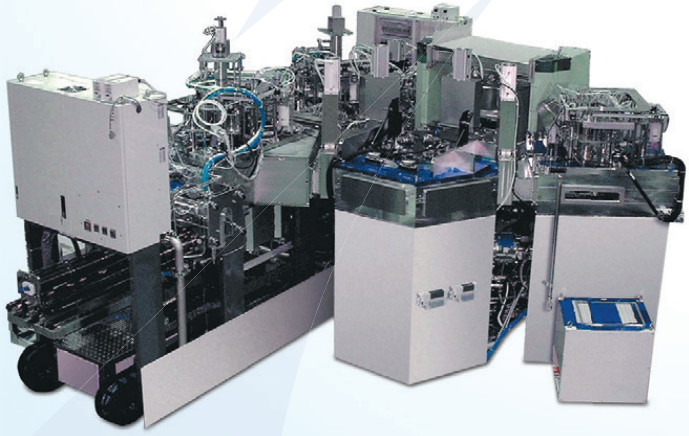

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