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AUGUST/SEPTEMBER 2018

Solid State TECHNOLOGY

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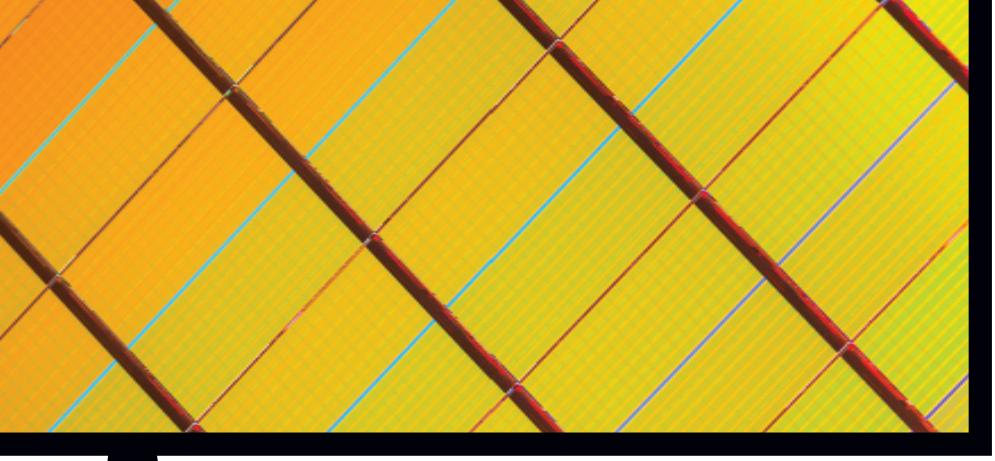

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Caption: 3D XPoint is a storage class memory (SCM) based on phase-change that fits in between fast DRAM and non-volatile NAND. Source: Intel

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The cobbler's children getting shoes?

There's an old proverb that the shoemaker's children always go barefoot, indicating how some professionals don't apply their skills for themselves. Until lately, that has seemed the case with the semiconductor manufacturing industry which has been good at collecting massive amounts of data, but no so good at analyzing that data and using it to improve efficiency, boost yield and reduce costs. In short, the industry could be making better use of the technology it has developed.

That's now changing, thanks to a worldwide focus on Industry 4.0 – more commonly known as "smart manufacturing" in the U.S. – which represents a new approach to automation and data exchange in manufacturing technologies. It includes cyber-physical systems, the Internet of things, cloud computing, cognitive computing and the use of artificial intelligence/deep learning.

At SEMICON West this year, these trends will be showcased in a new Smart Manufacturing Pavilion where you'll be able to see - and experience - data-sharing breakthroughs that are creating smarter manufacturing processes, increasing yields and profits, and spurring innovation across the industry. Each machine along the Pavilion's multi-step line is displayed, virtually or with actual equipment on the floor - from design and materials through front-end patterning, to packaging and test to final board and system assembly.

In preparation for the show, I had the opportunity to talk to Mike Plisinski, CEO of Rudolph Technologies, the sponsor of the Smart Pavilion about smart manufacturing. He said in the past "the industry got very good at collecting a lot of data. We sensors on all kinds of tools and equipment and we'd a track it with the idea of being able to do predictive maintenance or predictive analytics. That I think had minimal success," he said.

What's different now? "With the industry consolidating and the supply chains and products getting more complex that's created the need to go beyond what existed. What was inhibiting that in the past was really the ability to align this huge volume of data," he said. The next evolution is driven by the need to improve the processes. "As we've gone down into sub-20 manometer, the interactions between the process steps are more complex, there's more interaction, so understanding that interaction requires aligning digital threads and data streams." If a process chamber changed temperature by 0.1°C, for example, what impact did it have on lithography process by x, y, z CD control. That's the level of detail that's required. "That that has been a significant challenge and that's one of the areas that we've focused on over the last four, five years -- to provide that kind of data alignment across the systems,: Plisinski said.

Every company is different, of course, and some have been managing this more effectively than others, but the cobbler's children are finally getting new shoes.

—Pete Singer, Editor-in-Chief

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Web Exclusives

Top 10 semiconductor industry innovations

Over the past three decades, most of the world's innovations have centered largely on business models and involved iterative advances of existing technologies, with none matching the global impact of the top 10 semiconductor industry discoveries and advances, Dr. Morris Chang, founder of TSMC and the IC foundry model, said at SEMICON Taiwan 2018.

https://bit.ly/2xhzKaT

CEA-Leti at SEMICON West 2018

Pete Singer, Solid State Technology's Editor-in-Chief, talked with Leti's CEO at SEMICON West 2018 about this year's Leti Innovation Days.

https://bit.ly/2MxsItl

Next on-chip: Human organs

Many new innovations were discussed at imec's U.S. International Technology Forum (ITF) at the Grand Hyatt in San Francisco, including quantum computing, artificial intelligence, sub-3nm logic, memory computing, solid-state batteries, EUV, RF and photonics, but perhaps the most interesting was new technology that enables human cells, tissues and organs to be grown and analyzed on-chip.

https://bit.ly/2PsckYV

Subfab data growing in importance

The importance of data gathered and analysed in the subfab – the place where vacuum pumps, abatements systems and other supporting equipment operates – is growing. Increasingly, manufacturers are finding that these systems have a direct impact on yield, safety, cost-of-ownership and ultimately capacity and cycle time.

https://bit.ly/2o4v6sE

n&b news and blogs

2018 EUVL Workshop Update

The 2018 EUVL Workshop was held last June at CXRO, LBL in Berkeley, jointly organized by EUV Litho, Inc. and CXRO.

https://bit.ly/2BGFXCZ

Insights from the Leading Edge: Will Apple get caught in the trade war?

Why has the California-based company (Apple) enjoyed remarkable success in China, while some Chinese companies have experienced big losses amid a growing trade conflict with Washington?

https://bit.ly/2MvhNQS

Ruthenium nanolayers are ferromagnetic at RT

Researchers from Intel Corporation and the University of Minnesota and the University of Wisconsin have shown that strained atom-scale films of pure ruthenium (Ru) metal exhibit ferromagnetism at room temperature, openning up the possibility of using the material to build novel magnetic random access memory (MRAM) devices.

https://bit.ly/2MsM1UH

Gartner identifies five emerging technology trends that will blur the lines between human and machine

The 35 must-watch technologies represented on the Gartner Inc. Hype Cycle for Emerging Technologies, 2018 revealed five distinct emerging technology trends that will blur the lines between humans and machines. Emerging technologies, such as artificial intelligence (AI), play a critical role in enabling companies to be ubiquitous, always available, and connected to business ecosystems to survive in the near future.

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EUROPE - **Murata** announced investments in MEMS sensor manufacturing in Finland.

ASIA - **Toshiba** announced next-generation superjunction power MOSFETs.

USA - **Cabot Microelectronics** to acquire KMG Chemicals.

EUROPE - Soitec (Euronext Paris), a designer and manufacturer of semiconductor materials, and **MBDA** announce the joint acquisition of Dolphin Integration.

USA - **pSemi Corporation** (formerly Peregrine Semiconductor), a Murata company focused on semiconductor integration, introduced the world's first monolithic, silicon-on-insulator (SOI) Wi-Fi front-end module.

ASIA - **TowerJazz** announced details of its China Technical Global Symposium (TGS) event in Shanghai on August 22, 2018.

USA - **Synopsys, Inc.** and **IBM** announced a collaboration to apply design technology co-optimization (DTCO) to the pathfinding of new semiconductor process technologies for the 3-nanometer (nm) process node and beyond.

ASIA - **Samsung Electronics** started mass production of the industry's first 4-bit consumer SSD.

USA - **Entegris, Inc.** released the next generation EUV 1010 Reticle Pod for high-volume IC manufacturing using extreme ultraviolet (EUV) lithography.

USA - **Leti** and **CMP** announced the integrated-circuit industry's first multi-project-wafer (MPW) process for fabricating emerging non-volatile memory OxRAM devices on a 200mm foundry base-wafer platform.

Worldwide semiconductor revenue hit record $120.8B in Q2 2018

Global semiconductor industry revenue grew 4.4 percent, quarter over quarter, in the second quarter of 2018, reaching a record $120.8 billion. Semiconductor growth occurred in all application markets and world regions, according to IHS Markit (Nasdaq: INFO).

"The explosive growth in enterprise and storage drove the market to new heights in the second quarter," said Ron Ellwanger, senior analyst and component landscape tool manager, IHS Markit. "This growth contributed to record application revenue in data processing and wired communication markets as well as in the microcomponent and memory categories."

Due to the ongoing growth in the enterprise and storage markets, sequential microcomponent sales grew 6.5 percent in the second quarter, while memory semiconductor revenue increased 6.4 percent. "Broadcom Limited experienced exceptional growth in its wired communication division, due to increased cloud and data-center demand," Ellwanger said.

Memory component revenue continued to rise in the second quarter, compared to the previous quarter, reaching $42.0 billion dollars. "This is the ninth consecutive quarter of rising revenue from memory components, and growth in the second quarter of 2018 was driven by higher density in enterprise and storage," Ellwanger said. "This latest uptick comes at a time of softening prices for NAND flash memory. However, more attractive pricing for NAND memory is pushing SSD demand and revenue higher."

Semiconductor market share

Samsung Electronics continued to lead the overall semiconductor industry in the second quarter with 15.9 percent of the market, followed by Intel at 13.9 percent and SK Hynix at 7.9 percent. Quarter-over-quarter market shares were relatively flat, with no change in the top-three ranking. SK Hynix achieved the highest growth rate and record quarterly sales among the top three companies, recording 16.4 percent growth in the second quarter.

Top 10 semiconductor supplier growth rates by revenue

Q2-18 Rank	Company Name	Q2-17 Revenue($)	Q1-18 Revenue($)	Q2-18 Revenue($)	YoY Grwoth	QoQ Growth
1	Samsung Electronics	14,388	18,607	19,233	33.7%	3.4%
2	Intel	14,568	15,745	16,737	14.9%	6.3%
3	SK Hynix	5,884	8,152	9,488	61.3%	16.4%
4	Micron Technology	5,352	7,194	7,438	39.0%	3.4%
5	Broadcom Limited	4,186	4,768	4,488	7.2%	-5.9%
6	Qualcomm	4,011	4,001	4,134	3.1%	3.3%
7	Texas Instruments	3,575	3,697	3,905	9.2%	5.6%
8	nVidia	1,966	2,660	2,826	43.7%	6.2%
9	Toshiba Memory Corp.*	2,015**	2,766	2,780	38.0%	0.5%
10	Infineon Technologies	2,057	2,256	2,273	10.5%	0.8%
	Top 10 Companies	58,002	69,846	73,302	26.4%	4.9%
	All Others	43,192	45,899	47,536	10.1%	3.6%
	Total Semiconductor	**101,194**	**115,745**	**120,838**	**19.4%**	**4.4%**

*Toshiba Memory Corp new customer Q2 2018.

**Q2 2017 revenue derived from Toshiba Semiconductor memory revenue.

Source: Competitive Landscaping Tool Intelligence Service, Q2 2018

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New material could improve efficiency of computer processing and memory

A team of researchers led by the University of Minnesota has developed a new material that could potentially improve the efficiency of computer processing and memory. The researchers have filed a patent on the material with support from the Semiconductor Research Corporation, and people in the semiconductor industry have already requested samples of the material.

The findings are published in Nature Materials, a peer-reviewed scientific journal published by Nature Publishing Group.

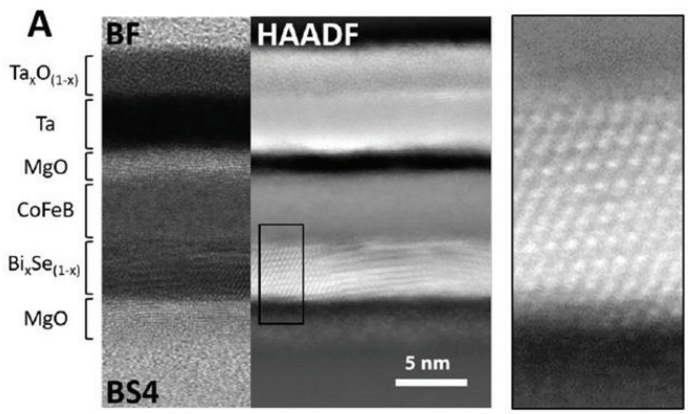
"We used a quantum material that has attracted a lot of attention by the semiconductor industry in the past few years, but created it in unique way that resulted in a material with new physical and spin-electronic properties that could greatly improve computing and memory efficiency," said lead researcher Jian-Ping Wang, a University of Minnesota Distinguished McKnight Professor and Robert F. Hartmann Chair in electrical engineering.

The new material is in a class of materials called "topological insulators," which have been studied recently by physics and materials research communities and the semiconductor industry because of their unique spin-electronic transport and magnetic properties. Topological insulators are usually created using a single crystal growth process. Another common fabrication technique uses a process called Molecular Beam Epitaxy in which crystals are grown in a thin film. Both of these techniques cannot be easily scaled up for use in the semiconductor industry.

In this study, researchers started with bismuth selenide (Bi_2Se_3), a compound of bismuth and selenium. They then used a thin film deposition technique called "sputtering," which is driven by the momentum exchange between the ions and atoms in the target materials due to collisions. While the sputtering technique is common in the semiconductor industry, this is the first time it has been used to create a topological insulator material that could be scaled up for semiconductor and magnetic industry applications.

However, the fact that the sputtering technique worked was not the most surprising part of the experiment. The nano-sized grains of less than 6 nanometers in the sputtered topological insulator layer created new physical properties for the material that changed the behavior of the electrons in the material. After testing the new material, the researchers found it to be 18 times more efficient in computing processing and memory compared to current materials.

"As the size of the grains decreased, we experienced what we call 'quantum confinement' in which the electrons in the material act differently giving us more control over the electron behavior," said study co-author Tony Low, a University of Minnesota assistant professor of electrical and computer engineering.



Researchers studied the material using the University of Minnesota's unique high-resolution transmission electron microscopy (TEM), a microscopy technique in which a beam of electrons is transmitted through a specimen to form an image.

"Using our advanced aberration-corrected scanning TEM we managed to identify those nano-sized grains and their interfaces in the film," said Andre Mkhoyan, a University of Minnesota associate professor of chemical engineering and materials science and electron microscopy expert.

Researchers say this is only the beginning and that this discovery could open the door to more advances in the semiconductor industry as well as related industries, such as magnetic random access memory (MRAM) technology.

"With the new physics of these materials could come many new applications," said Mahendra DC (Dangi Chhetri), first author of the paper and a physics Ph.D. student in Professor Wang's lab.

Wang agrees that this cutting-edge research could make a big impact.

"Using the sputtering process to fabricate a quantum material like a bismuth-selenide-based topological insulator is against the intuitive instincts of all researchers in the field and actually is not supported by any existing theory," Wang said. "Four years ago, with a strong support from Semiconductor Research Corporation and the Defense Advanced Research Projects Agency, we started with a big idea to search for a practical pathway to grow and apply the topological insulator material for future computing and memory devices. Our surprising experimental discovery led to a new theory for topological insulator materials.

"Research is all about being patient and collaborating with team members. This time there was a big pay off," Wang said.

Size of semiconductor acquisitions may have hit limit

The demise of Qualcomm's pending $44 billion purchase of NXP Semiconductors in late July along with growing regulatory reviews of chip merger agreements, efforts by countries to protect domestic technology, and the escalation of global trade friction all suggest semiconductor acquisitions are hitting a ceiling in the size of doable deals. It is becoming less likely that semiconductor acquisitions over $40 billion can be completed or even attempted in the current geopolitical environment and brewing battles over global trade.

Biggest Semiconductor Acquisition Announcements

Ranking	Acquisition-Buyer (Year Announced)	Price ($B)
1	**NXP** by Qualcomm (struck in 2016 and raised in 2018)*	$44.0
2	**Broadcom** by Avago (2015)	$37.0
3	**ARM** by SoftBank (2016)	$32.0
4	**SanDisk** by Western Digital (2015)	$19.0
5	**Toshiba Memory** by Bain Capital-Led Consortium (2017)	$18.0
6	**Freescale** by U.S Investment Companies (2006)	$17.6
7	**Altera** by Intel (2015)	$16.7
8	**Linear Technology** by Analog Devices (2016)	$14.8
9	**Freescale** by NXP (2015)	$11.8
10	**Burr Brown** by Texas Instruments (2000)	$7.6

*Canceled in late July 2018 after failing to win clearance from China.

Source: Companies, IC Insights

IC Insights believes a combination of factors—including the growing high dollar value of major chip merger agreements, complexities in combining large businesses together, and greater scrutiny of governments protecting their domestic base of suppliers—will stifle ever-larger mega-transactions in the semiconductor industry in the foreseeable future. Figure 1 ranks the 10 largest semiconductor merger and acquisition announcements and underscores the growth in size of these M&A transactions. Eight of the 10 largest announcements occurred in the last three years with only the biggest deal (Qualcomm buying NXP) failing to be completed.

It is important to note that IC Insights' M&A list only covers semiconductor suppliers, chipmakers, and providers of integrated circuit intellectual property (IP) and excludes acquisitions of software and system-level businesses by IC companies (such as Intel's $15.3 billion purchase of Mobileye, an Israeli-based developer of digital imaging technology for autonomous vehicles, in August 2017). This M&A list also excludes transactions involving semiconductor capital equipment suppliers, material producers, chip packaging and testing companies, and design automation software firms.

Qualcomm's $44 billion cash purchase of NXP would have been the largest semiconductor acquisition ever if it was completed, but the deal—originally announced in October 2016 at nearly $39 billion and raised to $44 billion in February 2018—was canceled in the last week of July because China had not cleared the transaction. China was the last country needed for an approval of the merger, and it was believed to be close to clearing the purchase in 2Q18, but growing threats of

tariffs in a brewing trade war with the U.S. and moves to block Chinese acquisitions of American IC companies caused China to taken no action on the $44 billion acquisition in time for a deadline set by Qualcomm and NXP. U.S.-based Qualcomm canceled the acquisition on July 26 and quickly paid NXP in the Netherlands a $2 billion breakup fee so the two companies could move on separately.

Prior to Qualcomm's failed $44 billion offer for NXP, the largest semiconductor acquisition was Avago Technologies' $37 billion cash and stock purchase of Broadcom in early 2016. Avago renamed itself Broadcom Limited after the purchase and launched a failed $121 billion hostile takeover bid for Qualcomm at the end of 2017. It lowered the unsolicited bid to $117 billion in February 2018 after Qualcomm raised its offer for NXP to $44 billion. In March 2018, U.S. President Donald Trump blocked Broadcom's $117 billion takeover bid for Qualcomm after concerns were raised in the U.S. government about the potential loss of cellular technology leadership to Chinese companies, if the hostile acquisition was completed. After the presidential order, Broadcom executives said the company was considering other acquisition targets, with cash, that would be smaller and more focused.

The global semiconductor industry has been reshaped by a historic wave of mergers and acquisitions during the past three years, with about 100 M&A agreements being reached between 2015 and the middle of 2018 with the combined value of these transactions being more than $245 billion, based on data collected by IC Insights and contained within its Strategic Reviews database subscription service and in The 2018 McClean Report on the IC Industry. A record-high $107.3 billion in semiconductor acquisition agreements were announced in 2015. The second highest total for semiconductor M&A agreements was then reached in 2016 at $99.8 billion. Semiconductor acquisition announcements reached a total value of $28.3 billion in 2017, which was twice the industry's annual average of about $12.6 billion in the first half of this decade but significantly less than 2015 and 2016, when M&A was sweeping through the chip industry at historic levels. In the first six months of 2018, semiconductor acquisition announcements had a total value of about $9.6 billion, based on IC Insights' running tally of announced M&A deals. ◆

Seven top 15 semi suppliers of the first half of 2018 register ≥20% gains

IC Insights released its August Update to the 2018 McClean Report earlier this month. This Update included a discussion of the top-25 semiconductor suppliers in 1H18 (the top-15 1H18 semiconductor suppliers are covered in this research bulletin) and Part 1 of an extensive analysis of the IC foundry market and its suppliers.

The top-15 worldwide semiconductor (IC and O-S-D—optoelectronic, sensor, and discrete) sales ranking for 1H18 is shown in Figure 1. It includes seven suppliers headquartered in the U.S., three in Europe, two each in South Korea and Taiwan, and one in Japan. After announcing in early April 2018 that it had successfully moved its headquarters location from Singapore to the U.S. IC Insights now classifies Broadcom as a U.S. company.

As shown, all but four of the top 15 companies had double-digit year-over-year growth in 1H18. Moreover, seven companies had ≥20% growth, including the five big memory suppliers (Samsung, SK Hynix, Micron, Toshiba/Toshiba Memory, and Western Digital/SanDisk) as well as Nvidia and ST.

The top-15 ranking includes one pure-play foundry (TSMC) and four fabless companies. If TSMC were excluded from the top-15 ranking, U.S.-based Apple would have been ranked in the 15th position. Apple is an anomaly in the top company ranking with regards to major semiconductor suppliers. The company designs and uses its processors only in its own products—there are no sales of the company's MPUs to other system makers. IC Insights estimates that Apple's custom ARM-based SoC processors and other custom devices had a "sales value" of $3.5 billion in 1H18.

IC Insights includes foundries in the top-15 semiconductor supplier ranking since it has always viewed the ranking as a top supplier list, not a marketshare ranking, and realizes that in some cases the semiconductor sales are double counted. With many of our clients being vendors to the semiconductor industry (supplying equipment, chemicals, gases, etc.), excluding large IC manufacturers like the foundries would leave

1H18 Top-15 Semiconductor Sales Leaders ($M, Including Foundries)

1H18 Rank	2017 Rank	Company	Headquarters	1Q18 Tot IC	1Q18 Tot O-S-D	1Q18 Tot Semi	2Q18 Tot IC	2Q18 Tot O-S-D	2Q18 Tot Semi	2Q18/1Q18 % Change	1H18 Tot Semi	1H17 Tot Semi	1H18/1H17 % Change
1	1	Samsung	South Korea	18,491	910	19,401	19,434	950	20,384	5%	39,785	29,181	36%
2	2	Intel	U.S.	15,832	0	15,832	16,753	0	16,753	6%	32,585	28,839	13%
3	4	SK Hynix	South Korea	8,016	125	8,141	9,421	192	9,613	18%	17,754	11,393	56%
4	3	TSMC (1)	Taiwan	8,473	0	8,473	7,839	0	7,839	-7%	16,312	14,601	12%
5	5	Micron	U.S.	7,486	0	7,486	7,920	0	7,920	6%	15,406	10,653	45%
6	6	Broadcom Ltd. (2)	U.S.	4,125	434	4,559	4,150	435	4,585	1%	9,144	8,404	9%
7	7	Qualcomm (2)	U.S.	3,897	0	3,897	4,087	0	4,087	5%	7,984	7,728	3%
8	9	Toshiba/Toshiba Memory	Japan	3,517	310	3,827	3,575	315	3,890	2%	7,717	6,159	25%
9	8	TI	U.S.	3,339	227	3,566	3,535	245	3,780	6%	7,346	6,595	11%
10	10	Nvidia (2)	U.S.	3,108	0	3,108	3,135	0	3,135	1%	6,243	4,083	53%
11	15	WD/SanDisk	U.S.	2,350	0	2,350	2,375	0	2,375	1%	4,725	3,715	27%
12	13	Infineon	Europe	1,360	907	2,267	1,388	926	2,314	2%	4,581	3,896	18%
13	11	NXP	Europe	2,017	252	2,269	2,035	255	2,290	1%	4,559	4,413	3%
14	12	ST	Europe	1,696	518	2,214	1,724	526	2,250	2%	4,464	3,732	20%
15	16	MediaTek (2)	Taiwan	1,696	0	1,696	2,032	0	2,032	20%	3,728	3,726	0%
—	—	Top-15 Total		85,403	3,683	89,086	89,403	3,844	93,247	4.7%	182,333	147,118	24%

(1) Foundry (2) Fabless

Source: Company reports, IC Insights' *Strategic Reviews* database

*Custom devices for internal use.

significant "holes" in the list of top semiconductor suppliers. Foundries and fabless companies are identified in the Figure. In the April Update to The McClean Report, market-share rankings of IC suppliers by product type were presented and foundries were excluded from these listings.

Overall, the top-15 list shown in **Figure 1** is provided as a guideline to identify which companies are the leading semiconductor suppliers, whether they are IDMs, fabless companies, or foundries.

In May 2018, Toshiba completed the $18.0 billion sale of its memory IC business to the Bain Capital-led consortium. Toshiba then repurchased a 40.2% share of the business. The Bain consortium goes by the name of BCPE Pangea and the group owns 49.9% of Toshiba Memory Corporation (TMC). Hoya Corp. owns the remaining 9.9% of TMC's shares. The new owners have plans for an IPO within three years. Bain has said it plans to support the business in pursing M&A targets, including potentially large deals. As a result of the sale of Toshiba's memory business, the 2Q18 sales results shown in **Figure 1** include the combined sales of the remaining semiconductor products at Toshiba (e.g., Discrete devices and System LSIs) and the new Toshiba Memory's NAND flash sales. The estimated breakdown of these sales in 2Q18 is shown below:

Toshiba System LSI: $468M
Toshiba Discrete: $315M
Toshiba Memory Corporation: $3,107M
Total Toshiba/Toshiba Memory Corporation 2Q18 Sales: $3,890M

In total, the top-15 semiconductor companies' sales surged by 24% in 1H18 compared to 1H17, four points higher than the total worldwide semiconductor industry 1H18/1H17 increase of 20%. Amazingly, the Big 3 memory suppliers—Samsung, SK Hynix, and Micron, each registered greater than 35% year-over-year growth in 1H18. Fourteen of the top-15 companies had sales of at least $4.0 billion in 1H18, three companies more than in 1H17. As shown, it took just over $3.7 billion in sales just to make it into the 1H18 top-15 semiconductor supplier list.

Intel was the number one ranked semiconductor supplier in 1Q17 but lost its lead spot to Samsung in 2Q17 as well as in the full-year 2017 ranking, a position it had held since 1993. With the continuation of the strong surge in the DRAM and NAND flash markets over the past year, Samsung went from having only 1% more total semiconductor sales than Intel in 1H17 to having 22% more semiconductor sales than Intel in 1H18!

It is interesting to note that memory devices are forecast to represent 84% of Samsung's semiconductor sales in 2018, up three points from 81% in 2017 and up 13 points from 71% just two years earlier in 2016. Moreover, the company's non-memory sales in 2018 are expected to be only $13.5 billion, up 8% from 2017's non-memory sales level of $12.5 billion. In contrast, Samsung's memory sales are forecast to be up 31% this year and reach $70.0 billion.

Chiplet tech discussed at DARPA ERI kickoff

PHIL GARROU,
Contributing Editor

With "Moore's Law", which has guided the electronics industry for more than 50 years, being challenged on both technical and economic grounds, the defense department (DARPA) is putting $1.5 billion into projects that could "radically alter how electronics are made".

Investments will support R&D in the areas of Architectures, Design, and Materials and Integration. It is hoped that investments in these three thrust areas will lead the next wave of U.S. semiconductor advancement.

DARPA kicked off the initiative and revealed some of the winning proposals July 23-25 in San Francisco.

Architectures: The goal of the *Software Defined Hardware (SDH)* program is to build runtime-reconfigurable hardware and software that enables near application-specific integrated circuit (ASIC) performance without sacrificing programmability for data-intensive algorithms. Intel, NVIDIA, Qualcomm, Systems & Technology Research, Georgia Tech, Stanford Univ, U Michigan, U of Washington and Princeton Univ were selected for the SDH program.

The goal of the *Domain-specific System on Chip (DSSoC)* program is to develop a heterogeneous SoC comprised of many cores that mix general-purpose processors, special-purpose processors, hardware accelerators, memory, and input/output (I/O). IBM, Oak Ridge National Labs, Arizona St Univ and Stanford Univ were chosen for the DSSoC program.

Design: The goal of the *Posh Open Source Hardware (POSH)* program is to create an open source SoC design and verification ecosystem that will enable the cost-effective design of ultra-complex SoCs. Univ of California,San Diego, Northrop Grumman, Cadence, Xilinx, Synopsys, Univ of Southern California, Princeton Univ and Sandia National Labs were selected for the POSH program.

Materials & Integration: The overall goal of the *Three Dimensional Monolithic System-on-a-Chip (3DSoC)* program is to develop 3D monolithic technology that will enable > 50X improvement in SoC digital performance at power. 3DSoC aims to drive research in process, design tools, and new compute architectures utilizing U.S. fabrication capabilities. Georgia Tech, Stanford Univ, MIT and Skywater Technology Foundry were chosen for the 3DSoC program.

The goal of the *Foundations Required for Novel Compute (FRANC)* program is to define the foundations required for assessing and establishing the proof of principle for beyond von Neumann compute architectures. HRL, Applied Materials, Ferric, UCLA, Univ of Minnesota and Univ of Illinois at Urbana-Champaign have been chosen for the FRANC program.

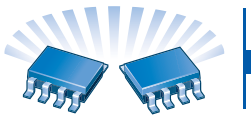
Also, *Common Heterogeneous Integration and Intellectual Property (IP) Reuse Strategies (CHIPS)* has now been included under the ERI umbrella. The CHIPS program envisions an ecosystem of discrete modular, reusable IP blocks that can be assembled into a system using existing and emerging integration technologies. The program will develop the design tools and integration standards required to demonstrate modular integrated circuit (IC) designs that leverage the best of DoD and commercial designs and technologies.

Instead of building complex SoC on silicon the CHIPS concept sees future systems where each function is made separately (chiplets) and are then connected together on a larger slice of silicon by high-bandwidth interconnects. One of the challenges will be getting these chiplets to communicate properly and do so at a speed and energy cost that's close to what they'd be if the system were all one piece of silicon. Interconnects using the standard will have to be capable of handling a lot of data without using much energy. It is estimated that it will have to cost less than 1 pico-joule to move a bit and be capable of moving 1 terabit per millimeter.

At the ERI kick-off, Intel CTO Mike Mayberry, who is VP and managing director of Intel Labs and holds responsibility for Intel's global research efforts in computing and communications, revealed that Intel will provide their Advanced Interface Bus (AIB) technology, to program participants, royalty-free to help link chiplets together. AIB is a standard communications interface made for connecting different dies (chiplets) in the same package. Intel already uses AIB in 2.5-D packages such as the company's Stratix 10 FPGA.

DARPAs Andreas Olofsson, manager of DARPA's CHIPS program, reitterated the need for a standard communications interface. "We need a plug-and-play standard," he said. "Once we have that standard, you can imagine vendors offering a ,number of chiplets for sale." The CHIPS program community is in the process of accepting the Intel AIB technology for this purpose. ◆

Packaging



Integrated 5G chip directions

ED KORCZYNSKI,
Sr. Technical Editor

To fulfill the promise of the Internet of Things (IoT), the world needs low-cost high-bandwidth radio-frequency (RF) chips for 5th-generation (5G) internet technology. Despite standards not being completely defined yet it is clear that 5G hardware will have to be more complex than 4G kit, because it will have to provide a total solution that is ultra-reliable with at least 10 Gb/second bandwidth. A significant challenge remains in developing new high-speed transistor technologies for RF communications with low power to allow IoT "edge" devices to operate reliably off of batteries.

At the most recent Imec Technology Forum in Antwerp, Belgium, Nadine Collaert, Distinguished MTS of imec, discussed recent research results from the consortium's High-Speed Analog and RF Program. In addition to working on core transistor fabrication technology R&D, imec has also been working on system-technology co-integration (STCO) and design-technology co-integration (DTCO) for RF applications.

Comparing the system specifications needed for mobile handsets to those for base-stations, transmitter power consumption should be 10x lower, while the receiver power consumption needs to be 2x lower. Today using silicon CMOS transistors, four power amplifiers alone consume 65% of a transmitter chip's power. Heterogeneous Bipolar Transistors (HBT) and High Electron Mobility Transistors (HEMT) built using compound semiconductors such as gallium-arsenide (GaAs), gallium-nitride (GaN), or indium-phosphide (InP) provide excellent RF device results. However, compared to making CMOS chips on silicon, HBT and HEMT manufacturing on compound semiconductor substrates is inherently expensive and difficult.

Heterogeneous Bipolar Transistors (HBT) and High Electron Mobility Transistors (HEMT) both rely upon the precise epitaxial growth of semiconductor layers, and such growth is easier when the underlying substrate material has similar atomic arrangement. While it is much more difficult to grow epi-layers of compound semiconductors on silicon wafers, imec does R&D using 300-mm diameter silicon substrates with a goal of maintaining device quality while lowering production costs. **FIGURE 1** shows cross-sections of the two "tracks" of III-V and GaN transistor materials being explored by imec for future RF chips.

Imec's High-Speed Analog/RF Program objectives include the following:

- High-speed III-V RF devices using low-cost, high-volume silicon-compatible processes and modules,
- Co-optimization with advance silicon CMOS to reduce form factor and enable power-efficient systems with higher performance, and
- Technology-circuit design co-optimization to enable complex RF-FEM modules with heterogeneous integration.

5G technology deployment will start with speeds below 6GHz, because technologies in that range have already been proven and the costs are known. However, after five years the frequency will change to the "mm-wave" range with the first wavelength band at ~28GHz. GaN material with a wide bandgap and high charge-density has been a base-station technology, and it could be an ideal material for low-power mm-wave RF devices for future handsets.

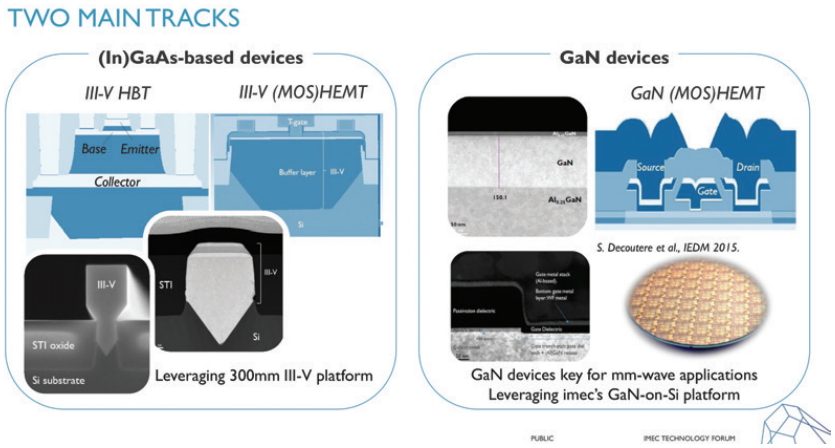


FIGURE 1. III-V on Silicon and GaN-on-Silicon RF device cross-sections, showing work on both Heterogeneous Bipolar Transistors (HBT) and High Electron Mobility Transistors (HEMT) for 5G applications. (Source: imec)

This R&D leverages the III-V on silicon capability that has been developed by imec for CMOS:Photonic integration. RF transistors could be stacked over CMOS transistors using either wafer- or die-stacking, or both could be monolithically co-integrated on one silicon chip. Work on monolithic integration of GaN-on-Silicon is happening now, and could also be used for photonics where faster transistors can improve the performance of optical links.

Semiconductors

Emerging memory types headed for volumes

DAVID LAMMERS, *Contributing Editor*

Two emerging memory types – 3D Xpoint and e-MRAM -- are now coming to the market.

After decades of R&D, two emerging memory types – the phase change memory-based 3D Xpoint, co-developed by Intel and Micron, and the embedded spin-torque transfer magnetic RAM (e-MRAM) from several foundries – are now coming to the market. One point of interest is that neither memory type relies on the charge-based SRAM and DRAM memory technologies that increasingly face difficult scaling challenges. Another is that both have inherent performance advantages that could extend their uses for decades to come.

3D XPoint is a storage class memory (SCM) based on phase-change that fits in between fast DRAM and non-volatile NAND; it is currently available in both SSDs and sampling in a DIMM form factor. David Kanter, an analyst at Real World Technologies (San Francisco) said the Optane SSDs are selling now but the DIMMs are shaping up to be "an early 2019 story" in terms of real adoption. "People are very excited about the DIMMs, including customers, software developers, the whole computer ecosystem. There is a lot of software development going on that is required to take advantage of it, and a lot of system companies are saying they can't wait. They are telling Intel 'give me the hardware.'"

"Intel is taking the long view" when it comes to 3D XPoint (the individual devices) and Optane (the SSDs and DIMMs), Kanter said. "This is a new technology and it is not a trivial thing to bring it to the market. It is a testament to Intel that they are taking their time to properly develop the ecosystem."

However, Kanter said there is not enough public information about 3D XPoint DIMMs, including performance, price, power consumption, and other metrics. Companies that sell enterprise database systems, such as IBM, Microsoft, Oracle, SAP, and others, are willing to pay high prices for a storage-class memory solution that will improve their performance.The Optane DIMMs, according to Intel, are well-suited to "large-capacity in-memory database solutions."

According to the Intel Web site, Optane DC persistent memory (**FIGURE 1**) "is sampling today and will ship for revenue to select customers later this year, with broad availability in 2019." It can be placed on a DDR4 module alongside DRAM, and matched up with next-generation Xeon processors. Intel is offering developers remote access to systems equipped with Optane memory for software development and testing.

Speaking at the Symposium on VLSI Technology in Honolulu, Gary Tressler, a distinguished engineer at IBM Systems, said "the reliability of 3D NAND impacts the enterprise," and predicted that the Optane storage class memory will serve to improve enterprise-class systems in terms of reliability and performance.

The DRAM scaling picture is not particularly bright. Tressler said "it could be four years before we go beyond the 16-gigabit size in terms of DRAM density." DRAM companies are eking out scaling improvements of 1nm increments," an indication of the physical limitations facing the established DRAM makers.

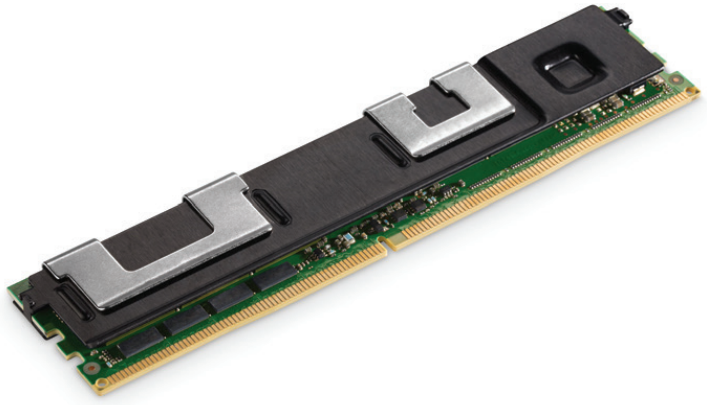
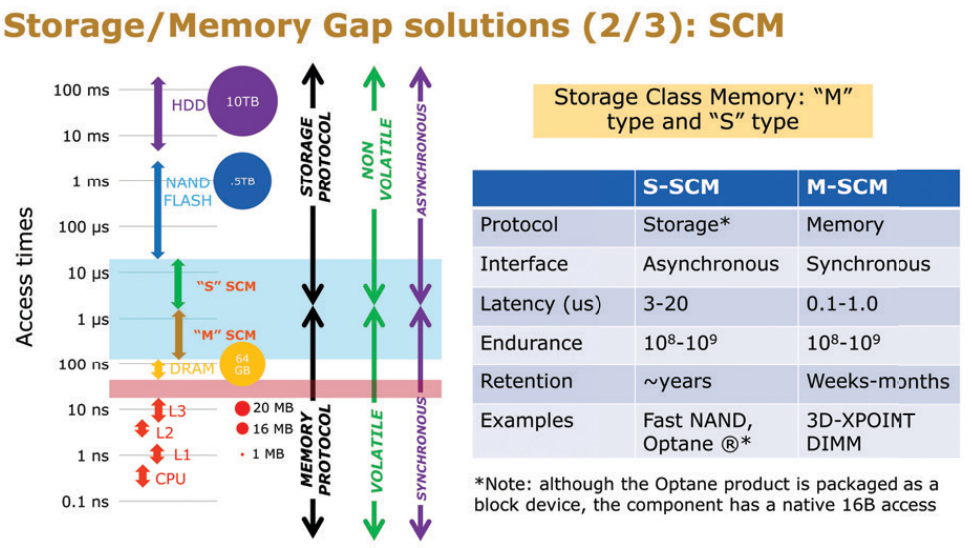


FIGURE 1. Optane DIMM reaches 'broad availability' in 2019.

Al Fazio, a senior fellow at Intel who participated in the memory-related evening panel at the VLSI symposia, and said that the early adopters of the Optane technology have seen significant benefits: one IT manager told Fazio that



	S-SCM	M-SCM
Protocol	Storage*	Memory
Interface	Asynchronous	Synchronous
Latency (us)	3-20	0.1-1.0
Endurance	10^8-10^9	10^8-10^9
Retention	~years	Weeks-months
Examples	Fast NAND, Optane ®*	3D-XPOINT DIMM

FIGURE 2. The drawback to phase change memories, such as 3D XPoint, is the relatively high write-energy-per-bit. Source: Chris Petti, Western Digital, short course presentation at 2018 Symposium on VLSI Circuits.

by adding a layer of Optane SSD-based memory he was able to rebuild a database in seconds versus 17 minutes previously. Fazio said he takes particular pride in the fact that, because of Optane, some doctors are now able to immediately read the results of magnetic resonance imaging (MRI) tests.

"An MRI now takes two minutes instead of 40 minutes to render," Fazio said, adding that a second-generation of 3D Xpoint is being developed which he said draws upon "materials improvements" to enhance performance.

Chris Petti, a senior director of advanced technology at Western Digital, said DRAM pricing has been "flat for the last five to seven years," making it more expensive to simply add more DRAM to overcome the latency gap between DRAM and flash. "DRAM is not scaling so there are a lot of opportunities for a new technology" such as Optane or the fast NAND technologies, he said. Samsung is working on a single-bit-per-cell form of Fast NAND.

In a Monday short course on emerging memory technologies at the Symposium on VLSI Circuits, Petti said the drawback to phase change memories (PCMs), such as 3D XPoint, is the relatively high write-energy-per-bit (**FIGURE 2**), which he estimated at 460 pJ/bit, compared with 250 pJ/bit for standard NAND (based on product spec sheets). In terms of cost, latency, and endurance, Petti judged the PCM memories to be in the "acceptable" range. While the price is five to six times the price-per-bit of standard NAND, Petti noted that the speed improves "because PCM (phase change memory) is inherently faster than charge storage."

Phase-change materials, such as $Ge_2Sb_2Te_5$, change between two different atomic structures, each of which has a different electronic state. A crystalline structure allows electrons to flow while an amorphous structure blocks the flow. The two states are changed by heating the PCM bit electrically.

Philip Wong, a Stanford University professor, said the available literature on PCM materials shows that they can be extremely fast; the latencies at the SSD and DIMM levels are largely governed by "protocols." In 2016, a team of Stanford researchers said the fundamental properties of phase-change materials could be as much as a thousand times faster than DRAM.

In a keynote speech at the VLSI symposia, Scott DeBoer, executive vice president of technology development at Micron (Boise, Idaho), said "clearly the most successful

of the emerging memories is 3D XPoint, where the technology performance has been proven and volume production is underway. 3D XPoint performance and density are midway between DRAM and NAND, which offers opportunities to greatly enhance system-level performance by augmenting existing memory technologies or even directly replacing them in some applications."

Currently, the 3D XPoint products are made at a fab in Lehigh, Utah. The initial technology stores 128Gb per die across two stacked memory layers. Future generations can either add more memory layers or use lithographic pitch scaling to increase die capacity, according to Micron.

DeBoer noted that "significant system-level enablement is required to exploit the full value of 3D XPoint memory, and this ongoing effort will take time to fully mature."

eMRAM race begins by major foundries

Magnetic RAM technology has been under serious development for three decades, resolving significant hurdles along the way with breakthroughs in MgO magnetic materials and device architecture. Everspin Technology has been shipping discrete MRAM devices for nearly a decade, and the three major foundries are readying embedded MRAM for SoCs, automotive ICs, and other products. The initial target is to replace NOR-type flash on devices, largely due to the large charge pumps required to program NOR devices which add multiple mask layers.

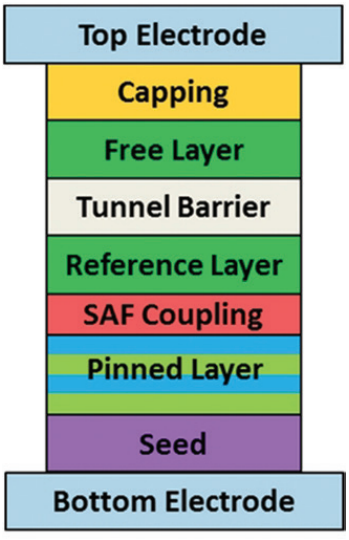


FIGURE 3. MRAM performance is largely controlled by the quality of the PVD-deposited layers in the MTJ (SAF is synthetic antiferromagnetic). Source: Lin Xue, et al, Applied Materials presentation at 2018 Symposium on VLSI Technology.

GlobalFoundries, which manufactures the Everspin discrete devices, has qualified eMRAM for its 22nm FD-SOI process, called 22FDX. TSMC also has eMRAM plans.

At the Symposium on VLSI Technology, Samsung Foundry (Giheung, Korea) senior manager Yong Kyu Lee described an embedded STT-MRAM in a 28-nm FDSOI logic process, aimed at high-speed industrial MCU and IoT applications. Interestingly, Lee said compared with the bulk (non-SOI) 28-nm process, the FD-SOI technology "has superior RF performance, low power, and better analog characteristics than 28-nm bulk and 14-nm FinFET CMOS." Lee indicated that the FD-SOI-based eMRAM would be production-ready later this year.

Samsung ported its STT perpendicular-MTJ (magnetic tunnel junction) eMRAM technology from its 28-nm bulk to its FD-SOI CMOS process. The company offers the eMRAM as a module, complementing an RF module. The "merged embedded STT MRAM and RF-CMOS process is compatible to the existing logic process, enabling reuse of IP," he said.

Looking forward to the day when MRAM could complement or replace SRAM, Lee said "even though we have not included data in this paper, our MTJ shows a potential for storage working memory due to high endurance (>1E10) and fast writing (<30ns).

Beyond embedded to last level cache

As foundries and their customers gain confidence in eMRAM's retention, power consumption, and reliability, it will begin to replace NOR flash at the 40-nm, 28-nm, and smaller nodes. However, future engineering improvements are needed to tackle the SRAM-replacement.

SRAM scaling is proving increasingly difficult, both in terms of the minimum voltages required and the size of the six-transistor-based bits. MRAM researchers are in hot pursuit of the ability to use replace some of the SRAM on processors with Last Level Cache (LLC) iterations of magnetic memory. These LLC MRAMs would be fabricated at the 7nm, 5nm, or beyond nodes.

Mahendra Pakala, senior director of memory and materials at the Applied Materials Advanced Product Technology Development group, said for eMRAM the main challenges now are achieving high yields with less shorting between the magnetic tunnel junctions (MTJs). "The big foundries have been working through those problems, and embedded MRAM is getting closer to reality, ramping up sometime this year," he said.

For LLC applications, STT-MRAM has approached SRAM and DRAM performance levels for small sample sizes. At the VLSI symposium, researchers from Applied Materials, Qualcomm, Samsung, and TDK-Headway, all presented work on SRAM cache-type MRAM devices with high performance, tight pitches, and relatively low write currents.

Applied's VLSI symposium presentation was by Lin Xue, who said the LLC-type MRAM performance is largely controlled by the quality of the PVD-deposited layers in the MTJ (**FIGURE 3**), while yields are governed by the ability to etch the MTJ pillars efficiently. Etching is extremely challenging for the tight pitches required for SRAM replacement, since the tight-pitch MTJ pillars must be etched without redepositing material on the sidewalls.

Deposition is also difficult. The MTJ structures contain multiple stacks of cobalt and platinum, and the thickness of the multilayers must be reduced to meet the 7nm node requirements. Any roughness in the interfaces creates secondary effects which reduce perpendicular magnetic anisotropy (PMA). "The performance is coming from the interface, essentially. If you don't make the interface sharp, you don't end up with the expected improvement in PMA," Pakala said.

Applied has optimized a PVD process for deposition of the 15-plus layers of many different materials required for the magnetic tunnel junctions. Pakala said the PVD technology can sputter more than 10 different materials. The Endura-based system uses a multi-cathode approach, enabling each chamber to have up to five targets. With a system of seven chambers, companies can deposit the required variety of materials and, if desired, increase throughput by doubling up on the targets.

The system would include a metrology capability, and because the materials are easily oxidized, the entire system operates at vacuum levels beyond the normal 10E-8 Torr level. For MRAM deposition, operating at 10 to minus 9 or even 10 to minus 10 Torr levels may be required.

"When we start talking about the 7 and 5 nanometer nodes for SRAM cache replacement, the cell size and distances between the bits becomes very small, less than 100 nm from one MTJ to another. When we get to such small distances, there are etching issues, mainly redepositing on the sidewalls. The challenge is: How do we etch at reduced pitch without shorting?" Pakala said.

"Integrated thermal treatment and metrology to measure the thicknesses, all of which has to be done at extremely low vacuum, are major requirements," he said. "At this point it is not a question of the basic physics. For MRAM, it is, as they say, 'just engineering' from here on out," he said.

Layout schema generation: Improving yield ramp during technology development

WAEL ELMANHAWY *and* **JOE KWAN**, *Mentor Graphics, Beaverton, OR*

Layout schema generation generates random, realistic, DRC-clean layout patterns of the new design technology for use in test vehicles

Predicting and improving yield in the early stages of technology development is one of the main reasons we create test macros on test masks. Identifying potential manufacturing failures during the early technology development phase lets design teams implement upstream corrective actions and/or process changes that reduce the time it takes to achieve the desired manufacturing yield in production. However, while conventional yield ramp techniques for a new technology node rely on using designs from previous technology nodes as a starting point to identify patterns for design of experiment (DoE) creation, what do you do in the case of a new design technology, such as multi-patterning, that did not exist in previous nodes? The human designer's experience isn't applicable, since there isn't any knowledge about similar issues from previous designs. Neither is there any prior test data from which designers can draw feedback to create new test structures, or identify process or design style optimizations that can improve yield more quickly.

An innovative new technology, layout schema generation (LSG), enables design teams to generate additional macros to add to test structures without relying on past designs for input. These macros are based on the generation and random placement of unit patterns that can construct more meaningful larger patterns. Specifications governing the relationships between those unit patterns can be adjusted to generate layout clips that look like realistic designs. Those layout clips can then be used in design of experiment (DoE) trials to predict yield, and identify potential design and process optimizations that will help improve yield. By using this new LSG process, designers can significantly reduce the time it takes to achieve the desired yield for designs that include new design techniques.

Issues affecting yield

Wafer yield is typically reduced by three categories of defects. The first category comprises random defects, which occur due to the existence of contamination particles in the different process chambers. A conducting particle can short out two or more neighboring wires, or create a leakage path. A non-conducting particle or a void can open up a wire or a via, or create high resistive paths. **FIGURE 1** shows scanning electron microscope (SEM) images of these two types of random defects.

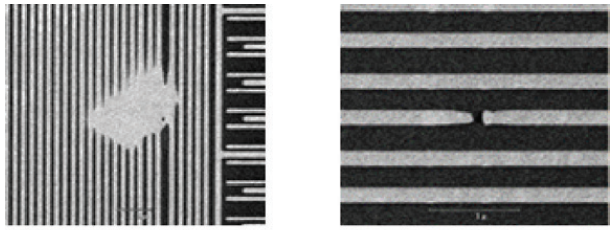


FIGURE 1. Random defects caused by contamination particles.

The second category contains systematic defects, which occur due to an imperfect physical layout architecture, or the impact of non-optimized optical process recipes and/or equipment. Systematic defects are typically the biggest source of yield detraction [1], but a majority of them can be eliminated through design-technology co-optimization (DTCO), in which the design and process sides communicate more freely to achieve faster rates of improvement.

The third category, which we're not addressing in this article, includes parametric defects (such as a lack of uniformity in the doping process) that may affect the reliability of devices.

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Layout schema generation

To demonstrate the use and applicability of the LSG process, let's look at designs that use the self-aligned multi-patterning (SAMP) process. Multi-patterning (MP) technology with ArF 193i lithography is currently the preferred choice over extreme ultraviolet (EUV) lithography for advanced technology nodes from 20 nm on down. At 7 nm and 5 nm nodes, the SAMP process appears to be one of the most effective MP techniques in terms of achieving a small pitch of printed lines on the wafer, but its yield is in question. Of course, before being deployed in production, it must be thoroughly tested on test vehicles. However, without any previous SAMP designs, design of an appropriate test vehicle is challenging. In addition to the lack of historical test data, the unidirectional nature of the SAMP design complicates the design of the conventional serpentine and comb test shapes, which contain bidirectional components.

Self-aligned multi-patterning process

In the SAMP process [3], the first mask is known as the mandrel mask. Sacrificial mandrel shapes are printed with a relaxed pitch, and then used to develop sidewalls. The sidewalls are at half the mandrel's pitch. Depending on the tone, target shapes may exist in the spaces between the sidewalls. The target shapes can be reused as sacrificial mandrel shapes to form another generation of sidewalls. Wafer shapes that don't have corresponding mask shapes are called non-mandrel shapes. This process can be repeated to achieve SAMP layouts with a reduced pitch. The SAMP process (**FIGURE 2**) restricts the designs to be almost unidirectional. Generated parallel lines will be cut later by a cut mask at the desired line ends to form the correct connectivity.

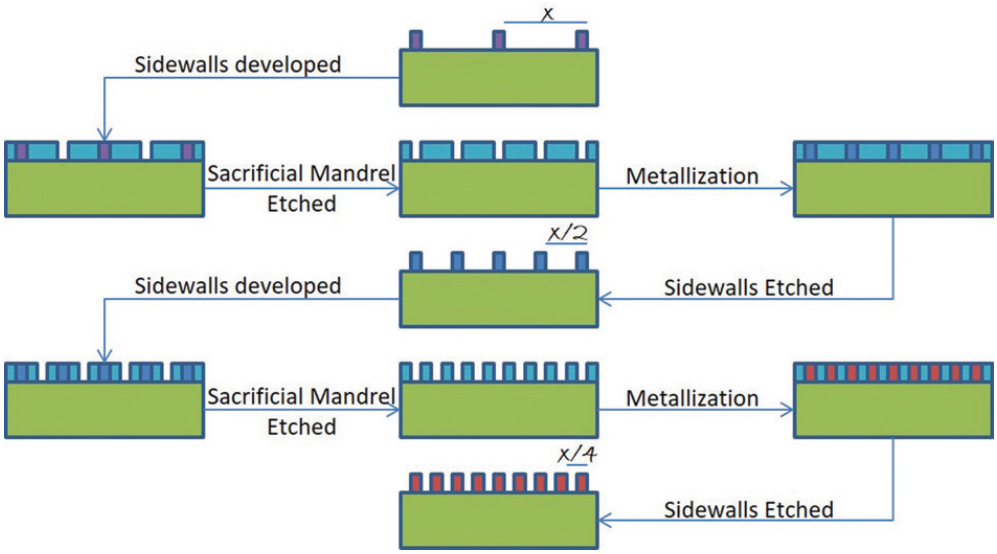

FIGURE 2. Basic schematic of SAMP process.

Test vehicles

A test vehicle is typically a subset of the masks for a design, designed specifically to induce potential systematic failures or lithographic hotspots on the layer under test. It may also contain some test structures specially designed for the detection of random defects. The main components in a test vehicle for any new node are serpentine and comb shapes (to capture random defects), and preliminary standard cell designs (with many variations, to assess their quality). Other structures are typically added based on experience derived from production chips of previous nodes.

In a new node, all test structures on the test vehicle are vital for process training and characterization. Feedback from the test process is used for design style optimization. For example, when "bad" layout geometries are discovered after manufacturing, they can be captured as patterns, assigned low scores, and stored in a design for manufacturing (DFM) pattern library [2]. The designer can then use DFM analysis to find the worst patterns in a given layout, and modify or eliminate them. Such early DTCO provides a faster yield ramp for new nodes. Even in mature nodes, test structures are used on production wafers to identify additional opportunities for process refinement and optimization, which will have a positive impact on future yield.

One of the obstacles in test vehicle design is that it depends mainly on human designer's experience and memory. Although experienced designers have seen multiple design styles in older nodes, the design shapes they are familiar with are limited to those styles. It typically takes a long time to design new test structures that cover new shapes, especially for a new process. The LSG solution adds more macros (generated in a random fashion) to the standard test structures strategy to speed up new shape yield analysis.

Random test pattern generation

The key component of the LSG solution is a method for the random generation of realistic design-like layouts, without design rule violations. The LSG process uses a Monte Carlo method to apply randomness in the generation of layout clips by inserting basic unit patterns in a grid. These unit patterns represent simple rectangular and square

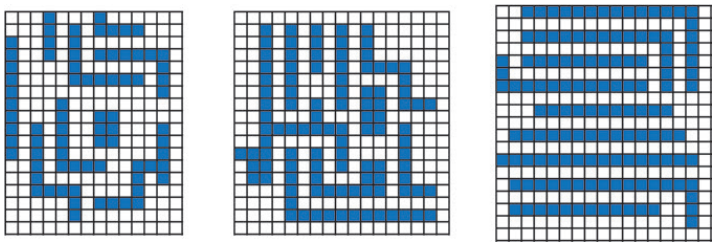

FIGURE 3. Realistic DRC-clean clips generated by a layout schema generation process.

polygons, as well as a unit pattern for inserting spaces in the design. Unit pattern sizes depend on the technology pitch value. During the generation of the layouts, known design rules are applied as constraints for unit pattern insertion. Once the rules are configured, an arbitrary size of layout clips can be generated (**FIGURE 3**).

To begin, the SAMP design rules are converted to a format readable by an automated LSG tool like the Calibre® LSG tool from Mentor, a Siemens Business. Once the rules are configured, the Calibre LSG process can automatically generate an arbitrarily wide area of realistic DRC-clean SAMP patterns. The area is only limited by the floorplan of the designated macro of SAMP test structures. Test patterns can be also generated with power rails to mimic the layouts of standard cells. **FIGURE 4** shows a sample clip of the generated output layout. To be ready for the experiments, the SAMP design is decomposed into the appropriate mandrel and cut masks, according to the decomposition rules. This operation also distinguishes between mandrel and non-mandrel shapes.

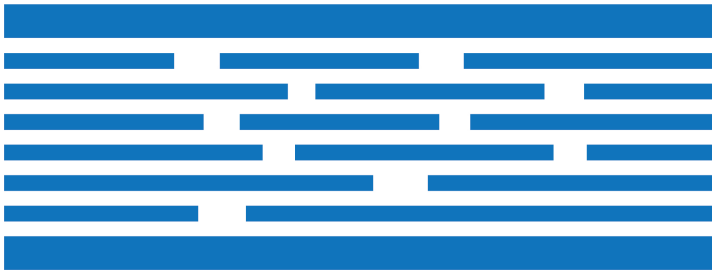

FIGURE 4. SAMP clip generated by automated LSG process.

Design of Experiment

In the design phase of the test vehicle, the generated SAMP patterns are added to the typical contents of regular test patterns. The random SAMP patterns are electrically meaningless, unless they are connected to other layers to set up the required experiment. The DoE determines the way the connections are made from the patterns up to the testing pads, to detect different fail modes. Fail modes include short circuits due to lithographic bridging or conducting particles, and open circuits due to lithographic pinching, non-conducting particles, voids, or open vias.

A via chain can be constructed to connect the random DoE of SAMP structures through a routing layer to external pads for electrical measurement. These clips are decomposed according to the decomposition rules of the technology into the appropriate mandrel and cut masks. The decomposed clips can be tested through simulations, or electrically on silicon to discover hotspots. The discovered hotspots can be analyzed to determine root cause, which can be used to modify design layouts and/or optimize the fabrication process and models to eliminate these hotspots in future production. They can also be used as learning patterns for DFM rule deck development. By expanding the size of the randomly generated test structures, more hotspots can be detected, which can provide an even faster way to enhance the yield of a new technology node.

To demonstrate the effectiveness of the LSG process, we performed two experiments on a set of SAMP patterns similar to those shown in **FIGURE 4**.

Detecting random conducting particles

The first experiment collected data about random defects caused by conducting particles. In this experiment, all mandrel shapes are connected through the upper (or lower) via and metal layers, up to a testing pad. All non-mandrel shapes are connected in the same way to another testing pad. The upper routing layer forms two interdigitated comb shapes. **FIGURE 5** shows a layout snippet of the connections. All via placements and upper metal routings were made with a custom script, without the intervention of a human designer. Ideally the two testing pads should be disconnected, as no mandrel shape can touch a non-mandrel shape. If the testing probes are found to be connected, this likely indicates a random conducting particle defect, or a lithographic bridge. The localization and analysis of such defects [4] can help with yield estimation and enhancement.

Detecting systematic cut mask resolution problems

One example of a systematic lithographic defect found in SAMP designs is when the cut mask is not resolved correctly. This causes two shapes on the same track to be shorted out through the unresolved cut shape. The testing of such a case requires connecting every other polygon on the same track. This was done with a generating script, without the intervention of human designers.

FIGURE 6 shows a snippet of the generated layout with the connections. If the test probes are found to be connected while the two pads (ideally) are disconnected, this may indicate an unresolved cut shape. The analysis of the defect location and data from multiple wafers can prove the root cause of the defect.

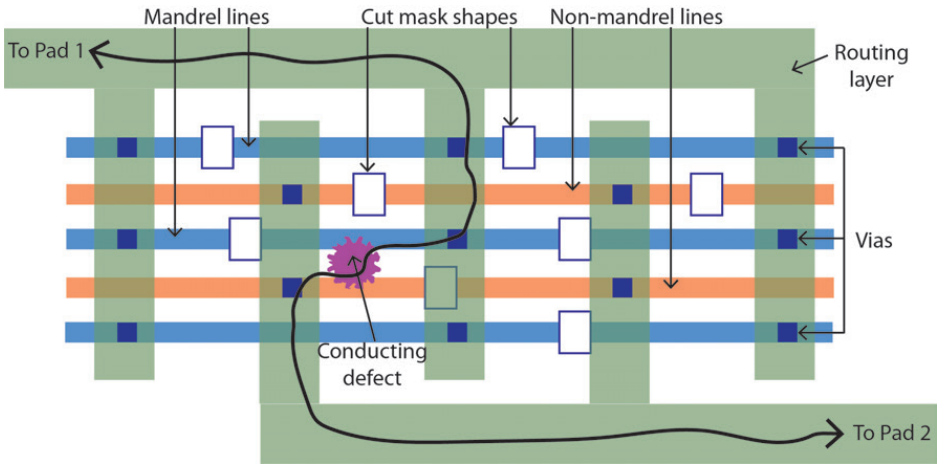

FIGURE 5. DoE for the detection of defects caused by conducting particles.

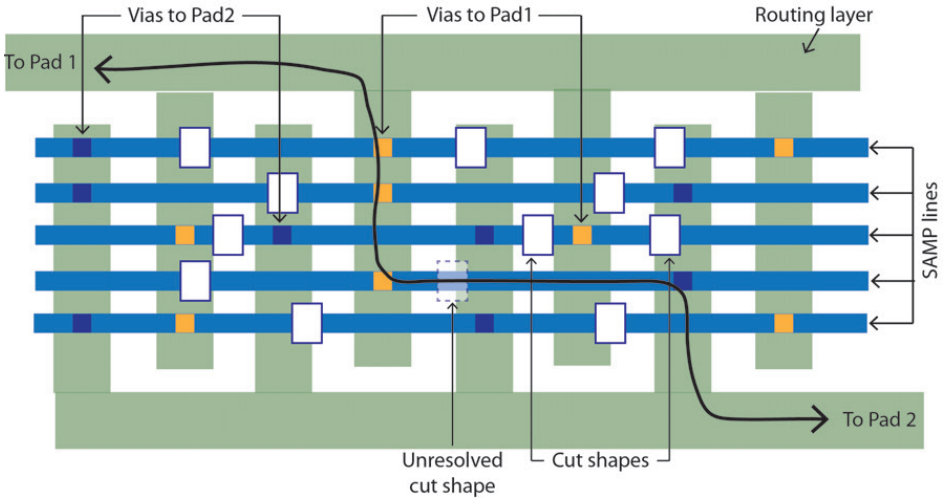

FIGURE 6. DoE for the detection of unresolved cut shapes.

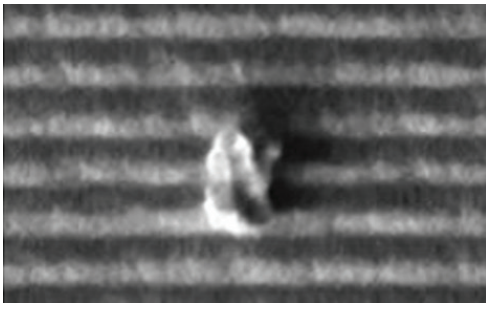

FIGURE 7. SEM image of a conducting defect shorting out mandrel and non-mandrel shapes.

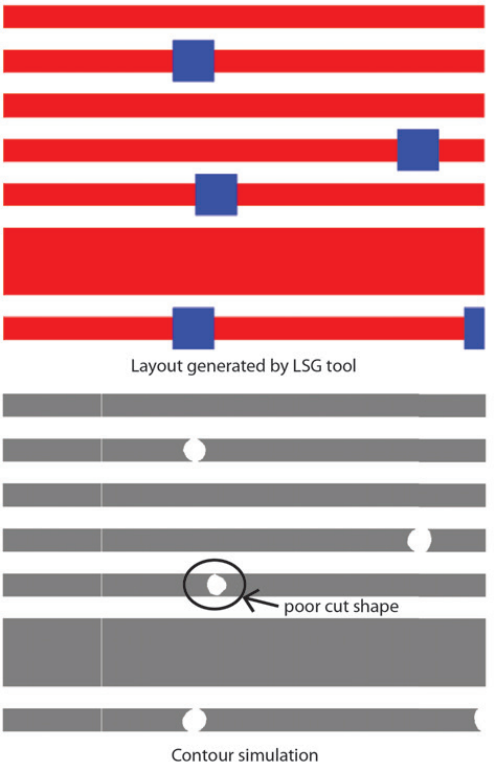

FIGURE 8. Systematic defect caused by poor cut shape.

Results

The two experiments described above were placed on a test vehicle of an advanced node. The test macro containing the first experiment setup successfully detected several conducting particle defects. A sample SEM image of the discovered defect is shown in **FIGURE 7**. Statistical data from multiple wafers were used to model the defect density and estimate the yield target.

Repetitive fail data from the test macro of the second experiment indicated systematic failures at particular locations. The analysis showed that the root cause of the failure was a poorly resolving cut shape in some process corners, as was predicted in the DoE. **FIGURE 8** shows a snippet of the generated layout and its contour simulation.

To test the effectiveness of the random approach in capturing defects, 20 SAMP design clips were generated with linearly increasing sizes, such that the 20th clip was 20X bigger than the first clip. Lithography simulations were executed on the cut mask to inspect potential failures. The contours were checked, and potential failures were identified and categorized. **FIGURE 9** shows the number of the unique hotspots found in each clip. The graph shows that the number of identified hotspots tends to saturate with the chip size. The second clip has 2X the number of

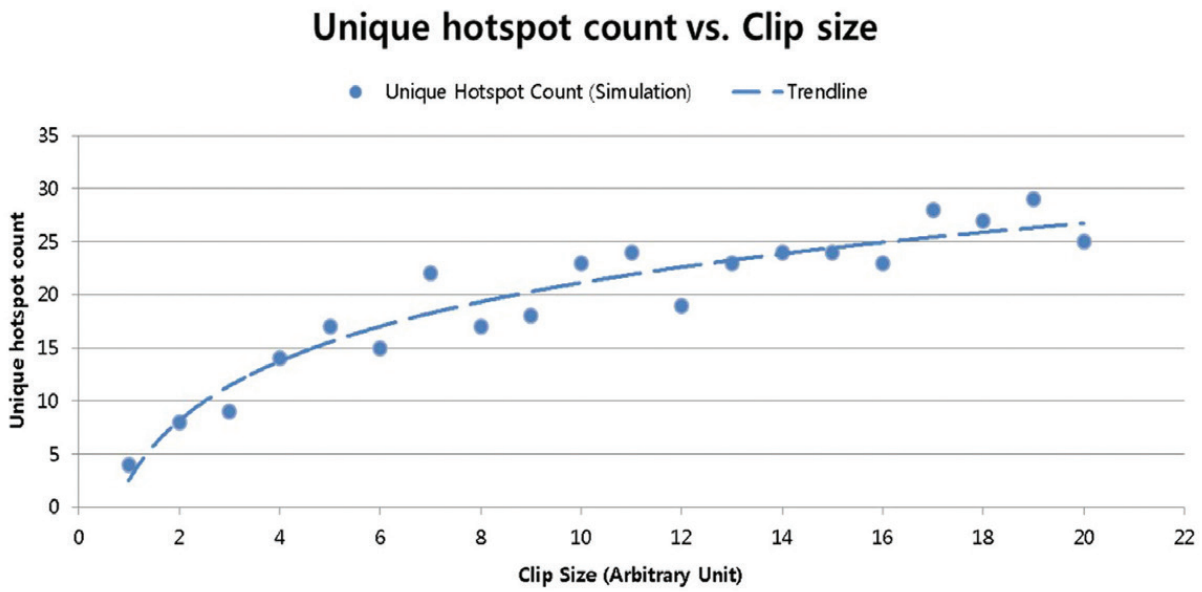

FIGURE 9. Unique hotspot count tends to saturate as the randomly generated clip size is increased.

unique hotspots found in the first clip, while the 20th clip only sees around a 6X increase. This result is expected, as many hotspots in the larger clips are just replicas of those found in the small clips. Assuming that the LSG tool is configured correctly, this result means most of the potential hotspots can be covered in a reasonable size test vehicle.

Conclusion

Test vehicles are vital for yield ramp up in new technologies and yield enhancement in mature nodes, but it can be difficult to design accurate test structures for new design styles and technologies that have no relevant history. Innovative techniques are needed to achieve comprehensive coverage of potential manufacturing failures created by new design styles, while ensuring full compliance with known design rule checks. A new solution using layout schema generation generates random, realistic, DRC-clean layout patterns of the new design technology for use in test vehicles. Experiments with this technology show it can provide high coverage of new design styles for an arbitrarily-wide design area. Circuitry can be added to the generated clips to make them electrically measurable for the detection of potential failures. The ability to discover lithographic hotspots and systematic failures early in the technology development process is significantly improved, at the expense of additional testing area. This design/technology co-optimization speeds up the yield optimization for new technology nodes, improving a critical success factor for market success.

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Automotive defect sensitivity requirements

DAVID W. PRICE, **DOUGLAS G. SUTHERLAND**, **JAY RATHERT**, **JOHN MCCORMACK** *and* **BARRY SAVILLE**,
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Author's Note: *The Process Watch series explores key concepts about process control—defect inspection, metrology and data analytics—for the semiconductor industry. This article is the third in a series on process control strategies for automotive semiconductor devices. For this article, we are pleased to include insights from our colleagues at KLA-Tencor, John McCormack and Barry Saville.*

Semiconductors continue to grow in importance in the automotive supply chain, requiring IC manufacturers to adapt their processes to produce chips that meet automotive quality standards. The first article in this series [1] focused on the fact that the same types of IC manufacturing defects that cause yield loss also cause poor chip reliability and can lead to premature failures in the field. To achieve the high reliability required in automotive ICs, additional effort must be taken to ensure that sources of defects are eliminated in the manufacturing process. The second article in this series [2] outlined strategies, such as frequent tool monitoring and a continuous improvement program, that reduce the number of defects added at each step in the IC manufacturing process. This article explores how to drive tool monitoring to a higher level of performance in order to help automotive IC manufacturers achieve chip failure rates below the parts per billion level.

As a reminder, tool monitoring is the established best practice for isolating the source of random defectivity contributed by the fab's process tools. During tool monitoring, a bare wafer is inspected to establish its baseline defectivity, run through a specific process tool (or chamber), and then inspected again. Any defects that were added to the wafer must have come from that specific process tool. This method can reveal the cleanest "golden" tools in the fab, as well as the "dog" tools that contribute the most defects and require corrective action. With plots of historical defect data from the process tools, goals and milestones for continuous improvement can be implemented.

When semiconductor fabs design their tool monitoring strategy, they must decide on the minimum size of defects that they want to detect and monitor. If historical test results have shown that smaller defects do not impact yield, then fabs will run their inspection tools at a lower sensitivity so that they no longer detect these smaller defects. By doing this, they can focus only on the larger yield-killer defects, avoiding distraction from the smaller "nuisance" defects. This approach works for a consumer fab that is only trying to optimize yield, but what about the automotive fab? Recall that yield and reliability issues are caused by the same defects types – yield and reliability defects differ only in their size and/or where they land on the device pattern. [2] Therefore, a tool monitoring strategy that leaves the fab blind to smaller defects may be missing the very defects that will be responsible for future reliability issues.

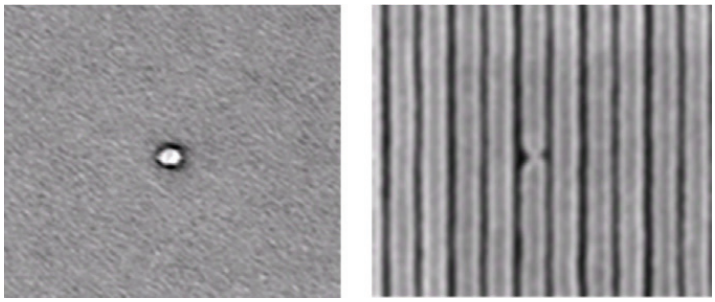

FIGURE 1. The left image shows small particle created at a deposition layer. The right image shows the exact same location on the wafer after the metal 1 pattern formation. The metal line defect was caused by the small particle at the prior deposition layer. This type of deformity in the metal line could easily become a reliability issue in the field.

Moreover, it's important to understand that defects that seem small and inconsequential at one process layer may have a dramatic impact later in the process flow – their impact can be exacerbated by the subsequent process steps. The two SEM images in **FIGURE 1** were taken at exactly the same location on the same wafer, but at different steps of the manufacturing process. The image on the left shows a single, small defect that was found on the wafer after a deposition layer. This defect was previously thought to

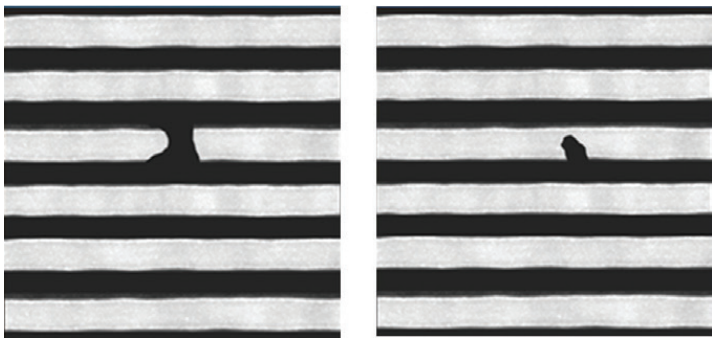

FIGURE 2. The image on the left shows a full line open, while the right image shows a ~50% line open. The chip on the left will fail at sort (assuming there is no redundancy). The chip on the right may pass electrical wafer sort but is a reliability risk in the field.

be a nuisance defect with no negative effect on the die pattern or chip performance. The image on the right shows that same deposition defect after metal 1 pattern formation. The presumed nuisance defect has altered the quality of the metal line printed several process steps later. This chip might pass electrical wafer sort, but this type of metal deformity could easily become a reliability issue in the field when activated by automotive environmental stressors.

So how does an automotive IC fab determine the smallest defect size that will pose a reliability risk? To start, it is important to understand the impact of different defect sizes on reliability. Consider, for example, the different magnitudes of a line open defect shown in **FIGURE 2**. A chip that has a pattern structure with a full line open will likely fail at electrical wafer sort and thus does not pose any reliability risk. A chip with a 50% line open – a line that is pinched or otherwise restricted to ~50% of its cross-sectional area – will likely pass electrical wafer sort but poses a significant reliability risk in the field. If this chip is used in a car, environmental conditions such as heat, humidity and vibrations, can cause degradation of this defect to a full line open, resulting in chip failure.

As a next step, it is important to understand how different size defects affect a chip's pattern integrity. More specifically, what is the smallest defect that will result in a line open? What is the smallest defect that will result in a 50% line open?

FIGURE 3 shows the results of a Monte Carlo simulation that models the impact of different size defects introduced at a BEOL film deposition step. Minimum defect size is plotted on the vertical axis against varying metal layer pitch dimensions. This data corresponds to the metal 1 spacing for the 7nm, 10nm, 14nm and 28nm design nodes, respectively.

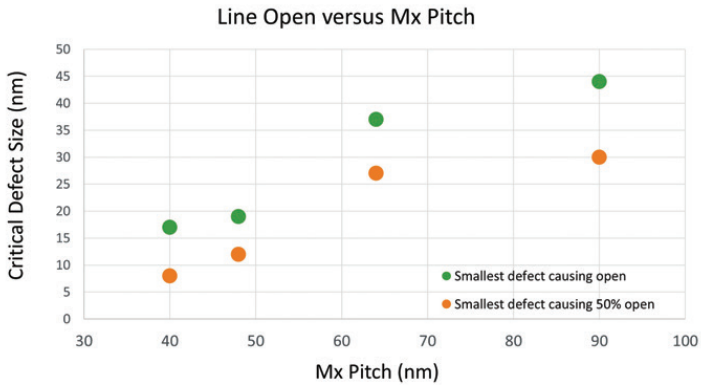

FIGURE 3. The green data points show the minimum defect size required to cause a full line open at the minimum metal pitch. The orange data points show the minimum defect size needed to cause a 50% line open. The x-axis is the metal 1 spacing for the 7nm (far left data point), 10nm, 14nm and 28nm (far right data point) design nodes.

The green data points correspond to the smallest defects that will cause a full line open and the orange data points correspond to the smallest defects that will produce a 50% line open (i.e., a potential reliability failure). In each case the smallest defect that will cause a potential reliability failure is 50-75% of the smallest defect that will cause a full line open.

These modeling results imply that to control for, and reduce, the number of *reliability* defects present in the process, fabs need to capture smaller defects. Therefore, they require higher sensitivity inspections than what is required for yield optimization. In general, detection of reliability defects requires an inspection sensitivity that is one node ahead of the current design node plan for yield alone. Simply put, a fab's previous standards for reducing defectivity to optimize yield will not be sufficient to optimize reliability.

Increasing the sensitivities of the tool monitoring inspection recipes, or in some cases, using a more

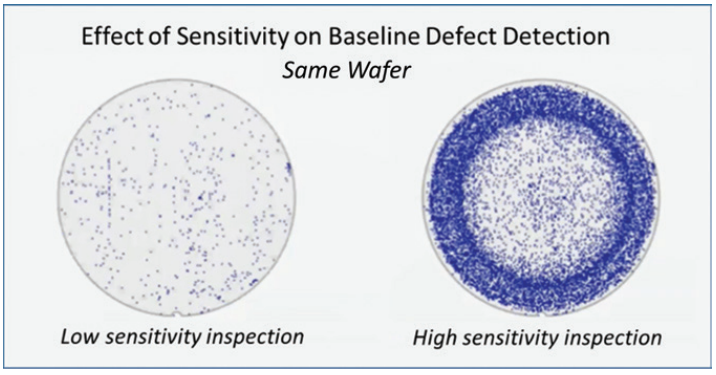

FIGURE 4. Hidden defect signatures that may impact reliability are often revealed with appropriate tool monitoring sensitivity. Zero Defect standards require corrective action on the process tool contributing these defects.

capable inspection system, will find smaller defects and possibly reveal previously hidden signatures of defectivity, as in **FIGURE 4**. While these signatures may have had a tolerable impact on yield in a consumer fab, they represent an unacceptable risk to reliability for automotive fabs pursuing continuous improvement and Zero Defect standards.

There are several important unpatterned wafer defect inspection factors for a fab to consider when creating a strategy to improve tool monitoring inspection sensitivity to find the small, reliability-related defects contributed by process tools. First, it is important to recognize that in a mature fab where yields are already high, there is rarely a single process layer or module that will be the "silver bullet" to reducing defectivity adequately to meet reliability improvement goals. Rather, it is sum of small gains across many layers that produce the desired gains in reliability. Because yield and the associated reliability improvements are cumulative across layers, reliability gains achieved through process tool monitoring using unpatterned wafer inspection are best demonstrated using a multi-layer regression model:

$$Yield = f(Ys) + f(SFS1) + f(SFS2) + f(SFS3) + \ldots.. f(SFSN) + error$$

- Ys = systematic yield loss (not particles related)
- SFS_x = cumulative Sursfcan unpatterned wafer inspection detected particles for many layers
- Error = Yield loss mechanisms not detected by Surfscan

This implies that reliability improvements require a fab's commitment to continuous improvement in defectivity levels across all processes and process modules.

Second, the fab should consider the quality of the bare wafer used for process tool monitoring. Recycling bare wafers increases the surface roughness with each cycle, an attribute known as haze. This haze level is fundamentally noise that affects the inspection system's ability to differentiate the signal of smaller defects. Variability in haze across the population of test wafers acts as a limit to overall inspection recipe capability, requiring normalization, calibration and haze limits to reduce the impact of this noise source on defect sensitivity.

Next, the fab should ensure that the monitor step closely mimics the process that a production, patterned wafer follows. Small time-saving deviations in the monitor wafer flow to short cut the process may inadvertently skip the causal mechanism of defectivity. Furthermore, an over-reliance on mechanical handling checks alone bypasses the process completely and misses the critical contribution the process plays in particle generation.

When increasing the inspection recipe sensitivity, the fab must co-optimize both the "pre" and "post" inspection together. Often cycling the bare wafer through a process step can "decorate" small pre-existing defects on the wafer that were initially below the detection threshold. Once decorated, the defects now appear bigger and are more easily detected. In an unoptimized "post" inspection, these decorated defects can look like "adders," leading to a false alarm and inadvertent process tool down time. Optimizing the inspections together maximizes the sensitivity and increases the confidence in the excursion alarms while avoiding time-consuming false alarms.

Lastly, it is important to review and classify the defects found during unpatterned inspection to correlate their relevance to the defects found at the equivalent patterned wafer process step. Only then can the fab be confident that the source of the defects has been isolated and appropriate corrective action has been taken.

To meet the high reliability demands of the automotive industry, IC manufacturers will need to go beyond simply monitoring and controlling the number of yield limiting defects on the wafer. They will need to improve the sensitivity of their tool monitoring inspections to one node smaller than what would historically be considered relevant. Only with this extra sensitivity can they detect and eliminate defects that would otherwise escape the fab and cause premature reliability failures. Additionally, when implementing a tool monitoring strategy, fabs need to carefully consider multiple factors, such as monitor wafer recycling, pre and post inspection sensitivity and the importance of a fab-wide continuous improvement program. With so much riding on automotive semiconductor reliability, increased sensitivity to smaller defects is an essential part of an optimal Zero Defect continuous improvement program.

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Solving the burden of Bourdon tubes

BRIAN SULLIVAN, *Valin Corporation, San Jose, CA*

Mini diaphragm gauges offer a new alternative to Bourdon tubes.

Fabs and OEMs in the semiconductor industry face a number of difficult challenges today, specifically in the etch and deposition/thin film processes. These incredibly specialized processes require extremely clean gases and vaporized chemical sources. The fabs and their process tools utilize gas delivery systems to provide these ultra-pure materials from their bulk sources to their process tools and systems. The increased use of highly aggressive and reactive gases in these processes has caused one very specific problem. These aggressive gases are picking up moisture (through leaks, flawed component installations, improper purging, poor PM practices, etc.) and then attacking and corroding the bourdon tubes located within the pressure gauges in the impacted lines. In a few instances, leaks have been created through these stressed system components.

Millions of dollars are spent inside the fabs and by OEMs to have a highly electropolished finish on the internal wetted surfaces of the many components that comprise their gas delivery systems. The gauges themselves have not been found to be the originating source of the leaks. Instead, the leaks form elsewhere, and the moisture laden and now highly corrosive gas immediately attacks the least corrosion resistant components found within the delivery line. Unfortunately, the bourdon tubes found in most "ultra-high purity (UHP) gauges" today are a principal target. When this type of event occurs, it doesn't take long for the exposed gauges to fail.

The root of this problem lies in the fact that a standard pressure gauge's main functioning component is typically an un-passivated, or only marginally passivated, bourdon tube. This tube is open to pressure on one end and welded closed at the other, a design invented by Eugene Bourdon more than 165 years ago. This is the principal weakness and ultimately leaves these gauges subject to corrosion.

As pressure enters this thin, hollow, C-shaped bourdon tube, it causes the tube to flex outward from its relaxed, round shape, stretching it up and away from its original form and position. The tip of the bourdon tube is connected to linkage that moves a pointer around the internal dial (or face) of the gauge, indicating the pressure the gauge is currently measuring. Of course, flexing components made of stainless steel – particularly if they aren't fully electropolished like the tubing, fittings, valves, regulators, and other components in the delivery system's line – become vulnerable to chemical attack through the micro fissures formed by the flexures they experience. Each time a bourdon tube flexes, it can suffer the creation of micro fissures. Over time these can then grow into macro fissures, and then ultimately create internal cracks or complete breaks in the bourdon tube's integrity. Throughout the life of a typical pressure/vacuum gauge in a dynamic system, going through gas source changes, pressure spikes, cycle purge sequences, and other events, the flexing bourdon tube will be subjected to the formation of countless micro fissures. If they are then exposed to a corrosive gas that has become aggressive through the introduction of moisture, it should be no surprise that the bourdon tubes will be aggressively assailed and damaged in the process.

It is well known throughout the industry that aggressive corrosive gases transported through the gas lines increase the likelihood of both internal particle generation and outbound leaks from any vulnerable component. Of course, the presence of any entrained moisture compounds the probability greatly. Any time a minimal quantity of atmospheric moisture makes its way into these corrosive gas lines, it will convert the corrosive gasses into corrosive acids. The bourdon tube acts as a dead leg in the system and is an ideal place for the corrosive gas to enter but does not allow it to get back out. Once the gas forms an acid, the acid will corrode any susceptible surface and generate an exit path by eating its way through the material. Many of the most vulnerable areas for this activity in a gas delivery system are the micro fissures found inside of bourdon tubes.

Although the process connection of a pressure gauge (typically a face seal fitting for semiconductor applications) will be fully passivated and electropolished and is clearly identified in the literature as such. The surface finish and Ra Max or Ra Average values of the bourdon tube itself is usually not provided. Gauge manufacturers measure their gauge connection's wetted surfaces, but when they

are asked about the bourdon tube, there is usually not a clear answer. The surface finish and passivation level of the bourdon tube inside the gauge is not disclosed in most cases. The reason for this is simple. Gauge manufacturers do not make a bourdon tube of electropolished and fully passivated stainless steel because the electropolishing process would damage the bourdon tube due to its thin, spring-like design. A bourdon tube must be able to flex to properly function and to do that it has to be made from thin metal.

Originally the industry used these "standard" bourdon tube gauges in non-critical applications because, compared to their more expensive transducer cousins, they were inexpensive, simple to use, and easy to obtain. However, as the industry has continued to evolve, and the processes used in the OEMs systems have required more aggressive and reactive gases, the use of these gauges has continued. Today, if decision makers want the best running and safest fabs their money can buy, they have to make a change.

The solution: mini diaphragm gauges

Engineers have been searching for a solution to the burden this issue presents to the fabs, and fortunately, a solution has been found and has proven itself to be both long-lasting and resilient.

Mini diaphragm gauges for both pressure and compound applications are now available that eliminate the bourdon tube completely. These mini diaphragm gauges employ a diaphragm made of Inconel®, which is highly flexible and extremely corrosion resistant. In an accelerated corrosion study, it exceeded the lifespan of a standard "UHP gauge" using a bourdon tube by a factor of twenty. This means that a gauge that would have lasted only six months in a corrosive application can now last up to ten years.

This Inconel® diaphragm will not suffer the effects of corrosion that its weaker, stainless steel bourdon tube counterpart does. It also removes the dead leg of the bourdon tube itself within the gauge. And all the wetted surfaces of these mini diaphragm pressure gauges are made of either fully electropolished 316L Stainless Steel (Ra <0.25 μm) or Inconel® 718. They also comply with SEMATECH and SEMI Standards.

In the mini diaphragm gauge, the Inconel® diaphragm is welded directly to the solid, stainless steel body which is machined out of a piece of 316L SS bar stock. This seals the wetted surfaces away from the atmosphere and the linkage used to actuate the gauge's pointer.

Standard (bourdon tube) gauges are made with two separate assemblies. The outer case that holds the dial and outer face is usually made from a very thin sheet of stainless steel and formed into a cylindrical cup-like shape. Its whole function is to hold and protect the dial, the window, the gauge's bourdon tube assembly and the associated linkage inside of it. The bourdon tube assembly is made of the process connection socket, welded to the bourdon tube, and welded to a tube end-piece. Those are then connected to the linkage and movement pieces that connect to the pointer. Additionally, there are usually a pair of screws that hold the housing onto the gauge's internal assembly and a couple more that fix the gauge's dial in place.

The mini diaphragm gauges are made in a manner similar to that of a UHP valve or regulator where the process connection and the case (body) are machined from one solid piece of 316L stainless steel. The Inconel® diaphragm is then welded in place, sealing the wetted surfaces away from the atmosphere, the linkage used to actuate the gauge's pointer, the face of the gauge, and its outer window. Additionally, the linkage inside the mini diaphragm gauge is not the simplistic linkage of a regular gauge. It is more like a swiss watch in its complexity.

The mini diaphragm gauges are currently only available in 1" and 1.3" dial sizes (hence the "mini" in the name) with ¼" face seal connections. As aggressive gases in gas delivery systems are typically run in ¼" inch lines, there is not a need for larger gauges for these applications, meaning a mini diaphragm gauge should suffice. Another benefit is these can also be used in surface mount applications common to the industry today. If there is a need for a gauge to be installed into a 1.125" or 1.5" surface mount application, this is a perfect fit.

Moving away from using a flexible un-passivated stainless steel internal component to a highly corrosion resistant diaphragm is the exact same technology path taken years ago when diaphragm valves overtook bellows valves for use in reactive and corrosive process gas applications and in nearly all UHP systems. It is a simple, fully-established, and well-proven solution for safer and cleaner gas delivery systems.

Having gauges follow this technology path is one that many OEMs and fabs are just beginning to move toward. This is especially true in the applications and processes where a costlier pressure transducer is not required.

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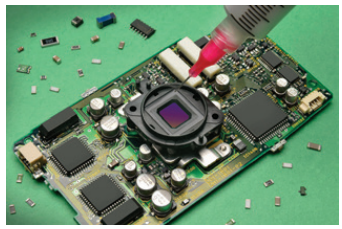

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The rebirth of the semiconductor industry

AJIT MANOCHA, *President and CEO of SEMI*

We're living in a digital world where semiconductors have been taken for granted. But, Artificial Intelligence (AI) is changing everything – and bringing semiconductors back into the deserved spotlight. AI's potential market of hundreds of zettabytes and trillions of dollars relies on new semiconductor architectures and compute platforms. Making these AI semiconductor engines will require a wildly innovative range of new materials, equipment, and design methodologies.

Moore's Law carried us the past 50-plus years and as we're now stepping into the dawn of AI's potential, we can see that the coming Cognitive Era will drive its own exponential growth curve. This is great for the world – virtually every industry will be transformed, and people's lives will get better – and it's fantastic for our industry. This truly is the very best time to be working in our industry. I'm excited to be at SEMI in this inflection period and at the center of the collaborative platforms that bring the electronics manufacturing supply chain together to Connect, Collaborate, and Innovate to realize the new Cognitive Era. I invite you to partner with SEMI in building the foundation for the Cognitive Era to increase the growth and prosperity of our industry.

The world wakes up

Our lives have become digital. An Amazon Echo wakes us up and answers questions about the weather and traffic. Google Maps tells us the best way to get to a meeting. Yelp finds the best nearby restaurant. A Tweet now even informs us of the latest change in government policy. It's a digital world that we live in – and the world already takes it for granted.

We in the industry know that the digital world only works because of the semiconductors we make and because of our integrated electronics manufacturing supply chain. We make the materials and equipment that, in turn, make the chips that become the beating hearts of the digital economy.

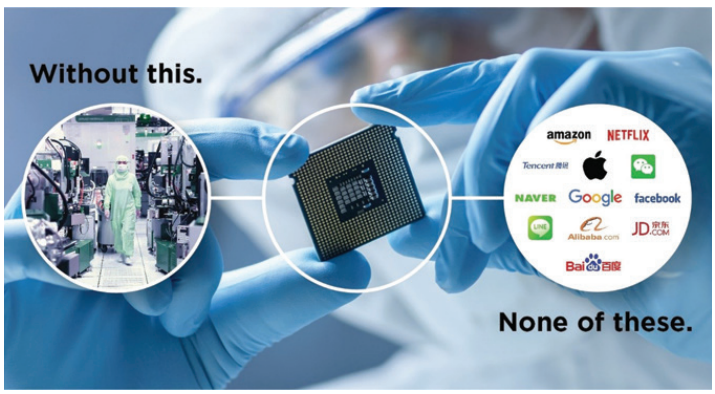

FIGURE 1

But, semiconductors have been largely invisible – hidden away under and inside a smart speaker, locked deep within a phone, buried in data centers and out of view. Meanwhile, the internet companies like Google, Amazon, Alibaba, Tencent, and Facebook stole the meaning of "Tech" and were given most of the credit for our digital world (**FIGURE 1**).

But, finally, things are changing – it's all coming back to semiconductors!

AI changing everything

Over $400B in semiconductors were sold in 2017 – those unseen chips like hearts beating away in Apple computers, in mobile phones for online shopping and social media, and in televisions showing Netflix. Now internet companies Alphabet, Alibaba, Amazon, Facebook, Microsoft and others are rushing to develop their own chips. Silicon is back in the Silicon Valley! Hardware is, once again, the place to be. Why? We are now entering the epoch of Artificial Intelligence (AI) – and semiconductors, and new compute architectures, are the key to AI. At this moment, hardware, not software, is the AI enabler to make leaps in performance and to usher in new architectures to become brain-like with neural networks.

Beyond major AI chip investments like Google's (Alphabet) $300M+ program to develop its Tensor Processing Unit (TPU) chip, there's been a surge in new chip startups and VC funding. Last year, VCs (with corporate investors) invested more than $1.5B in new AI chip startups – doubling the rate from the prior year.

After years of consolidation, there is, as some have described, a "Cambrian Explosion" of semiconductor startups with names like Cerebras, Graphcore, Wave Computing, Horizon Robotics, Cambricon Technologies, and DeePhi from the US, Europe, and China. Cambricon (China) has already become the first AI chip "Unicorn" (startup valued $1B+) with a valuation of more than $2.5B after their recent Round B financing. It's a new silicon world and a new race, as Cade Metz (The New York Times, 1/14/2018) said, "… everyone is starting from the same place: the beginning of a new market."

Winning at AI is very big business. John Kelly, SVP Cognitive Solutions and Research at IBM, in his SEMICON West keynote earlier this month, said, we're in the era of Artificial Intelligence with more than a $2T opportunity for AI decision making support on top of the $1.5T IT business in 2025. McKinsey estimates deep learning could account for between $3.5T and $5.8T in annual value.

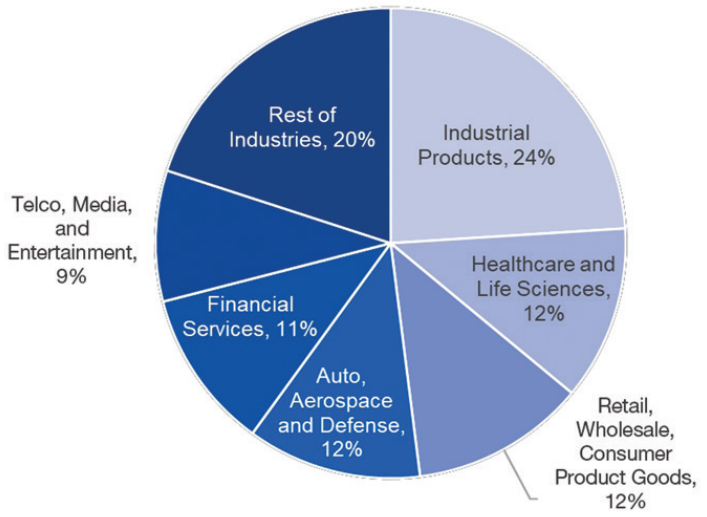

FIGURE 2

As John Kelly presented, AI will transform entire industries – not just our personal devices and lives. The $2T AI decision making support opportunity in 2025 is projected to transform the major economy industries as shown in **FIGURE 2**.

Moore's Law describes the exponential increase in the number of transistors per area that has driven growth, and has been the engine for digital innovation, through first the computer era and then the mobility era and now into the dawn of the data era (**FIGURE 3**). While the Dennard scaling approach to Moore's Law may be slowing, the data-centric era continues to drive demand and the industry continues to find new ways to pack more transistors into less volume. Chip sales are forecast to pass $0.5T in 2019 and I predict they will surpass $1T before 2030.

It turns out the Smart is not enough – we must reach "Beyond Smart."

Beyond Smart: The Cognitive Era

As we move further into the data-centric age, we see it is more than Big Data and AI, it is, instead, the dawn of a wholly new cognitive era. SEMICON West's 2018 theme was "Beyond Smart" because we are standing at the inflection from sensors triggering actions (smart) to systems that learn and make decisions (cognitive). Devices are moving "beyond smart" to being "cognitive or aware." Gary Dickerson (CEO of Applied Materials) at SEMICON West said, "… we are in the beginning of the first inning of a major inflection."

Even in the early dawn of the cognitive era, the volume of data is simply astonishing. In the last 24 months, we create more than 90% of all historic digital data. By 2025 we expect AI to generate 160 zettabytes – with 80% of that unstructured data. Moore's Law is an exponential, but as John Kelly points out, AI's deep learning is driving its own exponential with performance/watt increasing 2.5X each year (**FIGURE 4**).

AI was the focus of SEMICON West's Day 1 keynotes – and a common theme through much of the events programming. There was a common language in the keynotes by John Kelly, Gary Dickerson, and William Dally (Chief Scientist and SVP of Research NVIDIA), and others. We heard how AI is based on data, algorithms, and compute. I was inspired by these talks and for the potential for AI and the cognitive era.

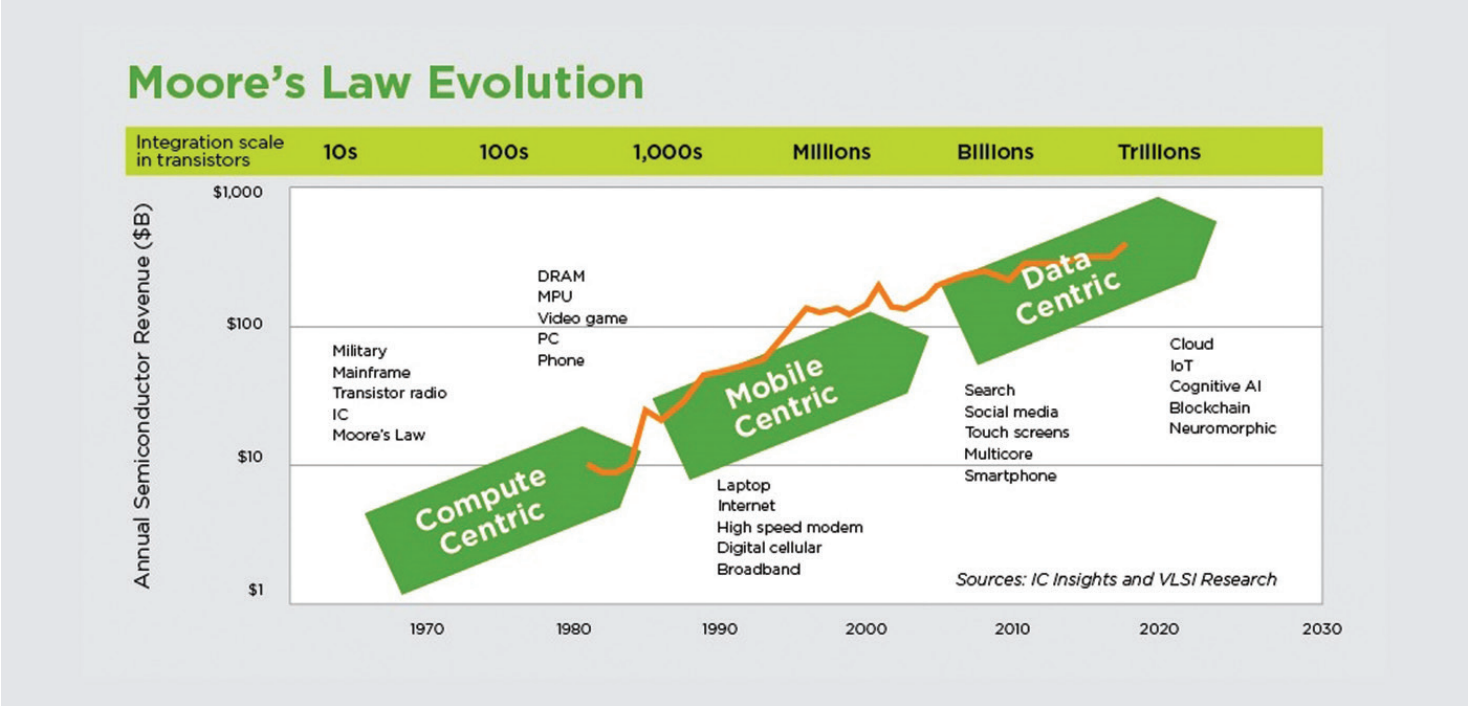

FIGURE 3

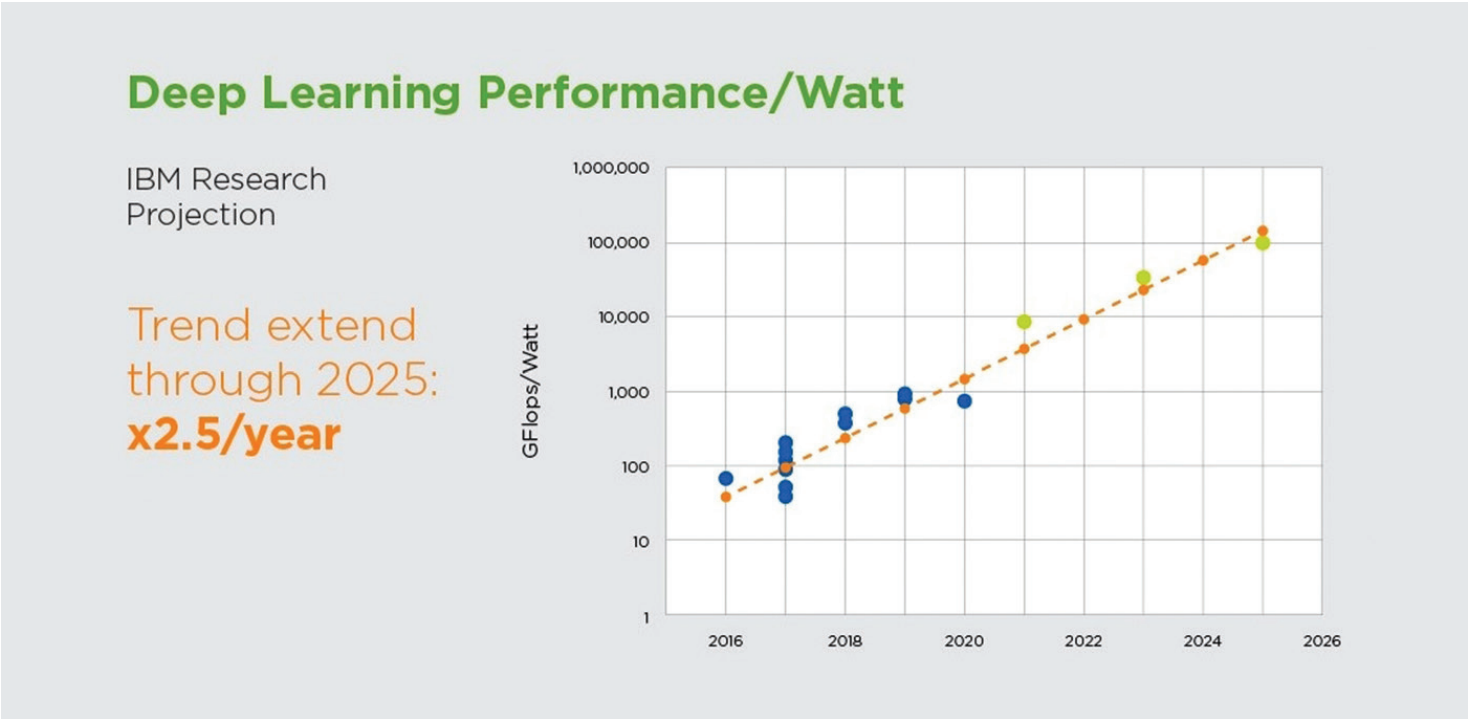

FIGURE 4

Looking ahead, I believe data + algorithms + compute + machine learning = knowledge and cognition. My vision is that this AI knowledge and cognition will be the catalyst to create new modes of systems transformations that will usher in the next Industrial Revolution. As the 4th Industrial Revolution becomes a reality, I look forward to working with others in SEMI Think Tanks to imagine the 5th Industrial Revolution – and its opportunities for our industry. I believe that it will make our lives better, healthier, more prosperous, and more fulfilled.

A sentiment shared by many speakers at SEMICON West was – this is the most exciting time to be in the semiconductor manufacturing industry. Many wished they were just now starting in the industry as this is the most interesting inflection and transformation ever. There is a flood of new architectures, new materials, new equipment, new processes – and a new system-based design approach to enable the Cognitive Era. We, in hardware manufacturing, are in the driver's seat for this incredible ride.

SEMI is working to help its members speed their time to better business results – and to take full advantage of the Cognitive Era and AI opportunity. At SEMICON West 2018, SEMI provided a broad and deep slate of program education and spotlighted AI expertise across the electronics manufacturing supply. In case you missed it, SEMI also provided

- Seven keynotes and dozens of expert panelists
- Semiconductor venture funding program – problems and solutions for the ecosystem
- SEMI Smart Workforce Pavilion with over 600 students registered to learn about the industry
- Smart Pavilions including Smart Manufacturing and Smart Automotive

SEMI highlighted the five key vertical application platforms where our industry needs to collaborate across the full supply chain and streamline the supply chain for efficiency. The five are: IoT, Smart Transportation, Smart Manufacturing, Smart MedTech, and Smart Data. These verticals drive huge business potential and are just one of the reasons that SEMICON West has become the gathering place of the extended electronics manufacturing supply chain.

With SEMI, together we can realize the potential of the coming Cognitive Era. SEMI members can advance the industry with SEMI collective action in Workforce Development, Advocacy (public policy and regulatory), Standards to synchronize the industry, and in the many SEMI technology communities and special interest groups – to increase the global industry's rate of growth and overall level of prosperity. For more information, please visit www.semi.org; to become a member, please visit http://www.semi.org/en/become-member-join-semi.◆

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