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JANUARY/FEBRUARY 2019

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Insights for Electronics Manufacturing

Executive Viewpoints: 2019 Outlook

P.10

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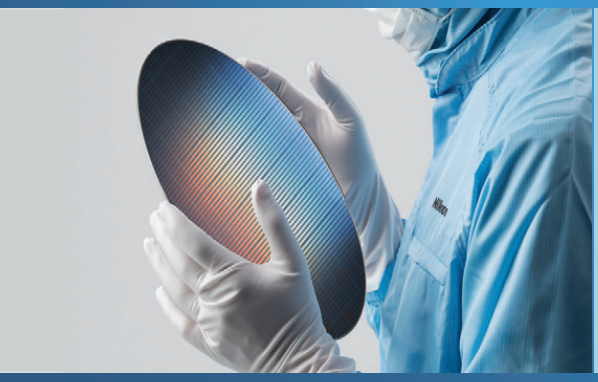

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Today's lithography systems provide overlay accuracy and throughput capabilities far beyond what was previously thought possible. However, it is real-world, on-product performance that is vital to chipmakers.

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JANUARY/FEBRUARY 2019 VOL. 62 NO. 1

Critical inflections in automotive, like EV and autonomous driving, require near-perfect quality standards to avoid serious liabilities from fab escapes that fail once the board is integrated in the car. These requirements will increase the emphasis manufacturers must place on chip reliability.

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editorial

AI needs memory

Artificial intelligence, which is extremely useful for analyzing large amounts of data (think image processing and natural language recognition), is already impacting every aspect of our lives. Products being made today are being redesigned to accommodate some form of intelligence that it can adapt to the preferences of the user. Smart speakers integrating Alexa or Siri are perhaps the best examples in the home and office, but there's huge value in AI for businesses. "AI is so fundamental to improving what we expect of devices and their ability to interpret our needs and even predict our needs, that's something that we're going to see more and more of in the consumer space. And then of course in the industrial environments as well," notes Colm Lysaght, vice president of corporate strategy at Micron Technology. "Many different industries are working and using machines and algorithms to learn and adapt and do things that were not possible before."

There are various ways to crunch this data. CPUs work very well for structed floating point data, while GPUs work well for AI applications – but that doesn't mean people aren't using traditional CPUs for AI. In fact, AI is being implemented today with a mix of CPUs, GPUs, ASICs and FPGAs. Data crunching also needs a lot of memory and storage.

A new report by Forrester Consulting, commissioned by Micron, takes a look at how companies are implementing AI and the hardware they are using, with a special focus on memory and storage.

Forrester conducted an online survey and three additional interviews with 200 IT and business professionals that manage architecture, systems, or strategy for complex data at large enterprises in the US and China to further explore this topic. Here are their key findings:

- AI/ML will continue to exist in public and private clouds. Early modeling and training on public data is occurring in public clouds, while production at scale and/or on proprietary data will often be in a private cloud or hybrid cloud to control security and costs.
- Memory and storage are the most common challenge in building AI/ML training hardware. While the CPU/GPU/custom compute discussion received great attention, memory and storage are turning out to be the most common challenge in real world deployments and will be the next frontier in AI/ML hardware and software innovation.
- Memory and storage are critical to AI development. Whether focusing on GPU or CPU, storage and memory are critical in today's training environments and tomorrow's inference.

"AI is having a very large impact on society and it is fundamentally rooted in our technology. Many different applications, all of which are interpreting data in real time, need fast storage and they need memory," Lysaght said. "At Micron, we're transforming the way the world uses information to enrich our lives."

To get to the next level in performance/Watt, innovations being researched at the AI chip level include: low precision computing, analog computing and resistive computing. This will require some new innovation in design, manufacturing and test. That's the focus of The ConFab, to be held May 14-17 at The Cosmopolitan of Las Vegas (see www.theconfab.com for more information).

—Pete Singer, Editor-in-Chief

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Web Exclusives

2018 IEDM

On December 1– 5, 2018, the good and the great of the electron device world made their usual pilgrimage to San Francisco for the 2018 IEEE International Electron Devices Meeting.

https://bit.ly/2sQ2mGo

A year of transformation and execution

Last year the industry posted another remarkable double-digit revenue growth year. IC shipments eclipsed one trillion units for the first time and continued to enable an ever-expanding array of silicon intensive-applications.

https://bit.ly/2DrJnbo

How to add machine intelligence or AI to EDA tools

Constant coverage of an invigorating topic like machine intelligence in the media often urges us to consider its use in EDA technology. As is often the case, there are many myths and falsehoods that consume our time and effort when trying to apply machine intelligence to EDA. This article aims to uncover the myths and to provide helpful advice on applying machine intelligence to your EDA project or product.

https://bit.ly/2CNS26s

Agile manufacturing of glass carriers for advanced packaging

SEMI met with Jay Zhang, business development director at Corning Incorporated, to discuss recent innovations at Corning that allow fine granularity CTE engineering as well as high Young's modulus.

https://bit.ly/2Uis4PL

n&b news and blogs

The packaging of Apple's A12X is... weird

Watching the video from the new iPad Pro launch back on October 30, there was a pseudo assembly sequence within it. Being the teardown nerd that I am, I kept running through it until I got a set of screen shots that showed the motherboard being populated.

https://bit.ly/2TgQrgs

Getting to low power in IoT/IIoT devices

Over the last three years the number of battery-operated electronic-component solutions for the Internet of Things (IoT) and Industrial IoT (IIoT) applications has been increasing steadily. This trend will continue for years to come, particularly with the growing popularity of mobile devices of all flavors.

https://bit.ly/2sMvApK

Semiconductor unit shipments exceeded 1 trillion devices in 2018

Annual semiconductor unit shipments, including integrated circuits and optoelectronics, sensors, and discrete (O-S-D) devices grew 10% in 2018 and surpassed the one trillion unit mark for the first time, based on data presented in the new, 2019 edition of IC Insights' McClean Report.

https://bit.ly/2Clpz20

Flash memory remains primary target for capex spending

The semiconductor industry is expected to allocate the largest portion of its capex spending for flash memory again in 2019, marking the third consecutive year that flash has led all other segments in spending.

https://bit.ly/2HH1RbY

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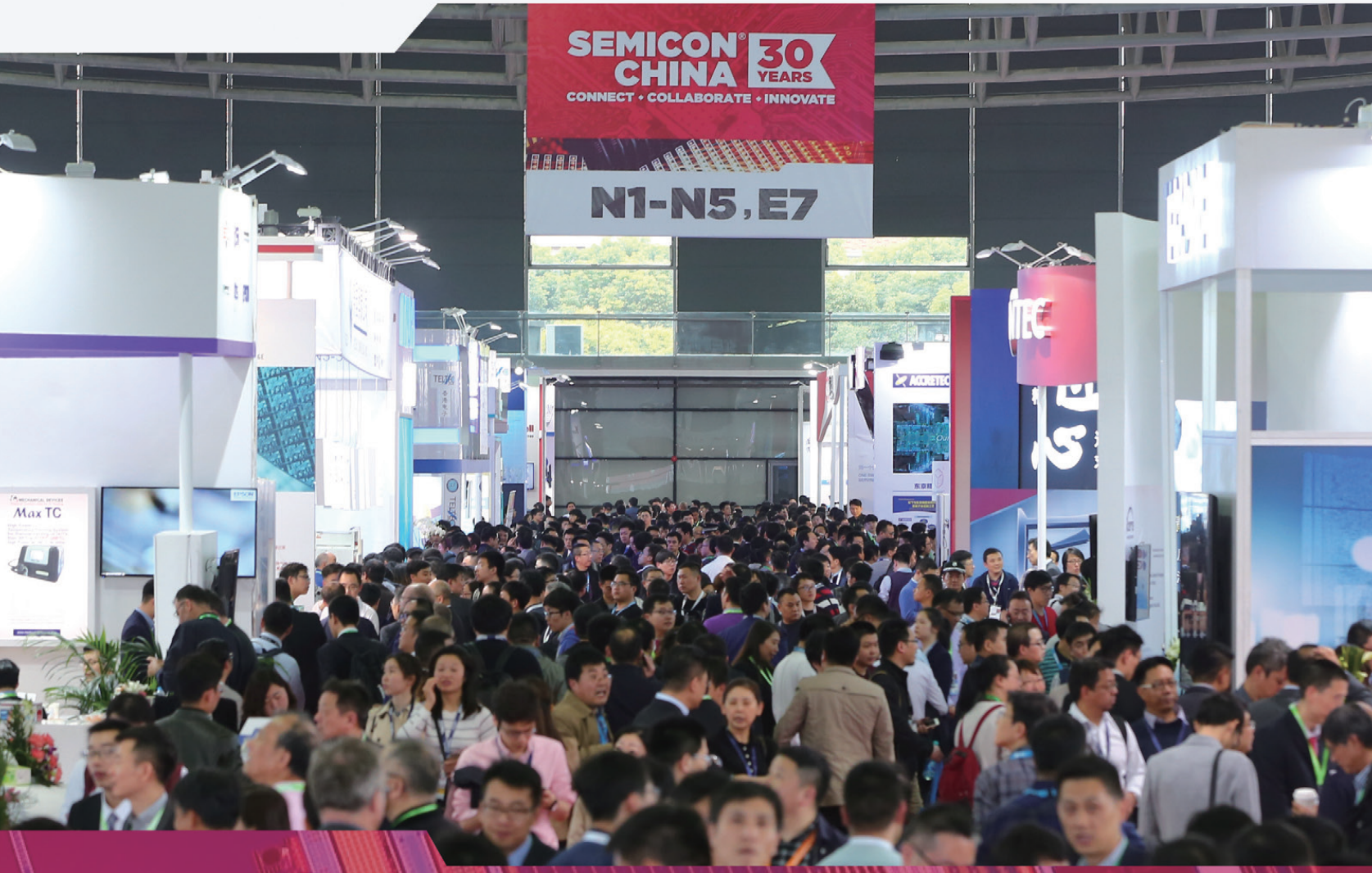

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worldnews

EUROPE - **LPKF Laser & Electronics** added a foundry service for thin glass substrates to its product portfolio.

USA - **ULVAC** introduced a high performance, low cost, compact LS series of dry screw pumps.

EUROPE - Researchers at the **University of Exeter** have developed an innovative technique that could help create the next generation of everyday flexible electronics.

ASIA - **GIGAPHOTON** announced seven major semiconductor chipmakers implemented FABSCAPE data products.

USA - **Corning Precision Glass Solutions** introduced advanced packaging carriers optimized for fan-out processes.

EUROPE - **ZEISS** unveiled a new suite of high-resolution 3D X-ray imaging solutions for failure analysis (FA) of advanced semiconductor packages, including 2.5/3D and fan-out wafer-level packages.

ASIA - **MagnaChip Semiconductor Corporation** announced it now offers foundry customers its third generation 0.18 micron Bipolar-CMOS-DMOS (BCD) process technology.

USA - **IBM** expanded its strategic partnership with **Samsung** to include 7nm chip manufacturing.

EUROPE - Researchers from **Chalmers University of Technology**, Sweden, have discovered a simple new tweak that could double the efficiency of organic electronics. OLED-displays, plastic-based solar cells and bioelectronics are just some of the technologies that could benefit from their new discovery, which deals with "double-doped" polymers.

USA – **HEIDENHAIN** opened a new office in Fremont, CA.

VIS to acquire GLOBALFOUNDRIES' Fab 3E in Singapore

Vanguard International Semiconductor Corporation (VIS) and GLOBALFOUNDRIES (GF) announced that VIS will acquire GF's Fab 3E in Tampines, Singapore. The transaction includes buildings, facilities, and equipment, as well as IP associated with GF's MEMS business. GF will continue to operate the facility through the end of 2019, providing a transition period to facilitate technology transfers for VIS and existing GF customers. Fab 3E currently manages a monthly capacity of approximately 35,000 8-inch wafers. The transaction amounts to $236 million USD and the transfer of ownership is set to be completed on December 31st, 2019.

VIS and GF have already reached consensus on the transfer of Fab 3E's employees and customers. Both companies believe that employees are the most important assets of a company, so their interests should be put as the first priority during the transition; while ensuring no disruption to customers whose products are in production at the fab. Under this premise, VIS will extend employment offers to all employees currently working at Fab 3E, as well as continuously provide existing customers at Fab 3E with its foundry service, including MEMS customers.

"I appreciate the support of GF's board and management team for this transaction, giving VIS an opportunity to continue expanding its capacity and reinforce momentum for future growth," said Mr. Leuh Fang, Chairman of VIS. "Since its foundation, VIS has already had three separate experiences of successfully transforming a DRAM fab into a foundry fab. We believe this transaction is a win-win for both VIS and GF; and to VIS, it is also a decision that benefits all of our customers, employees, and shareholders. VIS will uphold its philosophy and principles to continue satisfying customers' demands in capacity and technology, sustaining profitability and growth, and rewarding our shareholders."

"This transaction is part of our strategy to streamline our global manufacturing footprint and increase our focus in Singapore on technologies where we have clear differentiation such as RF, embedded memory and advanced analog features," said GF CEO Tom Caulfield. "Consolidating our 200mm operations in Singapore into one campus will also help reduce our operating costs by leveraging the scale of our gigafab facility in Woodlands. VIS is the right partner to leverage the Fab 3E asset going forward."

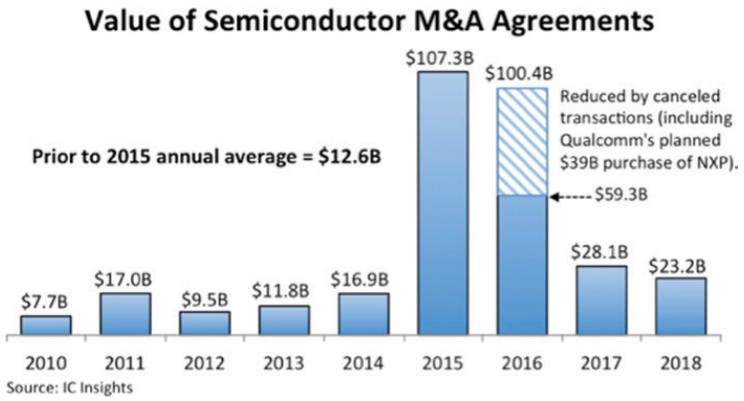
VIS's capacity has been fully utilized since 2018, and it is in the interests of its customers that VIS expands capacity to meet growing demands. The new fab is expected to contribute more than 400,000 8-inch wafers per year. This acquisition demonstrates the determination and commitment of VIS to accelerate capacity expansion.

Value of semiconductor mergers and acquisitions falls considerably

IC Insights is in the process of completing its forecast and analysis of the IC industry and will present its new findings in The McClean Report 2019, which will be published later this month. Among the semiconductor industry data included in the new 400+ page report is an analysis of semiconductor merger and acquisition agreements.

The historic flood of merger and acquisition agreements that swept through the semiconductor industry in 2015 and 2016 slowed significantly in 2017 and then eased back further in 2018, but the total value of M&A deals reached in the last year was still nearly more than twice the annual average during the first half of this decade. Acquisition agreements reached in 2018 for semiconductor companies, business units, product lines, and related assets had a combined value of $23.2 billion compared to $28.1 billion in 2017, based on data compiled by IC Insights. The values of M&A deals struck in these years were significantly less than the record-high $107.3 billion set in 2015 (**Figure 1**).

The original 2016 M&A total of $100.4 billion was lowered by $41.1 billion to $59.3 billion because several major acquisition agreements were not completed, including the largest proposed deal ever in semiconductor history—Qualcomm's planned purchase of NXP Semiconductor for $39 billion, which was raised to $44 billion before being canceled in July 2018. Prior to the explosion of semiconductor acquisitions that erupted four years ago, M&A agreements in the chip industry had a total annual average value of $12.6 billion in the 2010-2014 timeperiod.



Continued on pg 8

Value of semiconductor, *Continued from pg 7*

The two largest acquisition agreements in 2018 accounted for about 65% of the M&A total in the year. In March 2018, fabless mixed-signal IC and power discrete semiconductor supplier Microsemi agreed to be acquired by Microchip Technology for $8.35 billion in cash. Microchip said the purchase of Microsemi would boost its position in computing, communications, and wireless systems applications. The transaction was completed in May 2018. Fabless mixed-signal IC supplier Integrated Device Technology (IDT) agreed in September 2018 to be purchased by Renesas Electronics for $6.7 billion in cash. Renesas believes the IDT acquisition will strengthen its position in automotive ICs for advanced driver-assistance systems and autonomous vehicles. The IDT purchase is expected to be completed by June 2019.

Just two other semiconductor acquisition announcements in 2018 had values of more than $1 billion. In October 2018, memory maker Micron Technology said it would exercise an option to acquire full ownership of its IM Flash Technology joint venture from Intel for about $1.5 billion in cash. Micron has started the process of buying Intel's non-controlling interest in the non-volatile memory manufacturing and development joint venture, located in Lehi, Utah. The transaction is expected to be completed in 2H19. In September 2018, China's largest contract manufacturer of smartphones, Wingtech Technology, began acquiring shares of Nexperia, a Dutch-based supplier of standard logic and discrete semiconductors that was spun out of NXP in 2017 with the financial backing of Chinese investors. Wingtech launched two rounds of share purchases from the Chinese owners of Nexperia with a combined value of nearly $3.8 billion. The company hopes to take majority ownership of Nexperia (about 76% of the shares) in 2019. ◆

Soitec expands collaboration with Samsung Foundry on FD-SOI wafer supply

Soitec, a designer and manufacturer of semiconductor materials, announced an expanded collaboration with Samsung Foundry to ensure the volume supply of fully depleted silicon-on-insulator (FD-SOI) wafers. This agreement extends the current partnership and provides a solid foundation for both companies to strengthen the FD-SOI supply chain and guarantee high-volume manufacturing for customers.

With the leadership from the two companies, today FD-SOI is one of the standard technologies for cost-effective, low-power devices used in high-volume consumer, 4G/5G smartphones, IoT, and automotive applications. The agreement is built on the existing close relationship between the companies and guarantees wafer supply for Samsung's FD-SOI platform starting with 28FDS process.

"This strategic agreement validates today's high-volume manufacturing adoption of FD-SOI," said Christophe Maleville, Soitec's Executive Vice President, Digital Electronics Business Unit. "Soitec is ready to support Samsung's current and long-term growth for ultra-low power, performance-on-demand FD-SOI solutions."

FD-SOI relies on a very unique substrate whose layer thickness is controlled at the atomic scale. FD-SOI offers remarkable transistor performance in terms of power, performance, area and cost tradeoffs (PPAC), making it possible to cover low-power to high-performance digital applications with a single technology platform. FD-SOI delivers numerous unique advantages including the ability to mitigate process, temperature, voltage and aging variations through body bias, near-threshold supply capability, ultra-low sensitivity to radiation, and very high intrinsic transistor speed, making it most likely the fastest RF-CMOS technology on the market.

"Samsung has been committed to delivering transformative industry leading technologies. FD-SOI is currently setting a new standard in many high-growth applications including IoT with ultra-low-power devices, automotive systems such as vision processors for ADAS and infotainment, and mobile connectivity from 5G smartphones to wearable electronics," said Ryan Lee, Vice President of Foundry Marketing at Samsung Electronics. "Through this agreement with Soitec, our long-term strategic partner, we hope to lay the foundation for steady supply to meet high-volume demands of current and future customers." ◆

China wafer production capacity growth fastest in the world

Unwavering in its drive to build a strong, self-sufficient semiconductor supply chain, China plans more new fab projects than any other region in the world from 2017 to 2020, and its expansion of fab capacity recently picked up pace on the strength of new foundry and memory projects from both domestic and foreign companies, according to SEMI's 2018 China Semiconductor Silicon Wafer Outlook report. China's installed fab capacity is forecast to grow at a 12 percent CAGR from 2.3 million wafers per month (wpm) in 2015 to 4 million wpm in 2020, faster than all other regions.

Well known for its semiconductor packaging prowess, China in recent years shifted its focus to front-end semiconductor fabs and a few key material markets. In 2018, the region's surge in fab investment thrust it past Taiwan as the second largest capital equipment market in the world, behind only Korea.

However, China's semiconductor manufacturing growth faces strong headwinds. Chief among them is the tight supply of silicon wafers over the past two years due in large part to the sector oligopoly's firm control of global production, with the top five wafer manufacturers accounting for over 90 percent of market revenue. In response, China's central and local governments has made the development of its domestic silicon wafer supply chain a key initiative, funding multiple silicon wafer manufacturing projects.

According to the 2018 China Semiconductor Silicon Wafer Outlook report, many of China's domestic silicon suppliers capably provide wafers 150mm in size and smaller. And the while the region lags peers in 200m and 300mm processing technology and capacity, strong domestic demand and favorable policies have fueled progress in 200mm and 300mm silicon manufacturing with some Chinese suppliers having reached key large-diameter manufacturing milestones.

However, it will take these new suppliers several years before they can meet capacity and yield requirements of the larger-diameter silicon wafer market. Company plans and announcements indicate that by the end of 2020, total silicon supply capacity in China will reach 1.3 million wpm for 200mm, possibly leading to a slight oversupply, and 750,000 wpm for 300mm.

China's equipment suppliers, particularly crystal furnace vendors, are also investing in the development of 300mm wafer manufacturing, and domestic tool suppliers have developed most of the necessary tools for wafer manufacturing, except for inspection.

While China's silicon wafer suppliers continue to lag international peers in manufacturing capabilities, the region's silicon manufacturing ecosystem is maturing and becoming better integrated. The sector's growth is driven and accelerated by significant domestic market demand and favorable policies. ◆

Executive viewpoints: 2019 outlook

Each year, Solid State Technology turns to industry leaders to hear viewpoints on the technological and economic outlook for the upcoming year. Read through these expert opinions on what to expect in 2019.

Technology Trends and Innovations in 2019

By Sundeep Bajikar, Head of Corporate Strategy at Applied Materials

Big Data and Artificial Intelligence (AI) are fueling a new computing revolution, which is transforming many industries from transportation to healthcare. In 2019, the pace of this change will accelerate, creating new challenges and also tremendous opportunities for innovation.

Virtually all electronic devices are becoming smarter and more connected. This is causing an explosion of machine-generated data that now exceeds data generated from humans. The challenge is how to capture, store and process the very large data sets at virtually real-time speed. This will take a lot of storage, along with new types of memory and order of magnitude improvements in computing performance per watt.

But just as momentum is building to drive the AI revolution, classic Moore's Law scaling is slowing. While 2D shrinking previously delivered the required improvements in PPAC (performance, power and area/cost) for the PC era, the industry now needs new methods of driving chip improvements beyond Moore's Law. This will involve a combination of approaches: new chip architectures, 3D design techniques, novel materials, new ways to continue shrinking transistors, and advanced packaging schemes to connect chips together in new ways. We call this the "New Playbook" for semiconductor design and manufacturing. Enabling this new playbook will require major advances in materials engineering and greater collaboration across the industry ecosystem.

One of the biggest challenges for the semiconductor industry is how to enable faster processing speeds without raising the power envelope. Today there's a 1,000X gap in compute performance per watt that must be closed. Lowering power consumption will involve design changes at the chip- and system-level and innovations in materials and structures within the device. This is one of the critical hurdles that must be solved to unlock the potential of AI and Big Data.

New materials and architectures being developed focus on delivering PPAC solutions for the industry. For example, replacing copper with cobalt as a new material in the lower level wiring layers of a device reduces resistance and improves the RC delay problem, which results in higher speed and lower power consumption. A move to horizontal gate-all-around devices reduces transistor leakage providing further improvements in power and performance. Packaging is another key enabling area which provides systems solutions that bring logic and memory together for higher performance and lower power while also addressing form-factor requirements. Stacking DRAM chips together has brought about High Bandwidth Memory (HBM) which combined with logic in interposer designs has delivered major performance gains for AI computing.

With regard to materials, the days of working with individual materials from the periodic table are over. Continued advances in PPAC require new combinations of materials that work together to form novel structures with precise electrical properties. Assembling these new material combinations to achieve predictable properties and interactions is an increasingly complex task requiring Integrated Materials Solutions that can co-optimize multiple process steps, often within the same platform and under vacuum. More and more, engineering materials in vacuum permits precise engineering at the atomic-level.

Applied is expanding its capabilities to help enable the new semiconductor industry playbook. To collaborate with more customers on projects that can speed availability of new materials and process technologies, Applied announced plans for the new Materials Engineering

Technology Accelerator (META Center) in November of last year. The META Center will complement and extend the capabilities of Applied's Maydan Technology Center in Silicon Valley. Applied is also enabling advanced packaging capabilities with a full suite of 300mm advanced wafer level packaging equipment and personnel in Singapore. Our venture capital arm, Applied Ventures, is investing in AI chip startups with disruptive innovations in computing architecture. Last year Applied launched the AI Design Forum at SEMICON West to bring together design and manufacturing experts—from materials to systems—under one umbrella to collaborate at a higher level.

2019 is a pivotal year for semiconductors, where major collaborative efforts and innovations in manufacturing technologies will impact a wide range of industries. By providing breakthroughs in materials engineering, Applied is at the forefront of enabling the technologies shaping the future.

As roadmaps diverge, so does materials strategy development

George Barclay, Ph.D., Global Litho Technologies Business Director, DuPont Electronics & Imaging

At DuPont, we watch the semiconductor industry roadmap carefully and talk frequently with our customers about where they are going, so that we can align our product development strategically to best serve market needs. As we move into 2019, leading foundries and integrated device manufacturers have reached a fork in the road: one path leading to More Moore, and the other prioritizing More than Moore technologies.

As they've stated publicly, a handful of the industry giants are continuing to pursue advanced nodes, pushing logic beyond 7nm nodes to 3nm and memory to denser architectures. These efforts slowed as the world waited for the commercialization of EUV lithography, but in 2019, the time has finally come for EUV, and with it, renewed efforts to continue scaling.

Other companies have announced that they are strategically investing in optimizing legacy node technologies. These technologies are experiencing a renaissance, thanks to the growing automotive electronics, internet of things (IoT), and medical device markets. These require specialized devices that integrate various sensors, MEMS, RF, and discrete components.

This bifurcation of the market provides opportunities for materials suppliers with product portfolios that extend from 128nm down to 7nm and beyond.

Supporting advanced nodes

Supporting advanced node technologies means meeting the challenges that come with EUV lithography. This is complex as the pattern lines are becoming tiny, and EUV produces fewer photons than 193nm immersion lithography. These challenges require innovation in photoresists and underlayers. Photoresists must be made more sensitive to light, including the use underlayers that improve sensitization. They also must be designed to avoid pattern collapse by improving adhesion using these underlayers.

Supporting legacy nodes

As only a few companies will be using EUV lithography, supporting materials for other wavelengths, from 193 – 365 nm, is equally important. Here, the focus of development is not on printing smaller feature sizes, but on improving reliability and quality to meet the zero-defect requirements of automotive and other specialty electronics.

Therefore, DuPont's strategy for our lithography portfolio in 2019 is to support both paths: we will continue push the development of our advanced node photoresist, underlayer, and anti-reflective coating products; and to support legacy nodes, we will focus on improving the quality of our lithography products so they, in turn, improve the reliability of specialty devices.

The future looks bright for materials technology

Kim Arnold, Executive Director, Advanced Packaging Business Unit, Brewer Science Inc.

More than ever, in 2019, manufacturers of advanced power and memory ICs, driven by the continued growth in mobile, Industry 4.0 and data storage applications, will be looking for advances in high-quality materials to achieve their design goals. They are actively seeking materials that not only help create very small features with fewer defects, but also withstand ultrahigh temperatures.

One new development that these manufacturers are exploring is dual-layer temporary bonding technology, which addresses high-temperature and high-stress semiconductor applications. This technology, comprising two different materials—a thermoplastic bonding layer and a curable layer—can accommodate a range of advanced applications, including 3D-IC, power, MEMS, chip-first fan-out wafer-level packaging (FOWLP) and III-V materials, which are used widely in compound semiconductor fabrication. Because several different debonding techniques can be used, this material technology is highly flexible.

Another growing trend is the demand for sustainable materials. Environmental concerns are spurring manufacturers to work with environmentally oriented companies. And making materials more eco-friendly actually improves their quality, allowing materials providers to better address multiple customer requirements. Companies that can illustrate their commitment via proven quality and safety policies and compliance with environmental programs such as GreenCircle will be well positioned to establish or extend leadership in the materials space.

We also see a strong focus on optimizing cost of ownership for existing lithography equipment through materials innovation. This is where directed self-assembly (DSA) is beginning to enter the picture. While the industry is close to commercializing extreme ultraviolet (EUV) lithography, tool cost will limit its use. DSA is an alternative to existing processes, and it can be performed on existing, installed fab tool sets. DSA also complements EUV, for those who can afford it. As a result, we anticipate a steadily ramping demand for DSA materials for the foreseeable future.

Semiconductor device complexity requires tight integrated chemical process control

Marianna Rabinovitch, CEO, ECI Technology

We have seen the semiconductor industry grow rapidly over the last two years and, while the growth forecast softens, we do not expect the demand slowdown to be deep or long lived. The fundamentals of the industry are strong and there are important new applications and technologies on the horizon that will expand the electronics market and drive continuous growth beyond mobile phones. Semiconductor demand, which is driven by innovative applications, such as artificial intelligence and machine learning, 5G networks, VR/AR, IoT and the rapidly expanding use of electronics by the automotive industry, will continue to accelerate. Important semiconductor technology trends expected to continue include the ongoing effort to shrink feature sizes in leading-edge logic devices at the 7nm and 5nm nodes, the expansion of 3D NAND memory capacity with significant increase in number of layers, and the migration of frontend manufacturing processes to backend applications in advanced packaging.

ECI Technology provides high precision control of wet chemical manufacturing processes, including MEOL and BEOL metal plating and deposition used for contacts and interconnects and surface preparation, etching and cleaning steps. ECI systems are also widely used in advanced packaging manufacturing steps including bumping, TSV, fan-out, and wafer and panel-level packaging applications.

For 3D NAND memory we have developed a patented technology to control silicon nitride etch, which is critical for enabling the challenging selectivity for complex, multi-layered structures.

The most significant challenge for our customers is the growing complexity of advanced technology processes and the need for precise control of materials to ensure high yield combined with cost-efficient operation. We are well beyond the point where adequate control can be provided by single or common analytical techniques.

We have focused our efforts on developing customized metrology that integrates multiple analytical methods tailored for the advanced manufacturing technologies of the top-tier foundries and IDMs.

As the leading semiconductor manufacturers are progressing towards high-volume manufacturing of their latest technologies, they need to increase the control requirements throughout their supply chain, including equipment manufacturers and materials providers.

We are working closely with the industry to anticipate the requirements roadmap and to assure production-worthy metrology throughout the entire wafer manufacturing process, from incoming materials inspection and point-of-use analyses to fully-automated chemical process control.

Market volatility and process complexity will reward technical and operational agility

Paul Rawlings, President, Semiconductor Division, Edwards

There is clearly some uncertainty in the market right now, due to multiple factors, including some rebalancing of supply and demand, the negative effects of trade tensions and continuing concerns about protection of valuable intellectual property. There are also issues with achieving adequate yields from some leading-edge processes. The net result is likely to be significant market volatility for equipment suppliers in 2019. At Edwards, we are preparing for this by focusing on agility throughout our supply chain. Agility in not only being able to slow down in response to decreases in demand, but also being able to gear up quickly when demand increases.

One message we are receiving from our customers is a call for smaller footprints for sub-fab equipment, a result of the increasing complexity of leading-edge processes and the consequent requirement for more and more supporting equipment in the sub-fab. At the same time, there is significant pressure to improve reliability as the increasing number of systems raises the number of possible failure points and the high cost of a fab makes any downtime costlier. One way to address this is intelligent subfab connection to use the available space more efficiently and to integrate information from the connected systems to improve their overall reliability and availability.

Another major trend is the development of increasingly stringent emissions limits, and their extension beyond the usual targets, such as PFCs, to a wider variety of gases, including process byproducts like NOX and CO. At the same time, we are being asked for vacuum pumps that can handle a wider range of materials and conditions. The days when one type of pump or abatement system could do everything are long gone and manufacturers need specialized equipment that is set up and optimized specifically for particular processes.

Looking at all these issues, one thing that becomes clear is the need to work together with our customers, materials suppliers and other equipment suppliers to find solutions that are both effective and timely. This will be true not only for technical issues, but also for business issues, like market volatility that will require us to maximize the agility of our internal operations, our setup and configuration procedures, and our entire supply chain so that we can respond quickly to market needs as they arise.

Fusion bonding an enabling technology for "More Moore" scaling

Paul Lindner, Executive Technology Director, EV Group

While the major application drivers for the semiconductor industry may have changed over time – from PCs and cell phones to big data and cloud computing – the constant need for improved device performance at a lower cost while consuming less power remains the same. According to the International Roadmap for Devices and Systems (IRDS), parasitic scaling will become a dominant driver of logic device performance in the coming years, requiring new transistor architectures, such as gate all around (GAA) transistors, as well as engineered substrates and new high-mobility channel, interconnect and barrier materials.

The IRDS Roadmap also notes that new 3D integration approaches such as monolithic 3D (M3D) will be necessary to support the long-term transition from 2D geometry scaling to 3D very large-scale integration (VLSI), including backside power distribution, N and P device stacking or logic-on-memory. 3D VLSI is expected

to bring power, performance, area and cost (PPAC) gains for future nodes as well as pave the way for heterogeneous integration. Sequential integration through thin-silicon layer transfer processes will play an essential role in enabling the transition from 2D to 3D VLSI.

The good news is that process solutions for 3D System-on-Chip (3D SoC) applications are making significant progress and appear to be in alignment with the pace of the IRDS Roadmap. For example, fusion and hybrid wafer bonding is already a mature solution for certain 3D SoC applications, such as stacked image sensors, and is progressing at a pace of development coinciding with the development progress of memory and logic stacking.

Further integration density is restricted by metal wiring, which adds cost and restricts power gains – particularly at the first wiring levels. Wafer bonding approaches, such as hybrid bonding closer to the first wiring levels, could provide significant cost savings. Using wafer bonding in front-end-of-line processing to enable backside power distribution can also provide significant gains in area and power.

Solid market fundamentals support a strong outlook with major opportunities building toward 2020

Tim Kryman, V.P. Marketing, Rudolph Technologies, Inc.

The industry has been in a "super-cycle" for the last several years, driven by demand from IoT, automotive, mobile devices and memory for data centers, both NAND and DRAM. Capital expenditures over that period have exceeded most expectations, all tied to dramatic increases in the amount of data being created, stored and manipulated. Even as memory for data centers and handsets has begun to cool, a decrease in ASPs has resulted in increased memory content in other consumer and industrial segments. Now, AI and "deep learning" are adding to that demand in their effort to create a "smart world." The net result is a growing and sustained demand for more silicon. Right now, the market is in a soft patch that may linger for another six months, but market fundamentals are strong. The current softness is due, at least in part, to ongoing geo-political uncertainties that are difficult to predict, but we do not expect it to result in a traditional semiconductor industry downturn.

Historically, growth in our industry has been driven by technology inflections points. The next inflection point will likely be 5G networks. Starting in 2019 and ramping hard in 2020, 5G will unquestionably drive the development and adoption of myriad new technologies. Another trend that will impact the industry, especially our segment, is the explosive growth of electronics in automotive applications and that industry's drive to attain zero failure rates. Closely related is an expanded emphasis across all applications on improving reliability versus the traditional focus on yield. Typical yields have been quite good, but the focus has now shifted to reliability which leads to downstream device failures. Addressing these challenges will require innovative techniques that look for non-conventional defects and dramatically increased levels of inspection and process control.

Our customers are being asked to innovate at an unprecedented pace as they try to satisfy consumer demand for new technologies while also implementing the new manufacturing and packaging processes that advanced devices require. For Rudolph, and our customers, this represents a significant opportunity to drive new technology adoption. On the hardware front, larger, heterogeneous packages will require large field lithography with requirements that are quite different from front-end lithography. Inspection and metrology systems will have to deal with thinner films, smaller features and smaller defects-of-interest. Our software efforts are centered on smart manufacturing and supply chain management, driven by sophisticated approaches to data management and analysis. As one of few companies with experience and expertise spanning processes from bare wafers to final packaging and testing, we believe we are uniquely positioned to help our customers capitalize on these opportunities for innovation.

Advanced packaging lithography trends

Peter Porshnev, SVP & GM – Ultratech Business Unit, Veeco Instruments

Increased mobility, IoT, AI and deep learning are enjoying solid growth in step with global megatrends. However, the industry should not underestimate the technical challenges to be surmounted in order to fully realize its potential, enabled in no small measure by technologies like 3D integration

and advanced packaging (AP). We are seeing increasing AP lithography adoption and innovation worldwide as customers demand higher performance and added functionality within ever-smaller form factors to meet end consumers' needs.

2019 outlook

Analysts forecast mobile device growth—typically a major AP driver—to decelerate in 2019. However, overall wafer-level packaging (WLP) content will continue to grow due to increasing performance requirements coupled with ever-growing memory-CPU integration. Examples include the server/cloud industry where big data applications require more processing power and higher bandwidth memory as the industry moves towards the 5G platform, driving silicon interposer and fanout on substrate solutions. This is on top of the traditional flip chip market, which continues to show growth. High-end memories are no exception. Adoption of stacked DRAM with TSVs began in 2015 for HBM/DIMM; now mobile DRAM is converting to flip-chip packaging. All of the above will demand higher fan-out WLP (FOWLP) adoption, with increasing innovation in more advanced system in package (SiP), fanout on substrate and 2.5D chip on wafer packages.

Submicron challenges

In terms of high-density fanout, redistribution layers (RDL) with smaller critical dimensions (CD) below 1 micron enable reduction of the total number of redistribution process levels. This in turn reduces the total packaging cost and improves yield for customers. Most AP lithography systems are designed for minimum features of 2-micron or higher. Moving to smaller features requires exposing with a shorter wavelength (i-line of Hg) and having a larger lens numerical aperture (NA). The current lithography systems from Veeco, such as the AP200/300 steppers, already have these features. The major lithography challenges going forward for advanced fan-out packages include:

- Imaging submicron RDL with high aspect ratios
- Minimizing overlay errors that occur from die shifting
- Ability to handle extremely warped substrates
- Support for very large 2.5D chip on wafer package sizes

The technology team at Veeco works closely with customers to develop semiconductor manufacturing and process innovations that meet changing industry demands. The AP300 lithography tool for advanced packaging applications has a variable NA lens that can be optimized to maximize depth of focus while maintaining the higher resolution performance. Additionally, the AP300 stepper can be configured with an optical focus system that provides a full wafer topography map for optimizing the focus position for each exposure. These features, coupled with the capability for processing wafers with up to 7mm of warpage, provide a mature lithography solution for the challenging FOWLP processes required to manufacture high performance next-generation devices.

Longer term

Currently 1-micron RDL is in low volume, but we expect that it will increase significantly over the next few years. Initially, only high ASP devices will be able to afford this level of AP innovation. In the end, yield, cost and productivity will drive the adoption of advanced fan-out packages.

Another trend is continued consolidation in the industry as device manufacturers continue to push OSATs for more technical advances or choose to develop their own proprietary AP schemes. OSATs will need greater flexibility and will continue to push suppliers to offer more modular solutions to stay competitive.

Finally, OSATs and foundries will need to rely on more proven, global suppliers with design and full process support capabilities to partner with them as they look to build a competitive supply of advanced packaging.

2019: It's all about the data

Oreste Donzella, SVP/CMO, KLA Corp.

We are entering a new era for semiconductors – and technology in general – the era of data.

Every aspect of our modern life rotates around the data and semiconductors at the front and center of this new trend. The data economy and its impact on

semiconductors can be imagined as a wheel with four quadrants, representing creation, storage, analysis and transmission of data.

Data creation

We have been living in a mobile digital world for over 10 years, since the first smartphone was introduced. Since then, a billion devices have been sold, reaching unimaginable popularity all around the world. Smartphones are the primary instruments for creation of data and represent the number one driver of semiconductor revenue. The evolution of technology in the semiconductor front end and, more recently, packaging, is driving the smartphone's processors to be increasingly powerful and fast, while memory devices are called upon to store the massive amount of generated data. In addition, several custom chips are necessary for wireless communication, power management, camera control, display drivers and other functionalities. Semiconductors account for over 60% of an advanced smartphone's cost, with many players in the supply chain. The most advanced cars and IoT devices like wearables are also becoming a significant source of data, now driving more semiconductor content than ever.

Data storage

Once the data are generated, they need to be stored. In addition to local storage (e.g., inside smartphones or PCs), the last 2-3 years have seen an explosion of central storage in data centers. The demand for DRAM and NAND has exploded, driving a huge increase in overall CapEx and Wafer Fab Equipment (WFE) spending. WFE passed the $50B mark in 2017 and grew another 5% in 2018. The recent reduction in memory capacity investment is a result of excess inventory, given weaker smartphone demand and slower growth in data centers. Despite the recent correction, we expect long-term fundamentals for the memory business to remain strong, due to the large opportunity in data centers, where only 10% of data are stored in SSD NAND due to the relatively higher cost of SSD vs. HDD devices.

Data Analysis

DRAM will continue to be used in combination with high-performance computing chips, providing a powerful platform to analyze the massive amount of available data using machine learning algorithms.

The surge of AI applications is driving the transition from local centralized servers to massive cloud-based decentralized data centers, where it's possible to leverage the storage of large quantities of data and apply analytics for "learning." Semiconductors have been key to the rise of AI and data cloud services thanks to the advancement in high performing computing and accelerator chips, such as CPU, GPU and FPGA. Several 7nm design tape-outs support the proliferation of neural network models for AI learning in the cloud. This trend is going to accelerate once these AI applications are mature enough for significant adoption on connected devices beyond the cloud.

Data transmission

Once the data are created, stored and analyzed, the next step is to transfer the data over a communication medium to computing, network, communication or electronic devices. With the explosion of connected devices, digital communication has been increasingly challenged by bandwidth limitations, which 5G, fifth generation wireless technology, promises to solve. The expansion of frequency up to the millimeter waveband will dramatically increase data transfer speed and reduce network latency, two critical requirements for the next generation of autonomous cars and other applications. A new set of semiconductor devices, including processors, transceivers, RF modules, WiFi and modems will be designed to comply with new 5G protocol, thereby driving a significant growth opportunity throughout the semiconductor chain.

Conclusions

The semiconductor industry is entering a new golden era, with the data explosion driving multiple concurrent end applications for the first time in over fifty years. Process control continues to be a key enabler of semiconductor growth by accelerating new technology introductions and supporting yield ramps at leading and trailing edge logic and memory fabs. Critical inflections in automotive, like EV and autonomous driving, require near-perfect quality standards to avoid serious liabilities from fab escapes that fail once the board is integrated in the car. These requirements will increase the emphasis manufacturers must place on chip reliability. KLA is actively partnering with the entire automotive ecosystem, including OEMs, Tier 1 suppliers and IDMs, to explore new inline screening methodologies that minimize escapes and guarantee the highest standard of quality and reliability. ◆

Monitoring for excursions in automotive fabs

DAVID W. PRICE, **JAY RATHERT** *and* **DOUGLAS G. SUTHERLAND**, *KLA Corp., Milpitas, CA*

The Process Watch series explores key concepts about process control—defect inspection, metrology and data analytics—for the semiconductor industry. This article is the fourth in a series on process control strategies for automotive semiconductor devices.

The first three articles [1-3] in this series discussed methods that automotive semiconductor manufacturers can use to better meet the challenging quality requirements of their customers. The first paper addressed the impact of automotive IC reliability failures and the idea that combating them requires a "Zero Defect" mentality. The second paper discussed continuous improvement programs and strategies that automotive fabs implement to reduce the process defects that can become chip reliability problems. The third paper focused on the additional process control sensitivity requirements needed to capture potential latent (reliability) defects. This installment discusses excursion monitoring strategies across the entire automotive fab process so that non-conforming material can be quickly found and partitioned.

Semiconductor fabs that make automotive ICs typically offer automotive service packages (ASPs). These ASPs provide differentiated process flows – with elements such as more process control and process monitoring, or guaranteed use of golden process tools. The goal of ASPs is to help ensure that the chips produced meet the stringent reliability requirements of the automotive industry.

But even with the use of an automotive service package, excursions are inevitable, as they are with any controlled process. Recognizing this, automotive semiconductor fabs pay special attention to creating a comprehensive control plan for their critical process layers as part of their Process Failure Mode and Effects Analysis (PFMEA). The control plan details the process steps to be monitored and how they are monitored – specifying details such as the inspection sensitivity, sampling frequency and the exact process control systems to be used. A well-designed control plan will detect all excursions and keep "maverick" wafers from escaping the fab due to undersampling. Additionally, it will clearly indicate which wafers are affected by each excursion so that they can be quarantined and more fully dispositioned – thereby ensuring that non-conforming devices will not inadvertently ship.

To meet these objectives, the control plan of an automotive service package will invariably require much more extensive inspection and metrology coverage than the control plan for production of ICs for consumer products. An analysis of process control benchmarking data from fabs running both automotive and non-automotive products at the same design rule have shown that the fabs implement more defect inspection steps and more types of process control (inspection and metrology) for the automotive products. The data reveals that on average:

- Automotive flows use approximately 1.5 to 2 times more defect inspection steps
- Automotive flows employ more frequent sampling, both as a percentage of lots and number of wafers per lot
- Automotive flows use additional sensitivity to capture the smaller defects that may affect reliability

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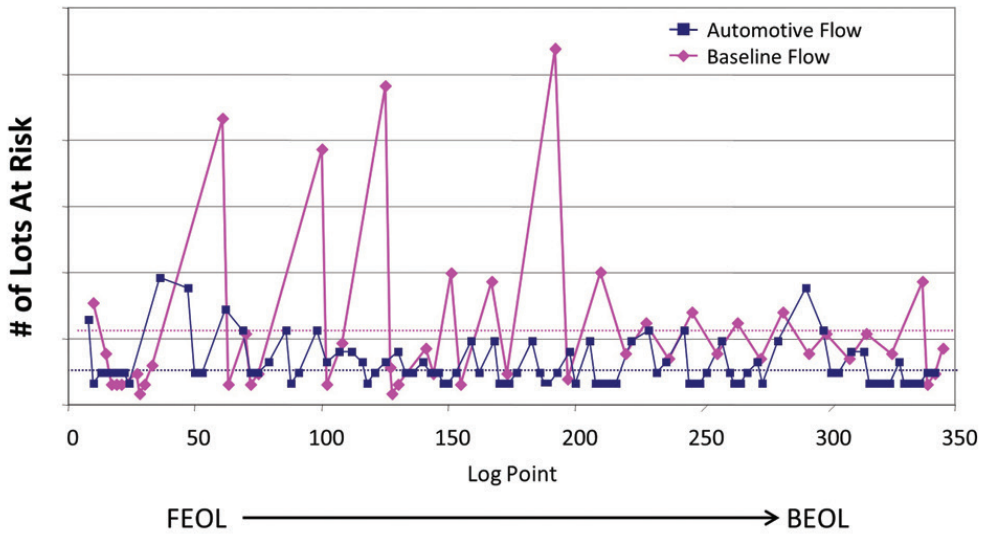

FIGURE 1. Example demonstrating the lots at risk between inspection points for an automotive process flow (blue) and a non-automotive (baseline) process blow (pink). The automotive process flow has many more inspection points in the FEOL and therefore fewer lots at risk when a defect excursion does occur.

The combined impact of these factors results in the typical automotive fab requiring 50% more process control capacity than their consumer product peers. A closer look reveals exactly how this capacity is deployed.

FIGURE 1 below shows an example of the number of lots between inspection points for both an automotive and a non-automotive process flow in the same fab. As a result of the increased number of inspection steps, if there is a defect excursion, it will be found much more quickly in the automotive flow. Finding the excursion sooner limits the lots at risk: a smaller and more clearly defined population of lots are exposed to the higher defect count, thereby helping serve the automotive traceability requirement. These excursion lots are then quarantined for high-sensitivity inspection of 100% of the wafers to disposition them for release, scrap, or when applicable, a downgrade to a non-automotive application.

The additional inspection points in the automotive service package have the added benefit of simplifying the search for the root cause of the excursion by reducing the range of potential sources. Fewer potential sources helps speed effective 8D investigations[4] to find and fix the problem. Counterintuitively, the increased number of inspection points also tends to reduce production cycle time due to reduced variability in the line.[5]

While increasing inspection capacity helps monitor and contain process excursions, there remains risk to automotive IC quality. Because each wafer may take a unique path through the multitude of processing chambers available in the fab, the sum of minor variations and marginalities across hundreds of process steps can create "maverick" wafers. These wafers can easily slip through a control plan that relies heavily on sub-sampling, allowing at-risk die into the supply chain. To address this issue, many automotive fabs are adding high-speed macro defect inspection tools to their fleet to scan more wafers per lot. This significantly improves the probability of catching maverick wafers and preventing them from entering the automotive supply chain.

Newer generation macro defect inspection tools[6] can combine the sensitivity and defect capture of many older generation brightfield and darkfield wafer defect inspection tools into a single platform that can

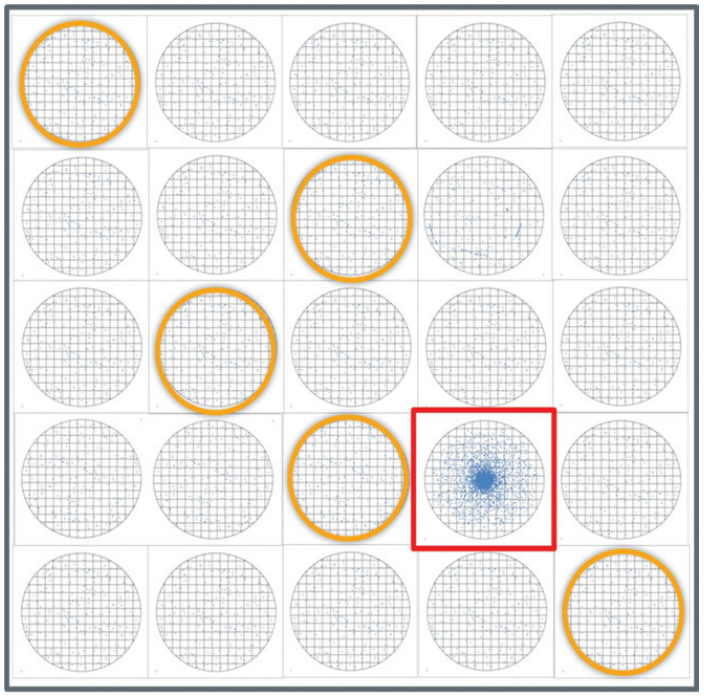

FIGURE 2. The legacy sample plan of 5 wafers per lot (yellow circles) would have allowed the single maverick wafer excursion (red square) to go undetected. High capacity macro defect inspection tools can stop escapes by reducing undersampling and the associated risks.

operate at nearly 150 wafers per hour, keeping cost of ownership low. In larger design rule 200mm fabs, the additional capacity often reveals multiple low-level excursions that had previously gone undetected, as shown in **FIGURE 2**.

In advanced, smaller design rule fabs, macro defect inspection tools lack the needed sensitivity to replace the traditional line monitoring and patterned wafer excursion monitoring roles occupied by broadband plasma and laser scanning wafer defect inspection tools. However, their high capacity has found an important role in augmenting the existing sample plan to find wafer-level signatures that indicate a maverick wafer.

A recent development in automotive control strategies is the use of defect inspection for die-level screening. One such technique, known as Inline Defect Part Average Testing (I-PAT™), uses outlier detection techniques to further enhance the fab's ability to recognize die that may pass electrical test but become reliability failures later due to latent defects. This method will be discussed in detail in the next installment of this series.

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Scalable SONOS based embedded non-volatile memory technology

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SONOS (Si-Oxide-Nitride-Oxide-Si) based eNVM technology is well-suited for System-On-a Chip (SOC) products as they are very compatible with standard logic/mixed-signal CMOS process flow. This paper describes how the SONOS based eNVM technology has been successfully developed and scaled down to 28nm node. With the shrink, SONOS has been seamlessly integrated into advanced front-end process flows with novel features such as stress enhancement techniques and High K-Metal Gate. Process/integration innovations have enabled the design rule shrink by minimizing the Vt variations of the memory cell devices in-spite of enhanced impact of dopant fluctuations. In addition, optimizations of the SONOS gate stack also have enabled the memory to have very high reliability even with scaling.

Why SONOS?

Critical factors for the choice of the NVM technology for an embedded memory include the cost of integration and the extent of its impact on the baseline CMOS device performance. SONOS is superior in both respects due to the simplicity of its integration (fewer extra lithography masks) as shown in **FIGURE 1** and the minimal impact on CMOS device performance (**FIGURE 2**) which means baseline device models are not affected by the integration. This gives a significant edge to SONOS for multiple product applications.

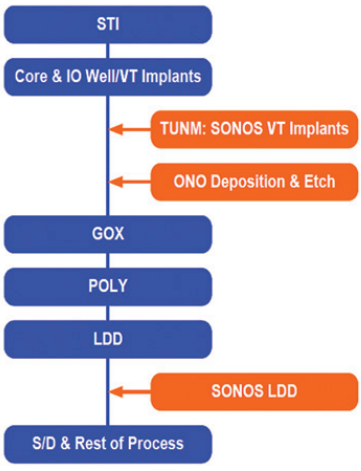

FIGURE 1. Typical process flow for SONOS integration.

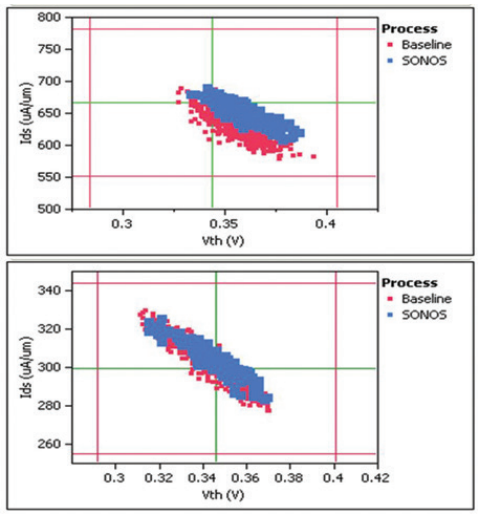

FIGURE 2. Device performance matching.

SONOS eNVM cell

A SONOS device structure and 2T-SONOS cell are schematically shown in **FIGURE 3**.

The cell consists of a SONOS Control Gate (CG) in series with a CMOS Select Gate. Structurally both are MOSFETs with the CG having a ONO gate dielectric and SG having a SiO2 or High K based gate dielectric. The CG is the memory device in which charge injected from the Si substrate across the thin tunnel oxide by Fowler-Nordheim tunneling is trapped in the Nitride (N) layer of the ONO stack. The charge can be either Positive (hole trapping) or negative (electron trapping) depending on the polarity of voltage applied to the gate. The trapped charge changes the threshold voltage (V_t) of the CG between a "Program (VTP)" and an "Erase (VTE)" state. The difference in Vt between the program and erase staes defines the memory window.

SONOS memory cell performance

The program/erase efficiency of a SONOS memory cell determines how well it can be programed or erased. The V_ts and Vt window are determined by the voltage appled across the ONO dielectric of the CG and the time duration of the program/erase pulse. The

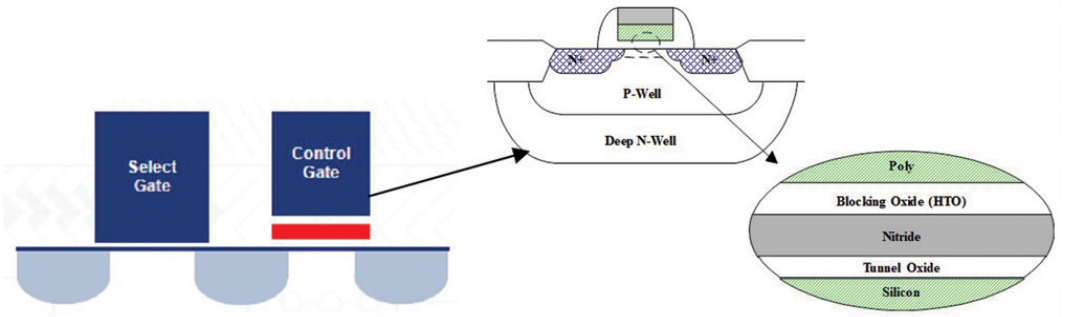

FIGURE 3. Schematic of 2T-SONOS Memory cell and SONOS device structure.

reliability of the memory cell defines its ability to maintain window enough to sense the two states clearly during the entire life of the memory. The initial window is maximized by optimizing the SONOS stack and program/erase conditions using the progamming curves which show how the VTP and VTE vary wit program/erase pulse width (**FIGURE 4a**).

The saturation in the VTE clearly indicates that the charge in the nitride, during erase, stops increasing because the additional hole charge injected from the substrate is compensated by the electron charge injected from the gate to the nitride. The injection from the gate is determined by the thickness and quality of the top oxide. Thinner or poor quality top oxide leads to increased injection from gate and shows increased erase saturation while a physically thicker top oxide drastically reduces injection from gate and hence results in much lower erase saturation (**FIGURE 4b**).

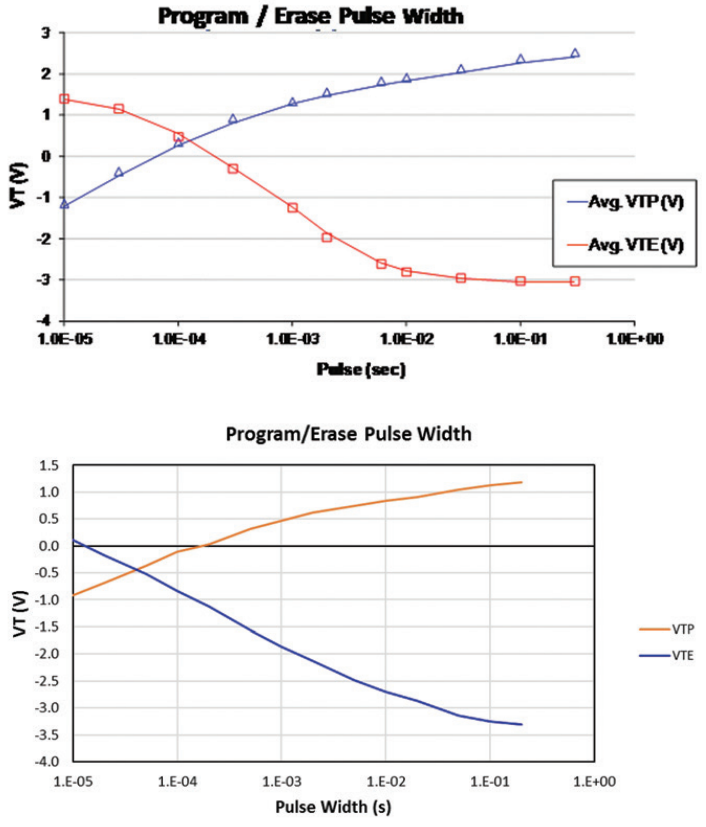

FIGURE 4. Program-Erase characteristics of SONOS cell with (a) Normal and (b) thicker top oxide.

Endurance and Data Retention are the most critical specifications for a NVM and these reliability requirements are becoming more stringent as embedded NVM products are getting into new markets such as automotive electronics. SONOS typically has good endurance performance (**FIGURE 5a**). With the engineering of a unique, proprietary ONO stack, robust retention performance has been achieved for all Cypress products (**FIGURE 5b**). On certain integration flows, SONOS eNVM can meet automotive retention specs.

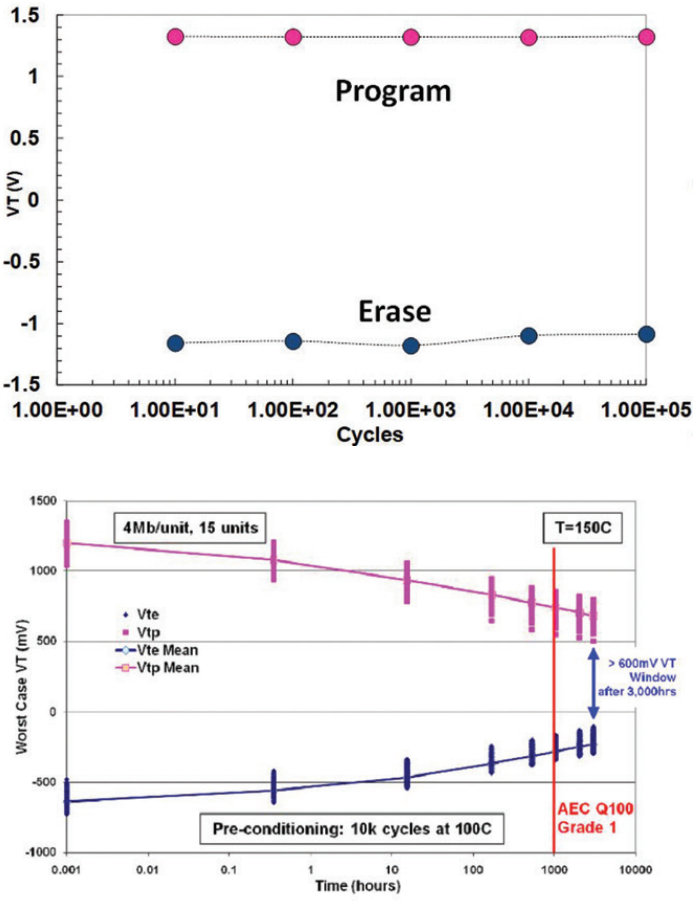

FIGURE 5. SONOS Reliability – (a) Endurance (b) Retention.

SONOS cell scaling – V_t uniformity

To meet the ever increasing demand for larger memories, the SONOS memory cell is shrunk by moving to more advanced technologies to take advantage of tighter design rules. Cell size trend with technology nodes, demonstrated on Silicon, is shown in **FIGURE 6** for two types of SONOS cells, Dedicated Source Line (DSL) and Common Source Line (CSL).

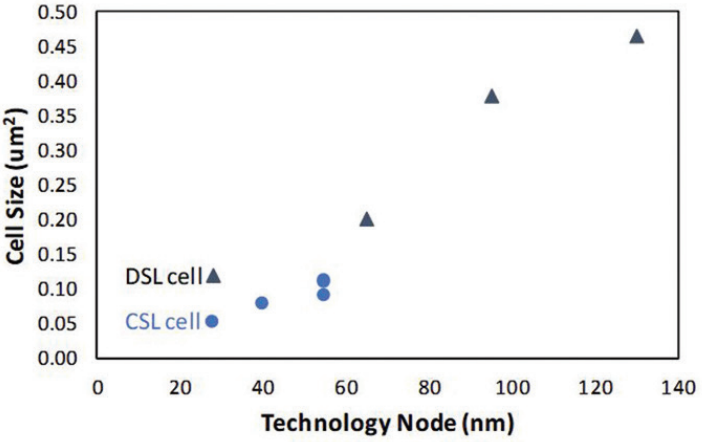

FIGURE 6. Trend of SONOS cell size.

The key challenege for the shrink is the degradation of V_t uniformity on account of increased impact of Random Dopant Fluctuations (RDF) at the surface of the channel of the SONOS device. This can be due to the inherent effect of dopants enhanced by diffusion of dopants during high temperature steps. For successful shrink, several process modifications, especially reduction of dopants in the surface of the channel of CG and use of deeper channel implants with heavier species such as Indium is required so as to keep surface dopant concentrations low. In addition, doping by species such as Carbon can reduce the transient enhanced diffusion of channel dopants. Reduction in thermal budget after SONOS stack formation also lowers the diffusion of dopants to the surface and hence reduces RDF. With the use of such techniques, the V_t sigma can be kept reasonably low with technology shrink as shown in **FIGURE 7**. The impact of new doping strategies on maintaining a low V_t sigma is clearly seen in this trend which shows how process optimizations lowers sigma in all technology nodes. At the beginning of technology development such as in 28nm node, the sigma is typically high. With process and /or cell optimizations, the sigma becomes lower. A typical example of Vt sigma improvement with reduction in the diffusion of dopants to the surface of channel of CG is shown in **FIGURE 8** below.

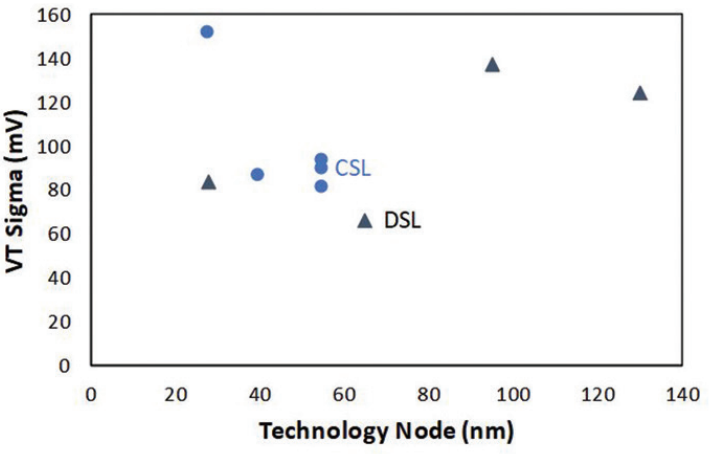

FIGURE 7. V_t sigma trend with technology shrink.

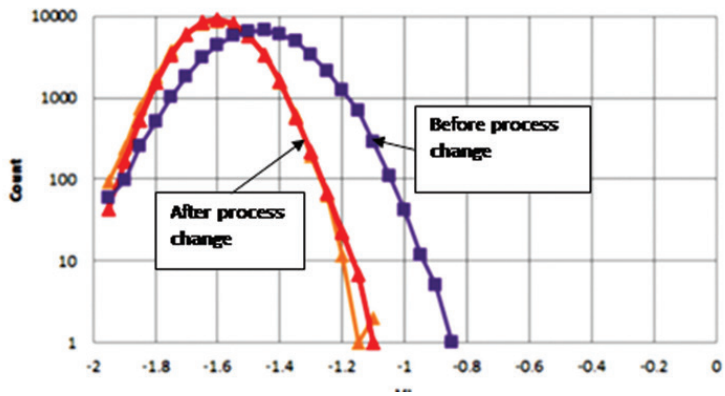

FIGURE 8. Vt sigma improvement.

Maintaining a low sigma greatly helps to minimize the flash yield loss due to widening of Vt distribution at Beginning of Life (BOL) and at End of Life (EOL), typically after a high temperature bake.

SONOS integration into High K-Metal gate process flow

With the transition of CMOS technology to High K-Metal Gate (HKMG) at 28nm node and beyond, it is imperative that SONOS be compatible with HKMG. This has been demonstrated at 28nm node with an integration approach that has the HK dielectric as part of the top oxide of the ONO stack and the MG as the gate of the CG. This is a true integration of HKMG into SONOS device and enables embedded memory products in very advanced technology nodes. Endurance and retention curves for a SONOS cell with HKMG (**FIGURE 9**) show that robust reliability can be achieved with a greatly shrunk NVM cell.

SONOS for analog NVM

Analog memory is emerging as a strong candidate for "AI edge" applications. Analog NVM uses NVM array with all WLs turned on in 1 block to sum currents. Power needed for making an "inference" is ~1000X lower using analog NVM compared to GPU. Applications are in speech

processing, image processing etc. without uploading to the cloud. The memory has multiple levels (8 or 16) and each I_D/V_T level is a "weight" for the inference and 16 levels can give very low error rates. ~1-3% overlap of distributions between neighboring VT levels is acceptable.

Key requirements for analog memory for AI edge are

1. 8 to 16 I_D/V_T levels between 1E-11A to 1E-5A (lower current levels improve power efficiency)
2. To achieve ~1-3% overlap of distributions we need levels to be ~5sigmas apart (peak to peak)
3. Uniform subthreshold slope is preferred, otherwise there is larger error in targeting different ID levels
4. 1K cycles endurance is sufficient; cycle-to-cycle stability in ID is required (no issue for SONOS)
5. Refresh of weights possible once a year (1 year at 55C retention is acceptable)
6. Program time of whole array is a concern

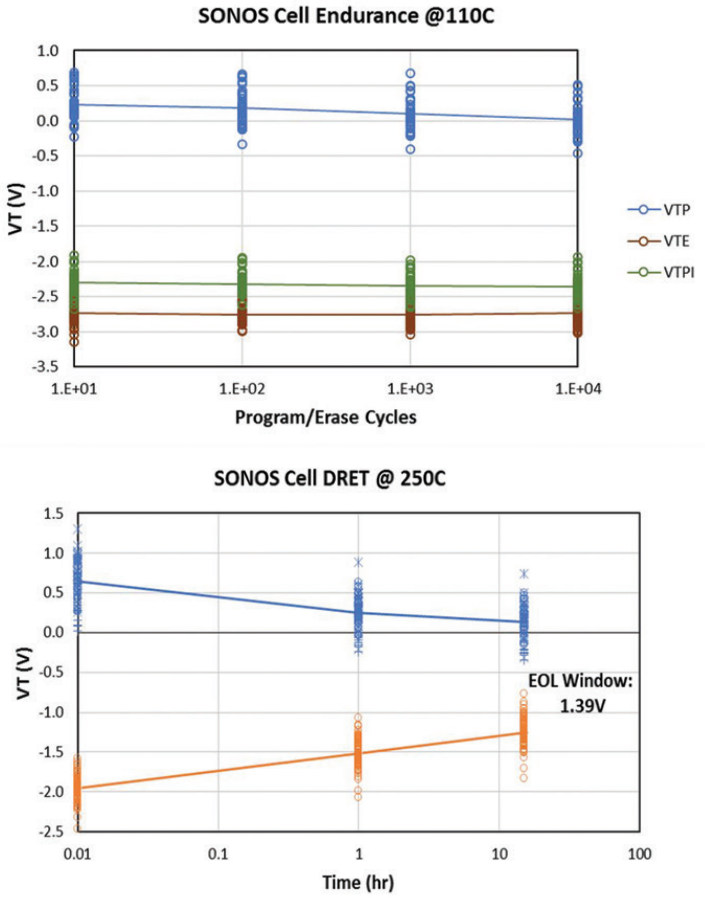

FIGURE 9. Endurance and Retention of SONOS cell integrated into High K-Metal Gate process flow.

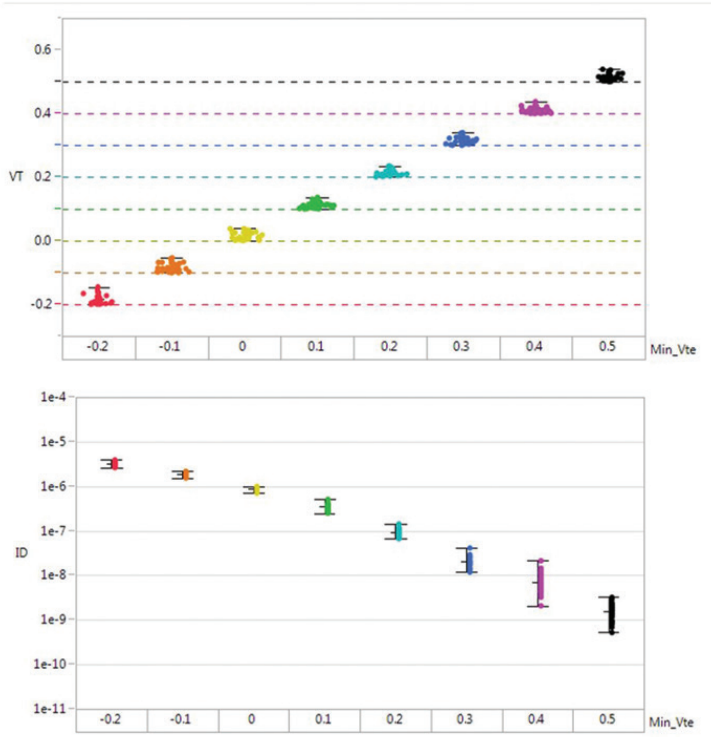

FIGURE 10. Multiple Vt (left) or Id (right) levels of analog SONOS memory.

SONOS is a very promising option for the analog memory with multiple levels due to the low Vt sigma. This can be achieved by programming / erasing the SONOS cell to different but distinct Vt or Cell current values, separated by gaps required to sense them as different states of the memory. Soft program or erase is used to place the memory cell at distinct target Vt/Id values with a tight distribution. An illustration of this concept, achieved on test structure arrays is shown in **FIGURE 10**.

Although this data is preliminary, it shows that SONOS array can be used for analog memory with the right conditions of program/erase.

Conclusions

It is clear from the above sections that SONOS is a very strong option for eNVM in all advanced nodes, the key advantage being the simplicity of integration into a baseline flow. In addition, it seems to be a very good option for analog memory used in AI edge applications.

A Colpitts Quadrature VCO for 2.4 GHz bluetooth/WLAN applications

FEI YU, **LIXIANG LI**, **LEI GAO**, **SHUO CAI** *and* **YUN SONG**, *Changsha University of Science and Technology, China*

A new symmetrical Colpitts quadrature voltage-controlled oscillator (QVCO) with Q-enhancement technique to improve phase noise performance in 0.18 μm CMOS process for 2.4 GHz Bluetooth/WLAN applications is proposed.

With development of the information technology, security issues are attracting increasing attention [1]. The demand for low-power and low-cost wireless CMOS transceivers is significantly increasing in the wireless encryption communication field, especially for Bluetooth and WLAN transceivers in the 2.4 GHz band IEEE 802.15.4 standard [2]. One of key building blocks in Bluetooth and WLAN transceivers is a quadrature voltage-controlled oscillator (QVCO) where low phase noise property and wide tuning range are required. Quadrature phases can be produced by ring oscillators, frequency dividers, RC poly-phase filters, delay-locked loops, and cross-coupled injection oscillator topologies. In these methods, the cross coupled LC QVCOs have attracted much attention due to its easy to realize and reliable start up [3]. In the previous work of the author, a LC QVCO was proposed with low phase noise by using the gate-modulated coupling technique [4]. However, the power consumption of the circuit was a bit large, and the flicker and thermal noise perturbed the oscillator outputs at their zero-crossings and degraded the LC QVCO phase noise [5]. Compared to the traditional cross-coupled LC QVCOs, colpitts oscillators have excellent cyclostationary noise characteristics and better phase noise performance [6].

In the recently reported QVCOs, the differential Colpitts oscillators have gradually replaced the cross-coupled oscillators to achieve a lower phase noise [5–13]. In [5], a current switching and gm-enhancement Colpitts QVCO are proposed, which has low phase noise and low power consumption. However, the disadvantage of this topology was that the active device must have a higher gain in order to start the oscillation. Injection-locked Colpitts QVCOs based on first-harmonics [7], [8] and super-harmonics [9], [10] injection have been widely used in RF circuits because of their good phase noise. In order to further improve the phase noise and ensure robust startup of the QVCO, tail-current shaping techniques are used [11–13]. By shaping the tail-current of the QVCO, the thermal noise power spectrum density which was produced by the transistors can be modulated to reduce the phase noise of the oscillator [11]. Meanwhile, in order to provide a reliable startup mechanism, the bias scheme was usually used to make it an ideal choice for high performance oscillator [13]

In this paper, a symmetrical Colpitts QVCO with tail-current and Q-enhancement techniques is presented that features low phase noise and wide tuning range. The Colpitts QVCO topology has excellent phase noise and low power consumption. The QVCO configuration uses the capacitance feedback devices at the core of the Colpitts oscillator and does not use other additional coupling devices. The proposed QVCO circuit is designed with the 0.18 μm CMOS process and operated in the 2.4 GHz band.

Analysis and design of Colpitts QVCO

Tail-current feedback structure: **FIGURE 1(a)** depicts the schematic of the conventional VCO with the tail injection method. The outputs of the oscillator V_p and V_n have the frequency component at the frequency $\omega 0$, while the common source of the switching transistors

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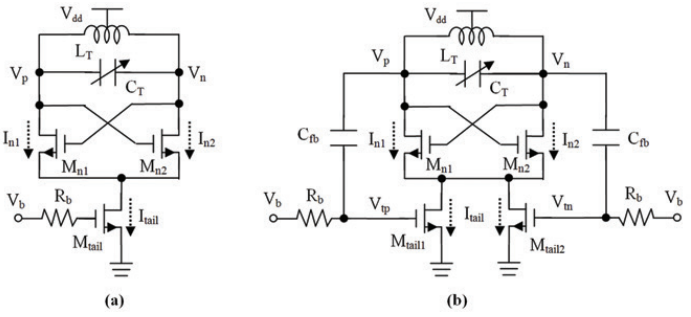

FIGURE 1. (a) Conventional tail injection VCO, (b) Tail-current feedback VCO.

oscillates at 2ω0 [8]. A VCO topology with tail-current feedback structure is shown in **Fig. 1(b)**. *Mtail*1,2 are DC biased by *Vb* through resistors *Rb* and outputs *Vp* and *Vn* are feedback to the gates of *Mtail*1,2 through capacitors *Cfb*. By setting the *Vb* to the threshold voltage, *Mtail*1,2 would periodically work from strong inversion to accumulation which physically reduces its 1/f noise [12]. Meanwhile, since the feedback capacitor *Cfb* is in parallel with *Cgsn*1 + *Cgstail*1 (*Cgsn*1, *Cgstail*1 are the gate-source capacitance of M*n*1 and M*tail*1 in saturation region), the actual parasitic capacitance is reduced and the larger tuning range can be provided, which is also demon- strated in [13]. The related waveforms are shown in **FIGURE 2**, the I*tail* reaches the maximum at the peaks of *Vn* when *Vn* > *Vdd* and the phase is less than 180◦, then I*tail* decreases to the zero when *Vn* < *Vdd*. Using the tail current feedback structure, the effective impulse sensitivity function of the noise sources from QVCOs can be reduced [12]. Therefore, a QVCO by use of tail-current structure is beneficial to low phase noise.

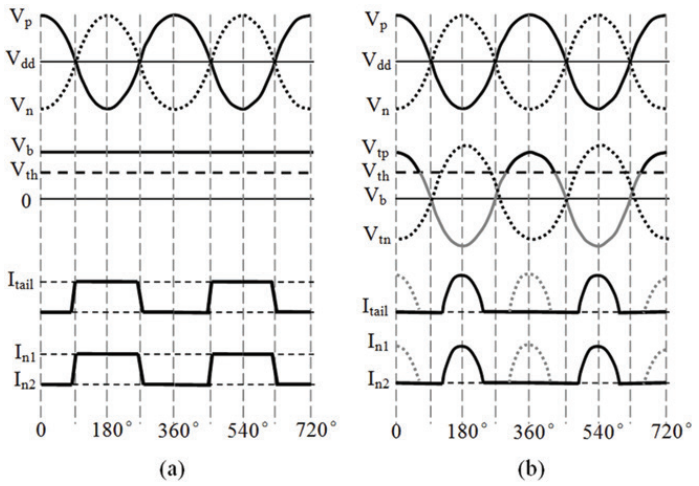

FIGURE 2. Waveforms of (a) conventional tail injection VCO and (b) tail-current feedback VCO.

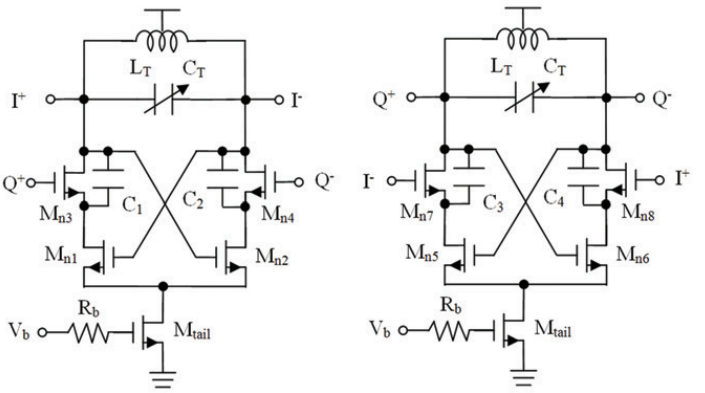

FIGURE 3. Colpitts QVCO with Q-enhancement circuit.

Q-enhancement technique **FIGURE 3** shows the architecture of a power-efficient current- switching Colpitts QVCO using Q-enhancement technique. The NMOS M*n*1, M*n*2, M*n*3 and M*n*4 are composed of cascode connection being symmetric architecture. Additional capacitances *C*1–4 in parallel with cross-couple devices (*Mn*1–8) that form a positive feedback loop which are used to increase the quality factor Q. The cross-coupled pair reuses the current from the core of the oscillator to improve the small-signal loop gain and the startup condition. Addition- ally, the external capacitances improve the amplitude of the oscillator outputs waveform [11]. Therefore, the phase noise of the QVCO can be further improved.

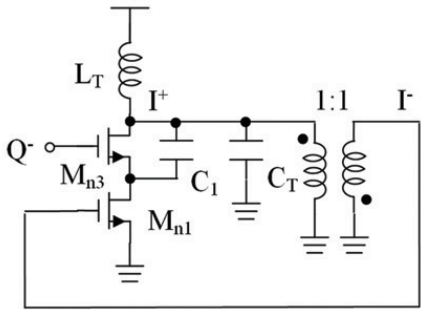

FIGURE 4. I-channel half circuit of the colpitts QVCO using Q-enhancement technique.

FIGURE 4 displays a half circuit (i.e., I-channel) of the Colpitts QVCO wherein the cross-coupled is modeled by using an ideal transformer. Therefore, a small-signal circuit diagram, as shown in **FIGURE 5**, can be generated. *In* is an input white noise current source, and *GT* is the conductance of the LC tank. The *gmn*1 and *gmn*3 are the small-signal transconductances of M*n*1 and M*n*3. *Cgsn*1 and *Cgsn*3 are the gate-source capacitance of M*n*1 and M*n*3. gdsn1 and *gdsn*3 are the gate- drain on resistance of M*n*1 and M*n*3 in triode region. The quality factor of the LC tank is assumed to be limited only by the loss of the inductor.

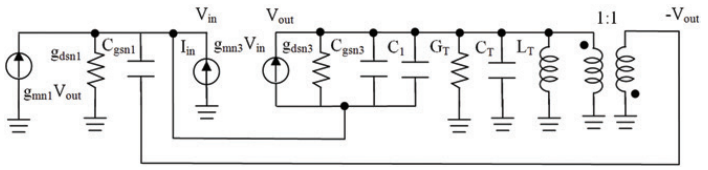

FIGURE 5. Small signal equivalent model of Fig. 4.

According to the Kirchhoff's Current Law, the loop gain of the I-channel half circuit of the Colpitts QVCO can be gotten as (1):

$$Z_{QVCO} = Z_R + jZ_I = -\frac{g_{dsn1}}{\omega^2 L_T C_p} - g_{mn1} + \frac{g_{dsn3}C_{gsn1} + G_T C_{gsn1} + g_{dsn1}C_q}{C_p} + j\left[\omega\frac{(C_1 + C_{gsn3} + C_T - C_{gsn1})C_{gsn1}}{C_p} + C_{gsn1}\right] - j\frac{C_{gsn1} + G_T L_T g_{dsn1} + g_{dsn1}g_{dsn3}L_T}{\omega C_p L_T}. \quad (1)$$

then

$$G_{QVCO} = \frac{1}{Z_{QVCO}}, \quad (2)$$

where $C_p = C_1 + C_{gsn1} + C_{gsn3}$, $C_q = C_1 + C_T + C_{gsn3} - C_{gsn1}$ and Z_{QVCO} can be derived as (2). According to the Barkhausen Criterion, the oscillation condition is satisfied with Z_{QVCO} in (2) real and negative. By setting $Z_I(\omega_0) = 0$, the oscillating frequency ω_0 is obtained:

$$\omega_0 = \sqrt{\frac{C_{gsn1} + L_T g_{dsn1}\left(g_{dsn3} + G_T\right)}{L_T C_{gsn1}\left(C_p + C_q\right)}}. \quad (3)$$

The loaded Q of the oscillator is defined as [14]:

$$Q(\omega) = \frac{\omega}{2}\left|\frac{df}{d\omega}\right| = \frac{\omega}{2}\left|\frac{1}{Z_R(\omega)}\right|\left|\frac{\partial Z_I(\omega)}{\partial \omega}\right|, \quad (4)$$

from (2), we have

$$Z_R(\omega) = -\frac{g_{dsn1}}{\omega^2 L_T C_p} - g_{mn1} + \frac{g_{dsn3}C_{gsn1} + G_T C_{gsn1} + g_{dsn3}C_q}{C_p},$$
$$\frac{\partial Z_I(\omega)}{\partial \omega} = \frac{C_q C_{gsn1}}{C_p} + C_{gsn1} + \frac{C_{gsn1} + g_{dsn1}g_{dsn3}L_T + G_T L_T g_{dsn1}}{\omega^2 C_p L_T}. \quad (5)$$

Substitute (5) and (6) into (4):

$$Q(\omega) = \frac{\omega}{2}\frac{\omega^2 C_{gsn1}L_T\left(C_p + C_q\right) + C_{gsn1} + g_{dsn1}L_T\left(g_{dsn3} + G_T\right)}{\omega^2 L_T\left[C_{gsn1}\left(g_{dsn3} + G_T\right) + g_{dsn1}C_q - g_{mn1}C_p\right] - g_{dsn1}}. \quad (6)$$

Consider (7) for the special case of $C_{gsn1} = C_{gsn3} = 0$ and $g_{dsn1} = g_{dsn3} = 0$ with: (7)

$$G_T = \frac{1}{\omega_0 Q_T L_T}. \quad (8)$$

Combining (3) and (7) gives:

$$\omega_0 \approx \frac{1}{\sqrt{L_T\left(C_T + 2C_1\right)}},$$
$$Q\left(\omega_0\right) \approx \frac{1}{2}\omega_0^2 Q_T L_T\left(C_T + 2C_1\right). \quad (9)$$

From the previous small-signal analysis and (9), it can be seen that the capacitive feedback technique can effectively enhance the quality factor Q.

The proposed Colpitts QVCO

Our designed Colpitts QVCO using tail-current feedback and Q-enhancement techniques is shown in **FIGURE 6**. QVCO quadrature outputs are fed to M_{n3}, M_{n4}, M_{n11} and M_{n12} through capacitors C_{fb} to achieve tail-current shaping. Two varactors C_{var} controlled by tuning voltage V_{ctrl}. Capacitances C_{1-4} in parallel with cross-couple devices (M_{n7}, M_{n8}, M_{n15} and M_{n16}) that form a positive feedback loop which are used to increase the oscillator quality factor Q. By periodically turning ON and OFF the transistors M_{n5}, M_{n6}, M_{n13} and M_{n14}, the tail-bias is reduced. This action averages the current flowing through the capacitor C_b thus bringing down the voltage at node V_b and reduces the conduction angle and improves the current efficiency [13]. Benefit from the relaxed voltage headroom of the proposed structure, additional PMOS cross-coupled pairs (M_{p1-p4}) can be added to implement the current-reuse complementary QVCO configuration to further improve g_m and reduce power consumption.

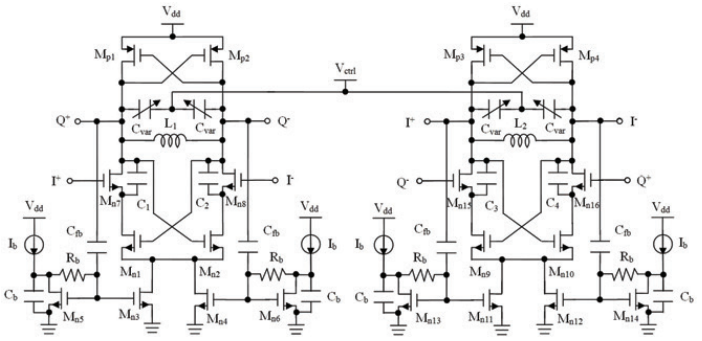

FIGURE 6. Proposed QVCO using tail-current feedback and Q-enhancement techniques.

Simulation Results

The proposed Colpitts QVCO is designed and simulated in a standard 0.18 μm RF CMOS process. **FIGURE 7** shows the simulated waveforms. When the frequency sweep from 0 to 1.4 V, the oscillation frequency ranges from 2.3 to 3.1 GHz, and the tuning range is 29.6%, as shown in **FIGURE 8**. The total dc current from 1.4 V power supply is 4.29 mA, resulting in the total power consumption of 6.0 mW. The proposed QVCO achieves a phase noise of -128 dBc/Hz at 1 MHz offset from a 2.4 GHz carrier frequency as shown in **FIGURE 9**.

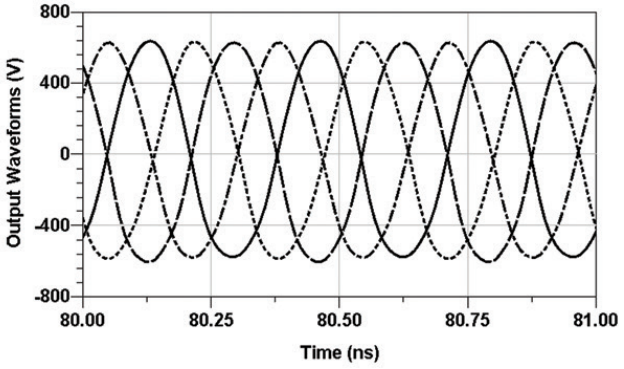

FIGURE 7. Voltage swing of the proposed QVCO.

Conclusion

The tail-current feedback and Q-enhancement techniques have been used to achieve a Colpitts QVCO with low phase noise, wide tuning range and high FOM. Based on the proposed architecture, the QVCO designed using 0.18 μm CMOS process exhibits a simulated 29.6% tuning range around 2.4 GHz. At a supply voltage of 1.4 V, the simulated phase noise is -128 dBc/Hz at a 1 MHz offset, and the QVCO consumes 6.0 mW dc power which can be applicable to 2.4 GHz Bluetooth/WLAN direct-conversion applications.

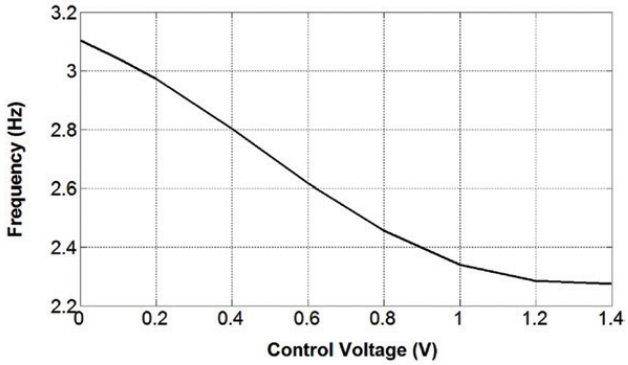

FIGURE 8. Characteristic of the proposed QVCO tuning range.

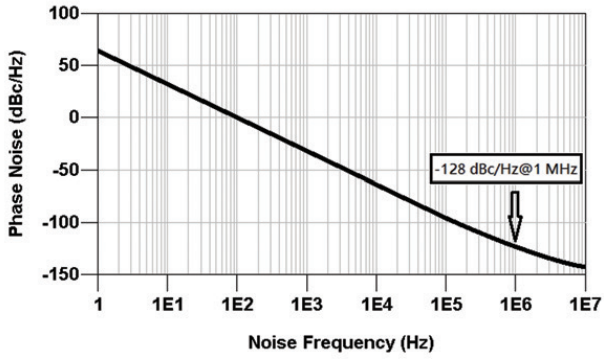

FIGURE 9. Phase noise of the 2.4 GHz Colpitts QVCO.

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Despite uncertainty, long-term semiconductor market outlook remains bright

This year, SEMI ISS covered it all – from a high-level semiconductor market and global geopolitical overview down to the neuro morphic and quantum level. Here are key takeaways from the Day 1 keynote and Economic Trends and Market Perspectives presentations.

In the opening keynote, Anne Kelleher from Intel pointed to the huge growth of data, with fabs collecting more than 5 billion sensor data points each day. The challenge, Kelleher noted, is to turn massive amounts of data into valuable information. Moore's law is not dead. New models of computing benefit still from Moore's law and advances in Si/CMOS technologies for conventional, deep learning, neuro morphic and quantum computing.

With customers expecting continual improvements in applications, the question is whether the chip industry is moving fast enough to meet these expectations, Kelleher said. A broad supply chain, equipment and materials innovations, and attracting the "best of the best" college graduates to fuel innovation is key, she said.

In the economic trends session, Nicholas Burns (ambassador ret.) from Harvard University pointed out that we will see a major shift in power. The U.S. will remain the major world power over the next 10 years, but we will see a major shift in power in the next coming decades as the gap with countries like China, Russia and India continues to narrow.

Duncan Meldrum from Hilltop Economics said that we are passing the peak growth of economic cycle. He warns that a more likely outlook is that a global growth recession is developing. Although semiconductor MSI growth will see a noticeable slowdown in 2019 and 2020, the semiconductor industry is still healthy over the longer term.

Bob Johnson from Gartner sees demand shifting from consumer to commercial applications with higher ROIs and budgets. AI, IoT and 5D are the major enablers. He sees structural changes in the semiconductor industry especially for memory but also for Moore's law with increasing costs and fewer players.

The DRAM markets shows volatility and NAND market may be negative in 2019 but non-memory are expected to accelerate mainly because of increasing content and some price hikes.

Overall Gartner expects good long-term growth with a CAGR (2017 to 2022) of 5.1%, outpacing 2011 to 2016 CAGR of 2.6%. After a strong 2018 with 13.4% revenue, he forecasts a slower 2019 with 2.6% growth followed by a 8% growth in 2020 and negative growth rate in 2021.

Andrea Lati of VLSI went "Back to fundamentals" in his presentation about the industry. VLSI sees a downside bias due to slowing global economy, tariffs, and trade wars. Future drivers are data economy, cloud, AI and automotive.

As memory leads the 2019 slowdown, analog, power, logic and other sectors remain in positive territory. VLSI lowered its semiconductor equipment forecast for 2018 from 20% (Jan. 2018) to 14% (Dec. 2018) but increased its sales outlook from 8% to 15% in 2018. VLSI expects revenue to slow into the first half of 2019 but increase to over 4% in the second half of the year, resulting in total 2019 drop of 2.7%. Semiconductor equipment sales are expected to drop from 14% in 2018 to -10% in 2019.

Michael Corbett of Linz Consulting, covering wafer fab materials in the years of 3D scaling, sees these as good

CHRISTIAN G. DIESELDORFF, *senior principal analyst in the Industry Research and Analysis group at SEMI*

times for the industry. His outlook for wafer fab materials is bullish based on strong MSI and because wafer fab materials suppliers are getting bigger because of M&As.

In the Market Perspective session, Sujeet Chand of Rockwell Automation pointed out that as more and more data is generated, the problem is how to get value of all the data collected. There is a need to create the right architecture for machine learning and AI and big data is increasingly being replaced by contextual/structured data. He expects Industry 4.0 to drive foundries to become smaller, more flexible and more productive.

In the Technology and Manufacturing session, Aki Sekiguchi of TEL addressed process challenges in the age of co-optimization. The semiconductor industry continues to expand, driven by massive growth of interconnected devices, with heavy demand for processing power and storage. He expects an exponential increase of data from about 40ZB in 2018 to 50ZB in 2020 to 163 ZB in 2026.

Major technologies such as DRAM, 3D NAND and logic are dealing with scaling challenges. The density of DRAM (Mb/chip) is plateauing according to 2015 to 2020 trend data, with DRAM is in need of EUV. Memory capacity demand is leading to increasing layers and higher aspect ratios that is concern for 3D NAND and mainly for plasma etch. With Logic already implementing 3D structures, it appears to be in a solid position.

Buddy Nicoson of Micron talked about his 50 years in the industry and looked ahead to the next 50. The anchors – quality, cost, scale and speed – won't change. It has been a great journey so far with unprecedented opportunities and challenges ahead of us. We are getting into a convergence (specialization, integration) and solution-based phase. We will see some inflection points in the coming years, with the best yet to come. ◆

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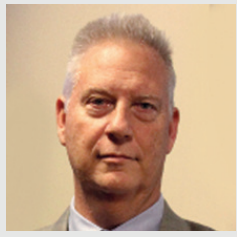

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