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Insights for Electronics Manufacturing

Overlay Performance of TSV-last Lithography for 3D Packaging P.16

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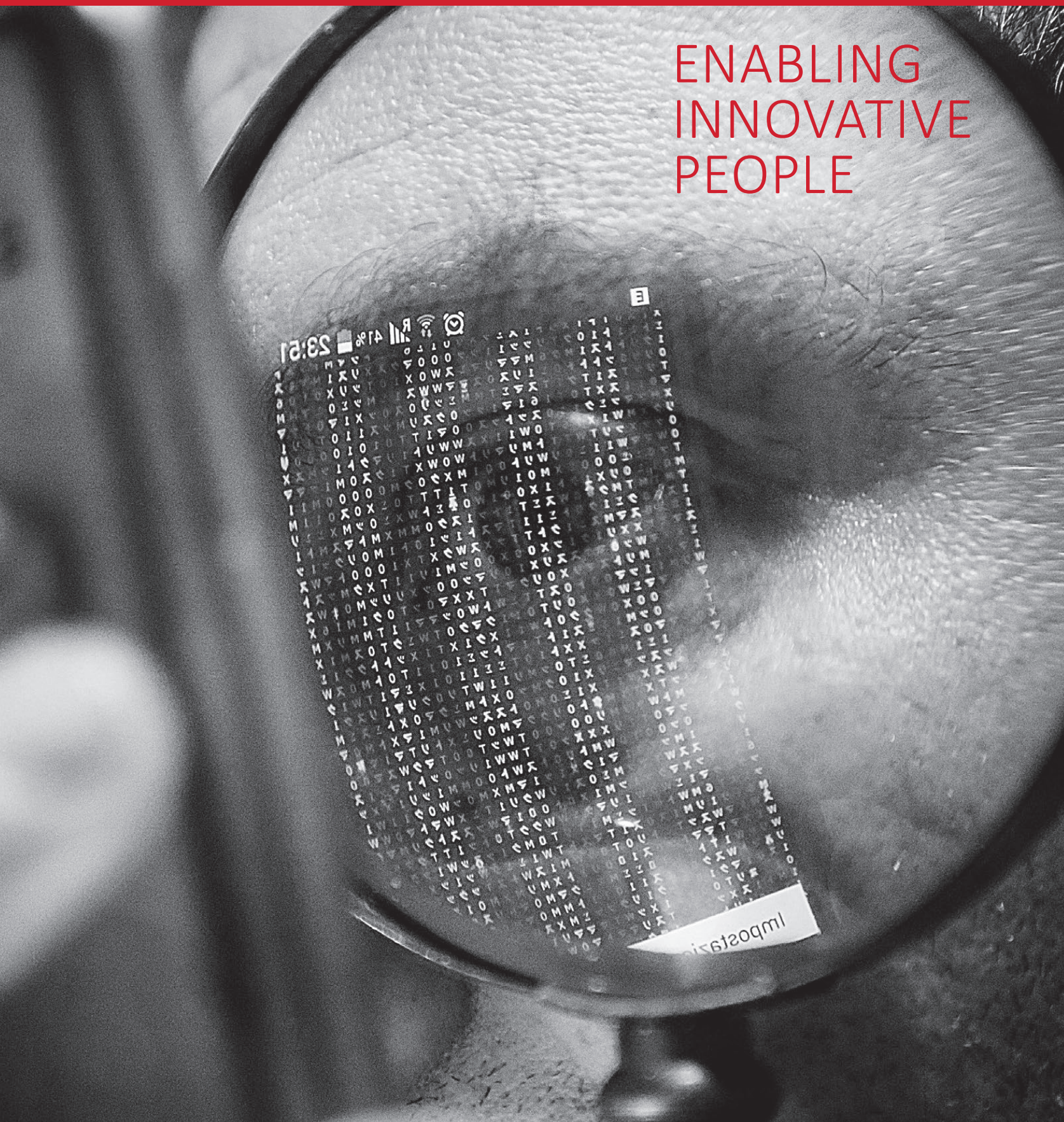

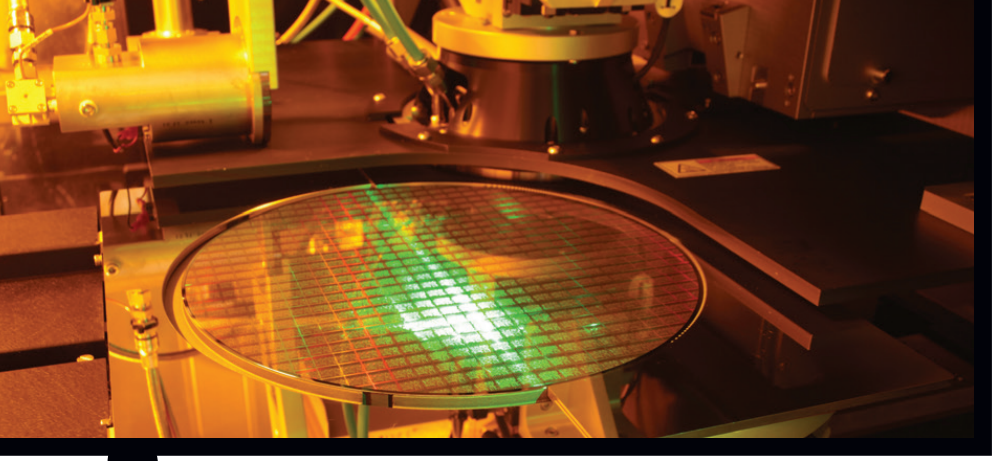

Solid State TECHNOLOGY®

JULY 2018 VOL. 61 NO. 5

Caption: The Veeco-Ultratech AP300 meets challenging 3D packaging requirements such as through silicon via with its variable numerical aperture lens that can be optimized to maximize depth of focus while maintaining higher resolution performance. Source: Veeco Instruments

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editorial

The cobbler's children getting shoes?

There's an old proverb that the shoemaker's children always go barefoot, indicating how some professionals don't apply their skills for themselves. Until lately, that has seemed the case with the semiconductor manufacturing industry which has been good at collecting massive amounts of data, but no so good at analyzing that data and using it to improve efficiency, boost yield and reduce costs. In short, the industry could be making better use of the technology it has developed.

That's now changing, thanks to a worldwide focus on Industry 4.0 – more commonly known as "smart manufacturing" in the U.S. – which represents a new approach to automation and data exchange in manufacturing technologies. It includes cyber-physical systems, the Internet of things, cloud computing, cognitive computing and the use of artificial intelligence/deep learning.

At SEMICON West this year, these trends will be showcased in a new Smart Manufacturing Pavilion where you'll be able to see - and experience - data-sharing breakthroughs that are creating smarter manufacturing processes, increasing yields and profits, and spurring innovation across the industry. Each machine along the Pavilion's multi-step line is displayed, virtually or with actual equipment on the floor - from design and materials through front-end patterning, to packaging and test to final board and system assembly.

In preparation for the show, I had the opportunity to talk to Mike Plisinski, CEO of Rudolph Technologies, the sponsor of the Smart Pavilion about smart manufacturing. He said in the past "the industry got very good at collecting a lot of data. We sensors on all kinds of tools and equipment and we'd a track it with the idea of being able to do predictive maintenance or predictive analytics. That I think had minimal success," he said.

What's different now? "With the industry consolidating and the supply chains and products getting more complex that's created the need to go beyond what existed. What was inhibiting that in the past was really the ability to align this huge volume of data," he said. The next evolution is driven by the need to improve the processes. "As we've gone down into sub-20 manometer, the interactions between the process steps are more complex, there's more interaction, so understanding that interaction requires aligning digital threads and data streams." If a process chamber changed temperature by 0.1°C, for example, what impact did it have on lithography process by x, y, z CD control. That's the level of detail that's required. "That that has been a significant challenge and that's one of the areas that we've focused on over the last four, five years -- to provide that kind of data alignment across the systems," Plisinski said.

Every company is different, of course, and some have been managing this more effectively than others, but the cobbler's children are finally getting new shoes.

—Pete Singer, Editor-in-Chief

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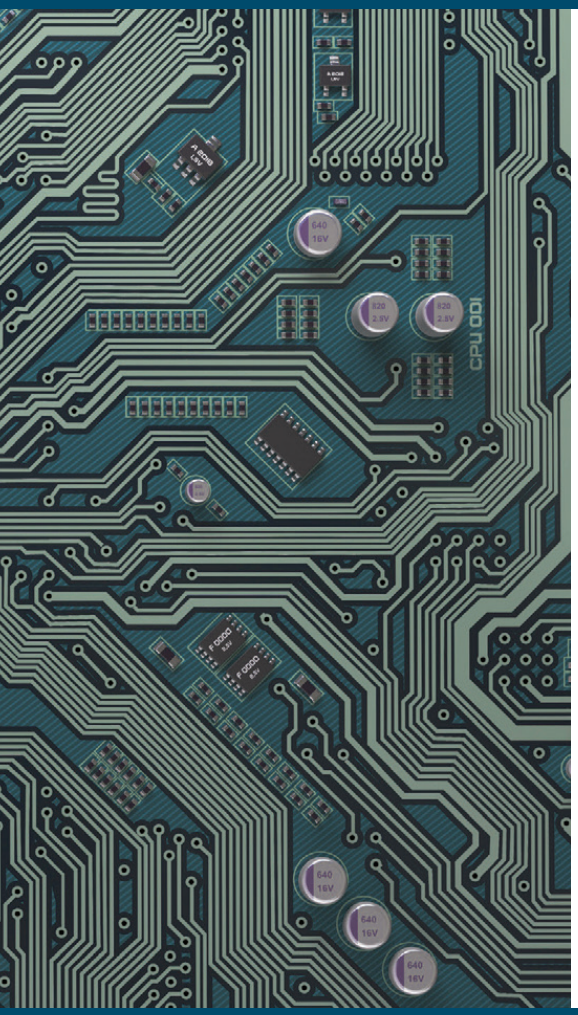

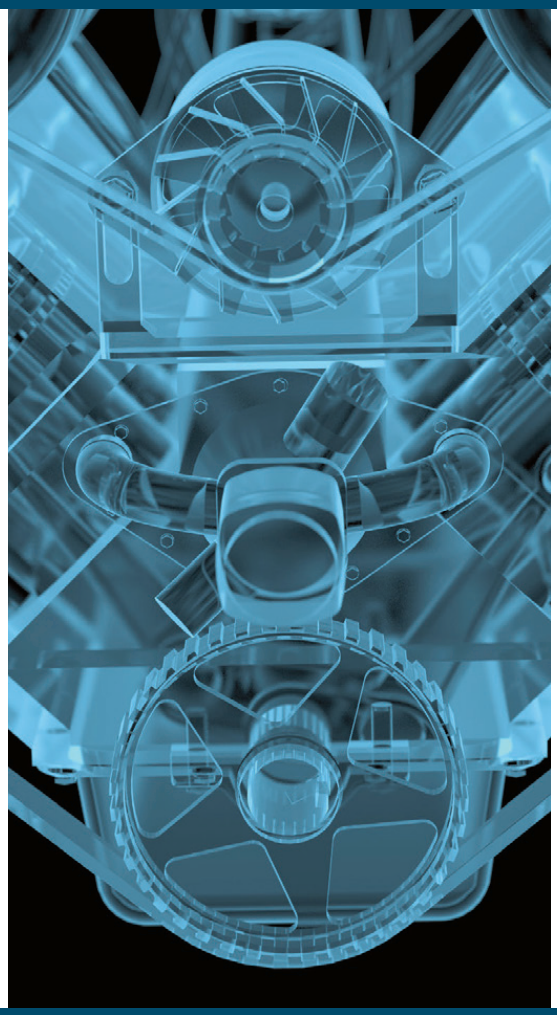

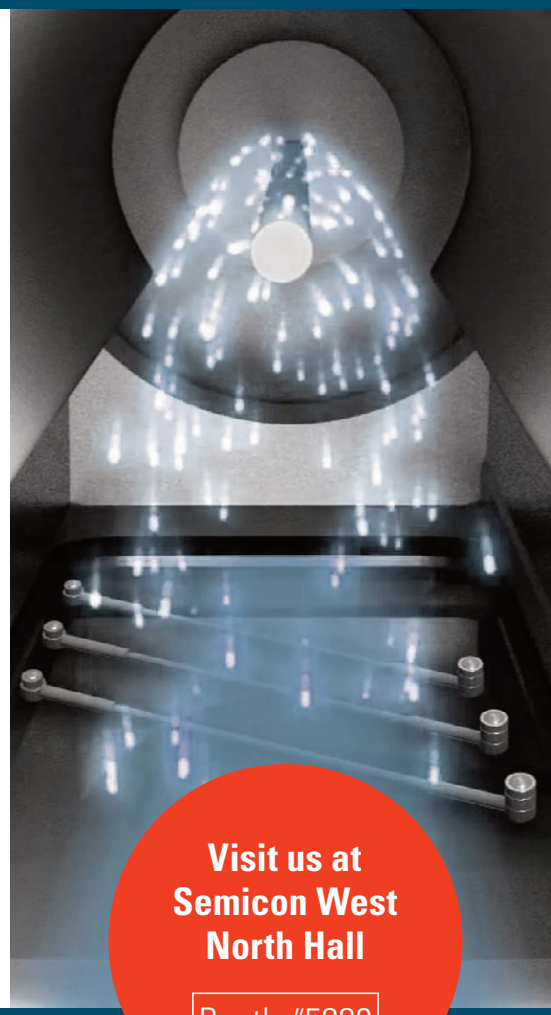

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Web Exclusives

When will self-driving cars become a reality?

Self-driving cars have been all the rage in both the trade and popular press in recent years. I prefer the term "autonomous vehicles," which more broadly captures the possibilities, encompassing not only small passenger vehicles but mass transit and industrial vehicles as well. Depending on who's talking, we will all be riding in fully autonomous vehicles in five to 25 years.

https://bit.ly/2JlYvC0

Insights from the Leading Edge: TSMC and Samsung flexing their muscle at ECTC

This ECTC saw TSMC and Samsung, usually minimal contributions or totally quiet participants, flexing their technical muscle and saying "see what we can do".

https://bit.ly/2lCFp66

SEMICON West preview: Exponential growth in data volumes drives change in system architecture

With artificial intelligence (AI) rapidly evolving, look for applications like voice recognition and image recognition to get more efficient, more affordable, and far more common in a variety of products over the next few years. This growth in applications will drive demand for new architectures that deliver the higher performance and lower power consumption required for widespread AI adoption.

https://bit.ly/2KfGsYh

Cautious optimism

Despite recent softening, global economic growth will remain robust at 3.1 percent in 2018 before slowing gradually over the next two years, as advanced-economy growth decelerates and the recovery in major commodity-exporting emerging market and developing economies levels off.

https://bit.ly/2lAmPoc

n&b news and blogs

Insights from the Leading Edge: Broadcom looks to advanced packaging

Boon Chye Ooi , Sr VP of Operations for Broadcom spoke at the IEEE ECTC luncheon addressing "Packaging advancements to enable artificial intelligence (AI), autonomous cars and wearables in the near future: cost and implications to supply chains."

https://bit.ly/2KjTqUU

China's semi capex forecast to be larger than Europe and Japan combined in 2018

Chinese semi firms to spend $11.0 billion in capex this year, up from only $2.2 billion in 2015.

https://bit.ly/2yOrK5e

SIA releases statement on Trump Administration tariff announcement

The Semiconductor Industry Association released the following statement regarding the Trump Administration's announcement on tariffs on products imported from China.

https://bit.ly/2Ke2WJr

North American semiconductor equipment industry posts May 2018 billings

"May 2018 monthly global billings of North American equipment manufacturers exceeded last month's level to set yet another record," said Ajit Manocha, president and CEO of SEMI. "Demand for semiconductor equipment remains strong on the back of smart, data-centric applications such as artificial intelligence (AI), Internet of Things (IoT), big data, and edge computing."

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worldnews

ASIA - **TowerJazz** announced a ramp for its radio frequency silicon-on-insulator (RF SOI) 65nm process in its 300mm Uozu, Japan fab.

USA - **Entegris** announced that it acquired Flex Concepts, Inc., a technology company focused on bioprocessing single-use bags, and fluid transfer solutions for the life sciences industry.

USA - **FormFactor** announced a collaboration with Keysight Technologies and GLOBALFOUNDRIES.

EUROPE - **Leti** demonstrated a new waveform for 5G low-power wide-area Internet of Things networks.

USA - **AMD** announced awards for key suppliers that contributed to the successful launch of 10 new high-performance computing and graphics product families in 2017.

USA - **The Linde Group** announced investments in the expansion of existing products while adding new products with improved purity to meet the growing needs of sub-10nm semiconductor factories and advanced flat panel manufacturers.

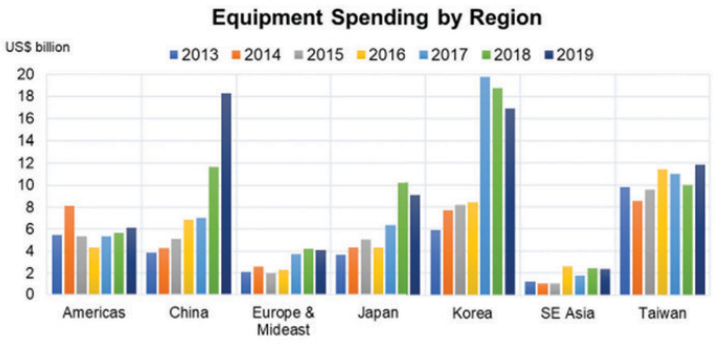
EUROPE - **imec** presented a process flow for a complementary FET (CFET) device for nodes beyond N3.

USA - **ON Semiconductor** expanded manufacturing operations in Mountain Top, Pennsylvania.

USA - **3D-Micromac** introduced a selective laser annealing system for semiconductor and MEMS manufacturing.

Semiconductor equipment record spending streak to continue through 2019

The semiconductor industry is nearing a third consecutive year of record equipment spending with projected growth of 14 percent (YOY) in 2018 and 9 percent in 2019, a mark that would extend the streak to a historic fourth consecutive growth year, according to the latest update of the World Fab Forecast report published by SEMI. Over the semiconductor industry's 71-year history, only once before – in the mid 1990s – has the industry logged four consecutive years of equipment spending growth.



Source: World Fab Forecast reports (May 2018), SEMI

Korea and China are leading the growth, with Samsung dominating global spending and ascendant China on a fast, steep rise, surging ahead of all other markets. See Figure 1.

While Samsung is expected to reduce equipment investments in 2018, the company still accounts for a dominant 70 percent of all investment in Korea. At the same time, SK Hynix is increasing its equipment spending in Korea.

China's equipment spending is forecast to increase 65 percent in 2018 and 57 percent in 2019. Notably, 58 percent of investments in China in 2018 and 56 percent in 2019 stem from companies with headquarters in other regions such as Intel, SK Hynix, TSMC, Samsung, and GLOBALFOUNDRIES. Domestic, Chinese-owned companies – backed by large government initiatives – are building a considerable number of new fabs that will start equipping in 2018. The companies are expected to double their equipment investments in 2018 and again in 2019.

Other regions are also ramping up investments. Japan is increasing equipment spending by 60 percent in 2018, with the largest increases by Toshiba, Sony, Renesas and Micron.

The Europe and Mideastern region will boost investments by 12 percent in 2018, with Intel, GLOBALFOUNDRIES, Infineon and STMicroelectronics the largest contributors.

Southeast Asia will boost investments by more than 30 percent in 2018, although total spending is proportionately smaller than in other regions owing to its size. The main contributors are Micron, Infineon and GLOBALFOUNDRIES, though companies including OSRAM and ams are also increasing investments.

The SEMI World Fab Forecast, which also includes information on other companies, covers data and predictions through the end of 2019, including milestones, detailed investments by quarter, product types, technology nodes and capacities down to fab and project level.

Learn more about the SEMI fab databases at: www.semi.org/en/MarketInfo/FabDatabase and www.youtube.com/user/SEMImktstats.

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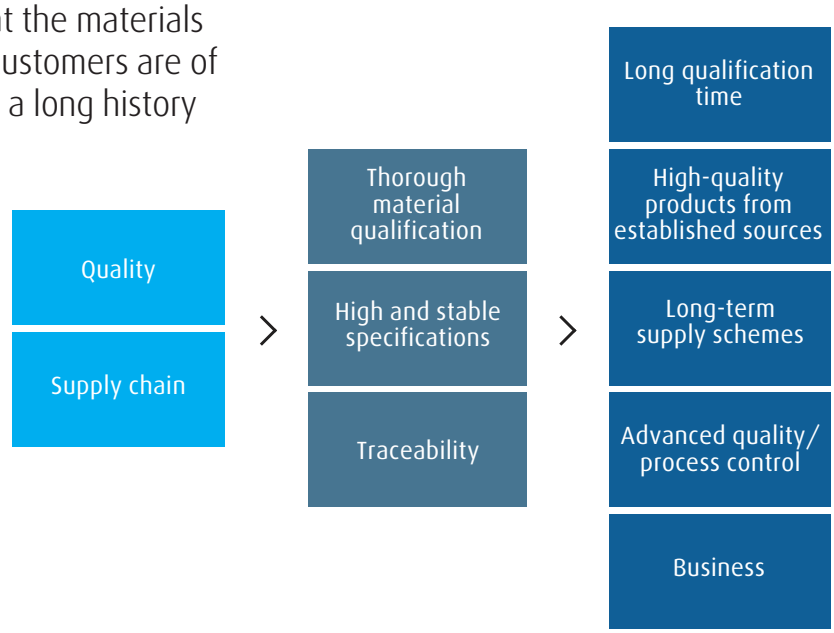

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Applied Materials breakthrough accelerates chip performance in the big data and AI era

Applied Materials, Inc. announced a breakthrough in materials engineering that accelerates chip performance in the big data and AI era.

In the past, classic Moore's Law scaling of a small number of easy-to-integrate materials simultaneously improved chip performance, power and area/cost (PPAC). Today, materials such as tungsten and copper are no longer scalable beyond the 10nm foundry node because their electrical performance has reached physical limits for transistor contacts and local interconnects. This has created a major bottleneck in achieving the full performance potential of FinFET transistors. Cobalt removes this bottleneck but also requires a change in process system strategy. As the industry scales structures to extreme dimensions, the materials behave differently and must be systematically engineered at the atomic scale, often under vacuum.

To enable the use of cobalt as a new conducting material in the transistor contact and interconnect, Applied has combined several materials engineering steps – pre-clean, PVD, ALD and CVD – on the Endura® platform. Moreover, Applied has defined an integrated cobalt suite that includes anneal on the Producer® platform, planarization on the Reflexion® LK Prime CMP platform and e-beam inspection on the PROVision™ platform. Customers can use this proven, Integrated Materials Solution to speed time-to-market and increase chip performance at the 7nm foundry node and beyond.

"Five years ago, Applied anticipated an inflection in the transistor contact and interconnect, and we began developing an alternative materials solution that could take us beyond the 10nm node," said Dr. Prabu Raja, senior vice president of Applied's Semiconductor Products Group. "Applied brought together its experts in chemistry, physics, engineering and data science to explore the broad portfolio of Applied's technologies and create a breakthrough Integrated Materials Solution for the industry. As we enter the big data and AI era, there will be more of these inflections, and we are excited to be having earlier and deeper collaborations with our customers to accelerate their roadmaps and enable devices we never dreamed possible."

While challenging to integrate, cobalt brings significant benefits to chips and chip making: lower resistance and variability at small dimensions; improved gapfill at very fine dimensions; and improved reliability. Applied's integrated cobalt suite is now shipping to foundry/logic customers worldwide.

Applied Materials, Inc. is a leader in materials engineering solutions used to produce virtually every new chip and advanced display in the world.

The memory market will grow 40% to US$177 billion in 2018

The semiconductor industry posted record results in 2017, with revenue exceeding US$400 billion. Overall demand for semiconductor devices was robust throughout the year, driven by the growing adoption of electronics components across all applications, with particular strength in the mobile and data center markets. Semiconductor growth in 2017 was led by the memory segment, with impressive revenue reaching US$126 billion. It represents an increase of over 60% year-over-year. Yole Développement (Yole) Memory Team forecasts the memory market to reach US$177 billion in 2018, with 40% growth.

Under this dynamic ecosystem, Yole and its partners System Plus Consulting and Knowmade, all parts of Yole Group of Companies, deeply scan the memory area. They propose today valuable memory services to deliver world class research, data and insight. Their aim is to ensure its clients are well-versed in all aspects of this competitive industry. Yole Group of Companies leverage decades of industry experience and expertise while partnering with its clients to make sure they are consistently well-informed on this pushy market.

Today two memory research services, DRAM Service and NAND Service have been developed by Yole Group of Companies. Full description of both services are available in a new dedicated Memory section on i-micronews.com. In addition, a selection of technology & market news are daily selected by Yole's memory team and posted in this section.

Make sure to collect deep insights and significant analyses from leading industry experts, combining over 50-year experience in memory and semiconductor-related fields.

Both DRAM and NAND markets were in a state of undersupply throughout the year, leading to rising prices and record revenue and profitability for the memory suppliers. Demand was very strong, led by mobile and data center / SSD and augmented by emerging growth drivers including AI , IoT and

automotive. Supply growth across both DRAM and NAND was constrained, due to a combination of limited wafer growth and technological challenges.

The current macro trends of AI and machine learning, mobility, and connectivity, are favorable to both the DRAM and NAND markets, and will likely result in Memory continuing to increase its share of the overall the semiconductor market.

"Understanding memory supply/demand dynamics and its relationship with pricing is vital to understanding the broader semiconductor market and all associated supply chains", asserts Emilie Jolivet, Division Director, Semiconductor & Software at Yole.

The DRAM market is constantly evolving and changing. Yole Group is announcing a 22% CAGR for bit demand over the next five years.

"New Chinese suppliers threaten the current market balance, and emerging memory technologies are poised to cannibalize huge chunks of DRAM demand while the demand drivers of the past, including PCs and smartphones lose steam and no longer push industry demand," comments Mike Howards, VP of DRAM & Memory research within the Semiconductor & Software division at Yole.

In parallel, NAND market is expected to set another revenue record in 2018, before a flattish 2019. Therefore it continues to expand, with several consecutive quarters of record revenue and profitability for suppliers.

NAND's competitive landscape remains incredibly dynamic. Samsung is prepping its first fab at its massive Pyeongtaek site; Intel is emerging as a stand-alone supplier with capacity in China; and the sale of Toshiba's memory business to a consortium led by Bain Capital is finally happening. Meanwhile, a new entrant looms on the horizon: China's Yangtze Memory Technologies Co. (YMTC), which threatens to disrupt the status-quo as well as multiple other Chinese projects.

"NAND demand remains robust, with strong growth for enterprise SSDs in data centers, increasing adoption of SSDs in laptop PCs, and continued content growth in smartphones and other mobile devices," asserts Walt Coon, VP of NAND and Memory Research at Yole."These segments will continue driving the bulk of NAND bit consumption, though several emerging trends are poised to augment future growth, including AI and VR adoption, automotive, and IoT," he adds.

Memory Research Service from Yole, provides all data related to NAND/DRAM revenue per quarter, NAND/DRAM shipments, pricing per NAND/DRAM type, near and long-term revenue, market share per quarter, CAPEX per company, and a market demand/supply forecast. It also includes a complete analysis and details on the demand side, with a deep dive into client and enterprise SSD, data centers, mobile,

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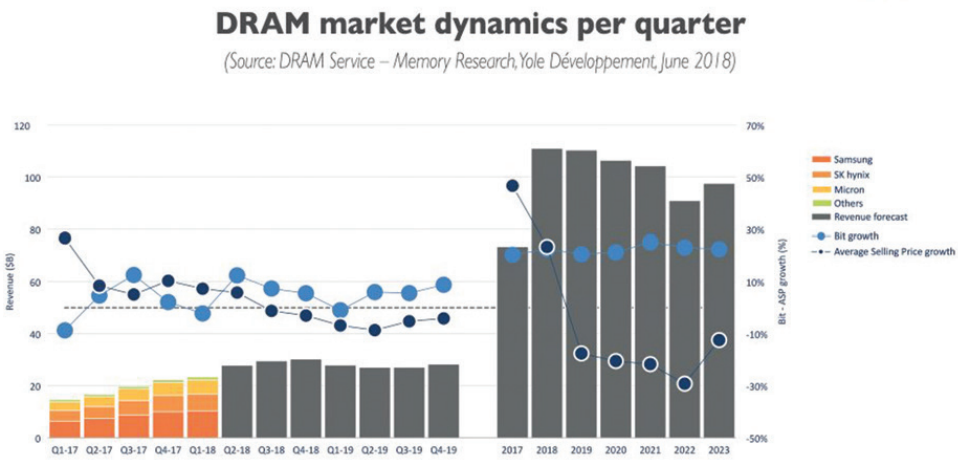
Continued from page 9

automotive, graphics, PC, and more. Each Memory Research Service is composed of both products, the Quarterly Market Monitor and the Monthly Pricing Monitor.

During the next few weeks, Yole's Memory Team will attend a selection of key trade shows and conferences to present the Memory Research Services. Make sure you will be there and ask for a meeting right now. Mike Howard and Walt Coon will for example be at SEMICON West mid-July and the Flash Memory Summit (Santa Clara, CA, North America – From August 6 to 9) in August.



Micron begins volume production of GDDR6 high performance memory

Micron Technology, Inc. (Nasdaq:MU) today announced volume production on its 8Gb GDDR6 memory. Built on experience and execution for several generations of GDDR memory, GDDR6 – Micron's fastest and most powerful graphics memory designed in Micron's Munich Development Center – is optimized for a variety of applications that require high performance memory, including artificial intelligence (AI), networking, automotive and graphics processing units (GPUs). Additionally, Micron has worked with core ecosystem partners to ramp GDDR6 documentation and interoperability, enabling faster time to market for designs.

"Micron is a pioneer in developing advanced high bandwidth memory solutions and continues that leadership with GDDR6. Micron demonstrated this leadership by recently achieving throughput up to 20 Gb/s on our GDDR6 solutions," said Andreas Schlapka, director, Compute Networking Business Unit, Micron. "In addition to performance increases, Micron has developed a deep partner ecosystem to enable rapid creation of GDDR6 designs, enabling faster time to market for customers looking to leverage this powerful new memory technology."

The need for high performance GDDR6 memory has grown as end-users demand advanced applications. GDDR6 enables advanced performance with lower power consumption in a number of segments including:

- **Artificial Intelligence** – Artificial intelligence, machine learning, deep learning are memory intensive applications that require more bandwidth from memory solutions. GDDR6 delivers the higher bandwidth required to accelerate AI in applications like computer vision, autonomous driving and the many other applications that require this higher bandwidth.
- **Graphics** – Enabling significant performance improvements for today's top GPUs, GDDR6 delivers enhanced graphic memory speeds to enable higher application bandwidth. Micron GDDR6 will be a core enabling technology of advanced GPU applications, including acceleration, 4K video and improved rendering, VR/AR and crypto mining applications.
- **Networking** – Advanced networking technologies require access to high speed/high bandwidth memory. GDDR6-powered smart Network Interface Cards (NIC) enable significant improvements in network bandwidth. Additionally, high bandwidth RAID controllers featuring GDDR6 memory deliver dramatic enhancements to data access and protection.
- **Automotive** – As auto manufacturers push for autonomous vehicles, high performance memory is required to process the vast amounts of real-time data required to make this technology a reality. Micron GDDR6 delivers 448 GB/s auto qualified memory solutions, that deliver more than double the bandwidth of LPDDR5 automotive memory solutions.

"As demand for advanced automotive applications such as ADAS and other autonomous driving solutions grows, the need for high bandwidth memory in automotive will grow as well. Advanced high bandwidth GDDR6 memory solutions are a key enabling technology for autonomous vehicles and will be an important tool for the automotive industry as they develop next generation transportation initiatives," said Kris Baxter, vice president, Marketing, Micron's Embedded Business Unit.

Targeting up to 64GB/s in one package, GDDR6 brings a significant improvement over the fastest available GDDR5. This unprecedented level of single-chip performance, using proven, industry-standard BGA packaging provides designers a powerful, cost-efficient and low-risk solution using the most scalable, high-speed discrete memory available to the market.

In order to deliver this leading edge high bandwidth memory technology to customers, Micron is working directly with ecosystem partners in order to enable learning on both pre-silicon verification as well as validation. Prior to mass production of GDDR6 memory, Micron shipped early validation silicon to our ecosystem partners to accelerate engineering efforts behind validating intellectual property and build robust models and toolsets in the ecosystem and deliver board layout validation. This ensures that engineers are able to implement GDDR6 in designs at a faster rate and bring bandwidth intensive applications to the marketplace. These ecosystem partners include Rambus and more.

"With nearly 30 years' experience in implementing designs for high-speed interfaces, Rambus is the first IP provider to launch a comprehensive GDDR6 PHY solution for next-generation AI, ADAS, networking and graphics applications and continues to be at the leading edge of implementing industry standards. We are proud to work with Micron and other ecosystem partners to help customers accelerate time to market for GDDR6 designs and deliver the most advanced solutions based on GDDR6 memory," said Frank Ferro, senior director of product marketing, Rambus.

Micron GDDR6 memory solutions will be on display in booth B-1340 at ISC 2018, June 24-28, in Frankfurt, Germany. For more information, visit www.micron.com.

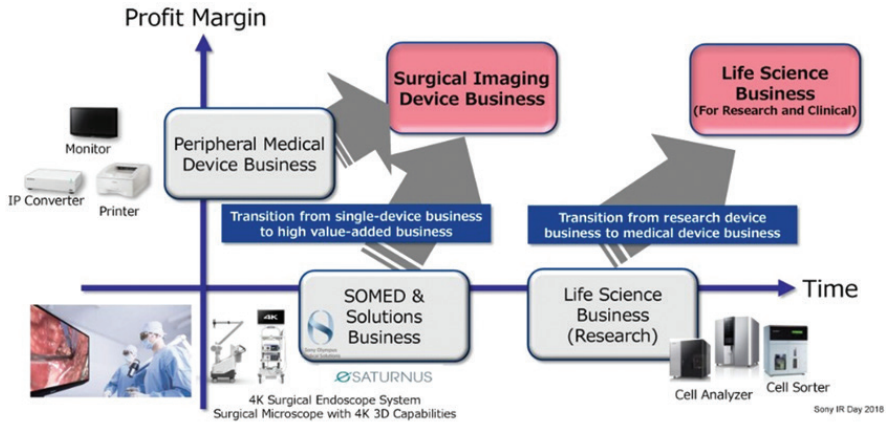
PHIL GARROU,
Contributing Editor

Sony refocuses on smartphones for 5G

Sony had some interesting things to say about their semiconductor and imaging technology businesses at their recent investor relations day May 22nd in Tokyo. As the industry moves forward to 5G, they seek to provide both hardware solutions and content services. Probably most startling to those in attendance appeared to be their announcement of a major focus on their mobile smartphone business.

Shigeki Ishizuka, Exec VP of Imaging products and mobile communications business discussed their theme of "light to display" as shown below. Imaging products and solutions is currently a 660B Yen business for Sony.

Their key applications for real time broadcasting include not only sporting events and concerts but also business to business communications, the education market which they call "active learning solutions" and medical room imaging solutions.



Their newly developed 3D surgical microscope allows doctors to operate without looking into the eye lenses of the microscope and the image can be shared real time with the whole operating team.

In the mobile communications segment Sony smartphone (Xperia) unit sales have decreasing since 2014. They will now focus on 5G phone solutions to revive their business position in that segment.

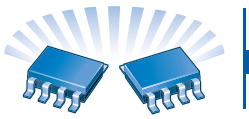
They will be seeking to advance smartphone competitiveness vs the industry leaders by bringing all their internal technology and their external partnerships to bear. They expressed a need to especially improve the design.

Post presentations, most of the questions focused on this announcement of increased focus on the mobile segment. When questioned about whether 5G mobile was an area that they HAD to be in, Sony answered that the technology hurdle for 5G is "quite high" including antenna technology ".... multi antenna array for beam focusing and switching has never happened before....high technology solutions are needed... its not like you can purchase an LSI chip and write some software and develop a solution...we will have to acquire these solutions and mature them." I assume this answer was meant to mean that this is not likely to be a commodity product and would require the technical expertise that only companies of Sony's stature could deliver.

When asked whether it was logical to focus on smartphones where Sony now has less than 1% market share they answered that "...with respect to smartphones the share is low-right- that's a pity...we don't have much product offering and product capability is very low...." The rest of the answer did not clearly explain how they intended to turn this around other than they would be focusing all their internal technical expertise on solving this problem.

It will be interesting to see if Sony can really become competitive with the likes of Samsung and Apple in the future 5G arena.

Packaging



Productivity for RF probe systems

PETE SINGER,
Editor-in-Chief

FormFactor, Inc. has extended its Contact Intelligence technology. With Contact Intelligence, FormFactor's advanced probe systems automatically and autonomously adapt in real time to changes in the testing environment, enabling customers to collect large amounts of RF data faster. As the race to bring 5G devices to market heats up, this addresses the need for higher productivity, to reduce time to market.

FormFactor is best known for it's probe card business, but with its acquisition of Cascade Microtech in 2016, it became more involved in the design and characterization side of chip-making, including RF and silicon photonic devices (probe cards are primarily used at the end of wafer manufacturing, testing the devices before they are packaged).

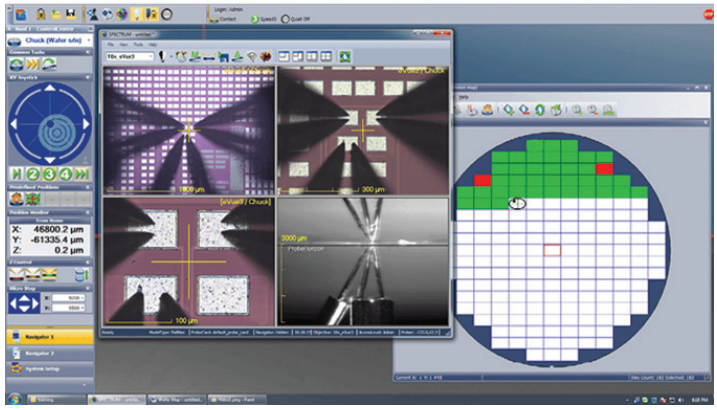
Mike Slessor, CEO of FormFactor, said with upcoming infrastructure changes -- such as 5G, more mobile communications and IoT -- RF is an important place to be. "The Cascade Microtech acquisition gave us an engineering systems business. These are pieces of customized capital equipment that help people very early on in their development and R&D -- even early pathfinding -- to figure out how their next device is going to perform, to characterize it and to improve its yield," he said. That systems business grew saw a double digit growth rate last year.

Slessor said the new Contact Intelligence technology is designed to help customers in the systems business get a lot of data faster. He said the push to improve yield, along with new materials and new devices, is driving a tremendous amount of data collection. "What Contact Intelligence really is positioned to do is to help people easily and efficiently collect that data. You can think of it as bringing almost production automation to the engineering lab. We're helping people do it autonomously over wide ranges of temperatures," he said. He said it enables engineering tools to be upgraded. Customers can "set it up, push a button and walk away for 48 hours, 96 hours even more and come back and have a hundreds of thousands of individual characterization data points."

New high frequency ICs, such as 5G (with multiple high frequency bands from sub-6 to more than 70 GHz) and automotive communication devices, need the highest quality process design kits (PDK's) to ensure working devices at first iteration. Traditional systems and methods require engineers to invest significant time for recalibration when the system invariably drifts, or to reposition probes with intentional changes in test temperatures.

At higher frequencies, calibrations and measurements are more sensitive to probe placement errors and there is more calibration drift, so recalibration is required more often. Over time and temperature, Contact Intelligence automatically makes these adjustments with no operator intervention, resulting in more devices tested in less time, for more accurate PDK's and faster time to market.

Four camera view



Slessor says the push to 5G brings many design and test challenges due to the significant increase in carrier frequencies – 10 times higher than 4G. "Although there are different bands and the carriers and the countries are still ironing out where they're going to operate, there are bands as high as 72 gigahertz," Slessor said. "Electrical signal propagation gets much, much more challenging as you go up in frequency. All kinds of new engineering and physics challenges emerge because you've got things that are radiating a good deal of power and there's a whole bunch of cross talk on the chip. There are all kinds of interesting phenomena that appear that make the designers and the test engineer's job much more difficult just because of these higher frequencies."

In an RF front end, instead of modems or radios communicating, a wide variety of a BAW and SAW filters are used to do the frequency band management and make sure that only the individual bands that are supposed to be used or being effectively used.

In addition to RF, Contact Intelligence is also designed for use in autonomous DC testing and for silicon phototonics. ◆

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By **YUKINOBU HAYASHI**, *Sr. Field Applications Engineer, CyberOptics*

CyberOptics' new WaferSense®, Auto Multi Sensor™ (AMS), combines an Auto Leveling Sensor (ALS), Auto Vibration Sensor (AVS), and a humidity sensor in a thin, light, all-in-one device. The ALS and AVS have well-established records of success, garnering praise from both users in the fab and equipment manufacturers for their ease-of-use, robust performance and convenient form factor. The addition of the humidity sensing (to tilt and vibration) in the AMS lets engineers also check for air leaks in the chamber and evaluate the efficiency of dry air purging procedures.

Parallelism and uniformity of tools and equipment in vacuum chambers and conventional open chambers are critical in reducing downtime, minimizing cost of consumable parts for maintenance, and maximizing yields. Poor leveling and lack of parallelism between a robot, pedestal, heater stage, and the wafer have potential to cause vibration during movements of parts such as lifter pins, clamp rings, and end-effectors. These causes can lead to shifting of the wafer position and degrading uniformity.

Yukinobu Hayashi, Senior Field Applications Engineer from CyberOptics, explains the application uses of the WaferSense® Auto Multi Sensor™ (AMS) for Leveling, Vibration, and Relative Humidity (RH) that facilitates maximizing uptime and optimizes maintenance. The combination of these attributes in a thin wafer shaped all-in-one wireless sensor, provides engineers the ability to acquire highly repeatable measurements while under a vacuum and without venting a chamber. The quantitative numeric results give engineers an objective basis for comparisons, and analysis that can be reproducible across multiple users over extended periods of time.

The AMS's ability to travel through the system just like a wafer, making measurements at all stages of the transport path, can make inspection and maintenance operations more efficient – saving significant time, expense, and improving yields.

IMAGE: AMS sensor

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Overlay performance of through silicon via last lithography for 3D packaging

WARREN W. FLACK, *Veeco Instruments, Plainview, NY and* **JOHN SLABBEKOORN**, *imec, Leuven, Belgium*

A lithographic method for TSV alignment to embedded targets was evaluated using in-line stepper self metrology, with TIS correction.

Demand for consumer product related devices including backside illuminated image sensors, interposers and 3D memory is driving advanced packaging using through silicon via (TSV) [1]. The various process flows for TSV processing (via first, via middle and via last) affect the relative levels of integration required at the foundry and OSAT manufacturing locations. Via last provides distinct advantages for process integration, including minimizing the impact on back end of line (BEOL) processing, and does not require a TSV reveal for the wafer thinning process. Scaling the diameter of the TSV significantly improves the system performance and cost. Current via last diameters are approximately 30µm with advanced TSV designs at 5 µm [2].

Lithography is one of the critical factors affecting overall device performance and yield for via last TSV fabrication [2]. One of the unique lithography requirements for via last patterning is the need for back-to-front side wafer alignment. With smaller TSV diameters, the back-to-front overlay becomes a critical parameter because via landing pads on the first level metal must be large enough to include both TSV critical dimension (CD) and overlay variations, as shown in **FIGURE 1**. Reducing the size of via landing pads provide significant advantages for device design and final chip size. This study evaluates 5µm TSVs with overlay performance of ≤ 750nm.

Alignment, illumination and metrology

Lithography was performed using an advanced packaging 1X stepper with a 0.16 numerical aperture (NA) Wynne Dyson lens. This stepper has a dual side alignment (DSA) system which uses infrared (IR) illumination to view metal targets through a thinned silicon wafer [3]. For the purposes of this study and its results, the wafer device side is referred to as the "front side" and the silicon side is referred to as the "back side." The side facing up on the lithography tool is the back side of the TSV wafer, as shown in **FIGURE 2**.

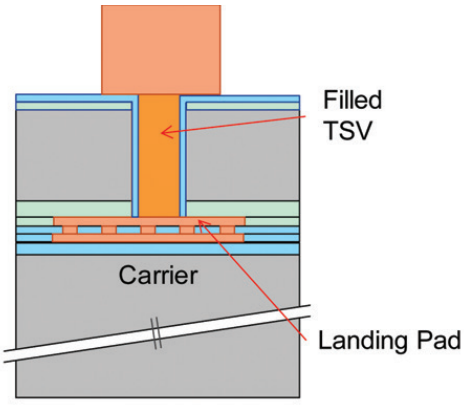

FIGURE 1. The landing pad on the first level metal must be large enough to include both the TSV CD and overlay variations.

The top IR illumination method for viewing embedded alignment targets, shown in Fig. 2, provides practical advantages for integration with stepper lithography. Since the illumination and imaging are directed from the top, this method does not interfere with the design of the wafer chuck, and does not constrain alignment target positioning on the wafer. The top IR alignment method illuminates the alignment target from the back side using an IR wavelength capable of transmitting through silicon (shown as light green in **FIGURE 2**) and the process films (shown in blue). In this configuration the target (shown in orange) needs to be made from an IR reflective material such as metal for optimal contrast. The alignment sequence requires that the wafer move in the Z axis in order to shift alignment focus from the wafer surface to the embedded target.

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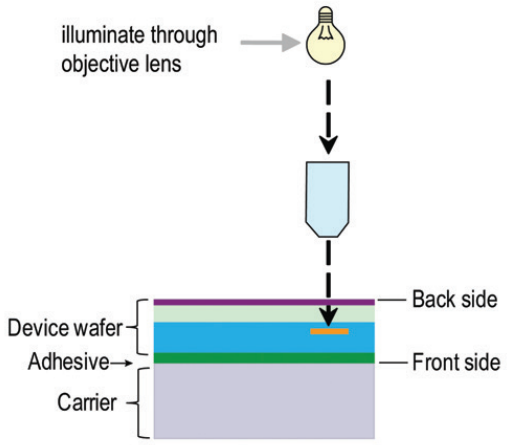

FIGURE 2. Off axis alignment configuration with IR illumination and imaging from above the wafer. This configuration is extremely flexible, providing access to the entire wafer for target alignment.

Back-to-front side registration was measured using a metrology package on the lithography tool which uses the DSA alignment system. This stepper self metrology package (DSA-SSM) includes routines to diagnose and compensate for measurement error from having features at different heights. For each measurement site the optical metrology system needs to move the focus in Z between the resist feature and the embedded feature. Therefore angular differences between the Z axis of motion, the optical axis of the alignment camera, and the wafer normal will contribute to measurement error for the tool [3]. The quality of the wafer stage motion is also very important because a significant pitch and roll signature would result in a location dependent error for embedded feature measurement, which would complicate the analysis.

If the measurement operation is repeatable and consistent across the wafer, then a constant error coming from the measurement tool, commonly referred to as tool induced shift (TIS), can be characterized using the method of TIS calibration, which incorporates measurements at 0 and 180 degree orientations. The TIS error—or calibration—is calculated by dividing the sum of offsets for the two orientations by two [4]. While the TIS calibration is effective for many types of measurements for planar metrology, for embedded feature metrology, the quality of measurement and calibration also depend on the quality and repeatability of wafer positioning, including tilt. In previous studies, the registration data obtained from the current method were self consistent and proved to be an effective inspection method [3, 5]. However given the dependencies affecting TIS calibration for embedded feature metrology, it is desirable to confirm the registration result using an alternate metrology method [5]. In order to independently verify the DSA-SSM, overlay data dedicated electrical structures were designed and placed on the test chip.

Electrical verification of TSV alignment is performed after complete processing of the test chip and relies on the landing position of a TSV on a fork-to-fork test structure in the embedded metal 1 (damascene metal). When the TSV processing is complete the copper filled TSV will make contact with metal 1. The TSV creates a short between the two sets of metal forks, allowing measurement of two resistance values which can be translated into edge measurements. For the case of ideal TSV alignment, the two resistances are equal. The measurement resolution of the electrical structure is limited by the pitch of the fork branches. In this study resolution is enhanced by creating structures with four different fork pitches. A similar fork-to-fork structure rotated 90 degrees is used for the Y alignment. Using this approach both overlay error and size of the TSV in both X and Y can be electrically determined [6].

Experimental methods

This study scrutinizes image placement performance by examining DSA optical metrology repeatability after TSV lithography, and then comparing this optical registration data with final electrical registration data.

The TSV-last process begins with a 300mm device wafer with metal 1, temporarily bonded to a carrier for mechanical support as shown in **FIGURE 3**. The back side of the silicon device wafer (light green) is thinned by grinding and then polished smooth by chemical mechanical planarization (CMP). The TSV is imaged in photoresist (red) and etched through the thinned silicon layer. **FIGURE 3** depicts the complete process flow including the TSV, STI and PMD etch, TSV fill, redistribution layer (RDL) and de-bonding from carrier. The aligned TSV structure must land completely on the metal 1 pad (dark blue).

TSV lithography is done with a stepper equipped with DSA. The photoresist is a gh-line novolac based positive-tone material requiring 1250mJ/cm2 exposure dose with a thickness of 7.5µm [5]. The TSV diameter is 5µm, and the silicon thickness is 50µm. TSV etching of the silicon

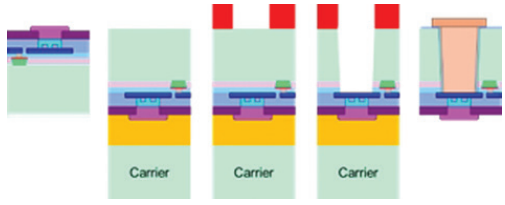

FIGURE 3. Representation of complete TSV-last process. From left to right: 1) Completed front-end wafer, 2) Temporary bonding of wafer and backside thinning, 3) TSV-last lithography, 4) TSV etch, 5) TSV filling, RDL and de-bonding from carrier.

is performed by Bosch etching [7]. Tight control of lithography and TSV etching is required to insure that vias land completely on metal 1 pads, as shown in **FIGURE 1**.

Acceptable features for DSA-SSM metrology need to fit the via process requirements for integration. Since the TSV etch process is very sensitive to pattern size and density, the TSV layer is restricted to one size of via, and the DSA-SSM measurement structure is constructed using this shape. The design of the DSA-SSM measurement structure uses a cluster of 5µm vias with unique grouping and clocked rotation to avoid confusion with adjacent TSV device patterns during alignment.

FIGURE 4 shows two different focus offsets of DSA camera images of the overlay structure. For this structure, the reference metal 1 feature (outlined by the blue ring) and the resist pattern feature (outlined by the red ring) are not in the same focal plane. For a silicon thickness of 50µm, focusing on one feature will render the other feature out of focus, requiring each feature to have its own focus offset, which is specified in the metrology measurement recipe.

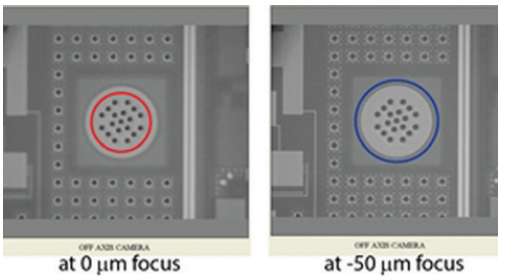

FIGURE 4. The left-hand image shows the resist target in focus (outlined in red ring). These are on the top surface (focus at 0 µm). The right-hand image shows the circle of metal 1 in focus at -50 µm (outlined by blue ring). The height difference between the two features is larger than the focal depth of the alignment camera so one of the two is always out of focus.

Optical registration process control

This study leveraged a sampling plan of 23 lithography fields with 5 measurements per field, resulting in a total of 115 measurements per wafer. Since the full wafer layout contains 262 fields, this sampling plan provides a good statistical sample for monitoring linear grid and intrafield parameters.

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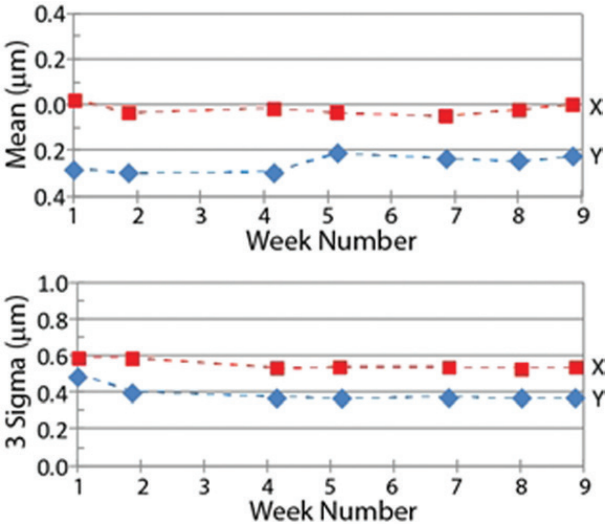

FIGURE 5. TSV registration trend charts for lot mean and lot 3σ using in-line optical metrology over nine weeks. The red squares are the X data and the blue diamonds are Y data.

In the initial run, the overlay settings were optimized using the DSA-SSM metrology feedback and then the parameters were fixed to investigate overlay stability over a nine-week period. Trend charts for mean and 3σ for seven TSV lots are shown in **FIGURE 5**. Each measurement lot consists of 8 wafers, with 115 measurements per wafer, and all data is corrected for TIS on a per lot basis using measurements of a single wafer at 0 and 180 degree orientations [3]. The lot 3σ is consistently less than 600nm over the nine-week period. There appears to be a consistent small Y mean error (blue diamond) that could be adjusted to improve subsequent overlay results. With a Y mean correction applied, the registration data shows mean plus 3σ ≤ 600nm.

Validating TSV alignment and in-line optical metrology

Two TSV last test chip wafers were completely processed to the stage that they can be electrically measured. TABLE 1 shows the registration numbers confirming a good match between the two metrology methods. It is important to note that an extra translation step is performed between the optical and the electrical measurement: the TSV etch.

Metrology type	Wafer D17				Wafer D10			
	Mean		1σ		Mean		1σ	
	X	Y	X	Y	X	Y	X	Y
Electrical	137	-51	186	121	90	-4	163	107
Optical	146	-41	132	78	140	-14	129	82
Difference	9	10	76	100	50	-10	63	68

TABLE 1. Statistical summary of electrical and optical registration data for wafer D17 and wafer D10, confirming a close match. All numbers are in units of nm.

In this analysis the TSV etch is assumed to be perfectly vertical. From the data we can conclude that the TSV etch is indeed vertical enough not to interfere with the overlay data. Otherwise this would show as translation or scaling effects between the two metrology methods.

Conclusions

The lithographic method for TSV alignment to embedded targets was evaluated using in-line stepper self metrology, with TIS correction. Registration data was collected over a nine-week period to characterize the stability of TSV alignment. With corrections applied, the registration data demonstrates mean plus 3σ ≤ 600nm. The in-line optical registration data was then correlated to detailed electrical measurements performed on the same wafers at the end of the process to provide independent assessment of the accuracy of the optical data. Good correlation between optical and electrical data confirms the accuracy of the in-line optical metrology method, and also confirms that the TSV etch through 50µm thick silicon is vertical.

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Waddle-room for black swans: EUV stochastics

ED KORCZYNSKI, *Sr. Technical Editor*

As the commercial IC fab industry begins ramping EUV lithography into HVM, engineers now must anticipate new stochastic failures.

Long-delayed and extremely complex, extreme ultra-violet (EUV) lithography technology is now being readied for the high-volume manufacturing (HVM) of commercial semiconductor integrated circuits (IC). The International Society for Optics and Photonics (SPIE) Advanced Lithography conferences held yearly in San Jose, California gather the world's top lithographers focused on patterning of ICs, and the 2018 gathering included several days of in-depth presentations on the progress of EUV sources, steppers, masks, and photoresists.

With a nod to Taleb's "black swan theory" stochastic defects in advanced lithography have been called the "black swans" of yield loss. They hide in the long-tail on the short side of the seven-sigma distribution of a billion contact-holes. They cause missing contacts and cannot be controlled with source-mask optimization (SMO). They breed in etch chambers.

Many yield losses in lithography are classified as "systematic" due to predicable interactions of photons and masks and photoresists, and modeling can show how to constrain them. White swan "random" defects—such as those caused by particles or molecular contaminants—can be penned up and controlled with proper materials-engineering and filtration of photoresist blends. In contrast, "stochastic" black swans appear due to atomic-scale inhomogeneities in resists and the wiggliness of atoms.

The wavelength of EUV is ~13.5nm, which the IC fab industry would like to use to pattern half-pitches (HP) in the range of 16-20nm in a single-exposure. At these dimensions, we find black swans hiding in lithography and in etch results.

An ongoing issue is lack of ability to model the multi-dimensional complexity of plasma etching multi-layer resist stacks. In Moshe Preil's 2016 SPIE keynote titled "Patterning Challenges in the sub-10 nm Era," he wrote:

It is certainly not surprising that etch simulation is not as predictive as lithography. The plasma environment is significantly more chaotic than the relatively well behaved world of photons and photosensitive molecules. Even the evolving need for stochastic simulation in the lithography domain is significantly simpler than the three dimensional controlled chaos of an etch chamber. The number of different chemical pathways available for reaction within an etcher can also present a daunting challenge. The etch process actually needs these multiple pathways to passivate sidewalls while etching vertically in order to carefully balance lateral vs. vertical etch rates and provide the desired material selectivity.

Etch faces additional challenges due to the resist pattern itself. Over the years, resist films have been reduced in thickness to such an extent that the resist itself is no longer adequate to act as the transfer mask for the entire etch process. Etch stacks are now a complex layer cake of optical materials (anti-reflection coatings) and multiple hard masks. While this simplifies the resist patterning process, it has shifted the burden to etch, making the stack more complex and difficult to model. Etch recipe optimization remains largely the domain of highly talented and diligent engineers whose work is often more an art than a science.

Today's Tri-Layer-Resist (TLR) stacks of photoresist over silicon-based hard-mask over carbon-based anti-reflective coating continue to evolve in complexity. Quadruple-Layer Resist (QLR) stacks add an adhesion/buffer layer of material between the photoresist and the hard-mask. Even without considering multi-patterning process integration, just transferring the pattern from a single-exposure now entails extreme etch complexity.

FIGURE 1 from "Line-edge roughness performance targets of EUV lithography" presented at 2017 SPIE by Brunner et al. (Proc. of SPIE Vol. 10143, 10143E-2) shows simulated stochastic variation in 18nm HP line grids. The authors explain why such black swan events cannot be ignored.

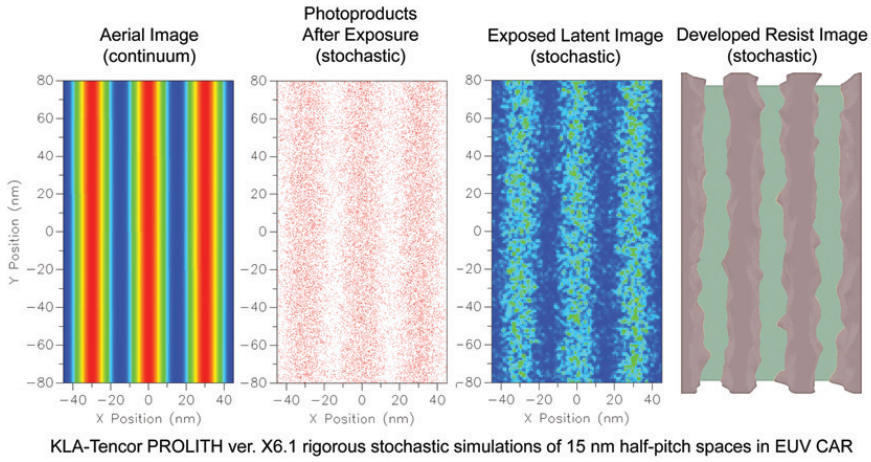

FIGURE 1. Stochastic image simulation in PROLITH™ software of a single exposure of EUV to form long trenches at 36nm pitch: (LEFT) aerial image first calculated as a smooth profile, (CENTER) stochastic calculation of photo-acid concentration before post-exposure bake (PEB) as "latent image", and (RIGHT) final calculated image after development, based on stochastic de-blocking reactions during PEB. (Source: Brunner et al., Proc. of SPIE Vol. 10143, 10143E-2, Image provided by KLA-Tencor.)

In "Stochastic effects in EUV lithography: random, local CD variability, and printing failures" by Peter De Bisschop of IMEC (J. Micro/Nanolith. MEMS MOEMS, Oct-Dec 2017, Vol. 16/4) data are shown in support of the need for new stochastic control metrics in addition to the established "process window" metrics. A dose experiment using a family of chemically-amplified resists (CAR) to produce 18nm HP line/space (L/S) grids showed that increasing dose in the range from 30 to 60 mJ/cm2 reduced line-width roughness (LWR) from 4.6 to 3.9nm, with no further improvement when increasing dose to 70 and 80 mJ/cm2. However, micro-bridging across spaces continued to drop by orders of magnitude over the entire range of doses, proving that stochastic defects are different "animals."

Such stochastic noise is present for all lithographic processes but is more worrisome for EUV lithography for several reasons:

- *fewer photons per unit dose, since each EUV photon carries 14X more energy than a 193nm photon,*
- *limited EUV power – only a fraction (~1%) of the source power at intermediate focus makes it to the wafer,*
- *only a fraction of EUV photons are actually absorbed within the resist, typically <20% for polymer materials, and*
- *smaller features as we progress to more advanced nodes, and so less area to collect EUV photons. Ideally, as the lithographic pixel size shrinks, the number of photons per pixel would stay the same.*

Stochastic phenomena – photon shot noise, resist molecular inhomogeneities, electron scattering events, etc. – now contribute to dimensional variation in EUV resist patterns at levels comparable to or greater than customary sources of variation, such as defocus. These stochastic effects help to limit k1 to higher values (worse resolution) than traditional optical lithography, and will counteract the benefits of high NA EUV optics. The quest to improve EUV lithography pattern quality will increasingly focus on overcoming stochastic barriers. Higher power EUV light sources are urgently needed as features shrink. Photoresist materials with higher EUV absorption will also help with stochastic issues. Alternative non-polymeric resist materials and post-develop smoothing processes may also play a future role.

In general, we can categorize sources of stochastic variation in advanced lithography as follows:

1. Number and spacial-distribution of photons absorbed (a.k.a. "shot noise"),
2. Quantum efficiency of photo-acid generation(PAG)/ diffusion along with quencher distribution,
3. Develop and rinse solution inhomogeneities,
4. Underlayer (hardmask/anti-reflective coating/ adhesion layer) optical and chemical interactions,
5. Smoothing techniques including deposition, etch, and infusion, and
6. Design layout and OPC and SMO.

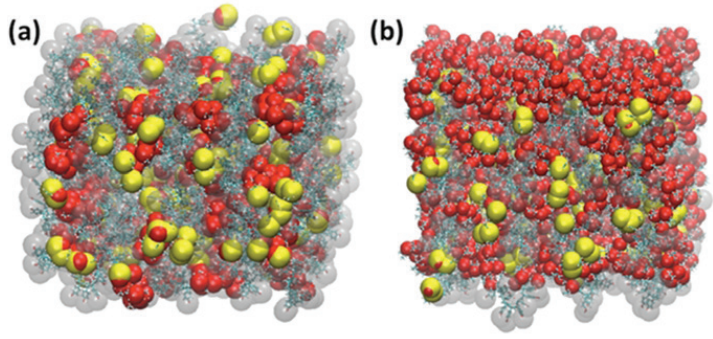

FIGURE 2. Molecular dynamics simulation of nano-scale domain separation within 8nm edge-length cubes of CAR composed of phenol groups (grey), TBA (red), and TPS (yellow) for (a) phenol-rich blend, and (b) TBA-rich blend. (Source: Wu et al., Proc. of SPIE Vol. 10586, 10586-10)

While we cannot eliminate stochastics by design, we can start to design around them using sophisticated process simulation models. At 2018 SPIE, Ping-Jui Wu et al. from National Taiwan University and TSMC used sophisticated molecular dynamics simulations to model "Nanoscale inhomogeneity and photoacid generation dynamics in extreme ultraviolet resist materials." **FIGURE 2** shows that ion-pair interactions in CAR create different nano-scale domains of poly(4-hydroxystyrene) (PHS) base polymers and triphenylsulfonium (TPS) based PAGs, depending upon the concentration of tert-butyl acrylate (TBA) copolymers in the blend.

16nm-HP EUVL Stochastics

PS-CAR "D"	LWR (nm)
EUV Photons	2.0
Acid Generation	1.2
Photo-Acid Generator	0.6
Quencher (base)	1.9
Protecting Groups	0.1
TOTAL	3.0

TABLE 1.

TABLE 1 shows modeled (Brainard, Trefonas & Gallatin, Proc. of SPIE Vol. 10583/10583-40) contributions to stochastic LWR from PS-CAR exposed with 0.33NA EUV to form 16nm HP L/S grids. For this PS-CAR blend the quencher variability contributes nearly as much LWR as the photon shot-noise, indicating room for improvement by fine-tuning the PS-CAR formulation.

One way to scare away black swans hiding in the resist is with bright light, as shown at 2018 SPIE by a team led by researchers from TEL in "EUV resist sensitization and roughness improvement by PSCAR™ with in-line UV flood exposure system." Photo-Sensitized (PS) CAR contains a precursor molecule that converts to PS when exposed to EUV light, in addition to PS-PAG and "photo decomposable base (quencher) which can be photosensitized" (PS-PDB) molecules. UV flood exposure after EUV pattern exposure but before development generates extra acid, allowing for higher quencher loading, such that higher image contrast with reduced LWR can be obtained. By increasing the concentrations of PAG and quencher in the resist blend there is a reduction in the stochastic at any target dose.

DUV Ducks: ArFi multi-patterning

As shown by Nikon Precision at the company's 2018 workshop in San Jose pre-SPIE, deep ultra-violet (DUV) steppers using 248nm KrF or 193 ArF sources continue to improve in IC fabrication capability. ASML also continues to improve its DUV steppers, including integrating the advanced metrology technology acquired from Hermes Microvision as part of the company's Holistic Lithography offering.

"The Challenge of Multi-Patterning Lithography for Contact Layer in 7nm and Beyond" by Wan-Hsiang Liang et al. of GLOBALFOUNDRIES at 2018 SPIE showed how multiple ArF-immersion (ArFi) exposures can replace one EUV step. They characterized the process window (PW) for patterning as limited by two types of defects: 1) single-layer bridging or missing contacts driven by lithography, and 2) multi-layer bridging or unlanded contacts or extra patterns driven by both lithography and hard-mask open (HMO) etch. They found that a patterning PW can only be obtained by co-optimizing lithography and etch.

DUV versus EUV cost estimates

The target metal HP for IMEC node 7nm (iN7) on-chip IC interconnects is 16nm, dropping to 10nm for the next iN5. A single-exposure of 0.33NA EUV can create the former half-pitch, but 10nm will require double-exposure of EUV.

The capital expenditure (CapEx) for 8 EUV or 16 ArFi steppers is ~US$1B. We know that EUV could improve fab yields, but we also know that black swans will cause new yield losses. The least risk for first use of EUV is for blocks/cuts to ArFi SAQP lines, so that multi-color ArFi masks could be substituted in an EUV yield-loss emergency without having to change the design.

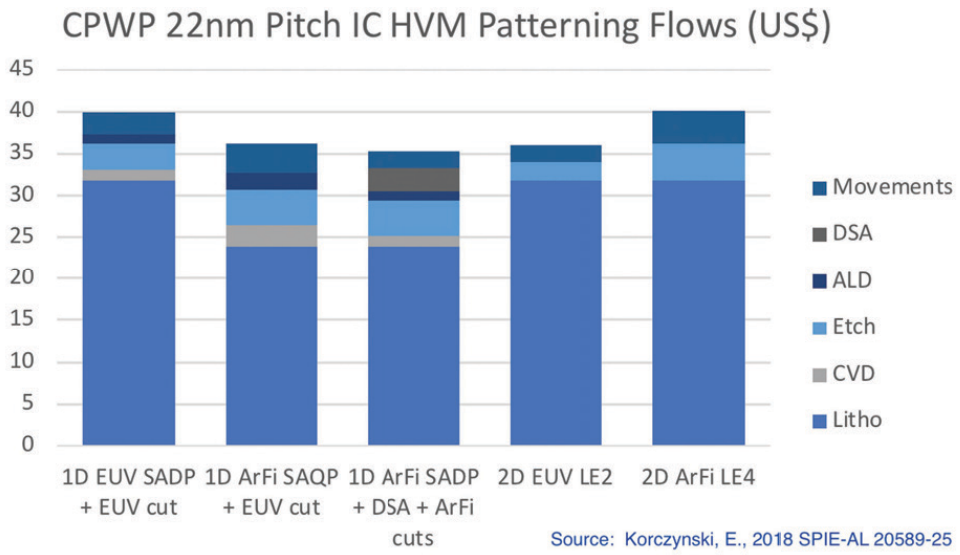

FIGURE 3. Cost Per Wafer Pass (CPWP)—with all yield losses including those from stochastics set to zero—modeled for different process flows to achieve 22nm pitch patterns, showing that flows using EUV could reduce HVM costs if yields can be managed. (Source: Korczynski, Proc. of SPIE Vol. 10589, 10589-25)

In my ongoing role as an analyst with TECHCET, at 2018 SPIE I presented a poster on "Cost modeling 22nm pitch patterning approaches" in HVM using either EUV or ArFi DUV steppers in complex multi-patterning process flows. In this model, all yield losses including those from stochastic black swans are assumed as zero to create a Cost Per Wafer Pass (CPWP) metric. Real Cost of Ownership (CoO) calculations can start with these relative CPWP numbers and then factor in systematic yield losses dependent upon design, as well as random yield losses dependent upon particles and wafer-breakage. CPWP includes only fab costs, not including EDA nor masks nor final test.

FIGURE 3 shows that EUV-based process flows could save money over strict use of ArFi in multi-patterning, assuming 1 EUV exposure can replace 3 ArFi exposures with similar yield. EDA for EUV should cost less than doing multi-color ArFi layouts, and design:process-induced systematic yield losses should be reduced. By reducing the number of deposition and etch steps needed in the full flow, use of EUV should significantly reduce the turn-around-time (TAT) through the fab. GLOBALFOUNDRIES' Gary Patton has said that such TAT savings for advanced logic chips could be a month or more.

EUV resist materials have additional stochastic constraints compared to ArFi resists, and as more highly engineered materials are expected to cost more. Nonetheless, the cost of stepper CapEx depreciation per wafer is ~10x the cost of all lithography materials for both ArFi and EUV in this model. More details of the CPWP model including materials assumptions will be presented at the 2018 Critical Materials Council (CMC) Conference, April 26-27 in Chandler, Arizona [*DISCLOSURE: Ed Korczynski is co-chair of this public conference*].

Conclusions

As the commercial IC fab industry begins ramping EUV lithography into HVM, engineers now must anticipate new stochastic failures. Perfect dose and focus cannot prevent them. A new constraint is added to the myriad challenges of engineering photoresist blends.

At the level of atoms we find plenty of kinetic energy to make things wiggle…or waddle. Waddling black swans have always been with us, but we used to be able to ignore them. While we can control random white swans, these black swans cannot be controlled but we can give them room to waddle around. ◆

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Developing a resist specific to EUV

DAVID URE, **ALEXANDRA MCCLELLAND** *and* **ALEX ROBINSON**, *Irresistible Materials, Wellesley, MA and Birmingham, U.K.*

Multi-Trigger chemistry, which is designed specifically for EUV, creates a high-chemical gradient at pattern boundaries, significantly reducing blurring and improving line-edge roughness to reduce the RLS trade off.

The semiconductor industry has invested billions of dollars to develop extreme ultraviolet (EUV) lithography and high-volume deployment of the technology is imminent. However, EUV lithography is not yet a complete solution. Most notably, new photoresist materials that enable the full benefits of EUV have yet to be developed.

While incremental modifications of incumbent 'chemically amplified resists' will be used for the planned initial EUV introduction in 2019, there are presently no clear solutions that address the industry feature size targets, defectivity requirements, and sensitivity needs for 2020 and onwards. This is a significant concern and continues to cast a shadow over the industry's long anticipated switch to EUV lithography. Indeed, the lack of a suitable resist for EUV lithography is now one of the biggest problems faced by the semiconductor industry.

What makes a good resist?

The critical performance parameters for any successful resist are: 1) Resolution (R): How narrow the lines on a microchip are, 2) Line-edge roughness LER (L): How 'wobbly' the lines are; and 3) Sensitivity (S): How small a dose of radiation is required (how quickly the pattern can be formed). These performance metrics are known as the RLS targets, and they are set out in the ITRS. For a given material, these metrics have a conflicting relationship (one can only be improved at the cost of another): The 'RLS tradeoff'. For a given material, improving one or two of the metrics leads to a loss in the third. To improve the RLS tradeoff, it is necessary to move to a new RLS graph. This can only be done by changing the resist material as illustrated in **FIGURE 1**.

In addition to the primary RLS targets, there are a series of critical secondary peformance metrics a commercially successful resist system needs to address, including the ability to pattern with extraordinarily low level of defects, high durability in the post processing steps, ultra-low contamination levels and wide process latitude.

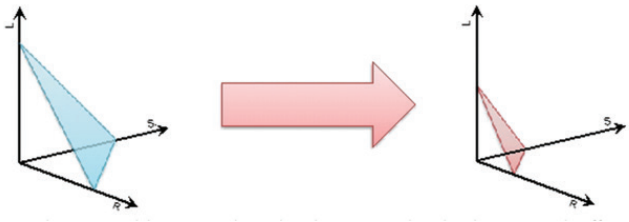

FIGURE 1. To improve the RLS tradeoff, it is necessary to move to a new RLS graph, which can only be done by changing the resist material.

The limitations with current state-of-art resist technology

Existing state-of-the-art photoresists are polymer-based platforms known as Chemically Amplified Resists (or CARs). The original CAR was based on a poly(hydroxystryene) chain with acid-labile tBOC protecting groups on the phenols, mixed with a photoacid generator. The photoacid released upon light exposure diffused through the polymer matrix catalytically removing the protecting groups, leading to a strong change in the solubility. While modern chemically amplified resists have increased in complexity, often using proprietary co-polymers with multiple functional units to address etch durability, adhesion and other properties, the core mechanisms of patterning have remained the same as the original CAR technology.

Such materials have demostrated significant design flexibility to address the evolving needs of the lithography industry. However, as feature sizes have continued to shrink, the diffuse nature of the acid – required for high senstitivity – has hampered resolution, and the acid quenchers, added to address this, have driven defects and roughness up. These limitations have risen to the fore as the industry prepares for the introduction of EUV lithography and the targeted feature sizes are increasingly incompatible with CAR technology.

Solving the EUV resist problem?

Given the limitations of polymer-platform photoresists originally developed for 193nm lithography, as the

industry prepares for EUV introduction, the approach to photoresist development is being challenged. Indeed, device manufacturers and scanner suppliers have urged the photoresist suppliers to consider novel approaches to design photoresist systems specifically to meet the needs of EUV lithography.

One of the new photoresist platforms that has risen to prominence has been given the name 'molecular resist' because it represents a departure from polymer-based photoresists to formulations based around 'small molecules.' Originally developed to reduce the chemical 'pixel' size of the resist, this platform has demonstrated promise in reducing line-edge roughness, but until recently has not fulfilled its early promise in EUV.

Another novel approach has been the development of metal-oxide resist platforms. These have demonstrated a compelling combination of high resolution, and low-line edge roughness, and sensitivities have improved recently. However, like other contenders, these materials currently demonstrate high defects and face a hurdle due to concerns over the use of metals in a cleanroom environment.

Another leading new 'EUV specific' resist system is being developed by Irresistible Materials Ltd (IM), a company headquartered in Birmingham, England. IM has developed a new approach to achieve high-resolution, high sensitivity, and a low LER resist called the Multi-Trigger Resist platform (MTR). MTRs comprise a small proprietary resin molecule; an MTR process compatible cross-linker; and (like a chemically amplified resist) a photo-acid generator (PAG). However, the novel Multi-Trigger chemistry creates a high-chemical gradient at pattern boundaries, significantly reducing blurring and improving line-edge roughness to reduce the RLS trade off (**FIGURE 2**).

In a Multi-Trigger material, resist exposure proceeds via a catalytic process in a similar manner to a chemically amplified resist. However, instead of a single photoacid causing a single deprotection event and then being regenerated, the Multi-Trigger resist uses multiple photoacids to activate multiple acid sensitive molecules, which then react with each other to cause a single resist event while also regenerating the photoacids. Importantly, it is only when two complimentary activated molecules react with each other that the resist is exposed – a single activated molecule, which is not near another will quench the acid, and remain unexposed.

In areas with a high number of activated photoacids (higher dose areas, for instance at the centre of a pattern feature), resist components are activated in close proximity and the multi-step resist exposure reaction proceeds, ending

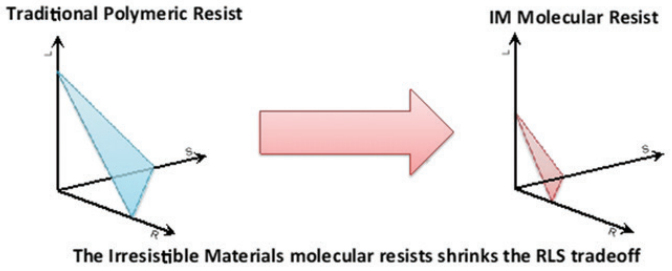

FIGURE 2. Multi-Trigger chemistry creates a high-chemical gradient at pattern boundaries, significantly reducing blurring and improving line-edge roughness to reduce the RLS trade off.

with photoacids regeneration and thus further reactions, ensuring high sensitivity. In areas with only a low number of activated photoacids (lower dose areas, for instance at the edge of a pattern feature), the activated resist components are too widely separated to react and the photoacids are thus removed, stopping the catalytic chain. The Multi-Trigger resist creates an increase in the chemical gradient at the edge of patterned features and reduces undesirable acid diffusion out of the patterned area. **FIGURE 3** and **4** illustrate how the Multi-Trigger approach departs from the traditional approach used in existing state-of-the-art resist systems (CARs).

How good is the MTR system and where is it in its development cycle?

The MTR system is presently in an advanced development phase. Results have already shown this system can match and exceed the performance capabilities of state-of-the-art CARs. Furthermore, the specific formulation of the MTR system can be tailored by changing the ratio of the components within the resist. To date, IM has demonstrated that the sensitivity of the resist can be varied from 12 mJ/cm2 to over 50 mJ/cm2, with the patterned resolution ranging from 20nm half pitch to under 16nm half pitch respectively, to meet varying lithographic requirements.

Some example data from the ASML NXE 3300 scanner at IMEC in Belgium is included for reference below. ASML's NXE platform is the industry's first production platform for extreme ultraviolet lithography (EUVL), using 13.5 nm EUV light, generated by a tin-based plasma source.

FIGURE 5 shows results for 20nm half-pitch lines patterned on a pitch of 40nm. At a dose of 44.5 mJ/cm2, the LER is 2.6nm. **FIGURE 6** shows 16nm half-pitch lines patterned on a pitch of 32nm. At a dose of 38.5 mJ/cm2, the LER is 3.7nm (unbiased values). These LER values compare very favorably with existing state-of-the-art CAR resists modified for EUV lithography. Importantly, the MTR technology is at the very beginning of its optimi-

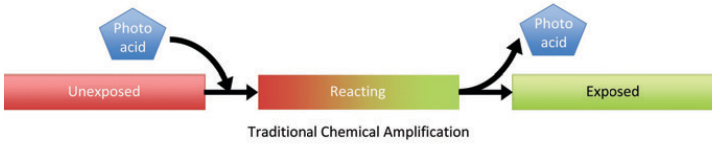

FIGURE 3. Schematic demonstrating traditional chemical amplification. A photoacid reacts with a photoresist molecule—to change its solubility or cause crosslinking—and is regenerated to allow further reactions.

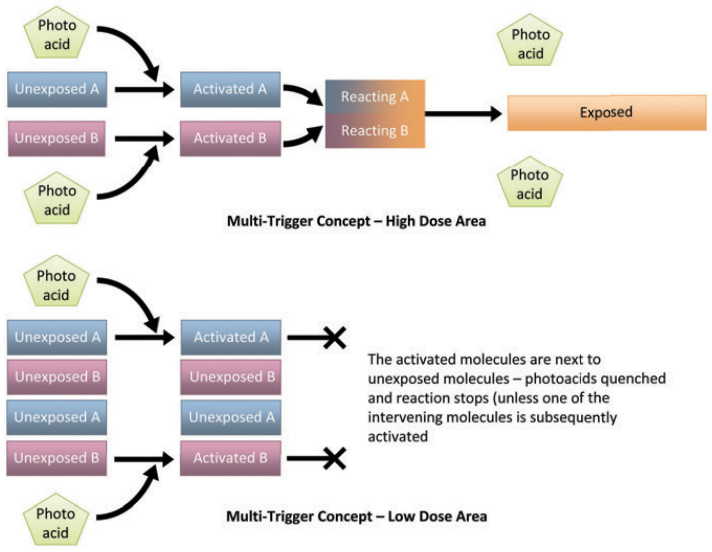

FIGURE 4. In a Multi-Trigger resist the photoacid activates a resist molecule but is not immediately regenerated. If two resist molecules are activated in close proximity the reaction proceeds as normal leading to a resist exposure event and photoacid regeneration (4a). If the activated molecules are further apart, the reaction stops, preventing further diffusion of the photoacids (4b).

zation cycle, with significant further performance enhancements expected as the technology matures. To this end, IM is in the process of scaling operations to accelerate the optimization of the MTR system in preparation for commercial launch.

The roadmap to commercial readiness

Prior to commercial integration into a Fab, it is also critical to address the 'secondary' performance metrics previously discussed. It is these tests that often prove a stumbling block to progressing from a promising new material. For an SME such as Irresistible Materials, passing this testing is a challenge as often new infrastructure and a specialist, custom tool set is required to pass stringent tests such as contamination. A resist that meets all lithography criteria could still fail to be adopted if, for example, the solubility of the components has not be synthesised with the required solubility in common fabrication solvents which will be present in the waste system.

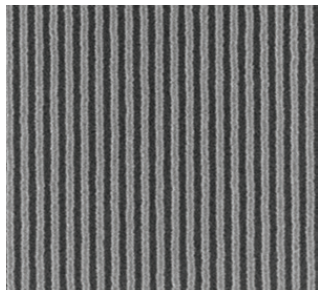

FIGURE 5. Dense line spaces patterned at pitch 40nm.

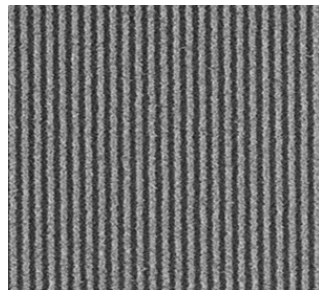

FIGURE 6. Dense line spaces patterned at pitch 32nm.

For IM's MTR, a precipitation test using waste drain solvents passed the precipitation test with no precipitate optically visible. These results indicate that the IM resist can be used within a fabrication facility with no precipitation issues. The resist also passes outgassing requirements so that it does not contaminate the lithography tool. Furthermore, because the resist is not metal based, there are no inherent track contamination issues. Metallic ion migration is a key concern for advanced device manufacturers and IM has implemented several protocols to address metal ion related concerns -- the current contaminant metal levels are below 15ppb for each individual metal and will reduce further as production system are optimized.

Another major step in the commercialization roadmap is the ability to produce material in a quality controlled, high-volume manufacturing process at commercially competitive costs. To address this requirement, IM has established a partnership with Nano-C for the high-volume supply of IM's proprietary resin molecule. Nano-C, Inc. is a leading supplier of specialist small molecules and has recently doubled the footprint at its Massachusetts site as preparations are made to scale production of the IM materials.

Looking towards the future

IM is targeting launch of its initial MTR products in 2020 (to address the industry N5 node),and is presently engaged in a variety of tests/trials with potential end-user and distribution partners as the resist system is optimized, scaled and readied for commercial release. However, IM also recognizes the potential of this resist system to go beyond N5 and has a clear pathway for addressing future industry nodes, to N3 and potentially beyond. Notable upgrade pathways from the gen 1 MTR include optimizing the metastable nature of the proton quenching, increasing opacity, reducing the number of components in the resist to reduce the impact of stochastics, and optimizing the ancillary process. ◁▶

Getting to 3nm: It really is scaling every which way!

DEBRA VOGLER, *SEMI, Milpitas, CA*

With chipmakers looking toward 5nm manufacturing, it's clear that traditional scaling is not dead but continuing in combination with other technologies. The industry sees scaling enabled by 3D architectures such as die stacking and the stacking of very small geometry wafers. Interconnect scaling also comes into play. This year's Scaling Technologies TechXPOT at SEMICON West (Scaling Every Which Way! – Thursday, July 12, 2:00PM-4:00PM) will provide an update on the evolution of scaling and describe how the various players (foundry, IDM, fabless, and application developers) are jockeying for innovation leadership. As a prelude to the event, SEMI asked speakers to provide insights on important scaling trends. For a full list of speakers and program agenda, visit http://www.semiconwest.org/programs-catalog/scaling-every-which-way.

Challenges for gate-all-around (GAA) and FinFET devices

Common performance boosters for gate-all-around (GAA) FETs and FinFETs include lower access resistance, lower parasitic capacitance, and stress. "However, one specific performance booster that only applies to GAA is the reduction of the spacing between the vertical wires or sheets," says Diederik Verkest, imec distinguished member of technical staff, Semiconductor Technology and Systems. "This reduces parasitic capacitance without affecting drive current and hence benefits both performance and power." He further notes that imec demonstrated the first stacked gate-all-around (GAA) devices in scaled nodes. "In fact, we are the only ones that published working circuits – ring oscillators in a scaled node using industry-standard processes – in our case replacement metal gate (RMG), and embedded in situ doped source/drain (S/D) epitaxy."

"There are two elements of the stacked GAA architecture that need to be addressed," says Verkest. "The first is that this architecture uses epitaxially-grown layers of Si and SiGe to define the device channel. The use of grown materials for the channel and the lattice mismatch between the two materials represent a departure from the traditional fabrication of CMOS devices, so the industry needs to develop and gain confidence in novel metrology that allows for good control of the layers and also proves their low defectivity." The second aspect is the three-dimensional nature of the GAA devices. "During the processing of these devices, we have 'non-line-of-sight' hidden features that are difficult to control and characterize and may also lead to new defect mechanisms that would impact yield, and possibly product reliability."

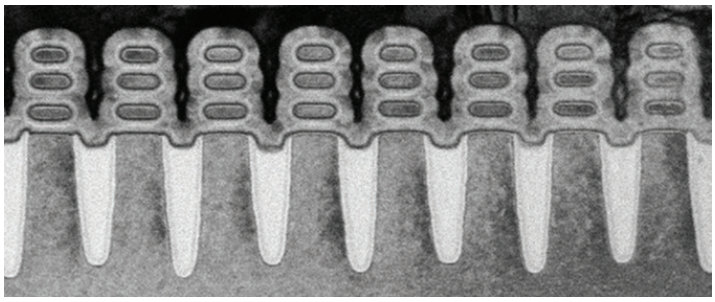

FIGURE 1. TEM cross section of stacked NanoSheet

Huiming Bu, director, Advanced Logic/Memory Research - Integration and Device, IBM Research, Semiconductor Group, says that naming of technology nodes has been used extensively for marketing strategies in "foundry land," but the designations have lost much of their meaning as technology scaling differentiators. "That said, when it comes to technology innovation and value proposition, IBM, in conjunction with Samsung and GLOBALFOUNDRIES, has developed the GAA NanoSheet transistor for 5nm to provide a full technology node scaling benefit in density, power and performance," says Bu (**FIGURE 1**). The key parameters for intrinsic device optimization when scaling to the 3nm node, explains Bu, are the NanoSheet width for better electrostatic characteristics, and the number of sheets for increased current density. Also necessary are strain engineering for carrier transport enhancement, and interconnect innovations for parasitic RC reduction. "Beyond that, the industry needs to look into something different, something more disruptive."

Materials challenges

Materials challenges are also a concern as the industry moves to 5nm and below. "We see increasing complexity in the material systems that are being used," explains Verkest. One example he cites in scaled FinFET or GAA

technologies is the use of two to three layers of different materials – typically metals such as TiN – to which small amounts of other elements are added to set device characteristics such as the threshold voltage. "At the same time, the requirements for the thickness of these materials, driven by gate dimensions for example, or the distance between the wires, are increasingly challenging." Other examples of materials challenges are the use of two to three different types of insulators in the middle-of-the-line, each with different etch contrasts. "We use novel materials such as carbon containing oxides or oxynitrides that have lower dielectric constants in order to boost the performance of circuits," he says, noting that the materials list "is quite long."

Several critical dimensions in transistors at advanced technology nodes have already reached a few monolayers of atoms, fueling expectations for innovation at the material level for transistor scaling, Bu notes. "The other argument is that there is a growing gap between computing demand and the slowdown of technology advancement driven by conventional scaling," says Bu. One trend that addresses this gap is integrating more computing functions that make the technology solution more modular, which naturally leads to the incorporation of more materials for more applications. Bu cautions, however, that introducing new materials in semiconductor technology has never been easy. "It takes many years of R&D to reach this implementation point, if it ever happens. So, do we need new materials when the industry moves to 5nm and 3nm? Yes, though I expect new material implementation to be a lot faster in interconnect and packaging at these nodes rather than intrinsic to the transistor."

Challenges in developing atomic-level processes

There will be challenges in developing atomic-level processes used in scaling, such as atomic layer depositions (ALD) and atomic layer etches, notes Verkest. "These classes of processes are both required to handle the scaled dimensions at the 5nm and 3nm nodes, and also the 3D nature of the scaled technologies – and here we are talking about logic and memories," Verkest says. "With respect to depositions, we would need to develop thermal ALD processes (not plasma-based) that enable accurate and conformal depositions in non-line-of-sight structures." Adhesion and wetting, smoothness, and throughput would also need to be addressed. "Longer term, these processes need to facilitate selectivity and self-alignment to address gap-fill challenges in highly scaled structures," he says. Other concerns he notes with respect to atomic layer etches are selectivity to various materials, and fidelity requirements that increase the requirements for metrology accuracy. "Throughput is also a concern."

Bu believes that a new device architecture beyond FinFET is required to provide a full technology node scaling benefit (i.e., density, power and performance) at 5nm and 3nm. "Beyond 3nm, we may need to continue the transistor scaling in the vertical direction and start to stack them together," Bu says. He also cites the need for parasitic R/C reduction in the interconnect to take advantage of the intrinsic transistor benefit at the circuit and chip levels. "We see a lot of opportunity in atomic-level processes, especially in atomic layer etch and selective material deposition, to address these challenges in the transistor and the interconnect." ◆

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The outlook for new metrology approaches

PAUL VAN DER HEIDE, *director of materials and components analysis, imec, Leuven, Belgium*

To keep up with Moore's law, the semiconductor industry continues to push the envelope in developing new device architectures containing novel materials. This in turn pushes the need for new solid-state analytical capabilities, whether for materials characterization or inline metrology. Aside from basic R&D, these capabilities are established at critical points of the semiconductor device manufacturing line, to measure, for example, the thickness and composition of a thin film, dopant profiles of transistor's source/drain regions, the nature of defects on a wafer's surface, etc. This approach is used to reduce "time to data". We cannot wait until the end of the manufacturing line to know if a device will be functional or not. Every process step costs money and a fully functional device can take months to fabricate. Recent advances in instrumentation and computational power have opened the door to many new, exciting analytical possibilities.

One example that comes to mind concerns the development of coherent sources. So far, coherent photon sources have been used for probing the atomic and electronic structure of materials, but only within large, dedicated synchrotron radiation facilities. Through recent developments, table top coherent photon sources have been introduced that could soon see demand in the semiconductor lab/fab environment.

The increased computational power now at our finger tips is also allowing us to make the most of these and other sources through imaging techniques such as ptychography. Ptychography allows for the complex patterns resulting from coherent electron or photon interaction with a sample to be processed into recognizable images to a resolution close to the sources wavelength without the requirement of lenses (lenses tend to introduce aberrations). Potential application areas extend from non-destructive imaging of surface and subsurface structures, to probing chemical reactions at sub femto-second timescales.

Detector developments are also benefiting many analytical techniques presently used. As an example, transmission electron microscopy (TEM) and scanning transmission electron microscopy (STEM) can now image, with atomic resolution, heavy as well as light elements. Combining this with increased computational power, allows for further development of imaging approaches such as tomography, holography, ptychography, differential phase contrast imaging, etc. All of which allow TEM/STEM to not only look at atoms in e.g. 2D materials such as MoS2 in far greater detail, but also opens the possibility to map electric fields and magnetic domains to unprecedented resolution.

The semiconductor industry is evolving at a very rapid pace. Since the beginning of the 21st century, we have seen numerous disruptive technologies emerge; technologies that need to serve in an increasingly fragmented applications space. It's no longer solely about 'the central processing unit (CPU)'. Other applications ranging from the internet of things, autonomous vehicles, wearable human-electronics interface, etc., are being pursued, each coming with unique requirements and analytical needs.

Looking ten to fifteen years ahead, we will witness a different landscape. Although I'm sure that existing techniques such as TEM/STEM will still be heavily used – probably more so than we realize now (we are already seeing TEM/STEM being extended into the fab). We will also see developments that will push the boundaries of what is possible. This would range from the increased use of hybrid metrology (combining results from multiple different analytical techniques and process steps) to the development of new innovative approaches.

To illustrate the latter, I take the example of secondary ion mass spectrometry (SIMS). With SIMS, an energetic ion beam is directed at the solid sample of interest, causing atoms in the near surface region to leave this surface. A small percentage of them are ionized, and pass through a mass spectrometer which separates the ions from one another according to their mass to charge ratio. When this is done in the dynamic-SIMS mode, a depth profile of the sample's composition can be derived. Today, with this technique, we can't focus the incoming energetic ion beam into a confined volume, i.e. onto a spot that approaches the size of a transistor. But at imec, novel concepts were introduced, resulting in what are called 1.5D SIMS and self-focusing SIMS (SF-SIMS). These approaches are based on the detection of constituents within repeatable array structures, giving averaged and statistically significant information. This way, the spatial resolution limit of SIMS was overcome.

And there are exciting developments occurring here at imec in other analytical fields such as atom probe tomography (APT), photoelectron spectroscopy (PES), Raman spectroscopy, Rutherford back scattering (RBS), scanning probe microscopy (SPM), etc. One important milestone has been the development of Fast Fourier Transform-SSRM (FFT-SSRM) at imec. This allows one to measure carrier distributions in FinFETs to unparalleled sensitivity.

Yet, probably the biggest challenge materials characterization and inline metrology face over the next ten to fifteen years will be how to keep costs down. Today, we make use of highly specialized techniques developed on mutually exclusive and costly platforms. But why not make use of micro-electro-mechanical systems (MEMS) that could simultaneously perform analysis in a highly parallel fashion, and perhaps even in situ? One can imagine scenarios in which an army of such units could scan an entire wafer in the fraction of the time it takes now, or alternatively, the incorporation of such units into wafer test structure regions. ◆

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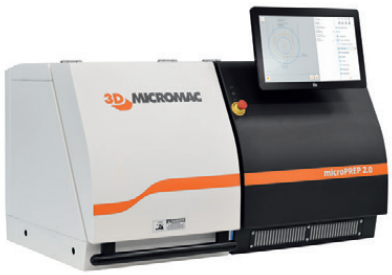

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