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JUNE 2018

Solid State TECHNOLOGY

Insights for Electronics Manufacturing

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Caption: Optimized fan-out lithography.
Source: Rudolph Technologies.

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Photonics integration coming

Increasingly, the ability to stay on the path defined my Moore's Law will depend on advanced packaging and heterogeneous integration, including photonics integration.

At The ConFab in May, Bill Bottoms, chair of the integrated photonics technical working group, and co-chair of the heterogeneous integration roadmap (HIR) spoke about the changing nature of the industry and specifically the needs of photonic integration.

Bottoms said the driving force behind photonics integration is pretty straightforward: "The technology we have today can't keep up with the expanding generation of transport and storage of data," he said. But doing so will be a challenge.

The integration of photonics, electronics and plasmonics at a system level is necessary. "These require heterogeneous integration by architecture, by device type, by materials and by manufacturing processes," Bottoms said. "We're changing the way we're doing things."

These kinds of changes are best thought of not as packaging but system level integration. "As we move the photons as close as to the transistors as possible, we're going to be faced with integrating everything on a simple substrate," he said.

There are a large number of devices that involve photons which share the common requirement of providing a photon path either into or out of the package or both. They include: Light emitting diodes (LEDs), laser diodes, plasmonic photon emitters, photonic Integrated circuits (PICs), MEMS optical switching devices, camera modules, optical modulators, active optical cables, E to O and O to E converters, optical sensors (photo diodes and other types), and WDM multiplexers and de-multiplexers. Many of these devices have unique thermal, electrical and mechanical characteristics that will require specialized materials and system integration (packaging) processes and equipment, Bottoms noted.

Of the biggest challenges might be thermal management: "We have things that make a lot of heat and things that can't have their temperature change by more than a degree without losing their functionality," Bottoms said.

The scope of the HIR Photonics Chapter includes defining difficult challenges and, where possible, potential solutions associated with: data systems and the global network, photonic components, integrating these components and subsystems into systems with the smallest size, lowest weight, smallest volume, lowest power and highest performance.

It will also address supply chain requirements, which may turn out to be the biggest challenge. "We will not beat the challenge of cost pressures unless we develop the supply chain that can justify high volume. It's the only way we know how to bring down costs," Bottoms said. Sounds like a great opportunity for today's equipment and materials suppliers to me!

—Pete Singer, Editor-in-Chief

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Web Exclusives

EUV lithography: Extending the patterning roadmap to 3nm

This year's Advanced Lithography TechXPOT at SEMICON West will explore the progress on extreme ultra-violet lithography (EUVL) and its economic viability for high-volume manufacturing (HVM), as well as other lithography solutions that can address the march to 5nm and onward to 3nm.

https://bit.ly/2JACUis

Economics of EUVL: Understanding commercial opportunities and financial impact

The technology of EUVL, coupled with its economic impact, are indeed complex and evolving. On the eve of EUVL's deployment in high-volume manufacturing, we need to understand both technology and economics. Moore's Law puts an additional time constrain on readiness for a manufacturing node, which a technology must meet. Ultimately it is the economics that will decide EUVL's long-term future, but it is very much coupled with technology and how it will evolve for future nodes. Here, I will describe these aspects briefly to give you an overview of what has been called an "epic challenge for advanced semiconductor manufacturing."

https://bit.ly/2M5T8yl

Insights from the Leading Edge: Sony refocuses on smartphones for 5G

Sony had some interesting things to say about their semiconductor and imaging technology businesses at their recent investor relations day May 22nd in Tokyo. As the industry moves forward to 5G, they seek to provide both hardware solutions and content services. Probably most startling to those in attendance appeared to be their announcement of a major focus on their mobile smartphone business.

https://bit.ly/2JnfHN3

n&b news and blogs

MEMS fabrication: Growth-enabler or industry roadblock?

The MEMS industry has huge growth potential. Will MEMS fabrication act as a bottleneck to continued expansion or a critical conduit to achieving that potential? Slow development cycles, multiple fabrication platforms and high cost for small R&D volumes are barriers to rapid development of new products. Understanding the special features of MEMS fabrication — with its many ecosystem options — will help your company to navigate successfully these challenges as you more quickly develop new and unique products.

https://bit.ly/2JyM66V

Automotive IC market on pace for third consecutive record growth year

Consumer demand and government mandates for electronic systems that improve vehicle performance, that add comfort and convenience, and that warn, detect, and take corrective measures to keep drivers safe and alert are being added to new cars each year. This system growth, along with rising prices for memory components within them, are expected to raise the automotive IC market 18.5% this year to a new record high of $32.3 billion, surpassing the previous record of $27.2 billion set last year.

https://bit.ly/2JmJQwg

Insights from the Leading Edge: Semiconductor activity in China

China is by far the largest consumer of semiconductors reportedly accounting for 45 percent of the worldwide demand for chips, used both in China and for exports. More than 90 percent of its consumption relies on imported ICs. At the end of 2016 IC Insights reported that China was responsible for ~ 11% of the worlds wafer capacity.

https://bit.ly/2JkJvho

worldnews

USA - **ROHM** and **GaN Systems** announced their collaboration in the GaN (gallium nitride) Power Semiconductor business.

ASIA - **Toshiba Memory Corporation** and **Synopsys** announced a collaboration to accelerate 3D flash memory verification.

USA - **SiTime Corporation** announced it has expanded its global footprint to support its rapid growth with the opening of a new Center of Excellence in Michigan.

EUROPE - **imec** presented 11 papers on advanced interconnects, ranging from extending Cu and Co damascene metallization, all the way to evaluating new alternatives such as Ru and graphene.

USA - **Micron Technology, Inc.** and **Intel Corporation** announced production and shipment of the industry's first 4bits/cell 3D NAND technology.

ASIA - **NVIDIA** and **Taiwan's Ministry of Science and Technology** announced an extensive collaboration that will advance Taiwan's artificial intelligence capabilities.

USA - **Microsemi Corporation** announced it will be expanding its Silicon Carbide (SiC) MOSFET and SiC diode product portfolios.

EUROPE - **STMicroelectronics** announced a new Executive Committee.

USA - **GLOBALFOUNDRIES** entered volume production of ultra high voltage process technology.

EUROPE - **EV Group** announced that it has received an order for its EVG120 automated resist processing system from VTT Technical Research Centre of Finland (VTT).

TI expands lead among top analog suppliers in 2017

The top 10 IC suppliers in the $54.5 billion analog market last year accounted for 59% of the category's worldwide sales in 2017, according to a recent monthly update to IC Insights' 2018 McClean Report. Collectively, the top 10 companies generated $32.3 billion in analog IC sales last year compared to $28.4 billion in 2016, which was a 14% increase and a gain of two percentage points in marketshare during 2017, said the 50-page April Update to The McClean Report. Eight of the top-10 suppliers exceeded the 10% growth rate of the total analog market in 2017, according to the update.

Leading Analog IC Suppliers ($M)

2017 Rank	Company	2016	2017	% Change	% Marketshare
1	Texas Instruments	8,536	9,900	16%	18%
2	Analog Devices*	3,790	4,310	14%	8%
3	Skyworks Solutions	3,205	3,710	16%	7%
4	Infineon	3,030	3,355	11%	6%
5	ST	2,519	2,930	16%	5%
6	NXP	2,430	2,415	-1%	4%
7	Maxim	1,900	2,025	7%	4%
8	ON Semi*	1,335	1,800	35%	3%
9	Microchip*	819	940	15%	2%
10	Renesas*	810	915	13%	2%

*Includes sales from acquired companies in 2016 and 2017.

Source: IC Insights, company reports

With analog sales of $9.9 billion and 18% marketshare, Texas Instruments was again the leading supplier of analog integrated circuits in 2017. In 2016, TI's marketshare was 17% in analog ICs. The company's analog sales increased by about $1.4 billion last year—rising 16%—compared to 2016 and were more than twice that of second-ranked Analog Devices (ADI). TI's 2017 analog revenue represented 76% of its $13.0 billion in total IC sales and 71% of its $13.9 billion total semiconductor revenue, based on IC Insights' estimates.

TI was among the first companies to manufacture analog semiconductors on 300mm wafers. TI has claimed that manufacturing analog ICs on 300mm wafers gives it a 40% cost advantage per unpackaged chip compared to using 200mm wafers. In 2017, about half of TI's analog revenue was generated on devices built using 300mm wafers.

Second-place ADI registered a 14% increase in analog IC sales in 2017 to $4.3 billion, according to IC Insights' supplier ranking. The 2016 and 2017 revenue numbers shown for ADI include sales from Linear Technology, which was acquired by the company in 1Q17 for $15.8 billion.

NXP was the only supplier in the top-10 ranking that experienced a decline (-1%) in its analog sales last year. Some of NXP's analog revenue decline can be attributed to the sale of its Standard Products business to a consortium of Chinese investors consisting of JAC Capital and Wise Road Capital. The $2.75 billion transaction was completed in February 2017. The Standard Products business was renamed Nexperia and headquartered in the Netherlands.

Among the top 10, ON Semiconductor showed the largest analog sales gain in 2017, with revenues increasing 35% to $1.8 billion, which represented a 3% share of the market. This follows a 16% rise in its analog sales in 2016. Some of the strong increases in sales during the last two years were a result of ON Semi's acquisition of Fairchild Semiconductor in September 2016 for $2.4 billion. ON's analog business was also boosted in 2017 by record sales of its power management products to the automotive market, specifically for active safety, powertrain, body electronics, and lighting applications. ◆

TSMC continues to dominate the worldwide foundry market

Research included in the recently released 50-page April Update to the 2018 edition of IC Insights' McClean Report shows that in 2017, the top eight major foundry leaders (i.e., sales of ≥$1.0 billion) held 88% of the $62.3 billion worldwide foundry market. The 2017 share was the same level as in 2016 and one point higher than the share the top eight foundries represented in 2015. With the barriers to entry (e.g., fab costs, access to leading edge technology, etc.) into the foundry business being so high and rising, IC Insights expects this "major" marketshare figure to remain at or near this elevated level in the future.

TSMC, by far, was the leader with $32.2 billion in sales last year. In fact, TSMC's 2017 sales were over 5x that of second-ranked GlobalFoundries and more than 10x the sales of the fifth-ranked foundry SMIC.

China-based Huahong Group, which includes Huahong Grace and Shanghai Huali, displayed the highest growth rate of the major foundries last year with an 18% jump. Overall, 2017 was a good year for many of the major foundries with four of the eight registering double-digit sales increases.

Of the eight major foundries, six of them are headquartered in the Asia-Pacific region. As shown, Samsung was the only IDM foundry in the ranking. IBM, a former major IDM foundry, was acquired by GlobalFoundries in mid-2015 while IDM foundries Fujitsu and Intel fell short of the $1.0 billion sales threshold last year. Although growing only 4% last year, Samsung easily remained the largest IDM foundry in 2017, with over 5x the foundry sales of Fujitsu, the second-largest IDM foundry. ◁▶

Sales increase 20% year-to-year in April; double-digit annual growth projected for 2018

The Semiconductor Industry Association (SIA) announced worldwide sales of semiconductors reached $37.6 billion for the month of April 2018, an increase of 20.2 percent from the April 2017 total of $31.3 billion and 1.4 percent more than last month's total of $37.1 billion. Monthly sales numbers are compiled by the World Semiconductor Trade Statistics (WSTS) organization and represent a three-month moving average. Additionally, a newly released WSTS industry forecast projects annual global market growth of 12.4 percent in 2018 and 4.4 percent in 2019.

"The global semiconductor industry has posted consistently strong sales so far in 2018, and the global market has now experienced year-to-year growth of greater than 20 percent for 13 consecutive months," said John Neuffer, president and CEO, Semiconductor Industry Association. "Although boosted in part by impressive growth in the memory market, sales of non-memory products also grew by double digits in April on a year-to-year basis, and all major regional markets posted double-digit year-to-year gains. The global market is projected to experience significant annual growth this year, with more modest growth expected next year."

Regionally, year-to-year sales increased in the Americas (34.1 percent), China (22.1 percent), Europe(21.4 percent), Japan (14.6 percent), and Asia Pacific/All Other (10.2 percent). Compared with last month, sales were up in China (3.2 percent), Japan (2.7 percent), Europe (1.4 percent), and the Americas (0.8 percent), but down slightly in Asia Pacific/All Other (-0.8 percent).

Additionally, SIA endorsed the WSTS Spring 2018 global semiconductor sales forecast, which projects the industry's worldwide sales will be $463.4 billion in 2018. This would mark the industry's highest-ever annual sales, a 12.4 percent increase from the 2017 sales total. WSTS projects year-to-year increases across all regional markets for 2018: the Americas (14.0 percent), Europe (13.4 percent), Asia Pacific (including China) (12.3 percent), and Japan (8.6 percent). In 2019, growth in the semiconductor market is expected to moderate, with sales increases of between 4-5 percent expected across each of the regions. WSTS tabulates its semi-annual industry forecast by convening an extensive group of global semiconductor companies that provide accurate and timely indicators of semiconductor trends.

Apr 2018

Billions

Month-to-Month Sales

Market	Last Month	Current Month	% Change
Americas	8.10	8.16	0.8%
Europe	3.58	3.63	1.4%
Japan	3.21	3.30	2.7%
China	11.98	12.36	3.2%
Asia Pacific/All Other	10.23	10.15	-0.8%
Total	**37.09**	**37.59**	**1.4%**

Year-to-Year Sales

Market	Last Year	Current Month	% Change
Americas	6.08	8.16	34.1%
Europe	2.99	3.63	21.4%
Japan	2.88	3.30	14.6%
China	10.12	12.36	22.1%
Asia Pacific/All Other	9.21	10.15	10.2%
Total	**31.28**	**37.59**	**20.2%**

Three-Month-Moving Average Sales

Market	Nov/Dec/Jan	Feb/Mar/Apr	% Change
Americas	8.63	8.16	-5.5%
Europe	3.40	3.63	6.6%
Japan	3.21	3.30	2.8%
China	12.01	12.36	2.9%
Asia Pacific/All Other	10.35	10.15	-1.9%
Total	**37.60**	**37.59**	**0.0%**

Applied Materials breakthrough accelerates chip performance in the big data and AI era

Applied Materials, Inc. announced a breakthrough in materials engineering that accelerates chip performance in the big data and AI era.

In the past, classic Moore's Law scaling of a small number of easy-to-integrate materials simultaneously improved chip performance, power and area/cost (PPAC). Today, materials such as tungsten and copper are no longer scalable beyond the 10nm foundry node because their electrical performance has reached physical limits for transistor contacts and local interconnects. This has created a major bottleneck in achieving the full performance potential of FinFET transistors.

Cobalt removes this bottleneck but also requires a change in process system strategy. As the industry scales structures to extreme dimensions, the materials behave differently and must be systematically engineered at the atomic scale, often under vacuum.

To enable the use of cobalt as a new conducting material in the transistor contact and interconnect, Applied has combined several materials engineering steps – pre-clean, PVD, ALD and CVD – on the Endura® platform. Moreover, Applied has defined an integrated cobalt suite that includes anneal on the Producer® platform, planarization on the Reflexion® LK Prime CMP platform and e-beam inspection on the PROVision™ platform. Customers can use this proven, Integrated Materials Solution to speed time-to-market and increase chip performance at the 7nm foundry node and beyond.

"Five years ago, Applied anticipated an inflection in the transistor contact and interconnect, and we began developing an alternative materials solution that could take us beyond the 10nm node," said Dr. Prabu Raja, senior vice president of Applied's Semiconductor Products Group. "Applied brought together its experts in chemistry, physics, engineering and data science to explore the broad portfolio of Applied's technologies and create a breakthrough Integrated Materials Solution for the industry. As we enter the big data and AI era, there will be more of these inflections, and we are excited to be having earlier and deeper collaborations with our customers to accelerate their roadmaps and enable devices we never dreamed possible."

While challenging to integrate, cobalt brings significant benefits to chips and chip making: lower resistance and variability at small dimensions; improved gapfill at very fine dimensions; and improved reliability. Applied's integrated cobalt suite is now shipping to foundry/logic customers worldwide.

Applied Materials, Inc. (Nasdaq:AMAT) is a leader in materials engineering solutions used to produce virtually every new chip and advanced display in the world.

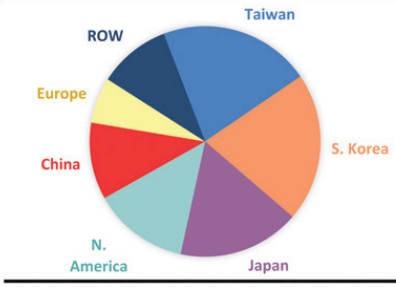
China Is Betting on AI

PHIL GARROU,
Contributing Editor

China is by far the largest consumer of semiconductors reportedly accounting for 45 percent of the worldwide demand for chips, used both in China and for exports. More than 90 percent of its consumption relies on imported ICs.

At the end of 2016 IC Insights reported that China was responsible for ~ 11% of the worlds wafer capacity (**FIGURE 1**).

Wafer Capacity at Dec-2016 – by Geographic Region
(Monthly Installed Capacity in 200mm-equivalents)



Region	Installed Capacity (K w/m)	% of Worldwide Total
Taiwan	3,645	21.3%
S. Korea	3,569	20.9%
Japan	2,925	17.1%
N. America	2,297	13.4%
China	1,849	10.8%
Europe	1,099	6.4%
ROW	1,730	10.1%
TOTAL	17,114	100%

Source: IC Insights

China has been working to reduce its dependence on technology imports, including computer chips for several years. In March, it was reported that state-backed China Integrated Circuit Industry Investment Fund Co. is in talks with government agencies to raise at least $24B to build up China's domestic semiconductor industry. Recently , the Wall Street Journal reported that China is poised to announce a new fund of ~ $47B for development of its semiconductor industry and close the technology gap with the U.S. and other rivals.

While the existence of such a fund has been rumored for months, the size of the fund has been hard to pin down. A few weeks ago, Reuters reported that the fund would be $19B, while Bloomberg reported $31.5B two months ago. The exact number appears to be under consideration among the Chinese leadership, and tied to the increasingly tense trade negotiations with the United States. If $47B is indeed the correct number, it would be identical in size to the $47 billion fund that was financed by Tsinghua University, to spur the development of an indigenous semiconductor industry back in 2015.

While China is playing catchup in many semiconductor areas, it has also been placing its bets on new areas like 5G wireless and AI (artificial intelligence) chips.

China releases its first cloud AI chip

Beijing artificial intelligence (AI) chip maker Cambricon Technologies Corp Ltd has just announced two new products, a cloud-based smart chip Cambricon MLU100 and a new version of its AI processor, Cambricon 1M, in Shanghai on May 3rd.

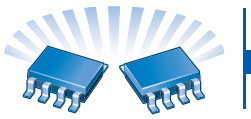
The cloud chip MLU100 (**FIGURE 2**), developed by China's Cambricon Technology, is China's first cloud artificial intelligence (AI) chip developed to have big data processing ability, for image and voice searching.

Cambricon 1M is the company's third generation AI chip (gen 1 was in 2015) for "edge devices". An edge device is a device which provides an entry point into enterprise or service provider networks such as routers, routing switches, integrated access devices (IADs), multiplexers, and WAN (wide area network) access devices. Using TSMC 7nm technology, the AI chip can be used in smartphones, smart speakers, cameras, and smart driving.

Cambricon MLU100 supports cloud-based machine learning, including vision, audio and natural language processing. It can process under complex scenarios, such as "...with huge amounts of data, multi-tasks, multi-modality and low latency." This processor reportedly can provide 166 TFLOPS in high-performance mode with energy consumption of no more than 110 watts at peak. The MLU100 is built with TSMC 16nm technology.

Lenovo has announced that their ThinkSystem SR650 server is based on the MLU100. Products built around MLU100 were also announced by Sugon and iFlytek who also announced collaboration with Cambricon. ◆

Packaging

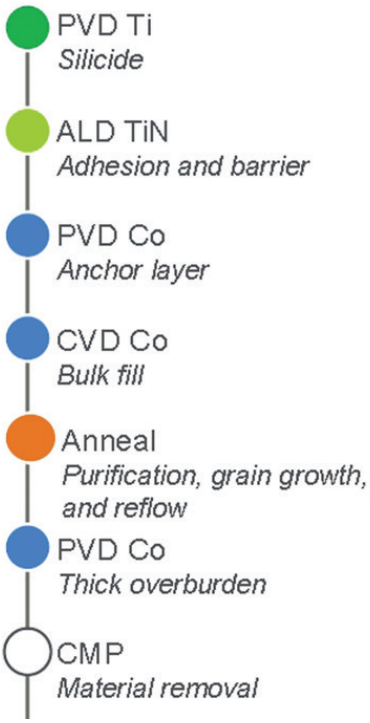


Applied Materials Fields Cobalt Solution for MOL

PETE SINGER,
Editor-in-Chief

Applied Materials has introduced a set of processes that enable cobalt to be used instead of tungsten and copper for contacts and middle-of-line interconnects. Higher levels of metal, which typically have wider dimensions, will still employ copper as the material of choice, but at more advanced nodes, cobalt will likely be the best option as linewidths continue to shrink. Tungsten will still be used at the gate contact level.

To enable the use of cobalt, Applied has combined several materials engineering steps – pre-clean, PVD, ALD and CVD – on the Endura® platform. Moreover, Applied has defined an integrated cobalt suite that includes anneal on the Producer® platform, planarization on the Reflexion® LK Prime CMP platform and e-beam inspection on the PROVision™ platform. The process flow is shown in **FIGURE 1**.

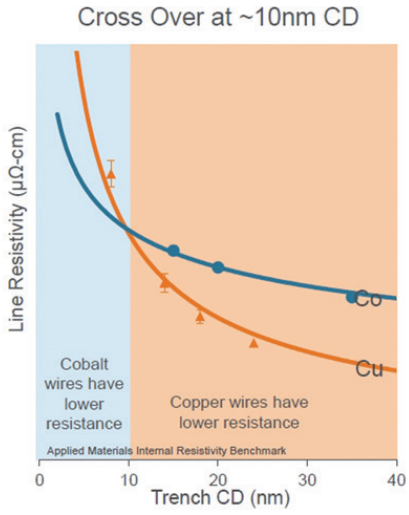


While challenging to integrate, cobalt brings significant benefits to chips and chip making: lower resistance and variability at small dimensions; improved gapfill at very fine dimensions; and improved reliability. The move to cobalt, which is underway at Intel, GlobalFoundries and other semiconductor manufacturing companies, is the first major change in materials used as conductors since copper dual damascene replaced aluminum in 1997. "You don't see inflections this large very often," said Jonathan Bakke, global product manager, Metal Deposition Products at Applied Materials. "This is a complete metallization change."

At IEDM last year, Intel said it would use cobalt for its 10nm logic process for several of the lower metal levels, including a cobalt fill at the trench contacts and cobalt M0 and M1 wiring levels. The result was much-improved resistivity–a 60 percent reduction in line resistance and a 1.5X reduction in contact resistance – and improved reliability.

Today, critical dimensions of contacts and interconnects are about 20 nm, plus or minus a few nanometers depending on the customer and how it's defined. "As you get smaller – and you typically get about 30% smaller with each node – you're running out of room for tungsten. Copper is also facing challenges in both gap fill and electromigration," Bakke said.

As shown in **FIGURE 2**, cobalt has advantages over copper when dimensions shrink to about 10nm. They are presently at 30 nm. It's not yet clear when that cross-over point will arrive, but decisions will be based on how much resistivity and electromigration improvement can be gained.



Applied Materials started developing cobalt-based processes in the mid-2000s, and released the Volta CVD Cobalt system in 2013, which was designed to encapsulate copper interconnects in cobalt, which helped improve gap fill and electromigration. "It was shortly thereafter that we started depositing thick CVD cobalt films for metallization. We quickly realized that there's a lot of challenges with doing this kind of metallization using cobalt because of its unique properties," Bakke said. Cobalt can be reflowed and recrystallized, which eliminates seams and leads to larger grain sizes, which reduces resistivity. "We started looking at things like interfaces, adhesion and microstructure of the cobalt to make sure that it was an efficient material and it had very low resistance and high yield for in-device manufacturers," he added. One perfected, it took several years before the processes were fully qualified at customers. "This year is when we start to see proliferation and expect HDM manufacturing of real devices with cobalt," Bakke said. ◆

Semiconductors

Optimized stepping for fan-out wafer and panel packaging

KEITH BEST, *Director of Lithography Applications Engineering, Rudolph Technologies, Inc., Wilmington, Mass.*

Optimized stepping, based on parallel analysis of die placement errors and prediction of overlay errors, can increase lithography throughput by more than an order of magnitude and deliver commensurate reductions in cost of ownership. The productivity benefits of optimized stepping are demonstrated using a test reticle with known die placement errors.

Fan out wafer and panel level packaging (FOWLP/FOPLP) processes place individual known good die on reconstituted wafer (round) or panel (rectangular) substrates, providing more space between die than the original wafer. The additional space is used to expand (fan out) the die's I/O connections in order to create a pad array large enough to accommodate solder balls that will connect the die to the end-use substrate. The processes used to create these redistribution layers (RDL) are similar to wafer fabrication processes, using patterns defined by photolithography, with feature sizes typically ranging from a few micrometers to tens of micrometers. The placement and reconstitution molding processes introduce significant die placement errors that must be corrected in the photolithography process to ensure accurate overlay registration among the multiple vias and distribution layers that are built up to form the RDL. The errors can be measured on the lithography tool, but this significantly impacts throughput as the measurement process for each die may take as much or more time than the exposure itself.

Current best-practice methods employ an external metrology system to measure the displacement of each die. This metrology data is converted into a stepper correction file that is sent to the lithography stepper tool, eliminating the need to measure displacement on the stepper and more than doubling stepper throughput. An important enhancement to this method, optimized stepping, varies the number of die per exposure based on a predictive yield analysis of the displacement measurements, potentially multiplying throughput 20X or more. Results obtained using a test reticle that includes intentionally displaced die pads, vias, and RDL features typical of an FOWLP/FOPLP process confirm the validity of the approach.

Introduction

Die placements on reconstituted wafer or panel substrates include translational and rotational placement errors. The pick and place process itself introduces initial error. Additional error is created in the mold process and by instability of the mold compound through repeated processing cycles. As a result, the position of the die must be measured before each exposure in the lithography system to ensure sufficient registration with the underlying layer.

Displacement errors can be measured in the lithography tool, but the measurements are slow, typically taking as much time as the exposure. Moving the measurement to a separate system and feeding corrections to the stepper can double throughput.

Optimized stepping adds predictive yield analysis to the external measurement and correction procedures and increases the number of die included in the exposure field up to a user-specified yield threshold. **FIGURE 1** illustrates the exposure/measurement loop. The measurement and analysis are repeated after each layer is exposed, calculating a new set of corrections. In addition to corrections, the software engine analyzes the displacement errors to predict yield (based on a user designated limit for acceptable registration error) for multiple die exposure fields of varying sizes. The method requires tight integration of the stepper and measurement system with the controlling software.

With RDL features currently reaching sizes as small as 2μm, die placement measurements and pattern overlay registration requirements are also continuing to tighten. The speed of the measurement/correction/prediction calculation for each wafer/panel is also an important

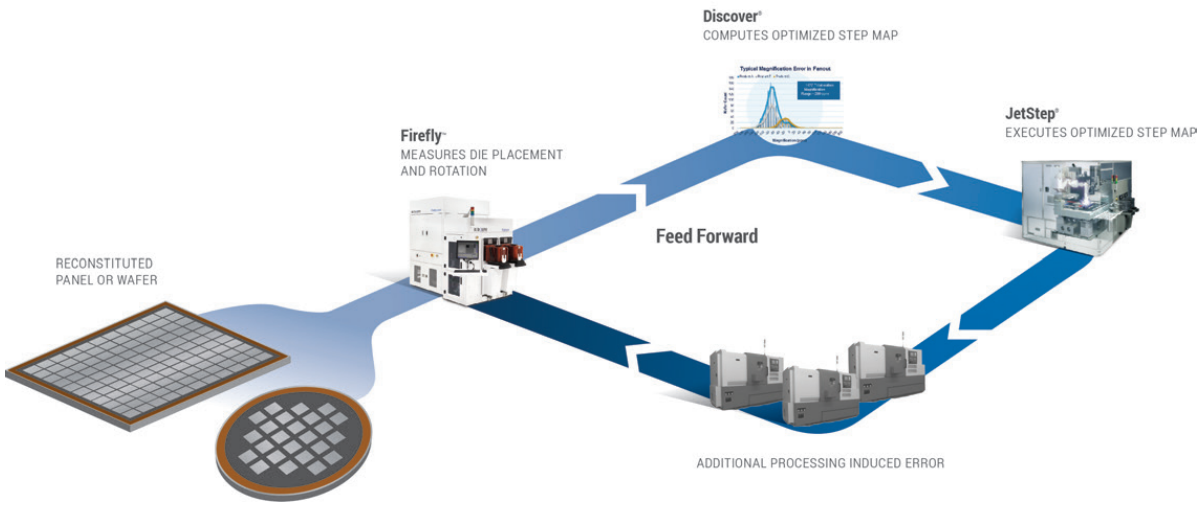


FIGURE 1. The optimized stepping process loop includes: 1) measurement of die displacement errors outside the stepper, 2) correction calculations and yield modeling, 3) exposure, 4) continuous run-to-run adjustments.

consideration. It must be faster than the exposure time to avoid becoming the throughput limiting step. Note that this requirement refers to the total exposure for multiple die per field which can be much less than the time needed to expose each die individually. The metrology system used in this work (Firefly system, Rudolph Technologies) can meet these challenges and measure placement errors for >5,000 die on a 510mm x 515mm panel in less than 10 minutes.

The stepper must be able to accept externally generated corrections for translation, rotation, and magnification. It must also have a large exposure field and the ability to automatically select different images from the reticle (masking blades), changing the size of the field for each exposure. The stepper used in this work was the JetStep system from Rudolph Technologies.

The third critical piece of the optimized stepping loop is the software engine (Discover software, Rudolph Technologies) which calculates displacement corrections and predicts yield for various multi-die exposure configurations. It also enables statistical process control (SPC) and controls genealogy.

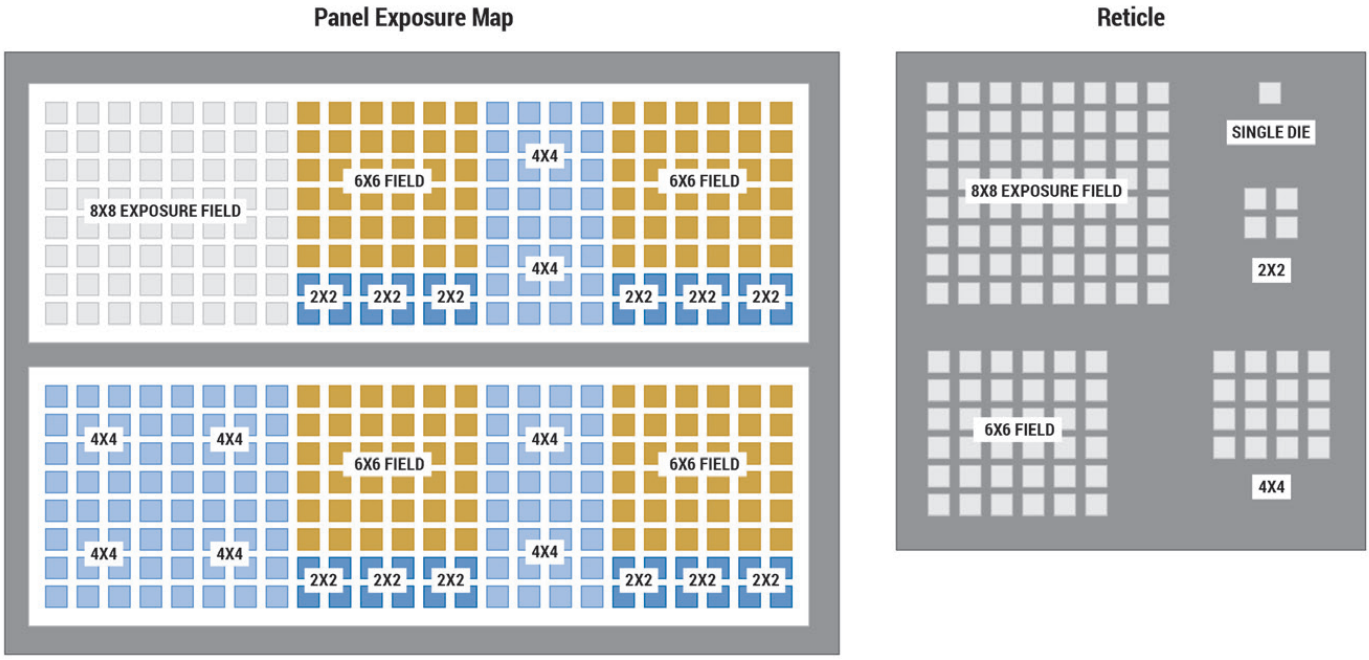


FIGURE 2. Optimized stepping uses a reticle (right) that contains multiple field sizes, each including a multi-die array of varying size (here ranging from 1X1 to 8X8). Under software control, the stepper exposes fields as required to cover the panel (left) while balancing throughput (field size) and yield (overlay error).

Exposure Shot Pyramid Example

LEVEL	MARK TYPE	PACKAGE #	FAILURE ALLOWED
1	1x1	1	0
2	1x2	2	0
3	2x2	4	0
4	4x4	16	1
5	8x8	64	4

Recursive Split Illustration

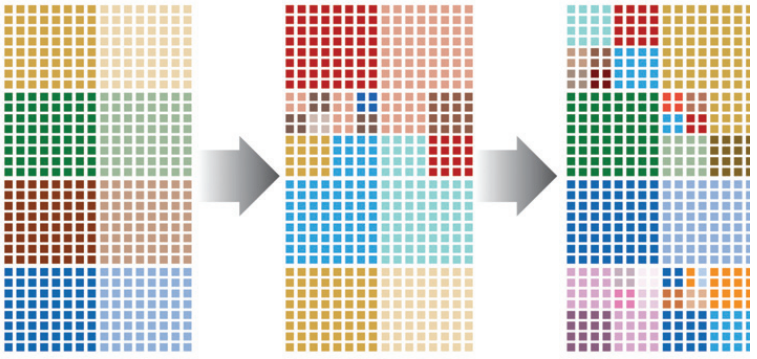


FIGURE 3. The operator specifies yield requirements in a shot pyramid that designates the maximum number of failures allowed for each field size, the software initially predicts yields at the largest field size and recursively splits the field to a smaller size if the prediction does not meet the yield requirement.

Balancing yield and throughput

Optimized stepping uses a reticle that includes multiple exposure fields each comprising die arrays of different sizes. In **FIGURE 2** the arrays range from a single die to an 8 X 8 array of 64 die. On a wafer containing random displacement errors, the smallest overlay error will be achieved by aligning the exposure pattern for each die individually. However, this accuracy comes at a high cost of reduced throughput. Optimized stepping analyzes the measured displacement errors and calculates the number of die that will meet a designated overlay error limit for various field sizes. It then selects the combination of fields that maximizes throughput. In operation, the stepper automatically selects the correct reticle image and adjusts the field size to expose the selected array.

The yield prediction algorithm (**FIGURE 3**) uses a recursive splitting procedure that initially predicts yield for the largest available field. If the prediction does not meet user-defined yield requirements, it splits the field and re-evaluates the prediction, repeating this cycle for decreasing field sizes until all exposures yield satisfactory results. The user designates an aggressiveness factor (larger values mean more aggressive splits) and specifies yield requirements in an exposure shot pyramid that determines the number of failures allowed for each available field size.

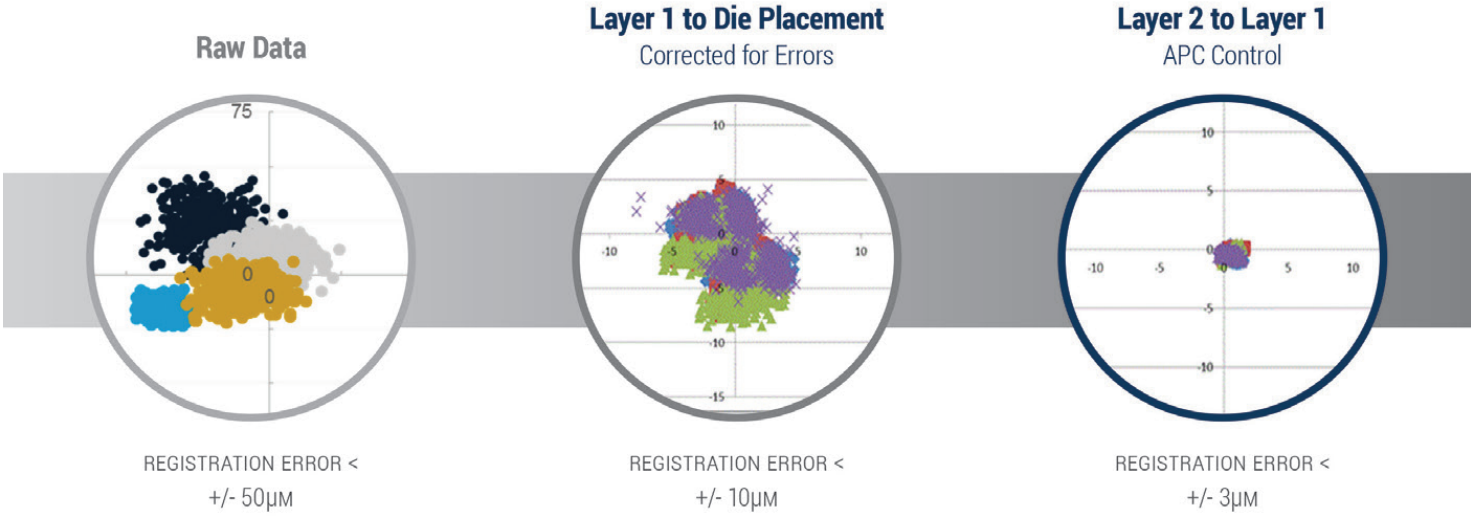


FIGURE 4. Compares registration errors for uncorrected, raw data (left), corrected exposures (middle), and APC run-to-run control (right) showing an improvement from +/-50µm to less than +/-3µm.

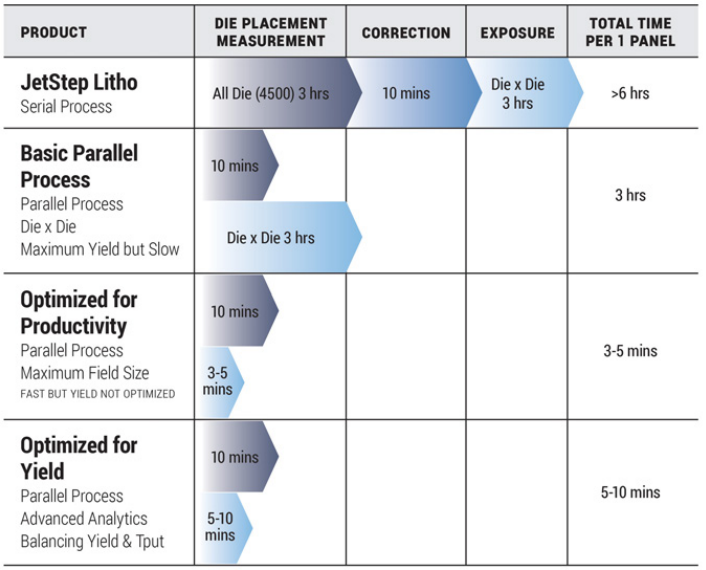


FIGURE 5. Making measurements in parallel outside the stepper cuts total cycle time in half, from six hours to three hours, and makes exposure time the rate limiting step. Optimized stepping can cut exposure time by an order of magnitude and permits the operator to balance productivity against yield.

Results

Optimized stepping was evaluated using a test reticle with multiple field sizes containing die that included pads, vias and RDL structures typical of FOWLP/FOPLP. The patterns included predefined offsets in some of the structures for feed forward measurement testing. Application of the corrections calculated from the die placement error measurements yielded overlay errors of < +/-3µm (**FIGURE 4**).

Productivity vs. yield

FIGURE 5 illustrates the potential benefits of optimized stepping applied to a panel process. In the example the panel contains approximately 4,500 die. A conventional serial process, with placement errors measured on the stepper, takes a little over six hours, including three hours for measurement and three hours for exposure. Making the measurements outside the stepper in parallel with the exposure halves the cycle time per panel to three hours, and the exposure time becomes the throughput limiting step. The third case is optimized for productivity, using larger field sizes and more relaxed yield requirements. It reduces cycle time to less than 10 minutes. The final case balances throughput against more stringent yield requirements and results slightly higher cycle times that are still nearly an order of magnitude shorter than the conventional serial process of the first case.

Conclusion

Optimized stepping can increase lithography throughput by more than an order of magnitude and deliver commensurate reductions in cost of ownership. The method also provides a means to balance productivity (throughput) against yield, adding an extra dimension of flexibility for optimizing profitability. Optimized stepping requires a stepper that can use externally calculated corrections and automatically change field size and reticle position. The metrology system must have sufficient accuracy and speed (faster than the accelerated exposure time). The control software must be able to predict yields based on measured displacement errors and control the stepper. Using a test reticle with known displacement errors, we have verified the accuracy of the metrology system and correction procedures and demonstrated the productivity benefits of optimized stepping.

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Material Innovations for advancements in fan-out packaging

KIM YESS, *Director of Technology Development, Wafer-Level Packaging Business Unit Brewer Science, Rolla, MO*

The development of a new class of materials with superior functionalities is essential to enable emerging process schemes for wafer- or panel-level FO packaging.

Fan-out (FO) packaging is one of the most talked-about advanced packaging solutions for heterogeneous integration. Although it has been available for nearly a decade for the chips used in mobile devices, its popularity has spiked in the past two years, thanks to Apple's adoption of TSMC's integrated fan-out package-on-package (InFO PoP) for its A10 and A11 processors, and the Apple Watch. As a result, FO has quickly progressed to the mainstream, with outsourced semiconductor and test service providers (OSATs), foundries and integrated device manufacturers (IDMs) vying for market share.

What's driving FO innovation?

According to Yole Développement, smartphone application processors are the main beneficiaries of high-density fan-out (HDFO)'s excellent performance and thin profile. As a result, as shown in **FIGURE 1**, the HDFO market was worth $500 million in 2017 and was predicted to exceed $1 billion if other players, namely Qualcomm, Samsung and Huawei switch to HDFO [1].

Jan Vardaman, TechSearch International, said Apple selected InFO PoP for its A10 processor because of power noise reduction and signal integrity improvement, in addition to being thin enough to enable a low-profile PoP solution as small as 15 x 15 mm.

In addition to HDFO, the market is growing for conventional FO, driven by new applications such as audio CODECs, power management ICs, radar modules and RF [2].

The automotive electronics market—particularly advanced driver assistance systems (ADAS) and autonomous vehicles—is also being explored as a viable application for FO because of the flexibility and fast time to market it provides, as well as the ability to adapt to new sensor system protocols.

Exploring new processes

In this race to provide the most reliable, highest-density solution, many manufacturing approaches have emerged. FO is not only becoming more versatile, it is also reaching high enough densities to offer a cost-effective alternative to 2.5D interposers. As the demand for FO increases, packaging processes are being explored in both the wafer and panel formats. This is driving a need for new and better-performing materials that address more stringent specifications to meet, for example, finer line and space requirements, as well as the improved elongation needed for advanced high-density FO.

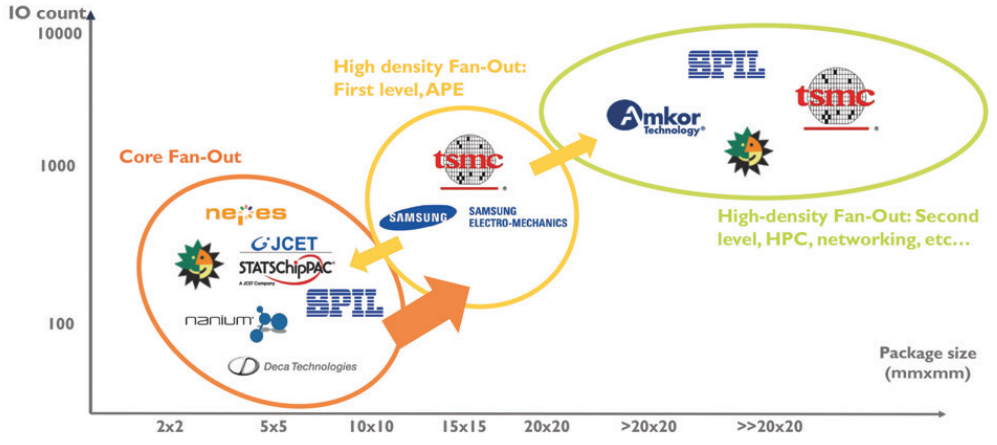

FIGURE 1. Different fan-out platforms for different applications and suppliers. (Image source: Yole Developpement, Fan-out: Technology Trends and Market Report 2017).

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Thanks to recent innovations in packaging materials, three new process approaches have been developed to bridge these gaps. One approach involves new carrier-assist release-layer materials for creation of the redistribution layer (RDL)-first/chip-last buildup processes. Another important development is an alternative to lithography dielectric patterning that uses laser-ablated dielectric materials. Lastly, an alternative to the molding process in the chip-first approach that uses a laminated die stencil and gap-fill materials is under development.

Carrier-assist release layer for chip-last FO

Low-density FO is built using a chip-first approach, which involves first placing the chips on a substrate wafer followed by over-mold to create a reconstituted wafer, with subsequent RDL and solder-ball placement. On the other hand, HDFO processes like TSMC's InFO technology use a chip-last approach. Also known as RDL-first, this approach (with target features of ≤2 µm l/s) begins with a layer-by-layer buildup of the RDL on a carrier wafer, followed by die placement and over-mold.

Currently, manufacturers turn to permanent bonding, followed by backgrinding to remove the carrier wafer. This is because conventional temporary bond/debond materials cannot withstand the downstream RDL processes that subject the build-up layers to high temperatures and vacuum conditions, as well as harsh chemical environments. However, backgrinding is a destructive process, creating debris that can cause damage to the device itself.

The new approach uses neither a temporary nor a permanent bonding process. Instead, it utilizes a release layer on the carrier substrate to allow separation of the FO wafer from the carrier at the end of the process flow.

The challenge with this new method is designing a material that withstands high-temperature process steps as well as strong mechanical stresses without delaminating or distorting the reconstituted wafer. Additionally, the material must be adaptable to the new FO panel-level processes (FOPLP) along with existing round wafers, as the industry innovates in that direction.

Manufacturers are investigating the use of copper foil lamination, as an alternative to physical vapor deposition of the seed layer. The copper laminating process requires a material that is flexible enough to sufficiently laminate layers on top of the substrate, and that can be cured using UV radiation or heat to yield a structurally stable base that meets the thermomechanical and chemical resistance requirements of the build-up process.

Additionally, it must be releasable by ultraviolet (UV) laser ablation or other UV exposure. To meet these needs, a new class of so-called "triangle" polymeric materials has been conceived that have advantages over standard-application release layers because they are multi-functional. Specifically, these "triangle" materials can be laminated, cured and debonded, adding flexibility to the carrier-assisted process (**FIGURE 2**).

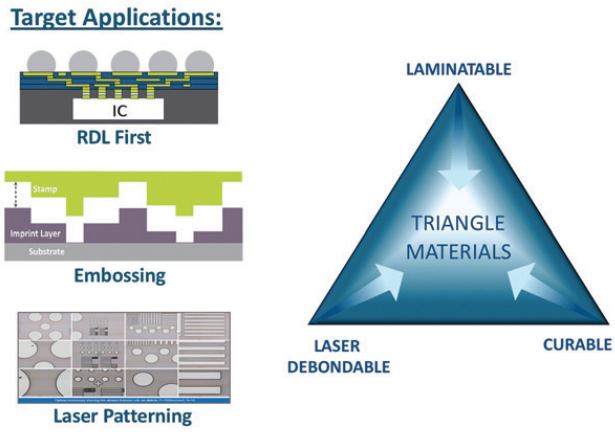

FIGURE 2. Triangle materials are those that are laminatable, curable and laser debondable.

Dielectric RDL patterning

Traditional RDL patterning uses a complicated, 24-step photolithography process that employs photosensitive dielectric materials and masks to create trace patterns, followed by Cu plating to route the signal from the chip out of the package to the solder balls. This process, developed with round wafers in mind, uses spin-coated dielectrics. Unfortunately, these lithography processes are too costly to utilize in innovative package designs that must meet the stringent requirements for most markets [3].

As the industry moves to HDFO and begins to investigate panel-level processes to reduce cost and improve yield, alternative patterning approaches are being developed that can achieve resolutions down to 5 µm with an ultimate goal of 2 µm l/s. Laser ablation is one alternative to photolithography for creating finer-featured RDL patterns while achieving all these goals.

The combination of a high-power excimer laser source, large-field laser mask and precision projection optics enables the accurate replication and placement of fine resolution circuit patterns without the need for any wet processing. In addition, with excimer laser patterning technology, the industry gains a much wider choice of dielectric materials (photopatternable and non-photopatternable) to help achieve further reductions in manufacturing costs as well as enhancements in chip or package performance [4].

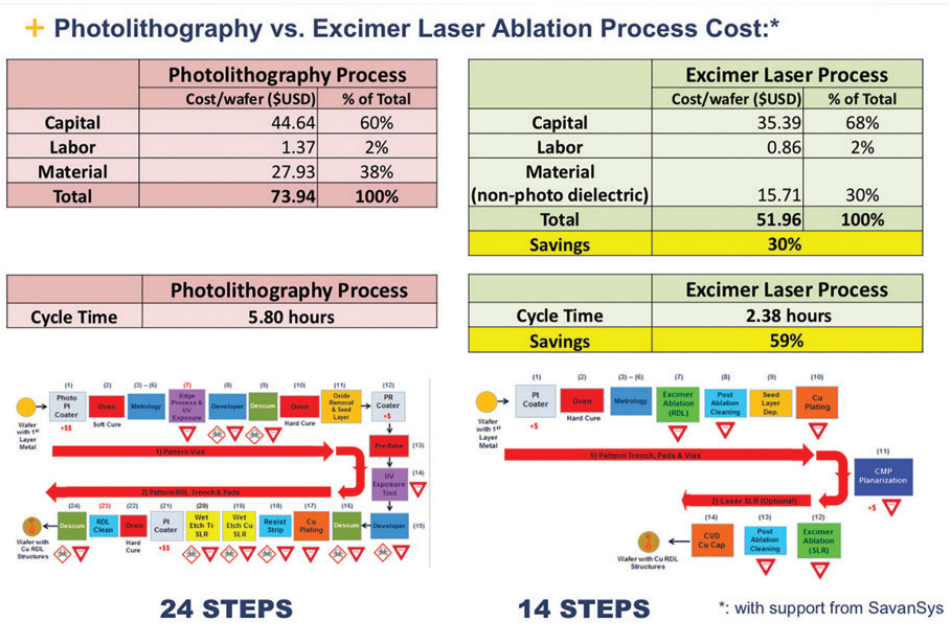

FIGURE 3. Excimer laser ablation provides the elimination of 10 process steps, a 30% per wafer processing cost reduction and a 59% cost savings in cycle time, when compared to spin-on dielectrics (Image source: SavanSys).

By using excimer laser ablation, many process steps and costly materials can be eliminated from the manufacturing flow, including resist coating, baking, developing and resist stripping and etching using harsh chemicals [5].

FIGURE 3 demonstrates the considerable cost savings of laser ablation over photolithography. Activity-based cost modeling was used to carry out the cost comparison between the two processes. With activity-based cost modeling, a process flow is divided into a series of activities, and the total cost of each activity is calculated. The cost of each activity is determined by analyzing the following attributes: time, amount of labor and cost of material required (consumable and permanent), tooling cost, all capital costs, and yield loss associated with the activity.

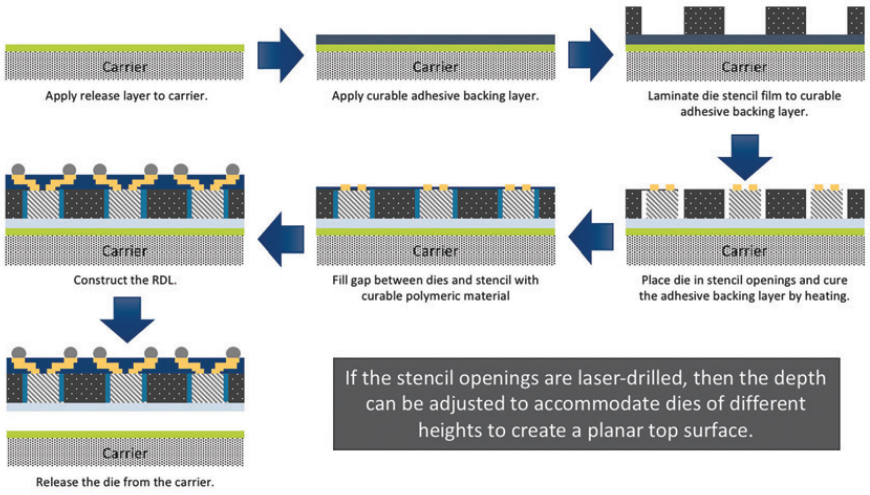

FIGURE 4. Process flow for a laminated polymeric die-stencil fill concept

Laser-ablated patterning is a room-temperature process that works by using a dielectric material to build up RDL fixtures, and excimer and solid-state lasers to ablate the material and direct-write a pattern. Laser ablation allows for depth and side-wall angle control, making it possible to create feature sizes <5 µm. It also reduces chemical waste streams. Additionally, fewer steps, fast removal rates and high throughput lead to a lower-cost solution in comparison with traditional photolithography (Fig. 3).

Photosensitive dielectric materials often fall short of meeting the required mechanical and thermal properties, and therefore need a variety of process "work-arounds" that add to the cost of ownership. Alternatively, non-photopatternable dielectric materials can be designed using a vast selection of chemical platforms, which improves the possibility of meeting the thermal and mechanical property requirements.

As with all new approaches, laser ablation is not without some challenges. Post-laser-ablation cleaning and debris removal, along with surface roughness as a result of the ablation step, need to be addressed. Additionally, the laser system needs to achieve a high ablation rate for high throughput. While the process costs of laser ablation are lower than photolithography, there is still a significant equipment capacity investment required to add laser tools to the manufacturing line. This may delay overcoming the most critical challenge: convincing the industry to embrace laser ablation patterning over conventional approaches.

Development of the dielectric material is ongoing to further push the resolution of laser-ablated materials. In addition to spin and spray coating, other deposition methods being investigated include slot-die coating, ink-jet printing, Vermeer coating, spray coating and laminate film.

Laminated polymeric die-stencil fill concept

Chip-first is the standard approach for conventional FO packages, including embedded wafer level ball grid arrays (eWLBs), redistributed chip packages (RCPs), M-Series and others. It calls for placing die into the mold compound before the RDL processing steps. One of the challenges of this approach that impacts final yield is the die shift that can occur during the RDL processes. Additionally, in multi-die FOWLP configurations that combine disparate technologies to essentially form a system-in-package (SiP), the dies may be of different sizes and heights. Additionally, the mismatch in coefficient of thermal expansion (CTE) between all of the materials involved leads to severe warpage of the reconstituted wafer.

A new carrier-based approach developed to combat this problem replaces the over-mold structure around the dies with a laminated die stencil (**FIGURE 4**). A release layer is first applied to a carrier, followed by a curable adhesive backing layer. Next, the die stencil film is laminated to the curable adhesive backing layer. The dies are then placed in the stencil openings and attached to the adhesive backing layer during thermal curing. The gaps between the dies and stencil are then filled with a flexible yet curable polymeric material, yielding a stable reconstituted substrate. This is followed by construction of the RDLs while still supported on the carrier. Finally, the reconstituted substrate is released from the carrier.

The stencil can be fabricated as a sheet from a variety of high-temperature-stable thermoplastics including, for example, carbon-fiber-filled polyetheretherketone (PEEK), which has an in-plane CTE of <10 ppm/K.

The pre-formed cavities can be configured for different die sizes and types to fabricate SiP components. The curable adhesive backing layer is comparatively soft and tacky before it is cured. This property allows the die-stencil film to be laminated to the structure at low temperatures.

This process not only addresses the die shift issue that plagues the chip-first approach, it also enables varying levels of die thickness. When placed in the stencil, the polymeric material allows the dies to sink and adjusts itself within the stencil. Once the dies are set, the material is cured, which locks them in place. Additionally, the process offers high-temperature stability, better CTE matching for warpage control, and high throughput.

Summary and conclusion

Fan-out packaging is on track to be a game-changing advanced packaging technology that will enable heterogeneous integration architectures. Applications have already expanded beyond smartphones, with HDFO targeting emerging applications.

Substrate handling and RDL strategies will be increasingly important, if not critical, for both conventional and HDFO technologies. To this end, the development of a new class of materials with superior functionalities is essential to enable emerging process schemes for wafer- or panel-level FO packaging.

The gamut of application needs for wafer support includes simple thinning processes during the backside processing of ultrathin, 300-mm silicon wafers, as well as reconstituted substrates for RDL fabrication. In addition to new materials, novel manufacturing approaches are also needed to further optimize the FO process flow.

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Void control in die attach joint

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To eliminate voids, it is important to control the process to minimize moisture absorption and optimize a curing profile for die attach materials.

Polymeric die attach material, either in paste or in film form, is the most common type of adhesive used to attach chips to metallic or organic substrates in plastic-encapsulated IC packages. It offers many advantages over solders such as lower processing temperatures, lower stress, ease of application, excellent adhesion and a wide variety of products to meet a specific application. As microelectronics move towards thinner, smaller form factors, increased functionality, and higher power density, void formation in die attach joints (**FIGURE 1**), i.e. in die attach materials and/or at die attach interfaces, is one of the key issues that pose challenges for thermal management, electrical insulation and package reliability.

Impact of voids

Voids in die attach joints have a significant impact on die attach material cracking and interfacial delamination. Voids increase moisture absorption. If plastic packages with a larger amount of absorbed moisture are subject to a reflow process, the absorbed moisture (or condensed water in the voids) will vaporize, resulting in a higher vapor pressure. Moreover, stress concentrations occur near the voids and frequently are responsible for crack initiation. On the other hand, voids at the interface can degrade adhesive strength. The combined effect of higher vapor pressure, stress concentration around the voids and decreased adhesion, as a result of void formation, will make the package more susceptible to delamination and cracking [1].

Additionally, heat is dissipated mainly through die attach layer to the exposed pad in plastic packages with an exposed pad. Voids in die attach joints can result in a higher thermal resistance and thus increase junction temperatures significantly, thereby impacting the power device performance and reliability.

And finally, voiding is known to adversely affect electrical performance. Voiding can increase the volume resistivity of electrically conductive die attach materials, while decreasing electrical isolation capability. Therefore, it is crucial to minimize or eliminate voids in die attach joints to prevent mechanical, thermal and electrical failures.

Void detection

The ability to detect voids is key to ensuring the quality and reliability of die attach joints. There are four common techniques to detect voids: (1) Scanning Acoustic Microcopy (SAM), (2) X-ray imaging, (3) cross-section or parallel polishing with optical or electron microscope, and (4) glass die/slide with optical microscope (Fig. 1). The significant advantage of SAM over other techniques lies in its ability to detect voids in different layers within a package non-destructively. Void size detection is limited by the minimal defect size detected by SAM. If the void is too small, it may not be detected at all, depending on the package and equipment used. X-ray analysis allows for non-destructive detection of voids in silver-filled die attach materials. However its limits lie in its low resolution and magnification, a low sensitivity for the detection of voids in a thick sample, and its inability to differentiate voids at different interfaces [2]. Cross-section or parallel polishing with electronic microscope provides a very high magnification image to detect small voids, although it is destructive and time-consuming. Glass die or glass substrate with an optical microscope provides a simple, quick and easy way to visualize the voids.

Potential root causes of voids and solutions

There are four major sources of voids: (1) air trapped during a thawing process, (2) moisture induced voids, (3) voids formed during die attach film (DAF) lamination, and (4) volatile induced voids.

Freeze-thaw voids When an uncured die attach paste in a plastic syringe is removed from a freezer (typically -40oC) to an ambient environment for thawing, the syringe warms and expands faster than the adhesive. This introduces a gap between syringe and the adhesive. Upon thawing, the adhesive will re-wet the syringe wall and

air located in between the container and adhesive may become trapped. As a result, voids form. This is referred as freeze-thaw void [3]. The voids in pastes may cause incomplete dispensing pattern leading to inconsistent bond line thickness (BLT) and die tilt, thus causing delamination. Planetary centrifugal mixer is the most commonly used and effective equipment to remove this type of void.

Moisture induced voids Die attach material contains polar functional groups, such as hydroxyl group in epoxy resins and amide group in curing agents, which will absorb moisture from the environment during exposure in die attach process. As the industry moves to larger lead frame strips (100mm x 300mm), the total number of units on a lead frame strip increase significantly. As a result, die attach pastes may have been exposed to a production environment significantly longer before die placement. After die placement, there could also be a significant amount of waiting time (up to 24 hours) before curing. Both can result in a high moisture absorption in die attach pastes. Moreover, organic substrates can absorb moisture, while moisture may be present on metal lead frame surfaces. As temperatures increase during curing, absorbed moisture or condensed water will evolve as stream to cause voiding. Voids can also form at the DAF-substrate interface as a result of moisture uptake during the staging time between film attach and encapsulation process. Controlling moisture absorption of substrates and die attach materials at each stage before curing and production environment are critical to prevent moisture induced voids in die attach joints.

Void formation during DAF lamination One challenge associated with DAF is voiding during DAF lamination, especially when it is applied to organic substrates [**FIGURE 1(d)**]. There is a correlation of void pattern with the substrate surface topography [4]. Generally, increasing temperature, pressure and press time can reduce DAF melt viscosity and enable DAF to better wet lead frame or substrates, thereby preventing entrapment of voids at die attach process. If the DAF curing percentage is high before molding, then DAF has limited flow ability, and thus cannot completely fill the large gaps on the substrate. Consequently, voids present at the interface between DAF and an organic substrate since die bonding process. But if DAF has a lower curing percentage before molding, then DAF can re-soft and flow into large gaps under heat and transfer pressure to achieve voids-free bond line post molding [4].

Volatile induced voids Voids in die attach joints are generally formed during thermal curing since die attach pastes contain volatiles such as low molecular

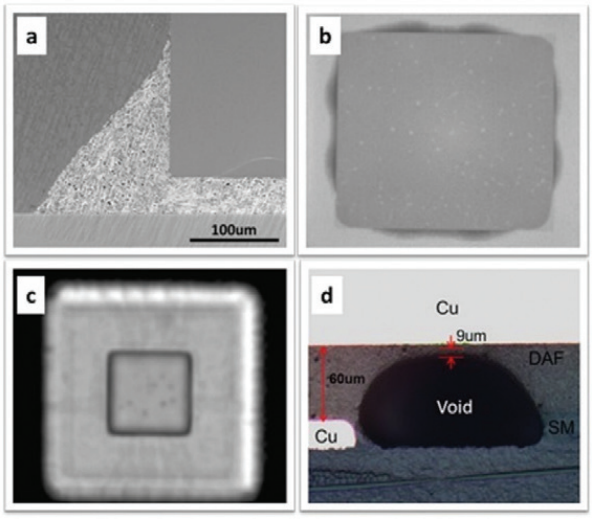

FIGURE 1. Examples on voids detected by (a) cross-section/SEM, (b) X-ray, (c) SAM, and (d) cross-section/optical microscopy.

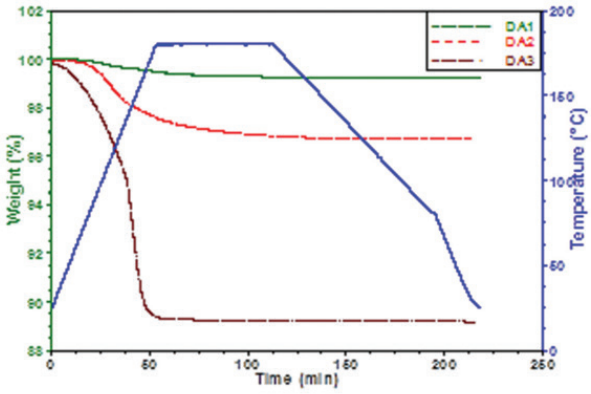

FIGURE 2. TGA of the three die attach materials using the same heating profile.

weight additives, diluents, and in some cases solvents for adjusting the viscosity for dispensing or printing. To study the effect of outgassing amounts on voids, we select three commercially available die attach materials with a significant difference in outgassing amounts using the same curing profile. As shown in **FIGURE 2**, as temperature increases, all die attach pastes outgas. DA1 shows a weight loss of 0.74wt%, DA2 3.1wt% and DA3 10.62wt%. Once volatiles start to outgas during thermal curing, they will begin to accumulate within the die attach material or at die attach interfaces. Voids begin to form by the entrapment of outgassing species or moisture. After voids initially form, voids can continue to grow until the volatiles have been consumed or the paste has been cured enough to form a highly cross-linked network. **FIGURE 3** shows optical images of dices assembled onto glass slides using three die attach materials. As expected, DA1 shows no voids for both

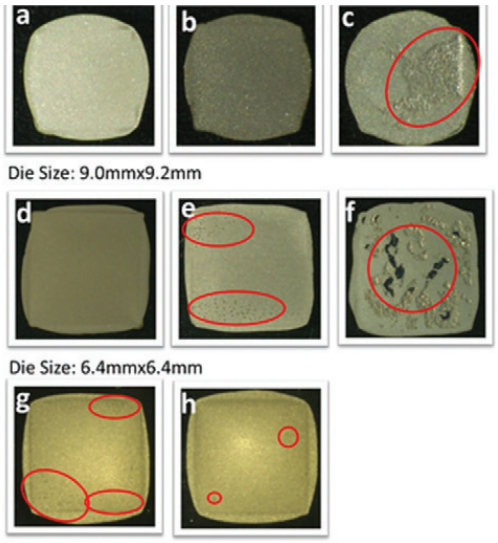

FIGURE 3. Die assembled onto glass slides with different die attach materials. (a) and (d): DA1; (b) and (e): DA2; (c) and (f): DA3. No voids observed in (a), (b) and (d). Small voids were observed in (e) Large voids were observed in (c) and (f). In (f), some area has no die attach material in the bond line and the black area is die backside. (g) and (h): DA2. (g) a single-step curing and (h) a two-step curing.

die sizes of 2.9mm x 2.9mm and of 9.0mm x 9.2mm, due to a very low amount of outgassing (0.74wt%). DA2 shows no voids for the small die size, but many small voids under the die periphery for the large die. Large voids are observed for DA3 for both die sizes since it has a very large amount of outgassing (10.62wt%). DA2 also shows voids even with a medium die size 6.4mm x 6.4mm [**FIGURE 3(g)**]. Differential Scanning Calorimetry (DSC) was used to further study the curing behaviors of DA2 and DA3, as shown in **FIGURES 4** and **5**. Comparing **FIGURE 4** with **FIGURE 5**, it is interesting to observe the difference in thermal behavior of the two die attach materials. For DA2, as curing starts, the weight loss rate becomes slower, while the weight loss rate for

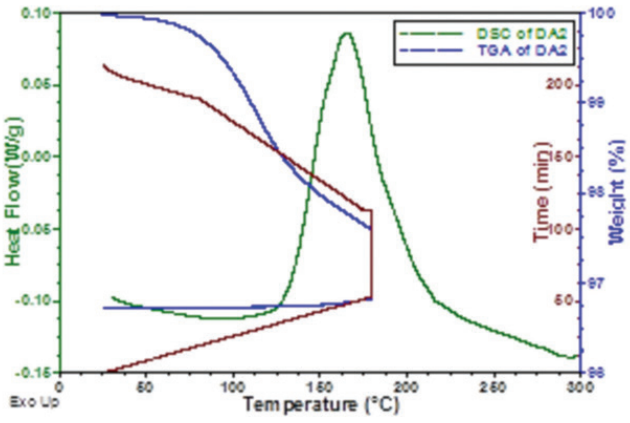

FIGURE 4. TGA and DSC of DA2 (heating rate: 10°C/min).

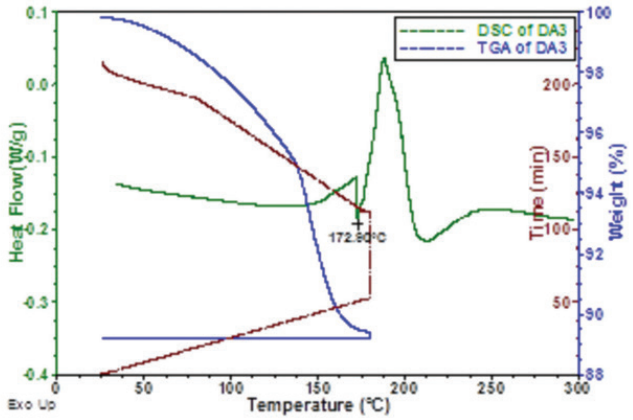

FIGURE 5. TGA and DSC of DA3 (heating rate: 10°C/min).

DA3 accelerates as curing starts. It is very likely that the outgassing species in DA2 is reactive diluent, which has a lower weight loss rate when the reaction starts. But for DA3, outgassing is a non-reactive solvent, and possibly with other reactive species. The non-reactive solvent has a boiling point at 172.9oC, as verified in the DSC. Heat generated in the curing process accelerates evaporation of the solvent. The continuous, slow release outgassing amount during ramp and curing at 180oC explains the formation of small voids in DA2, while fast evaporation of solvent accounts for large voids in DA3. To reduce or eliminate voids during thermal curing, a simple and the most common approach is to use a two-step (or multi-step) cure. The first step is designed to remove volatiles, followed by a second step of curing. With the first step at 120oC for 1h to remove more volatiles, DA2 shows significantly less voids for a die size of 6.4mm x 6.4mm [**FIGURE 3(h)**].

Ideally, the majority (if not all) of volatiles should be removed prior to the gelation point, which is defined as the intersection of G' and G" in a rheological test. Because the viscosity of die attach, materials increases dramatically after their gelation point. A higher amount of volatiles released after gelation point (or later stage of curing) are more likely to form voids. Therefore, the combined characterization of TGA and DSC, as well as rheological test, provides a good guideline to design optimal curing profiles to minimize or eliminate voids.

Summary

This article provides an understanding of void impact in die attach joints, the techniques to detect voids, voiding mechanisms, and their corresponding solutions. To eliminate voids, it is important to control the process to minimize moisture absorption and optimize a curing profile for die attach materials. TGA, DSC and Rheometer

are key analytical tools to optimize a curing profile to prevent voiding. In addition, many other properties such as modulus, coefficient of thermal expansion (CTE), and adhesion need to be considered when optimizing curing profiles. Last but not least, it is crucial to develop die attach materials with less outgassing and moisture absorption without compromising manufacturability, reliability and performance.

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Patterned wafer geometry grouping for improved overlay control

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Process-induced overlay errors from outside the litho cell have become a significant contributor to the overlay error budget including non-uniform wafer stress.

As ground rules shrink, advanced technology nodes in semiconductor manufacturing demand smaller process margins and hence require improved process control. Overlay control has become one of the most critical parameters due to the shrinking tolerances and strong correlation to yield. Process-induced overlay errors, from outside the litho cell, including non-uniform wafer stress, has become a significant contributor to the error budget. Previous studies have shown the correlation between process-induced stress and overlay and the opportunity for improvement in process control [1, 2]. Patterned wafer geometry (PWG) metrology has been used to reduce stress-induced overlay signatures by monitoring and improving non-litho process steps or by compensation for these signatures by feed forward corrections to the litho cell [3,4]. Of paramount importance for volume semiconductor manufacturing is how to improve the magnitude of these signatures, and the wafer to wafer variability. Standard advanced process control (APC) techniques provide a single set of control parameters for all wafers in a lot, and thereby only provide aggregate corrections on a per chuck basis. This work involves a novel technique of using PWG metrology to provide improved litho-control by wafer- level grouping based on incoming process induced overlay.

Wafer stress induced overlay is becoming a major challenge in semiconductor manufacturing, and the percentage contribution to the overlay budget is increasing. Addressing non-litho overlay is paramount to reducing wafer level variability. The amplitude of stress and the overlay budget differ by market segment. We observe from **FIGURE 1** that the 3D NAND, for example, has the largest magnitude of wafer shape induced stress, but also has a relatively large overlay budget of 8 to 20 nm. DRAM, on the other hand, has less stress, but has a much tighter overlay spec of 2 to 3 nm. The relative stress level and overlay budget dictate different process control use cases. For the case of 3D NAND, the improved overlay can be achieved using the PWG stress data for process monitoring as mentioned earlier, or by directly providing the stress based feed forward corrections to the litho cell [3, 4]. In this work, we will focus on the DRAM device application. Key topics include identifying process signatures in the shape data, and using those signatures to reduce within lot variability.

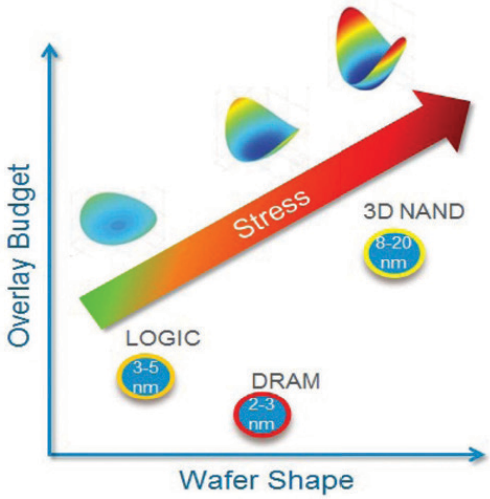

FIGURE 1. Wafer shape vs. overlay budget for advanced semiconductor processing. Each major technology sector (logic, DRAM, and 3D NAND) has different levels of stress and different overlay budgets.

Firstly, we will discuss the connection between wafer shape and overlay. During integrated circuit manufacturing many layers are printed on a silicon wafer. There is a critical need to align precisely pattern layers to an underlying pattern. This requirement is often complicated

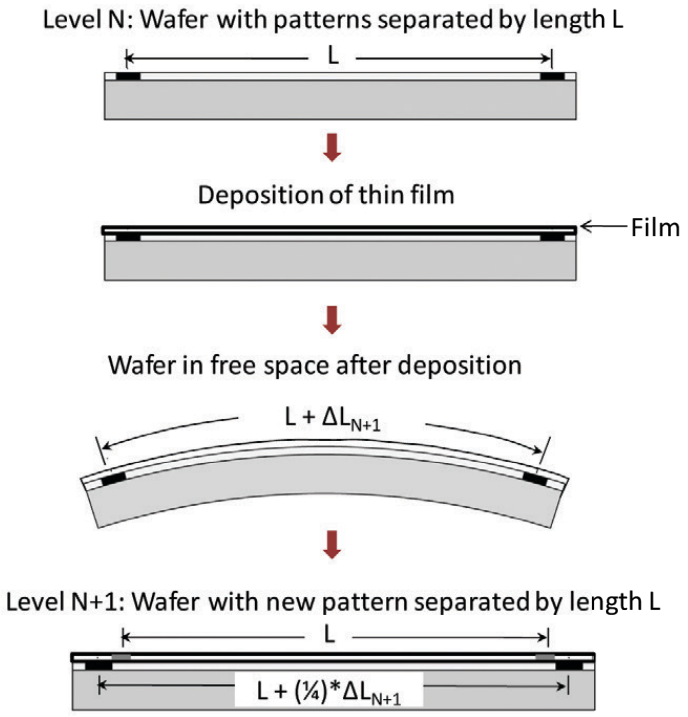

FIGURE 2. Illustration of the effect of film stress on wafer shape leading to overlay errors [6].

by process induced stress variations distorting the under-layer pattern, as illustrated in **FIGURE 2** [5, 6]. A reference layer pattern is formed at a certain level N (or layer N) and the pattern is initially defined by the characteristic length L shown. To form level N+1, a film is first deposited on top of level N. Film stress causes the wafer to warp in free-state resulting in a change to shape of wafer. This is typically manifested as both out-of-plane displacement (OPD) and in-plane displacement (IPD), affecting lateral placement of the under-layer pattern (level N). To print the level N+1 pattern the wafer is forced flat (e.g. lithography vacuum chucked). For the most part, chucking the wafer fully reverses the out-of-plane displacement but the in-plane displacement is only partially reversed. Thus, the under-layer pattern is now displaced relative to where it was originally printed. If level N+1 pattern is printed without correcting for the under-layer distortion, it results in misalignment or overlay error between the two layers. Such an overlay error is known as process-induced or process-stress induced overlay error and it can be caused by any type of stress inducing semiconductor process such as film deposition, thermal anneal, etch, CMP, etc.

Wafer shape is measured by a unique implementation of a dual-Fizeau interferometer on KLA-Tencor Corporation's WaferSight™ PWG patterned wafer geometry and nanotopography metrology system [7]. Simultaneous back side and front side measurements are made with the wafer in a vertical orientation to eliminate gravitational distortion.

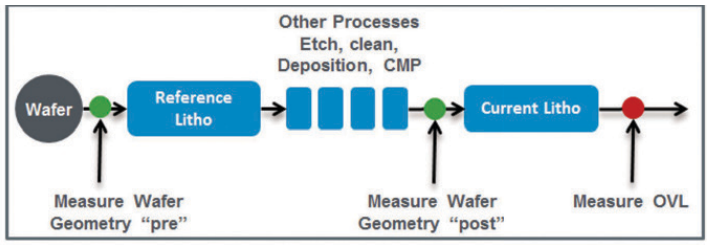

FIGURE 3. Metrology and processing sequence used for this investigation: Pre- and post-wafer geometry metrology, and post-litho overlay metrology.

Overlay is measured on a KLA-Tencor Corporation Archer™ 500 overlay metrology system using Archer AIM® optical imaging metrology targets.

It has been shown that process-induced overlay error can be accurately estimated from the change in shape induced by semiconductor processes [2, 6, 8, 9]. **FIGURE 3** shows a simplified schematic of a semiconductor process flow of a single layer. To estimate potential overlay error induced by processes between the reference lithography step (e.g. level N) and the current lithography step (e.g. level N+1), it is necessary to make wafer geometry measurement at the two indicated points in the figure as "pre" and "post", corresponding to before and after the shape or stress inducing process steps. Once wafer geometry measurements become available, the change in the shape induced by processing is calculated as the difference between two measurements. Process-induced overlay error can then be calculated from the shape change by using one of several algorithms that have been developed [2, 6, 8, 9]. In this paper, we use an advanced IPD algorithm based on two-dimensional plate mechanics for the accurate estimation of the process-induced overlay error referred to as GEN3 [2].

Shape based overlay for DRAM

As discussed previously, different semiconductor processes have varying levels of stress and different overlay error budgets, including 3D NAND, DRAM, logic, etc. These differences require different process control use cases, such as feedback, feed forward, grouping, etc., alone or in combination. In this work we describe an advanced grouping process control use case for DRAM in order to minimize overlay. For this investigation we look at a specific implementation of wafer grouping which is appropriate to R&D environments and ramp-up of high volume manufacturing (HVM) called here send-ahead grouping (SG). The more general grouping use case for HVM will be addressed in a future report.

In order to meet the tight overlay specifications for the next generation DRAM devices, a send-ahead grouping

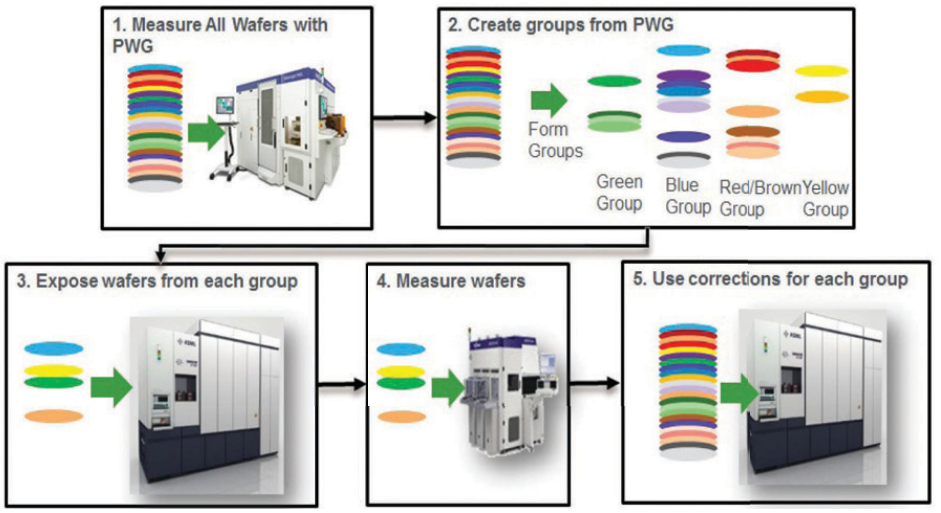

FIGURE 4. Shape based overlay control grouping use case for DRAM R&D and process ramp.

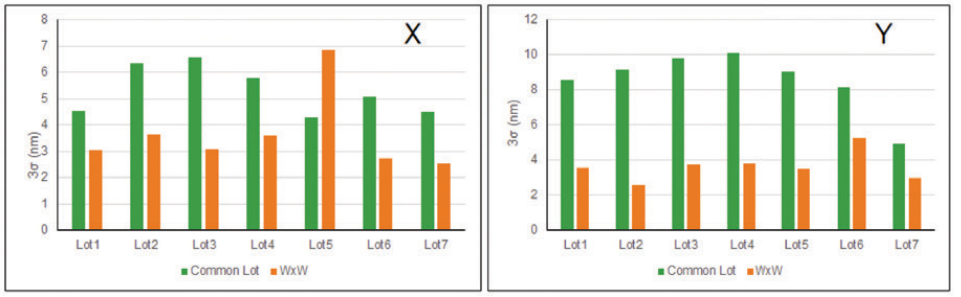

FIGURE 5. Overlay budget breakdown analysis by a rigorous ANOVA to quantify wafer-by-wafer variability: 3σ in nm for X and Y directions.

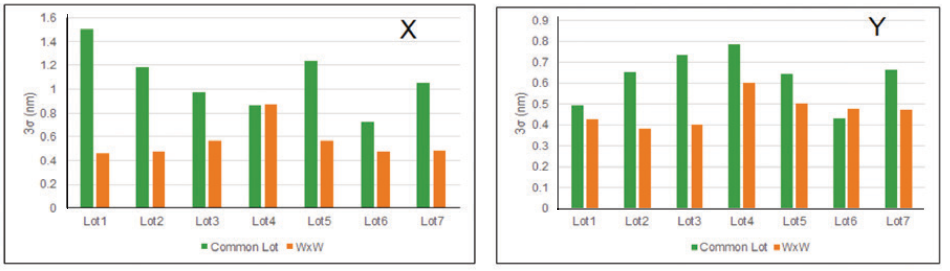

FIGURE 6. Budget Breakdown Analysis of the predicted overlay using wafer shape data: 3σ in nm for X and Y directions.

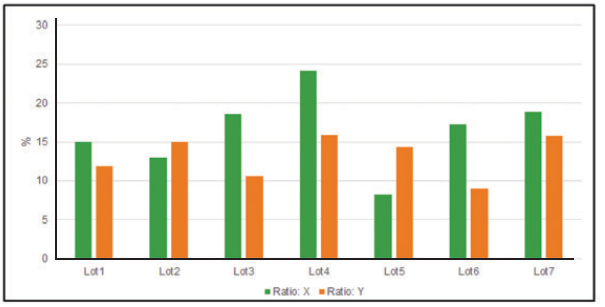

FIGURE 7. Ratio % of the shape WxW variability to the total overlay WxW variability by lot for X and Y.

(SG) based on the shape data has been evaluated. The flow of the proposed SG is outlined in **FIGURE 4**. Firstly, all the wafers in a lot are measured with a PWG tool for both "pre" and "post" layers. The shape data from the difference of these measurements is then used in the GEN3 algorithm to determine stress or shape based predicted overlay. The wafers are then grouped by similarity of wafer signatures. Grouping optimization is performed using the predicted overlay after removing the POR scanner alignment model. The grouping optimization: (i) decides the optimal number of process signatures; (ii) identifies the process signatures; and, (iii) provides a list of recommended wafers for metrology and exposure (step 2 in Fig. 4). The selected wafers are then exposed by the scanner in step 3 and the overlay measurement is performed in step 4. Finally, the correctable coefficients for each group will be calculated separately using the overlay metrology data. The exposed wafers will be reworked and then the entire lot will be exposed using the group by group corrections.

Within lot variability

The work is aimed at reducing the within lot variability. The within lot variability or wafer by wafer (WxW) variability is becoming one of the most important challenges to achieve tight overlay specifications for next generation DRAM devices. First we quantify within lot variability for both the shape and the overlay data using a rigorous analysis of variance (ANOVA). We analyzed seven lots individually and the results for both the overlay and PWG data are presented in **FIGURES 5** and **6** respectively. The overlay data show an average of 3.6 nm WxW variation in both the X and Y direction. The shape based overlay average within lot variation is 0.55 nm in X and 0.46 nm in the Y direction.

It should be noted that the within lot variation of the overlay data is comprised of different sources and the shape based overlay explains only part of the total within lot overlay variation. **FIGURE 7** shows the ratio % of the within lot variation shape based overlay versus the total overlay for both the X and Y

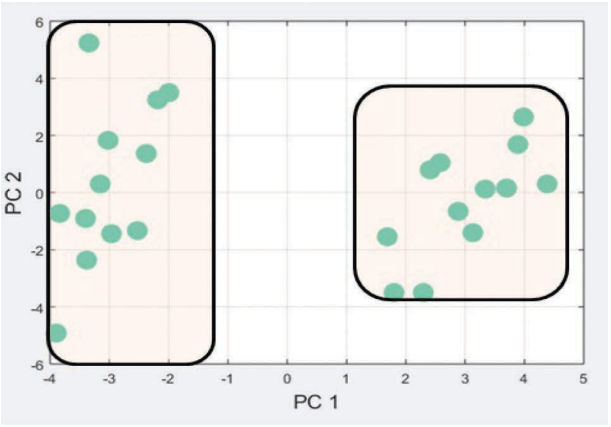

FIGURE 8. Identification of shape signatures based on PCA: two populations are clearly visible.

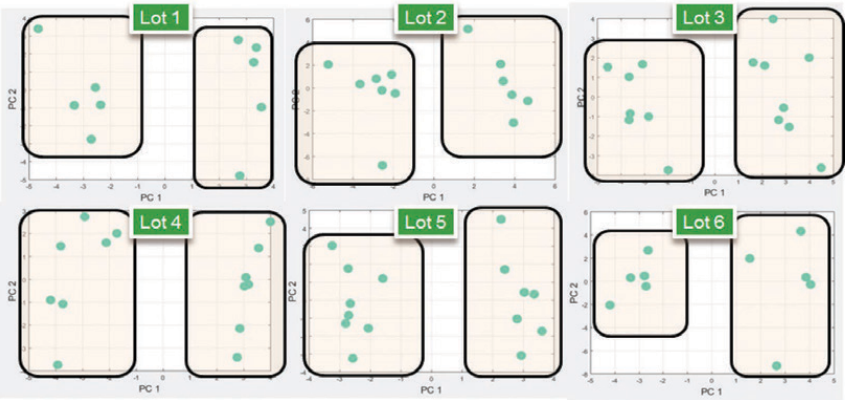

FIGURE 9. PCA analysis for the other lots. Shape data successfully captures the process context.

direction. It can be seen that shape overlay can explain as much as up to 25% of the total overlay variability. These findings indicate that minimizing the impact of stress based overlay, from processes outside the litho cell, will provide potentially significant improvement, which is critical in the drive towards 2 nm overlay.

DRAM clustering results

For all of the analyses presented in this study, the GEN3 algorithm was used to calculate stress based overlay. To perform grouping the scanner alignment model was first removed from the stress based overlay for each wafer. The alignment removes some of the within lot variations, however, wafer level alignment is not sufficient to remove all the wafer level variations. One useful way to visualize data variation is by performing Principle Component Analysis (PCA) of the data. By performing PCA, we express data in terms of Eigen functions of the covariance matrix of the data. Eigen values of the covariance matrix are calculated such that the first principle component explains the largest variation of the data, the second explains the second largest variation and so on. The coefficient for each principle component (PC) is referred to as the score. **FIGURE 8** shows scores for the PC1 (first principle component) versus the PC2 (second principle component) for all the wafers for a single lot using stress based overlay. Two distinct groups, indicating two distinct process signatures can clearly be observed in this lot.

The same analysis was performed for the rest of the six lots as shown in **FIGURE 9**. For all the lots in this example, two signatures can clearly be observed in their leading scores plot. Some excursion wafers were removed from the analysis. After observing these clear process signature groupings, it was confirmed that the signatures correspond to the two stages of a process tool. This clearly proves that the stress overlay grouping method can successfully identify and distinguish significant process signatures. It should be noted that in the general case the optimal number of groups would not necessarily be two.

We quantified the stress overlay grouping by performing comprehensive send-ahead grouping (SG) simulation study. Grouping optimization was performed using the shape data to select optimal number of groups and also the send-ahead wafers for processing and metrology. Then using the send-ahead wafers for each group, ideal corrections were simulated and applied to each group in the lot. From the composite group residual, $|\text{mean}|+3\sigma$ for each wafer was recorded. The residual $|\text{mean}|+3\sigma$ was also calculated using the standard plan of record (POR) wafers. The root mean square for the average of the $|\text{mean}|+3\sigma$ for X and Y is compared between SG and POR in **FIGURE 10**. The average $|\text{mean}|+3\sigma$ improved by more than 0.5 nm using the SG solution.

The range is defined as the difference of the maximum and minimum $|\text{mean}|+3\sigma$ per lot for both the X and Y direction. **FIGURE 11** shows the comparison of the RMS of X and Y ranges for the six lots. The range has been improved by about 1 nm, underscoring the benefit of controlling wafer level variation by using shape data to identify signatures and group wafers for exposure and metrology.

Conclusions

Process induced overlay errors from outside the litho cell have become a significant contributor to the overlay error budget. It is no longer sufficient to focus exclusively on litho cell overlay improvement. Addressing non-litho overlay is key to reducing wafer level variability. We demonstrated a novel technique of using PWG metrology

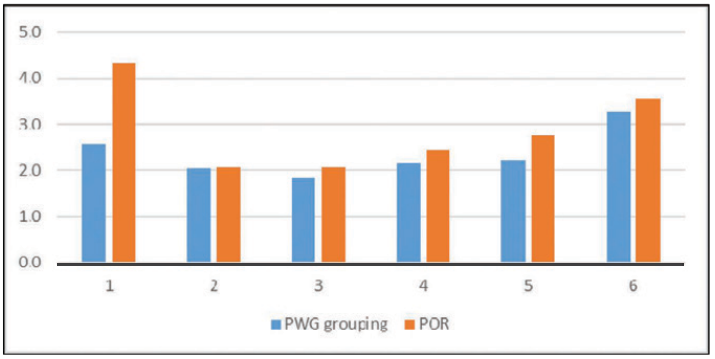

FIGURE 10. Improvement of wafer-by-wafer variability: average of |mean| + 3s by lot resulting in > 0.5 nm average improvement.

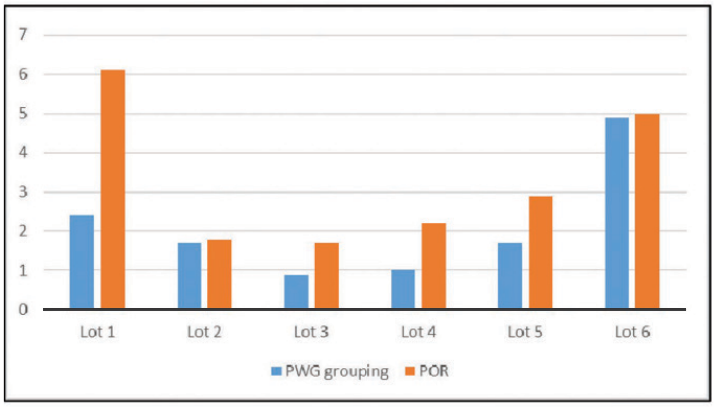

FIGURE 11. Improvement of wafer-by-wafer variability: range of |mean| + 3s by lot resulting in > 1.0 nm range improvement.

to provide improved litho control by wafer-level grouping based on incoming process induced overlay in a 19 nm DRAM manufacturing process driving towards a 2 nm overlay budget. Wafer to wafer variability range was reduced by around 1 nm across the lots in this study. Future directions include a full HVM implementation of the grouping methodology.

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Capturing future sources of profitable growth

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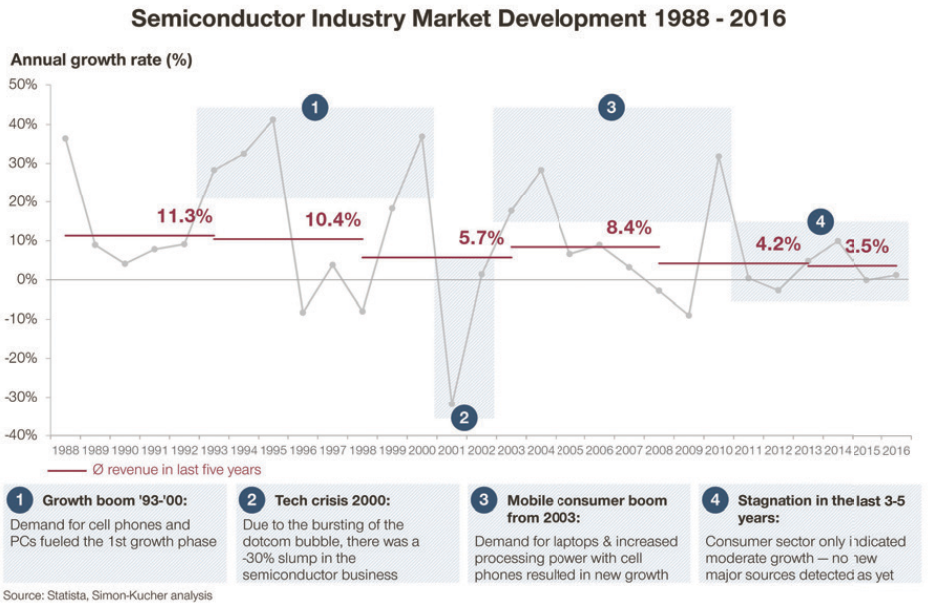
The semiconductor industry is facing key challenges. In recent years, M&A mega deals have led to consolidations within the market, while the industry continues to mature. This leaves rather moderate growth prospects for the next three years. Semiconductor companies will have to consistently farm limited organic growth sources whilst at the same time tapping into new and growing macrotrends. To be successful in the long term, they must recognize the potential of the disruptive technologies and new markets that the Internet of Things will bring.

How can companies relive the previous successes in the mobile consumer segment?

In the 1990s and even early 2000s, growth booms in the industry with annual sales growth of 30 to 40 percent were the norm. Thanks to the sharply increasing demand in the consumer market for PCs, laptops and mobile phones, many smaller technology companies were able to grow into giants in the semiconductor business (**FIGURE 1**). However, since 2011, the industry has had to manage its growth expectations for the consumer market. With an average annual growth rate of 3.4 percent expected from 2015 to 2020, the strong growth period seems to be over and the dynamic start-up atmosphere of the past appears to be more or less history. The entire industry already has a market size of over 350 billion euros, with intense rigid competition among existing players. M&A mega deals (**FIGURE 2**) such as Qualcomm-NXP, Avago-Broadcom, Softbank-ARM and Western Digital-SanDisk have severely consolidated the market and now these companies are deep in operations integration and rationalization mode.

Is this the end of the period of constant growth outperformance? Not at all. Simon-Kucher project experience tells us that even organic growth sources based on dynamic market trends can be tapped, meaning companies can relive the successes in the mobile consumer sector. However, two fundamental strategic questions need to be answered: Where will these new growth waves come from?



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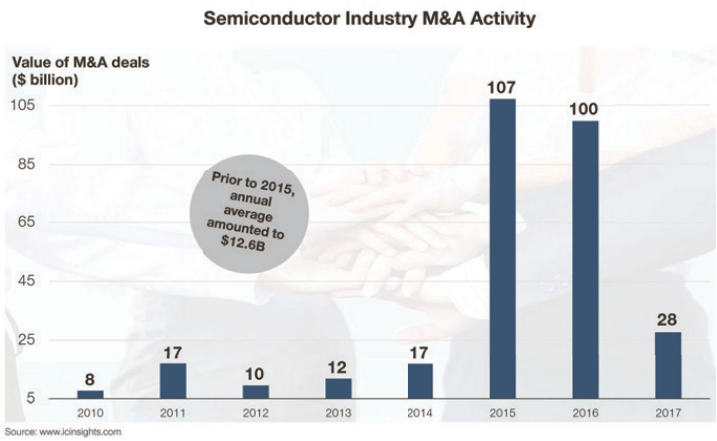
And how can the imminent stagnation be avoided? We have identified three sources of organic growth that will play a pivotal role in the future of the semiconductor industry.

1.Exploit new disruptive technologies such as silicon carbide

Semiconductors based on silicon carbide (SiC) represent a strong area for future growth. Compared to semiconductors made of regular silicon, SiC-based semiconductors can operate at much higher frequency and temperature and convert electric power at lower losses, promising increased speed, robustness and efficiency. SiC devices are capable of managing the same power level as Si devices at half the size, boosting power density and reliability.

While a handful of players have already secured a favorable starting position in the market, there continues to be strong medium-term growth forecasts which means that the current market



volume in this emerging product segment (~$200 million) still offers attractive entry potential for second and third movers. Several suppliers such as Dow Corning and Nippon Steel have entered and increased activity in the SiC market while companies such as Wolfspeed/Cree are experiencing decline in market share. This goes to show that there is still room to wrangle for territory.

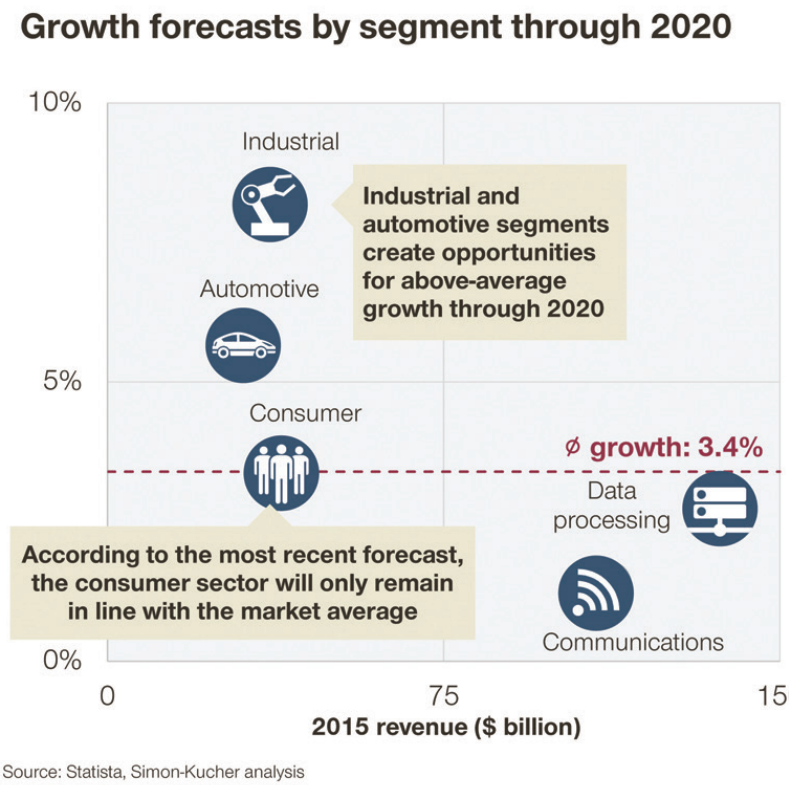
We anticipate that hype will become mass reality within the next five to eight years, particularly driven by the growing demand in hybrid and electric mobility, regenerative power generation and industrial applications. Notably, SiC may have a huge impact on the automotive industry, in particular on electric vehicles and e-mobility due to the high efficiency levels. In each of these markets, customers continue to demand and expect smaller wafers and devices with increasingly better performance profiles than Si-based devices, made possible by SiC technology. According to a recent Simon-Kucher study, global demand in the SiC technology segment and its sister technology gallium nitride (GaN) will amount to more than three billion euros by 2025, with double-digit annual growth rates. Industry analysts note that SiC has gradually emerged as "mainstream" material since 2016 which will result in drop in prices for devices from 2018 onwards. This would translate to possibly large increases in volume demand.

At the moment, the technology is still relatively cost-intensive and more complex in production primarily due to lack of scale. As such, SiC and GaN remain niche markets for now. However, having achieved first significant design-wins, first-moving companies are proof of the future market potential. The remaining semiconductor companies need to adapt their innovation strategies or risk trailing the pack. To successfully implement SiC and GaN system solutions, it is essential to closely orient new product development towards emerging market needs, starting from initial development phases. Here, semiconductor companies have to identify the applications where customers already demand high switching voltage and speed, low switching losses, and a small size and weight. Only in doing so can they expect customer-oriented market success from design-in to design-win.

2. Anticipate and seize new markets materializing from the Internet of Things

The Internet of Things (IoT) has now become the catch-all phrase that encapsulates an enormous spectrum of potential applications and markets revolving around interconnected physical devices and appliances. As it continues to evolve and numerous markets around it become commercially viable, semiconductor companies have a huge opportunity to capture the underlying profit pools. By some accounts, something like 3 billion new IoT-enabled devices are manufactured per year; at the most rudimentary level, each of these devices require microcontrollers, sensors, actuators and a whole host of other semiconductor-enabled parts. Another indirect area of growth for semiconductor companies will likely emerge from the fact that the exponentially increasing amount of data generated by IoT products need to be processed and stored. This will lead to demand for more server farms and greater storage capacities.

IoT products and applications would not be possible without the continued advancements in semiconductor technology, and the demand for inexpensive chips that can be mass-produced will only continue to increase. Rather than



Source: Statista, Simon-Kucher analysis

spectating and reacting to this market macrotrend from the sidelines, semiconductor companies should see the IoT as an integral part of the future market's DNA.

The current challenge is the fragmented nature of the market, with no clear "killer application" or common platform; rather, there is a multitude of smaller niche opportunities that in its entirety promise overall attractive growth potential. No player has yet been able to establish a market-dominant position in this highly diversified market. There are, however, specific end-markets that have taken the lead (for now) in terms of showing promise of growth, such as smart home applications, consumer wearables (e.g. fitness bracelets, smart watches), medical electronics, and connected cars (**FIGURE 3**). The IoT will turn these individual niche segments into potential game-changers for the semiconductor industry.

Amid these fast-evolving segments, critical for the success of semiconductor companies is their agility in swiftly responding to emerging trends and integrating hardware and software components along the value chain and ultimately, offering a seamless IoT solution. Semiconductor companies already focusing on seamless security, communication intelligence and user-friendliness are a step ahead in strengthening their position. To not be left behind, semiconductor companies need to make the strategic decision of prioritising resources and investments into IoT-related growth sources and resist the inertia and temptation to solely rely on existing "bread and butter" revenue streams, regardless of how healthy the current margins are. Related to this, to get serious about this emerging opportunity, semiconductor companies should not view the IoT markets as a nebulous concept with opportunistic revenue streams, but rather conduct in-depth analyses of their current position within the changing value chains and competitive landscape to formulate concrete go-to-market plans.

3. Shift from component-centric sales to supplying system solutions

Finally, a third dimension of growth beyond new products and new markets for semiconductor companies is to move up the value chain. Increasingly, leading market players are integrating chips, drivers, software and sensors to offer partial system solutions, with the ultimate objective of being ecosystem enablers. Naturally, this requires the capability to not only sell hardware (semiconductors, wafers, etc.) but an entire system and services around it that several entities from different industries can utilise to establish their own IoT products. However, for companies traditionally built around selling components, doing this successfully is not a straightforward undertaking. Many sales forces are finding themselves lacking the organisational setup and solution-selling approach critical for success. In addition, in order to integrate products in the portfolio into systems solutions, companies have to establish effective cross-industry channel management on the sales front and at the same time develop strong alliances with partners along the value chain to ensure a stable ecosystem. Successful players will be those in the market with the capability to provide modular solutions that can readily interlink products with security, software and system consulting services.

As a result, we believe that the desire of companies to move towards being system suppliers and ecosystem enablers will further increase M&A activity due to the need to acquire specialised knowledge. Notably, Intel has acquired three companies within the space of a year from different parts of the industry to assimilate specific expertise related to IoT i.e. Altera (designer and manufacturer of programmable logic devices), Nervana Systems (artificial intelligence software developer) and Itseez (specialist in computer vision technology and algorithms).

In summary, despite some notions otherwise, we are bullish about the imminent growth potential in the semiconductor market driven by very powerful macrotrends in product technology, emerging applications and also value chain shifts. Semiconductor companies thirsty for new waves of exponential growth would do well to heed the signposts from these trends and re-orient their product development, industry alliances and sales approaches rapidly in order to capitalise on these opportunities before the winner takes all.

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