MARCH 2018

Extension MED

Α

Insights for Ele

EUV Adds to Increasing Hydrogen Demand P. 18

The (Automotive) **Problem** with **Semiconductors** P. 23

Making the Most of Color in Multi-Patterning Layouts P. 26





www.solid-state.com



May 20 - 23, 2018 THE COSMOPOLITAN of LAS VEGAS

& Design Executive Conference

Connect with Industry Leaders

- Key topics on: Semiconductor Manufacturing and Design | Economics, Trends, New Technologies and Applications | Mainstream Semiconductor Manufacturing | plus Artificial Intelligence, IoT, 5G, EUV Lithography, Advanced Packaging, Virtual and Augmented Reality, Automotive, Cloud Computing, Networking, Healthcare | Market Trends and Expected Business Climate Moving Forward
- Hear from outstanding leaders at: Google, IBM, Qorvo, Nvidia, GLOBALFOUNDRIES, Qualcomm, Cisco, ASE, Silicon Catalyst, Skywater Technology Foundry, IHS Markit, Semico Research, Siemens, ULVAC
- The ConFab 2018 connects key decision-makers, clients, colleagues, partners, suppliers and analysts in conference sessions and multiple networking breakfasts, lunches, cocktail receptions and private meetings. Don't miss a valuable opportunity to meet face-to-face.

LEVERAGE THIS NEW ERA IN SEMICONDUCTOR GROWTH! 2018 VISIONARY SPEAKERS



Dr. Rama Divakaruni IBM Distinguished Engineer Advanced Process Technology Research



Howard Witham

VP of Texas Operations

OORVO

John M. Martinis Google Quantum AI Lab Worster Chair, Univ. of California Santa Barbara, Experimental Physics



George Gomba VP of Technology Research GLOBALFOUNDRIES



Dr. John Hu Director of Advanced Technology Nvidia Corporation



Bill von Novak Wireless Power Group Lead **OUALCOMM**

RESERVE NOW - SEATING LIMITED www.theconfab.com







The ConFab 2018 Conference Chair

Solid State Technology Editor-in-Chief, Pete Singer

Solid State TECHNOLOGY

MARCH 2018 VOL. 61 NO. 2

imec and Cadence tape out industry's first 3nm test chip (pg. 6)

FEATURES



RELIABILITY Mechanism and improvements of Cu voids under via bottom

This work explores the effect of underlying metallic alloys and the influence of Cu loss under via bottom after dry etching and wet cleaning processes. To Improve the Cu loss under via bottom, effective approaches are proposed. The modified actions for via bottom improve not only wafer yield but also reliability of the device.

Cheng-Han Lee and Ren-Kae Shiue, Department of Materials Science and Engineering, National Taiwan University, Taiwan, ROC



MATERIALS | EUV Lithography adds to increasing hydrogen demand at leading-edge fabs

On-site production an option for supply. Dr. Paul Stockman, Linde Electronics, Stewartsville, NJ

	\frown	
(
	23	

PROCESS WATCH | The (automotive) problem with semiconductors

Some of the challenges involved in the automotive supply chain are introduced. Future articles in the series will address specific process control solutions to those challenges.





EDA Making the most of color in your multi-patterning layouts

There are many different situations in which special attention to color choices provide the potential to improve the manufacturing results of multi-patterned masks.

David Abercrombie and Alex Pearson, Mentor Graphics, Wilsonville, OR

COLUMNS

- 2 Editorial AI focus of The ConFab, Pete Singer, Editor-in-Chief
- 10 Packaging Samsung starts production of Gen-2 HBM2 Phil Garrou, Contributing Editor
- 11 Semiconductors imec and Cadence tape out industry's first 3nm test chip
- 31 **Industry Forum** New insights from failures, Guido Groeseneken, imec fellow

DEPARTMENTS

- Web Exclusives Δ
- 6 News
- 30 Ad Index



editorial

AI focus of The ConFab

Artificial Intelligence will be a focus of The ConFab 2018, to be held May 20-23 at The Cosmopolitan of Las Vegas. We'll hear from a variety of speakers on why A.I. is so important to the semiconductor industry, not only in terms of the new types of chips that will be required, but how A.I. will bring dramatic improvements to the semiconductor manufacturing process.

"The exciting results of AI have been fueled by the exponential growth in data, the widespread availability of increased compute power, and advances in algorithms," notes Rama Divakaruni of IBM, our keynote speaker. "Continued progress in AI - now in its infancy - will require major innovation across the computing stack, dramatically affecting logic, memory, storage, and communication."

Rama will explain how the influence of AI is already apparent at the system-level by trends such as heterogeneous processing with GPUs and accelerators, and memories with very high bandwidth connectivity to the processor. The next stages will involve elements which exploit characteristics that benefit AI workloads, such as reduced precision and in-memory computation. Further in time, analog devices that can combine memory and computation, and thus minimize the latency and energy expenditure of data movement, offer the promise of orders of magnitude power-performance improvements for AI workloads.

John Hu, Director of Advanced Technology, Nvidia Corporation will also address AI in a talk titled "The Era of Deep Learning IC Industry Driven by AI, Autonomous Driving and Virtual Reality." Hu notes that the "big bang" of AI and autonomous driving has driven the IC industry into a new era of rapid growth and innovation. In his talk, Hu will describe how the next 1000 times of improvement requires a new paradigm shift in the collaboration and co-optimizations across the whole industry; from materials, process technologies, design and chip/system platform. In this era that machine(s) can improve themselves by deep learning, hear how the semiconductor industry also needs to have the capability of deep learning for innovation, to stay ahead in the changing competitive landscape.

"Artificial intelligence has brought human beings to a point in history, for our industry and the world in general, that is more revolutionary than a small, evolutionary step," says Howard Witham, Vice President of Texas Operations at Qorvo, who will speak on the potential of AI in the semiconductor fab. Howard will describe how AI provides predictive maintenance, auto defect and wafer map classification, outlier detection, automated recipe setups based on device requirements and upstream data, and dynamic interpolation and guard-banding.

Please join us for these and other insightful talks, including one from Google's John Martinis on quantum computing. Visit www.theconfab.com for more information.

-Pete Singer, Editor-in-Chief

Solid State TECHNOLOGY.

Pete Singer, Editor-in-Chief Ph: 978.470.1806, psinger@extensionmedia.com

Shanon Davis, Editor, Digital Media Ph: 603.547.5309 sdavis@extensionmedia.com

Ed Korczynski, Senior Technical Editor, edk@extensionmedia.com

Dave Lammers, Contributing Editor

Phil Garrou, Contributing Editor

Dick James, Contributing Editor Vivek Bakshi, Contributing Editor CREATIVE/PRODUCTION/ONLINE Marjorie Sharp, Production Traffic Coordinator

Nicky Jacobson, Senior Graphic Designer

Simone Bradley, Graphic Designer Slava Dotsenko, Senior Web Developer

MARKETING/CIRCULATION Jenna Johnson, jjohnson@extensionmedia.com

CORPORATE OFFICERS

Extension Media, LLC Vince Ridley, President and Publisher vridley@extensionmedia.com

Clair Bright, Vice President and Publisher Embedded Electronics Media Group cbright@extensionmedia.com

For subscription inquiries: Tel: 847.559.7500; Fax: 847.291.4816; Customer Service e-mail: sst@omeda.com; Subscribe: www.sst-subscribe.com

MARCH 2018 VOL. 61 NO. 2 • Solid State Technology ©2018 (ISSN 0038-111X) Subscriptions: Domestic: one year: \$258.00, two years: \$413.00; one year Canada/Mexico: \$360.00, two years: \$573.00; one-year international airmaii: \$434.00, two years: \$691.00; Single copy price: \$15.00 in the US, and \$20.00 elsewhere. Digital distribution: \$130.00. You will continue to receive your subscription free of charge. This fee is only for air mail delivery. Address correspondence regarding subscriptions (including change of address) to: *Solid State Technology. 1786* 18th Street, San Francisco, CA 94107-2343. (8 am – 5 pm, PST). Solid State Technology is published eight times a year by Extension Media LLC, 1786 Street, San Francisco, CA 94107. Copyright © 2018 by Extension Media LLC. All rights reserved. Printed in the U.S.



1786 18th Street San Francisco, CA 94107



JUNE 26-28 2018 EXHIBIT DATES JUNE 27-28

McEnery Convention Center SAN JOSE, CA





THE INDUSTRY'S LARGEST EVENT DEDICATED TO Sensors, Connectivity, And Systems.

Sensors Expo & Conference is where you'll find the best of the best in the sensors industry, along with new and innovative ways to jump start your sensor solutions. Be a part of the ONLY event where technologists find opportunities and engineers innovate solutions. This year's event features three exciting days of all-new Pre-Conference Symposia, Conference Technical Sessions across 10 updated tracks, visionary Keynote Presentations, Networking Events, Exhibits, and much more!



6,500+ ATTENDEES // 300+ EXHIBITORS // 100+ SPEAKERS // 65+ CONFERENCE TECHNICAL SESSIONS // 5 PRE-CONFERENCE SYMPOSIA // 2 KEYNOTES



f 🕑 💿 (in

INDUSTRY SPONSOR

MEDIA

CO-LOCATED WITH





Register today! Use code EXT100 for \$100 off

Use code **EXT100** for \$100 off Conference Passes or a FREE Expo Hall Pass!

*Discount is off currently published rates and cannot be combined with other offers or applied to previous registrations.

Sensors

Online@www.solid-state.com

Web Exclusives

Entering 2018 on solid ground

2017 finished on an upturn – both in the USA and globally. Based on consolidated fourth-quarter actual and estimated revenues of 213 large, global electronic manufactures, sales rose in excess of 7 percent in 4Q'17 vs. 4Q'16.

http://bit.ly/2ox3Eoj

Testing: The key to Al-enabled autonomous driving

Since 2010, 474 companies have poured \$51 billion into developing products enabled by artificial intelligence (AI), with the bulk of these investments targeting autonomous driving and in-vehicle experiences, according to the McKinsey reports. With AI and automotive electronics promising massive growth potential, it's no surprise that IHS Market predicts the Advance Driver Assistance Systems (ADAS) market will reach \$67.43 billion by 2025 and that, by 2040, 33 million AI-enabled autonomous vehicles will be on the road worldwide.

http://bit.ly/2F2kulc

3D depth sensing & VCSEL technology surges: Key takeaways from SEMI Member Forum

Since Apple unveiled iPhone X with face-recognition functionality in early November 2017, interest in 3D sensing technology has reached fever pitch and attracted huge investments across the related supply chains. The global market for 3D depth sensing is estimated at US\$1.5 billion in 2017 and will grow at a CAGR of 209 percent to US\$14 billion in 2020, Trendforce estimates.

http://bit.ly/2Hw3o0H

Integrated circuit technology advances continue to amaze

The success and proliferation of integrated circuits has largely hinged on the ability of IC manufacturers to continue offering more performance and functionality for the money. http://bit.ly/2FG9ZFc



Latest on EUV source technology: Highlights from 2017 Source Workshop

As we look forward to 2018 SPIE Advanced Lithography conference, it is good to review the current status and recent development for EUV source technology. In this blog, Vivek Bakshi presents the latest status on EUV source technology from the 2017 Source Workshop, held last November at UCD in Dublin.

http://bit.ly/2FfmmKN

Insights from the Leading Edge: SEMI ISS: Market opportunities and drivers

Let's take a look at some of the presentations given at the SEMI ISS (Industry Strategy Symposium) conference in January at Half Moon Bay. http://bit.ly/2CNUJ5Z

Insights from the Leading Edge: SEMI ISS Part 2

Finishing up our look at the 2018 SEMI ISS meeting, let's take a look what John Hunt, ASE, had to say about the "Transformative Power of Fan-Out."

http://bit.ly/2GRc8xa

North American semiconductor equipment industry posts January 2018 billings

"The strong billings levels from late 2017 have carried over into the new year," said Ajit Manocha, president and CEO of SEMI.

http://bit.ly/2FG6EGj



MARCH 14–16, 2018 SNIEC, SHANGHAI, CHINA

跨界全球 · 心芯相联 CONNECT · COLLABORATE · INNOVATE

For the past 30 years, SEMICON China has witnessed the robust growth of China's semiconductor industry and is the premier place to connect with the companies, people, products, and information shaping the future of design and manufacturing of microelectronics—all at SEMICON China and FPD China 2018!

- The entire semiconductor industry ecosystem, including device manufacturing, equipment, materials, assembly and test services, design, and more.
- The premier platform for exploring and discussing cutting-edge technologies with engineers, executives, and experts from around the world.
- Connect and engage suppliers, partners, and customers.
- Expand your business opportunities with industry leaders.





Contact SEMI China Tel: +86.21.6027,8500

E-mail: semichina@semi.org

www.semiconchina.org



Please send news articles to sdavis@extensionmedia.com

worldnews

EUROPE – ClassOne

Equipment was selected by a major UK fab to upgrade its facilities.

USA - Brewer Science,

Inc. introduced its OptiLign commercial-quality directed self-assembly (DSA) material set developed in collaboration with **Arkema**.

EUROPE -

STMicroelectronics and Sigfox announced a collaboration agreement to support and accelerate the growing demand for connected devices.

ASIA - Air Products

announced an agreement to supply **Samsung Electronics'** second 3D V-NAND fab in western China.

USA - Supermicro

announced an expansion of its Silicon Valley corporate headquarters.

ASIA - Gigaphoton announced the shipment of its latest ArF Excimer Laser GT65A.

EUROPE - imec presented initial electrical results on N5 32nm pitch metal-2 layer at 2018 SPIE Advanced Lithography Conference.

ASIA - Seoul Semiconductor filed a third patent infringement litigation against Mouser for sale of Everlight products in Italy.

USA - Peter Trefonas, Ph.D., corporate fellow in **Dow Electronic Materials**, has recently been elected a Fellow of **SPIE**, for achievements in design for manufacturing and compact modeling.

ASIA - Samsung Display and Universal Display Corporation entered into long-term OLED agreements.

Samsung Electronics breaks ground on new EUV line in Hwaseong

Samsung Electronics announced that it broke ground on a new EUV (extreme ultraviolet) line in Hwaseong, Korea.

With this new EUV line, Samsung will be able to strengthen its leadership in single nanometer process technology by responding to market demand from various applications, including mobile, server, network, and HPC (high performance computing), for which high performance and power efficiency are critical.

The new facility is expected to be completed within the second half of 2019 and start



Samsung Electronics Hwaseong Campus EUV line bird's eye view

production ramp-up in 2020. The initial investment in the new EUV line is projected to reach USD 6 billion by 2020 and additional investment will be determined depending on market circumstances.

"With the addition of the new EUV line, Hwaseong will become the center of the company's semiconductor cluster spanning Giheung, Hwaseong and Pyeongtaek in Korea," said Kinam Kim, President & CEO of Device Solutions at Samsung Electronics. "The line will play a pivotal role as Samsung seeks to maintain a competitive edge as an industry leader in the coming age of the Fourth Industrial Revolution."

Samsung has decided to utilize cutting-edge EUV technology starting with its 7-nanometer (nm) LPP (Low Power Plus) process. This new line will be set up with EUV lithography equipment to overcome nano-level technology limitations. Samsung has continued to invest in EUV R&D to support its global customers for developing next-generation chips based on this leading-edge technology.

imec and Cadence tape out industry's first 3nm test chip

The research and innovation hub in nanoelectronics and digital technologies, imec, and Cadence Design Systems, Inc. today announced that its extensive, long-standing collaboration has resulted in the industry's first 3nm test chip tapeout. The tapeout project, geared toward advancing 3nm chip design, was completed using extreme ultraviolet (EUV) and 193 immersion (193i) lithography-oriented design rules and the Cadence Innovus Implementation System and Genus Synthesis Solution. Imec utilized a common industry 64-bit CPU for the test chip with a custom 3nm standard cell library and a TRIM metal flow, where the routing pitch was reduced to 21nm. Together, Cadence

and imec have enabled the 3nm implementation flow to be fully validated in preparation for next-generation design innovation.

The Cadence Innovus Implementation System is a massively parallel physical implementation system that enables engineers to deliver high-quality designs with optimal power, performance and area (PPA) targets while accelerating time to market. The Cadence Genus Synthesis Solution is a next-generation, high-capacity RTL synthesis and physical synthesis engine that addresses the latest FinFET process node requirements, improving RTL designer productivity by up to 10X. For more information on the Innovus Implementation System, please visit www.cadence.com/go/innovus3nm, and to learn about the Genus Synthesis Solution, visit www.cadence. com/go/genus3nm.

For the project, EUV and 193i lithography rules were tested to provide the required resolution, while providing PPA comparison under two different patterning assumptions. For more information on EUV technology and 193i technology, visit https://www.imec-int.com/en/articles/imec-presentspatterning-solutions-for-n5-equivalent-metal-layers.



Post place and route layout of 21 nm pitch metal layers

"As process dimensions reduce to the 3nm node, interconnect variation becomes much more significant," said An Steegen, executive vice president for semiconductor technology and systems at imec. "Our work on the test chip has enabled interconnect variation to be measured and improved and the 3nm manufacturing process to be validated. Also, the Cadence digital solutions offered everything needed for this 3nm implementation. Due to Cadence's well-integrated flow, the solutions were easy to use, which helped our engineering team stay productive when developing the 3nm rule set."

"Imec's state-of-the-art infrastructure enables pre-production innovations ahead of industry demands, making them a critical partner for us in the EDA industry," said Dr. Chin-Chi Teng, corporate vice president and general manager in the Digital & Signoff Group at Cadence. "Expanding upon the work we did with imec in 2015 on the industry's first 5nm tapeout, we are achieving new milestones together with this new 3nm tapeout, which can transform the future of mobile designs at advanced nodes."

ing of Fan-Out Wafer Level Packaging

Vacuum Polymer Cure Oven

Automated. Flexible. Comprehensive.

- Shorter process time
- No trapped solvent/oxygen
- No outgassing at metallization

Cleaner Process. Cleaner Maintenance.



Yield Engineering Systems, Inc.

888-YES-3637

www.yieldengineering.com

newscont.

Top 10 semiconductor R&D spenders increase outlays 6% in 2017

The ten largest semiconductor R&D spenders increased their collective expenditures to \$35.9 billion in 2017, an increase of 6% compared to \$34.0 billion in 2016. Intel continued to far exceed all other semiconductor companies with R&D spending that reached \$13.1 billion. In addition to representing 21.2% of its semiconductor sales last year, Intel's R&D spending accounted for 36% of the top 10 R&D spending and about 22% of total worldwide semiconductor R&D expenditures of \$58.9 billion in 2017, according to the 2018 edition of The McClean Report that was released in January 2018. **Figure 1** shows IC Insights' ranking of the top semiconductor R&D spenders, including both semiconductor manufacturers and fabless suppliers.

Top 10 Semiconductor R&D Spenders (Companies with ≥\$1B in Spending)

2017 Rank	Company	R&D Exp (\$M)	R&D/Sales (%)	17/16 % Chg in R&D
1	Intel	13,098	21.2%	3%
2	Qualcomm	3,450	20.2%	-4%
3	Broadcom*	3,423	19.2%	4%
4	Samsung	3,415	5.2%	19%
5	Toshiba	2,670	20.0%	-7%
6	TSMC	2,656	8.3%	20%
7	MediaTek*	1,881	24.0%	9%
8	Micron	1,802	7.5%	8%
9	Nvidia	1,797	19.1%	23%
10	SK Hynix	1,729	6.5%	14%
	Top 10 Total	35.921	13.0%	6%

Source: Company reports, IC Insights' *Strategic Reviews* database *Sales and R&D spending of acquired semiconductor supplier are included.

FIGURE 1.

Intel's R&D expenditures increased just 3% in 2017, below its 8% average annual growth rate since 2001, according to the new report. Still, Intel's R&D spending exceeded the combined R&D spending of the next four companies— Qualcomm, Broadcom, Samsung, and Toshiba—listed in the ranking.

Underscoring the growing cost of developing new IC technologies, Intel's R&D-to-sales ratio has climbed significantly over the past 20 years. In 2017, Intel's R&D spending as a percent of sales was 21.2%, down from an all-time high of 24.0% in 2015. In 2010, the ratio was 16.4%, 14.5% in 2005, 16.0% in 2000, and just 9.3% in 1995.

Qualcomm—the industry's largest fabless IC supplier—was again ranked as second-largest R&D spender, a position it first achieved in 2012. Qualcomm's semiconductor-related R&D spending was down 4% in 2017, after a 7% drop in 2016, and it was close to being passed up by third place Broadcom and fourth placed Samsung, whose R&D spending increased 4% and 19%, respectively.

Despite increasing its R&D expenditures by 19% in 2017, Samsung had the lowest investment-intensity level among the top-10 R&D spenders with research and development funding at 5.2% of sales last year. Samsung's 49% increase in semiconductor revenue in 2017 (driven by strong growth in DRAM and NAND flash memory) lowered its R&D as a percent of sales ratio from 6.5% in 2016. Micron Technology's revenues surged 77% in 2017, but its research and development expenditures grew 8%, resulting in an R&D/sales ratio of 7.5% compared to 12.5% in 2016. Similarly, SK Hynix's sales climbed 79% in 2017, while its research and development spending increased 14% in the year, which resulted in an R&D/sakes ratio of 6.5% versus 10.2% in 2016.

Fifth-ranked Toshiba and sixth-ranked Taiwan Semiconductor Manufacturing Co. (TSMC) each allocated about the same amount for R&D spending in 2017. Toshiba's R&D spending was down 7% while TSMC had one of the largest increases in R&D spending among the top 10 companies shown in the figure. TSMC's R&D expenditures grew by 20% as the foundry raced rivals Samsung and GlobalFoundries in launching new process technologies, while its sales rose 9% to \$32.2 billion in the year.

Rounding out the top-10 list were MediaTek, Micron, Nvidia, which moved from 11th place in 2016 to 9th position to displace NXP in the 2017 ranking, and SK Hynix. Collectively, the top-10 R&D spenders increased their outlays by 6% in 2017, two points more than the 4% R&D increase for the entire semiconductor industry. Combined R&D spending by the top 10 exceeded total spending by the rest of the semiconductor companies (\$35.9 billion versus \$23.0 billion) in 2017.

A total of 18 semiconductor suppliers allocated more than more than \$1.0 billion for R&D spending 2017. The other eight manufacturers were NXP, TI ST, AMD, Renesas, Sony, Analog Devices, and GlobalFoundries. <>

New IC manufacturing lines to boost total industry wafer capacity 8%

IC industry wafer capacity, specifically in the memory segment, was inadequate to meet demand throughout 2017. However, with Samsung, SK Hynix, Micron, Intel, Toshiba/WD, and XMC/ Yangtze River Storage Technology planning to significantly ramp up 3D NAND flash capacity over the next few years, and Samsung and SK Hynix boosting DRAM capacity this year and next, what does this mean for total industry capacity growth? In its 2018-2022 Global Wafer Capacity report, IC Insights shows that new manufacturing lines are expected to boost industry capacity 8% in both 2018 and 2019 (**Figure 1**). From 2017-2022, annual growth in IC industry capacity is forecast to average 6.0% compared to 4.8% average growth from 2012-2017.



FIGURE 1.

Large swings in the addition or contraction of wafer capacity by the industry, as a whole, appear to be moderating. Since 2010, annual changes in wafer capacity volume have been in the relatively narrow range of 2-8%, with the largest year-to-year difference being just three percentage points. This suggests that IC manufacturers are better today than in years past about trying to match supply with demand. It's still an incredibly difficult task for companies to gauge how much capacity will be needed to meet demand from customers, especially given the time it takes a company to move from the decision to build a new fab to that fab being ready for mass production.

Many companies, DRAM and NAND flash suppliers in particular, have become much more active with new fab construction and expansion projects at existing fabs. This surge in activity comes after four years (2014-2017) when capacity growth lagged wafer start volume increases. During the past few years, IC producers have worked to increase utilization rates from the low levels in 2012-2013.

If all the new fab capacity expected to be brought on-line in 2019 happens as planned, the volume of capacity added that year will approach the record set in 2007. **Figure 2** shows more that 18 million wafers per year of new capacity is expected to



FIGURE 2.

be added in 2019, and this number even assumes some of the massive DRAM and NAND fabs being built by Chinese companies will not be carried out quite as aggressively as has been advertised. IC Insights believes that construction of these China-owned fabs is progressing slower than planned.



sheaths in ASM[®] Epsilon[®] epitaxial reactors up to **3X longer**. Find out how EtchDefender[™] can eliminate 1-2 maintenance cycles and **reduce your annual spend by 30%.**



+1 800 223 2389 conaxtechnologies.com/etchdefender SM⁴ and EPSILON⁴ are registered trademarks of ASM⁴ International Neither Conax Technolog

Samsung Starts Production of Gen-2 HBM2



PHIL GARROU, Contributing Editor

First introduced in June 2016, the Samsung HBM2 consists of eight 8Gb HBM2 dies and a buffer die at the bottom of the stack, vertically interconnected by TSVs and μ bumps. With each die containing over 5,000 TSVs, a single Samsung 8GB HBM2 package has over 40,000 TSVs. Including spares TSVs ensures high performance, by enabling data paths to be switched to different TSVs when a delay in data transmission occurs. The HBM2 is also designed to prevent overheating beyond certain temperature to guarantee high reliability. The HBM2 reports a 256GB/s data transmission bandwidth, offering



FIGURE 1. The new HBM2, Aquabolt[™], features today's highest DRAM performance levels, for use in next-generation supercomputers, Al solutions and graphics systems.

more than an 8X increase over a 32GB/s GDDR5 DRAM chip. With capacity double that of 4GB HBM2, the 8GB solution contributes greatly to improving system performance and energy efficiency, offering ideal upgrades to data-intensive, high-end computing (HPC) applications that deal with machine learning and graphics processing.

In January, Samsung announced that it has started mass production of its 2nd-generation 8-gigabyte (GB) High Bandwidth Memory-2 (HBM2) with the fastest data transmission speed on the market today. Dubbed "Aquabolt",

> it is claimed to be the industry's first HBM2 to deliver a 2.4 gigabits-persecond (Gbps) data transfer speed per pin, at 1.2V for the supercomputing and the graphics card market.

This performance is reportedly 50% greater than the 1st-generation 8GB HBM2 package with its 1.6Gbps pin speed at 1.2V and 2.0Gbps at 1.35V.

A single Samsung 8GB HBM2 package will offer a 307 GBps data bandwidth, achieving 9.6 times faster data transmission than an 8 gigabit (Gb)

GDDR5 chip, which provides a 32GBps data bandwidth. Using four of the new HBM2 packages in a system will enable a 1.2 terabytes-per-second (TBps) bandwidth.

In addition, Samsung increased the number of thermal bumps between the HBM2 dies, enabling better thermal control in each package. The new HBM2 also includes an additional protective layer at the bottom, which increases the package's overall physical strength.

Packaging



Practical Spin Wave Transistor **One Step Closer**

University of Groningen physicists have managed to alter the flow of spin waves through a magnet, using only an electrical current. This is a huge step towards the spin transistor that is needed to construct spintronic devices. These promise to be much more energy efficient than conventional electronics. The results were published on 2 March in Physical Review Letters.



FIGURE 1. Schematic illustration of the magnon transistor. The device consists of a substrate of gadolinium gallium garnet (GGG), a thin film of yttrium iron garnet (YIG, the magnetic insulator) and platinum electrodes (the grey structure on the surface of the YIG). The narrow electrodes on the sides are used to inject or detect magnons, and the broad middle electrode is the modulator contact: By sending a dc current through the modulator, the magnon density in the magnetic insulator can be influenced. A positive DC current generates extra magnons, while a negative current reduces the magnon density. This causes the magnon current between the outermost electrodes to increase or decrease. Credit: Ludo Cornelissen / University of Groningen

In a conventional computer, separate devices are needed for data storage and data processing. Spintronics could integrate both in one device, so it would no longer be necessary to move information between storage and processing units. Furthermore, spins can be stored in a non-volatile way, which means that their storage requires no energy, in contrast to normal RAM memory. All this means that spintronics could potentially make faster and more energy-efficient computers.

Semiconductors



Wave

The Physics of Nano Devices group of physics professor Bart van Wees at the University of Groningen's Zernike Institute of Advanced Materials is at the forefront of this field. In their latest paper, they present a spin transistor based on magnons. Magnons, or spin waves, are a type of wave that only occurs in magnetic materials. 'You can view magnons as a wave, or a particle, like electrons', explains Ludo Cornelissen, PhD student in the Van Wees group and first author of the paper.

In their experiments, Cornelissen and Van Wees generate magnons in materials that are magnetic, but also electrically insulating. Electrons can't travel through the magnet, but the spin waves can – just like a wave in a stadium moves while the spectators all stay in place. Cornelissen used a strip of platinum to inject magnons into a magnet made of yttrium iron garnet (YIG). 'When an electron current travels through the strip, electrons are scattered by the interaction with the heavy atoms, a process that is called the spin Hall effect. The scattering depends on the spin of these electrons, so electrons with spin up and spin down are separated.'

Spin flip

At the interface of platinum and YIG, the electrons bounce back as they can't enter the magnet. 'When this happens, their spin flips from up to down, or vice versa. However, this causes a parallel spin flip inside the YIG, which creates a magnon.' The magnons travel through the material and can be detected with a second platinum strip.

'We described this spin transport through a magnet some time ago. Now, we've taken the next step: we wanted to influence the transport.' This was done using a third platinum strip between injector and detector. By applying a positive or negative current, it is possible to either inject additional magnons in the conduction channel or drain magnons from it. 'That makes our set up analogous to a field effect transistor. In such a transistor, an electric field of a gate electrode reduces or increases the number of free electrons in the channel, thus shutting down or boosting the current.'

Cornelissen and his colleagues show that adding magnons increases the spin current, while draining them causes a significant reduction. 'Although we were not yet able to switch off the magnon current completely, this device does act as a transistor', says Cornelissen. Theoretical modelling shows that reducing the thickness of the device can increase the depletion of magnons enough to stop the magnon current completely.

RELIABILITY

Mechanism and improvements of Cu voids under via bottom

By **CHENG-HAN LEE** and **REN-KAE SHIUE**, Department of Materials Science and Engineering, National Taiwan University, Taiwan, ROC

This work explores the effect of underlying metallic alloys and the influence of Cu loss under via bottom after dry etching and wet cleaning processes. To Improve the Cu loss under via bottom, effective approaches are proposed. The modified actions for via bottom improve not only wafer yield but also reliability of the device.

ith metal line dimensional shrinkage in advanced packaging, Cu voids in metal lines cause the failure of via-induced metal-island corrosion. It impacts not only yield loss but also device reliability, specifically electron migration (EM) and stress migration (SM). One of the Cu voids is located under via bottom which is more unpredictable than others. The Cu void under via bottom is caused by integrated processes such as via etch and Cu electrochemical plating (ECP). It is not similar to the Cu void caused by barrier Cu-seed and ECP Cu. The mechanism of Cu voids under via bottom formation from dry etching and wet cleaning are related to Cu dual-damascene interconnection. Both plasma damage and chemical reaction are proposed to explain its failure mechanism. In the integrated process of Cu interconnects, we can design not only the safety dimension of Cu line via depth but also process criteria with less damage and oxidation in dry etching and wet clean based on Cu loss amount (Cu recess) in TEM inspection. The modified actions for via bottom improve not only wafer yield but also reliability of device.

Introduction

For deep sub-micrometer CMOS integrated circuit, copper (Cu) metallization has been applied in semiconductor metallization processes of ULSI beyond 0.13 μ m technology because of its lower resistivity and better reliability, especially better electron migration resistance than that of aluminum (Al) [1–4]. Under 10 nm technology, frontend-of-line (FEOL) device process had already transferred from planar to fin-fet MOS, but the Cu formation process only have slight change in backend-of-line (BEOL) metallization. There are two kinds of schemes, single- and dual- damascene processes. In fact, the main body of Cu interconnection in dualdamascene process includes metal trench and via etching, post etching, wet clean, deposition of barrier films and Cu-seed layer, Cu ECP and Cu chemical mechanical polishing (CMP). They are all similar technologies.

Even though many well-known modifications were implemented in both mature and advanced processes, a few lethal defects which significantly damage wafer yield and device reliability, such as Cu voids and scratches, always exist after Cu-CMP process due to the Cu metal corrosion. Most previous studies in Cu voids, such as Lu et al. [5], Song et al. [6], Wrschka et al. [7] and T.C. Wang et al. [8], were focused on Cu voids on metal line due to wafer yield concern. It meant that Cu voids on metal line could be detected by on-line electron-beam inspection as demonstrated by Guldi et al. [9].

Although Reid et al. [10] have described that the formation of Cu voids could be resulted from step coverage of Cu-seed, waveform function and additives (Accelerator, Suppressor and Leveler), chemical formulation of ECP. However, the mechanism of Cu voids during the via-formation process is still unclear. Coverage or quality of seed layers being poor, thin and/or discontinuous will induce via bottom void which results in deteriorating the plating process. A systematic study of Cu void effects has not been reported. For the mature technology to reduce via resistance, a Cu

CHENG-HAN LEE and **REN-KAE SHIUE** are with the Department of Materials Science and Engineering, National Taiwan University, Taipei 106, Taiwan, ROC

RELIABILITY

surface cleaning (pre-cleaning) process prior to deposit the diffusion barrier metal to remove the CuOx on via bottom in order to improve yield was mentioned by Wang et al. [8]. However, it caused a significant Cu loss under via bottom as well as deteriorating reliability window of the process.

With the metal line shrinkage in advanced CMOS process, Cu void under via bottom becomes much crucial than before. Actually, it perhaps is the most important defect in device reliability concern. Unlike Cu voids or pits on metal line, such defects cannot be easily detected by on-line defect screen methodology, neither electrical test nor wafer yield testing. The reason is that Cu interconnection is still valid at that time. The most decisive step of Cu void detection under via bottom is the reliability test. Alers et al. [11] showed that Cu voids affected electron migration resistance. Wang et al. [12] had pointed out that Cu voids under via bottom were the major factor resulting in failure during stress and/or electron migration tests. In our experiment, Cu loss under via bottom was strongly related to high temperature storage (HTS) and high temperature operation life (HTOL) reliability tests. Thermal and/or

electronic stresses may resulted from many processes, including Si manufacturing, bumping, wafer yield test and even early failure rate (EFR) stage in reliability test. It should be further clarified.

Experimental procedures

A. Cu scheme and process

A via structure consisted of metal chains and via holes as displayed in **FIGURE 1**. Dual Cu damascene with "via first" process was applied to prepare the test sample. The Cu interconnection was made by BEOL Cu dual-damascene process which included an etching stop layer, dielectric deposition, metal line/via lithography, metal line/via dry etching, post etching wet clean containing deionized water (DIW) with discharging gas, deposition of barrier films and Cu-seed layer, Cu ECP and Cu CMP.

In advanced technology, EM resistance decreasing with metal line shrinkage of Cu interconnects was a major concern, specifically for dimensions of metal line and via bottom less than 30 nm. As the interconnect dimension



RELIABILITY



FIGURE 1. A schematic diagram of Cu daul-damascene via structure.

shrunk, the EM resistance of Cu interconnects was deteriorated and decreasing the service life of device. In order to improve EM resistance of Cu damascene, doping the Cu interconnects with appropriate elements was one of engineering approaches. Manganese (Mn) is one of the most popular element applied in Cu dopping. Mn could diffuse through the Cu interconnects and segregate along the interface between Cu and low-k dielectric layer. It was served as the barrier layer, adhesion promoter and oxidation retardant because the diffusivity of Mn in Cu was much faster than self-diffusivity of Cu, approximately one order of magnitude higher. It indicated that Mn atoms initially alloyed in Cu were migrated into surface and interface, and formed an oxide layer leaving the pure Cu behind after annealing step. In addition, Mn could also repair discontinuous barrier layer (Ta/TaN) by forming a local manganese silicate diffusion barrier layer. It was so called self-forming Cu-Mn diffusion barriers [13,14].

In this research, both Cu/1% Mn and Cu/1% Al served as underlying alloys were evaluated by Cu recess. The introduction of Cu/1% Al in the test was for the purpose of comparison. The main body of Cu interconnection of dual-damascene process included via etching, post etching wet clean, deposition of barrier films and Cu-seed layer and ECP. They were separated by different key process variables, such as dry etching power split, post etching as well as wet clean discharging gas flow rate split. The effect of these process variables on Cu loss under via bottom was evaluated in the experiment.

B. Methodology

FIGURE 2 illustrated a schematic diagram of Cu recess in the device. The Cu recess of via bottom was observed using the step-by-step TEM followed by dry etch and wet clean processes. The Cu line was receded back into the bottom of Cu metal after the process. The Cu recess data were helpful to define which stage played the crucial role in Cu loss of via bottom. Electrical and wafer yield tests were applied in order to locate any abnormality after all processes were completed.



FIGURE 2. A schematic diagram of Cu recess in device.

To unveil the effects of thermal/electronic stresses on Cu voids under via bottom, HTS (175oC) and HTOL (175oC with double device operation voltages) were performed to evaluate wafer yield swap after HTS and HTOL. Wafer yield swap was able to exam the yield before/after HTS and HTOL. The good die was failed if the Cu loss under via bottom occurred. After wafer yield swap dice was confirmed, failure analysis was performed by focus ion beam (FIB), scanning electron microscope (SEM) and transmission electron microscope (TEM). In addition, the chemical analysis was examined using energy dispersive spectroscope (EDS).

Results and discussion

A special design of metal line via structure with high aspect ratio of approximately 5 was performed in order to deteriorate Cu loss under via bottom. We inspected Cu recess of two different underlying metals, Cu/1% Mn and Cu/1% Al. **FIGURE 3** displayed Cu recesses of Cu/1% Al and Cu/1% Mn underlying metals, respectively. Under the same process condition, the Cu recess of Cu/1% Mn was only half of Cu/1% Al, so Cu/1% Mn was more protective than Cu/1% Al. There was a strong correlation between EM cumulative failure rate and the type of underlying metals. Cu/1% Al showed much lower time to failure (TTF) and deteriorated EM performance as compared with that of Cu/1%Mn. It clearly demonstrated that Cu/1% Mn was more protective than Cu/1% Al, and failure rate of Cu/1% Mn was only 1/30 of Cu/1%. The performance of



FIGURE 3. Cu recesses of Cu/1% Mn and Cu/1% Al underlying metals.

RELIABILITY

Cu/1% Al was significantly inferior to that of Cu/1% Mn. Therefore, Cu/1% Al was selected in following tests in order to enhance the differences of other key process variables.

In the standard (STD) condition, Cu recess was inspected by step-by-step TEM of dry etching and post etching wet clean with discharging gas process, and there were approximately 5 nm and 7 nm (12 nm - 5 nm = 7 nm) in depth of Cu loss as shown in **FIGURE 4**. The following barrier films and Cu-seed process only slightly consumed underlying Cu. The Cu recess only slightly increased 0.3 nm in barrier film deposition process. The pre-cleaning process was necessary before barrier film deposition in order to remove CuO on Cu surface for improved adhesion. Based on observations of Cu recess results in step-by-step TEM, post etching wet clean process also played an important role in Cu recess of via bottom.



FIGURE 4. Step-by-step TEM observations of the Cu recesses in different process stages.

Dry etching by plasma not only eroded about 5 nm in depth of Cu under the via bottom but also oxidized the underlying Cu which was supposed to be removed in subsequent wet cleaning process. Post etching wet clean included applying chemical solvent to clean by-product of dry etching and DI water clean to remove the chemical solvent. The DI water was with aid of discharging gas, such as CO_2 , in order to neutralize the accumulated charge generated by the plasma in previous dry etching. However, the discharging gas acidified the DI water and resulted in Cu loss in post etching wet cleaning process.

FIGURE 5 shows Cu recesses with different dry etching power splits. The change of plasma power split changed the degree of Cu recess. At the condition of 200 W less than STD, i.e., STD-200W, the Cu recess was less than 3 nm. Although the structure looks good in shape, poor performance was observed from electrical test and wafer yield after the process was completed. Via open resulted in upper Cu disconnected from underlying Cu as demonstrated by TEM observation (Fig. 5). It was deduced that dry etching process did not etch entire via hole, especially for the dielectric layer. Although post wet cleaning slightly extended the open area under via



FIGURE 5. Cu recesses in different dry etching power splits.

bottom, barrier films were not well deposited on the via hole. Therefore, poor coating was obtained from the subsequent ECP process. The via resistance marked up significantly as the dry etching power decreased to 200 W less than STD, i.e., STD-200W.

FIGURE 6 shows wafer yields after open/short tests with different dry etching power splits. In the open/short tests, the failure rate was decreased with decreasing the dry etching power from STD+100W to STD-100W due to less damage to the Cu substrate for lower dry etching power. The Cu recess was decreased from 17.9 nm (STD+100W) to 8.7 nm (STD-100W) as demonstrated in **FIGURE 5**. However, dramatically increased failure rate was observed when the dry etching power was decreased to 200 W less than STD (STD-200 W). Because the lowest dry etching power, STD-200W, was insufficient to enlarge the via hole, and resulted in increasing the via resistance. Therefore, the failure rate of STD-200W was as high as 10% as displayed in Fig. 6. There was an optimal dry etching power of STD-100W in order to maximize the wafer yield in the experiment.



FIGURE 6. The wafer yield failure rate changed with different dry etching power splits.





FIGURE 7. The Cu recess changed with different discharging gas flow splits.

FIGURE 7 showed the variation of Cu recess with different discharging gas flow splits in the post etching wet cleaning process. The discharging gas flow was strongly related to the Cu recess, and it demonstrated that the chemical property of wet clean also played a crucial role in Cu recess. **FIGURE 8** showed that the wafer yield failure rate was decreased with decreasing the post wet clean discharging flow from STD+200 sccm to STD-400 sccm. The major function of discharging gas, CO₂, neutralized the accumulated charge generated by the plasma in previous dry etching. It was necessary in post etching wet cleaning process. However, it should be kept below STD-300sccm in order to improve wafer yield in the experiment.

The reliability test result of HTOL with thermal and electronic stresses over 168 hours showed several good chips transferred to bad ones with open short bin, which was called bin swap. FIB, SEM, TEM and EDS were used in failure analyses. **FIGURE 9** showed the comparison of Cu recesses before and after HTOL tests for 168 hours. It was obvious that a deeper Cu recess was observed after stress applied. Before the stress applied, the via inter-



FIGURE 8. The wafer yield failure rate changed with different post wet clean discharging gas splits.



FIGURE 9. TEM micrographs in comparison of the via bottom before/after HTOL tests for 168 hours.

connect linked with underlying metal line. This is the key reason why it was difficult to detect this type of failure in the electrical test. In Fig. 9, the Cu recess before stress applied was 23.3 nm and it extended into 42.4 nm after HTOL test for 168 hours. The Cu recess extended into twice or even triple after thermal and electronic stresses applied. Therefore, quality of the via bottom joint was greatly deteriorated if there were Cu voids under the via bottom. With increasing applied thermal and electrical stresses to via bottom, the crack propagated to entire via bottom. The via bottom finally was disconnected from underlying metal line. It was so-called via open in semiconductor industry.

FIGURE 10 showed TEM bright field and EDS mapping of Ta at the failure location after HTOL for 168 hours. Taking a close look at the via bottom next to the interface of underlying metal line, the non-uniform barrier film was widely observed as shown in Fig. 10(a). It was the original failure location. In Fig. 10(a), TEM inspection of the failure location after HTOL test for 168 hours showed significant Cu loss, more than 30 nm, under via bottom. It was much greater than the Cu recess before thermal and electrical stress applied (12 nm). Based on the EDS mapping of Ta (Fig. 10(b)), the barrier film, TaN, was formed adjacent to the Cu loss of via bottom. It was important to note that the TaN was almost disappeared from corner of the via bottom. The disconnection of barrier film from the corner resulted in deteriorated Cu interface, and the Cu began to degenerate and shrink under applied thermal and electronic



FIGURE 10. (a) TEM bright field and (b) EDS mapping of Ta at the failure location after HTOL for 168 hours.

stresses. It finally resulted in separation of the upper and underlying Cu. The via bottom was completely opened and caused the failure of device.

Summary

With the metal line dimensional shrinkage in advanced packaging, Cu metallization has increased the concerns on long-term reliability of devices caused by Cu loss under via bottom. This work explores the effect of underlying metallic alloys and the influence of Cu loss under via bottom after dry etching and wet clean. Important conclusions are listed below:

- 1. Cu/1% Mn is more protective than original Cu/1% Al. The application of Cu/1% Mn improves both EM and SM resistances of via bottom.
- 2. Both plasma power of dry etching and the discharging gas flow of wet clean play important roles in the Cu loss under via bottom. Cu loss was initiated first after dry etching due to plasma damage. The plasma not only etched the underlying Cu of via bottom, but also oxidized the underlying Cu surface. Subsequent post etching wet clean with acidic water generated by discharging gas removes CuO at interface, and causes more Cu loss in subsequent wet cleaning process. They are the major mechanism of Cu loss under via bottom. Pre-cleaning of barrier films to remove superficial CuO on Cu for better adhesion is only a minor factor in Cu loss under via bottom.
- 3. To Improve the Cu loss under via bottom, effective approaches include applying protective metal line, such as Cu/ 1% Mn, minimizing interfacial damage by decreasing the power of dry etching, and the discharge gas flow of post etching.

Acknowledgement

Authors greatly acknowledge the support of Taiwan Semiconductor Manufacturing Company (TSMC) for this study.

References

- K. Ueno, M. Suzuki, A. Matsumoto, K. Motoyama, T. Tonegawa, N. Ito, K. Arita, Y. Tsuchiya, T. Wake, A. Kubo, K. Sugai, N. Oda, H. Miyamoto, S. Satio, "A high reliability copper dual-damascene interconnection with direct-contact via structure", 2000 IEDM Tech. Digest IEEE (2000), p. 265.
- M.H. Tsai, W.J. Tsai, S.L. Shue, C.H. Yu, M.S. Liang, "Reliability of dual damascene Cu metallization," in: Proceedings of the 2000 International Interconnect Technology Conference, IEEE (2000), p. 214.
- C. Ryu, K.W. Kwon, A.L.S. Loke, H. Lee, T. Nogami, V.M. Dubin, R.A. Kavari, G.W. Ray, S.S. Wong, "Microstructure and reliability of copper interconnects," IEEE Trans. Electron Devices 46 (1999), p. 1113.

- M.H.Tsai, R. Augur, V. Blaschke, R.H. Havemann, E.F. Ogawa, PS. Ho, W.K. Yeh, S.L. Shue, C.H Yu, M.S. Liang, "Electromigration reliability of dual damascene Cu/CVD SiOC interconnects," in: Proceedings of the 2001 International Interconnect Technology Conference, IEEE (2001).
- J.P. Lu, L. Chen, D. Gonzalez, H.L. Guo, D.J. Rose, M. Marudachalam, W.U. Hsu, H.Y. Liu, F. Cataldi, B. Chatterjee, P.B. Smith, P. Holverson, R.L. Guldi, N.M. Russell, G. Shinn, S. Zuhoski, J.D. Luttmer, "Understanding and eliminating defects in electroplated Cu films," in: Interconnect Technology Conference, Proceedings of the IEEE 2001 International (2001), p. 280.
- Z.G. Song, S.K. Loh, M. Gunawardana, C.K. Oh, S. Redkar, "Unique defects and analyses with copper damascene process for multilevel metallization," in: IPFA 2003, Proceedings of the 10th International Symposium on the Physical and Failure Analysis of Integrated Circuits, (2003), p. 12.
- P. Wrschka, J. Hernandez, G.S. Oehrlein, J.A. Negrych, G. Haag, P. Rau, J.E. Currie, "Development of a slurry employing a unique silica abrasive for the CMP of Cu damascene structures," J. Electrochem. Soc. 148 (2001), p. 321.
- T.C. Wang, Y.L. Wang, T.E. Hsieh, S.C. Chang, Y.L. Cheng, "Copper voids improvement for copper dual damascene interconnection process," J. Phy. Chem. Sol. 69 (2008), p. 566.
- R.L. Guldi, J.B. Shaw, J. Ritchison, S. Oestreich, K. Davis, R. Fiordalice, "Characterization of copper voids in dual damascene processes," in: Proceedings of Advanced Semiconductor Manufacturing 2002 IEEE/SEMI Conference and Workshop (2002), p. 351.
- J. Reid, V. Bhaskaran, R. Contolini, E. Patton, R. Jackson, E. Broadbent, T. Walsh, S. Mayer, R. Schetty, J. Martin, M. Toben, S. Menard, "Optimization of damascene feature fill for copper electroplating process," in: Proceedings of Interconnect Technology, IEEE International Conference (1999), p. 284.
- G.B. Alers, D. Dornisch, J. Siri, K. Kattige, L. Tam, E. Broadbent, G.W. Ray, "Trade-off between reliability and post-CMP defects during recrystallization anneal for copper damascene interconnects," in: Reliability Physics Symposium, 2001. Proceedings of the 39th Annual 2001 IEEE International (2001), p. 350.
- T.C. Wang, T.E. Hsieh, M.T. Wang, D.S. Su, C.H. Chang, Y.L. Wang, J.Y.M. Lee, "Stress migration and electromigration improvement for copper dual damascene interconnection," J. Electrochem. Soc. 152 (2005), p. 45.
- J. Koike, M. Haneda, J. Iijima, M. Wada, "Cu alloy metallization for self-forming barrier process," IEEE Interconnect Technology Conference (2006), p. 161.
- J. Koike, M. Wada, "Self-forming diffusion barrier layer in Cu-Mn alloy metallization," App. Phy. Lett. 87, 041911 (2005)
- J.P. Wang, Y.K. Su, "Effects of surface cleaning on stressvoiding and electromigration of Cu-damascene interconnection,"Trans. Device. Mater. Relia. IEEE (2008), p. 210. ◆

MATERIALS

EUV Lithography adds to increasing hydrogen demand at leading-edge fabs

DR. PAUL STOCKMAN, Linde Electronics, Taipei, Taiwan

On-site production an option for supply

ydrogen usage at leading-edge logic and foundry fabs has steadily increased over the past 20 years. What was supplied in individual cylinders is now frequently delivered by specialized bulk trucks carrying over one ton of hydrogen per vehicle; some fabs require multiple deliveries per day. With EUV (extreme ultraviolet) lithography nearing commercial, high-volume use, the demand for hydrogen will experience another inflection. In this article, we explain the current and future applications driving this demand, the geographical variation in supply, and on-site production solutions for high-volume customers.

Existing process applications

Hydrogen has been adopted as a material in processes throughout the fab. Its unique chemical properties continue to expand its usefulness. These applications typically use flows of 100s to 1,000s of sccm (standard cubic centimeter per minute):

- **Epitaxy:** Hydrogen is used as a reducing agent during the epitaxial growth of crystalline thin-films. This is often used to make a starting silicon surface for semiconductor manufacturing by reacting newly cut and polished silicon wafers with trichlorosilane (SiHCl₃) in an epi-house or end-user fab. The hydrogen reduces the gas-phase chlorine atoms, and the HCl product is removed from the reactor as a gas. Leading-edge channel materials like strained silicon, silicon-germanium, and germanium are also grown using hydrogen-mediated epitaxy.
- **Deposition:** Hydrogen can also be incorporated directly into thin-films to disrupt crystal lattices to make them less crystalline, more amorphous. This is often used with silicon thin-films, which need to be made more electrically insulating.

- **Plasma etch:** Hydrogen and hydrogen-containing plasmas are used to directly react with the surface of the wafer in order to clean or remove unwanted thin films, especially for removing unwanted fluorocarbon deposits on silicon oxides.
- **Anneal:** Silicon wafers are heated to temperatures over 1,000 C, often at elevated pressure, in order to repair their crystal structures. Hydrogen assists by transferring heat uniformly over the surface of the wafer, and also by penetrating into the crystal lattice to react with atomic impurities.
- **Passivation:** Hydrogen is used to react and remove native oxides on silicon surfaces and to mediate the reconstruction of silicon-silicon bonds in the final layers of the crystal.
- **Ion implantation:** With more precision than bulk annealing and passivation, protons produced from hydrogen gas can be implanted to specific depths and concentrations in a thin film using ion implanters. Not only can hydrogen atoms be inserted to modify a thin film, but in higher doses and implantation energies, it can be used to cleave slivers of silicon and sapphire wafers.
- **Carrier gas:** Hydrogen is used as a carrier gas to entrain (entrap) and transport less volatile chemicals ordinarily liquids at atmospheric pressure and room temperature—into the reaction chamber. The hydrogen is heated and bubbled through the liquid chemicals. Because the mass of hydrogen is very light compared to entrained chemical vapor, specialized mass flow controllers can then be used to sense, measure, and precisely control the amount of chemical vapor dispensed.

- **Material stabilization:** The addition of hydrogen extends the shelf life of important electronic materials like diborane (B₂H₆) and digermane (Ge₂H₆), which otherwise slowly decompose.
- **Polysilicon manufacturing:** Although not part of the process flow in semiconductor fabs, hydrogen is used in large quantities in the upstream process of manufacturing polysilicon: thousands of Nm³ per hour hydrogen are used, and typically an on-site hydrogen plant is required. Polysilicon is the starting material for making crystallized silicon, from which silicon wafers are sliced.

Application for EUV

Extreme ultraviolet (EUV) lithography is the muchanticipated new application expected to simplify the process patterning complexity for critical dimensions in leading-edge devices. While it has taken a long time for this technology to come close to commercialization, top-tier manufacturers are coalescing their predictions for volume manufacturing adoption in the 2018-2020 window. Whereas other hydrogen-consuming applications have a usage rate of 100s of sccm, EUV will require much larger flows of 100s of slm (standard liters per minute), or roughly 100 to 1,000x more per individual tool.

Deep ultraviolet (DUV) lithography, the current workhorse of the patterning tools, uses an electrical discharge in neon or krypton mixed with halogen gases like fluorine to produce UV light at 193 nm and 248 nm; EUV light production is much more complicated. Tin metal is heated above its melting point of 232 C, and small droplets of tin (~25 μ m diameter) are rapidly (50,000 droplets per second) produced. These droplets are first vaporized and then excited with high-power CO₂ lasers. The excited tin atoms emit EUV light at 13.5 nm, which is more than 14 times shorter than the DUV tools.

The light is emitted in all directions and is collected and collimated (aligned) by an array of mirrors. The light is then passed to the primary lithography tool for focusing and image transfer before illuminating the photoresist on the wafer. All materials heavily absorb EUV light. Absorption losses are minimized by using multi-layer



NEXTFLEX FACILITY | SAN JOSE, CALIFORNIA

REGISTER TO ATTEND TODAY AT MEPTEC.ORG





FIGURE 1.

reflective optics instead of the transmissive lenses used in DUV lithography, and the entire light source and patterning systems are housed in vacuum chambers. These highly complex tools are expected to cost end users around \$100 million USD each, and when fully adopted, a leading-edge fab could require 20 or more of these tools.

Scattered tin debris from the vaporization of droplets is a major potential source of contamination of both the collector and focusing optics. Unmitigated, the lifetimes of these expensive components would be unacceptable. Hydrogen gas is used to shroud the tin excitation region, and tin vapor and aberrant droplets are reacted to form stannane (SnH₄), which is then removed from that section of the housing by means of the vacuum line. Higher flows of hydrogen can be used in periodic plasma-based cleaning to remove tin that deposits on the collector optics.

Demand and supply

Even before the adoption of EUV technology, leadingedge logic and foundry processes have begun consuming several normal cubic meters (1,000 liters) of hydrogen per wafer processed. This usage trend is expected to continue increasing in the 10 nm and 7 nm nodes commercialized before wide-spread EUV use. Consequently, major fabs now use hundreds of Nm³ per hour. EUV, when fully extended to all of the critical layers, will roughly double the amount of hydrogen used in these fabs. In a related application, the largest LED fabs also use hundreds of Nm³ of hydrogen per hour, primarily as a carrier gas and diluent for the gallium, arsine, and phosphorus precursors used to make the light-emitting devices.

Supply of hydrogen to electronics customers has been historically driven by regional source types, engineering and transportation codes, and by end user preferences and process qualification. However, steep demand curves are causing users to consider new supply schemes for access to larger volumes, greater supply chain security, and lessening of local fab logistics.

Over 60 million metric tons of hydrogen are produced globally, almost exclusively from hydrocarbon feedstocks: natural gas, oil, and coal. Most of this is used as a chemical intermediate to make ammonia, methanol, and transportation fuels. Electronics uses much less than 1% of hydrogen, yet relies on industrial technologies and sources as supply origins.

Hydrogen is supplied in the following modes (**FIGURES 1** and **2**):

• **Cylinders:** In smaller volumes, hydrogen is supplied in standard-sized gas cylinders, which hold about 7 m³ of gas pressurized at approximately 175 bar (250 cu ft at 2,500 psi). The largest fabs now consume this amount in less than one minute. Individual cylinders can be manifolded together to create larger packs of cylinders, which are typically mounted into metal pallets for easier handling. These packs can even be arrayed into full truck trailers of connected cylinders. Despite the increased volume, there is a limitation on the level of mass flow that can be safely achieved from this configuration.



- **Compressed gaseous hydrogen (CGH) trailers:** To improve on both mass distribution and packaging/handling costs, specialized trailers with much larger, pressurizable vessels are used. These CGH (compressed gaseous hydrogen) trailers can hold 10,000 Nm³ at pressures similar to smaller packages, yet are the distribution equivalent to over 1,400 individual cylinders. Just as importantly, fewer, larger vessels are faster to fill, and easier to maintain quality to the very high standards required by the semiconductor industry. Fewer components and human interactions also reduce safety risks.
- **Liquefied hydrogen transport:** In North America and much of Europe, liquefied hydrogen transport is allowed. This further increases the amount of hydrogen per truck to 40,000 Nm³ gas, or the equivalent of around 6,000 cylinders. In addition to increasing the volume, liquefication of hydrogen is also an added purification step. By cooling the material down to the boiling point of 21 K (-252 C), most impurities are solidified and can be reduced in concentration by absorption.

These benefits come with a trade-off, however. Liquefying hydrogen to the very low required temperatures consumes a lot of energy, and mandates additional safety protocols. Moreover, there are fewer liquid hydrogen production sources versus gaseous facilities, and transportation distances and supply logistics can be substantially increased. It is important to note that liquid hydrogen transport is not allowed in the primary semiconductor producing countries of Asia (China[1], Japan, Singapore, South Korea, and Taiwan), and therefore not a consideration for users in that region.

On-site hydrogen production

A solution that is becoming appropriate for some fabs is on-site hydrogen production (**FIGURES 3 and 4**). All major fabs already have either direct on-site production of gaseous nitrogen, or are supplied via pipeline by local plants. On-site hydrogen production has similar considerations of planning, footprint, redundancy, and back-up.

• **Planning and footprint:** On-site gas production should be planned at the outset of the entire fab concept. Like on-site nitrogen production, construction of the hydrogen facility usually begins at the same time as groundbreaking for the fab. The footprint of the plant and auxiliary equipment needs to be accounted for, either on the user's property, or





on an adjacent parcel reserved for the gas supplier. Pipeline delivery needs to be routed. And importantly for hydrogen, permits must be applied for which differ according to location.

• Redundancy and back-up: Continuous supply is essential for all semiconductor material supply chains. On-site production must ensure continuous supply for planned and unplanned equipment downtime, or in the case that fab demand grows past the on-site generating capacity. This can be accomplished by choosing from among three alternatives. If liquefication of on-site generated hydrogen is part of the production and purification scheme, excess hydrogen can be liquefied and stored in cryogenic tanks. Hydrogen generators appropriate to produce semiconductor-grade material are often modular, meaning that several will be used in parallel to make the full requirement of a fab. By installing an additional or redundant module, excess capacity is available in the event of planned maintenance or



FIGURE 4.

other event. Finally, off-site hydrogen is usually qualified as a supplement or temporary replacement. Often, this is the original source for the process of record for the manufacturer.

On-site hydrogen technologies suitable for semiconductor processes are either electrolysis of water, or so-called "reforming" and "shifting" of hydrocarbon feedstocks.

• **Electrolysis:** Electrolysis uses direct current electricity to split a water molecule into elemental hydrogen and oxygen. Actually, the reaction takes place in two physically distinct electrical poles of the equipment – the anode and the cathode – as two separate half-reactions. The net reaction is

$$2 H_2 O_{(\ell)} \rightarrow 2 H_{2(g)} + O_{2(g)}$$

Electrolysis is relatively expensive at volume because of the energy needed to break water molecule bonds even though achieving purity in the feedstock water is relatively simple.

Steam Reforming and Shifting: More economical are the industrial steam reforming and shifting processes, using hydrocarbon feedstocks like natural gas, LPG (liquefied petroleum gas – mostly propane and butane), and methanol. In fact, this is the process which produces most of the bulk hydrogen already used by existing semiconductor fabs, and is responsible for 95% of global hydrogen production. Natural gas (CH₄) and steam are heated over a catalyst to form syngas (a mixture of hydrogen and carbon monoxide).

$$CH_4 + H_2O \rightarrow CO + 3H_2$$

The syngas is then separated to give hydrogen. The carbon monoxide can then be further reacted (shifted) with the steam to yield additional hydrogen.

$$CO + H_2O \rightarrow CO_2 + H_2$$

Taken together, these process plants are known as steam methane reformers, or SMR plants. Choices for the exact plant technology depend upon the local feedstocks available and the customer quality profile requirements.

Regardless of whether the hydrogen is supplied in gaseous or liquefied containers or made on-site, semiconductor hydrogen supply schemes incorporate on-site, and often additional point-of-use, purification using various technologies: adsorption, gettering, and application of the unique property of hydrogen to diffuse through palladium metal membranes, which are impervious to most other molecules. In addition, hydrogen purity is monitored at several points in the distribution by multiple types of detectors.

Safety

As with all chemical supplies, safety is paramount. With hydrogen, the main safety risk is associated with its wide range of flammability and explosivity. Throughout production and packaging, multiple types of redundant protocols are used to ensure that no oxidizers are contacted or incorporated into the hydrogen and plant designs minimize the risk for leaks. Specialized clothing resistant to fire and static is worn in some hydrogen producing and using environments. Materials of construction and component qualification are also important to guard against a phenomenon known as hydrogen embrittlement, where at elevated temperatures and/or pressures, hydrogen can permeate and weaken certain metals and alloys. Finally, liquefied hydrogen introduces the additional risk associated with cryogenic materials and the need to use insulating vessels and personal protection.

Conclusion

Semiconductor manufacturing has long used hydrogen in an essential and expanding portfolio of applications. Already, hydrogen supply is considered a bulk material scheme, with source, transport, and logistic considerations. The adoption of EUV at leading-edge fabs in the next few years will accelerate the pace of hydrogen consumption, and drive the consideration of new supply schemes. End users should evaluate hydrogen supply options for future fabs as part of their advanced planning to ensure that their quality, supply and process integrity requirements will be met.

References

 China is in the process of approving liquefied hydrogen transport at the time of this publication. The details are not yet defined.

The (automotive) problem with semiconductors

DAVID W. PRICE, DOUGLAS G. SUTHERLAND and JAY RATHERT, KLA-Tencor, Milpitas, CA

The Process Watch series explores key concepts about process control—defect inspection, metrology and data analysis—for the semiconductor industry. This article is the first in a five-part series on semiconductors in the automotive industry. In this article, we introduce some of the challenges involved in the automotive supply chain. Future articles in the series will address specific process control solutions to those challenges.

n the 1950s less than 1% of the total cost of manufacturing a car was comprised of electronics. Today that cost can be more than 35% of the total and it is expected to increase to 50% by the year 2030.[1] The rapid increase in the use of electronics in the automotive industry has been driven by four main areas:

- 1. Systems monitoring and control (electronic fuel injection, gas-electric hybrids, etc.)
- 2. Safety (anti-lock brakes, air bags, etc.)
- 3. Advanced Driver Assistance Systems (lane departure warning, parking assist, blind spot monitoring, adaptive cruise control, etc.)
- 4. Convenience (satellite navigation, infotainment, etc.)

Semiconductor components are at the core of the electronics integrated in cars, and depending on the make and model, a modern car may require as many as 8000 chips.[2] This number will only increase as autonomous driving gains popularity – additional electronic subsystems with their underlying ICs will power the sensors, radar and AI needed for driverless cars.

With over 88 million cars and light trucks produced every year, [3] each with thousands of chips, the

influence of the automotive industry on semiconductor manufacturing is starting to take hold. There is one simple fact about these thousands of chips found in a car: they cannot fail. Reliability is absolutely critical for automotive semiconductor components. Any chip that fails in the field can result in costly warranty repairs and recalls, can damage the image of the automaker's brand – or at the extreme, can result in personal injury or even loss of life.

If the average car contains 5000 chips and the automaker produces 25,000 cars per day, then even a chip failure rate at the parts per million (ppm) level will result in more than 125 cars per day that experience reliability issues as a result of chip quality. With semiconductors as the top issue on automakers' failure Pareto,[4] Tier 1 automotive system suppliers are now demanding parts per billion (ppb) levels of semiconductor quality with an increasing trend toward a maximum number of "total allowable failure events" regardless of volume. Current methods for finding reliability failures are overly dependent on test and burn-in, and as a result, the quality targets are missed by orders of magnitude. Increasingly, challenging audit standards are pushing for reliability failures to be found at their source in the fab, where costs of discovery and corrective action are the lowest. To enter this growing market segment – or simply maintain share - IC manufacturers must aggressively address this inflection in chip reliability requirements.

DR. DAVID W. PRICE and **JAY RATHERT** are Senior Directors at KLA-Tencor Corp. **DR. DOUGLAS SUTHERLAND** is a Principal Scientist at KLA-Tencor Corp.

PROCESS WATCH



FIGURE 1. The same defect types that impact yield also affect reliability. They are distinguished primarily by their size and where they occur on the device's pattern structure.

Fortunately for semiconductor manufacturers, chip reliability is highly correlated to something they know very well: random defectivity.[5] In fact, for a welldesigned process and product, early-life chip reliability



FIGURE 2. Yield curves (Yield versus Time) for different fab types. The yellow line is for non-automotive fabs where the major consideration is fab profitability. At some point the yield is high enough that it is no longer practical to continue trying to drive down defectivity. The blue dashed line is the yield curve that also factors in reliability. For IC products used in the automotive supply chain additional investment must be made to ensure high reliability, which is strongly correlated to yield.



issues (extrinsic reliability) are dominated by random defectivity.[6-12] A killer defect (one that impacts yield) is a defect that causes the device to fail at time t = 0 (final test). A latent defect (one that impacts chip reliability) is a defect that causes the device to fail at t > 0 (after burn-in). The relationship between killer defects (yield) and latent defects (reliability) stems from the observation that the same defect types that impact yield also impact reliability.

distinguished primarily by their size and where they occur on the device structure. **FIGURE 1** shows examples of killer and latent defects that result in open and short circuits.

The relationship between yield and reliability defects is not limited to a few specific defect types; any defect type that can cause yield loss is also a reliability concern. Failure analysis indicates that the majority of reliability defects are, in fact, process-related defects that originate in the fab. Because yield and reliability defects share the same root cause, increasing yield (by reducing yieldrelated defects) will have the additional benefit of improving reliability.

The yellow line in **FIGURE 2** shows a typical yield curve. If we only consider chip yield, then at some point, further

investment in this process may not be cost-effective and thus the yield tends to level off as time progresses. The blue dashed line in Fig. 2 shows the curve for the same fab making the same product. However, if they want to supply the automotive industry then they must also account for the costs of poor reliability. In this case further investment is warranted to drive down defect density even further, which will both increase yield and deliver the improved reliability required for automotive suppliers.

The change from being a consumer-grade chip supplier to an automotive supplier requires a paradigm shift at the fab management level. Successful semiconductor manufacturers who supply the automotive industry have long adopted the following strategy: The best way to reduce the possibility of latent (reliability) defects is to reduce the fab's overall random defectivity levels. This means having a world class defect reduction strategy:

- 1. Higher baseline yields
- 2. Lower incidence of excursions
- 3. When excursions do occur, quickly find and fix them inline
- 4. Ink out suspicious die using die-level screening

These and other strategies will be addressed in forthcoming articles in this Process Watch automotive series.

References

- 1. https://www.statista.com/statistics/277931/automotiveelectronics-cost-as-a-share-of-total-car-cost-worldwide/
- 2. Senftleben and Froehlich, Aspects of Semiconductor Quality from an OEM Perspective, April 2017.
- 3. http://www.businessinsider.com/2016-was-a-record-breakingyear-for-global-car-sales-and-it-was-almost-entirely-driven-bychina-2017-1
- 4. https://www.consumerreports.org/car-reliability-owner-satisfaction/consumer-reports-car-reliability-survey-2017/
- Price and Sutherland, "Process Watch: The Most Expensive Defect, Part 2," Solid State Technology, July 2015.
- Riordan et al., "Microprocessor Reliability Performance as a Function of Die Location for a .25um, Five Layer Metal CMOS Logic Process," 37th Annual International Reliability Physics Symposium Proceedings (1999): 1-11. http://dx.doi.org/10.1109/ RELPHY.1999.761584
- Barnett et al., "Extending Integrated-Circuit Yield Models to Estimate Early-Life Reliability," IEEE Transactions on Reliability, Vol. 52, No. 3., 2003.
- Shirley, "A Defect Model of Reliability," 33rd Annual International Reliability Symposium, Las Vegas, NV, 1995.
- Kim et al., "On the Relationship of Semiconductor Yield and Reliability," IEEE Transactions on Semiconductor Manufacturing, Vol. 18, No. 3, 2005.

- Roesch, "Reliability Experience," Published lecture #12 for Quality and Reliability Engineering ECE 510 at Portland State University, 2013. http://web.cecs.pdx.edu/~cgshirl/Quality%20 and%20Reliability%20Engineering.htm
- Shirley and Johnson, "Defect Models of Yield and Reliability," Published lecture #13 for Quality and Reliability Engineering ECE 510 course at Portland State University, 2013. http://web. cecs.pdx.edu/~cgshirl/Quality%20and%20Reliability%20 Engineering.htm
- 12. Kuper et al., "Relation between Yield and Reliability of Integrated Circuits: Experimental results and Application to Continuous Early Failure Rate Reduction Programs," Proceedings of the International Reliability Physics Symposium (1996): 17-21.

that is no longer the case.

coloring scheme for their designs.

EDA

In multi-patterned designs, each color assignment represents a different manufacturing mask. Each mask is processed through a lithography operation, and the pattern is etched onto the wafer. Once all the masks are processed, the goal is to have all the shapes created from all the masks act as if they were all generated from one mask, with very similar process biases and variations.

Making the most of color in

your multi-patterning layouts

There are many different situations in which special attention to color choices provide

the potential to improve the manufacturing results of multi-patterned masks.

DAVID ABERCROMBIE and ALEX PEARSON, Mentor Graphics, Wilsonville, OR

ulti-patterning design rules don't care about

color (mask assignments). As long as all the

spacing and alternation constraints are met, any coloring arrangement is legal. In the

beginning of multi-patterning, all possible

color combinations that passed the design rule checks

(DRC) were considered and treated as equal. As the

technology moves into more advanced nodes, however,

As it turns out, one legal coloring choice can, in fact,

be significantly better than another when it comes to manufacturing success and chip performance. Designers working on multi-patterned layouts need

to understand the issues and conditions that affect

their color choices, so they can determine the optimal

To ensure that type of consistency, all the masks need to resemble each other in terms of the total area and distribution of shapes. Clumping shapes in one area of one mask, while distributing shapes evenly across another, is going to result in very different process bias behavior and results. Balancing the color density across each mask provides the best manufacturing result.

To explain why, let's look at a standard cell library design. Because power rails are typically much wider than the routing tracks inside the cells, they constitute a large portion of the polygon area inside the standard cell design block. The number of tracks in the library force the power rails into certain color pairings (**FIGURE 1**). In the first case, the power rails are forced to opposite colors, while in the second, they are forced to the same color.

The color ratio distribution charts tell the story of the two designs. When the power rails alternate color, the distribution of the color density ratio is well-centered

5-track (odd) standard-cell library (Power rails forced to opposite colors)

	Window Color Ratio Distribution		
T0 T1 T2 T3 T4 T5	Berut Coul	25 (493)	22
Ratio of Color1/all = 48.97% Ratio of Color2/all = 51.05%	0	00 0.10307 0.28571 0.028571 DV	6571629 6716286 6.857162 1 Propeny

4-track (even) standard-cell library (Power rails forced to same colors)





DAVID ABERCROMBIE is the Program Manager for Advanced Physical Verification Methodology at Mentor, a Siemens business. He may be reached at david_abercrombie@mentor.com. **ALEX PEARSON** is a Calibre Technical Marketing Engineer in the Design to Silicon division of Mentor. He can be reached at alex_pearson@mentor.com.





FIGURE 2. Effect of coloring choices on local density distribution.

around the 50% point. However, forcing the power rails to be a single color can dramatically shift the color ratio towards that single color. This distribution is more problematic to manufacture.

But uniform color density isn't just a chip-wide, global issue—even local differences can have negative impacts, because local areas with excessive or insufficient color density can impact the biases of nearby shapes during processing. In **FIGURE 2**, both coloring options are legal, but the polygons within each connected component are not equal in area, so the choice of G-B-G-B vs. B-G-B-G affects how much area of each color ultimately exists within this local region. The second coloring choice results in a more uniform area density of each color.

However, some layouts contain polygon configurations that inherently make it almost impossible to balance colors simply by changing color choices. For example, sometimes you have a very large area polygon in the



FIGURE 3. A single large area polygon can dominate color density.

midst of your layout (**FIGURE 3**). No matter what color you assign to the large polygon, it will dominate the color density in this region. Changing color selections in the nearby polygons doesn't help, because they can't all be assigned to the other color.

In this case, a new (and perhaps unexpected) solution is needed. Placing evenly distributed polygons of the opposite color in a grid on top of the large area polygon (known as reverse tone overlay fill) adds shapes to the opposite color mask in a region that would otherwise have been empty (**FIGURE 4**). The smaller polygons on top don't create openings (they merely "double" block the etch), so they have no real purpose in terms of the final wafer shape. In that regard, they are similar to dummy fill. This technique ensures the two masks have more similar color densities in this region.



FIGURE 4. Adding evenly distributed polygons of the opposite color helps ensure that one large polygon does not skew the color density balancing.

Color regularity

Specific configurations, such as those found in memory applications, may also need strongly controlled, repetitive coloring patterns to help the optical proximity correction (OPC) process generate more consistent results. **FIGURE 5** shows three vertical instantiations of a repetitive pattern with horizontal color alternation constraints. On the left, a density-balanced legal coloring assignment is shown. However, by adding a few extra coloring constraints, you can also achieve a regular repetitive coloring pattern, as shown on the right. By introducing this color regularity, you can increase the chances of consistency in the post-OPC results.



FIGURE 5. Regular coloring patterns enable a more consistent application of foundry processes.

Layout symmetry is another aspect of design that benefits from color regularity. When there is a significant amount of symmetry around a central point, such as a sensitive analog circuit, the most desirable coloring solution maintains x and y axis symmetry around the central point. In **FIGURE 6**, the constrained coloring solution on the right adds constraints for x and y axis symmetry to generate a mirrored coloring pattern.

DFM-aware coloring

EDA

In design for manufacturing (DFM) optimization, weak lithographic configurations are often captured as process hotspot patterns, which can be used with DFM and/or resolution enhancement technology (RET) processes to minimize the chance of a hotspot forming during manufacturing. As it turns out, the coloring of these patterns in multi-patterned designs can influence whether or not a pattern becomes a hotspot, or actually change the hotspot severity or impact of a particular pattern. If a hotspot pattern is consistently colored in all its instantiations, it may prevent that hotspot from forming, or allow a carefully tuned OPC recipe to be applied.



FIGURE 6. Mirrored coloring helps enforce symmetry when needed.



FIGURE 7. Applying different coloring to multiple pattern instances may determine whether or not a specific instance becomes a lithographic hotspot.

In **FIGURE 7**, a different, but still legal, coloring is applied to a rotated/reflected pattern. Because the OPC process will now affect each instance differently, the rotated pattern may become a lithographic hotspot, while the original pattern does not.

FIGURE 8 shows the same legal coloring applied to both pattern instances, which allows the same OPC to be applied to the layout in both locations, because the coloring is the same, and the polygons that end up on each mask are consistent.

Sometimes there are cases where information from other layers indicate a color preference for certain shapes. These preferences are typically the result of analysis on another layer, or from information the designer provides, such as for critical or high voltage nets. While these preferences may sometimes conflict with each other for neighboring shapes in the same

Constrained Coloring



EDA



FIGURE 8. Using the same coloring for all pattern instances helps standardize the results of the OPC process.

component, applying these preferences whenever possible helps drive an optimal coloring solution. In **FIGURE 9**, the red markers indicate a preference for placing those shapes on the green mask. In this case, there is one component that cannot comply, but placing three of the four tagged polygons on the preferred mask maximizes the preferred placements, making this optimal coloring solution.





Conclusion

In advanced process nodes, achieving the best performance and yield requires moving beyond the minimum requirements of the design rules to optimizing the layout. This optimization is a fundamental principle of all design for manufacturing (DFM) activities, including multi-patterning decomposition. There are many different situations in which special attention to color choices provide the potential to improve the manufacturing results of multi-patterned masks. Designers involved with generating the decomposed mask data before tapeout can expect to see more emphasis on color optimizations as the industry continues to refine and enhance multi-patterning processes. ◆

Solid State Product Showcase

A D V E R T I S E M E N T



Advanced Plasma Strip and MEMS Release

The ULVAC ENVIRO-1Xa plasma resist strip system offers low cost, exceptional performance in wafers from 4" to 8" in a compact footprint (14.6ft²). The system performs high-speed photo resist removal at >10 μ / min, with excellent repeatability and reliability.

www.ulvac.com



YES-ÉcoClean

Automated Plasma Resist Strip & Descum System

Automated wafer handling

- Multiple wafer sizes
- Small footprint
- Neutral plasma means gentle process

888-YES-3637

www.yieldengineering.com

ad index

Advertiser

Conax	9
ECTC	
Heidenhain	C4
LED Expo Thailand	C3
MEPTEC	19
SEMI	5
Sensors Expo	3
The ConFab	C2
Ulvac	
Y.E.S	7,30



EXECUTIVE OFFICES

Extension Media 1786 18th Street, San Francisco, CA 94107-2343.

ADVERTISING

Pg

Sales Manager Kerry Hoffman 1786 18th St. San Francisco, CA 94107-2343 Tel: 978.580.4205 khoffman@extensionmedia.com

North America Kerry Hoffman Tel: 978.580.4205 khoffman@extensionmedia.com

Germany, Austria, E. Switzerland & E. Europe

Holger Gerisch Tel: +49.0.8856.8020228 holgerg@pennwell.com

China, Hong Kong Adonis Mak Tel:+852.90182962 adonism@actintl.com.hk Taiwan Diana Wei Tel: +886.2.23965128 ext: 270 diana@arco.com.tw

Rest of World Kerry Hoffman Tel: 978.580.4205 khoffman@extensionmedia.com

Webcasts Jenna Johnson Tel: 612.598.3446 ijohnson@extensionmedia.com

The ConFab Kerry Hoffman Tel: 978.580.4205 khoffman@extensionmedia.com

industry forum

New insights from failures

To be able to guarantee the reliability of transistors, we have been conducting research for some years now at imec to see what happens when transistors operate properly and when they fail. We've been doing this in terms of circuits, devices and materials – and sometimes right down to the level of atoms. The insights that we gather from this work help us to provide the right feedback to the process technologists, who in turn are able to make the transistors more reliable. It is particularly interesting to note that in recent years the knowledge we have gained about these failure mechanisms can also be applied to other areas. These insights no longer only serve to solve problems, but are the basis for innovative and surprising solutions in very diverse domains.

Last year, imec spent a lot of time working on selflearning chips, data security codes, FinFET biosensors and computer systems that can correct themselves. These are innovations that draw on the knowledge present in imec's reliability group.

Self-learning chips

For example, take the self-learning or neuromorphic chip that gave imec such extensive coverage in the media in 2017. The development of this chip is based, among other things, on our knowledge of "resistive RAM" or RRAM memories, which use the breakdown of an oxide to switch a memory bit on or off (0 or 1). This oxide breakdown which was previously (and still is) a reliability problem occurs because a conductive path is created through the oxide, known as a filament. However, the work conducted by imec's reliability group has demonstrated that not only can you create a filament or make it disappear, but that there are intermediate levels as well, which means that the strength of the filament can be controlled. And that is precisely what happens in our brains: the connections between neurons can become stronger or weaker according to the occurrence they are processing or the learning process they use, etc. This means that these RRAM filaments can be used in chips that work like our brains. It was this insight that provided us with the foundation for the development of imec's neuromorphic



chip, which – as has been demonstrated – can even compose music.

GUIDO GROESENEKEN, imec fellow

Since recently we are also working closely with COSIC, an imec research group at KU Leuven that specializes in computer security and cryptography. Also here we can draw on our knowledge of transistor breakdown mechanisms. These can be used to create and read out a fingerprint that is unique for each chip and that cannot be predicted, hence the name 'physically unclonable functions' (or PUFs). This unique fingerprint makes it possible to ascertain the identity of chips in data exchanges and thus to prevent hacking by means of rogue chips.

The phenomenon of 'Random Telegraph Noise', which has long been known in the area of transistor reliability, could also be used as a security fingerprint. Random telegraph noise is a name for sudden jumps in voltage or current levels as the result of the random trapping of charges in traps within the gate insulation of a transistor. This phenomenon is unpredictable and random, and hence it could also be perfectly usable as PUF. What was once a problem for us – the breakdown of oxides or the existence of random telegraph noise – is now at the base of major new solutions for computer security.

Biosensors

A third example of discipline-overlapping innovation brings us to the world of life sciences. FinFET transistors are essential for the current and future generations of



FIGURE. Imec's neuromorphic chip, developed by researchers from both the reliability group and the computer architecture group.

industry forum

computer chips. As a result of the research carried out in our group, we have now found out a great deal about the way they work, including their failure mechanisms, etc. So much so that we can now explore the possibility to use them as biosensors. What happens is that biomolecules have a certain charge and when that charge comes into the vicinity of a FinFET, the current in the FinFET will be influenced. As a result, there is the potential that the presence of a single biomolecule can be detected by such a FinFET.

Self-healing chips

And, finally, we are also working with system architects to produce reliable chips, even with transistors that are no longer reliable. Extremely small transistors with dimensions smaller than 5 nanometers can be very variable and the way they behave is unpredictable. For that reason we are working with system architects on solutions such as selfhealing chips, based among other things on the existing models of the failure mechanisms that we provide them with. These self-healing chips will contain monitors that detect local errors. A smart controller then interprets this information and decides how to solve the problem, after which actuators are directed by the controller to carry out the task required.

What about scaling?

Numerous methods are currently being investigated to ensure that transistors can still be miniaturized and improved for as long as possible, as propounded in Moore's Law. To do so, the classic transistor architecture has already been replaced by a FinFET architecture and in the future this will evolve even to nanosheets or nanowires. Materials other than silicon, with greater mobility, are also being looked at, such as III-V materials (germanium for pMOS and InGaAs for nMOS).

In the choice made for these future architecture, it is extremely important to also look right from the start to the failure mechanisms and reliability of the new solutions. As an example, last year, our reliability team focused extensively on III-V transistors. Although these transistors score well in terms of mobility, their stability is still one of the main challenges remaining before we are able to take the next step and start manufacturing. The insulation layers in III-V transistors contain a lot of traps that cause this instability in transistor characteristics. Understanding this phenomenon is essential if we are to find a solution for it. So, a breakthrough in this area is needed urgently and our results, which were published in a recent IEDM paper, are certainly a step in the right direction. In the invited paper by Jacopo Franco these instabilities are first analyzed in detail. Then, based on this analysis, practical guidelines are given for the development of III-V gate stacks that offer sufficient reliability.

It's very difficult to look ahead even further into the future, because as the end of Moore's Law approaches, increasing numbers of different technologies and concepts are already on the radar (quantum computers, 2D materials, neuromorphic computers, spinwave logic, etc.). However, none of these concepts has yet made a real breakthrough. But in my view 2017 was the year in which the industry began to take a strong interest in quantum computers, with major investments from important players such as Google and Intel. Imec also plans to play a major role in this field, with the launch of a new program on quantum computing, gathering the extensive expertise available. In the past, quantum computing has been considered more as a purely academic field of research – something of value for physicists at universities, but not for engineers and companies. So perhaps the breakthrough of industrial quantum computing will be the next milestone in the history of electronics. Or perhaps this milestone will come from a totally unexpected angle – by combining knowledge and people from entirely different disciplines, creating totally new ideas and concepts. Only the future will tell us!

Guido Groeseneken is an imec fellow and expert in the reliability of transistors and electrical characterization. \blacklozenge



Platinum Sponsor PHILIPS Gold Sponsor



FUTURE OF LED

ASEAN's Largest International Exhibition on LED Products & Technology

VISIT

10-12 MAY, 2018

CHALLENGER 1 IMPACT EXHIBITION & CONVENTION CENTER BANGKOK, THAILAND

www.ledexpothailand.com

REACH OUT TO ASEAN REGIONS LED TECHNOLOGY & LIGHTING MARKET

ORGANIZERS

@MEX

MEX Exhibitions Pvt. Ltd. 9 LGF, Sant Nagar, East of Kailash, New Delhi-110065, India Ms. Himani Gulati Tel .: +91-9312285142 E-mail: himani@mexexhibits.com Mr. Gaurav Juneja Tel .: +91-9810301644 E-mail: gaurav@mexexhibits.com

IMPACT Exhibition Management Co., Ltd. Bangkok Land Building, 10 Floor, 47/569-576, Moo 3, Popular 3 Road, Banmai Sub-district, Pakkred District, Nonthaburi 11120







FSC Association









中華民國對外貿易發展協會 Taiwan External Trade Development Council



HEIDENHAIN

Where Accuracy Meets Throughput.

Enabling technology. Let us help with your next project.

HEIDENHAIN CORPORATION, 333 East State Parkway, Schaumburg IL, 60173 847-490-1191 www.heidenhain.us

Angle Encoders + Linear Encoders + Contouring Controls + Subsequent Electronics + Length Gauges + Rotary Encoders