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Caption: IBM scientists at the SUNY Polytechnic Institute Colleges of Nanoscale Science and Engineering's NanoTech Complex in Albany, NY prepare test wafers with 5nm silicon nanosheet transistors. (Credit: Connie Zhou)

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The ConFab 2019 Speakers and Prelim Agenda

The ConFab - an exclusive conference and networking event for semiconductor manufacturing and design executives from leading device makers, OEMs, OSATs, fabs, suppliers and fabless/design companies - announces a preliminary list of speakers for the May 14-17 event being held at The Cosmopolitan of Las Vegas.

The ConFab 2019 is excited to welcome these distinguished speakers:

- Jeff Welser, Vice President and Lab Director, IBM Research - Almaden
- Martin Fink, Executive Vice President and Chief Technology Officer, Western Digital
- Stephen S. Pawlowski, Vice President, Advanced Computing Solutions, Micron Technology, Inc.
- Dave Roach, Senior Vice President - Worldwide Manufacturing Operations, Western Digital
- John Chen, Vice President, Technology and Foundry Operations, Nvidia
- Sagar Pushpala, Vice President, Business Development - Specialty Technologies, TSMC
- Steve Teig, Chief Technology Officer, Xperi Corp.
- Dan Armbrust, CEO and co-founder, Silicon Catalyst
- Ren Wu, Founder and CEO, Novumind
- Alissa Fitzgerald, Founder and Managing Member, A.M. Fitzgerald & Associates
- Len Jelinek, Senior Director, Semiconductor Manufacturing, IHS Markit
- Weston Twigg, Senior Research Analyst and Managing Director, Keybanc Captial Markets

We'll start off with our usual "big picture" session, focusing on the hottest areas for semiconductor growth in the coming years: artificial intelligence, quantum computing, automotive, cloud computing, the IoT, 5G, virtual reality/augmented reality (VR/AR), smart cities and healthcare. Speakers will discuss how these and other applications will challenge the semiconductor industry in new and different ways in the near future.

This is especially true in the case of AI, which we'll explore in the second session, focusing it is ushering in a new era for semiconductor devices that will bring many new opportunities but also many challenges. The semiconductor industry will continue to drive microprocessors and memory technology forward, although perhaps at a slower pace defined by Moore's Law. An equally important trend known as "More than Moore (MtM)" devices, where added value to devices is provided by incorporating functionalities that do not necessarily scale according to "Moore's Law". These devices include MEMS, silicon photonics and biosensors. We'll be delving into that in Thursday morning's session.

I'm particularly excited about Thursday afternoon's panel discussion "Detect the Undectables, In-line Inspection and Diagnosis for sub-10nm IC Fab Processes." On Friday, leading analysts and economists will give their perspectives on global market trends.

This is a preliminary agenda – stay tuned for announcements on additional sessions and speakers at www.theconfab.com.

To inquire about participating - if you represent an equipment, material or service supplier, contact Kerry Hoffman, Director of Sales, at khoffman@extensionmedia.com. To inquire about attending, contact Sally Bixby, Sr. Events Director at sbixby@extensionmedia.com. I hope you can join us!

—Pete Singer, Editor-in-Chief

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Web Exclusives

SEMI Europe keynote to highlight Europe's competitiveness at EFECS 2018 in Lisbon

Joining distinguished speakers from the European Commission, industry, academia and Member States, Laith Altimime, SEMI Europe president, will keynote on "European Competitiveness in the Context of the Global Digital Economy" on 20 November at the European Forum for Electronic Components and Systems (EFECS) in Lisbon, Portugal.

https://bit.ly/2z7VNTk

Emerging MEMS and Sensor Technologies

When developing industry forecasts, market analysts gather data from hundreds of companies to provide actionable insights on established technologies and to identify near-term business opportunities. As a developer of new MEMS and sensor technologies for a range of commercial applications, clients often ask us, "What's going to be hot?" Gauging the promise of emerging technologies that are five to 10 years from commercialization requires taking a different tack.

https://bit.ly/2S1nV1D

SEMI supports U.S. return to trade talks with China, issues trade negotiation principles

SEMI, the global industry association serving the electronics manufacturing supply chain, voiced support and encouragement for trade discussions between U.S. President Donald Trump and People's Republic of China President Xi Jinping – talks that are planned for Dec. 1 during the G20 Summit in Argentina.

https://bit.ly/2zeObyh

BISTel partners with Siemens to deliver MindSphere applications for advanced data analytics and predictive maintenance

BISTeL, a provider of adaptive intelligent (AI) applications for smart manufacturing today announced that it has joined the MindSphere Partner Program, Siemens' partner program for Industrial IoT solution and technology providers. BISTel applications are expected to be available on the MindSphere platform Q1 2019.

https://bit.ly/2QQ3Nza

n&b news and blogs

Emerging MEMS and Sensor Technologies to Watch – 2019 and Beyond

When developing industry forecasts, market analysts gather data from hundreds of companies to provide actionable insights on established technologies and to identify near-term business opportunities. As a developer of new MEMS and sensor technologies for a range of commercial applications, clients often ask us, "What's going to be hot?" Gauging the promise of emerging technologies that are five to 10 years from commercialization requires taking a different tack.

https://bit.ly/2S1nV1D

MEMS and sensors in autonomous and electric vehicles: Key takeaways from IHS Markit at MSEC

Automobiles have become an even more important segment for MEMS and sensors as carmakers integrate more chips for propulsion, navigation, and control into their designs. However, these advanced functions and their crisp rate of adoption have fragmented the sourcing of automotive chips. IHS Markit's Jérémie Bouchaud provided a closer look at and outlook for this key market at the MEMS and Sensors Executive Congress in late October in Napa.

https://bit.ly/2DJgg4P

Nine Top-15 2018 semi suppliers forecast to post double-digit gains

Samsung expected to extend its number one ranking and sales lead over Intel to 19%.

https://bit.ly/2Kg8v73

New efficiency record set for perovskite LEDs

Researchers have set a new efficiency record for LEDs based on perovskite semiconductors, rivalling that of the best organic LEDs (OLEDs). Compared to OLEDs, which are widely used in high-end consumer electronics, the perovskite-based LEDs, developed by researchers at the University of Cambridge, can be made at much lower costs, and can be tuned to emit light across the visible and near-infrared spectra with high colour purity.

https://bit.ly/2QTyTpP

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USA - **Cabot Microelectronics** Corporation completed its acquisition of KMG Chemicals.

EUROPE - **EV Group** partnered with Plessey to drive GaN-on-Silicon monolithic microLED technology for AR applications.

USA - **Micron** announced a collaboration with a premium German automaker to advance automotive memory technologies.

ASIA - **Entegris** expanded its clean manufacturing facility in Malaysia.

USA - **GLOBALFOUNDRIES**, **indie Semiconductor** announced a collaboration to deliver performance-enhanced microcontrollers for automotive applications.

ASIA - **Praxair** signed a long-term supply agreement with Samsung in Hwaseong, South Korea.

USA - **Semiconductor Research Corporation** welcomed SK hynix to its acclaimed GRC and NST research programs.

USA - **Rudolph Technologies** releases NovusEdge System for edge, notch and backside inspection of unpatterned wafers.

EUROPE - **Leti** and **Taiwanese National Applied Research Laboratories** teamed up to strengthen microelectronics innovation in France and Taiwan.

USA- **KLA-Tencor** announced plans to establish R&D facility in Ann Arbor, Michigan.

Third quarter silicon wafer shipments increase, set new quarterly record

Worldwide silicon wafer area shipments increased during the third quarter 2018, surpassing record second quarter 2018 area shipments to set another all-time high, according to the SEMI Silicon Manufacturers Group (SMG) in its quarterly analysis of the silicon wafer industry.

Total silicon wafer area shipments reached 3,255 million square inches during the most recent quarter, a 3.0 percent rise from the 3,164 million square inches shipped during the previous quarter. New quarterly total area shipments clocked in 8.6 percent higher than third quarter 2017 shipments.

"Silicon shipment volumes remained at record levels during the third quarter," said Neil Weaver, chairman SEMI SMG and Director, Product Development and Applications Engineering of Shin Etsu Handotai America. "Silicon shipments are mirroring this year's strong semiconductor unit growth in support of a growing and diversified electronics market during our stable economy."

Silicon Area Shipment Trends – Semiconductor Applications Only

Silicon wafers are the fundamental building material for semiconductors, which in turn, are vital components of virtually all electronics goods, including computers, telecommunications products, and consumer electronics. The highly engineered thin round disks are produced in various diameters (from one inch to 12 inches) and serve as the substrate material on which most semiconductor devices, or chips, are fabricated.

All data cited in this release is inclusive of polished silicon wafers, including virgin test wafers and epitaxial silicon wafers, as well as non-polished silicon wafers shipped by the wafer manufacturers to the end-users.

The Silicon Manufacturing Group (SMG) is a sub-committee of the SEMI Electronic Materials Group (EMG) and is open to SEMI members involved in manufacturing polycrystalline silicon, monocrystalline silicon or silicon wafers (e.g., as cut, polished, epi, etc.). The purpose of the group is to facilitate collective efforts on issues related to the silicon industry including the development of market information and statistics about the silicon industry and the semiconductor market.

Millions of Square Inches							
	1Q2017	2Q2017	3Q2017	4Q2017	1Q2018	2Q2018	3Q2018
Total	2,858	2,978	2,997	2,977	3,084	3,164	3,255

Source: SEMI, (www.semi.org), November 2018

ECI Technology

The Global Leader in Wet Chemistry Process Control for Semiconductor and Printed Circuit Board Manufacturers

ECI Technology is a leading provider of chemical process control equipment to semiconductor and PCB industries worldwide. ECI develops and manufactures cutting-edge control systems for metal deposition, cleaning and etching processes used for manufacturing of advanced semiconductor devices. ECI products are installed throughout the leading fabs— assuring chamber / bath conditions are within specifications, qualifying incoming materials and monitoring chemical waste. ECI systems are widely accepted as critical enablers for the successful implementation of wet processes.

Semiconductor Manufacturing

ECI's chemical management systems are essential in meeting the challenging requirements of advanced semiconductor manufacturing where processes must operate within narrowing process windows. By precisely controlling the composition of chemicals, the company's accurate, reliable analyzers help manufacturers accelerate process development and ramp-to-volume, shorten time-to-market for new products and maximize yields in high-volume manufacturing. Building on decades of innovative research and critical IP, ECI works with end users, tool manufacturers and materials suppliers to provide optimized control solutions for new and estab¬lished processes. Its products interface seamlessly with process tools to monitor chemical concentrations and automatically control replenishment systems.

Advanced Packaging and PCB

ECI pioneered QUALILAB plating bath analyzer, that has become the standard for plating appli¬cations in the PCB industry worldwide. The speed and accuracy of ECI measurements enable precise control of bath composition to ensure void-free plating. Today, as the rate of development in packaging and PCB processes matches the fast pace maintained by the semiconductor industry, ECI leverages its deep expertise and adaptability to help its back-end customers tighten process windows and maximize yields as they strive to meet the rapidly-changing demands of their industry.

Product Portfolio

- QUALI-LINE® Market Leader for Cu Damascene, fully automated on-line chemical metrology for Inter¬connects metallization processes, **Copper** and **Cobalt**
- QUALI-FILL® Market Leader for Packaging, fully automated on-line chemical management, metrology and replenishment, for metallization processes in Advanced Packaging, including: WLP, CSP, Fan-Out, TSV, PLP, PCB and others
- QUALISURF® Market Leader for Wet Processing, fully automated on-line and benchtop chemical metrology for surface preparation technology: Cleans & Etch for process control, cost reduction by reclaim and materials inspection
- QUALILAB®, benchtop plating bath analyzer

A Complete Portfolio of Analyzers for Wet Chemistry Processing

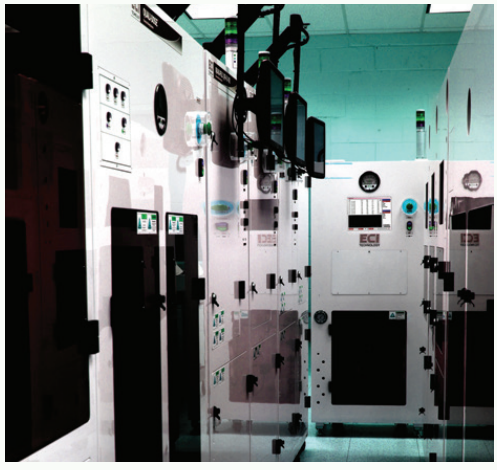
What Makes ECI Different

Technology Innovation and Leadership

Since its inception in 1987, ECI has established itself as the technical leader in chemical process control. The company has been recognized repeatedly for innovation and holds a broad portfolio of patents.

A Team with Unsurpassed Experience and Expertise

Team work is at the heart of ECI's problem solving approach and core team members average 10-20 years of experience with the company. The R&D staff includes world-renowned scientists who speak regularly at major analytical conferences. All products are designed and manufactured in-house by a staff of dedicated engineers and technicians.



A Comprehensive Problem Solving Approach

ECI's broad analytical expertise and deep experience permit a comprehensive approach to meeting customer challenges. ECI integrates multiple analytical techniques to create an optimal solution that not only gives the best answer but also meets the challenging demands of the high-volume manufacturing environments for speed, reliability, cost-of-ownership and ease-of-use. Partial list of techniques:

Global Sales, Service & Support

ECI maintains a global sales and service organization that supports thousands of successful installations in major fabs around the world. The organization provides comprehensive technical support, service and training for all products. Staffing in every territory includes service and process engineers.

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Global semiconductor sales in September up 13.8% year-to-year

The Semiconductor Industry Association (SIA), representing U.S. leadership in semiconductor manufacturing, design, and research, announced worldwide sales of semiconductors reached $122.7 billion during the third quarter of 2018, an increase of 4.1 percent over the previous quarter and 13.8 percent more than the third quarter of 2017. Global sales for the month of September 2018 reached $40.9 billion, an uptick of 2.0 percent over last month's total and 13.8 percent more than sales from June 2017. All monthly sales numbers are compiled by the World Semiconductor Trade Statistics (WSTS) organization and represent a three-month moving average.

"Three-quarters of the way through 2018, the global semiconductor industry is on pace to post its highest-ever annual sales, comfortably topping last year's record total of $412 billion," said John Neuffer, president and CEO, Semiconductor Industry Association. "While year-to-year growth has tapered in recent months, September marked the global industry's highest-ever monthly sales, and Q3 was its top-grossing quarter on record. Year-to-year sales in September were up across every major product category and regional market, with sales into China and the Americas continuing to lead the way."

Regionally, sales increased compared to September 2017 in China (26.3 percent), the Americas (15.1 percent), Europe (8.8 percent), Japan (7.2 percent), and Asia Pacific/All Other (2.4 percent). Sales were up compared to last month in the Americas (6.0 percent), China (1.8 percent), and Europe (1.2 percent), but down slightly in Asia Pacific/All Other (-0.1 percent) and Japan (-0.6 percent). ◁▶

Micron announces mass production of industry's highest-capacity monolithic memory for mobile applications

Micron Technology, Inc., (Nasdaq: MU) announced that it has begun mass production of the industry's highest-capacity and first monolithic 12Gb low-power double data rate 4x (LPDDR4x) DRAM for mobile devices and applications. This latest generation of Micron's LPDDR4 memory brings key improvements in power consumption while maintaining the industry's fastest LPDDR4 clock speeds, thereby delivering advanced performance for next-generation mobile handsets and tablets. In addition, Micron's 12Gb LPDDR4x doubles memory capacity to offer the industry's highest-capacity monolithic LPDDR4 without increasing the footprint compared to the previous generation product.

The exponential increase in usage of compute and data-intensive mobile applications such as artificial intelligence (AI), augmented reality (AR) and 4K video has been accompanied with demands by mobile users to maximize battery life and performance and increase capacity. Next-generation mobile devices that integrate multiple high-resolution cameras and increasingly use AI for image optimization also require higher DRAM capacities to support these features.

As the industry transitions towards deployment of 5G mobile technology, the memory subsystem in mobile handsets will have to support these dramatically higher data rates and the associated processing of data in real-time. New applications built upon 5G technology will also be able to leverage the increased capabilities of the memory subsystem to enable new and immersive user experiences.

As the industry's highest-capacity monolithic mobile memory, Micron's LPDDR4x DRAM delivers industry-leading bandwidth and power efficiency, along with the benefit of enabling higher DRAM capacities in the handset.

"Micron is a recognized pioneer in bringing low-power DRAM technology to the world and we once again have delivered another milestone with the launch of the industry's first, highest-capacity monolithic 12Gb mobile DRAM," Senior Vice President and General Manager of Micron's Mobile Business Unit Raj Talluri said. "This latest generation of LPDDR4 enables mobile handset manufacturers to deliver a rich user experience for ultra-slim mobile devices as user demands for performance, capacity and longer battery life continue to rise as a result of data-intensive applications."

The LPDDR4x DRAM will be produced based on 1Y-nm (10-nanometer-class) process technology, resulting in improved efficiency and reduction in battery power consumption. Micron's LPDDR4x mobile DRAM is capable of reducing power by up to 10 percent at similar data rates of 4,266 megabits per second (Mb/s) compared to previous generations. ◁▶

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New Applied Materials R&D center to help customers overcome Moore's Law challenges

Applied Materials, Inc. announced plans for the Materials Engineering Technology Accelerator (META Center), a major expansion of the company's R&D capabilities aimed at creating new ways for Applied and its customers to drive innovation as classic Moore's Law scaling becomes more challenging.

The primary goal of the META Center is to speed customer availability of new chipmaking materials and process technologies that enable breakthroughs in semiconductor performance, power and cost. The new center will complement and extend the capabilities of Applied's Maydan Technology Center in Silicon Valley.

The META Center will be a hub for innovation, delivering on a call to action by Applied CEO Gary Dickerson for increased collaboration and speed across the technology ecosystem.

"Realizing the full potential of Artificial Intelligence and Big Data will require significant improvements in performance, power consumption and cost both at the edge and in the cloud," said Gary Dickerson, president and CEO of Applied Materials. "The industry needs new computing architectures and chips enabled by innovative materials and scaling approaches. The META Center creates a new platform for working with customers to accelerate innovation from materials to systems."

Scheduled to open in 2019, the META Center will be a first-of-its kind facility, spanning 24,000 square feet of cleanroom. It will be furnished with a broad suite of Applied's most advanced process systems along with complementary technologies needed for new chip materials and structures to be piloted for high-volume production at customer sites.

To be located at the State University of New York Polytechnic Institute (SUNY Poly) campus in Albany, New York, the META Center will be created under agreements to be entered into with New York State, The Research Foundation for The State University of New York and SUNY Poly, that have been approved by the Empire State Development Board of Directors and are subject to further approval by The New York State Public Authorities Control Board.

"SUNY Poly provides an ideal combination of infrastructure, capabilities and talent in a thriving academic and entrepreneurial setting with deep roots in the semiconductor industry," said Steve Ghanayem, senior vice president of New Markets and Alliances at Applied Materials. "The technology ecosystem will benefit from the acceleration of materials innovation through collaboration at the META Center."

According to Samsung R&D, "We value our collaboration with Applied Materials on process development. The industry needs new innovations beyond traditional device scaling including the exploration of new materials. We are very pleased to see Applied Materials' effort to expand its advanced R&D capabilities to provide added resources to customers and accelerate chip development."

"TSMC welcomes closer collaboration with critical suppliers like Applied Materials in both equipment and materials," said J.K. Lin, TSMC's Vice President of Information Technology and Risk Management & Materials Management. "Working together to accelerate the industry's innovation and address high-growth opportunities is very much in the spirit of TSMC's Grand Alliance, the largest ecosystem in the semiconductor industry."

"IBM and Applied Materials have a long history of collaboration in materials engineering to advance semiconductor industry breakthroughs," said Dr. Mukesh V. Khare, IBM Research Vice President. "AI is one of the biggest opportunities of our time and will require innovations across materials, devices and architectures. We are pleased to see Applied expanding its capabilities to support the industry through the AI journey with its new META Center in Albany, New York."

"As complexity increases and costs rise, traditional device scaling is slowing for the latest technology nodes," said Tom Caulfield, CEO GLOBALFOUNDRIES. "It's great to see Applied Materials investing in a broad range of advanced R&D capabilities to bring new and new combinations of materials into chip manufacturing, and I look forward to our continued collaborative efforts as we develop more differentiated solutions for our clients."

"Delivering the improvements in performance and efficiency that allow Arm partners to continue to advance compute will mean overcoming the challenges presented by scaling transistors and interconnect in the deep nanometer process nodes," said Greg Yeric, fellow, Arm. "There are many novel ideas being explored in this area, but the timeline from concept to production needs to be accelerated, and the expansion of Applied Materials' R&D capabilities will help enable this research to advance at a faster pace."

"Applied Materials is the world leader in semiconductor process and tools," said Kurt Busch, CEO of Syntiant Corp. "We strongly value our relationship with Applied Materials and look forward to the benefits their latest technology will bring to breakthrough edge device machine learning products." ◁▶

Greene Tweed – A History of Semiconductor Innovation

Greene Tweed has been developing high-performance sealing solutions to withstand the extreme conditions of semiconductor processing since the 1980s, and has continually evolved to meet the increasingly demanding needs of the industry.

Greene Tweed leverages decades of engineering, materials, and applications expertise to design customized sealing solutions for specific operating environments, such as the oxygen- and fluorine-intense etch and deposition processes.

Greene Tweed was the first U.S. company to build a seal manufacturing cleanroom to meet the microcontamination needs of semiconductor manufacturers. Greene Tweed's Elastomer Center of Excellence (CoE) cleanroom provides the complete integration of elastomer development – from initial raw material mixing & development to final product packaging for new semiconductor compounds. These capabilities, now housed in a single cleanroom environment, enable Greene Tweed to deliver the highest quality product with industry standard contamination controls.

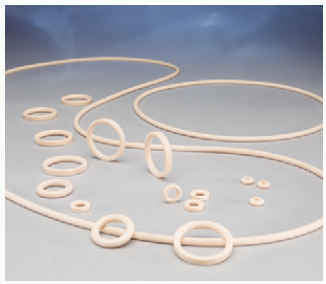
Greene Tweed engineers work collaboratively with customers to select materials and design seals that provide superior performance in their specific operating environments. Greene Tweed's broad range of Chemraz® FFKM formulations are utilized by some of the world's leading semiconductor fabs because of their performance and reliability.

Chemraz® sealing solutions are utilized throughout a broad range of mission-critical equipment in key process areas of the world's semiconductor fabs, including etch, deposition, aqueous, subfab, electro-chemical (electroplating), and more. The company's range of integrated solutions leverages bonding, encapsulation, and coating capabilities to provide high performance for critical components.

In addition to its elastomeric sealing portfolio, Greene Tweed also manufactures and designs finished components composed of filled and unfilled grades of PEEK, PTFE, and a range of thermoplastic composite materials.


Fusion™ F10


Chemraz® SubFAB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- Chemraz® 513 – recommended for dry process processing applications, providing excellent performance in static plasma, photolithography, and diffusion processes
- Chemraz® 629 – excellent O_2 plasma resistance with low contamination
- Fusion™ F10 – delivers performance similar to high-end polymers in both etch and deposition systems, and can be used in more than 80 percent of fab sealing applications

Etch Solutions

Processes: Conductor etch, dielectric etch, and ash/strip

Materials:

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- Chemraz® 657 – provides enhanced plasma resistance and minimal contamination in dry plasma systems
- Chemraz® E38 – specifically designed for high-density plasma systems and diffusion processes where seal reliability and minimal contamination are essential
- Fusion™ F10 delivers performance similar to high-end polymers in both etch and deposition systems, and can be used in more than 80 percent of fab sealing applications

Aqueous Solutions

Processes: Wet etch (acid, base), wet stripping (solvents), wet cleaning (UPDI), electroplating, Chemical Mechanical Planarization (CMP)

Materials:

- Chemraz® 571 – Durable compound for wet applications with high sealing loads
- Chemraz® 570 – Minimal particulation and maximum plasma resistance
- Chemraz® 551 – Broad chemical resistance at high temperatures

Electroplating Solutions

Processes: Electroplating and electrochemical deposition

Materials:

- Chemraz® 570 – recommended for equipment wet processing applications where stringent seal reliability and contamination control are required

Subfab Solutions

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Overcoming challenges of futuristic transistor technology below 5nm node

PAVAN H VORA, **AKASH VERMA** *and* **DHAVAL PARIKH**, *eInfochips, an Arrow company*

The potential transistor structures and materials like Carbon Nano-tube FET, Gate-All-Around FET, and compound semiconductors as solutions to overcome the problems of scaling the existing silicon FinFET transistor below 5nm node are reviewed.

The "semiconductor era" started in 1960 with the invention of the integrated circuit. In an integrated circuit, all the active-passive components and their interconnection are integrated on a single silicon wafer, offering numerous advantages in terms of portability, functionality, power, and performance. The VLSI industry is following Moore's law for many decades, which says, "the number of transistors on a chip becomes double approximately every two years". To get the benefits of a scaled-down transistor, VLSI industry is continuously improving transistor structure and material, manufacturing techniques, and tools for designing IC. Various techniques, which have been adopted for transistors so far, include high-K dielectric, metal gate, strained silicon, double patterning, controlling channel from more than one side, silicon on insulator and many more techniques. Some of these techniques are discussed in 'A Review Paper on CMOS, SOI and FinFET Technology.' [1]

Nowadays, the demand of the internet of things, autonomous vehicles, machine learning, artificial intelligence, and internet traffic is growing exponentially, which acts as a driving force for scaling down transistor below the existing 7nm node for higher performance. However, there are several challenges of scaling down a transistor size.

Issues with submicron technology

Every time we scale down a transistor size, a new technology node is generated. We have seen transistor sizes such as 28nm, 16nm, etc. Scaling down a transistor enables faster switching, higher density, low power consumption, lower cost per transistor, and numerous other gains. The CMOS (complementary metal-oxide-semiconductor) transistor base IC technology performs well up to 28nm node. However, the short channel effects become uncontrollable if we shrink down CMOS transistor below 28 nm. Below this node, a horizontal electric field generated by drain-source supply tries to govern the channel. As a result, the gate is unable to control leakage paths, which are far from the gate.

16nm/7nm transistor technology: FinFet and FD-SOI

The VLSI industry has adopted FinFET and SOI transistor for 16nm and 7nm nodes, as both the structures are able to prevent the leakage issue at these nodes. The main objective of both the structures is to maximize gate-to-channel capacitance and minimize drain-to-channel capacitance [1]. In both transistor structures, the channel thickness scaling is introduced as the new scaling parameter. As the channel thickness is reduced, there are no paths, which are far from the gate area. Thus, gates have a good control over the channel, which eliminates short channel effects.

In Silicon-on-Insulator (SOI) transistor, a buried oxide layer is used, which isolates the body from the substrate shown in **FIGURE 1a**. Owing to the BOX layer, drain-source parasitic junction capacitances are reduced, which results in faster switching. The main challenge with the SOI

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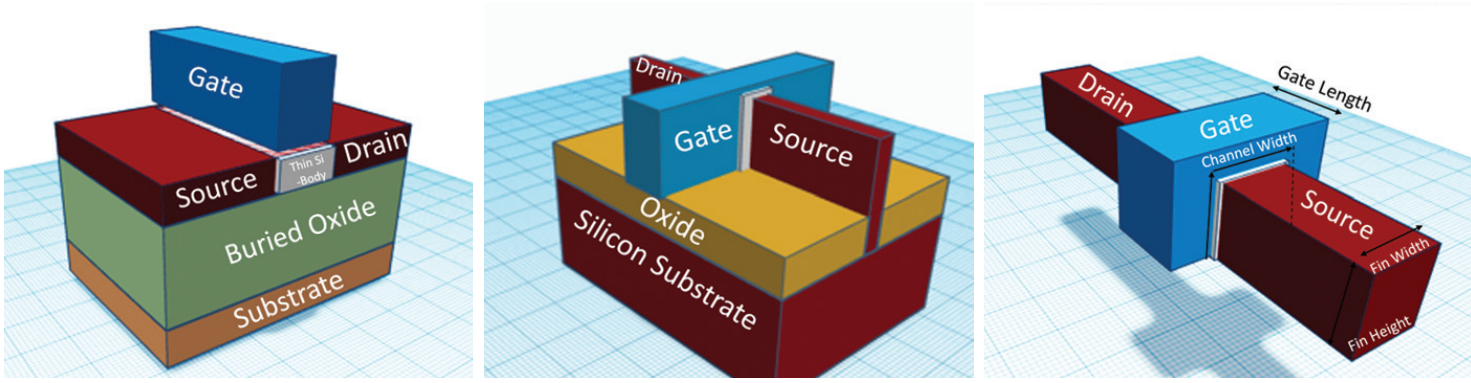

FIGURE 1. a) FD-SOI structure b) FinFET structure and channel.

transistor is that it is difficult to manufacture a thin silicon layer on the wafer.

FinFET, which is also called as tri-gate controls channel is shown from three sides in **FIGURE 1b**. There is a thin vertical Si-body, which looks like a back fin of fish wrapped by the gate structure. A width of the channel is almost two times Fin height. Thus, to get higher driving strength, a multi-Fin structure is used. One of the gains with FinFET is higher driving current. The main challenge with FinFET is the complex manufacturing process.

Challenges with technology node below 5nm: What next?

Reducing the body thickness results into lower mobility as surface roughness scattering increases. Since FinFET is a 3-D structure, it is less efficient in terms of thermal dissipation. Also, if we scale down the FinFET transistor size further, say below 7nm, the leakage issue becomes dominant again. Consequently, many other problems come into consideration like self-heating, threshold flattening, etc. These concerns lead to research on other possible transistor structures and replacing existing materials with new effective materials.

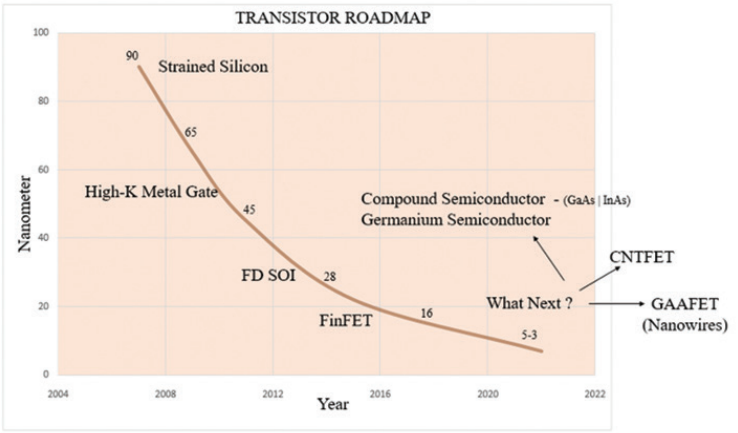

FIGURE 2. Transistor technology roadmap.

According to the ITRS roadmap (International Technology Roadmap for Semiconductors), the next technology nodes are 5nm, 3nm, 2.5nm, and 1.5nm. Many different types of research and studies are going on in VLSI industry and academia for potential solutions to deal with these future technology nodes. Here we discuss some promising solutions like carbon nanotube FET, GAA transistor structure, and compound semiconductor for future technology nodes (**FIGURE 2**).

CNTFET - Carbon Nano Tube FET

CNT (Carbon Nanotube) showcases a new class of semiconductor material that consists of a single sheet of carbon atoms rolled up to form a tubular structure. CNTFET is a field-effect transistor (FET) that uses semiconducting CNT as a channel material between the two metal electrodes, which behave as source and drain contacts. Here we will discuss carbon nanotube material and how it is beneficial to FET at a lower technology node.

CNT is a tubular shaped material, made of carbon, having diameters measurable on the nanometer scale. They have a long and hollow structure and are formed from sheets of carbon that are one atom thick. It is called "Graphene". Carbon nanotubes have varied structures, differing in length, thickness, helicity, and the number of layers. Majorly, they are classified as Single Walled Carbon Nanotube (SWCNT) and Multi-Walled Carbon Nanotube (MWCNT). As shown in **FIGURE 3a**, one can see that SWCNTs are made up of a single layer of graphene, whereas MWCNTs are made up of multiple layers of graphene.

The carbon nanotube delivers excellent properties in areas of thermal and physical stability as discussed below:

1. Both Metallic and Semiconductor Behavior

The CNT can exhibit metallic and semiconductor behavior. This change in behavior depends on the direction in which the graphene sheet is rolled. It is termed as chirality vector. This vector is denoted by a pair of integer (n, m) as shown in **FIGURE 3b**. The CNT behaves as metallic if 'n' equals to 'm' or the difference of 'n' and 'm' is the integral multiple of three or else it behaves as a semiconductor. [2]

2. Incredible Mobility

SWCNTs have a great potential for application in electronics because of their capacity to behave as either metal or as a semiconductor, symmetric conduction and their capacity to carry large currents. Electrons and holes have a high current density along the length of a CNT due to the low scattering rates along the CNT axis. CNTs can carry current around 10 A/nm^2, while standard metal wires have a current carrying capacity that is only around 10 nA/nm^2. [3]

3. Excellent Heat Dissipation

Thermal management is an important parameter for the electronic devices' performance. Carbon nanotubes (CNTs) are well-known nanomaterials for excellent heat dissipation. Moreover, they have a lesser effect of the rise in temperature on the I-V characteristics as compared to silicon. [4]

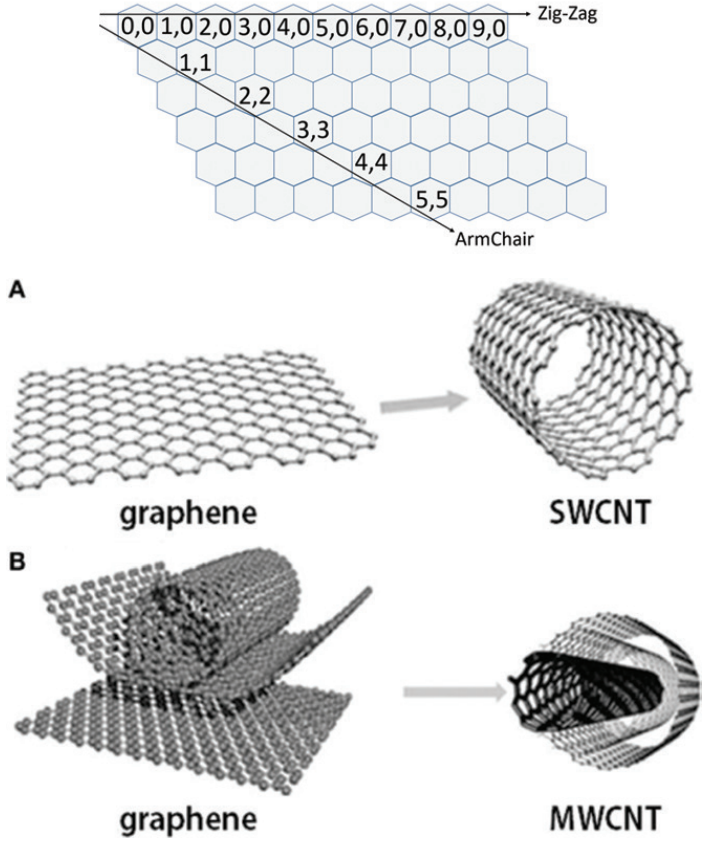

FIGURE 3. a) Single-walled and multi-walled CNTs b) chirality vector representation.

CNT in transistor applications: CNFET

The bandgap of carbon nanotubes can be changed by its chirality and diameter and thus, the carbon nanotube can be made to behave like a semiconductor. Semiconducting CNTs can be a favorable candidate for nanoscale transistor devices for channel material as it offers numerous advantages over traditional silicon-MOSFETs. Carbon nanotubes conduct heat similar to the diamond or sapphire. Also, they switch more reliably and use much less power than silicon-based devices. [5]

In addition, the CNFETS have four times higher transconductance than its counterpart. CNT can be integrated with a High-K material, which is offering good gate control over the channel. The carrier velocity of CNFET is twice as compared to MOSFET, due to increased mobility. A carrier mobility of N-type and P-type CNFET is similar in offering advantages in terms of same transistor size. In CMOS, PMOS (P-type metal-oxide-semiconductor) transistor size is approximately 2.5 times more than NMOS (N-type metal-oxide-semiconductor) transistor as mobility values are different.

The Fabrication process of CNTFET is a very challenging task as it requires precision and accuracy in the methodologies. Here we discuss the Top-gated CNTFET fabrication methodology.

The first step in this technique starts from the placement of carbon nanotubes onto the silicon oxide substrate. Then the individual tubes are isolated. Source and drain contacts are defined and patterned using advanced lithography. The contact resistance is then reduced by refining the connection between the contacts and CNT. The deposition of a thin top-gate dielectric is performed on the nanotube via evaporation technique. Lastly, to complete the process, the gate contact is deposited on the gate dielectric. [6]

Challenges of CNTFET

There are lots of challenges in the roadmap of commercial CNFET technology. Majority of them have been resolved to a certain level, but a few of them are yet to be overcome. Here we will discuss some of the major challenges of CNTFET.

1. Contact Resistance

For any advanced transistor technology, the increase in contact resistance due to the low size of transistors becomes a major performance problem. The performance of the transistor degrades as the resistance of contacts increases significantly due to the scaling down of transistors. Until now, decreasing the size of the contacts on a device caused a huge drop in execution — a challenge facing both silicon and carbon nanotube transistor technologies. [7]

2. Synthesis of Nanotube

Another challenge with CNT is to change its chirality such that it behaves like a semiconductor. The synthesized tubes have a mixture of both metals and semiconductors. But, since only the semiconducting ones are useful for qualifying to be a transistor, engineering methodologies need to be invented to get a significantly better result at separating metal tubes from semiconducting tubes.

3. To develop a non-lithographic process to place billions of these nanotubes onto the specific location of the chip poses a challenging task.

Currently, many engineering teams are carrying out research about CNTFET devices and their logic applications, both in the industries and in the universities. In the year 2015, researchers from one of the leading semiconductor companies succeeded in combining metal contacts with nanotubes using "close-bonded contact scheme". They achieved this by putting a metal contact at the ends of the tube and making them react with the carbon to form different compounds. This technique helped them to shrink contacts below 10 nanometers without compromising the performance. [8]

Gate-All-Around FET: GAAFET

One of the futuristic potential transistor structures is Gate-all-around FET. The Gate-all-around FETs are extended versions of FinFET. In GAAFET, the gate material surrounds the channel region from the four directions. In a simple structure, a silicon nanowire as a channel is wrapped by the gate structure. A vertically stacked multiple horizontal nanowires structure is proven excellent for boosting current per given area. This concept

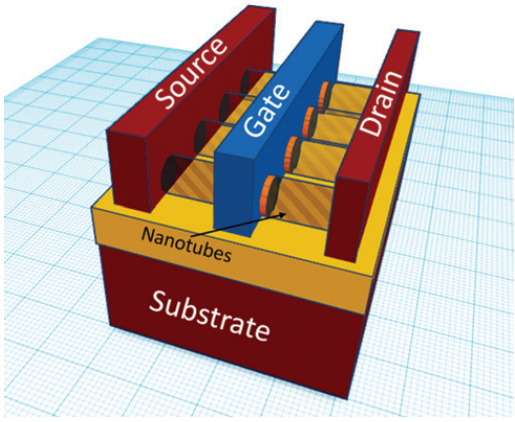

FIGURE 4. Concept of carbon-nanotube FET.

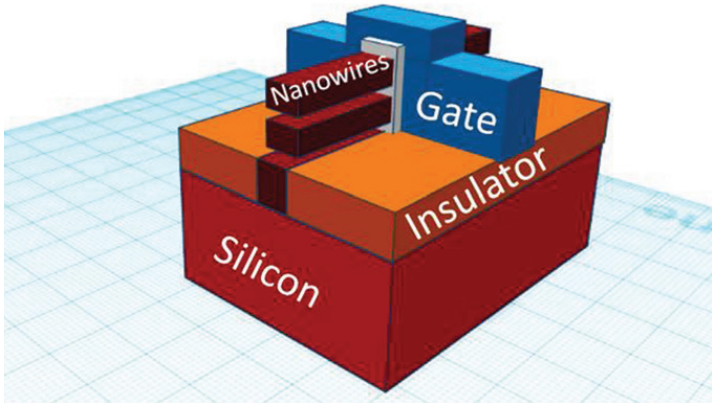

FIGURE 5. Vertically Stacked Nanowires GAAFET

of multiple vertically stacked gate-all-around silicon nanowire is shown in **Figure 5**.

Apart from silicon material, some other materials like InGaAs, germanium nanowires can also be utilized for better mobility.

There are many hurdles for GAAFET in terms of complex gate manufacturing, nanowires, and contacts. One of the challenging processes is fabricating nanowires from the silicon layer as it requires a new approach for the etching process.

There are many research labs and institute working for Gate-all-around FET for lower nodes. Recently, Leuven based R&D firm claimed that they achieved excellent electrostatic control over a channel with GAAFET at sub 10nm diameter nanowire. Last year, one of the leading semiconductor companies unveiled a 5nm chip, which contains 30 billion transistors on a 50mm^2 chip using stacked nanowire GAAFET technology. It claimed to achieve 40% improvement in performance compared to 10nm node or 70% improvement in power consumption at the same performance.

Compound semiconductors

Another promising way to scale down a transistor node is the selection of novel material that exhibits higher carrier mobility. A compound semiconductor with ingredients from columns III and V are having higher mobility compared to silicon. Some compound semiconductor examples are Indium Gallium Arsenide (InGaAs), Gallium Arsenide (GaAs), and Indium Arsenide (InAs). According to various studies, integration of compound semiconductor with FinFET and GAAFET showing excellent performance at lower nodes.

The main concerns with compound semiconductor are large lattice mismatch between silicon and III-V semiconductor, resulting in defects of the transistor channel. One of the firms developed a FinFET containing V-shaped trenches into the silicon substrate. These trenches filled with indium gallium arsenide and forming the fin of the transistor. The bottom of the trench is filled with indium phosphide to reduce the leakage current. With this trench structure, it has been observed that defects terminate at the trench walls, enabling lower defects in the channel.

Conclusion

From the 22nm node to 7nm node, FinFETs have been proven successful and it may be scaled down to one more node. Beyond that, there are various challenges like self-heating, mobility degradation, threshold flattening, etc. We have discussed how carbon nanotube's excellent properties of motilities, heat dissipation, high current carrying capability offer promising solutions for replacing existing silicon technology. As the stack of horizontal nanowire opened a "fourth gate", Gate-all-around transistor structure is also a good candidate for replacing vertical Fin structure of FinFET for achieving good electrostatic property. It is not clear what comes next in the technology roadmap. However, in the futuristic transistor technology, there must be changes of existing material, structure, EUV (Extreme ultraviolet) lithography process, and packaging to sustain Moore's law.

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Recovery and recycling of process gases: What are the options?

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Any consideration of recycling must take a systems-level approach, thoroughly considering all predictable and potential costs, including risks of downtime, contamination and safety.

Many wafer processes use only a small proportion of the gases that pass through the process chamber and discharge the rest, often after considerable cost and effort to mitigate any negative environmental impact. Recovery and recycling of most materials is possible, but is it worth it? The answer depends on value and cost. Cost includes both the cost of the technology and potential cost resulting from increased risk and system complexity. Value depends on many factors related to the specific problems to be solved, such as material scarcity, supply reliability, logistics, cost differential between recycled and purchased material, and environmental benefits. We will briefly review the benefits and costs that must be considered with an eye toward identifying circumstances that might justify recycling and recovery.

Benefits

Recycling can provide a reliable supply at a stable, predictable cost. The primary consideration is the cost differential between new and recycled material. New material will have a baseline price set by the inherent cost of production, though the price actually paid will be influenced by market forces of supply and demand. Some gases are abundant in nature and others inherently scarce. The price of abundant gases is driven primarily by separation and purification costs. In some cases, it is less expensive to simply extract a gas from the atmosphere on-site than to purchase or recycle it. Inherently scarce materials will never become more plentiful and their prices are, therefore, more susceptible to changes caused by swings in demand. When increased demand can be predicted, for instance, based on the wide spread adoption of a new application, it may be prudent to consider recycling in anticipation of increasing prices. The risk and potential cost of price volatility caused by geopolitical or natural events that are difficult or impossible to predict must also be factored into a cost analysis. Recycling gases can directly reduce fab emissions and the load on (and cost of) downstream abatement equipment. Finally, the cost of transport and local storage for new material must also be considered in the analysis.

Costs

The costs of recycling begin with the initial investment in equipment and ongoing operating expenses. Point-of-use systems will also carry a cost for additional space in the sub-fab. Generally, equipment in the sub-fab is also expected to fit within the "shadow" of the fab system it supports. Although recycling largely eliminates the risk

of supply interruptions caused by external events, it adds the risk of interruption caused by failure of the recycling system. The risk of wide spread contamination may also increase compared to batch supplies where contamination is typically restricted to a specific container or lot. There are additional risks to the safety of fab personnel and the surrounding community associated with the handling and storage of hazardous gases. Clearly, a thorough risk assessment must be part of any cost analysis.

Recycling technologies

Costs are primarily determined by choices made in two areas, technology and complexity. The most important drivers on the technology side are the type of material to be recovered, other materials in the stream, the purity required, and the process duty cycle. Typically, recycling includes separating wanted and unwanted components of the gas stream, pressurizing the recovered gas for storage and reuse, and purifying the gas to the required level. Many technologies are available, including:

Separation

Adsorption – either the wanted or unwanted material is selectively attracted to the surface of an adsorbent. The adsorbent will eventually become saturated and require replacement or regeneration, during which adsorbed material is released to allow the adsorbent to be reused.

Membrane – relies on pressure (concentration or chemical potential) gradients and selective diffusion across a membrane to achieve separation.

Electrochemical – gases that have reversible redox reactions, e.g. H2 <=> 2H+ + 2e-, can be separated electrochemically under ambient pressure and temperature conditions in a fuel cell like device. The gas is electrochemically converted to an ion at an electrode, transported across an ion-conductive membrane by a potential gradient, and reconverted to the gas at the other electrode.

Phase change – uses differences in phase change temperatures to selectively remove components from the stream (e.g. distillation).

Pressure/temperature swing adsorption – is a variation on adsorption that exploits the tendency of different gases to adsorb more strongly at elevated pressures or temperatures. Vacuum swing adsorption is similar but swings between sub-atmospheric and atmospheric pressures.

Chromatography – separates components in a mobile phase (the gas) based on differences in their interactions with a stationary phase (a liquid or solid material) as they travel through it.

Pressurization

Mechanical – mechanical pumps use a wide variety of mechanisms to compress the gas.

Electrochemical – similar to electrochemical separation, gas, ionized at an anode, is driven across an ion-conductive membrane to a cathode. Multistage compressors, which link many membrane-electrode assemblies (MEA) in series can achieve very high pressures (> 1000bar). They are noiseless, scalable, modular and energy efficient.

Purification

Membrane – used similarly to membrane separation, relying on different diffusion rates between the recycled gas and impurities.

Getter – a getter is a reactive material that interacts with contaminants chemically or through adsorption to remove them from the recycled gas.

System complexity

Costs and risks typically go up with increasing system complexity. The primary driver of system complexity is the difficulty of the recycling process. In some cases, a single stage process will be sufficient, other cases will require multiple steps. Other drivers include requirements for:

Scalability – does the system need to support multiple tools and different processes?

Traceability – can the effects contaminants and sub-standard materials be isolated and contained to prevent wide-spread impact?

Duty cycle – is the supported process intermittent or continuous? Are multiple synchronized recycling systems needed to support continuous demand? How much storage capacity is needed to buffer and synchronize intermittent demand? Will the frequency of the duty cycle accommodate any settling or stabilization requirements in the recycling system?

Maintenance and regeneration - are idle periods in intermittent processes sufficiently long to permit maintenance and regeneration?

Availability, redundancy and backup – is the recycling system reliable enough to meet the uptime requirements of the supported process?

Hazard assessment – what risks to fab personnel and the local population are associated with handling and storage of hazardous materials?

Facilities – is space available in the sub-fab or will the system be housed externally?

System complexity options fall into two major categories (**table 1**): single chamber or area (multiple tool) support and open-loop (process waste sent to an offsite refiner) or closed-loop (on-site recycling). A single chamber approach is well suited to continuous processes with constant flow rates and unchanging process reactions. It scales easily to additional systems. An area approach can smooth out the flow from multiple discontinuous process tools and accommodate changes in output concentration caused by varying process reactions. A closed-loop system eliminates supply logistics problems and avoids the need to arrange outbound transport or find a refiner that will accept waste material. An open-loop system provides a supply that is independent of fluctuations in flow rate, shifts the burden of purification to the refiner, and provides batch-level containment of contaminants.

	Single Chamber	Area
Closed	Supply matches demand Scalable Containment of contamination Solves logistics concerns	Multiple asynchronous chambers flatten demand from discontinuous applications
Open	Purity assured by refiner	Amortization of costs across multiple tools Purity assured by refiner

TABLE 1. Compares open-loop, closed-loop, single chamber and area system design options

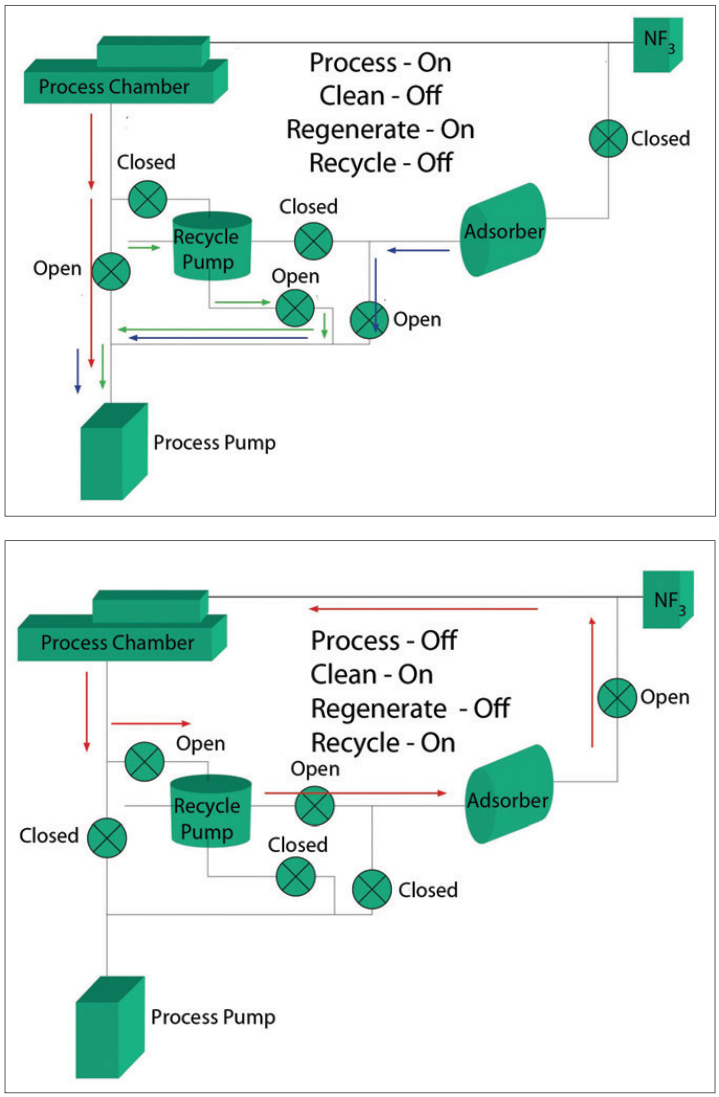

FIGURE 1. Fluorine recycling from a PECVD system requires careful synchronization with deposition and clean cycles to permit regeneration of the PSA adsorbent.

Examples

Edwards has designed and built recycling systems for a variety of applications, including: CF_4, F_2, Xe, SF_6, and H_2. Of these, F_2, Xe, and H_2 are the perhaps the most interesting, for very different reasons.

Fluorine

F_2 is relatively abundant but highly reactive. It is widely used for chamber cleaning. The impetus for this development project was a shortage of NF_3 caused by an increase in demand and a supply hiatus that turned out to be temporary. The system was designed to recover F_2 used to clean a PECVD chamber. The effluent gas stream contained F_2 and SiF_4. During the cleaning phase, exhaust flow was diverted through a pressure swing absorber (PSA), which collected SiF_4 and returned F_2 to the process chamber. During the deposition phase, the PSA was regenerated, with SiF_4 removed by the process pump and abated downstream (**FIGURE 1**). The system required careful synchronization based on signals from the process tool. It was crucial that the ratio of deposition to cleaning was sufficient to allow complete regeneration of the PSA. Interestingly, we found that on-site generation would have provided a simpler and more cost effective solution. Ultimately the problem was solved when the NF_3 supply chain was restored.

Xenon

Xenon is very rare and very stable, both of which is why it is recommend for recycling. Although Xenon currently has no mainstream applications, it has interesting properties that justify continuing investigation, including its behavior in plasma where its use has been considered to support reduced energy ion etch to extend hard mask life. Xenon was also considered for use in EUV light sources. Xenon's scarcity virtually mandates recycling, especially if it were to become part of a widely

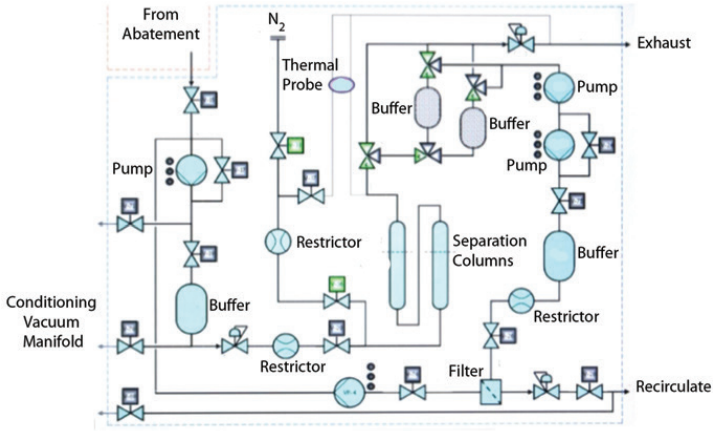

FIGURE 2. Xenon's scarcity and stability make it a strong candidate for recycling should it become widely used. The system shown here -- schematically combined chromatography and membrane separation technologies in a self-contained enclosure that included pumping and back-up storage.

adopted process. In the etch application, the primary hurdle was separating it from other components in the waste stream. Ultimately, the solution was an integrated, self-contained system that included a vacuum pump, a chromatography separator, a membrane separator and a backup supply reservoir (**FIGURE 2**).

Hydrogen

Hydrogen is at the other end of the scarcity/abundance scale from Xenon. It is the most common element in the universe and readily available in some form almost anywhere. It is relatively stable, except that it is highly flammable. The primary recycling challenges are related to safe handling and storage. Hydrogen is already used in many semiconductor manufacturing processes, but the adoption of EUV lithography is expected to dramatically increase hydrogen consumption. EUV light sources use very high hydrogen flows, hundreds of liters per minute, to remove scattered debris that would otherwise contaminate expensive collection optics. The debris originates from Sn, which is injected into the source and irradiated by a high-power laser to create a plasma that emits EUV light. Even without EUV lithography, leading edge fabs may consume as much as several normal cubic meters (Nm_3 = 1000 standard liters) of hydrogen per wafer, equating to hundreds of Nm_3 per hour per fab. Some estimates have that rate doubling with the adoption of EUV lithography. [1]

Given adequate measures to address the safety risks posed by its flammability, hydrogen is a good candidate for recycling (**FIGURE 3**). EUV lithography systems are very expensive ($100M+) and therefore intolerant of downtime. Good recycling system design with adequate provision for redundancy and backup can assure a

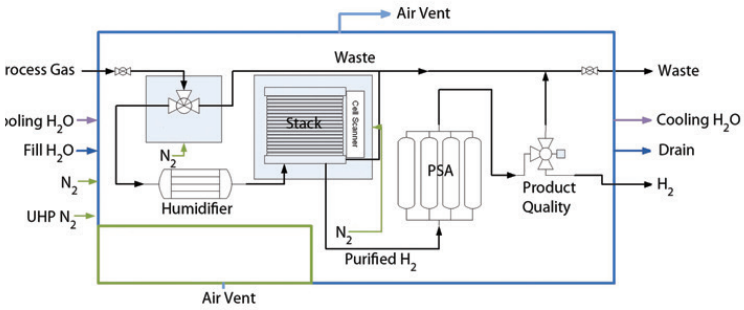

FIGURE 3. Hydrogen recycling may be justified by the dramatic increases in consumption anticipated with the adoption of EUV lithography. Its simple chemistry and continuous flow rate make it a good candidate, in spite of its relative abundance. The primary challenge is the safety risk posed by its flammability.

reliable local source. Hydrogen is consumed in a steady continuous flow. Its recovery involves relatively simple chemistry, and well-proven electrochemical technologies exist for separation and compression. A PSA can be used to remove added water.

Conclusion

Many semiconductor manufacturing processes use only a small fraction of the materials supplied to the process chamber. While we have focused here on recycling gases, it is worth noting that some metal precursors, ruthenium, for example, may also be candidates for recovery and recycling for similar reasons. Proven technologies exist for recovering and recycling unused materials. The value of recycling depends primarily on the cost differential between new and recycled material. The cost of recycling is driven primarily by the technology required and the complexity of the recycling system. Steady state processes and simple chemistries are likely to be the most viable candidates. Discontinuous processes and complex chemistries increase system complexity and add cost and risk. Any consideration of recycling must take a systems-level approach, thoroughly considering all predictable and potential costs, including risks of downtime, contamination and safety. Though recycling of process gases is not now common, there is much to recommend considering it, from both economic and environmental points of view. It represents the kind of out-of-the-box thinking that has contributed again and again to our industry's impressive history of innovation and success.

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OASIS vs GDS: Time to switch?

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Hint: the answer is YES

As foundries advance their process technology, integrated circuit (IC) layout designers have the ability to deliver more functionality in the same chip area. As more content goes into a layout, the file size also increases. The results? Design companies are now dealing with full-chip Graphic Database System (GDSII/GDS™) layouts that are hundreds of gigabytes, or even terabytes, in size. Although additional storage can be purchased relatively inexpensively, storage availability is becoming an ongoing and increasingly larger concern.

And storage is not the only, or even the most important, issue. File size and layout loading time become increasingly critical concerns as process technology advances. Electronic design automation (EDA) tools can struggle to effectively manage these larger layouts, resulting in longer loading times that can frustrate users and impact aggressive tape-out schedules. Layout loading happens repeatedly throughout the design process—every time designers create or modify a layout, check timing, run simulations, run physical verification, or even just view a layout—so the effect of loading time becomes cumulative throughout the design and verification flow.

Layout designers often try to address the file size problem by zipping their GDS layouts. This approach does reduce file sizes, but it can actually increase loading times, as tools must unzip the file before they can access the data. Need a better, more permanent, solution?

Switch to the Open Artwork System Interchange Standard (OASIS®) format, which can reduce both file sizes and loading times. The OASIS format has been available for almost 15 years [1] and is accepted by every major foundry. It is also supported by all industry standard EDA tools [2].

The OASIS format has several features that help reduce file size compared to the GDS format.

- OASIS data represents numerical values with variable byte lengths, whereas the GDS format uses fixed byte lengths.
- OASIS functionality can also recognize complex patterns within a layout and store them as repetitions, rather than as individual instances or geometry objects.
- The OASIS CBLOCKs feature applies Gzip compression to the individual cells within a layout. Because this compression is internal to the file, tools do not need to create a temporary uncompressed file, which is often necessary with normal Gzip compression. Additionally, although unzipping a Gzip file is typically a single-threaded process, CBLOCKs can be uncompressed in parallel.
- Strict mode OASIS layouts contain an internal lookup table that can tell a reader the location of different cells within the file. This information allows the reader to more efficiently parallelize the loading of the layout and can offer significant loading time improvement.

Although features such as CBLOCK compression and strict mode are not required, it is highly recommended that layout designers utilize both to realize the fastest loading times in their tools while maintaining small file sizes.

What's wrong with gds.gz?

Many layout designers have resorted to zipping their GDS layouts, which in measured testcases reduced file sizes by an average of 85%. However, beyond cell placements, designs typically contain a lot of repetition that is not recognized by the GDS format. As a result, much of a GDS file is redundant information, which is why zipping a GDS layout can achieve such significant compression ratios. The OASIS format natively recognizes this repetition and stores this information more compactly. Additionally, taking advantage of

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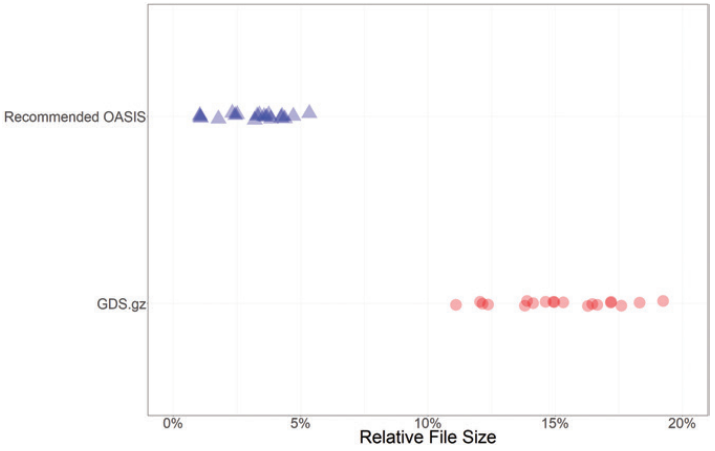

FIGURE 1. File sizes relative to the uncompressed GDS layout (smaller is better). In all measured testcases, the recommended OASIS options delivered smaller file sizes than zipping the uncompressed GDS layout.

CBLOCKs reduced file sizes by an additional 80% from the zipped GDS layouts and by almost 97% from the uncompressed GDS layouts. **FIGURE 1** shows the file size reduction that can be achieved by using the OASIS format instead of a zipped GDS layout.

In addition, a zipped GDS layout's file size reductions are usually offset by longer loading times, as tools must first unzip the layout. As seen in **FIGURE 2**, the DRC tool took, on average, 25% longer to load the zipped GDS layout than the corresponding uncompressed GDS layout. Not only were the corresponding recommended OASIS layouts smaller, the DRC tool was able to load them faster than the uncompressed GDS layouts in all measured testcases, with improvements ranging from 65% to over 90%.

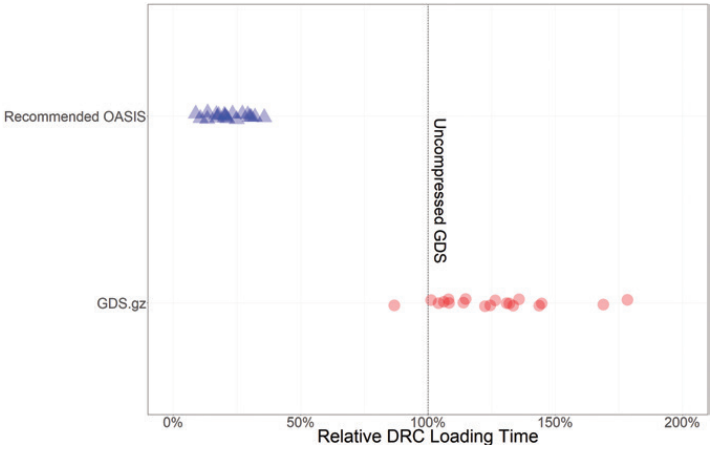

FIGURE 2. DRC loading times relative to the uncompressed GDS layout (smaller is better). In all measured testcases, the recommended OASIS options delivered faster DRC loading times than zipping the uncompressed GDS layout.

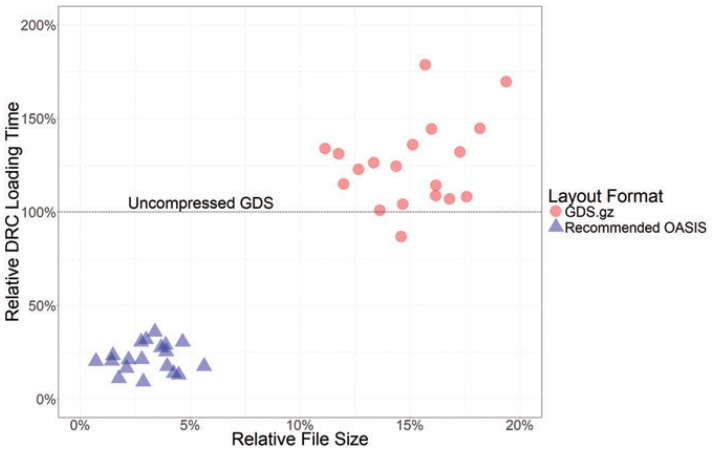

FIGURE 3. DRC loading times versus file size, both relative to the uncompressed GDS layout (smaller is better for both axes). In all measured testcases, the recommended OASIS options delivered faster DRC loading times and smaller file sizes than zipping the uncompressed GDS layout.

While Figs. 1 and 2 considered file sizes and loading times separately, the reality is that layout designers must deal with both together. As seen in **FIGURE 3**, plotting both quantities on the same chart makes it even clearer that the recommended OASIS options deliver significant benefits in terms of both file size and loading time.

Loading time costs are incurred throughout the design process every time a user runs physical verification or even just views a layout. DRC tools are typically run in batch mode, where slow loading performance may not be as readily apparent. However, when viewing a layout, users must actively wait for the layout to load, which can be very frustrating. As seen in **FIGURE 4**, viewing a zipped GDS layout took up to 30% longer than viewing the uncompressed GDS layout. In addition to the file

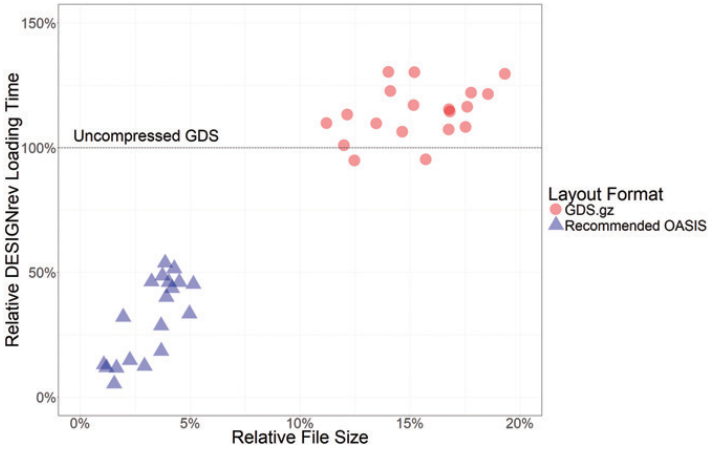

FIGURE 4. Layout viewer loading times versus file size, both relative to the uncompressed GDS layout (smaller is better for both axes). In all measured testcases, the recommended OASIS options also delivered faster loading times than zipping the uncompressed GDS layout.

size reduction of almost 80% (compared to the zipped GDS layout), switching to the OASIS format with the recommended options reduced the loading time in the layout viewer by an average of over 70%.

What about zipping an OASIS layout?

Layout designers may think that zipping an OASIS layout can provide additional file size reductions. However, CBLOCKs and Gzip use similar compression algorithms, so using both compression methods typically provides only minimal file size reductions, while loading times actually increase because tools must uncompress the same file twice.

In a few cases, zipping an uncompressed OASIS layout may reduce file sizes more than using CBLOCKs. However, layout readers cannot load a zipped OASIS layout in parallel without first unzipping the file, which leads to increased loading times. As seen in **FIGURE 5**, the zipped OASIS layout had 6% smaller file sizes when compared to the recommended OASIS layout. However, DRC loading times increased by an average of over 60% to offset this benefit, and, in several cases, the loading time more than doubled.

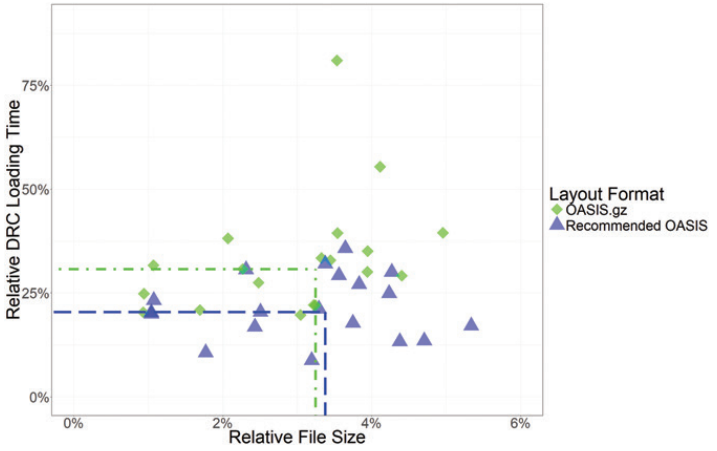

FIGURE 5. DRC loading time versus file size, both relative to the uncompressed GDS layout (smaller is better for both axes), with the means of both axes overlaid. There is a small file size reduction when zipping the uncompressed OASIS layout, but there is a significant loading time penalty.

What should I do next?

At 16 nm and smaller nodes, block-level and full-chip layouts should be in the OASIS format, specifically with the strict mode and CBLOCKs options enabled. Moving flows to utilize these recommendations can provide dramatically smaller file sizes and faster loading times.

Maintaining data integrity is critical, so layout designers may want to first switch a previous project to the OASIS format to reduce the risk and see firsthand the benefits of switching. They can also run an XOR function to convince themselves that no data is lost by switching to the OASIS format. Additionally, every time physical verification is run on an OASIS layout, it is another check that the layout is correct.

Layout designers can convert their layouts to the OASIS format using industry-standard layout viewers and editors. For best results, designers should enable both CBLOCKs and strict mode when exporting the layout. Designers should also confirm that these features are utilized in their chip assembly flow to reduce the loading time when running full-chip physical verification using their DRC tool.

Conclusion

File size and layout loading time have become increasingly important concerns as process technology advances. While storage is relatively inexpensive, it is an unnecessary and avoidable cost. Longer layout loading times encountered throughout the design process are similarly preventable.

The OASIS format has been around for almost 15 years, is accepted by every major foundry, and is supported by all industry-standard EDA tools. Switching to the OASIS format and utilizing features such as CBLOCKs and strict mode can provide users with dramatically smaller file sizes and faster loading times, with no loss of data integrity. ◆

IEDM 2018 preview

The annual International Electron Devices Meeting (IEDM) conference will be held December 1-5, 2018 at the Hilton San Francisco Union Square Hotel. In this issue, we'll give a preview of what will be presented, including paths to extreme scaling in advanced CMOS logic devices and DRAM memories, quantum computing devices, 5G, wide bandgap power electronics, and interconnect scaling challenges and solutions.

Extreme scaling for logic and memories

Since the integrated circuit (IC) was invented in the late 1950s, the continued scaling of transistors and related devices to smaller dimensions and higher levels of integration has led to increasingly powerful computers and other electronic systems. Continued scaling has now become tremendously expensive, yet it remains vital to developing the ultra-fast, lower-power processors and denser memories needed for demanding applications such as artificial intelligence (AI), graphics processing, cloud computing and others. Two noteworthy late-news papers, from Samsung and Imec, will describe paths to extreme scaling in advanced CMOS logic devices and DRAM memories, respectively.

First Steps Toward 3nm CMOS Technology: Samsung researchers will describe their 3nm CMOS technology featuring gate-all-around (GAA) transistors with channels made from horizontal layers of nanosheets that are completely surrounded by gate structures. Samsung calls this a Multi-Bridge-Channel architecture, and says it is highly manufacturable as it makes use of ~90% of the company's existing FinFET fabrication technology, requiring only a few revised photomasks. They built a fully functioning high-density SRAM macro with it. They say the process demonstrates excellent gate controllability (65 mV/dec subthreshold swing), 31% higher on-current than the company's FinFET technology, and offers design flexibility because the nanosheet channel widths can be varied by means of direct patterning. *(Paper #28.7, "3nm GAA Technology Featuring Multi-Bridge-Channel FET for Low-Power and High-Performance Applications," G. Bae et al, Samsung)*

Scaling DRAM Technology To 16nm And Beyond: DRAM memory technology is used in virtually all electronic systems because of its speed and density. DRAM memory comprises arrays of capacitor-transistor pairs which store data as electrical charge in the capacitor; the presence of charge indicates "1" and its absence "0." Manipulation of these digits is the basis of computer programming. It's difficult to scale DRAM to the 16nm generation and beyond because of space limitations which make it hard to pack enough capacitance within the pitch. Imec researchers used an atomic layer deposition (ALD) process to pattern and build a novel 11nm pillar-shaped capacitor using new dielectric materials ($SrTiO_3$, or STO). By tailoring the material properties of the capacitor and the $SrRuO_3$ (SRO) epitaxial template on which it was grown, the researchers achieved a very high dielectric constant (k~118) and low electrical leakage (10^{-7} A/cm^2 at ±1V). This means that pillar-shaped capacitors can be used instead of existing cup-shaped capacitors, without paying too great a penalty in terms of reduced data-storage capability. These results make the STO capacitors suitable for continued scaling for 16nm and smaller DRAMs. *(Paper #2.7, "High-Performance (EOT<0.4nm, Jg~10^{-7} A/cm^2) ALD-Deposited Ru/SrTiO3 Stack for Next-Generation DRAM Pillar Capacitor," M. Popovici et al, Imec)*

Neural networks/artificial intelligence/neuromorphic computing

Analog Synaptic Cell Based On Ferroelectric FET for DNNs: Deep neural networks (DNNs) are used in machine learning for tasks such as image and speech recognition. Work is ongoing to make faster, more energy-efficient DNNs by optimizing their training and inferencing operations. Current von Neumann-based DNN architectures move data back and forth between memory and processors, which limits speed and power efficiency and, hence, overall DNN performance. A team of university researchers participating in the SRC/DARPA-sponsored ASCENT program will describe an in-memory computing architecture in which computing is done at the location of the data storage to accelerate training. This approach also trades unnecessarily high levels of precision during inferencing for greater speed and energy efficiency. Previous such "in-memory computing" approaches have made use of various non-volatile memories (NVMs), but their overall accuracy has suffered. Here, the team proposes a novel compact analog synaptic weight cell consisting of two MOSFETs and one ferroelectric transistor (2T-1FeFET) to handle both the training and inferencing functions. They validated its performance based on an experimentally validated FeFET

SPICE model and embedded in a convolutional neural network using both the MNIST and CIFAR-10 training datasets, and achieved accuracies of ~97.3% and ~87%, respectively. *(Paper #3.2, "Exploiting Hybrid Precision for Training and Inference: A 2T-1FeFET-Based Analog Synaptic Weight Cell," X. Sun et al, Arizona State Univ./Univ. Notre Dame/Georgia Institute of Technology)*

Electrochemical Synaptic Cell: Various non-volatile memory technologies such as RRAM and PCM are being investigated for use as synaptic cells for neuromorphic computing, but they tend to have non-ideal switching characteristics (e.g., asymmetric weight update, limited endurance, and elevated levels of stochasticity, or random behavior). Instead, IBM researchers will describe a novel scalable electrochemical random access memory (ECRAM) device based on lithium (Li) ion intercalation in tungsten oxide (WO_3) that can be used as a scalable synaptic cell (**FIGURE 1**). These non-volatile ECRAMs showed high levels of switching symmetry and linearity, good data retention, and up to 1,000 discrete conductance levels useful for multi-level operation in large memory arrays. The researchers demonstrated successful high-speed programming, using 5ns pulse widths with 300x300nm^2 ECRAM devices. Ultra-low switching energy of 1 fJ is projected for scaled 100x100nm^2 devices. MNIST image-recognition simulations based on experimental data showed 96% accuracy. *(Paper #13.1, "ECRAM as Scalable Synaptic Cell for High-Speed, Low-Power Neuromorphic Computing," J. Tang et al, IBM)*

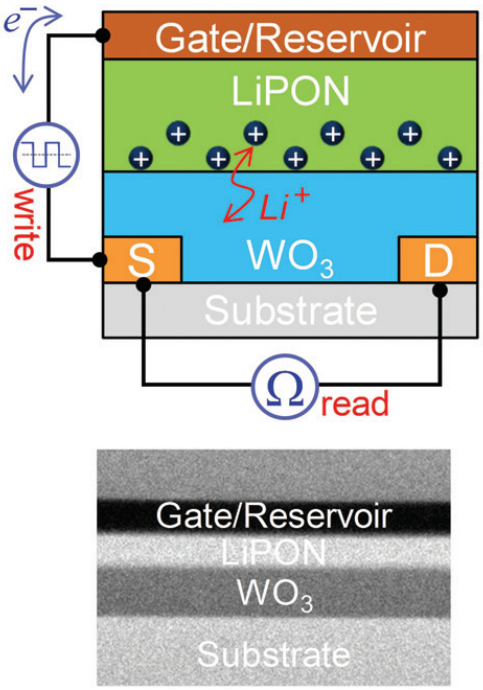

FIGURE 1. A schematic of the ECRAM device (on top) and a cross-sectional electron microscope image (below it).

Memory technology

Intel Integrates e-MRAM With 22nm FinFETs: Embedded non-volatile memory (e-NVM) technologies, which retain data when power is turned off, are essential for Internet of Things (IoT), mobile and other applications, but the dominant embedded technology, e-flash, suffers from cost and scaling issues. Embedded MRAM (magnetoresistive random access memory), with its low manufacturing costs and high data retention and switching endurance, is a compelling alternative. It also has the potential to replace other types of embedded memory besides e-flash, and to serve as a building block for future logic devices as well. Integrating MRAM with mainstream CMOS technology has been problematic for various reasons, but Intel researchers will describe the successful integration of embedded MRAM into the company's ultra-low-power 22nm FinFET CMOS technology on full 300mm wafers (**FIGURE 2**). The work represents a major step forward toward commercial use of the technology for high-performance, low-power applications. The magnetic tunnel junction-based memory cells are built from dual MgO magnetic tunnel junctions (MTJs) separated by a CoFeB-based layer in a 1 transistor-1 resistor (1T-1R) configuration in the interconnect stack. To demonstrate their performance, Intel built 7.2 Mb MRAM arrays which achieved industry-leading data retention (10 years with <1e-6 error rate at 200°C) and endurance (>10^6 write endurance). *(Paper #18.1, "MRAM as Embedded Non-Volatile Memory Solution for 22FFL FinFET Technology," O. Golonzka et al, Intel)*

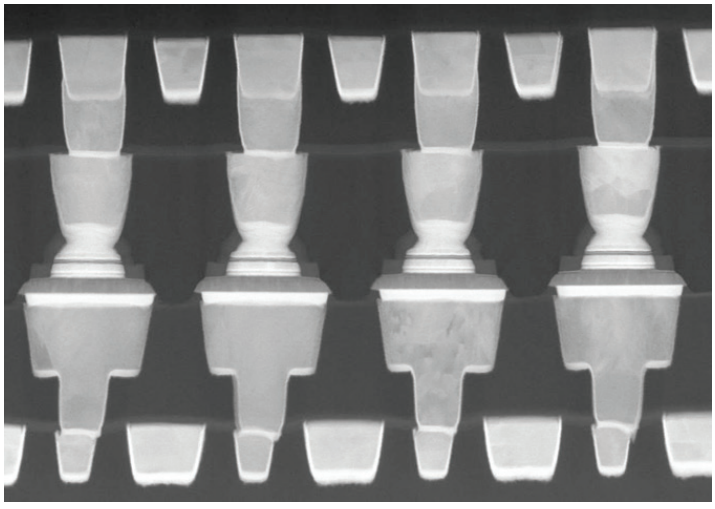

FIGURE 2. An electron microscope image showing the cross-section of the MTJ array, which is embedded between Metal 2 and Metal 4 in Intel's 22nm FinFET logic process.

Advances in CMOS Technology

Highest-Density 3DS Stacked FinFETs: Imec researchers will report on 3D stacked FinFETs that have the tightest pitches ever reported in such a stacked architecture – 45nm fin pitch and 110nm gate pitch (**FIGURE 3**). The 3D architecture makes use of a sequential integration process yielding tight alignment between very thin top and bottom Si layers. The junction-less devices in the top layer were fabricated and transferred using low-temperature (≤525°C) processes to avoid performance degradation, and a 170nm dielectric was used to bond the two wafers. The top layer is so thin that the bottom layer could be patterned right through it by means of 193nm immersion lithography, which connects the two via local interconnect. The researchers evaluated various gate stacks, ultimately choosing TiN/TiAl/TiN/HfO_2 with a $LaSiO_x$ dipole inserted into the stack. The combination demonstrated good threshold voltage tuning, reliability and low-temperature performance. *(Paper #7.1, "First Demonstration of 3D Stacked FinFETs at a 45nm Fin Pitch and 110nm Gate Pitch Technology on 300mm Wafers," A. Vandooren et al, Imec)*

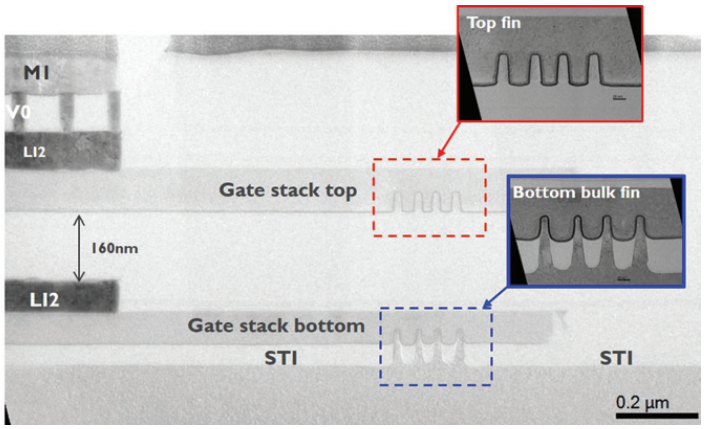

FIGURE 3. A cross-sectional image of the final devices across fins with the gates covering the fins.

Ge Channels For CMOS: To build higher-performance CMOS devices, replacing their silicon (Si) channels with ones made from germanium (Ge) is a promising approach because Ge has greater electron and hole mobility than Si. Ge P-FETs have shown great potential and SiGe P-FETs are commonly used in CMOS technologies. However, one issue is that CMOS devices are built from both N-FETs and P-FETs and it has been challenging to build high-quality Ge N-FET gate stacks because of internal material defects and high contact resistance. TSMC researchers will report how they overcame these N-FET roadblocks to achieve low Dit hysteresis-free P- and N-type Ge nanowire gate stacks combined with record low N-FET/metal contact resistivity (1.6e-9Ωcm^2). Key to the effort was a multi-layer in-situ doped epitaxy process that enabled high dopant activation. Based on this they built the industry's first vertically stacked Ge high-k nanowire gate stacks that meet all requirements for use in CMOS devices, and demonstrated high performance GAA Ge nanowire P-FETs with diameter scaling down to 6nm (**FIGURE 4**). The work paves the way for the possibility of fully complementary Ge-based devices in future technology nodes. (Paper 21.1, "Ge CMOS Gate Stack and Contact Development for Vertically Stacked Lateral Nanowire FETs," M.J.H. van Dal et al, TSMC)

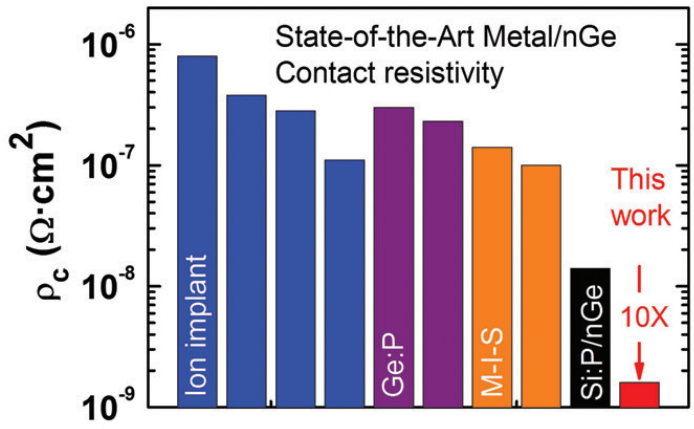

FIGURE 4. Low contact resistivity of N-type Ge which resulted from the combination of multi-layer in-situ doped epitaxy and nanosecond laser anneal in this work versus other fabrication techniques.

InGaAs Channels For High-Mobility N-FET Nanosheets: IBM researchers, on the other hand, did look to III-V materials as a replacement for Si channels. They monolithically integrated high-performance InGaAs gate-all-around nanosheet N-FETs on Si using what they call a "Template-Assisted-Selective-Epitaxy" (TASE) process designed to integrate high-mobility material formed into nanoscale sheets. The nanosheets are scaled to 10nm thicknesses and the transistors have <40nm gate lengths, with the gate metal wrapping around the channel for optimal gate control. The devices demonstrated excellent current drive capability (I_{on}=355µA/µm), as well as subthreshold swing of 72 mV/decade. The researchers say device performance can be further improved by scaling gate length/nanosheet dimensions. The devices are compatible with current silicon manufacturing tooling. *(Paper #39.2, "High-Performance InGaAs Gate-All-Around Nanosheet FET on Si Using Template-Assisted Selective Epitaxy," S. Lee et al, IBM)* ◆

The ASOPS system as a multiphysics measurement device for research and industry

WILFRIED VOGEL, *NETA, Talence, France*

Insights into the rise of ASynchronous OPtical Sampling technology as a future measurement standard and how it can be used in the industry.

Downsizing and thinning all the electronic parts has always been a trend in our modern era. However, the nanoscience and nanotechnologies were still science fiction in the '60s and the word nanotechnology was used for the first time in 1974. At the same time, the first atomic force microscopes (AFM) and scanning acoustic microscopes (SAM) were developed. Today nanotechnologies represent huge investments - even from governments - and a global market of several thousand of billions of euros.

Non-destructive testing at the nanometric scale is the purpose here. Ultrasounds are widely used in the aeronautics industry or during medical echography. The spatial resolution reached in that case is around the millimeter which is a million time too large when we speak of nanotechnologies.

FIGURE 1. JAX imaging system.

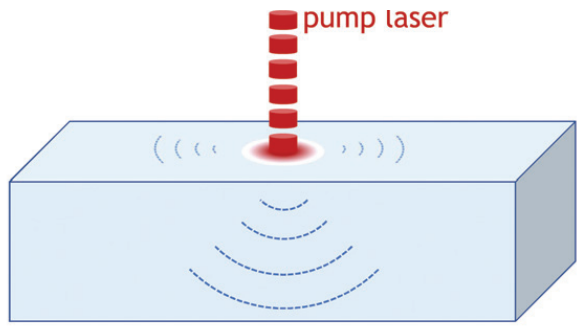

FIGURE 2. ASOPS principle: ultrasound generation.

SAM systems benefit from a higher definition thanks to MHz/GHz ultrasounds, the smallest axial resolution found on the market is below the micron.

The nanometric world requires another 2 to 3 orders of magnitude below and it can only be reached thanks to THz ultrasounds. These frequencies cannot be generated with standard transductors, that's why the ASynchronous OPtical Sampling (ASOPS) systems are equipped with ultrafast lasers.

This complex technology is now available on the market in a compact instrument. The JAX is the first industrial imaging ASOPS system (**FIGURE 1**).

When the pump hits the surface, the most part of the energy is absorbed by the first layers of atoms and converted into heat without damaging the sample (**FIGURE 2**), leading to transient thermoelastic expansion

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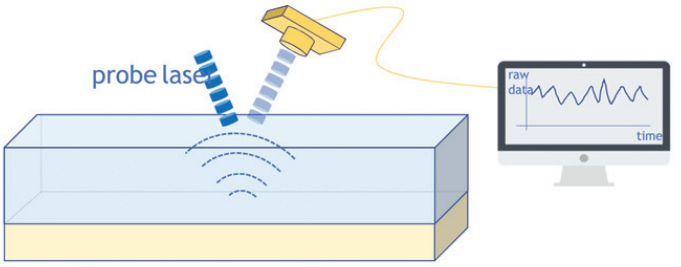


FIGURE 3. ASOPS principle: ultrasound detection.

and ultrasound emission. The choice of the probe is also important to keep the temporal and the spatial resolution as low as possible, that's why another ultrafast laser is used as a probe (**FIGURE 3**).

The elastic answer of the thin film to a pump excitation is too fast to be measured in real time. You have to artificially extend time and reconstruct the signal of the probe.

The ultrasound is propagating a few nanometers per picosecond through the thin film and at some point will bounce back partially or completely to come back to the surface when meeting a different medium.

The probe laser is focused at the surface, when the ultrasound hits back the surface, the reflectivity fluctuates locally over time. The variation of reflectivity is detected and stored into the computer as a raw data. This technique is often called *picosecond ultrasonics*, it has been developed at Brown University in the USA by Humphrey Maris in the mid 80's.

The ASOPS is not the only kind of technology able to perform picosecond ultrasonics, but it's the latest evolution and the fastest to perform a full measurement. The trick here is to slightly shift the frequency of the probe laser compared to the pump's one (**FIGURE 4**). Both lasers are synchronized by a separate electronical unit. The probe arrives slightly after the pump and this delay is extending with time until the whole sampling is over.

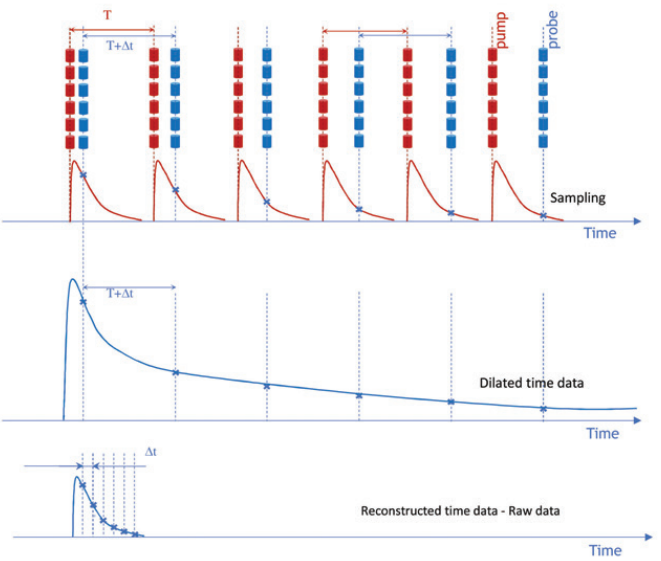


FIGURE 4. Asynchronous pump and probe lasers sampling concept.

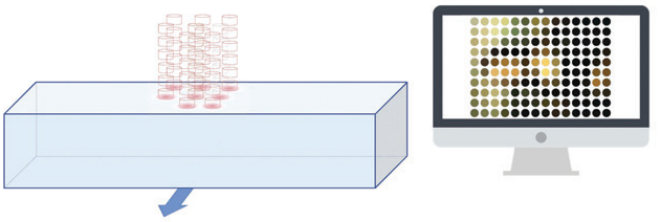


FIGURE 5. Mapping of sample's thickness.

The measure described above is for one single point. With a more standard instrument able to perform picosecond ultrasonics, it would take several minutes. Here with the ASOPS, the measure takes less than a second. It means that by simply scanning point by point all over the surface (**FIGURE 5**), you will get a full map of the studied mechanical parameter in minutes.

Thickness measurement

For instance, if your interest is in the thickness of a thin film, you can easily retrieve an accurate value by measuring the time between two echoes of the ultrasound at the surface of the sample (**FIGURE 6**).

Until recently, the kind of setup required to make these measurements was found in a optical lab with a large honeycomb table full of mirrors and lenses. Even though the results are respectable, the time to install and repeatability are often the main issue.

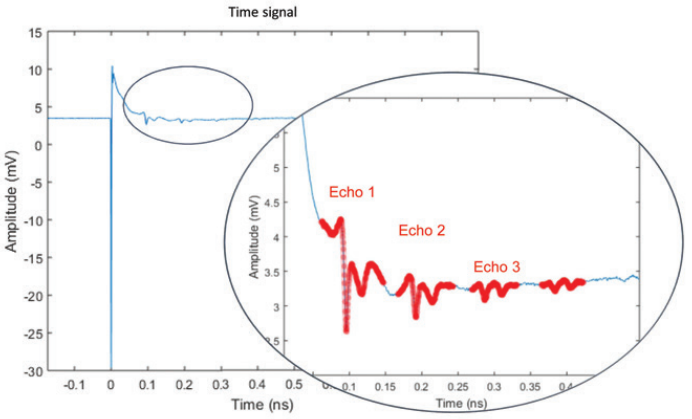


FIGURE 6. Example of raw data.

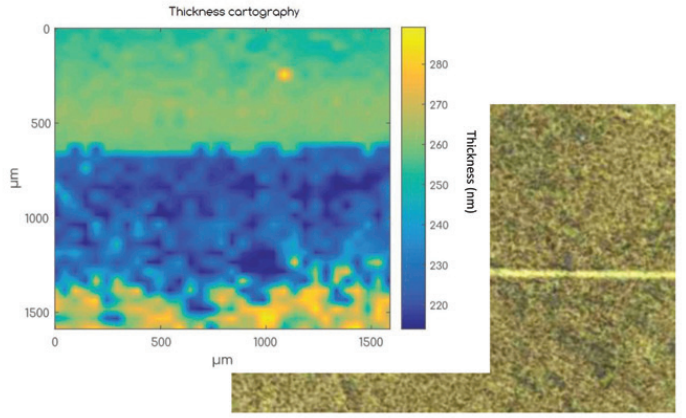


FIG. 7: Example of sample thickness mapping with ASOPS system / microscope view of the sample

Hopefully the technology is now accessible for non-specialists who just want to focus on measuring the mechanical properties of their samples and not to take care of all the optical part. The industrialization of such an innovative and complex device is giving an easy access to new information.

Since a punctual measurement takes a few milliseconds, it is easily feasible to measure all over the surface of the sample and get a full mapping of the thickness.

In the example below (**FIGURE 7**), the sample consists of a 500 µm silicon substrate and 255 nm sputtered tungsten single layer. The scanned surface is approximately 1.6 mm x 1.6 mm and the lateral resolution in X-Y is 50 µm, 999 points in total.

A large scratch is being highlighted at the surface but the average thickness remains in the range of 250 nm. The total time of measurement is less than 10 minutes, which is comparable to a single point measurement with one laser and a mechanical delay line (homodyne system).

Until now, the industry offer for production management was only homodyne instruments performing picosecond ultrasonics measurements, reducing the full scan of the surface to a very few points checked only over a full wafer.

We just saw that single layer thin film thickness measurement is pretty straight forward. If you are dealing with more than one layer the raw data is much more complex to read. However, it is possible to model the sample and to compare the simulated signal to the actual measure with an incredible fit.

Multiphysics

When you chat with several experts of thin films, they will all agree to tell you that:

- Thickness is a key parameter
- Adhesion is always a problem
- Non-destructive measurement is a fine improvement
- Faster is better
- Imaging is awesome

In the industry, thickness and adhesion are the main concern at all steps of the manufacturing process, whether you are working in the display or the semiconductor field. The picosecond ultrasonics technique is already used in-line for wafer inspection, which shows its maturity and yet confidentiality.

The standard procedures for adhesion measurement are applicable only on flat and large samples, and they are destructive. When it comes to 3D samples and if you want to check the adhesion on a very small surface, the laser is the only solution. Adhesion can now be verified inline all over the sample during every step of the manufacturing process.

Now the academic world has different concerns and goes deeper and deeper in the understanding of the material behavior at the atomic scale.

The ASOPS system can go beyond the picosecond ultrasonics -- which is already a great source of information if we stick to thickness and adhesion -- and get even more from the raw data such as thermal information or critical mechanical parameters.

Thermal conductivity

Thermal conductivity is the parameter representing the heat conducting capability of a material.

Thin films, superlattices, graphene, and all related materials are of broad technological interest for applications including transistors, memory, optoelectronic devices, MEMS, photovoltaics and more. Thermal performance is a key consideration in many of these applications, motivating efforts to measure the thermal conductivity of these films. The thermal conductivity of thin film materials is usually smaller than that of their bulk counterparts, sometimes dramatically so.

Compared to bulk single crystals, many thin films have more impurities which tend to reduce the thermal conductivity. Besides even an atomically perfect thin film is expected to have reduced thermal conductivity due to phonon leakage or related interactions.

Using pulsed lasers is one of the many possibilities to measure the thermal conductivity of a thin material.

The time-domain thermoreflectance (TDTR) is a method by which the thermal properties of a material can be measured. It is even more suitable for thin films materials, which have properties that vary greatly when compared to the same materials in bulk.

The temperature increase due to the laser can be written as follows :

$$\Delta T(z) = (1-R)\frac{Q}{C(\zeta A)}\exp(-\frac{z}{\zeta})$$

where R is the sample reflectivity,
Q is the optical pulse energy,
C is the specific heat per unit volume,
A is the optical spot area,
ζ is the optical absorption length,
z is the distance into the sample

The voltage measured by the photodetector is proportional to the variation of R, it is possible then to deduce the thermal conductivity.

In some configuration, it can be useful to shoot the probe on the bottom of the sample (**FIGURE 8**) or vice versa in order to get more accurate signal from one side or the other of the sample.

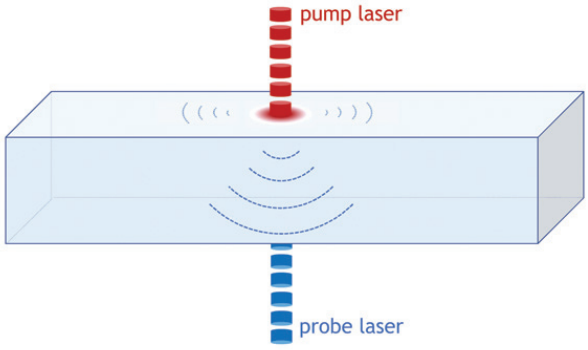


FIG. 8: ASOPS principle: Top / Bottom configuration

Surface acoustic wave

When the pump laser hits the surface, the ultrasound generated is actually made of two distinct waves modes, one propagating in the bulk, which is called longitudinal (see Fig. 2), one traveling along the surface, it's called the Rayleigh mode.

In the industry the detection of surface acoustic wave (SAW) is used to detect and characterize cracks.

The surface wave is very sensitive to the presence and characteristics of the surface coatings, even when they are much thinner than the penetration depth of the wave.

Young's Modulus can be determined by measuring the velocity of the surface waves.

The propagation velocity of the surface waves, c, in a homogeneous isotropic medium is related to:

the Young's modulus E,
the Poisson's ratio ν,
the density ρ

by the following approximate relation

$$c = \frac{0.87+1.12\nu}{1+\nu}\sqrt{\frac{E}{2\rho(1+\nu)}}$$

When using an industrial ASOPS system to measure and image the SAW, the pump laser is fixed (Fig. 8) and always hitting the same spot. The probe is measuring its signal around the pump laser thanks to a scanner installed in the instrument.

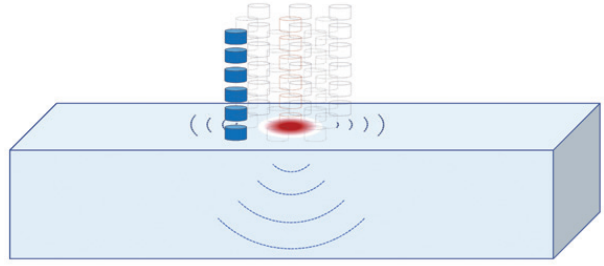
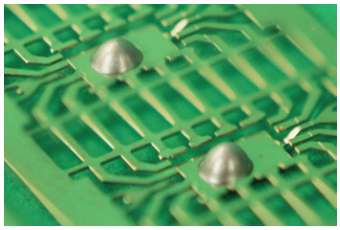


FIGURE 9. Surface acoustic wave detection.

Future challenges

Today ASOPS technology is moving from the margin to the mainstream. The academic community already recognizes this non-destructive technology as truly operational and able to deliver reliable and accurate measurements. For industrial applications, ASOPS systems will most certainly begin to replace standard systems in the short term and to fill the gap of ultrasonic inspection at nanometric scale. It is also easily nestable in the production line while some other instruments are meant to remain research devices because they require much more care, vacuum pumps, complex settings etc.

However, the industry is far from done exploiting the full range of capabilities offered by ASOPS systems, this versatile technology also continues to be developed and validated for a broad range of other critical applications. Indeed, ASOPS systems has already shown a great potential on biological cell research. We can expect new developments to be done in the future and see instruments help the early disease detection within the next few years. ◆



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Six leading startups driving Japan's AI

YOICHIRO ANDO, *marketing director, SEMI Japan*

Artificial intelligence (AI) is on the verge of transforming entire industries as it gears up to power semiconductor industry innovation and growth, thrusting the technology to front and center at SEMICON Japan 2019, December 12-14 at the Tokyo Big Sight (Tokyo International Exhibition Center).

A number of Japanese startups are on leading edge of AI innovation in machine and deep learning. One is Preferred Networks Inc., a company that applies cutting-edge deep learning technology to Internet of Things (IoT) applications across transportation, manufacturing and healthcare.

In his opening day keynote at SEMICON Japan 2019, Toru Nishikawa, president and CEO of Preferred Networks, Inc., will highlight the latest developments and promise of using deep learning for industrial applications. Nishikawa will unpack how AI companies jockeying for competitive advantage will win by harnessing technologies to process massive amounts of data efficiently and quickly.

Following is look at Preferred Networks, Inc. and five other Japanese startups that are driving AI innovation.

SC Japan Preferred Networks

Within Japan's world of AI, machine learning, and deep dearning, Preferred Networks is likely the most well-known Japanese company. The parent company, Preferred Infrastructure, was founded in March 2006 by Toru Nishikawa and Daisuke Okanohara, who focused on search engine development before turning to machine learning and establishing Preferred Networks to commercialize the technology.

Preferred Networks established itself as one of the world's top providers of machine learning technology with the development of Chainer – an open source deep learning framework that has been offered free of charge since June 2015 and was released before TensorFlow, Google's renowned Deep Learning framework.

SC Japan Abeja

Established in 2012, ABEJA is thought to be Japan's first venture company to specialize in deep learning. ABEJA's core technology is its AI platform ABEJA Platform. Based on this platform, the company offers various solutions to more than 100 client companies. ABEJA also offers ABEJA Insight, a specialized package service for the retail and distribution, manufacturing, and infrastructure industries.

SC Japan BrainPadData analytics provider BrainPad Inc. was the first Japanese AI venture listed on the Tokyo Stock Exchange. Established in 2004, before the advent of big data, BrainPad Inc. cultivated a vision of analyzing vast amounts of data in increase the competitiveness of Japanese companies.

SC Japan Leapmind

LeapMind Inc. aims to offer deep learning technology that uses fewer computing resources and draws less power. Both are important capabilities since deep learning requires considerable computing resources to perform image and speech recognition. The company's answer to this deep learning challenge is a small form factor FPGA with low power consumption.

In April 2018, LeapMind started offering the tool DeLTA-Lite to support model construction for Deep Learning. The tool simplifies the development of deep learning design models, eliminating the need for model design, hardware, and software expertise.

SC Japan Hacarus

Hacarus Inc.'s HACARUS-X AI technology, which combines sparse modeling and machine learning technology, features low power consumption and small devices such as FPGAs. In collaboration with semiconductor trading company PALTEK, Hacarus is integrating HACARUS-X algorithms with Xilinx's FPGA Zynq UltraScale + MPSoC. Both companies area also implementing HACARUS-X algorithms in a box computer.

Sparse modeling is gaining attention as a modeling method by which humans can understand the judgment process of AI by extracting features from a small amount of learning data.

SC Japan LPixel

With expertise in life science fields such as medical and biology and image processing technology, LPixel, Inc. develops image analysis systems with original algorithms and machine learning techniques. It has developed a cloud-based AI image analysis platform and an AI medical image diagnosis support technology that streamlines the review of large amounts of research data and detects image fraud in research papers and other documents for the medical and biology fields, freeing researchers to devote more time to their core work. ◆

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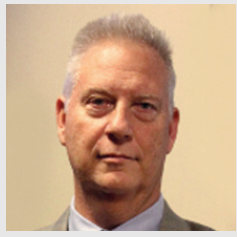

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