Solid State TECHNOLOGY

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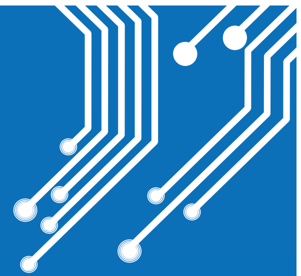

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10 Reasons to Attend The ConFab 2016

The ConFab Conference and Networking Event will be held June 12-15. Presented by Solid State Technology, this executive-level event is designed exclusively for those driving growth and innovation in the semiconductor industry. Here are 10 reasons to register now.

1. The keynotes. Hear from Dr. Thomas Caulfield, senior vice president and general manager of GlobalFoundries' latest leading-edge 300mm semiconductor wafer manufacturing facility; Sunny Hui, senior vice president of worldwide marketing, Semiconductor Manufacturing International Corp., and Bill McClean, President of IC Insights.

2. The networking. The semiconductor industry has undergone unprecedented consolidation over the last year and the only way to know who's who in the new landscape it to get out and talk to people. There are plenty of opportunities to get together at breakfast, lunch and for evening receptions.

3. The meetings. We arrange strategic meetings between technology suppliers and manufacturers, including IDMs, foundries and OSATs. Fabless companies, which are increasingly driving manufacturing decisions, are also involved.

4. The big picture. You'll walk away with a high level overview of the myriad of challenges and opportunities now facing the semiconductor industry.

5. The semiconductor industry needs to change the way it thinks about innovation, both technical innovation and business model innovation, especially when it comes to the Internet of Things (IoT).

6. Fab Management. Today's fab managers must continually be thinking of ways to improve operational efficiency, optimize asset utilization, boost tool and worker productivity (and safety), increase throughput, maximize yield and reduce defectivity.

7. System Level Integration: New Directions in Packaging. How will these technologies be used in advanced data centers & network systems, in future smart phones, and the growing medical, industrial and lifestyle IoT applications?

8. China. We will examine how the China "wild card" and increased M&A activity designed to bring advanced technology into China is a true game-changer for the worldwide semiconductor industry.

9. Great location. The ConFab will take place at the beautiful Encore at The Wynn right in downtown Las Vegas.

10. Collaboration. It's clear that the need for real collaboration has never been greater. At The ConFab, industry leaders will gather to tackle tough questions, take a look at the new post-consolidation landscape, network in a unique environment and collaborate on the future.

I hope to see you there! Check out **www.theconfab.com** for more information.

—Pete Singer, Editor-in-Chief

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Web Exclusives

Synopsys debuts tools at Users Group Meeting

Aart de Geus, the chairman and co-chief executive officer of Synopsys, used his keynote address at the 2016 Synopsys Users Group conference in Silicon Valley to tout a pair of new products. (From SemiMD.com)

http://bit.ly/1PShzIn

A new virtuous cycle for the MEMS industry

Since 2000, we have entered the age of sensing and interacting with the wide diffusion of MEMS and sensors that give us a better, safer perception of our environment. MEMS have grown in volume to be almost a 15 billion units market today.

http://bit.ly/1N7j7yt

European 3D Summit: Economic profit in today's microelectronics

Dr. Phil Garrou continues his look at the 2016 SEMI European 3D Summit.

http://bit.ly/1SNZHD6

Functional safety, security for IoT stressed at Cadence event

The "big trends" in the electronics industry are social, mobility, the Internet of Things, and security, Lip-Bu Tan, the president and chief executive officer of Cadence Design Systems, said in his keynote address at the CDNLive Cadence User Conference in Santa Clara, Calif.

http://bit.ly/1TPEOd2

Gartner identifies the top 10 Internet of Things technologies for 2017 and 2018

Gartner, Inc. has highlighted the top 10 Internet of Things (IoT) technologies that should be on every organization's radar through the next two years.

http://bit.ly/1QM2Xfr

Collaborative SoC verification

Extensive intellectual property (IP) use, design re-use, and re-design from both internal and external sources have made successful IC design as much about efficient IP management and integration, as it is about creating new blocks and functionality.

http://bit.ly/1XtLYTu

Insights from the Leading Edge: ASE takeover of SPIL halted but not stopped

The Taipei Times reported that the Taiwan Fair Trade Commission has suspended its review of ASE's bid to take over SPIL. ASE's prior acquisition of a 25% stake in SPIL has raised anti-trust concerns and fears that the merger would undermine competition in the market.

http://bit.ly/1RCOAOq

Goodbye, EDAC; Hello, ESD Alliance

The Electronic Design Automation Consortium (EDAC) is no more. The industry organization, founded in 1989, is changing its name to the Electronic System Design Alliance, or ESD Alliance. (From SemiMD.com)

http://bit.ly/1RCNU8r

A tribute to Andy Grove

Andy Grove, the man who codified the commercial IC industry dynamic as "Only the Paranoid Survive" died in March at the age of 79.

http://bit.ly/23ezVgq

The United States leads growing global industrial semiconductor market

The industrial semiconductor market will post an 8 percent compound annual growth rate (CAGR), as revenue rises from $43.5 billion in 2014 to $59.5 billion in 2019. Increased capital spending and continued economic growth, especially in the United States, will spur demand and industrial semiconductor sales growth, according to IHS Inc.

http://bit.ly/1SyFX3H

Please send news articles to sdavis@extensionmedia.com

news

worldnews

ASIA **- Samsung Electronics** announced that it has begun mass producing the industry's first 10nm class, 8-gigabit DDR4 (double-data-rate-4) DRAM chips and the modules derived from them.

EUROPE **- STMicroelectronics** has surpassed two billion unit sales of its robust and versatile STM8 microcontrollers, less than two years after reaching one billion unit sales.

ASIA **- TSMC** announced that the company and the municipal government of Nanjing, China have signed an investment agreement to establish TSMC Nanjing, a wholly-owned subsidiary managing a 12-inch wafer fab and a design service center.

USA **- Texas Instruments Incorporated** announced that Devan Iyer has been elected vice president of the company.

ASIA **- Alpha and Omega Semiconductor** announced a joint venture agreement in China.

USA **- SEMI** reported that worldwide sales of semiconductor manufacturing equipment totaled $36.53 billion in 2015, representing a year-over-year decrease of 3 percent.

EUROPE **- The University of Bath** is now the only university in the UK to have installed a unique nano-lithography printing system.

USA **- GLOBALFOUNDRIES** announced new advanced radio-frequency (RF) silicon solutions.

ASIA **– MagnaChip Semiconductor** surpasseed six million display driver ICs shipped.

USA **- Mentor Graphics Corporation** announced further enhancements and optimizations to the Calibre platform and Analog FastSPICE (AFS) platform by completing TSMC 10nm FinFET V1.0 certification.

imec opens new 300mm cleanroom for 7nm and beyond chip scaling

Nanoelectronics research center imec has announced the opening of its new 300mm cleanroom. With this 4000m^2 new facility, imec's semiconductor research cleanrooms now totals 12,000m^2, one of the most advanced research facilities in the world dedicated to scaling IC technology beyond 7nm. This facility will enable imec to keep its global leading position as a nanoelectronics R&D center serving the entire semiconductor ecosystem. Its global partners including foundries, IDMs, fabless and fablite companies, equipment and material suppliers, will benefit from topnotch semiconductor processing equipment (including alfa and beta tools) to develop innovative solutions for more powerful, high-performing, cheaper and energy-efficient ICs, which are crucial in the evolution of the Internet of Everything and a sustainable digital future.

Extending the existing cleanroom, the new facility complies with the newest standards in the semiconductor industry, and provides additional space for the most advanced tools that will lead innovations in new device and system concepts. Installations of the first tools began in January 2016. The new 300mm

Continued on page 8

Taiwan passes South Korea to become #1 in total IC wafer fab capacity

IC Insights recently released its new Global Wafer Capacity 2016-2020 report that provides in-depth detail, analyses, and forecasts for IC industry capacity by wafer size, by process geometry, by region, and by product type through 2020. Figure 1 breaks down the world's installed monthly wafer production capacity by geographic region (or country) as of December 2015. Each regional number is the total installed monthly capacity of fabs located in that region regardless of the headquarters location for the companies that own the fabs. For example, the wafer capacity that South Korea-based Samsung has installed in the U.S. is counted in the North America capacity total, not in the South Korea capacity total. The ROW region consists primarily of Singapore, Israel, and Malaysia, but also includes countries/regions such as Russia, Belarus, Australia, and South America.

Some highlights of regional IC capacity by wafer size are shown below.

As of Dec-2015, Taiwan led all regions/countries in wafer capacity with nearly 22% of worldwide IC capacity installed in the country. Taiwan surpassed South Korea in 2015 to become the largest capacity holder after having passed Japan in 2011. China became a larger wafer capacity holder than Europe for the first time in 2010.

For wafers 150mm in diameter and smaller, Japan was the top region in terms of the amount of capacity. The fabs running small size wafers tend to be older and typically process low-complexity, commodity type products or specialized devices.

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Intel honors 27 companies with Preferred Quality Supplier and Achievement Awards

Intel Corporation recognized 26 companies with its 2015 Preferred Quality Supplier (PQS) award, which celebrates exceptional performance and continuous pursuit of excellence. The 2015 recipients exhibited extraordinary achievements across key focus areas of quality, cost, availability, technology, customer service, labor and ethics systems, and environmental sustainability.

Along with the distinguished PQS award, Intel recognized one supplier with the Supplier Achievement Award, which is a specific recognition for outstanding accomplishments in one or more key performance areas. The company also presented eight companies with its highest honor, the Supplier Continuous Quality Improvement (SCQI) award.

Award winners will be honored in a ceremony last night in Santa Clara, California. The theme of the ceremony is "Delivering the Future Together" as this dedicated group of suppliers has helped Intel push the boundaries of smart and connected technology and brings innovative products to market quickly.

"Intel is honored to recognize our Preferred Quality Suppliers for their sustained excellence in 2015 to deliver leading-edge technology with world-class cost, velocity and sustainability," said Robert Bruck, corporate vice president and general manager of Global Supply Management at Intel. "Close collaboration and superb execution by these suppliers remains one of the crucial factors in enabling Intel to extend our industry-leading silicon, packaging and test technologies, and is a clear demonstration of leadership in their respective markets."

"The winners of the Preferred Quality Supplier and Achievement Award are an integral part of Intel's success," added Jacklyn Sturm, vice president, Technology and Manufacturing Group and general manager of Global Supply Management at Intel. "The absolute focus and rigorous attention to continuous improvement and time-to-market innovation are a testament to their world-class support, providing Intel with a critical part of the foundation to be a leader in computing innovations."

The PQS award is part of Intel's Supplier Continuous Quality Improvement (SCQI) program, which encourages suppliers to innovate and continually improve. To qualify for PQS status, suppliers must exceed high expectations and uncompromising performance goals while scoring at least 80 percent on an integrated report card that assesses performance throughout the year. Suppliers must also achieve 80 percent or greater on a challenging continuous improvement plan and demonstrate solid quality and business systems.

The PQS winners provide Intel with the following products or services:

- **Amkor Technology Inc.**: semiconductor advanced packaging design, assembly and test services
- **ASM International:** front-end equipment supplier for atomic layer deposit (ALD), plasma-enhanced ALD, metal gate and diffusion
- **Daewon Semiconductor Packaging Industrial Co. Ltd.**: plastic injection molded tray (PIMT) media for bare die automation, substrate transport, device assembly and test, final shipping and storage, bare die tape and reel (BDTR) media for bare die transport
- **Daifuku**: automated material handling systems
- **DISCO Corporation**: precision cutting, grinding and polishing machines
- **EBARA Corporation**: chemical mechanical polishers, plating systems, and dry vacuum pumps and abatement systems
- **Edwards Vacuum LLC**: vacuum system products and abatement solutions
- **Fujimi Corporation**: chemical mechanical planarization and silicon polishing slurries
- **Hitachi High-Technologies Corporation**: dry etching, ashing, metrology and advanced packaging systems
- **Hitachi Kokusai Electric Inc.**: batch processing and single wafer processing systems
- **JLL**: facilities management
- **KLA-Tencor Corporation**: process control and yield management solutions
- **Lam Research Corporation**: fab capital equipment
- **Mitsubishi Gas Chemical Company Inc.**: high-purity peroxide and custom back-end cleans
- **ModusLink Global Solutions Inc.**: channel box CPU for Penang, Shanghai and Miami, and finished goods warehouse distribution for Miami
- **Murata Machinery Ltd.**: automated material handling systems, hoist vehicles and stockers
- **The PEER Group Inc.**: automation software and services
- **SCREEN Semiconductor Solutions Co. Ltd.**: wafer cleaning and anneal equipment and services for semiconductor manufacturing
- **Shin Etsu Chemical Co., Ltd**: silicon wafers, advanced photoresists, photomask blanks, and thermal conductive materials.
- **Shinko Electric Industries Co. Ltd.**: plastic laminated packages and heat spreaders
- **Siltronic AG**: polished and epitaxial silicon wafers
- **Tokyo Ohka Kogyo Co. Ltd**: high-purity photo resists, developers, cleaning solutions and supporting chemistries
- **Tosoh SMD, Inc.**: sputtering targets

- **Tosoh Quartz Inc.**: quartzware for semiconductor wafer processing equipment
- **VWR**: products, services and solutions to laboratory and production facilities
- **Veolia North America**: waste management services

- The Supplier Achievement Award winner is:
- **Nanium**: outsourced semiconductor packaging, assembly and test provider (recognizing extraordinary results in product availability. ◈

Lifetime breakthrough promising for low-cost and efficient OLED displays and lights

With just a tiny tweak, researchers at Kyushu University greatly increased the device lifetime of organic light-emitting diodes (OLEDs) that use a recently developed class of molecules to convert electricity into light with the potential for increased efficiency at a lower cost in future displays and lighting.

The easily implemented modifications can also potentially increase the lifetime of OLEDs currently used in smartphone displays and large-screen televisions.

Typical OLEDs consist of multiple layers of organic films with various functions. At the core of an OLED is an organic molecule that emits light when a negatively charged electron and a positively charged hole, which can be thought of as a missing electron, meet on the molecule.

Until recently, the light-emitting molecules were either fluorescent materials, which can be low cost but can only use about 25% of electrical charges, or phosphorescent materials, which can harvest 100% of charges but include an expensive metal such as platinum or iridium.

Researchers at Kyushu University's Center for Organic Photonic and Electronics Research (OPERA) changed this in 2012 with the demonstration of efficient emitters based on a process called thermally activated delayed fluorescence (TADF).

Through clever molecular design, these TADF materials can convert nearly all of the electrical charges to light without the expensive metal used in phosphorescent materials, making both high efficiency and low cost possible.

However, OLEDs under constant operation degrade and become dimmer over time regardless of the emitting material.

Devices that degrade slowly are key for practical applications, and concerns remained that the lifetime of early TADF devices was still on the short side.

Continued on page 8

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***Lifetime breakthrough**, Continued from page 7*

But with the leap in lifetime reported in a paper published online March 1, 2016, in Scientific Reports, many of those concerns can now be put to rest.

"While our initial TADF devices lost 5% of their brightness after only 85 hours," said postdoctoral researcher Daniel Tsang, lead author on the study, "we have now extended that more than eight times just by making a simple modification to the device structure."

The newly developed modification was to put two extremely thin (1-3 nm) layers of the lithium-containing molecule Liq on each side of the hole blocking layer, which brings electrons to the TADF material, the green emitter 4CzIPN in this case, while preventing holes from exiting the device before contributing to emission.

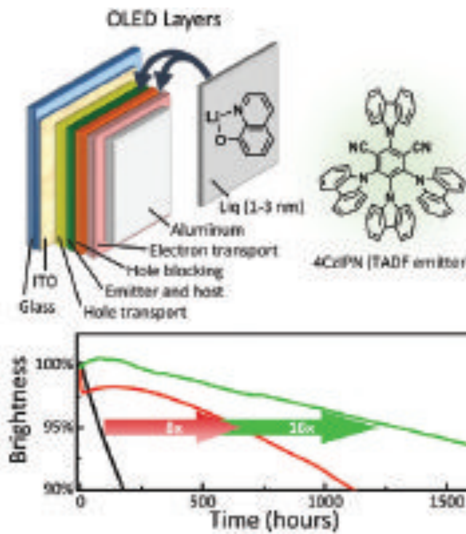


Figure: Using the OLED structure in this schematic, researchers were able to delay the degradation in brightness of an OLED with the TADF emitter 4CzIPN by eight to sixteen times. Credit: Daniel Ping-Kuen Tsang and William John Potscavage Jr.

The benefits of the Liq layers are not limited to TADF-based OLEDs as the researchers also found an improvement using a similar device structure with a phosphorescent emitter.

Though still trying to completely unravel the degradation mechanism, the researchers found that devices with the Liq layers contain a much lower number of traps, a type of defect that can capture and hold a charge, preventing it from moving freely in the device.

These defects were observed by measuring tiny electrical currents created when charges that were frozen in the traps at extremely cold temperatures escape by receiving a jolt of thermal energy as the device is heated, a process called thermally stimulated current.

The devices will last even longer in practical applications because the tests are performed at extreme brightnesses to accelerate the degradation.

Applying additional optimizations that have been previously reported, the 5% drop was further delayed to longer than 1,300 hours, over 16 times that of the initial devices.

"What we are finding is that the TADF materials themselves can be very stable, making them really promising for future displays and lighting," said Professor Chihaya Adachi, director of OPERA.

Having charges stuck in these traps may increase the chance for interactions with other charges and electrical excitations that can destroy the molecules and lead to degradation.

One of the next major challenges for TADF is stable and efficient blue emitting materials, which are necessary for full color displays and are also still difficult using phosphorescence.

"With the continued development of new materials and device structures," said Prof. Adachi, "we think that TADF has the potential to solve the challenge of efficient and stable blue emission."◈

***imec**, Continued from page 4*

cleanroom complements imec's other production facilities including its bio-nanolabs, neuroelectronics labs, imaging and wireless and electronics test labs, photovoltaic pilot lines, and GaN-on-Si, Silicon photonics and MEMS pilot lines.

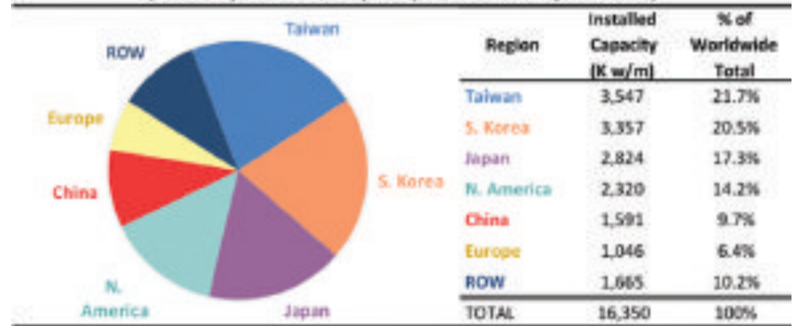
"Since our founding in 1984, imec has become the world's largest independent nanoelectronics research center with the highest industry commitment," stated Luc Van den hove, president and CEO at imec. "This success is the result of the unique combination of our broad international partner network, including the major global players of the semiconductor industry, top scientific and engineering talent, and imec's one of a kind infrastructure. The extension of our cleanroom provides our partners with the necessary resources for continued leading edge innovation and imec's success in the future within the local and global high-tech industry."

The cleanroom was constructed by M+W, an internationally renowned contractor of large-scale high-tech infrastructure. The construction was completed in 20 months, and includes a reflecting facade, from Architect Stéphane Beel, which is intended to integrate the building with the environment. The new cleanroom comprises a total investment (building and equipment) of more than 1 billion euro of which 100 million euro funding from the Flemish Government and more than 900 million euro investments from joint R&D with the leading players from the entire semiconductor industry, totaling more than 90 industrial partners. ◈

***Taiwan**, Continued from page 4*

The capacity leaders for 200mm wafers were Taiwan and Japan. There have been many 200mm fabs closed over the past several years, but not in Taiwan and that resulted in the country becoming the largest source of 200mm capacity beginning in 2012. With Taiwan being home to most of the IC industry's foundry capacity, the country's share of 200mm capacity will likely rise further in the coming years.

For 300mm wafers, South Korea was at the forefront, followed by Taiwan. Taiwan lost its position as the leading supplier of 300mm wafer capacity in 2013. That was in large part because ProMOS closed its large 300mm fabs, but it was also due to Samsung and SK Hynix continuing to expand their fabs in South Korea to support their high-volume DRAM and flash businesses. ◈



Wafer Capacity at Dec-2015 – by Geographic Region
(Monthly Installed Capacity in 200mm-equivalents)

Region	Installed Capacity (K w/m)	% of Worldwide Total
Taiwan	3,547	21.7%
S. Korea	3,357	20.5%
Japan	2,824	17.3%
N. America	2,320	14.2%
China	1,591	9.7%
Europe	1,046	6.4%
ROW	1,665	10.2%
TOTAL	16,350	100%

Source: IC Insights

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Samsung announces 4GB HBM2 DRAM

PHIL GARROU,
Contributing Editor

Samsung Electronics announced that it has begun mass producing the industry's first 4-gigabyte (GB) DRAM package based on the second-generation High Bandwidth Memory (HBM2) interface, for use in high performance computing (HPC), advanced graphics and network systems, and enterprise servers.

The newly introduced 4GB HBM2 DRAM, uses Samsung's 20nm process technology and is reportedly more than seven times faster than the current DRAM.

The 4GB HBM2 package is created by stacking a buffer die at the bottom and four 8-gigabit (Gb) core dies on top (FIGURE 1). These are then vertically interconnected by TSV holes and microbumps (FIGURE 2). A single 8Gb HBM2 die contains > 5,000 TSV holes, which is more than 36 times that of a 8Gb TSV DDR4 die, offering a dramatic improvement in data transmission performance compared to typical wire-bonding based packages.

Samsung's new DRAM package features 256 GBps of bandwidth, which is double that of a HBM1 DRAM package. This is equivalent to a more than seven-fold increase over the 36GBps bandwidth of a 4Gb GDDR5 DRAM chip, which has the fastest data speed per pin (9Gbps) among currently manufactured DRAM chips. Samsung's 4GB HBM2 also enables enhanced power efficiency by doubling the bandwidth per watt over a 4Gb-GDDR5-based solution, and embeds ECC (error-correcting code) functionality to offer high reliability.

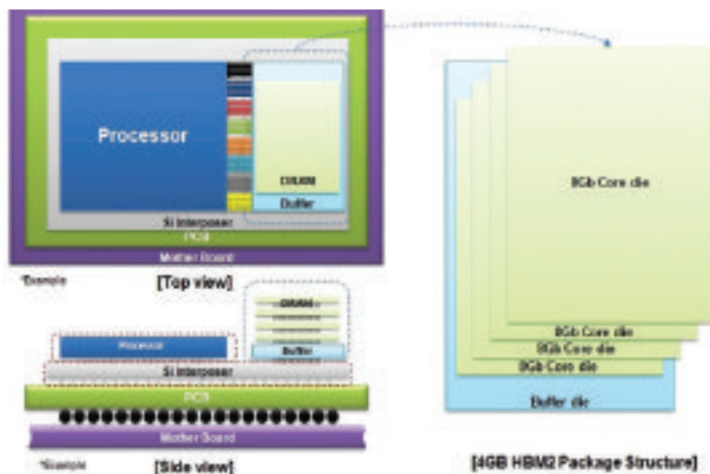


Figure 1. Samsung HBM2 memory.

Samsung also plans to produce an 8GB HBM2 DRAM package in the next 12 months. This will offer designers a 95 percent space savings vs GDDR5 DRAM.

Samsung announced that production volume of HBM2 DRAM will increase over the remainder of the year.

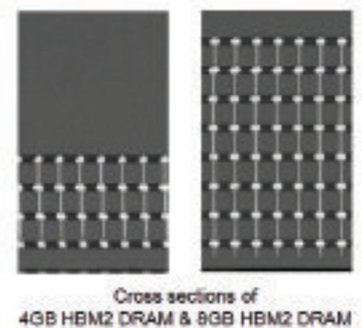


Figure 2. Photos of 4GB and 8GB HBM2 DRAM.

The second-generation HBM (HBM2) technology is outlined by the JESD235A standard. It uses 128-bit DDR interface, 1024-bit I/O, 1.2 V I/O and core. Just like HBM1, HBM2 supports two, four or eight DRAM devices on a base logic die (2Hi, 4Hi, 8Hi stacks). HBM Gen 2 expands capacity of DRAM devices within a stack to 8 Gb and increases supported data-rates up to 1.6 Gb/s or even to 2 Gb/s per pin. ◆

Packaging

Molecular modeling of materials defects

ED KORCZYNSKI,
Sr. Technical Editor

New materials are being integrated into High Volume Manufacturing (HVM) of semiconductor ICs, while old materials are being extended with more stringent specifications. Defects within materials cause yield losses in HVM fabs, and engineers must identify the specific source of an observed defect before corrective steps can be taken. Honeywell Electronic Materials has been using molecular modeling software provided by Scienomics to both develop new materials and to modify old materials. Modeling allowed Honeywell to uncover the origin of subtle solvation-based film defects within Bottom Anti-Reflective Coatings (BARC) which were degrading yield in a customer's lithographic process module.

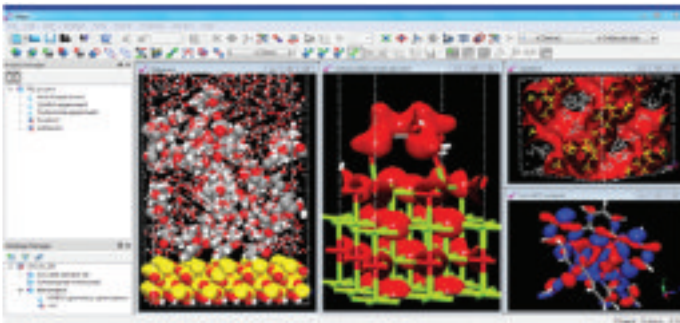


Figure 1. Materials Processes and Simulations (MAPS) gives researchers access to visualization and analysis tools in a single user interface together with access to multiple simulation engines (Source: Scienomics).

Scienomics sponsored a Materials Modeling and Simulations online seminar earlier this year, featuring Dr. Nancy Iwamoto of Honeywell discussing how Scienomics software was used to accelerate response to a customer's manufacturing yield loss. "This was a product running at a customer line," explained Iwamoto, "and we needed to find the solution." The product was a Bottom Anti-Reflective Coating (BARC) organo-silicate polymer delivered in solution form and then spun on wafers to a precise thickness.

Originally observed during optical inspection by fab engineers as 1-2 micron sized vague spots in the BARC, the new defect type was difficult to see yet could be correlated to lithographic yield loss. The defects appeared to be discrete within the film instead of on the top surface, so the source was likely some manner of particle, yet filters did not capture these particles.

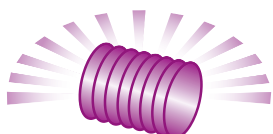
The filter captured some particles rich in silicon, as well as other particles rich in carbon. Sequential filtration showed that particles were passing through impossibly small pores, which suggested that the particles were built of deformable gel-like phases. The challenge was to find the material handling or processing situation which resulted in thermodynamically possible and kinetically probable conditions that could form such gels.

Molecular modeling and simulation is a powerful technique that can be used for materials design, functional upgrades, process optimization, and manufacturing. FIGURE 1 shows a dashboard for Scienomics' modeling platform. Best practices in molecular modeling to find out-of-control parameters in HVM include a sequential workflow:

- Build correct models based on experimental observables,
- Simulate potential molecular structures based on known chemicals and hierarchical models,
- Analyze manufacturing variabilities to identify excursion sources, and
- Propose remedy for failure elimination.

Honeywell Electronic Materials researchers had very few experimental observables from which to start: phenomenon is rare (yet effects yield), not filterable, yet from thermodynamic hydrolysis parameters it must be quasi-stable. Re-testing of product and re-examination of Outgoing Quality Control (OQC) data at the Honeywell production site showed that the molecular weight of the product was consistent with the desired distribution. There was also an observed BARC thickness increase of ~1nm on the wafer associated with the presence of these defects.

Using the modeling platform, Honeywell looked at the solubility parameters for different small molecular chains off of known-branched back-bone centers. Gel-like agglomerations could certainly be formed under the wrong conditions. Once the agglomerations form, they are not very stable so they can probably dis-aggregate when being forced through a filter and then re-aggregate on the other side. ◆



Spintronic majority gates: A new paradigm for scaling

IULIANA RADU *and* **AARON THEAN**, *imec, Leuven, Belgium*

Spintronic majority gates could revolutionize circuit design. They will completely change the paradigm – both at device and circuit level – in how to approach scaling

Spin logic devices are an emerging beyond-CMOS technology that may push beyond Moore's law, enabling functional scaling beyond the 5nm technology node. These exotic devices lend themselves to majority logic operation, which differs in many ways from the classical NAND-based operation. Imec looks into spin torque majority gates and spin wave majority gates, two concepts that completely change the way we think of computing and scaling. As shown at the 2015 IEDM conference, circuit simulations with these majority gates outperform equivalent CMOS circuits in terms of area and power consumption. Meanwhile, experimental work has been started to learn about the materials, about the devices behavior and about the technology challenges that lie ahead.

Spintronic majority gates, an efficient way to build circuits

As we approach 5nm logic technology in 2020, CMOS device density scaling faces serious challenges due to escalating process costs and parasitics. This inevitably leads to questions of sustainability of traditional Moore's law where cost and data processing supposedly scale favorably with increasing device density. This begs the question: are there specialized devices and computational paradigms out there that break away from these fundamental trappings of CMOS scaling? The search is on and novel beyond-CMOS devices are being intensively studied.

This varied class of devices may enhance and complement the functionality of CMOS circuits. Among the promising concepts are spintronic devices (**FIGURE 1**), which exploit the electron's spin, a quantum attribute that relates to magnetism, rather than its charge to perform logic operations. Spin logic devices promise to be non-volatile and lend themselves to ultralow-energy operation. But one of their biggest trumps is the ability to build majority gates, 'democratic' devices that return true if more than 50% of their inputs are true. For example, if two inputs are in a true state and a third one is in a false state, the expected state at the output is true. With these majority gates, logic AND and OR operations can be emulated. Also, this concept of majority logic operation differs in many ways from the classical NAND-based logic, where an output is false only if all its inputs are true. It presents a concept shift that completely changes the way we synthesize circuits. But the advantages are huge: majority gates enable arithmetic circuits that are much more compact and energy-efficient than conventional NAND or XOR gate-based circuits. For example, while a one-bit adder in CMOS technology requires about 25 transistors, the equivalent wave computing circuit only requires 5 transducers and 4 waveguides to perform the same operation.

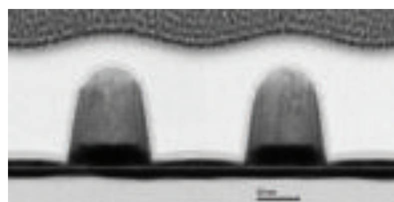


FIGURE 1. TEM cross-section of two magnetic tunnel junction pillars, critical building blocks of the spin torque majority gate.

Two ways of encoding information

Spintronic majority gates can come in several flavors, differing in the way the information is encoded and processed in the device, and in the way transduction from the charge domain to the spin (magnetism) domain is executed. At imec, two concepts are studied extensively: the spin torque majority gate (STMG) and the spin wave majority gate (SWMG).

In a STMG, the information is encoded in magnetic domain

IULIANA RADU *is a program manager and* **AARON THEAN** *is the Vice President of Process Technologies and the Director of the Logic Devices Research at imec, Leuven, Belgium.*

walls. Domain walls are interfaces that separate regions with different magnetization direction. The majority gate itself consists of a cross-shaped free layer that is common to 4 magnetic tunnel junctions (3 inputs, 1 output). The magnetization direction of the 3 'input' free layers is switched using spin transfer torque, provided by a current through each of the magnetic tunnel junctions. Based on quantum interactions between electrons known as exchange, the domain walls propagate and interact, and the majority magnetization direction wins. The output state is measured via tunneling magnetoresistance.

In a SWMG, the computation principle is based on the interference of spin waves. The information can be encoded either in the amplitude or in the phase of the waves. Spin waves are low-energy collective excitations in magnetic materials. They can be generated by a so-called magneto-electric cell, which converts voltage into a spin wave. Key elements of this cell are a piezoelectric layer (that converts voltage into strain) and a magnetostrictive layer (in which the strain produces a change in magnetization or magnetization anisotropy). In its turn, the change in magnetization can generate a spin wave in a magnetic spin wave bus. The same cell is used to read the output state of the majority gate (**FIGURE 2**).

FIGURE 2. Sketches of (left) a STMG and (right) a SWMG with 3 inputs and one output.

Both concepts have been studied intensively, and approaches of how to handle the computation have been proposed. An experimental demonstration is however still missing. At imec, we have enlarged our basic understanding of both STMG and SWMG and used simulations to validate device functioning. We have compared the two types of majority gates against equivalent circuits in 10nm FinFET CMOS technology. And we present our first experimental results, and highlight the main challenges for both concepts.

Spin torque majority gate – compact and technology friendly

We used micromagnetic simulations to validate the functioning of the STMG and identify its operating conditions. For this majority gate, the switching of the magnetization state is current controlled. If the applied current or the pulse length are not enough,

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the output fails to switch. Even if the applied current pulses provide enough energy to switch, other failure modes can appear. For example, the domain walls that are being formed can become 'stuck' at the crossing of the device. This happens when the width of the cross exceeds a certain value, typically in the 15-20nm range. This makes these devices difficult to demonstrate experimentally as it requires patterning and etching to small size and tight pitch between the magnetic tunnel junctions. However, this initial impediment holds great promise for further device scaling. A major advantage of this majority gate is the use of technology friendly materials, comparable to the materials used in magnetic memories.

We have benchmarked the device against equivalent 10nm CMOS circuits by comparing key metrics of area, power and delay. On average, the STMG circuits have about 10x smaller area, and provide a means for further scaling. However, being current controlled, the STMG circuits have a longer delay, making them less efficient than equivalent CMOS circuits. Further advances in materials stacks are needed to improve their performance, comparable to those needed in general for magnetic memory.

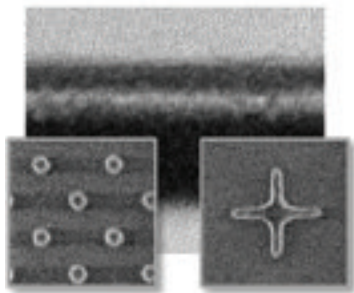

FIGURE 3. Experimental work on STMGs: TEM cross section of etch stopping close to the tunnel barrier interface. Insets are top-view SEM pictures of the magnetic tunnel junction pillars and the cross-shaped free layer.

At imec, we are currently building the first STMG devices on 300mm wafers. Particular attention is paid to the magnetic tunnel junction pillar etch development (**FIGURE 3**).

Spin wave majority gate – compact, ultralow-power but challenging materials

We used micromagnetic simulations to model the spin wave propagation in SWMGs and to simulate the magnetic behavior of the magneto-electric cell that converts the applied voltage into a spin wave. This cell is a critical component for the device functionality. We mapped out the parameter space where the magneto-electric cell is expected to work optimally and used these parameter ranges as input for circuit synthesis. Building magneto-electric cells experimentally is very challenging as the materials to be used are not typically used in standard fabs and cleanrooms. For this reason, and to help choose the right materials, we have performed circuit synthesis and benchmarked them against CMOS. Based on materials parameters extracted from these simulations we have chosen a starting set of materials for our experiments.

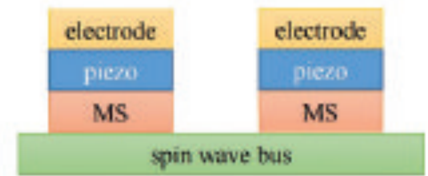

FIGURE 4. Schematic representation of the magneto-electric elements on a spin wave bus.

One of the questions to be answered is how piezoelectrics behave at very high frequencies (gigahertz range) as needed for logic devices. Piezoelectric materials are being used in many applications, where they typically operate at low frequencies (up to hundreds of kHz). At imec, we started first experiments to grow piezoelectric materials in a thin film and to learn how these materials behave in the high frequency domain. And although more experiments are needed to improve the performance and map out the reliability behavior, our preliminary results are very encouraging. An important drawback of the spin wave technology is that the required materials (both the magnetostrictive and the piezoelectric materials) are very different from standard CMOS materials (**FIGURE 4**).

The spin wave technology was also benchmarked against CMOS circuits. The spin wave circuits take on average 3.5 times less area and about 400 times lower power than their CMOS counterparts. However, the spin wave circuits are on average 12 times slower, mainly because of the large switching delay of the magneto-electric cell. SWMGs may therefore be used for ultralow-power applications, where latency is a secondary consideration (**FIGURE 5**).

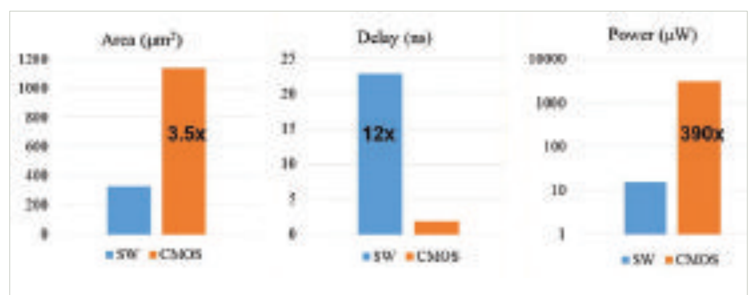

FIGURE 5. Spin wave majority gates: a comparison of area, delay and power between circuits synthesized with SWMGs and 10nm CMOS.

Building arithmetic circuits on top of CMOS

Spintronic majority gates could revolutionize circuit design. They will completely change the paradigm – both at device and circuit level – in how to approach scaling. In the future, more experimental work is planned to learn about the new materials required, to validate circuit assessment, and to finally demonstrate functional devices.

Once these technologies have become more mature, we can start thinking of multi-device architectures that combine CMOS-based and spin logic devices. An interesting approach is to stack, on top of CMOS technology, arithmetic circuits made of spintronic majority gates. The high-performance functions could be executed by the CMOS-based devices and the ultralow-power functions by the spin logic arithmetic circuits. So, rather than replacing Si CMOS based transistors in the future, this beyond-CMOS technology is intended to enhance and complement the functionality of CMOS-based devices.

Spintronics belongs to the beyond-CMOS segment, where we look into new materials and device architectures, and even into new computing paradigms and circuits. Beyond-CMOS research is part of imec's multiple roadmap scenario that is built around 3 pillars: Si extension, beyond Si and beyond CMOS. Each of these segments has its own mission and approach to enabling scaling. And each of the new technologies will bring in enabling modules and devices that will serve the application diversity in the new era of electronics: the internet of things. And the results will support the quest of the semiconductor industry to find solutions that enable continual functional scaling of cost and energy per bit by departing from the familiar CMOS scaling.

Suggested additional reading

1. Spintronic majority gates, I. P. Radu et al., IEDM 2015 (https://www.researchgate.net/publication/286882975_Spintronic_Majority_Gates)
2. Design and benchmarking of hybrid CMOS-spin wave device circuits compared to 10nm CMOS, O. Zografos et al., Proceedings of the 15th International IEEE Conference on Nanotechnology (NANO), 2015(http://infoscience.epfl.ch/record/211004)
3. "With our multiple roadmap scenario, we anticipate the application diversity in the new Era of Electronics", imec annual overview 2015, vision by Aaron Thean (click on the name of Aaron at http://magazine.imec.be/data/80/reader/reader.html?t=1452505511353#!preferred/1/package/80/pub/86/page/8) ◆

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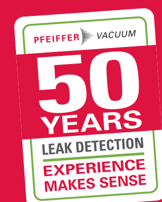

From catching up to forging ahead: China's new role in the semiconductor industry

DIETER ERNST, *East-West Center, Honolulu, HI*

How will China's new role transform the global semiconductor industry?

China has become the largest and fastest growing semiconductor market in the world, absorbing 40% of the worldwide semiconductor shipments. For US semiconductor firms, nothing compares to the China market.

China however faces a fundamental dilemma. As the world's leading exporter of electronic products, it remains heavily dependent on imports of semiconductors and technology, primarily from the US, but also from Japan, Korea, Taiwan and Europe. At least 80 percent of the semiconductors used in China's electronics manufacturing are imported and virtually all leading-edge devices like multi-component semiconductors (MCOs). For instance, 43% of the inputs for handsets and networking equipment of China's second largest telecom company, ZTE, are supplied by US companies (Avnet, Qualcomm, Broadcom, Jabil, Intel, Microsoft, Micron, Xilinx, Nvidia and Finisar) [1].

As a result, China's trade deficit in semiconductors has more than doubled since 2005 and now exceeds the huge amount it spends on crude oil imports. To correct this unsustainable imbalance, China's new strategy to upgrade its semiconductor industry seeks to move from catching up to forging ahead in semiconductors through progressive import substitution. The "National Semiconductor Industry Development Guidelines (Guidelines)" and the "Made in China 2025" (MIC 2025, 中国制造2025) plan were published by China's State Council in June 2014 and May 2015, respectively [2]. Both policies seek to strengthen simultaneously advanced manufacturing and innovation capabilities in China's integrated circuit (IC) design industry and its domestic IC fabrication, primarily through foundry services.

As part of the Guidelines, a CNY120 billion (US$19 billion) national industry investment fund has been set up to help local foundries finance the build-up of advanced manufacturing processes, and also to assist local IC firms to form mergers and/or make acquisitions internationally. With the MIC 2025 plan, China is aiming to improve the self-sufficiency rate for ICs in the nation to 40% in 2020, and boost the rate further to 70% in 2025. MIC 2025 specifically defines the following priorities: i) Catch up with world best practice in IC design cores and design tools; ii) move to the frontier of multicomponent semiconductors (MCOs); iii) win design-in contracts from China-based electronic equipment manufacturers (both large global MNCs and Chinese firms like Lenovo or Huawei); and iv) strengthen China's capacity to design and produce high-density chip packages and 3D micro-package technology.

Both policies have already led to a major push in the development of the local IC industry, with investments in semiconductor memories, designs, foundries, OSATS, and equipment and materials. In addition, strategic partnerships, joint ventures and mergers and acquisitions have proliferated across China's semiconductor industry, both among domestic firms (to increase economies of scale and scope), and with leading global semiconductor firms (to access cutting-edge technology and best-practice management techniques).

Based on a review of policy documents and interviews with China-based industry experts, this paper explores how realistic these objectives are, and how this might affect international firms and the global semiconductor industry.

How realistic are the objectives of China's new policies?

Over the last 60 or so years, China's semiconductor industry has come a long way from being a completely government-owned part of the defense technology production system, with

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state-owned enterprises (SOEs) as the only players, toward a gradually more market-led development model. The role of SOEs has dramatically declined, and a deep integration into international trade and global networks of production and innovation has transformed decisions on pricing and investment allocation, with private firms as the main drivers. Major achievements include the rapid growth of China's IC design industry from practically zero at the turn of the century to $17.05 billion in 2014, with an almost 37% compound annual growth rate since 2003. Other achievements include the successful diversification into optical devices (especially LED-related), sensors and discrete devices; first steps to move from silicon to wide band-gap semiconductor materials; and the surge of China's semiconductor assembly, packaging, and testing (APT) industry, which has become the global market leader.

However, China's achievements are overshadowed by persistent weaknesses, despite massive government support. Buying decisions for advanced ICs consumed in China are mostly made in Taiwan, Korea, US (for mobile devices), Japan, and Singapore. Of particular concern is the large and growing gap between semiconductor consumption and production, which has ballooned to a record $ 120 billion in 2013, and is forecast to reach $ 151.5 billion in 2017.[3] Equally important, China continues to play second fiddle in wafer fabrication - China's 2015 share of total worldwide semiconductor wafer fab capacity is 11.7%,but advanced technology nodes (28nm and below) account for only 5 % of worldwide wafer fab capacity. Foreign IDMs dominate (Intel, Samsung, Hynix), and Chinese foundries have a long way to go to catch up in process technology and wafer size. Most importantly, China lags behind in innovation, especially for advanced semiconductors, despite all the government's previous plans and efforts.

Will China's policy on semiconductors this time around work better than before? Our research finds that China's new semiconductor policy does not represent a radical break with its deeply embedded statist tradition [4]. However, there are some important changes toward a more bottom-up, market-led approach to industrial policy. If sustained, these changes may considerably improve China's chances to succeed in its new push in semiconductors.

China's new semiconductor policy (as defined in the Guidelines) relies on private equity investment rather than subsidy as the tool of industrial policy. The government participates in equity investment but claims it will do so without intervening in management decisions. This is expected to reduce the cost of investment for a selected group of firms comprising a "national team" in the semiconductor industry. The underlying financial networks are complex and difficult to disentangle. Take Hua Capital Management Co., Ltd (HCM), a Chinese investment management company, which was chosen to manage the chip design and testing fund under the Beijing government's 30-billion-yuan (HK$37.8 billion) Semiconductor Industry Development Fund.

According to industry observers, the real driving force behind HCM is Chen Datong, who is HCM's chairman as well as co-founder and managing partner of WestSummit Capital, a leading China-based global equity firm focused on helping high-growth technology companies access the China market. Dr. Chen has more than 20 years of investment and operations experience in the technology and semiconductor industries, and he owns 34 US and European patents. [5] Another major player is Liu Yue, the deputy chairwoman of HCM, who also has a wealth of experience in China's IC industry. Of particular interest is her role as an early investor in China's leading foundry SMIC through Walden Capital, and her continuous involvement with SMIC. HCM's president, Xisheng (Steven) Zhang, started out in 1994 as a post-doctorate researcher at University of California, Berkeley, worked his way into senior management positions at Agilent Technologies and Silicon Valley start-up IC design companies, and joined Beijing- based private equity investment company WestSummit Capital in 2013. Zhang has over 20 years industry experience in semiconductors, and in managing start-up companies in Silicon Valley and in Beijing.

Based on this information, one might conclude that HCM qualifies as a professional fund manager with considerable knowledge of key aspects of the semiconductor industry value chain, especially related to IC design. In the view of the United States Information Technology Office (USITO), the use of professional investment fund managers, as opposed to government subsidies or investment, "suggest a new approach to industrial policy that focuses on building a strong and sustainable investment environment in China."[6] It remains unclear, however, how private equity fund managers, who are supposed to maximize the return to capital, can nevertheless serve as proxies for the government and support its policy to strengthen indigenous innovation. A final assessment thus has to wait until more information is available on how funds will ultimately be deployed.

MIC 2025, on the other hand, seeks to provide a new framework for coordinating industrial support policies, in order to overcome a persistent gap in technological, management and innovation capabilities. Improved policy coordination is considered to be essential for overcoming deeply entrenched disconnects between industry, academia and government. Over two and a half years, 50 experts from the China Academy of Engineering and the Chinese Academy of Sciences worked together with around 100 experts from industry and research institutes to design the MIC 2025 plan. An equally important objective is to reduce the fragmentation of decision-making across government agencies and

between the Central government and local governments. As an important step in this direction, 14 state-run associations from different sectors worked together and created a voluntary quality management standard for automated and intelligent manufacturing.

In short, China's government seems more open to experimentation with new approaches to policy formulation, investment finance and flexible, bottom-up policy implementation. Among Chinese technology planners, there seems to be a growing consensus that the closer China moves to the technology frontier, the less scope there is for imitation and low-level incremental innovation. Chinese firms now are encouraged to develop and protect their own intellectual property rights and accelerate the commercialization of new ideas, discoveries and inventions.

China's leadership is very conscious that the United States is far ahead in advanced semiconductors and that China has a long way to go to close the gap. But at the same time, Beijing's new semiconductor policies also convey a new sense of optimism. Global transformations in semiconductor markets and technology, including a new interest in strategic partnerships and mergers, are no longer perceived exclusively as threats. In fact, China's technology planners now seek to identify pathways to innovation- led development that could benefit from new technologies, such as the technology convergence in mobile devices, the Internet of Things in industrial manufacturing, and "green development", focusing on a reduction of energy consumption, water usage and pollution. Forging ahead in semiconductors is considered essential for realizing this potential.

Above all, the role of the government appears to be gradually shifting away from the selection of priority sectors and technologies toward the facilitation of an interactive learning process led by the private sector. In this new model of industrial policy, which is slowly taking hold in China's semiconductor industry, the government role is to provide incentives and remove regulatory constraints to empower the private companies that are most capable of realizing China's domestic innovation potential.

It is however an open question whether China's transition to innovation-led growth in semiconductors could be derailed, for instance, by the threat of overcapacity or by the Leadership's (cyber-) security objectives. As is typical for China, the implementation of the semiconductor policy is left to the local governments who have become masters in producing overcapacity due to misaligned incentives that are focused exclusively on the region's GDP growth.

China's policy on cyber security seeks to protect China-based information systems against perceived threats to national and public security. [7] In response to Edward Snowden's disclosure of US National Security Agency (NSA) global surveillance practices in China and elsewhere, China's concern with cybersecurity receives prominent attention in the Guidelines. It is unclear at this stage whether the drumbeat on security is used primarily as a tactic to mobilize support for aggressive investment funding? [8] Or is this focus on security an overriding concern for China's leadership that will cast aside many of the aforementioned economic considerations?

In the end, there is reason for cautious optimism that pragmatism will continue to shape China's policy for semiconductors [9]. Learning from global industry leaders will play a critical role, based on a quite realistic set of expectations: "In the next ten years, there will be a large amount of M&A cases in China, but many of them will fail…But it is better than nothing. China's enterprises will gain experience."[10] More than before, such pragmatism will be shaped by economic constraints, such as the country's rising debt and dwindling foreign exchange reserves due to the collapse in Chinese exports [11].

Implications for international firms and the global semiconductor industry

As U.S. and other foreign semiconductor companies heavily depend on the China market, they seem to have little choice but to adjust their strategies to China's new semiconductor policy. Intel, for instance, now depends on China for one-fifth of its revenues, while Qualcomm relies on the China market for nearly half of its income. In fact, U.S. and other foreign firms are quite explicit that they would be willing to accede to Chinese demands to transfer technology and form joint ventures with its firms, if only they could expand or at least sustain their share of the China market.

Examples include Intel's substantial investment in Spreadtrum, one of China's leading IC design firms, and Qualcomm's investment in China's leading IC fabrication company, SMIC. As foreign firms seek to cooperate more closely with Chinese firms in exchange for continued market access, this raises the question to what degree this might amplify China's policies. Might foreign firms in some cases actually provide more effective support than the Beijing government in expanding China's semiconductor industry?

To conclude, both Chinese and U.S. semiconductor companies have much to gain by learning from each other as they each face their own upgrading imperatives. While they compete in global markets, they would both benefit from cooperation in advanced semiconductor manufacturing and technology to solve the challenges of economic growth, better and lower-cost health systems, and a greener environment. Given the importance of both countries in the global semiconductor

industry, it is striking to see that such cooperation remains as yet quite limited.

There is however ample scope to extend such cooperation. While China is catching-up in semiconductors, the US is still way ahead in overall innovation capacity. China's persistent innovation gap implies that Chinese firms continue to need access to American technology, whether in terms of equipment, core components, software or system integration. For America, this implies that China's new policies for semiconductors creates new markets for American firms, provided they stay ahead on the innovation curve.

But implementing such cooperation faces many hurdles. While incumbent industry leaders seek to retain the status quo, newcomers like China seek to adjust the old rules to reflect their interests as latecomers. But progress towards greater cooperation should be possible, once China acknowledges that US semiconductor firms need safeguards against forced technology transfer through policies like compulsory licensing, information security standards and certification, and restrictive government procurement policies. The US, in turn, needs to acknowledge that Chinese firms feel disadvantaged by restrictions on Chinese foreign direct investment (through CFIUS), and by restrictions on the export of technology to China, like the recent decision of the Commerce Department to slap technology export restrictions on US suppliers of semiconductor to China's ZTE. In the end, such policies may encourage China to shift to alternative suppliers in Korea, Taiwan, and to promote more aggressively domestic suppliers.

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Many mixes to match litho apps

ED KORCZYNSKI, *Senior Technical Editor*

The world's leading lithographers gather each year in San Jose, California at SPIE's Advanced Lithography conference to discuss how to extend optical lithography. So of all the NGL technologies, which will win out in the end?

"Mix and Match" has long been a mantra for lithographers in the deep-sub-wavelength era of IC device manufacturing. In general, forming patterns with resolution at minimum pitch as small as 1/4 the wavelength of light can be done using off-axis illumination (OAI) through reticle enhancement techniques (RET) on masks, using optical proximity correction (OPC) perhaps derived from inverse lithography technology (ILT). Lithographers can form 40-45nm wide lines and spaces at the same half-pitch using 193nm light (from ArF lasers) in a single exposure.

FIGURE 1 shows that application-specific tri-layer photoresists are used to reach the minimum resolution of 193nm-immersion (193i) steppers in a single exposure. Tighter half-pitch features can be created using all manner of multi-patterning processes, including Litho-Etch-Litho-Etch (LELE or LE2) using two masks for a single layer or Self-Aligned Double Patterning (SADP) using sidewall spacers to accomplish pitch-splitting. SADP has been used in high volume manufacturing (HVM) of logic and memory ICs for many years now, and Self-Aligned Quadruple Patterning (SAQP) has been used in HVM by at least one leading memory fab.

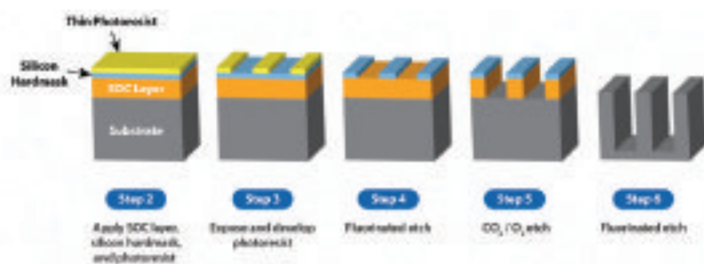

FIGURE 1. Basic tri-layer resist (TLR) technology uses thin Photoresist over silicon-containing Hard-Mask over Spin-On Carbon (SOC), for patterning critical layers of advanced ICs. (Source: Brewer Science)

Next-Generation Lithography (NGL) generally refers to any post-optical technology with at least some unique niche patterning capability of interest to IC fabs: Extreme Ultra-Violet (EUV), Directed Self-Assembly (DSA), and Nano-Imprint Lithography (NIL). Though proponents of each NGL have dutifully shown capabilities for targeted mask layers for logic or memory, the capabilities of ArF dry and immersion (ArFi) scanners to process >250 wafers/hour with high uptime dominates the economics of HVM lithography.

The world's leading lithographers gather each year in San Jose, California at SPIE's Advanced Lithography conference to discuss how to extend optical lithography. So of all the NGL technologies, which will win out in the end?

It is looking most likely that the answer is "all of the above." EUV and NIL could be used for single layers. For other unique patterning application, ArF/ArFi steppers will be used to create a basic grid/template which will be cut/trimmed using one of the available NGL. Each mask layer in an advanced fab will need application-specific patterning integration, and one of the rare commonalities between all integrated litho modules is the overwhelming need to improve pattern overlay performance.

Naga Chandrasekaran, Micron Corp. vice president of Process R&D, provided a fantastic overview of the patterning requirements for advanced memory chips in a presentation during Nikon's LithoVision technical symposium held February 21st in San Jose, California prior to the start of SPIE-AL. While resolution improvements are always desired, in the mix-and-match era the greatest challenges involve pattern overlay issues. "In high volume manufacturing, every nanometer variation translates into yield loss, so what is the best overlay that we can deliver as a holistic solution not just considering stepper resolution?" asks Chandrasekaran. "We should talk about cost per nanometer overlay improvement."

Extreme Ultra-Violet (EUV)

As touted by ASML at SPIE-AL, the brightness and stability and availability of tin-plasma EUV sources continues to improve to 200W in the lab "for one hour, with full dose

control," according to Michael Lercel, ASML's director of strategic marketing. ASML's new TWINSCAN NXE:3350B EUVL scanners are now being shipped with 125W power sources, and Intel and Samsung Electronics reported run their EUV power sources at 80W over extended periods.

During Nikon's LithoVision event, Mark Phillips, Intel Fellow and Director of Lithography Technology Development for Logic, summarized recent progress of EUVL technology: ~500 wafers-per-day is now standard, and ~1000 wafer-per-day can sometimes happen. However, since grids can be made with ArFi for 1/3 the cost of EUVL even assuming best productivity for the latter, ArFi multi-patterning will continue to be used for most layers. "Resolution is not the only challenge," reminded Phillips. "Total edge-placement-error in patterning is the biggest challenge to device scaling, and this limit comes before the device physics limit."

Directed Self-Assembly (DSA)

DSA seems most suited for patterning the periodic 2D arrays used in memory chips such as DRAMs. "Virtual fabrication using directed self-assembly for process optimization in a 14nm DRAM node" was the title of a presentation at SPIE-AL by researchers from Coventor in which DSA compared favorably to SAQP.

Imec presented electrical results of DSA-formed vias, providing insight on DSA processing variations altering device results. In an exclusive interview with Solid State Technology and SemiMD, imec's Advanced Patterning Department Director Greg McIntyre reminds us that DSA could save one mask in the patterning of vias which can all be combined into doublets/triplets, since two masks would otherwise be needed to use 193i to do LELE for such a via array. "There have been a lot of patterning tricks developed over the last few years to be able to reduce variability another few nanometers. So all sorts of self-alignments."

While DSA can be used for shrinking vias that are not doubled/tripled, there are commercially proven spin-on shrink materials that cost much less to use as shown by Kaveri Jain and Scott Light from Micron in their SPIE-AL presentation, "Fundamental characterization of shrink techniques on negative-tone development based dense contact holes." Chemical shrink processes primarily require control over times, temperatures, and ambients inside a litho track tool to be able repeatably shrink contact hole diameters by 15-25 nm.

Nano-Imprint Litho (NIL)

For advanced IC fab applications, the many different options for NIL technology have been narrowed to just one for IC HVM. The step-and-pattern technology that had been developed and trademarked as "Jet and Flash Imprint Lithography" or "J-FIL" by, has been commercialized for HVM by Canon NanoTechnologies, formerly known as Molecular Imprints (http://cnt.canon.com/). Canon shows improvements in the NIL mask-replication process, since each production mask will need to be replicated from a written master. To use NIL in HVM, mask image placement errors from replication will have to be reduced to ~1nm., while the currently available replication tool is reportedly capable of 2-3nm (3 sigma).

FIGURE 2 shows normalized costs modeled to produce 15nm half-pitch lines/spaces for different lithography technologies, assuming 125 wph for a single EUV stepper and 60 wph for a cluster of 4 NIL tools. Key to throughput is fast filling of the 26mmx33mm mold nano-cavities by the liquid resist, and proper jetting of resist drops over a thin adhesion layer enables filling times less than 1 second.

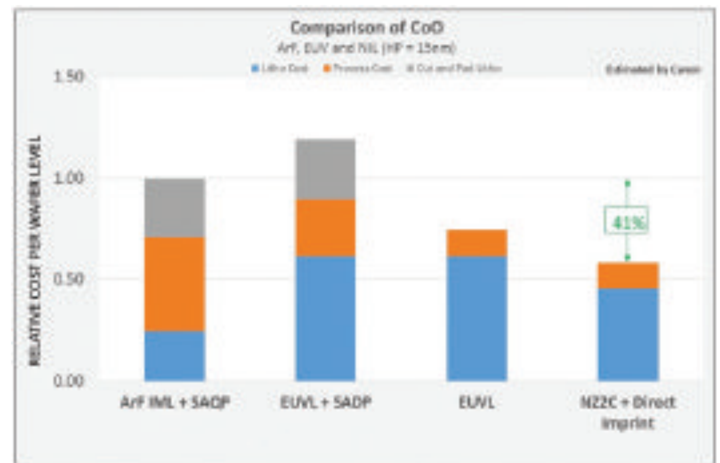

FIGURE 2. Relative estimated costs to pattern 15nm half-pitch lines/spaces for different lithography technologies, assuming 125 wph for a single EUV stepper and 60 wph for a cluster of 4 NIL tools. (Source: Canon)

Researchers from Toshiba and SK Hynix described evaluation results of a long-run defect test of NIL using the Canon FPA-1100 NZ2 pilot production tool, capable of 10 wafers per hour and 8nm overlay, in a presentation at SPIE-AL titled, "NIL defect performance toward high-volume mass production." The team categorized defects that must be minimized into fundamentally different categories—template, non-filling, separation-related, and pattern collapse—and determined parallel paths to defect reduction to allow for using NIL in HVM of memory chips with <20nm half-pitch features. ◆

Studying post-etching silicon crystal defects on 300mm wafers by automatic defect review AFM

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Atomic force microscopy is essential for obtaining three-dimensional information of crystal defects.

As integrated devices continue to shrink, incoming bare silicon wafer defectivity requirements become more and more stringent. The inspection of bare silicon wafers for surface defects is predominantly accomplished by measuring the difference in laser light scattering (LLS) between the clean surface and a surface defect, where the intensity of the scattered signal is compared to the LLS of a standard latex sphere. The actual surface defectivity can originate from added particles, topological defects, and crystal imperfections. To be able to reduce the number of defects one must know the source of the defect. LLS inspection can only give defectivity counts and a relative size. Therefore, one must rely on defect review techniques such as SEM and AFM to determine the nature and origin of the defects.

SEM provides two-dimensional aerial images of the defects which lacks the information about depth or height of the defects. On the other hand, AFM can provide three-dimensional topography images of the defects with the highest vertical resolution among all techniques[1]. The shortcomings of conventional AFM systems were low throughput, limited tip life, and arduous efforts for locating the DOI on the 300 mm wafers. To address the limitations of conventional of AFM systems for defect review, ADR AFM has been introduced for 300 mm wafers recently[2]. We used ADR AFM in this study for studying the defects found by LLS inspection tool.

In this study we focus on very small crystal imperfections which are not easily observed by LLS without some means to make them larger. We have used a decorative etching technique to highlight crystal imperfections to be studied by LLS, SEM, and AFM. The defect analysis can only be accomplished with accurate and reproducible defect coordinate transfer between analysis tools. Here we show how we have successfully and reliably found and characterized the decorated defects by ADR AFM.

ADR AFM procedure

The process in ADR AFM is depicted in **FIGURE 1**. During this process, the defects of interest are located accurately and imaged non-destructively. Two factors are essential in order to achieve these objectives. First proper linkage between ADR AFM and LLS inspection tool is required to minimize the positioning errors and locate the defects accurately. The linkage for blank wafers is achieved by sample coordinate alignment. Generally there are no alignment markers or fiducials available on blank wafers to be used for alignment. Therefore ADR AFM uses specialized vision to perform the sample alignment

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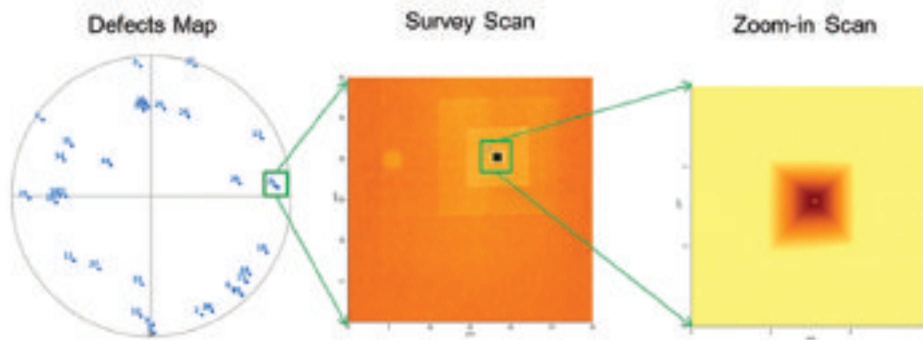

FIGURE 1. The schematic shows ADR AFM process for this study. After completing coordinate mapping, ADR AFM will automatically perform survey scan, zoom-in scan, processing, analysis, and classification for each defect.

properly. Another important factor in AFM defect review is non-contact mode imaging which is required for non-destructive imaging of the samples while preserving AFM tip life such that the tip can last throughout the process for multiple defects.

Coordinate alignment

Sample coordinate alignment is needed for proper linkage between the stage coordinates of ADR AFM andLLS inspection tool. In the case of blank wafers, no fiducial or alignment marker exists on the sample to be used for sample alignment. To overcome this challenge, a coarse alignment followed by a fine alignment is performed. In the coarse alignment, three randomly selected peripheral and the notch or an angular reference are selected to correct for translational and rotational errors. This is followed by a fine alignment to eliminate positioning errors due to non-affinity between the stage coordinates of ADR AFM and LLS inspection tool. A few large defects with known inspection coordinates are used for performing fine alignment. Since the defects are hardly visible in a standard AFM optical image, an enhanced vision is used to locate the defects in the optics of the ADR AFM and utilize the defects as aligner markers. Upon the sample alignment, ADR AFM is able to locate additional defects accurately. More details on coordinate alignment can be found in ref [2].

Enhanced vision

Enhanced vision is utilized during fine coordinate alignment to locate the defects in the optical vision of ADR AFM. The technique is developed based on well-known differential frame averaging of the optical frames collected from the sample surface at two accurately separated locations. The sample can be moved accurately since ADR AFM uses a separated Z and XY scanners configuration. This architecture was initially developed to eliminate the crosstalk between the XY and Z scanners (which has been a common artifact in tube scanner based AFM systems)[2]. In this setup, sample is moved by XY scanner while tip is following the sample topography by Z scanner. In enhanced vision, the optical frames of the sample are collected at

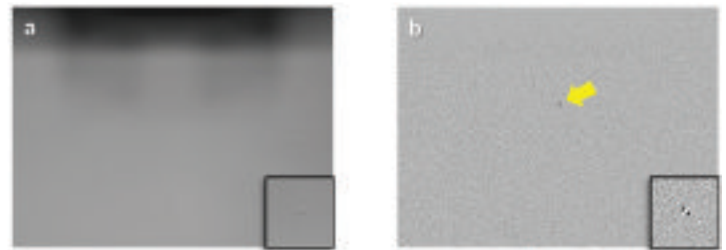

FIGURE 2. Images collected viaa) standard vs. b) enhanced vision of the surface of a bare silicon wafer with one small defect are shown. The insets showmagnified views of the defect. The small defect is easily observable in enhanced vision. The larger image dimensions are 550 μm × 413 μm.

two precisely separated locations, and then the final frame is generated from the difference between the collected frames. The resulting frame possesses an enhanced contrast of surface details which are not easily observable in the standard vision of ADR AFM. A comparison between the frames collected by standard vision versus enhanced vision is depicted in **FIGURE 2**.

Non-contact mode imaging

Non-contact mode is the standard imaging mode in ADR AFM. It is essential to maintain tip sharpness during the defect review process from the first to the last defect that is located and imaged. In addition to keeping tip costs low, well-maintained tip sharpness ensures consistent image quality and accuracy between the images of all defects during the process. It therefore enables the automated system to uninterruptedly locate and image the defects with a high throughput. In order to perform non-contact mode imaging, the AFM cantilever is oscillated at its resonance frequency. The oscillating cantilever is brought close enough to the sample that the oscillation amplitude reduces to a pre-defined set point due to the van der Waals tip sample interaction. ADR AFM maintains the oscillation amplitude to avoid tip contacting the sample. As the tip scans the sample surface, the oscillation amplitude is maintained by moving the cantilever up and down

with the Z scanner to maintain its tip sample interaction in attractive regime. More details on non-contact mode imaging can be found in reference[4]. Although ADR AFM's functionality is based on non-contact mode imaging, it is capable of performing in other dynamic or contact imaging modes if needed.

Automatic defect search and imaging

The significant improvements in throughput of defect review are obtained by ADR AFM due to its fully automated process. Once defect coordinates from LLS inspection tool are entered into ADR AFM, coordinate alignment is performed, the defect is located and imaging starts for the list of selected defects. The process of locating and imaging the defects is fully automated. The automation includes locating the defect, tip-sample engagement, non-contact mode parameter optimization, survey scan, optimizing the scan size, final scan, processing, and defect classification. Defects can be classified into two groups of bumps and pits. Defects are typically located within ±10 µm of their LLS coordinates.

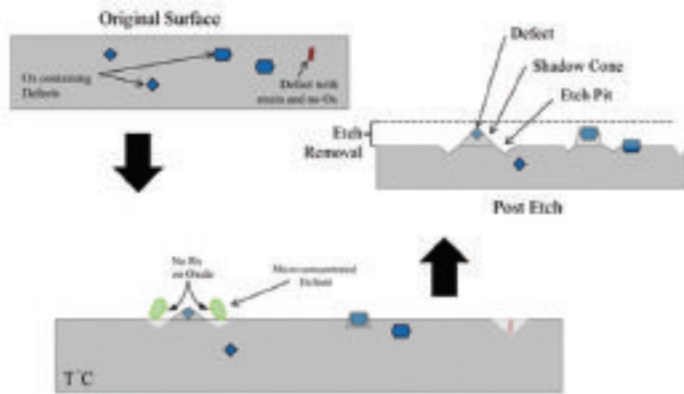

FIGURE 3. Schematic of the process used to decorate crystal imperfections for defect inspection.

Sample preparation

Bare 300mm diameter CZ silicon wafers were treated with a gaseous acid in a reducing atmosphere at a temperature and for a sufficient duration to grow the crystal imperfections [3]. The size and shape of the decorated defects depends on the nature of the original defect as shown in **FIGURE 3**. Once decorated, the defect size is capable of being detected as LLS event. The LLS inspection tool locates and sizes the LLS events, providing the coordinates to be used by the SEM and AFM.

FIGURE 4. The results of defect review with ADR AFM and comparison with SEM are shown. ADR AFM was able to locate and image all the 34 defects. Defects 22 to 34 were not found in SEM. Wafer notch is up in AFM and down in SEM. AFM and SEM images are 180 degree rotated with respect to each other.

Results

A wafer containing surface decorated defects was inspected by a LLS tool and 34 defects were selected to be reviewed by ADR AFM. The coordinates of the defects were entered to ADR AFM, coordinate alignment performed, and the defects were located and imaged by ADR AFM. The first 21 defects had been imaged by SEM before being studied by ADR AFM. However, SEM images only provide aerial two-dimensional view of defects without sufficient information on the defects depth and out of plane dimensions. The remaining 13 defects were not found by SEM despite the signal collected by the LLS tool. The summarized results of decorated defect study with ADR AFM and comparison with SEM results aredemonstrated in **FIGURE 4**. ADR AFM was able to find all the 34 defects including those that had not been found by SEM.

The defects selected to be reviewed by ADR AFM belong to eight types according to their LLS signal. The tentative classification by the LLS tool is based on the defect's light scattering which is dependent on morphology, depth, and presenece of a central defect. As the decorative etching process proceeds, crystal imperfections are exposed and etch at a different rate than the perfect crystal surface. Defects exposed at the initial stages of the etch are deeper and more developed than defects exposed late in the etching proccess. Defects with an inverted pyramid shape are generally deeper and posses higher LLS signal. They are classified as "Facet". Defects with curved shape formed during the late stages of etching are shallower. These defects are classified as "Shallow". Some defects

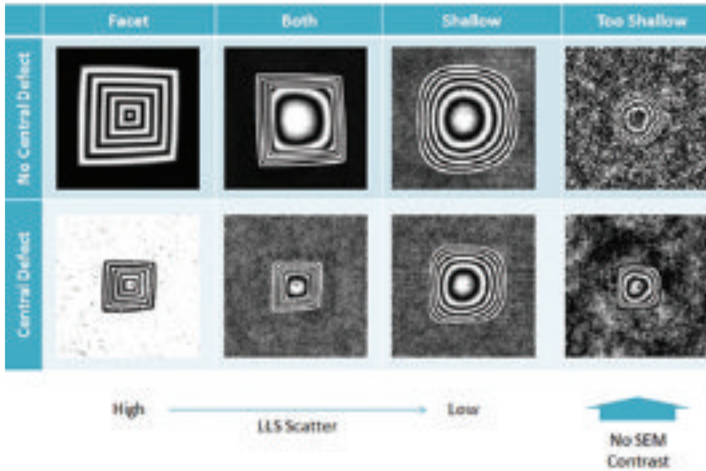

FIGURE 5. Defect classification based on the LLS, SEM and AFM data.

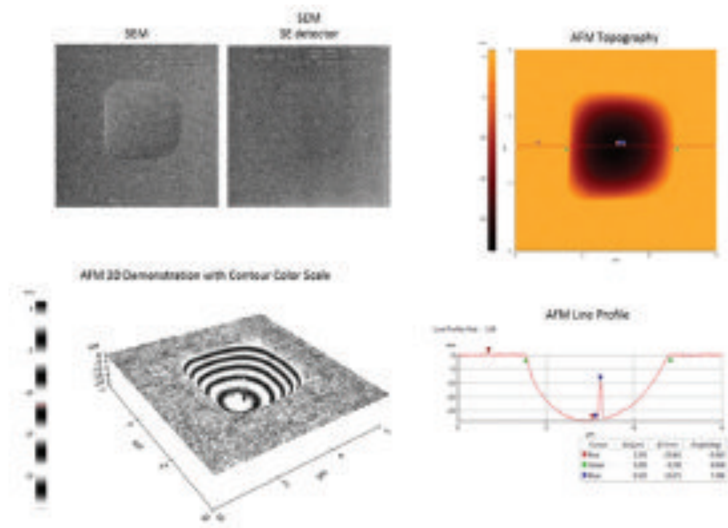

FIGURE 6. Comparison between the data collected with SEM versus AFM. SEM image provides an aerial 2D view of the defect. Secondary electron image indicates the presence of center defect. AFM image, in addition to aerial 2D view, includes the 3D data. Therefore a line profile, 3D demonstration, and contoured color scale can be utilized to obtain more information.

are exposed at an intermediate point in the decorative etch and have some degree of faceted walls with curved bottom. This category is classfied as "Both". Defects which have only started to be decorated have a very weak LLS signal and are classified as "Too shallow". The defects are also categorized whether or not they have the center defect, hence, a total of eight defect types were identified. The defect classification is tabulated in **FIGURE 5**.

As we go from left to right side of the table in figure 5, the LLS signal become weaker. This was attributed to the depth of defects and the sharpness of the defect's edges. AFM images confirmed the depth difference between different classes of defects. Since the AFM images contain Z heights, we were able to use a banded color scale to depict the surface topography of the defects more accurately in 2D view.

Discussion

FIGURE 6 depicts a comparison between the data collected with SEM vs. AFM for the same defect. Primary SEM image provides an aerial 2D view of the defect. However, the shallow depth of the defect reaches the limitations of SEM, hence, poor contrast in the image. As indicated in Fig. 5, shallower defects were not found by SEM. A secondary electron image helps identify the center defect. Identification of center defect by secondary electron is possible only if the defect was found in primary SEM image.

On the other hand, AFM image not only provides an aerial view of the defect, it also contains the height/depth values for each pixel. Therefore, more information can be obtained about the true topology of the defect by using a 3D representation of the AFM image or using a contoured color scale. Contoured color scales can also help understanding the topology of the defect in aerial view as shown in figure 5. As indicated before, AFM has the highest vertical resolution among all imaging techniques [1], hence, better contrast of AFM images in aerial view.

All of the 34 defects were found by ADR AFM including the 13 defects that were not found by SEM. **FIGURE 7** depicts the AFM images a defect that was not found by SEM. The defect depth is below 4 nm and contains a center defect. This example indicates once again the limitation of SEM resolution in out of plane direction.

It was indicated above that ADR AFM is a non-destructive imaging technique. It utilizes non-contact mode imaging

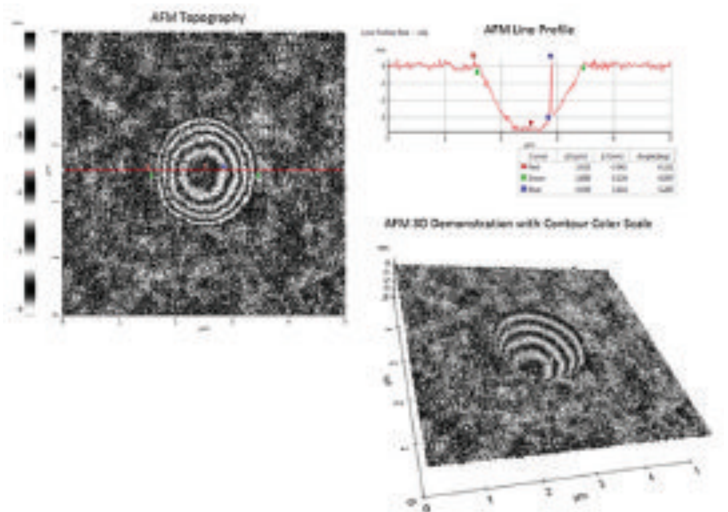

FIGURE 7. AFM data for defect #24 is shown here. The defect was not found by SEM due to its shallow depth.

for survey scan and final imaging scan. However, SEM beam can still modify the sample surface. **FIGURE 8** indicates the sample contamination as a result of electron beam "burning" the surface during SEM imaging. These SEM burn-mark sizes are related to the SEM magnification. Figure 8 shows that several SEM magnifications were used in analyzing this defect.

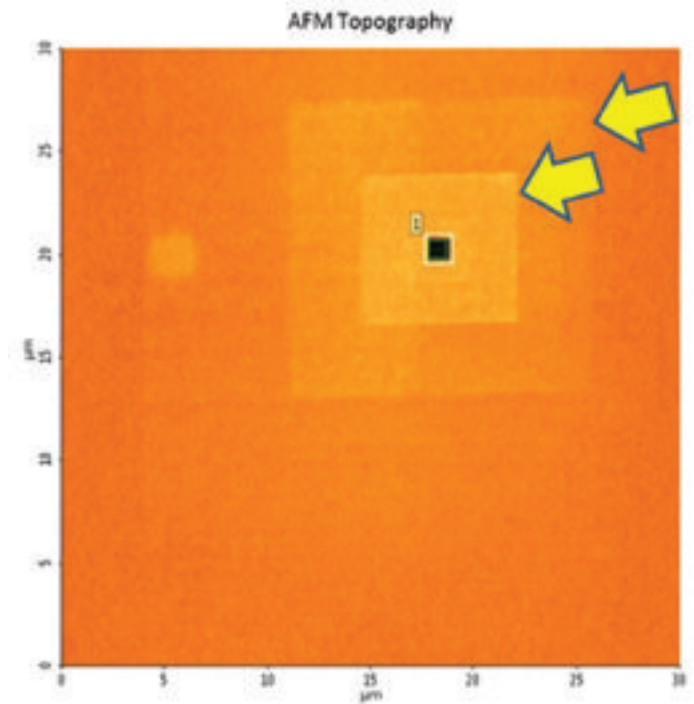

FIGURE 8. AFM image of a Facet defect with several SEM burn-marks is shown. The SEM burn-marks are marked by arrows.

Summary

We have demonstrated the power of the ADR AFM to provide quality 3D information for defect review on bare silicon wafers. Crystal defects on surface of a 300 mm wafer are highlighted using a decorative etching technique. The surface defects are located by LLS inspection. Select defects of various classes are studies by SEM and ADR AFM. While shallow defects are not found by SEM, ADR AFM successfully found all the defects and provided high resolution three-dimensional topographical information of the defects. With the automated ADR AFM this type of analysis is simple and yet powerful.

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Monolithic Schottky diode in ST F7 LV MOSFET technology: Performance improvement in application

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Standard solutions and devices are compared to a 60 V MOSFET with monolithic Schottky diode as evaluated in SMPS and motor control environments.

In synchronous rectification and in bridge configuration, R_{DSon} and Q_g are not the only requirements for power MOSFETs. In fact, the dynamic behavior of intrinsic body-drain diode also plays an important role in the overall MOSFET performances. The forward voltage drop ($V_{F,diode}$) of a body-drain diode impacts the device losses during freewheeling periods (when the device is in off-state and the current flows from source to drain through the intrinsic diode); the reverse recovery charge (Q_{rr}) affects not only the device losses during the reverse recovery process but also the switching behavior, as the voltage spike across the MOSFET increases with Q_{rr}. So, low V_{FD} and Q_{rr} diodes, like Schottky, can improve overall device performance, especially when mounted in bridge topologies or used as synchronous rectifiers—especially at high switching frequency and for long diode conduction times. In this article, we compare standard solutions and devices to a 60 V MOSFET with monolithic Schottky diode as evaluated in SMPS and motor control environments.

Intrinsic MOSFET body-drain diode and Schottky features

In **FIGURE 1**, the typical symbol for an N-channel Power MOSFET is depicted. The intrinsic body-drain diode is formed by the p-body and n--drift regions and is shown in parallel to the MOSFET channel.

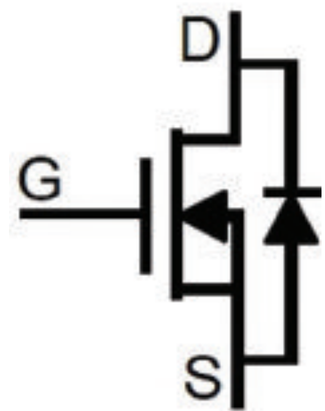

FIGURE 1. Symbol of a Power MOSFET.

Once a Power MOSFET is selected, the integral body diode is fixed by silicon characteristic and device design. As the intrinsic body diode is paralleled to the device channel, it is important to analyze its static and dynamic behavior, especially in applications where the body diode conducts. So, maximum blocking voltage and forward current have to be considered in reverse and forward bias, while, when the diode turns-off after conducting, it is important to investigate the reverse recovery process (**FIGURE 2**). When the diode goes from forward to reverse bias, the current doesn't reduce to zero immediately, as the charge stored during on-state has to be removed. So, at $t = t_0$, the diode commutation process starts, and the current reduces with a constant and slope

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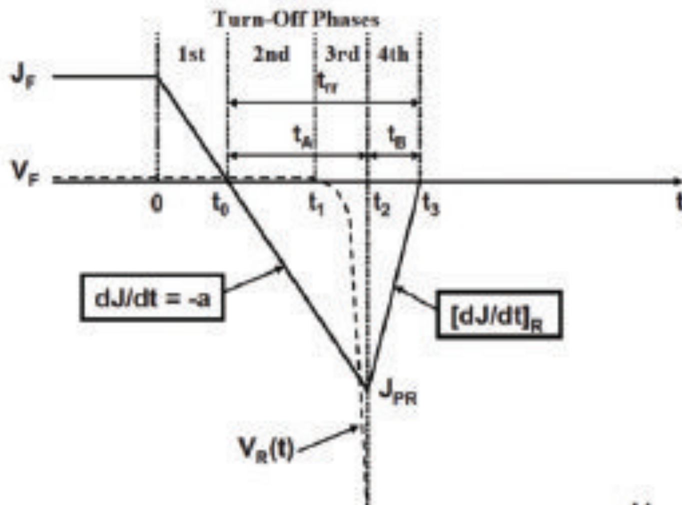

FIGURE 2. Diode reverse recovery process.

(-a), fixed only by the external inductances and the supply voltage. The diode is forward biased until t1, while from t_1 to t_2, the voltage drop across the diode increases, reaching the supply voltage with the maximum reverse current at $t=t_2$. The time interval (t_3-t_0) is defined as reverse recovery time (t_{rr}) while the area between negative current and zero line is the reverse recovery charge (Q_{rr}).The current slope during t_B is linked mainly to device design and silicon characteristics.

The classification of soft and snap recovery is based on the softness factor : ($S = \frac{t_B}{t_A}$) this parameter can be important in many applications. The higher the softness factor, the softer the recovery. In fact, if t_B region is very short, the effect of quick current change with the circuit intrinsic inductances can produce undesired voltage overshoot and ringing. This voltage spike could exceed the device breakdown voltage: moreover, EMI performances worsen. As shown in Fig. 2, during diode recovery, high currents and reverse voltage can produce instantaneous power dissipation, reducing the system efficiency. Moreover, in bridge topologies, the maximum reverse recovery current of a Low Side device adds to the High Side current, increasing its power dissipation up to maximum ratings. In switching applications, like bridge topologies, buck converters, or synchronous rectification, body diodes are used as freewheeling elements. In these cases, reverse recovery charge (Q_{rr}) reduction can help maximize system efficiency and limit possible voltage spike and switching noise at turn-off. One strategy to reach this target to integrate a Schottky diode in the MOSFET structure. A Schottky diode is realized by an electrical contact between a thin film of metal and a semiconductor region. As the current is mainly due to majority carriers, Schottky diode has lower stored charge, and consequently, it can be switched from forward to reverse bias faster than a silicon device. An additional advantage is its lower forward voltage drop (≈0.3 V) than Si diodes, meaning that a Schottky diode has lower losses during the on state.

Embedding the Schottky diode in a 60V power MOSFET is the right device choice when Q_{rr} and $V_{F,diode}$ have to be optimized to enhance the overall system performance. In **FIGURE 3**, the main electrical parameters of standard and integrated Schottky devices (same BVD_{SS} and die size) are reported.

	BV @ 250µA	R_{DSon} @ 30 A	Q_{rr}	$V_{F,diode}$
60V MOS std	>60 V	1.2 mΩ	100 nC	600 mV
60V MOS with Schottky	>60 V	1.3 mΩ	90 nC	250 mV

FIGURE 3. MOSFET parameters.

Benefits of Mono Schottky in a power management environment

In a synchronous buck converter (**FIGURE 4**), a power MOSFET with integrated Schottky diode can be mounted as a Low Side device (S2) to enhance the overall converter performance.

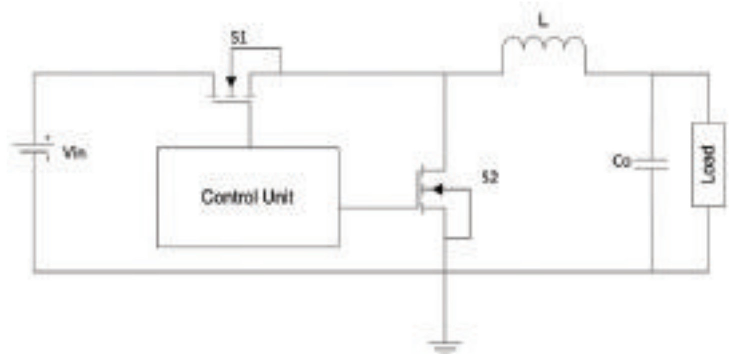

FIGURE 4. Single phase synchronous buck converter topology.

In fact, Low Side body diode conduction losses ($P_{diode,cond}$) and reverse recovery losses (P_{Qrr}) are strictly related to the diode forward voltage drop ($V_{F,diode}$) and its reverse recovery charge (Q_{rr}):

$$P_{diode,cond} = V_{F,diode} \cdot I_{OUT} \cdot f_{SW} \cdot t_{dead} \quad (1)$$

$$P_{Qrr} = Q_{rr} \cdot f_{SW} \cdot V_{IN} \quad (2)$$

As shown in (1) and (2), these losses increase with the switching frequency, the converter input voltage, and the output current. Moreover, the dead time, when both FETs are off and the current flows in the Low Side body diode, seriously affects the diode conduction losses: with long dead times, a low diode forward voltage drop helps to minimize its conduction losses, therefore increasing the efficiency. In **FIGURE 5**, the efficiency in a 60W, 48V - 12V, 250 kHz synchronous buck converter is depicted.

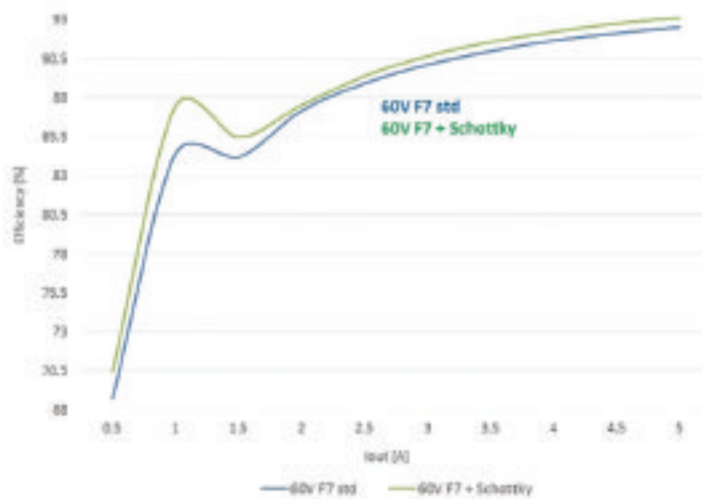

FIGURE 5. Efficiency in a synchronous buck converter.

Now, considering isolated power converters' environment, when the output power increases and the dead time values are high, the right secondary side synchronous rectifier should have not only R_{DSon} as low as possible to reduce conduction losses, but also optimized body diode behavior (in terms of Q_{rr} and $V_{F,diode}$) in order to reduce

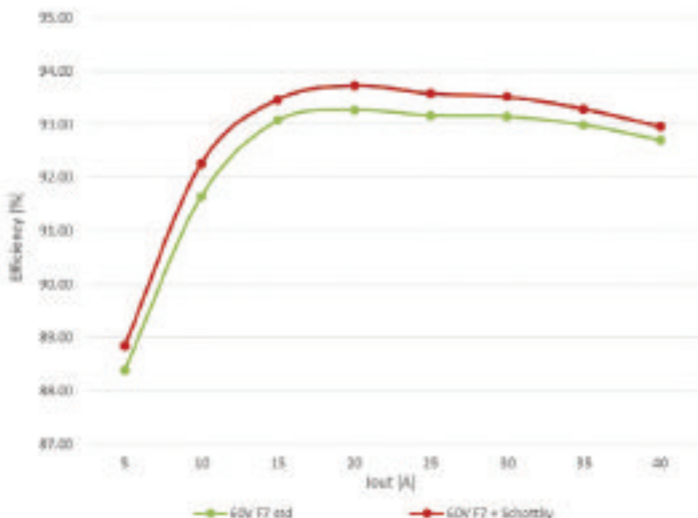

FIGURE 6. Efficiency in LLC converter.

diode losses (as reported in (1) and (2)) and to minimize possible voltage spikes during turn-off transient. The 60V standard MOSFET and one with Schottky integrated devices are compared in a 500W digital power supply, formed by two power stages: power factor corrector and an LLC with synchronous rectification. The maximum output current is 42 A, while the switching frequency at full load is 80 kHz, and the dead time is 1μs. The efficiency curves are compared in **FIGURE 6**.

In both topologies, the *60 V plus Schottky* device shows higher efficiency in the entire current range, an improvement in overall system performance.

Switching behavior improvement in bridge topologies

In bridge topologies, reverse recovery process occurs at the end of the freewheeling period of the Low Side device (Q2 in **FIGURE 7**), before the High Side (Q1 in Fig. 7) starts conducting. The resulting recovery current adds to the High Side current (as previously explained). Together with the extra-current on the High Side device, the Low Side reverse recovery and its commutation from $V_{ds} \approx 0$ V to V_{dc} can produce spurious bouncing on the Low Side gate-source voltage, due to induced charging of Low Side C_{iss} (input capacitance) via C_{rss} (Miller capacitance).

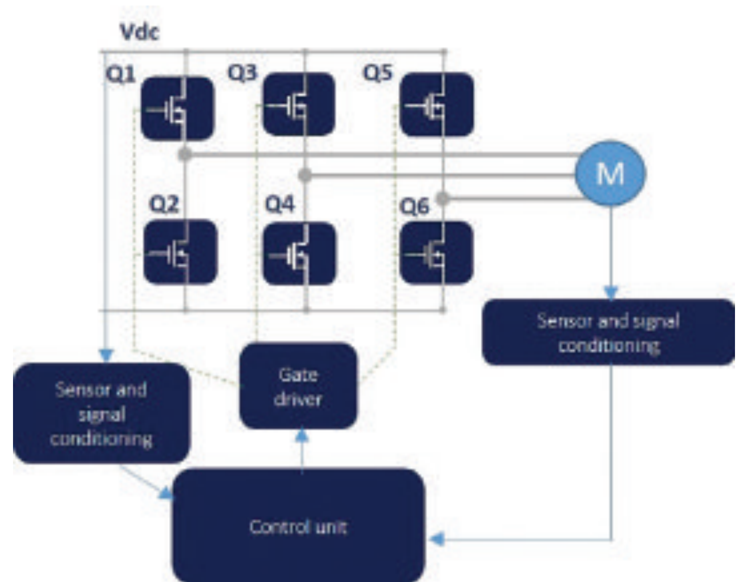

FIGURE 7. Full-bridge converter schematic.

As a consequence, the induced voltage on Q2 gate could turn-on the device, worsening system robustness and efficiency. A Low Side device, in bridge configuration, should have soft commutation, without dangerous

voltage spikes and high frequency ringing across drain and source. This switching behavior can be achieved using power MOSFETs with integrated Schottky diode as Low Side devices. In fact, the lower reverse recovery charge (Q_{rr}) has a direct impact on the overshoot value. In fact, the higher the Q_{rr}, the higher the overshoot. Lower values for V_{ds} overshoot and ringing reduce the spurious voltage bouncing on the Low Side gate, limiting the potential risk for a shoot-through event. Furthermore, soft recovery enhances overall EMI performances, as the switching noise is reduced. In **FIGURE 8** are shown the High Side turn-on waveforms for standard and embedded Schottky devices; purple trace (left graph) and green trace (right graph) are Low Side gate-source voltages. The device with Schottky diode shows a strong reduction of Low Side spurious bouncing.

Summary

In many applications (synchronous rectification for industrial and telecom SMPS, DC-AC inverter, motor drives), choosing the right MOSFET means not only considering R_{DSon} and Q_g but also evaluating the static and dynamic behavior of the intrinsic body-drain diode. A 60V "F7" power MOSFET with integrated Schottky diode ensures optimized performances in efficiency and commutation when a soft reverse recovery with low Q_{rr} is required. Furthermore, the low $V_{F,diode}$ value achieves higher efficiency when long freewheeling periods or dead-times are present in the application.

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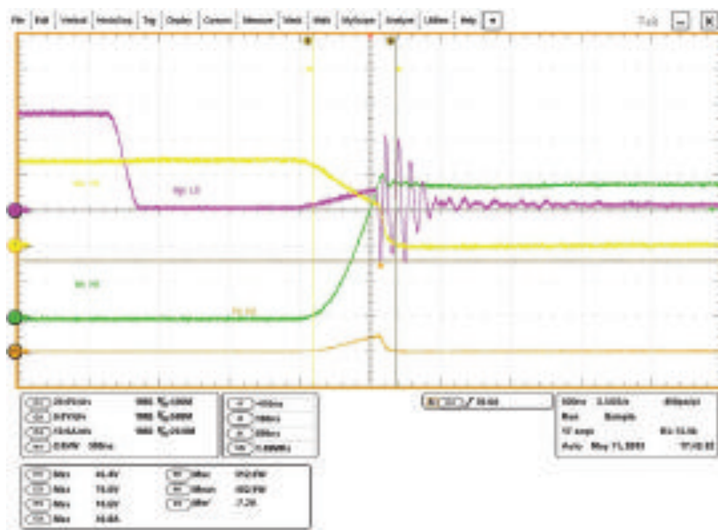

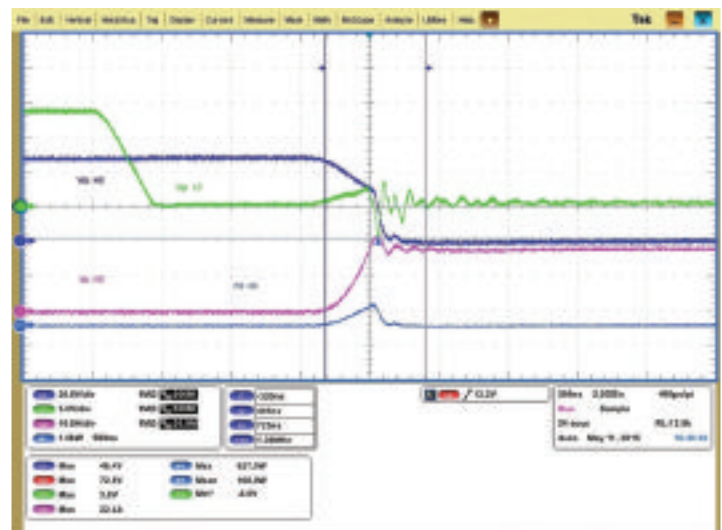

FIGURE 8. Standard FET HS turn-on (left) and embedded Schottky FET HS turn-on waveforms (right).

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Tech Industry security highlighted by the iPhone access controversy

The confrontation between Apple and the FBI over the FBI's request for assistance in hacking a known terrorist's iPhone brought the topic of security to the top of the agenda for the tech industry. Recent developments, including the FBI's withdrawal of its request and Apple's subsequent demand that the FBI now share information the security vulnerability that permitted a third party to hack the iPhone, have only emphasized the "moving target" nature of security. Whether manufacturing a car, a smartphone, or a smartcard, security is an important aspect to consider and plan into the supply chain. And concerns about security will only increase if the IoT grows as explosively as many industry pundits are now predicting.

> "It is imperative to establish a certain level of trust that such objects will not provide a backdoor or counterfeit identity that could jeopardize an entire network…"

One of the defining characteristics of "things" for the IoT is their autonomous connectivity. With the likelihood that there will soon be tens or hundreds of millions of these things connected to networks everywhere, it is imperative to establish a certain level of trust that such objects will not provide a backdoor or counterfeit identity that could jeopardize an entire network and the costly infrastructure of service providers.

Fortunately, the industry has already encountered this problem and developed a workable solution for smartcards with the concept of secured product manufacturing test flows. Admittedly, it has an impact on the requirement for test infrastructure and complexity, but it is a well proven solution. Essentially, it addresses the security and confidentiality requirements of IoT devices for encrypted certificates of authentication or secret token keys by isolating the injection of these secrets at the die or SiP (system in package) level within a secured final test and assembly environment.

The specific concerns that must be addressed in this secure environment include:

- How to ensure that each die in an IoT SiP/McM (multichip module) device can be tested along a route of trust.
- How to provide a seamless test manufacturing flow that efficiently and effectively detects manufacturing quality issues while injecting secrets from customers, without storing the secret information, needing to decrypt it, or leaving it open to reverse engineering.
- How the injection of secrets/certificates impacts DFT and diagnosis of the chip.

These sensitive operations require the insertion of secret keys, tokens, certificates and boot loaders into the device during wafer probe or at final test on the package level. The secret vectors must be dynamically allocated and are often reshuffled by the end-customers to disaggregate the supply chain. The test floor must include an encrypted server gateway, and the ability to selectively push the encrypted information into the right device on wafer, which is usually locked at the end of the wafer test and completely isolated when the wafer is sawn. Test and assembly is really the only opportunity to address confidentiality since the heterogeneous nature an IoT devices necessarily involves the sourcing of die from different vendors and requires validation of trust for each component. Test providers that can deliver a secure workflow will be critical contributors to the security of the IoT. ◑

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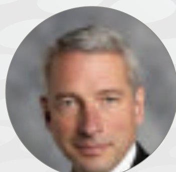

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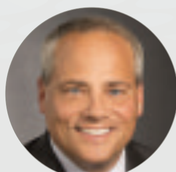

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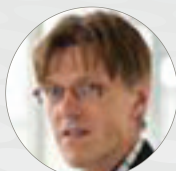

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