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FD-SOI is increasingly the de facto technology for many applications including entry-level application processors for smartphones, system-on-chip (SoC) devices for autonomous driving and IoT, and all mmWave applications such as 5G transceivers and radar systems for automotive electronics.

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The ConFab Preview

The agenda is set for The ConFab, to be held May 14-17, 2017 in San Diego at the iconic Hotel del Coronado. While reviewing the abstracts for just the Monday morning session, it struck me how well our speakers will cover the complex opportunities and challenges facing the semiconductor industry.

In the opening keynote, for example, Hans Stork, Senior Vice President and Chief Technical Officer, ON Semiconductor we will discuss the challenge to realize high signal to noise ratio in small (read inexpensive) and efficient form factors, using examples of image sensors and power conversion in automotive applications. "It seems that at last, after many decades of exponential progress in logic and memory technologies, the "real world" devices of power handling and sensor functions are jointly enabling another wave of electronics progress in autonomously operating and interacting Things," he said.

Next, Subramani Kengeri, Vice President of CMOS Platforms Business Unit, GLOBALFOUNDRIES, will describe how the rapid growth of applications in the consumer, auto and mobile space coupled with the emergence of the Internet of Things (IoT) is driving the need for differentiated design and technology solutions. "While die-cost scaling is slowing down and power density is emerging as a major challenge, fabless semiconductor companies are hungry for innovation using application optimized technology solutions. Specifically, emerging SoC innovations are driving the need for low-power, performance, cost, and time-to-volume that solves the issues of voltage scaling and integration of "user-experience" functions," he notes.

Islam Salama, a Director with Intel Corporation responsible for packaging substrate Pathfinding of the high-density interconnect across all Intel products, looks at it from a connectivity perspective. "The pervasive nature of computing drives a need for connecting billions of people and tens of billions of devices/things via cloud computing. Such connectivity effect will generate tremendous amounts of data and would require a revolutionary change in the technology infrastructures being used to transmit, store and analyze data," he said.

Next-generation electronics will require several new packaging solutions, he adds. Smaller form factors, lower power consumption, flexible designs, increased memory performance, and-more than ever, a closely managed silicon package, co-optimization and architectural innovations. Heterogeneous integration through package with technologies such as system in package (SIP), on package integration (OPI) and fan-out (WLFO and PLFO) are poised to change the packaging industry and play a disruptive role in enabling next generation devices.

Heterogeneous Integration is also the focus of a talk by Bill Bottoms, Chairman and CEO, Third Millennium Test Solutions. Bill will report on the collaboration in the making of the HIR Roadmap to address disruptive changes in the global IT network, the explosive growth coming for IoT sensors and the multi-sensor fusion and data analytics that extract "awareness" from the expanding data.

I'm very much looking forward to these and many other talks this year, and the exciting panel discussions and networking events we have planned.

—Pete Singer, Editor-in-Chief

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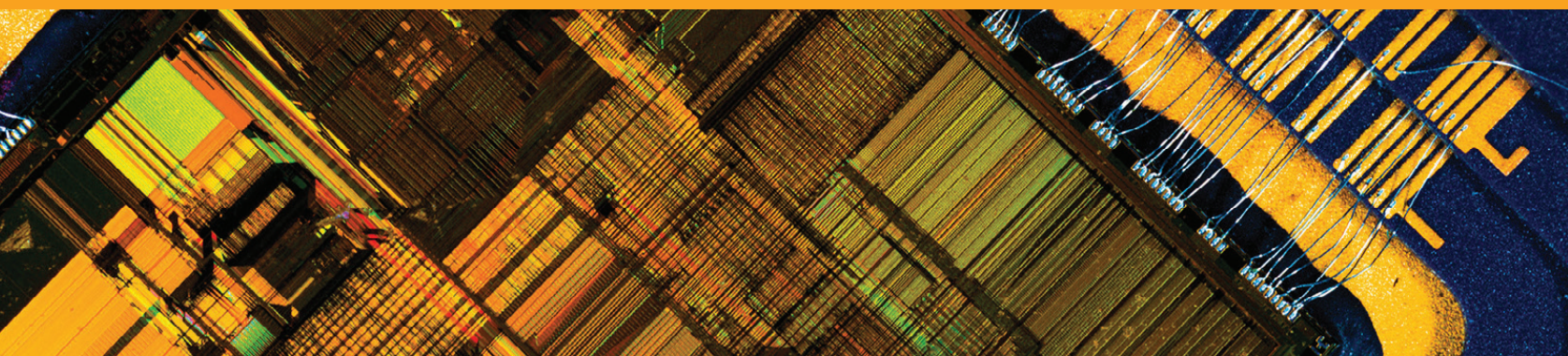

Web Exclusives

Lithographic stochastic limits on resolution

The physical and economic limits of Moore's Law are being approached as the commercial IC fab industry continues reducing device features to the atomic-scale. Early signs of such limits are seen when attempting to pattern the smallest possible features using lithography. Stochastic variation in the composition of the photoresist as well as in the number of incident photons combine to destroy determinism for the smallest devices in R&D. The most advanced Extreme Ultra-Violet (EUV) exposure tools from ASML cannot avoid this problem without reducing throughputs, and thereby increasing the cost of manufacturing.

http://bit.ly/2omsIAS

The ConFab 2017 announces leading semiconductor industry keynotes

The ConFab 2017 is excited to welcome these distinguished Keynote speakers: Hans Stork, Senior Vice President and Chief Technical Officer at ON Semiconductor; Mohan Trivedi, Distinguished Professor of Electrical and Computer Engineering and founding director of the Computer Vision and Robotics Research Laboratory, as well as the Laboratory for Intelligent and Safe Automobiles at the University of California San Diego; Dr. Alissa Fitzgerald, Founder and Managing Member of A.M. Fitzgerald & Associates, and Bill McClean, President of IC Insights.

http://bit.ly/2oDQt2b

Edge placement error control in multi-patterning

SPIE Advanced Lithography remains the technical conference where the leading edge of minimum resolution patterning is explored, even though photolithography is now only part of the story. Leading OEMs continue to impress the industry with more productive ArFi steppers, but the photoresist suppliers and the purveyors of vacuum deposition and etch tools now provide most of the new value-add. Tri-layer-resist (TLR) stacks, specialty hard-masks and anti-reflective coatings (ARC), and complex thin-film depositions and etches all combine to create application-specific lithography solutions tuned to each critical mask. (From SemiMD.com)

http://bit.ly/2miYPid

n&b news and blogs

Insights from the Leading Edge: IMAPS DPC Part 1: New MIL Qualified Player in FOWLP

The annual IMAPS Device Packaging Workshop was held at its usual location outside Scottsdale, AZ in early March.

http://bit.ly/2oe043k

Further thoughts from the 2017 SPIE AL EUV Lithography conference

In the previous blog, I listed technology status and would now like to discuss a couple of topics in detail. During last year's SPIE AL conference, the message for EUVL was "Not If, but When." This year the message was "Not If, but When and How Much Volume." It was nice to see the technology that I bet on so long ago coming so far and doing so well.

http://bit.ly/2odTvh4

How critical area analysis optimizes memory redundancy design

As any design engineer knows, the farther downstream a design goes, the less likely a manufacturing problem can be corrected without a costly and time-consuming redesign. And it doesn't matter if you are a fabless, fab-lite, or independent device manufacturer (IDM) company—reducing a design's sensitivity to manufacturing issues should ideally be handled by the design teams. By identifying and resolving design for manufacturing (DFM) problems while the design is still in its early stages, many manufacturing ramp-up issues can be avoided altogether. (From SemiMD.com)

http://bit.ly/2nkuXPe

EUVL masks may need to be tool-specific

Now we hear that EUVL might require fabs to park work-in-progress (WIP) lots of wafers behind a single critical tool with an idealistic 80% availability on a good day, and lots of downtime bad days. (From SemiMD.com)

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EUROPE - **Soitec** and **Silicon Genesis Corp.** have successfully brought an end to the dispute regarding the importation and sale in the United States of certain SOI wafers.

USA - **Intel** announced that Omar Ishrak and Greg Smith have been elected to Intel's board of directors.

ASIA - **Microsemi** announced the planned closure of its manufacturing facility in China.

USA - **Peregrine Semiconductor** announced the acquisition of Arctic Sand Technologies.

ASIA - **STATS ChipPAC** announced that it has shipped 1.5 billion fan-out wafer level packages (FOWLP), also known in the industry as embedded Wafer Level Ball Grid Array (eWLB).

USA - **SEMI** announced that it has moved its headquarters office to Milpitas, Calif.

ASIA - Over 60,000 were in attendance at the **SEMICON China** opening at Shanghai New International Expo Centre (SNIEC).

EUROPE - **EV Group (EVG)** unveiled the IQ Aligner NT–its latest and most advanced automated mask alignment system for high-volume advanced packaging applications.

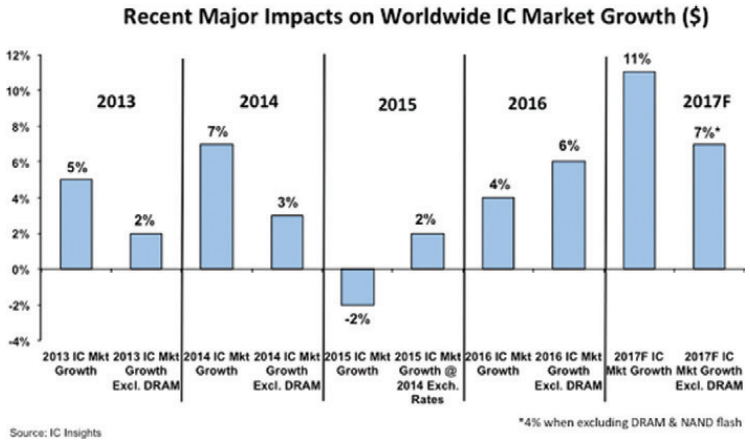
USA - **Kateeva** announced that it is expanding its Silicon Valley headquarters, leasing an adjacent building at its Newark campus, adding 75,000 sq. ft. that is zoned for manufacturing and business operations.

ASIA - **Soitec** began the ramp up to high-volume production of 200mm silicon-on-insulator (SOI) wafers at the manufacturing facility of its Chinese partner Shanghai Simgui Technology Co., Ltd.

EUROPE – **Imec** announced that their 200mm gallium nitride-on-silicon (GaN-on-Si) e-mode power devices with a pGaN gate architecture showed no degradation after heavy ion and neutron irradiation.

IC Insights more than doubles its 2017 IC market growth forecast

IC Insights has raised its worldwide IC market growth forecast for 2017 to 11%—more than twice its original 5% outlook—based on data shown in the March Update to the 20th anniversary 2017 edition of The McClean Report. The revision was necessary due to a substantial upgrade to the 2017 growth rates forecast for the DRAM and NAND flash memory markets.



IC Insights currently expects DRAM sales to grow 39% and NAND flash sales to increase 25% this year, with upside potential from those forecasts. DRAM market growth is expected to be driven almost entirely by a huge 37% increase in the DRAM average selling price (ASP), as compared to 2016, when the DRAM ASP dropped by 12%. Moreover, NAND flash ASPs are forecast to rebound and jump 22% this year after falling by 1% last year.

Continued on page 9

Record spending for fab equipment expected in 2017 and 2018

SEMI announced updates to its World Fab Forecast report, revealing that fab equipment spending is expected to reach an industry all-time record – more than US$46 billion in 2017. The record is expected to be broken again in 2018, nearing the $50 billion mark. These record-busting years are part of three consecutive years of growth (2016, 2017 and 2018), which has not occurred since the mid-1990s. The report has been the industry's most trusted data source for 24 years, observing and analyzing spending, capacity, and technology changes for all front-end facilities worldwide.

SEMI's World Fab Forecast report (end of February 2017) provides updates to 282 facilities and lines equipping in 2017, 11 of which are expected to spend over $1 billion each in 2017. In 2018, SEMI's data reflect 270 fabs to equip, with 12 facilities spending over $1 billion each. The spending is mainly directed towards memory (3D NAND and DRAM), Foundry and MPU. Other strong product segments are Discretes (with LED and Power), Logic, MEMS (with MEMS/RF), and Analog/Mixed Signal.

SEMI (www.semi.org) forecasts that China will be third for regional spending in 2017, although China's annual growth is minimal in 2017 (about 1 percent), as many of the new fab projects are in the construction phase. China is busy constructing 14 new fabs in 2017 and these new fabs will be equipping in 2018. China's annual spending growth rate in 2018 will be over 55 percent (more than $10 billion), and ranking in second place for worldwide spending in 2018. In total for 2017, China is equipping 48 fabs, with equipment spending of $6.7 billion; looking ahead to 2018, SEMI predicts that 49 fabs to be equipped, with spending of about $10 billion. ◁▶

Micron to establish its site for DRAM in Taiwan

Micron Technology, Inc., a developer of advanced semiconductor systems, announced that on March 14 it successfully won the auction for Cando Corporation assets, which will be utilized in establishing a back-end site for Micron Taiwan. Micron has now completed the title acquisition process for the new site.

The acquisition includes the cleanroom and tools that are adjacent to Micron's existing Taichung fab, bringing the company's fabrication and back-end together in one location. The new site will be focused on establishing a centralized back-end operation.

"This marks a significant step in our plan to create a center of excellence for leading-edge DRAM in Taiwan," said Wayne Allan, VP, Global Manufacturing. "Bringing fabrication and back end together, all in one location, builds an efficient support structure for end-to-end manufacturing with quicker cycle times that benefit our business and customers."

The new back-end site is expected to begin production in August, and the new integrated center of excellence is expected to bring greater operational cost efficiency that will benefit Micron's DRAM business on a global scale. These cost efficiencies are part of the overall US$500 million of ongoing operational enhancement opportunities cited at the company's 2017 analyst conference.

The strategic acquisition, with a winning bid of US$89.2 million, also highlights Micron's goal to grow its presence in Taiwan – where it is the largest foreign employer and investor – from its current wafer manufacturing function to a broader center of expertise in the global memory industry. The back-end site will further enhance the company's strong presence on the island, which already includes 300mm wafer fabrication facilities in Taichung and Taoyuan, as well as sales and technical support offices in Taipei.

The back-end operation will be led by site director Mike Liang, who joined Micron in November 2016 with more than 35 years of experience in the semiconductor industry. Having previously served in leadership roles at Ti-Acer, KYEC and Amkor Taiwan, Liang brings significant expertise in both front-end wafer fabrication and back-end assembly and test manufacturing.

EUV lithography progress emphasized at SPIE Advanced Lithography

New extreme-ultraviolet (EUV) lithography equipment unveiled by ASML, announcement by Intel of eight EUV programs ready to be rolled out, and introduction by IMEC of the industry's first comprehensive solution for EUVL-enabled high-volume manufacturing systems were among highlights at SPIE Advanced Lithography 2017 in San Jose earlier this month.

Sponsored by SPIE, the international society for optics and photonics, the annual event is the year's primary forum for the industry. Attendance was up this year over last, with nearly 2,300 participating, and ran 26 February through 2 March.

Speakers from ASML, Intel, KLA-Tencor, JSR Corp, IMEC, Samsung, and other organizations emphasized progress being made toward manufacturing computer chips using sub-10nm node lithography, sparking much discussion about when, where, and how — plus the occasional if — the next generation of lithography tools will enable high-volume and high-throughput manufacturing at an EUV wavelength of about 13.5nm. Presentation recordings are viewable on the SPIE Newsroom on SPIE.org.

Product System Engineer Mark van de Kerkhof reported on ASML's NXE:3400B EUV scanner, which enables sub-10nm-node lithography — ASML's first scanner that can produce 125 wafers/hour, the throughput rate needed in production fabs.

With ever-smaller feature sizes being designed, mask makers must continuously advance their technologies as EUV sources and other lithography tools advance, noted plenary speaker Frank Abboud, Vice President of Technology and Manufacturing Group at Intel, and General Manager, Intel Mask Operation.

"Almost every module in the mask shop is touched," he said, including blank preparation, fiducial mark patterning, device patterning, black-border patterning, and metrology/characterization."

Plenary speaker Ben Tsai, Chief Technology Officer and Executive Vice President of Corporate Alliances at KLA-Tencor, spoke on the return on investment of defect detection.

Inspection and metrology can involve 1,000 process steps for an advanced graphics processing unit, each requiring extremely high accuracy, he noted. In such a process model, if each step was 99.5% perfect, fewer than 1% of manufactured devices would work, illustrating the importance of investment in inspection and metrology to identify and resolve essentially all defects.

Starting with a vision of drivers for next-generation computing such as artificial intelligence (AI) and the computational power required, Nobu Koshiba, President and CEO of JSR Corporation, pointed out the extent to which the information explosion trending for years is continuing, with estimated data traffic in 2020 being 7× greater than in 2015.

The growth is stimulating AI advances, as are autonomous driving, precision medicine, genomic science, and cognitive computing, he said.

In a keynote talk, Philippe Leray, IMEC Group Leader of Advanced Metrology, described development of the first comprehensive solution for EUVL enablement in high-volume manufacturing. The approach serves as a basis for industry requirements for power, performance, area and cost, and includes proposals for design rules, masks, photoresists, etching, and metrology and an extensive process variation assessment, Leray said.

Donis Flagello, President, CEO, and COO of Nikon Research Corporation of America (NRCA), was presented with the 2017 Frits Zernike Award for Microlithography.

Semiconductor pioneer Burn Lin (National Tsin Hua University) was honored on the 30th anniversary of the Optical Microlithography conference in recognition of his serving as the first chair of the conference in 1988, and of his outstanding contributions to the lithography community. Lin was the founding editor of the SPIE Journal of Microlithography, Microfabrication, and Microsystems (JM3).

Six new Fellows of SPIE were recognized: Emily Gallagher (IMEC), Yuri Granik (Mentor Graphics), Qinghuang Lin (IBM Thomas J. Watson Research Center), David Pan (University of Texas, Austin), Mark Phillips (Intel Corp.), and James Thackarey (Dow Electronic Materials).

Bruce Smith, Rochester Institute of Technology, served as symposium chair, and Will Conley of Cymer, an ASML company, was symposium co-chair.

SPIE Advanced Lithography included seven conferences on lithographic topics, along with technical courses taught by experts from industry and academia, and a two-day exhibition. ◆

IC Insights, continued from page 6

The DRAM market started 2017 the way it ended 2016—with strong gains in DRAM ASP. In April 2016, the DRAM ASP was $2.41 but rapidly increased to $3.60 in January 2017, a 49% jump. A pickup in DRAM demand from PC suppliers during the second half of 2016 caused a significant spike in the ASP of PC DRAM. Currently, strengthening ASPs are also evident in the mobile DRAM market segment.

With total DRAM bit volume demand expected to increase by 30% this year and DRAM bit volume production capacity forecast to increase by 20%, IC Insights believes that quarterly DRAM ASPs could still surprise on the upside in 2017. Furthermore, DRAM output is also being slowed, at least temporarily, by the ongoing transition of DRAM production to ≤20nm feature sizes by the major DRAM producers this year.

At $57.3 billion, the DRAM market is forecast to be by far the largest IC product category in 2017, exceeding the expected MPU market for standard PCs and servers ($47.1 billion) by $10.2 billion this year. Figure 1 shows that the DRAM market has been both a significant tailwind (i.e., positive influence) and headwind (i.e., negative influence) on total worldwide IC market growth in three out of the past four years.

Spurred by a 12% decline in the DRAM ASP in 2016, the DRAM market slumped 8% last year. The DRAM segment became a headwind to worldwide IC market growth in 2016 instead of the tailwind it had been in 2013 and 2014. As shown, the DRAM market shaved two percentage points off of total IC industry growth last year. In contrast, the DRAM segment is forecast to have a positive impact of four percentage points on total IC market growth this year. It is interesting to note that the total IC market growth rate forecast for 2017, when excluding the DRAM and NAND flash markets, would be only 4%, about one-third of the current worldwide IC market growth rate forecast including these memory devices.

The March Update to the 2017 edition of The McClean Report further describes IC Insights' IC market forecast revision, updates its 2017-2021 semiconductor capital spending forecast, and shows the final 2016 top 10 OSAT company ranking. ◆

New business models emerging

PHIL GARROU,
Contributing Editor

Jim Walker, who retired from Gartner and is now consulting as World Level Packaging Concepts, gave a plenary talk at the recent IMAPS Device Packaging Conference in Scottsdale on the state of the semiconductor industry which contained some interesting perspectives on emerging new business models.

While Gartner 2020 projections show wireless and computer will still account for ~ 50% of the overall market activity, automotive, storage and industrial will show significant growth (7-9%) between now and then and account for ~ 30% of the total market (combined).

Gartner expects consolidation to continue "...with semi companies sitting on $135B in cash and profit margins decreasing there is a need to diversify into new markets" with specifics including:

- IoT related M&A activity will drive consolidation in MCU, analog and sensor technologies.
- Companies will initiate sale of unprofitable divisions and product lines to prepare themselves for M&A (i.e., make themselves more attractive to be acquired).
- China will continue to buy or invest in U.S. and European companies, even as governments impose restrictions.

Gartner sees the industries maturation resulting in traditional business models changes. The traditional semiconductor ecosystem is shown in **FIGURE 1**.

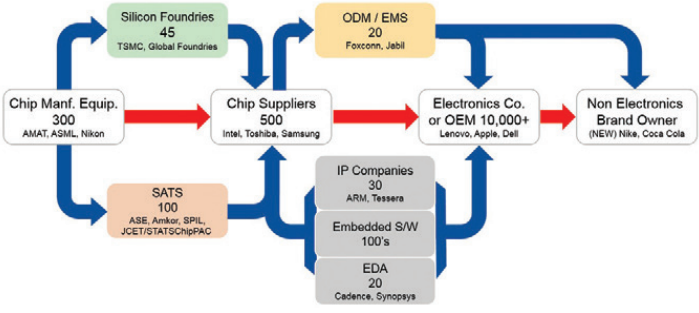


FIGURE 1. The semiconductor ecosystem.

Gartner reports that a relatively new problem for some OEMs and Electronics Brands is that they are being bypassed by a direct relationship between the ODM/EMS company and a non-electronics brand owner buyer who could be in any industry. This model emerged with Operator branded handsets, although those were recognizable as say Nokia or Motorola. This (Brand) Direct to ODM/EMS business model is good for chip suppliers but bad for traditional electronics companies (**FIGURE 2**).

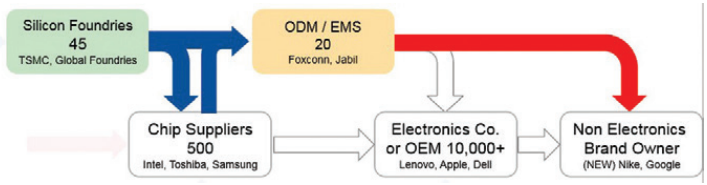


FIGURE 2. The Brand Direct model.

Another relatively new problem for some chip companies now is that they are being bypassed by a direct relationship between the foundry and the EMS/ODM company and the OEM –- the OEM Direct model. These could be chips designed by Apple or Facebook (for example) and manufactured by TSMC (**FIGURE 3**).

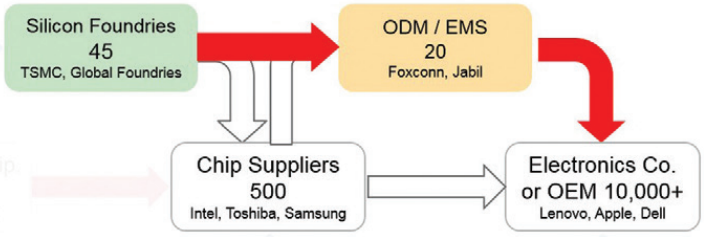
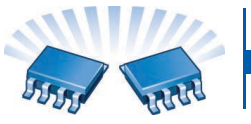


FIGURE 3. The OEM Direct model.

Walker specifically suggests we keep an eye on Hon Hai/Foxconn which appears to be building strong and broad manufacturing capabilities through acquisitions such as Japan's Sharp (Feb 2016) and a bid on the Toshiba memory business (2017).

Packaging is currently ~17% ($53B) of the $265B electronics market. By 2020, 55% of all packaging is expected to be done at OSATS with foundries like TSMC (and maybe others soon) becoming competitors with their own wafer based packaging offerings like InFO. Walker sees a bright future for IoT packaging, but cautions that it is composed of many small to mid-sized applications, not one big one like the smart phone, and thus will require many custom packaging solutions. ◆

Packaging



Silicon photonics advances

ED KORCZYNSKI,
Sr. Technical Editor

With rapidly increasing use of "cloud" client:server computing there is motivation to find cost-savings in the cloud hardware, which leads to R&D of improved photonics chips. Silicon photonics chips could reduce hardware costs compared to existing solutions based on indium-phosphide (InP) compound semiconductors, but only with improved devices and integration schemes. Now MIT researchers working within the US AIM Photonics program have shown important new silicon photonics properties. Meanwhile, GlobalFoundries has found a way to allow for automated passive alignment of optical fibers to silicon chips, and makes chips on 300-mm silicon wafers for improved performance at lower cost.

In a recent issue of Nature Photonics, MIT researchers present "Electric field-induced second-order nonlinear optical effects in silicon waveguides." They also report prototypes of two different silicon devices that exploit those nonlinearities: a modulator, which encodes data onto an optical beam, and a frequency doubler, a component vital to the development of lasers that can be precisely tuned to a range of different frequencies.

This work happened within the American Institute for Manufacturing Integrated Photonics (AIM Photonics) program, which brought government, industry, and academia together in R&D of photonics to better position the U.S. relative to global competition. Federal funding of $110 million was combined with some $500 million from AIM Photonics' consortium of state and local governments, manufacturing firms, universities, community colleges, and nonprofit organizations across the country. Michael Watts, an associate professor of electrical engineering and computer science at MIT, has led the technological innovation in silicon photonics.

"Now you can build a phase modulator that is not dependent on the free-carrier effect in silicon," says Michael Watts in an online interview. "The benefit there is that the free-carrier effect in silicon always has a phase and amplitude coupling. So whenever you change the carrier concentration, you're changing both the phase and the amplitude of the wave that's passing through it. With second-order nonlinearity, you break that coupling, so you can have a pure phase modulator. That's important for a lot of applications."

The frequency doubler uses regions of p- and n-doped silicon arranged in regularly spaced bands perpendicular to an undoped silicon waveguide. The space between bands is tuned to a specific wavelength of light, such that a voltage across them doubles the frequency of the optical signal passing. Frequency doublers can be used as precise on-chip optical clocks and amplifiers, and as terahertz radiation sources for security applications.

At the start of the AIM Photonics program in 2015, MIT researchers had demonstrated light detectors built from efficient ring resonators that they could reduce the energy cost of transmitting a bit of information down to about a picojoule, or one-tenth of what all-electronic chips require. Jagdeep Shah, a researcher at the U.S. Department of Defense's Institute for Defense Analyses who initiated the program that sponsored the work said, "I think that the GlobalFoundries process was an industry-standard 45-nanometer design-rule process."

GlobalFoundries has found a way to automatically align twelve optical fibers to a silicon chip while the fibers are dark. Because the micron-scale fibers must be aligned with nanometer precision, default industry standard has been to expensively align actively lit fibers. Leveraging the company's work for Micro-Electro-Mechanical Sensors (MEMS) customers, GlobalFoundries uses an automated pick-and-place tool to push ribbons of multiple fibers into MEMS groves for the alignment. Ted Letavic, Global Foundries' senior fellow, said the edge coupling process was in production for a telecommunications application. Silicon photonics may find first applications for very high bandwidth, mid- to long-distance transmission (30 meters to 80 kilometers), where spectral efficiency is the key driver according to Letavic.

GobalFoundries has now transferred its monolithic process from 200mm to 300mm-diameter silicon wafers, to achieve both cost-reduction and improved device performance. The 300mm fab lines feature higher-N.A. immersion lithography tools which provide better overlay and line width roughness (LWR). Because the of the extreme sensitivity of optical coupling to the physical geometry of light-guides, improving the patterning fidelity by nanometers can reduce transmission losses by 3X. ◁▶

Semiconductors

FD-SOI: How a pioneering technology entered mainstream markets

MANUEL SELLIER, *Soitec, Bernin (Grenoble), France*

With its unique characteristics, FD-SOI is generating increasingly strong interest from major players in the semiconductor ecosystem for a very wide range of markets.

Fully depleted silicon-on-insulator or FD-SOI is the only technology bringing together two substantial characteristics of CMOS transistors: 2D planar transistor structure and fully depleted operation. It relies on a unique substrate whose layer thicknesses are controlled at the atomic scale. FD-SOI offers remarkable transistor performance with one of the best power, performance, area and cost tradeoffs (PPAC) among all advanced CMOS technologies. In addition, FD-SOI has numerous other unique advantages including back bias ability, very good transistor matching, near threshold supply capability, ultra-low sensitivity to radiation and very high intrinsic transistor speed, which allows it to handle mmWave frequencies.

All these key features are progressively making FD-SOI a de facto technology for many applications including entry-level application processors for smartphones, system-on-chip (SoC) devices for autonomous driving and IoT, and all mmWave applications such as 5G transceivers and radar systems for automotive electronics.

FD-SOI technology is supported by multiple foundries and IDMs with full technology offerings now available for the 28nm and 22nm nodes and emerging for the 65nm and 12nm nodes. With this global ecosystem in place, FD-SOI is ready for applications development for diversified markets.

There are several striking characteristics of FD-SOI substrates that give this technology unique advantages. This article summarizes the latest advances and the various elements of the global ecosystem that support widespread implementation of FD-SOI as well as the applications that most benefit from it.

The heart of FD-SOI

Everything in FD-SOI technology starts with the substrate. The substrate directly defines the transistor architecture, as shown in **FIGURE 1**. To allow the fully depleted operation of transistors, the thickness of the top silicon layer defining the device channel represents a real challenge, with the thickness target typically around 60 Å or 11 atomic layers. Given the consumption of silicon material during device fabrication, a 120 Å incoming top silicon specification is usually required by foundries. Uniformity is another very challenging specification needed to keep transistor variability as low as possible. Uniformity of +/-5 Å or 1 atomic layer is typically considered essential. Buried oxide (BOx) thickness also must be very thin - around 20nm - to maximize electrostatic control in the transistor channel due to the ground plane effect.

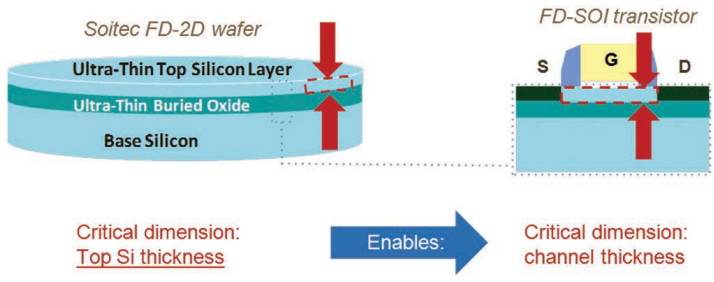


FIGURE 1. Transistor channel thickness is directly linked to top silicon SOI layer definition.

MANUEL SELLIER *is a product marketing manager at Soitec, Bernin (Grenoble), France*

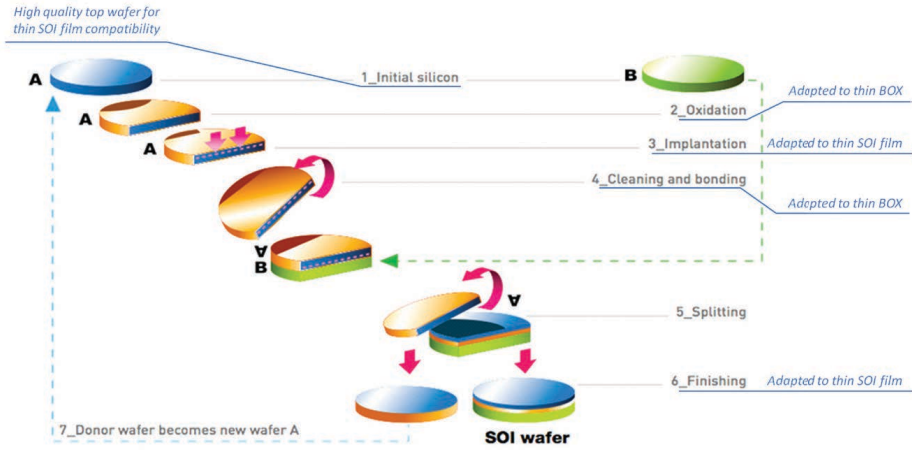


FIGURE 2. Smart Cut process and its adaptation to FD-SOI.

Manufacturing a 300mm piece of crystalline silicon with a thickness specification as low as 11 +/-1 atomic layers is understandably difficult. Ten years ago, it sounded unachievable so people studied other paths to enable fully depleted transistors [1]. But it is now possible.

Fabrication relies on the well-known Smart Cut TM process (**FIGURE 2**). As shown, wafer A first undergoes an oxidation step followed by high-dose ion implantation, creating a weakened layer just beneath the surface. After careful cleaning steps, wafer A is bonded to wafer B through molecular-bonding technology. Splitting is then induced at the precise location of the weakened zone of wafer A. Finally, the formed SOI wafer is subjected to other smoothing process steps to achieve the targeted thickness specification. It is noteworthy that high-quality wafer A can be recycled for further reuse, making Smart Cut the most cost-effective solution for SOI manufacturing.

The FD-SOI substrate-manufacturing process is now fully mature. In particular, thickness uniformity is very well controlled at all levels, from transistor to wafer, as shown in **FIGURE 3**. This ensures a very low level of transistor variability.

When less is more

The way of getting more performance out of silicon below 28nm node adds more complexity to the

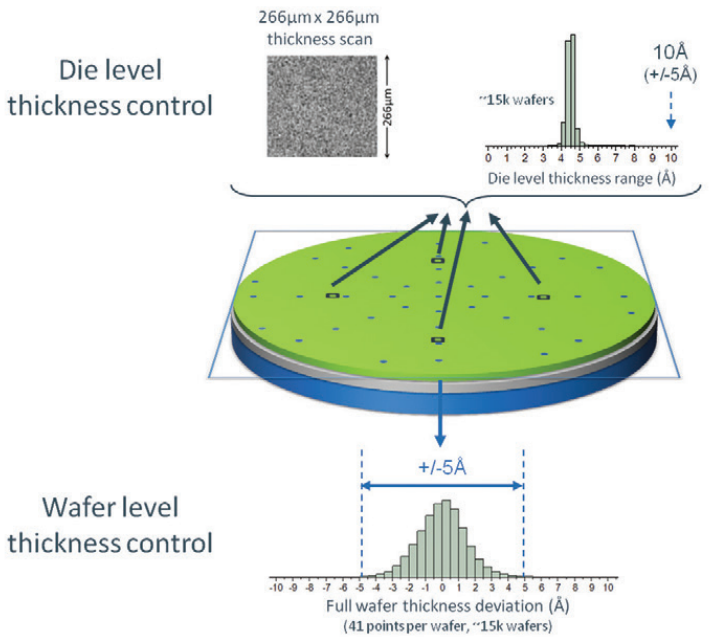


FIGURE 3. FD-SOI thickness is controlled at all levels - from die to wafer.

manufacturing process. Consequently, as illustrated in **FIGURE 4**, the smaller nodes get, the greater number of masks are needed to create chips. This increases manufacturing costs as well as other non-recurring engineering costs including design flow, design verification, mask sets and more.

On the other hand, FD-SOI is a simple technology from a manufacturing standpoint. In fact, it offers more performance while decreasing the manufacturing process complexity. Most of the channel engineering work is actually done directly at the substrate level, making FD-SOI easier to implement than bulk silicon, as major foundries have reported [2] [3].

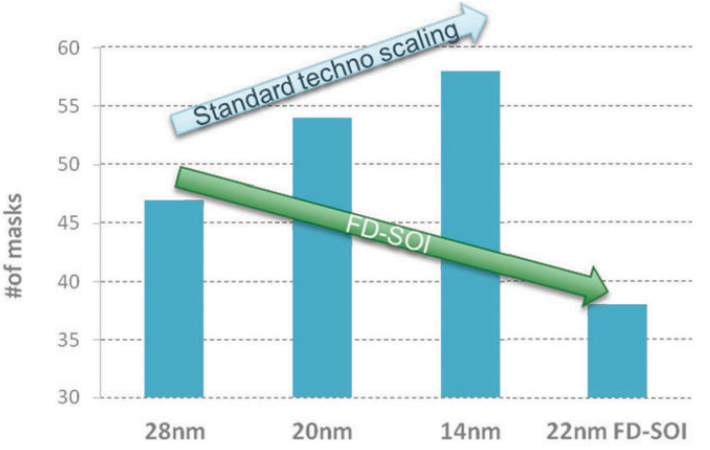


FIGURE 4. Number of masks required per technology node (from [2]).

The next level of transistor performance

In addition to simpler manufacturing, FD-SOI offers other substantial benefits, as depicted below and summarized in **FIGURE 5**.

1. Better design flexibility through body bias

The thin BOx of FD-SOI not only enhances electrostatic control of the channel, but also makes it possible to completely tune the threshold voltage through back biasing. All the complex Vth adjustment techniques through channel doping can be avoided. Low, mid-range and high Vth can be achieved simply through back-gate polarization. The thin BOx behaves like a real second gate and, most importantly, it can be used dynamically. This means that the same functional block can operate under high or low power, on demand. Back bias potential is huge: selective body bias for critical path improvements [4], process variation compensation [5] and reliability drift compensation [6]. Full back biasing is a very unique feature, only achievable with SOI on thin BOx technology.

2. Power-performance-area-cost tradeoff: Best PPAC of all planar technologies

Thanks to simpler manufacturing, better control of random mismatch, minimizing of junction leakage and capacitances, enhanced electrostatic control through fully depleted transistor operation and the possibility of tuning body bias, FD-SOI technology presents the best power-performance-area-cost tradeoff (PPAC) among all planar technologies.

3. Ultra-low power through near-threshold supply voltage

Almost all CMOS technologies achieve their best energy efficiency – i.e., the lowest amount of energy per function, regardless of the frequency – at around 0.4 V supply voltage, often referred to as Vdd [7]. At this level of supply voltage, variability management is a real challenge. Thanks to body bias and to its intrinsic low-variability characteristics, FD-SOI can achieve very low supply voltages. More generally, the ability to lower the supply voltage, although not necessarily as low as 0.4 V, is a real challenge in many applications in which power is a greater challenge than performance. Given the fact that dynamic power scales with Vdd^2, a technology like FD-SOI that is capable of strong power savings through tremendous supply voltage reduction presents a unique advantage.

4. Best RF-CMOS technology with almost 2 times maximum frequency over 3D devices

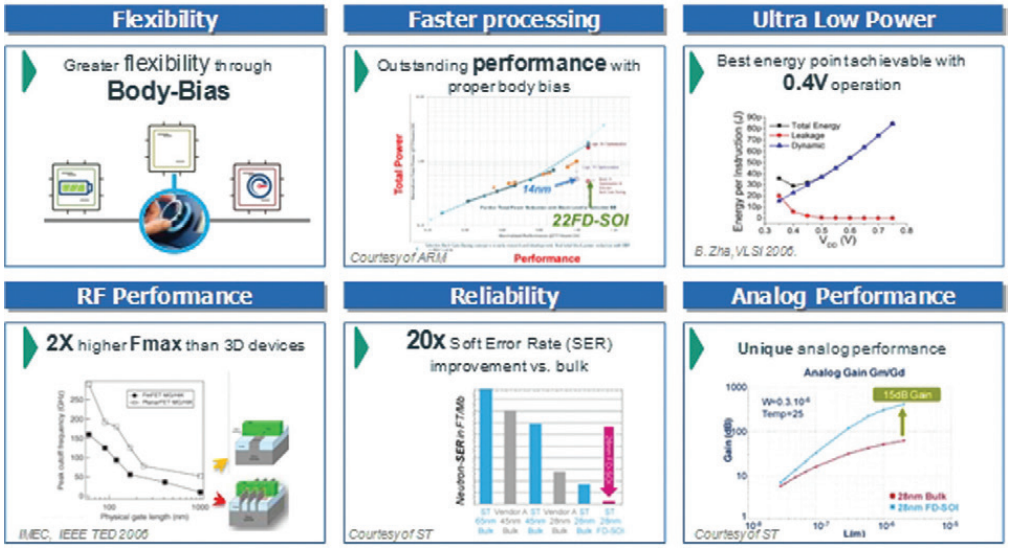


FIGURE 5. Benefits of using FD-SO [4] [7] [9] [10].

Integrating as many analog/RF functions as possible into a single RF-CMOS silicon platform is becoming an increasingly important issue in many markets for obvious cost and power reasons. However, one limitation of RF-CMOS platforms is the limited ability to increase frequency, especially in the mmWave spectrum (30 GHz and above). This is a bigger issue with 3D devices such as FinFETs, which must carry very strong parasitic capacitances due to their 3D structures [8]. As a result, SiGe-Bipolar platforms are often used for this frequency range. FD-SOI is a planar technology and, as such, it should not suffer from the limitations of 3D devices. Ft/Fmax in the range of 325-350 GHz have been reported [3], allowing full usage of the mmWave spectrum up to 100 GHz and giving FD-SOI RF-CMOS platforms a bright future in many applications.

5. Enhanced reliability

Low sensitivity to high-energy particles is another key characteristic of FD-SOI. High-energy particles can interact with silicon and generate a significant amount of charges capable of flipping transistor logic state, thus increasing the soft errors rate (SER). FD-SOI devices are completely isolated from the substrate due to the BOx layer. This means that any charge generated in the substrate is unlikely to modify the device logic state. In short, FD-SOI is much less sensitive to SER [9]. This has very important consequences for safety-critical devices such as autonomous car systems.

6. Outstanding analog transistor characteristics

Often, analog designers have to make their designs work with more and more degraded transistors as technology shrinks. Meeting speed, noise, power, leakage and variability requirements is increasingly challenging. By providing a transistor with improved matching, gain and parasitic, FD-SOI can greatly simplify device design [10].Moreover, the back bias has potential for the design of many new analog structures [11].

FD-SOI's growing use at foundries

Some of the most pioneering work with FD-SOI has been done at semiconductor foundries around the world.

STMicroelectronics adopted FD-SOI technology in 2012 [12] and started several projects. The company demonstrated an ARM-based application processor for smartphones with 3 GHz+ operating frequency on 28nm FD-SOI

[13]. The technology is now used at STMicroelectronics for many diversified markets [14] [15].

In 2014, Samsung announced the adoption of 28nm FD-SOI technology for its foundry division [15]. Mass production maturity was reached in 2016 [2], and the first product release was announced recently [16] [17].

In 2015, GLOBALFOUNDRIES developed a 22nm FD-SOI technology called 22FDX [18], which it positioned as offering the best performance/cost ratio. This FD-SOI technology platform achieved performance close to 16nm/14nm FinFET at a cost similar to 28nm bulk silicon [19]. The first commercial product was announced in February 2017 by GLOBALFOUNDRIES and Dream Chip Technologies [20]. GLOBALFOUNDRIES' technology is now almost fully qualified, with volume ramp-up expected this year.

In Asia, the Chinese foundry Huali has announced its intention to include 22nm FD-SOI technology in its fab2 plan [21], offering the Chinese market greater access to FD-SOI technology.

In Japan, Renesas' experience with FD-SOI includes work on a very low-power FD-SOI technology called silicon-on-thin-BOx (SOTB), which targets low-power MCU markets. This technology has been supported by the LEAP initiative (Low-Power Electronics Association and Project) and is now available in 65nm. Renesas has reported very low-power consumption with this platform, as small as a tenth of that achieved using bulk silicon.

IP/CAD status and roadmap

The design ecosystem is well established for 28nm FD-SOI with complete libraries and foundation IP and growing at a fast pace for 22nm technology. EDA companies are on board and developing IP ported to FD-SOI.

In September 2016, GLOBALFOUNDRIES announced a new partner program called FDXcelerator™ to facilitate 22FDX SoC design and reduce time to market for its customers including Synopsys, Cadence, INVECAS, VeriSilicon, CEA-Leti, Dream Chip and Encore Semi [22]. In December 2016, the foundry announced the addition of eight new partners to its growing FDXcelerator program including Advanced Semiconductor Engineering (ASE Group), Amkor Technology, Infosys, Mentor Graphics, Rambus, Sasken, Sonics and QuickLogic [23].

As for the technology roadmap, FD-SOI is available on a wide range of technology nodes from 65nm to 12nm with visibility down to 7nm. Building on the success of its 22FDX offering, in 2016 GLOBALFOUNDRIES unveiled a new 12nm FD-SOI semiconductor technology called 12FDX [24]. Staying with fully depleted planar processing allows the foundry to take advantage of the low parasitic capacitance, avoid the complex lithography steps required by equivalent 3D transistors, and leverage back biasing to boost transistor performance, especially at low supply voltages. Customer product tape-outs are expected to begin by the end of 2017.

Leti, which pioneered FD-SOI development 15 years ago, worked with GLOBALFOUNDRIES on the 22FDX and 12FDX platforms. The organization recently developed test devices on 10nm FD-SOI technology and produced models for 10nm and 7nm on FD-SOI. Leti strongly believes that FD-SOI can be scaled down to 7nm.

Both Samsung and GLOBALFOUNDRIES plan to have embedded non-volatile memory integrated into their FD-SOI technology platforms by 2018 [2] [3].

FD-SOI traction in power and analog/RF integration

Thanks to the growing maturity of the FD-SOI ecosystem, there is now a wide range of applications seeing strong differentiation possibilities through FD-SOI. These include single-chip solutions for entry-level mobile communications, general purpose application processors, image signal processors, SoC for set-top boxes, embedded computer vision, microcontrollers, mixed-signal applications such as transceivers, GPS/satellite receivers, wi-fi/BT combos and mmWave radar systems.

For all these applications, power budget is typically very limited and must be balanced with performance targets. A good example of this can be found in embedded computing applications such as ADAS, where designers must constantly find compromises to achieve the required performance with a very limited power budget, typically around 3 W. For all embedded computing applications, FD-SOI - and its ability to run on very low supply voltages - is gaining momentum as the reference technology.

In addition, RF/analog integration is often key for these applications. Having best-in-class RF-CMOS technology available on the same silicon die as the digital parts is a unique advantage of FD-SOI. It opens up possibilities for single-chip solutions covering a wide range of functions. This is particularly advantageous in entry-level markets such as low-end mobile, where the price pressure is so great that integration must be pushed to its limits, or in mmWave applications including radar and 5G transceivers,

FIGURE 6. Huami Amazfit smartwatch with FD-SOI-based GPS inside.

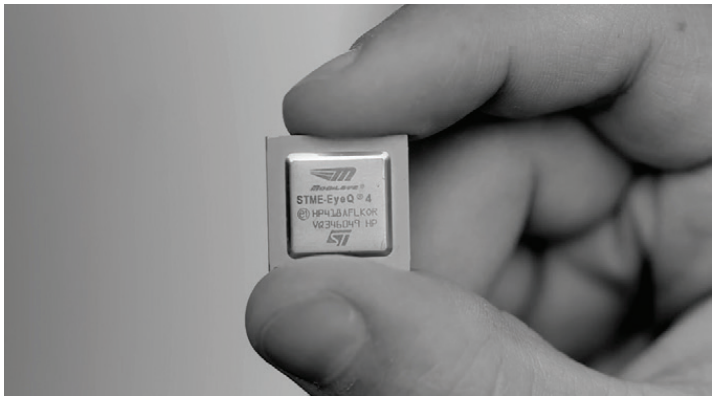


FIGURE 7. Mobileye EyeQ4 chip dedicated to ADAS autonomous level3 applications (http://www.mobileye.com/).

where the mmWave RF functions can be integrated on the same die as the computing functions.

A new wave of ground-breaking products

The list of FD-SOI-based products is increasing at a very fast pace, with multiple product announcements over the past months.

In September 2016, Huami (a Xiaomi partner company) introduced a new fitness smartwatch that includes a FD-SOI-based global positioning system (GPS) chip demonstrating record energy efficiency (**FIGURE 6**) [25]. The chip allows the watch to reach an unsurpassed battery life of 35 hours with the GPS turned on, which represents two to five times more than today's similar devices. The chip, revealed in February 2016 at the International Solid-State Circuits Conference (ISSCC) in San Francisco [27], dramatically lowers power usage and opens the door for always-on GPS applications in smartwatches, smartphones, drones and a large number of devices for the IoT.

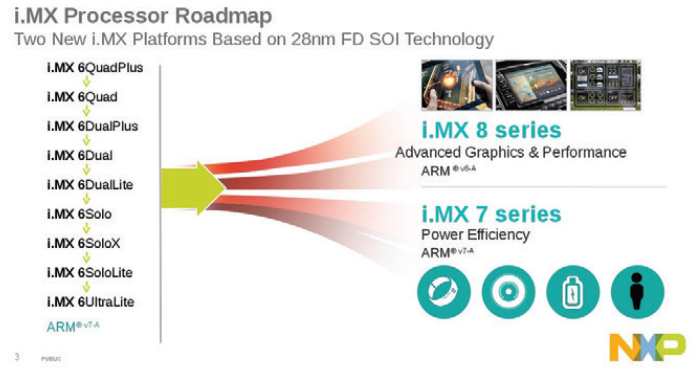


FIGURE 8. i.MX processor roadmap (courtesy of NXP).

Also in 2016, Mobileye posted on its website that its next EyeQ4 product family dedicated to level3 autonomous driving will be based on FD-SOI technology [26] (**FIGURE 7**).

In March 2017, NXP released two general-purpose processor families (i.MX7ULP and i.M8X) [16] [17] based on Samsung's 28FDS FD-SOI technology for ultra-low

power consumption and rich graphics in battery-powered applications (see NXP roadmap **FIGURE 8**). NXP reported a deep-sleep suspended power consumption of 15 µW or less for its i.MX7ULP product, 17 times less in comparison to previous low-power bulk devices, while the dynamic power efficiency improved by 50 percent. This high-performance, low-power solution is optimized for customers developing IoT, home control, wearable and other applications that spend a significant amount of time in standby mode with short bursts of performance-intense activity that require exceptional graphics processing.

In March 2017, Eutelsat Communications and STMicroelectronics announced a new-generation SoC for interactive applications that represents a step down in the overall cost of interactive satellite terminals while reducing power consumption [14].

FIGURE 9. Dream Chip Technologies' first 22nm FD-SOI product dedicated to ADAS (courtesy of Dream Chip)

On the 22nm side, Dream Chip announced the industry's first 22nm FD-SOI product for a new ADAS SoC for automotive computer-vision applications [20]. The SoC device (**FIGURE 9**) offers high-performance image acquisition and processing capabilities and supports convolutional neural network (CNN) vision workloads to meet the demand for complex automotive object detection and processing.

The 22nm FD-SOI product portfolio is expected to grow significantly in the coming year as the technology ramps up.

Adding fabs to meet overall FD-SOI demand

Faced with the growing interest of FD-SOI, particularly in China, foundries are organizing themselves to build up enough production capacity. In February 2017, GLOBALFOUNDRIES announced plans to expand the capacity of its Fab 1 facility in Dresden by 40 percent by 2020. Dresden will continue to be the center for FDX technology development [27].

In China, GLOBALFOUNDRIES and the Chengdu municipality have announced a partnership to build a fab. The partners plan to establish a 300mm fab to support the growth of the Chinese semiconductor market and to meet accelerating global customer demand for 22FDX [27]. The fab will begin producing mainstream process technologies in 2018 and then focus on manufacturing GLOBALFOUNDRIES' commercially available 22FDX process technology, with volume production expected to start in 2019.

With these two announcements, GLOBALFOUNDRIES will have a future production capacity of more than 2 million FD-SOI wafers per year.

Regarding FD-SOI substrate manufacturing capacity, Soitec owns one 300mm fab in France and has another one in Singapore (currently in standby mode) with a combined global capacity of 1.5 million wafers per year (for manufacturing FD-SOI and other emerging SOI products). The company has plans to go beyond that to meet additional customer demand.

Conclusion

Growing interest in FD-SOI reflects today's new paradigm for semiconductor technologies. Customers are demanding for more computing capability with drastically reduced power consumption, enabled by enhanced analog/RF integration. With its unique characteristics, FD-SOI is generating increasingly strong interest from major players in the semiconductor ecosystem for a very wide range of markets, especially for embedded computing applications. FD-SOI is now a mainstream technology, which device designers are leveraging for key competitive advantages.

Acknowledgements

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Deep learning could boost yields, increase revenues

DAVE LAMMERS, *Contributing Editor*

Deep learning is "a shiny new hammer" that chip industry may figure out how to use.

While it is still early days for deep-learning techniques, the semiconductor industry may benefit from the advances in neural networks, according to analysts and industry executives.

First, the design and manufacturing of advanced ICs can become more efficient by deploying neural networks trained to analyze data, though labelling and classifying that data remains a major challenge. Also, demand will be spurred by the inference engines used in smartphones, autos, drones, robots and other systems, while the processors needed to train neural networks will re-energize demand for high-performance systems.

Abel Brown, senior systems architect at Nvidia, said until the 2010-2012 time frame, neural networks "didn't have enough data." Then, a "big bang" occurred when computing power multiplied and very large labelled data sets grew at Amazon, Google, and elsewhere. The trifecta was complete with advances in neural network techniques for image, video, and real-time voice recognition, among others.

During the training process, Brown noted, neural networks "figure out the important parts of the data" and then "converge to a set of significant features and parameters."

Chris Rowen, Cognite Ventures

Chris Rowen, who recently started Cognite Ventures to advise deep-learning startups, said he is "becoming aware of a lot more interest from the EDA industry" in deep learning techniques, adding that "problems in manufacturing also are very suitable" to the approach.

For the semiconductor industry, Rowen said, deep-learning techniques are akin to "a shiny new hammer" that companies are still trying to figure out how to put to good use. But since yield questions are so important, and the causes of defects are often so hard to pinpoint, deep learning is an attractive approach to semiconductor companies.

"When you have masses of data, and you know what the outcome is but have no clear idea of what the causality is, (deep learning) can bring a complex model of causality that is very hard to do with manual methods," said Rowen, an IEEE fellow who earlier was the CEO of Tensilica Inc.

The magic of deep learning, Rowen said, is that the learning process is highly automated and "doesn't require a fab expert to look at the particular defect patterns."

"It really is a rather brute force, naïve method. You don't really know what the constituent patterns are that lead to these particular failures. But if you have enough examples that relate inputs to outputs, to defects or to failures, then you can use deep learning."

Juan Rey, senior director of engineering at Mentor Graphics, said Mentor engineers have started investigating deep-learning techniques which could improve models of the lithography process steps, a complex issue that Rey said "is an area where deep neural networks and machine learning seem to be able to help."

In the lithography process "we need to create an approximate model of what needs to be analyzed. For example, for photolithography specifically, there is the transition between dark and clear areas, where the slope of intensity for that transition zone plays a very clear role in the physics of the problem being solved. The problem tends to be that the design, the exact formulation, cannot be used in every space, and we are limited by the computational resources. We need to rely on a few discrete measurements, perhaps a few tens of thousands, maybe more, but it still is a discrete data set, and we don't know if that is enough to cover all the cases when we model the full chip," he said.

Juan Rey, Mentor Graphics

"Where we see an opportunity for deep learning is to try to do an interpretation for that problem, given that an

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exhaustive analysis is impossible. Using these new types of algorithms, we may be able to move from a problem that is continuous to a problem with a discrete data set."

Mentor seeks to cooperate with academia and with research consortia such as IMEC. "We want to find the right research projects to sponsor between our research teams and academic teams. We hope that we can get better results with these new types of algorithms, and in the longer term with the new hardware that is being developed," Rey said.

Many companies are developing specialized processors to run machine-learning algorithms, including non-Von Neumann, asynchronous architectures, which could offer several orders of magnitude less power consumption. "We are paying a lot of attention to the research, and would like to use some of these chips to solve some of the problems that the industry has, problems that are not very well served right now," Rey said.

While power savings can still be gained with synchronous architectures, Rey said brain-inspired projects such as Qualcomm's Zeroth processor, or the use of memristors being developed at H-P Labs, may be able to deliver significant power savings. "These are all worth paying attention to. It is my feeling that different architectures may be needed to deal with unstructured data. Otherwise, total power consumption is going through the roof. For unstructured data, these types of problem can be dealt with much better with neuromorphic computers."

The use of deep learning techniques is moving beyond the biggest players, such as Google, Amazon (**FIGURE 1**), and the like. Just as various system integrators package the open source modules of the Hadoop data base technology into a more-secure offering, several system integrators are offering workstations packaged with the appropriate deep-learning tools.

Robert Stober, director of systems engineering at Bright Computing, bundles AI software and tools with hardware based on Nvidia or Intel processors. "Our mission statement is to deploy deep learning packages, infrastructure, and clusters, so there is no more digging around for weeks and weeks by your expensive data scientists," Stober said.

Deep learning is driving new the need for new types of processors as well as high-speed interconnects. Tim Miller, senior vice president at One Stop Systems, said that training the neural networks used in deep learning is an ideal task for GPUs because they can perform parallel

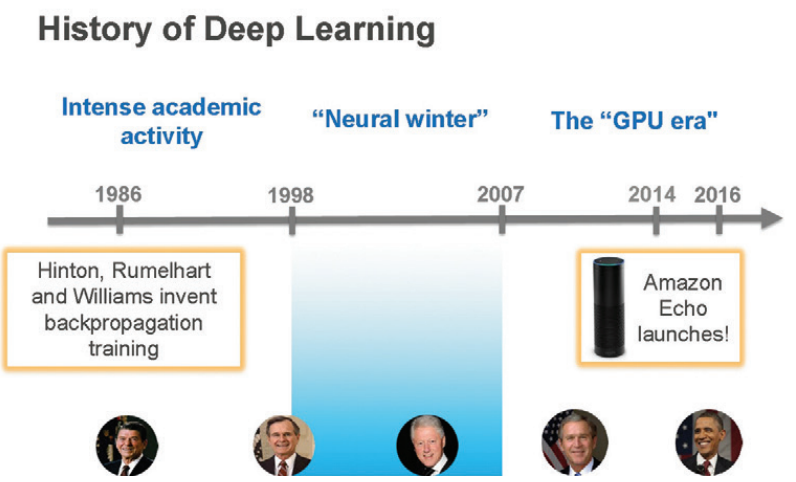


FIGURE 1. Deep learning has evolved to play a role in speech recognition used in Amazon's Echo. Source: Amazon

calculations, sharply reducing the training time. However, GPUs often are large and require cooling, which most systems are not equipped to handle.

David Kanter, principal consultant at Real World Technologies, said "as I look at what's driving the industry, it's about convolutional neural networks, and using general-purpose hardware to do this is not the most efficient thing."

However, research efforts focused on using new materials or futuristic architectures may over-complicate the situation for data scientists outside of the research arena. At the International Electron Devices Meeting (IEDM 2017), several research managers discussed using spin torque magnetic (STT-MRAM) technology, or resistive RAMs (ReRAM), to create dense, power-efficient networks of artificial neurons.

While those efforts are worthwhile from a research standpoint, Kanter said "when proving a new technology, you want to minimize the situation, and if you change the software architecture of neural networks, that is asking a lot of programmers, to adopt a different programming method."

While Nvidia, Intel, and others battle it out at the high end for the processors used in training the neural network, the inference engines which use the results of that training must be less expensive and consume far less power.

Kanter said "today, most inference processing is done on general-purpose CPUs. It does not require a GPU. Most people I know say Google does not use a GPU. Since the (inference processing) workload load looks like the processing of DSP algorithms, it can be done with special-

purpose cores from Tensilica (now part of Cadence) or ARC (now part of Synopsys). That is way better than any GPU," Kanter said.

Rowen was asked if the end-node inference engine will blossom into large volumes. "I would emphatically say, yes, powerful inference engines will be widely deployed" in markets such as imaging, voice processing, language recognition, and modeling.

"There will be some opportunity for stand-alone inference engines, but most IEs will be part of a larger system. Inference doesn't necessarily need hundreds of square millimeters of silicon. But it will be a major sub-system, widely deployed in a range of SoC platforms," Rowen said.

Kanter noted that Nvidia has a powerful inference engine processor that has gained traction in the early self-driving cars, and Google has developed an ASIC to process its Tensor deep learning software language.

In many other markets, what is needed are very low power consumption IEs that can be used in security cameras, voice processors, drones, and many other markets. Nvidia CEO Jen Hsung Huang, in a blog post early this year, said that deep learning will spur demand for billions of devices deployed in drones, portable instruments, intelligent cameras, and autonomous vehicles.

"Someday, billions of intelligent devices will take advantage of deep learning to perform seemingly intelligent tasks," Huang wrote. He envisions a future in which drones will autonomously find an item in a warehouse, for example, while portable medical instruments will use artificial intelligence to diagnose blood samples on-site.

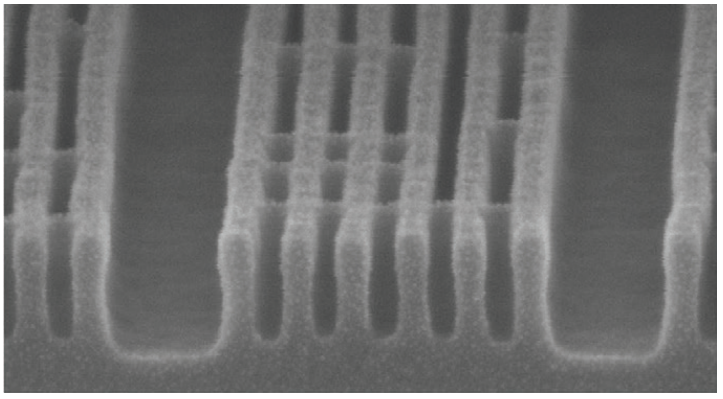
In the long run, that "billions" vision may be correct, Kanter said, adding that the Nvidia CEO, an adept promoter as well as an astute company leader, may be wearing his salesman hat a bit.

"Ten years from now, inference processing will be widespread, and many SoCs will have an inference accelerator on board," Kanter said.

First EUV lithography high-volume manufacturing solution for N5 BEOL

JOOST BEKAERT *and* **MING MAO**, *imec, Leuven, Belgium*

Immersion-based self-aligned quadruple patterning is combined with EUV lithography block patterning to achieve metal layers with pitches as small as 32nm.



At the 2017 SPIE Advanced Lithography conference, imec – in close collaboration with its suppliers – presented an industry relevant platform for patterning the most advanced back-end-of-line metal layers, conform with the foundry N5 technology node. Imec's solution includes two scenarios for EUV lithography insertion, as well as proposals for design rules, masks, photoresists, etching, metrology and variation assessment. In this article, one of these scenarios is described in more detail. It combines immersion-based self-aligned quadruple patterning with EUV lithography block patterning, to achieve metal layers with pitches as small as 32nm. To assess the platform's suitability for high-volume manufacturing, the uniformity of the layers and their local variability is discussed.

The patterning of advanced logic back-end-of-line layers

As we move towards more advanced technology nodes, the patterning of critical back-end-of-line (BEOL) metal layers with ever more aggressive pitches (e.g. 32nm) has become very challenging. In these BEOL layers, typically, trenches are created which are then filled with metal in a final metallization step. In order to create a disconnection in the continuous trenches, block layers perpendicular to the trenches are added, resulting in small metal tip-to-tips. In the industry, various options are considered to pattern the most aggressive BEOL layers and blocks. One option is to use immersion lithography in combination with so-called self-aligned quadruple patterning (SAQP) for the metal lines, and triple patterning for the block layers. This option however requires a triple block mask and a triple litho-etch process flow, which adds to the cost and complexity of the proposed solution. Another option is to pattern the BEOL metal layers directly with EUV lithography (EUVL) in one single exposure. Although this direct EUVL integration flow is very simple and cost-effective, pattern fidelity (e.g. the shape of the pattern) and pattern variability, as well as mask making are expected to be extremely challenging, especially for very small tip-to-tips.

One of the alternatives imec is evaluating is a 'hybrid' option, in which immersion-based SAQP of metal lines is combined with a direct EUV print of the block layer – using ASML's NXE:3300 scanner.

The imec N7 (iN7) EUV platform

To evaluate the viability of this 'SAQP + EUV block patterning' option, imec makes use of its iN7 platform. This platform has been developed to evaluate EUV patterning of advanced logic BEOL layers. The platform considers two layers: metal1, with 42nm pitch, and metal2, with 32nm pitch and 7.5 track design. Via1 connects the two metal layers using a dual damascene process flow. With these aggressive pitches, iN7 corresponds to IDM N7 and foundry N5 requirements for the BEOL. The patterning of both metal1 and via1 can be achieved through EUV single exposure. The iN7 platform is used to evaluate the hybrid immersion/EUVL solution for patterning metal2.

JOOST BEKAERT *is a Lithography R&D engineer and* **MING MAO** *is an etch process R&D engineer at imec, Leuven, Belgium.*

Optimizing design rules, mask and etch process

Prior to printing and evaluating the pattern, considerable efforts and innovations were performed in various litho-related areas. First, imec developed compliant design and design rules to support the possible patterning schemes. Also, an appropriate resist material was chosen for the EUV block process, and its impact on the optical proximity correction was studied – leading to a 2D OPC full-chip model. This model and other computational lithography techniques were used to design and fabricate the right EUV block masks. And finally, new chemistries and novel integration schemes for the etch process have been developed.

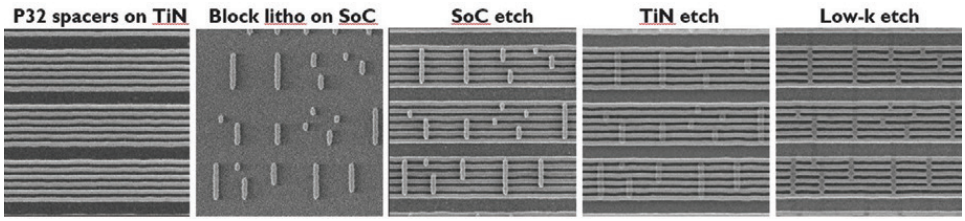


FIGURE 2. Illustration of the iN7 process flow for metal2 SAQP + block.

Creating SAQP lines and EUV blocks

SAQP (or self-aligned quadruple patterning) is a double spacer technique that is already well established in industry. Basically, this process uses one lithography step and additional deposition and etch steps to define spacer-like features.

Imec's process flow starts from metal2 core lines, i.e. a (pre) pattern of lines created by immersion lithography (using the ASML NXT:1970i immersion scanner). On top of this pattern, a layer of spacer material is deposited. Then, the spacer is etched and the core material is removed. This second 'core' pattern is then used to apply the second spacer, by re-iterating the sequence of spacer deposition, spacer etch and core removal. After these steps, each edge of a core line results in a doublet of spacer lines. As a final result, groups of 6 spacer lines are created with a 4x denser pitch (16nm half pitch) than the initial (pre)pattern. This grating is then transferred into SiN, leaving a pattern of SiN lines on top of a TiN layer (**FIGURE 1**).

In a next step, block features are added on top of the SAQP pattern. First, spin-on carbon (SoC) is coated on top of the spacer pattern. After resist coating, EUV exposure on the ASML NXE:3300 scanner then creates the block features in the resist material on top of the SoC. After SoC etch, pillar-like SoC block features of 65nm height stand on the spacer lines. This joint SAQP + block pattern is then patterned into the underlying TiN layer, which serves as a hard mask. By etching the trenches within this pattern into the low-k dielectric layer below, and metallizing them, the final metal2 pattern is obtained. The width of the block features determines the metal2 tip-to-tip critical dimension (**FIGURE 2**).

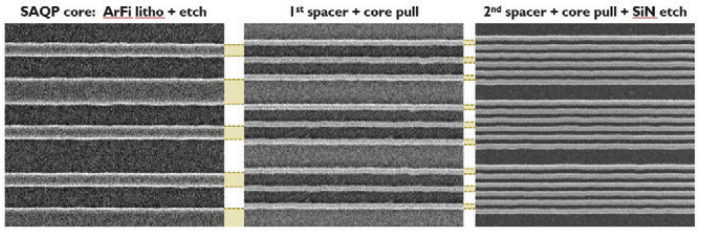


FIGURE 1. Illustration of the iN7 SAQP process.

Assessing pattern fidelity and local variability

An important part of this work is to qualify the pattern fidelity and variability, as this will contribute to the viability of the proposed solutions for industrial manufacturing. At this small pitch of 32nm, even minor process variations in EUV lithography may have significant impact on the device performance. Such variations are due to overlay and CD uniformity, but also to stochastic effects in the resist.

In particular, the uniformity of the width and length of the block features are important parameters. The width of a block at the location of a trench determines the resulting metal tip-to-tip on that trench. The final target for the iN7 design is to achieve a critical dimension of 21nm metal tip-to-tip after low-k etch. The experiments show that the critical dimension is sufficiently uniform over the wafer. With further fine-tuning, it is expected to remain below 1nm 3sigma. Also the local variation of the block width and placement are important and determine the overlap of the metal line-end with the via that connects to a layer above or below. The major contributor to the local variation turns out to be the stochastic noise, coming from statistical variations in how the available photons interact with the resist. Added to the overlay (which involves the ability of the scanner to align the various layers accurately on top of each other), an edge placement error of the metal tip position of ~5nm 3sigma is obtained. Whether this provides sufficient overlap with the via layer, will depend on the design rule. For example, if no direct neighboring vias are allowed, there will be sufficient margin through the design extension of the metal tip over the via.

Another critical dimension is related to the length of the block, as this will be critical in determining the metal trench 'blocking' efficiency. A too short block feature

could lead to an incomplete cut of the metal trench, and a too long feature can pinch neighboring metal trenches. Ideally, the block end is positioned halfway the spacer line. The maximum budget for the variation of the block end vs. the spacer edges is +/- 8nm. The dominant consumers of this budget are again the overlay and stochastics, adding to a local variation of ~6nm 3sigma. Thus, with a 3sigma requirement and if other contributors (such as intra-wafer CDU) can be kept small, the spacer width (16nm) is expected to provide sufficient budget to enable the SAQP + block technology for the iN7 (**FIGURE 3**).

Towards EUV implementation for high-volume manufacturing

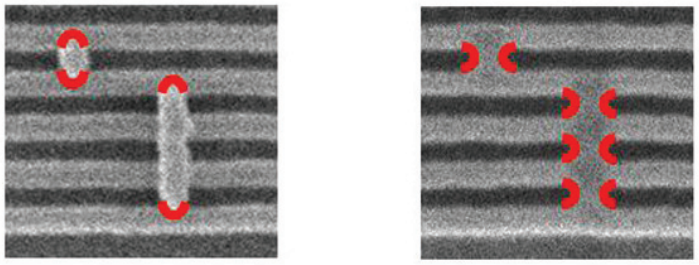


FIGURE 3. (Left) the length of the blocks determines the metal trench 'blocking' efficiency, while (right) the width determines the metal tip-to-tip.

Imec researchers have investigated the use of SAQP in combination with a single EUV blocking step for printing the critical 32nm pitch metal2 layer in the back-end-of-line. An important finding is that the current imaging performance of the ASML NXE:3300 is sufficient to print the metal2 block layer. The results clearly show the successful integration capability of the EUVL defined block. However, overlay and stochastics came forward as key attention points and will need further improvement, especially if further downscaling is pursued.

The proposed solution is a viable alternative to SAQP + immersion triple block patterning of the 32nm metal layer. From a cost perspective, a 20% cost reduction can be expected from the 'hybrid' solution with direct EUV block print, and EUV print of the vias. An additional cost reduction of 3% is expected from a scenario that uses only EUV in one single exposure for patterning the BEOL metal layers. First results point towards pattern fidelity and mask making as the main challenges for this option. Optimizations for this option are ongoing.

As pitch-only scaling doesn't meet the full requirements for the foundry N5 node, the solutions have been complemented by co-optimizing the technology and the standard cell libraries, resulting in significantly lower standard cell heights. This will allow a full node definition whereby the wafer cost increase of scaling boosters (approx. 3%) is offset by an area reduction gain of approx. 21%.

Including the proposals for design rules, masks, photoresists, etching and metrology, for which imec worked in close collaboration with equipment and material suppliers, all these studies form the first comprehensive solution towards EUVL enablement for high-volume manufacturing. ◆

Discovery of new PVD chalcogenide materials for memory applications

LARRY CHEN, **MARK CLARK**, **CHARLENE CHEN**, **SUSAN CHENG** *and* **MILIND WELING**, *IMI Inc., San Jose, CA*

A case study is presented based on the use of high throughput experimentation (HTE) for the discovery of new memory materials.

The ever increasing demands for data translate into more sophisticated and specific thin film requirements for semiconductor materials. Each film layer has to not only demonstrate desired film properties, but also show good interfacial behavior with neighboring layers to contribute to the performance of the whole film stack or device. As a result, modern thin film material systems are including more elements from the periodic table with more complex compositions. The demand for short time to market has also increased, making the development of new materials even more difficult. In this paper, we present a case study of using high throughput experimentation (HTE) for the discovery of new memory materials. By using a combinatorial approach of sputtering technology, HTE can be applied to PVD chalcogenides and other materials targeted at memory semiconductors.

PVD background

Ever since the deposition of materials by magnetron sputtering was introduced by F. M. Penning, the technology has become a major method for industrial thin film deposition, which typically generates dense, hard, and robust thin film materials at relatively low production cost. The technology has been applied to major industries such as semiconductors, photovoltaics, optical coatings, displays, hard mechanical coatings, and so on. However, optimizing the magnetron sputtering processes has always been challenging to process and hardware design engineers, since material properties like density, crystalline structure, grain size, optical indices of a deposited film strongly depend on various process parameters, such as power, pressure, substrate temperature, sputter gas type, plasma type, sputter source to substrate distance, substrate bias, and pumping throughput. Additionally, the material properties heavily depend on the underlying layers, including the chosen substrate, below a film stack due to a texture effect in film structure and a formation of interfacial layers which comes from the intermixing of both materials. All the above parameters contribute to increasing the level of complexity of the development.

The semiconductor industry is constantly searching for new materials with unprecedented physical, optical, electrical, and mechanical properties, not only as a single film but also as a component of complex featured film stacks or functioning devices. This requires exploration of new materials not limited to pure or binary systems, but to ternary, quaternary systems and beyond. A very efficient solution to cope with the increasing complexity of development and the demand for short development time is a combinatorial approach.

The combinatorial approach can be defined as a process that couples the capability for parallel production of large arrays of diverse materials together with different high-throughput measurement techniques for various intrinsic and performance properties supported by data analytics for identifying lead materials [3]. For magnetron sputtering technology, the optimization of process parameters has to be included as a major component of combinatorial approach. Considering all the multi-dimensional space of the development mentioned above, the combinatorial approach can be an excellent and efficient way of developing new materials in magnetron sputtering in terms of cost and time.

HTE methodology for PVD materials discovery

Platform Considerations As all process parameters in magnetron sputtering are somewhat correlated, it has been challenging for process engineers to come up with fully

LARRY CHEN, **MARK CLARK**, **CHARLENE CHEN**, **SUSAN CHENG** *and* **MILIND WELING** *are from IMI Inc., San Jose, CA.*

optimized process parameters for thin film production. In addition, semiconductor production facilities are typically optimized for consistent, efficient, high volume production of a single product at a time, and not for a wide range of simultaneous experiments. These factors make it challenging for memory manufacturers to test multiple materials, conditions and devices in an efficient manner, and without compromising either data quality or production throughput.

IMI's high throughput experimentation (HTE) platform is set up for accelerated experimentation. Its combinatorial PVD tool typically has four sputter guns and one additional port at the center. All sputter guns can be equipped with various types of target materials including chalcogenides, pure metals, oxides, and nitrides, and each sputter source can be operated by different plasma modes independently, such as direct current (DC), pulsed direct current (PDC), and radio frequency (RF) with the ability to co-sputter with all four guns. The additional port at the center can be equipped with an ion beam source for ion beam assisted deposition, or ion beam cleaning, or an additional sputter gun which enables five gun co-sputtering operation. Process parameter windows can cover larger regimes than most production tool process parameters (**Table 1**).

FIGURE 1 shows an example of a multi-target sputter chamber capable of controllably forming a variety of compounds in an array across a 300 mm substrate and an example substrate shown at right. The materials can also be deposited on a die-to-die basis (not shown) over a 300mm wafer test vehicle for direct device testing without the need for patterning. The effectiveness of the combinatorial screening can be increased by guiding the selection of material compositions using both semi-phenomenological and DFT-based modeling, as well as relating the experimental data to the results obtained from simulated annealing using ab-initio molecular dynamics and further DFT analysis of the simulated quasi-amorphous structures.

Process parameter	Range
Power density	1 – 9 W/cm2
Pressure	1 – 20 mTorr
Substrate temperature	RT – 400°C
Plasma type	DC, PDC, & RF
O2 concentration in sputter gas	0 – 100%
Annealing temperature	100 - 650°C
Annealing gas	Ar, N2, Air, O2, and forming gas

TABLE 1. Process range of PVD tool for HTE

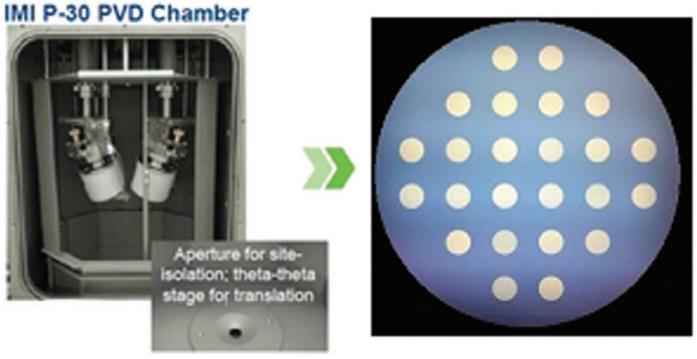


FIGURE 1. Multi-target PVD chamber with aperture (left), and 300 mm substrate with site isolated compositional variation array (right).

Deposition methodology

Two different methods can be used to deposit the combinatorial films of interest: site isolated spot and gradient approaches. For the site isolated spot approach, multiple numbers of spots were deposited on a substrate. Each individual spot represents a split condition from a design of experiment (DOE). Film composition can be controlled through the co-sputter of guns, which are equipped with targets consisting of different materials. Also, the process condition of each spot can be varied through the process parameter settings. All deposition conditions and procedures are fully automated.

In the gradient approach, non-uniform film in terms of composition and thickness is intentionally generated on top of a substrate by co-sputtering through an open large area aperture. A semi-empirical model is used for the control of non-uniformity. The modeling also helps in controlling the film composition throughout a target's lifetime. In this approach, composition gradients and the thickness gradients can be generated by a single film deposition on a substrate. Theoretically, an infinite number of variations can be analyzed within a film, which is only limited by the spatial resolution of metrologies.

Characterization and device performance

Once films have been deposited via PVD, characterization can be carried out, including testing of physical, optical and electrical parameters. These can range from general film characteristics including composition, thickness and crystallinity, to device-specific electrical parameters such as leakage, threshold voltage, and On/Off ratio.

Measuring and analyzing large numbers of data generated from HTE methodology can be time-consuming. By using the automated metrology tools and

a unified database system, measurements and analysis steps can be expedited to limit bottlenecks and deliver data most efficiently. A multi-stage approach can also help to prioritize and focus experimental resources on the most promising candidates.

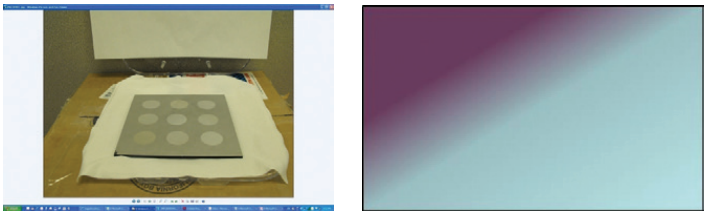


FIGURE 2. Site-specific on coupon (L) vs Gradient (R) deposition.

HTE vs traditional methods

Key benefits of the HTE approach include the expedited learning cycle, cost reduction, and improved data quality. For semiconductor applications, a single 200mm or 300mm wafer can hold more than 30 splits, which can lead to a reduction in cycle of learning time (one device wafer instead of more than 30). Additionally, as all spots on a single wafer go through the same follow-up device fabrication steps together, data can be free from unexpected fluctuations of subsequent steps. Overall, the HTE approach can expedite the learning cycle by 5 ~ 10 times compared to single substrate based approach. A comparison of both HTE with traditional methods is summarized in Table 2.

	Traditional Approach	HTE approaches	
		Site isolated spot	Gradient
Process per substrate	1	~ 30	1
Unique spots per run	1	1	> 100*
Number of substrates per week	30	10	30
Number of unique spots per week	30	300	3000
Number of unique spots per month	120	1200	12000
R&D cost	High	Low	Low
Time to market	Slow	Fast	Fast
Data quality	Low	High	High

* Unique spot number depends on spatial resolution of metrologies.

TABLE 2. Comparison of HTE with traditional methods

A case study in NVM

New materials for memory elements such as non-volatile memory (NVM) selectors must meet a wide range of performance parameters (**FIGURE 3** shows a typical memory cell with the selector element called out), in order to reduce sneak currents and manage variability in memory arrays.

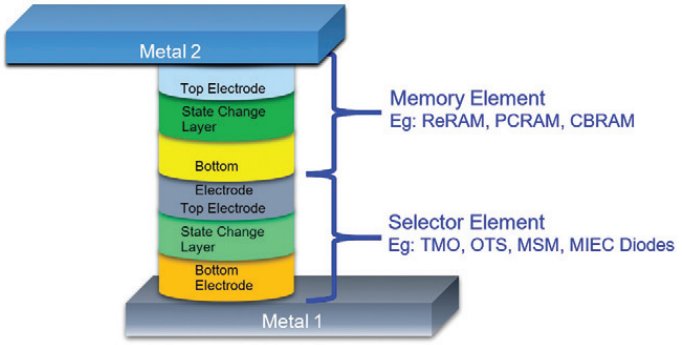


FIGURE 3. Generic cross-point memory cell.

	Traditional Approach	HTE approaches	
		Site isolated spot	Gradient
Process per substrate	1	~ 30	1
Unique spots per run	1	1	> 100*
Number of substrates per week	30	10	30
Number of unique spots per week	30	300	3000
Number of unique spots per month	120	1200	12000
R&D cost	High	Low	Low
Time to market	Slow	Fast	Fast
Data quality	Low	High	High

* Unique spot number depends on spatial resolution of metrologies.

TABLE 3.

Table 3 lists some of the key parameters desired in a memory selector material.

Of course, optimizing all of these parameters simultaneously in a single element or compound (and one that is practical for high volume memory manufacturing) is challenging. IMI's HTE methodology enables rapid and simultaneous optimization of key trade-offs between performance, reliability and integration, in the quest for an ideal selector.

HTE for NVM selector materials

Use of a HTE methodology allows rapid screening of NVM selector candidate material compounds, compositions and stacks. IMI has conducted multiple customer engagements in memory selector materials screening, and a typical experimental workflow is outlined in **FIGURE 4**, showing progression from PVD deposition,

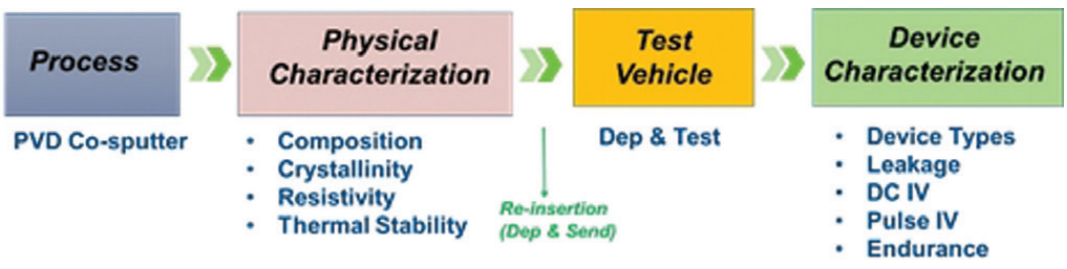


FIGURE 4. HTE Methodology for NVM Selector.

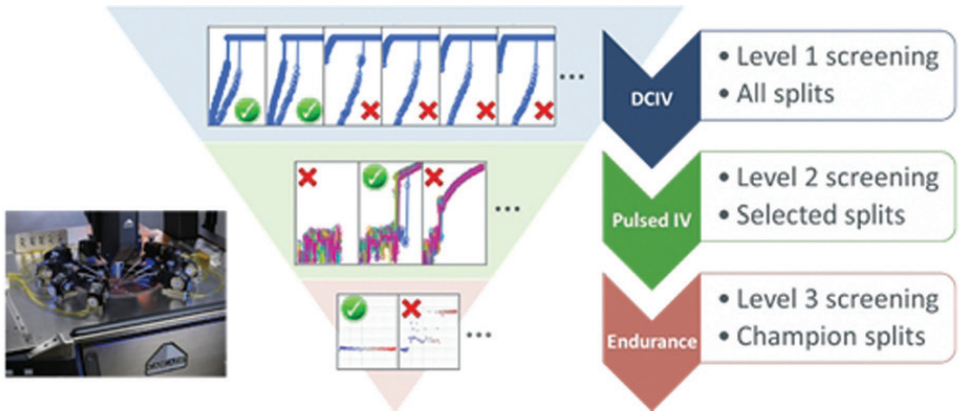


FIGURE 5. Increasingly advanced electrical characterizations to realize promising selector candidates

through physical and electrical characterizations of films and devices.

This experimental process can be carried out multiple times, through subsequently more advanced stages on a fewer number of samples, as promising candidates are narrowed down and further optimized. FIGURE 5 shows a possible strategy for testing a series of candidates through three different stages. In the earlier stages, a wide range of options could be screened quickly, but the more extensive (and time consuming) characterization and analysis can be saved for later stages, when only the best performing candidates are already selected. This enables the best use of deposition and testing resources, leading to optimal results in an efficient timeframe.

Fast and high-quality experimental results

IMI has extensive experience in working both on dynamic random access memory (DRAM) as well as NVM materials. In DRAM, the company has worked on development of dielectric, electrode and interface layer materials. IMI's process engineers, materials scientists and electrical engineers work upfront with a customer on the design of experiments to ensure the delivery of rapid cycles of learning with the most efficient use of resources.

A typical customer project might range between a few months up to a year or more, encompassing hundreds or even thousands of different experiments. In NVM selectors alone, IMI has conducted:

- 2500+ experiments on Metal Chalcogenides
- 2000+ experiments on MIEC
- 1000+ experiments on Transition Metal Oxides

Conclusion

High throughput experimentation can offer rapid, high quality materials data when effectively applied to PVD memory selector development. However it does require an advanced platform, and a facility and team experienced in efficient deposition and testing of the materials and devices. Materials and device expertise is also helpful in managing and optimizing the experimental workflow for maximum efficiency and high quality data. ◆

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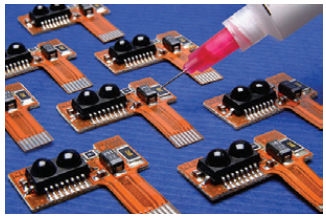

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MRAM lowers system power

ST-MRAM (spin-transfer magnetic RAM) is an extremely promising new technology with the potential to replace major segments of the market for flash, SRAM, and DRAM semiconductors in applications such as mobile products, automotive, IoT, and data storage. With ST MRAM technology, data is stored in minute magnetic nodes—a physical mechanism different from traditional non-volatile memory (NVM). MRAM technology fundamentally requires less energy to use, and features like byte-addressability that further contributes to energy efficiency.

Embedded MRAM primarily fills the role that is currently handled by embedded NOR flash: storage of code and data that must survive when the power is removed. Indeed, MRAM is challenging NOR flash due to overall lower power and byte-addressability.

Energy consumption starts with voltages and currents: their product yields the power of the device – that is, the rate of energy consumption. Lower voltages and currents mean lower power. Energy consumed is determined by how long that rate is sustained – power multiplied by operating time. Therefore speed, the ability to finish a job sooner, also contributes to lower energy consumption especially when devices can enter sleep mode after tasks are complete.

To understand how NOR flash consumes energy, we need to look at how it operates. Let's say we have a 32-bit word whose value we wish to update. With NOR flash, you can store data only in locations that have been freshly erased. This means you have to erase the old value before you can write the new value.

But there's a more significant challenge; you can't just erase those 32 bits. NOR flash can only be erased in sectors. So, in order to update those 32 bits, you have to find a new place to write them. This means creating and maintaining pointers to keep track of stored data since, with each update, the data location will move. Eventually, you run out of fresh space, and must perform garbage collection to free up the space used by all the out-of-date instances.

By contrast, MRAM has none of these requirements. Because it is byte-addressable, you can read and write just as you would with SRAM. Those 32 bits that needed updating? You simply write the new value over the old value.

BARRY HOBERMAN, *CEO, Spin Transfer Technologies*

MRAM consumes less energy for a number of reasons:

No erase before writing: NOR flash erasure is very slow. With MRAM, there's really no notion of erasing data; you're either writing 1s or 0s, in any combination. The need to erase is a key contributor to the energy consumption of a NOR flash device.

Faster, lower-power writing: Not only can MRAM devices be written more quickly than NOR flash (even without considering erasure), the power while writing is also lower. The fact that you can complete the operation sooner means you can put the device to sleep sooner, yet another advantage to lowering energy.

No charge pumps: NOR flash, unlike MRAM, needs high voltages internally – much higher than the voltages at the external power pins. Those voltages are generated by internal charge pumps. Ideally, power would stay the same, but real charge pumps aren't ideal; their inefficiency means lost energy.

Charge pumps also take longer to power up, and settle after a sleeping device awakens. This increases wake-up times dramatically. MRAM wakes up in nanoseconds to micro-seconds; NOR flash in milliseconds.

No complex storage management: The lack of byte-addressability in NOR flash creates complexity that increases the time to store data and code. Data tables must be maintained, along with the occasional garbage collection. The CPU, or some other circuit, must manage this data storage. These other devices consume energy, so the more time spent managing data, the more energy consumed. This energy consumption doesn't apply to MRAM technology.

Mixed read/write stream: NOR flash storage operations, due to complexity, mean long lock-out times during writes. No data reading is permitted during these times. If certain pieces of data are quickly needed, then further management may be required to anticipate this ahead of a data write, so the data can be cached. By contrast, MRAM can handle a stream of operations – reads and writes – in any combination.

Staggered writing: Data can be stored 32 bits at a time. While overall energy consumption in doing this is lower for MRAM than for NOR flash, it still might challenge the peak current capabilities of a battery-powered device. The ability for MRAM to break the write into four successive single-byte writes, a feature known as "staggered write," reduces current demands on the battery. ◆

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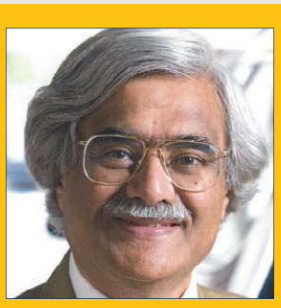

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