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SEPTEMBER 2016 VOL. 59 NO. 6

NIL, combined with sealing and bonding processes, can enable the production of next-generation biotechnology devices. Source: EVG.

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editorial

A changing industry

The semiconductor industry is changing in some big ways. Demand for PCs and mobile devices – once the main drivers of growth – has slowed. Gains from traditional scaling are harder to come by. Cost per transistor is now increasing. Consolidation is widespread up and down the supply chain, which may slow innovation. ITRS efforts have been abandoned.

Yet, despite this "maturing" of the industry – at least as we know it -- opportunities abound. The Internet of Things (IoT) is set to explode, which will result in a demand for "things" such as sensors and actuators, but also cloud computing.

Earlier this year, Brian Krzanich, CEO of Intel, wrote about five core beliefs that he holds to be "undeniably true" for the future:

- The cloud is the most important trend shaping the future of the smart, connected world – and thus Intel's future.
- The many "things" that make up the PC Client business and the Internet of Things are made much more valuable by their connection to the cloud.
- Memory and programmable solutions such as FPGAs will deliver entirely new classes of products for the data center and the Internet of Things.
- 5G will become the key technology for access to the cloud and as we move toward an always-connected world.
- Moore's Law will continue to progress and Intel will continue to lead in delivering its true economic impact.

While it's true that it's difficult to forecast what the overall impact of the IoT movement will have on the semiconductor industry, or how big it will be. Speaking at The ConFab in June, Tom Caulfield, SVP and GM of Fab 8 at GLOBALFOUNDRIES, said the IoT opportunity represents "magnitudes that are well beyond anything we've done before." A recent McKenzie study estimates $50-75 billion dollars of additional semiconductor revenue in an industry that today is $350 billion.

IoT, cloud computing and 5G will result in increased demand for leading edge semiconductor technology, which in turn will create a demand for 7 and 5nm devices and beyond. Perhaps more importantly, there will be tremendous demand for a wider variety of solid state devices, including MEMS, LEDs, power electronics, biomedical devices, thin film batteries and photonics/plasmonics.

There will be a need to integrate these devices for the usual reasons: to improve performance, and reduce cost and size. This will lead to innovative new packaging strategies and better chip-package co-design tools. It will create a demand for new types of manufacturing equipment and materials. New business models and new approaches to collaboration will also be required.

In short, the semiconductor industry is going through some fundamental changes, but the future has never looked brighter. As Caulfield said at The ConFab, "The demand for silicon is going to grow in an incredible way. What we need to do in this industry, is what we've done all along. We've reinvented ourselves every 18 months to 2 years with Moore's Law. Now we have to start reinventing ourselves in how we engage and collaborate together."

—Pete Singer, Editor-in-Chief

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Web Exclusives

Kateeva: Enabling OLED success

Kateeva is out to change the way displays are being made, and during Tuesday's Silicon Innovation Forum keynote at SEMICON West 2016, Kateeva President and COO Conor Madigan, PhD, laid out how their YIELDJet inkjet system is making that happen.

http://bit.ly/2aPkTt2

Packaging and displays drive new litho requirements

Fan-out wafer level packaging (FOWLP) is gaining traction, leading to higher I/Os and larger formats, and new mobile displays are pushing the limits of pixel per inch (PPI) while also moving to larger formats. Both trends are driving new requirements for lithography equipment, including steppers, track systems and photoresists. Both packages and displays are employing new types of materials and thinner substrates as well.

http://bit.ly/2b1TuVG

Insights from the Leading Edge: IMEC 20m pitch thermo compression copper pillar bonding

Contributing Editor Dr. Phil Garrou continues his look at IEEE ECTC 2016.

http://bit.ly/2aPl07Z

Flexible medical device manufacturing developments

Medical and health/wellness monitoring devices provide critical information to improve quality-of-life and/or human life-extension. To meet the anticipated product needs of wearable comfort and relative affordability, sensors and signal-processing circuits generally need to be flexible. The SEMICON West 2016 Flexible Electronics Forum provided two days of excellent presentations by industry experts on these topics, and the second day focused on the medical applications of flexible circuits.

http://bit.ly/2aPn7c4

n&b news and blogs

IEDM 2016 has "new twists," supplier exhibits for the first time

A bit earlier than usual, the IEDM (International Electron Devices Meeting) press kit is available, and among the announcements are a couple of surprises. The biggest practical change is the addition of an exhibit hall – up to now the conference has been almost religiously anti-commercial, to the extent that forums sponsored by Applied Materials, ASM, and Synopsys have had to be held offsite in other hotels.

http://bit.ly/2aWdVV6

Update from EUVL Workshop in Berkeley

The 2016 EUVL Workshop was held last month at LBL in Berkeley, where we heard the latest news on EUV Lithography R&D development topics.

http://bit.ly/2aWdGta

Established technology nodes: The most popular kid at the dance

The Internet of Things (IoT) means many things to many people, but the segment of IoT related to sensors and connectivity is the answer to the longevity question. The functionality we crave, such as smart power management for longer battery life, and Wi-Fi and Bluetooth for more connectivity, are more cost-effective when implemented at established nodes between 40 nm and 180 nm. Consequently, the high consumer demand for these capabilities is driving increased demand for ICs manufactured using these processes. In a nutshell, the nodes that best support radio frequency (RF) and mixed-signal IC designs with low power, low cost and high reliability are seeing a much higher demand than in the past.

http://bit.ly/2bDSg62

Power semiconductor market revenues decline

Overall revenue for the power semiconductors market globally dropped slightly in 2015, due primarily to macroeconomic factors and application-specific issues, according to a new report from IHS Markit.

http://bit.ly/2aN0NOe

worldnews

USA - **Lam Research Corp.** introduced an atomic layer deposition process for depositing low-fluorine-content tungsten films.

ASIA - **Samco** announced that it will open its Malaysia branch office on Aug. 10, 2016 in Petaling Jaya, a suburb of Kuala Lumpur.

USA - **Cascade Microtech** announced the release of a comprehensive low-frequency noise measurement solution for device modeling, characterization and reliability testing with MeasureOne solution partner **Keysight Technologies**.

ASIA - **Mouser Electronics, Inc.** announced the appointment of Sam Katsuta as Vice President of Mouser Electronics-Japan.

EUROPE - **STMicroelectronics** was named the MEMS Manufacturer of the Year at the MEMS World Summit.

EUROPE - **EV Group** introduced the EVG50 automated metrology system.

ASIA - **GLOBALFOUNDRIES** announced that Wallace Pai has been appointed as vice president and general manager of China.

USA - **Busch, LLC.** announced plans to build a new 44,000 sq. ft. building in Austin, Texas.

ASIA - **A*STAR's Institute of Microelectronics** launched two consortia on advanced packaging, the Silicon Photonics Packaging consortium (Phase II) and the MEMS Wafer Level Chip Scale Packaging (WLCSP) consortium.

EUROPE - **imec** and **Synopsys, Inc.** announced an interconnect resistivity model to support the screening and selection of alternative interconnect metals and liner-barrier materials at the 7nm node and beyond.

What's happening in Japan's semiconductor industry?

By Yoichiro Ando, SEMI Japan

The 2016 global semiconductor market is forecast to decrease by 2.4 percent from the previous year according to the World Semiconductor Trade Statistics (WSTS). SEMI forecasts that the global semiconductor manufacturing equipment market will be effectively flat this year. However, SEMI also forecasts double-digit growth in 2017 with significant new fab construction starts in 2016 and 2017 that will drive later equipment. The forecast foresees the Japan market will shrink through 2017. This article provides insight behind those forecast numbers.

Toshiba's new Fab 2 cleanroom (Source: Toshiba)

Overview

Large-scale investments in 300mm wafer lines in Japan are primarily made by three companies: Toshiba (NAND Flash), Sony (image sensors) and Micron Memory Japan (DRAM). The logic players' investments are largely for upgrading and expanding existing capacity; the companies producing power, surface acoustic wave (SAW), and automotive semiconductor devices are actively adding capacity by constructing new fabs and expanding existing fabs. These activities are planned on 200mm or smaller wafers, so the investments are smaller in terms of dollar values. However, they are important to Japan's semiconductor industry in the coming Internet of Things (IoT) age.

Toshiba plans a new mega fab

Toshiba continues to expanding its 300 mm NAND fabs in Yokkaichi in 2015 and 2016 including the second phase construction of Fab 5, new Fab 2 for 3D NAND flash memory production, and plan for a new fab (Fab 6).

The new Fab 6 will be dedicated to 3D NAND flash memory production, and is planned to be built in an adjacent area of the current Yokkaichi factory site. Detailed plans of the construction (such as construction period, production capacity, and investment to manufacturing instrument used) will be decided in FY 2016 based on market trends. Fab 6 is expected to be built in FY 2017. Production capacity of the fab is projected to be more than 200,000 wafers per month (300mm wafers) at full capacity.

Toshiba and Western Digital announced a plan in July 2016 to invest a total of 1.5 trillion JPY for the next three years in Yokkaichi operations. This investment will be for the construction of the new fab as well as for updating equipment for existing fabs such as new Fab 2 and Fab 5.

Sony expands 300mm capacity

Sony is also actively expanding its 300mm wafer fabs for increased production of complementary metal-oxide-semiconductor (CMOS) image sensors. Sony plans to expand production capacity not only with its existing lines but also to acquire fabs from other companies. Specifically, Sony acquired Tsuruoka factory in Yamagata prefecture in 2014 from Renesas Electronics

Continued on page 7

China's final chance to achieve its IC industry ambitions now underway

Over the past 20 years, China has become increasingly frustrated over the gap between its IC imports and indigenous IC production (**Figure 1**). It has oftentimes been quoted over the last couple of years that China's imports of semiconductors exceeds that of oil.

In its upcoming Mid-Year Update to The McClean Report 2016 (released at the end of this week), IC Insights examines the "Three-Phase" history of China's attempt at strengthening its position in the IC industry that started in earnest in the late 1990s (**Figure 2**).

In the late 1990s, China began to contemplate ways to grow its indigenous IC industry and assisted in creating Hua Hong NEC, which was founded in 1997 as a joint venture between Shanghai Hua Hong and Japan-based NEC (it merged with Grace in 2011). Then, as part of the country's 10th Five Year Plan (2000-2005), establishing a

Continued on page 8

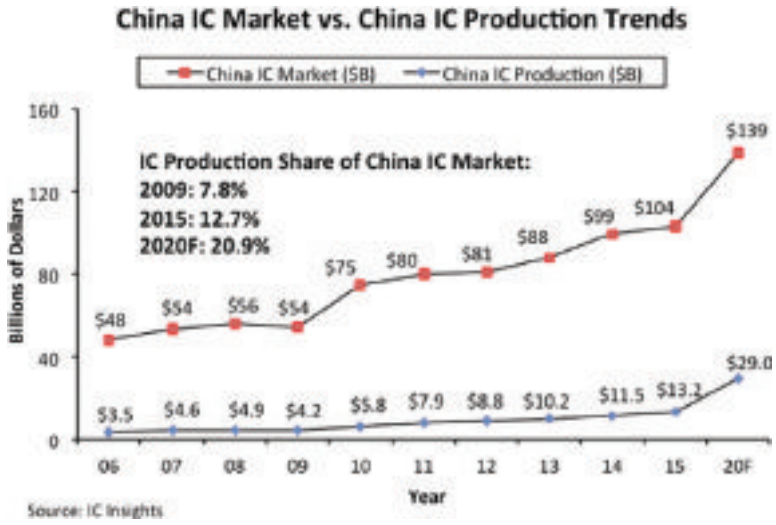


FIGURE 1.

International Technology Roadmap for Semiconductors examines next 15 years of chip innovation

The Semiconductor Industry Association (SIA) announced the release of the 2015 International Technology Roadmap for Semiconductors (ITRS), a collaborative report that surveys the technological challenges and opportunities for the semiconductor industry through 2030. The ITRS seeks to identify future technical obstacles and shortfalls, so the industry and research community can collaborate effectively to overcome them and build the next generation of semiconductors – the enabling technology of modern electronics. The current report marks the final installment of the ITRS.

"For a quarter-century, the Roadmap has been an important guidepost for evaluating and advancing semiconductor innovation," said John Neuffer, president and CEO, Semiconductor Industry Association. "The latest and final installment provides key findings about the future of semiconductor technology and serves as a useful bridge to the next wave of semiconductor research initiatives."

Faced with ever-evolving research needs and technology challenges, industry leaders have decided to conclude the ITRS and transition to new ways to advance semiconductor research and bring about the next generation of semiconductor innovations. While the final ITRS report charts a path for existing technology research, additional research is needed as we transition to an even more connected world, enabled by innovations like the Internet of Things. Some of these technology challenges were outlined in a recent SIA-Semiconductor Research Corporation (SRC) report, "Rebooting the IT Revolution," but work continues to define research gaps and implement new research programs.

The ITRS is sponsored by five regions of the world – Europe, Japan, Korea, Taiwan, and the United States. Through the cooperative efforts of the global chip manufacturers and equipment suppliers, research communities and consortia, the ITRS has identified critical gaps, technical needs, and potential solutions related to semiconductor technology.

"SIA appreciates the hard work, dedication, and expertise of those involved with the ITRS over the years and looks forward to continuing the industry's work to strengthen semiconductor research and maintain the pipeline of semiconductor innovations that fuel the digital economy," Neuffer said.

Huge 2H16 spending surge expected from Samsung, TSMC, and Intel

In addition to the monthly Updates, IC Insights' subscription to The McClean Report includes three "subscriber only" webcasts. The first of these webcasts was presented on August 3, 2016 and discussed semiconductor industry capital spending trends, the worldwide economic outlook, the semiconductor industry forecast through 2020, as well as China's failures and successes on its path to increasing its presence in the IC industry.

In total, IC Insights forecasts that semiconductor industry capital spending will increase by only 3% this year after declining by 2% in 2015. However, driven by the top three spenders—Samsung, TSMC, and Intel—capital spending in 2016 is expected to be heavily skewed toward the second half of this year. Figure 1 shows that the combined 2016 outlays for the top three semiconductor industry spenders are forecast to be 90% higher in the second half of this year as compared to the first half.

Combined, the "Big 3" spenders are forecast to represent 45% of the total semiconductor industry outlays this year. An overview of each company's actual 1H16 spending and their 2H16 spending outlook is shown below.

Samsung — The company spent only about $3.4 billion in capital expenditures in 1H16, just 31% of its forecasted $11.0 billion full-year 2016 budget.

TSMC — Its outlays in the first half of 2016 were only $3.4 billion, leaving $6.6 billion to be spent in the second half of this year in order to reach its full-year $10.0 billion budget. This would represent a 2H16/1H16 spending increase of 92%.

Intel — Spent just $3.6 billion in 1H16. The company needs to spend $5.9 billion in the second half of this year to reach its current $9.5 billion spending budget, which would be a 2H16/1H16 increase of 61%.

2016 Capital Spending Forecast (1H16 vs 2H16)

2016F Rank	Company	2015 ($M)	2016F ($M)	16/15 % Change	1H16 Actual ($M)	2H16 Spending Needed to Make Budget ($M)	2H16/1H16 % Change
1	Samsung	13,018	11,000	-15%	3,439	7,561	120%
2	TSMC	8,089	10,000	24%	3,426	6,574	92%
3	Intel	7,326	9,500	30%	3,646	5,854	61%
—	Top 3 Total	28,425	30,500	7%	10,511	19,989	90%
—	Others	36,427	36,610	1%	19,932	16,678	-16%
—	Total Cap Spending	64,852	67,110	3%	30,443	36,667	20%

Source: IC Insights, Company Reports

In contrast to the "Big 3" spenders, capital outlays by the rest of the semiconductor suppliers are forecast to shrink by 16% in the second half of this year as compared to the first half. In total, 2H16 semiconductor industry capital spending is expected to be up 20% over 1H16 outlays, setting up a busy period for the semiconductor equipment suppliers through the end of this year.

Further trends and analysis relating to semiconductor capital spending through 2020 are covered in the 250-plus-page Mid-Year Update to the 2016 edition of The McClean Report.

Japan's semiconductor industry, Continued from page 4

Corporation, and it is now operated as Yamagata Technology Center (TEC) of Sony Semiconductor Manufacturing Corporation, which is a semiconductor production subsidiary of Sony Corporation. In 2015, Sony acquired the 300mm line of the Toshiba Oita factory, for production of CMOS image sensors.

Sony plans to invest 70 billion JPY in FY 2016, and expand image sensor production capacity now 70,000 wafers per month as of first quarter of 2016. The restoration of Kumamoto TEC damaged by the Kumamoto earthquake would make investment in other TECs decrease.

Micron and TowerJazz

Micron Technology operates a 300mm fab in Hiroshima (Micron Memory Japan Fab 15). The fab manufactures DRAM with 12nm process technology. Micron invested US$750 million in 2015 and $500 million in 2016 for the technology upgrades. The capacity has been flat in these two years.

Panasonic TowerJazz Semiconductor, a Panasonic and TowerJazz joint venture, operates a 300mm foundry fab in Uozu. The company invested $10 million in 2015 and plans to invest the same amount in 2016 to improve the productivity.

Investments in 200mm and smaller wafer lines

Other major semiconductor manufacturers primarily invest in existing fabs and lines for maintenances and productivity improvements. Therefore, investment amount is modest. However, these fabs will be the major source for semiconductor devices of the Internet of Things applications.

- Renesas Electronics Corporation plans upkeep of production capacity of Kumamoto fab (200mm wafer fab) and Naka fab (300mm wafer fab).

- Fujitsu enhances Fab B2 of Mie Fujitsu Semiconductor Limited, which provides foundry services with 300mm wafer lines. Taiwan's major foundry UMC participated in capital of Mie Fujitsu Semiconductor Limited, and assists with 40nm process technology.

- Rohm Co., Ltd. plans to invest more than 10 billion JPY in enhancement of 200mm lines of fab and others in the headquarters.

- Fuji Electric Co., Ltd. continues enhancement of its 200mm wafer lines for IGBT of Yamanashi plant in FY 2016. Fuji Electric further expands its SiC power device production capacity by enhancing 200mm wafer lines at Matsumoto fab.

- Mitsubishi Electric Corporation manufactures power devices at 200mm wafer line of Kumamoto fab. Mitsubishi Electric continues enhancement of power device production capacity.

- Shindengen Electric Manufacturing Co., Ltd. is enhancing its power semiconductor module production by adding a new line each for Akita Shindengen Co., Ltd. and Higashine Shindengen Co., Ltd. from FY 2015.

Electronic parts and optoelectronic devices

The electronic parts companies are emerging as new fab owners in Japan. Their recent activities are summarized below:

- New Japan Radio Co., Ltd. continues enhancement of production capacity of SAW devices and GaAs ICs at its Kawagoe fab in 2016.

- Hamamatsu Photonics K.K. continues enhancement of MEMS fabrication facility (Fab 13) which started operation in March 2014.

- Upkeep of new clean room of Toyota Motor Corporation, which started operation in 2014, is now underway. Currently, this line is used for research and development, and trial production of SiC devices.

- Murata Manufacturing Company, Ltd. is building a new fab for SAW filter production at its headquarter factory in Toyama. The new fab construction will be completed in September 2016. Total investment to the facility is planned to be 12 billion JPY. Then it will be equipped with 200 mm (mostly secondary) equipment.

- Taiyo Yuden Co., Ltd. continues its enhancement plan of Oume fab in FY 2016, which was acquired from Hitachi in 2013 for SAW device production.

- TDK agreed to acquire 125mm wafer lines in Tsuruoka Factory from Renesas Electronics Corporation in November 2015. TDK plans to enhance its production capacity of super miniature electronic components at this plant. Production will start in FY 2016 after replacement of manufacturing equipment to conform to products to be manufactured. Investment will continue in FY 2016 as well for startup of the mass production and maintenance at this plant.

China's final chance, Continued from page 5

strong China-based IC foundry industry became a priority. As a result, pure play foundries SMIC and Grace (now Hua Hong Semiconductor) were both founded in 2000 and XMC was founded in 2006. This effort is categorized by IC Insights as Phase 1 of China's IC industry strategy.

In the early 2000s, to help boost the sales of its indigenous foundries, as well as ride the strong wave of fabless IC supplier growth, the Chinese government began attempts to foster a positive environment for the creation of Chinese fabless companies. It should be noted that eight of the current top 10 Chinese fabless IC suppliers were started between 2001 and 2004 and seven of them were in the top 50 worldwide ranking of fabless IC companies last year. This stage of China's IC industry strategy is labeled by IC Insights as Phase 2.

IC Insights believes that Phase 3 of China's attempt at creating a strong China-based IC industry began in 2014, just before the start of its 13th Five Year Plan which runs from 2015 through 2020. As discussed in detail in the Mid-Year Update, this Phase is being supported by a huge "war chest" of cash that is intended to be used to purchase IC companies and their associated intellectual property, provide additional funding to China's existing IC producers (e.g., SMIC, Grace, XMC, etc.), and to help establish new IC producers (e.g., Sino King Technology, Fujian Jin Hua, etc.).

In 1Q16, the U.S. Department of Commerce slapped an export ban on U.S. IC suppliers' shipments of ICs to China-based telecom giant ZTE in response to the company allegedly shipping telecommunications equipment to Iran while it was under trade sanctions by the U.S. This ban, if fully enacted, would have a devastating effect on ZTE's telecom equipment sales (including mobile phones). Thus far, the export ban has been postponed until August 30, 2016 pending further investigation by the U.S. Department of Commerce.

The Three Phases of China's IC Industry Strategy

Phase	Approach	Timeframe Initiated	Successful?
1	Build a strong indigenous pure-play foundry industry	Late 1990s - Early 2000s	No
2	Build a strong presence in the fabless IC supplier space	Early 2000s - Mid 2000s	No
3	Build a strong China-based IC supplier/manufacturer base with startups, acquisitions, and mergers	Mid 2010s - Late 2010s	????

Source: IC Insights

FIGURE 2.

The situation regarding ZTE and the abrupt announcement earlier this year of export controls on the company by the U.S. government sent shock waves throughout the Chinese government as well as China's electronic system manufacturers. At this point in time, such potentially drastic measures taken by the U.S. government against such a large Chinese electronics company has bolstered the Chinese government's resolve to make China more self-sufficient regarding IC component production, spurring increased emphasis on "Phase Three."

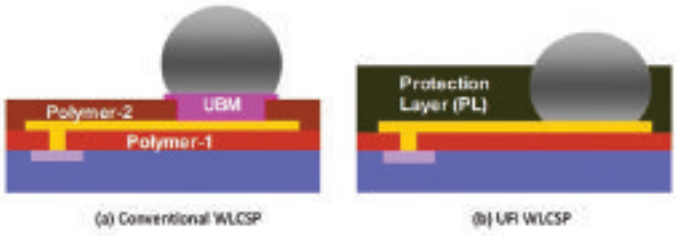
TSMC's UBM-free fan-in WLCSP

PHIL GARROU,
Contributing Editor

At the 2016 ECTC Conference, TSMC discussed their UFI (UBM-Free Integration) Fan-In WLCSP technology which they claim enables large die fine pitch packages.

Development of low-cost WLCSP for large die with high I/O count is desired for broadening its applications. Reliability issues including solder cracking and high chip warpage are known to be the main challenges for extending the die size of conventional WLCSP to more than 5x5 mm2 with ball pitch smaller than 350 µm.

TSMC has discovered that by controlling the maximum strain location and optimizing materials, chip warpage and the stress between silicon and the PCB can be reduced which improves both component and board-level reliabilities of WLCSP packages. Packages as large as 10.3x10.3 mm2 with both 400 and 350 µm ball pitches have been developed.



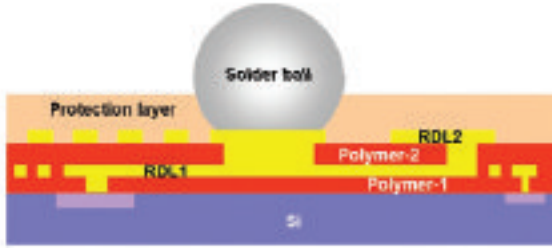
UBM is used as an interfacial layer between the metal pad of the integrated circuit and the solder ball. The formation of UBM/solder intermetallic compounds (IMC) limits the board level reliability of the package due to the poor mechanical robustness of IMCs. When the die size is increased, stress increases which promotes cracking at the UBM/solder ball interface.

TSMC claims their UFI WLCSP fabrication cost is lower than conventional WLCSPs due to the elimination of the UBM. Removal of the UBM also reduces the thickness of the package by 30%.

Figure 1 compares the structures of a standard WLCSP vs the TSMC UFI WLCSP. In the UFI WLCSP, the solder balls are directly mounted to the Cu RDL followed by the polymeric PL (protection layer which secure the balls.

Very similar removal of UBM and subsequent thickening of the copper pad has been reported before by Amkor in 2010 [1].

TSMC simulation results showed the solder joint fatigue life decreases with increasing die sizes for both UFI and the conventional WLCSP. Predicted solder ball fatigue life was found to increases with decreasing die thickness. The authors suggest that decreasing the die thickness not only reduces the thermal expansion difference between the die and the PCB, but also causes the die to bend more under thermal loading. In addition, simulation results imply that solder joint creep strain for solder mask defined (SMD) structures is 72% higher than for non-solder mask defined (NSMD) structures because of its reduced flexible solder joint height and the constraint of the solder mask. Thus they concluded that it is better to use NSMD type of PCB for UFI WLCSP. The use of NSMD structures to increase reliability has been known since the work of Bell Labs Ejim [2].



The UFI WLCSP passes all component-level tests and exhibited board-level thermal cycle life that is 1.4 and 2.3 times longer than that of the conventional WLCSP in terms of the first failure and the Weibull distribution, respectively. 10mm UFI WLCSP have passed component-level reliability tests such as TCB1000, uHAST96 and HTS1000, and board-level reliability tests of TCG500 and drop tests.

To demonstrate the possibility of higher interconnect density, they fabricated UFI- WLCSP with multiple RDL layers. The package with two RDL layers had die size of 10.3 x 10.3 mm2 and ball pitch of 350 µm (Figure 2). Again such structures passed all component level reliability testing.

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Packaging

Fab facilities data and defectivity

ED KORCZYNSKI,
Sr. Technical Editor

At the 4th annual Entegris Yield Forum held during Semicon West, attendees heard from executives representing the world's leading memory fabs discuss manufacturing challenges Among the excellent presenters was Norm Armour, managing director worldwide facilities and corporate EHSS of Micron. Armour has been responsible for some of the most famous fabs in the world, including the Malta, New York logic fab of GlobalFoundries, and AMD's Fab25 in Austin, Texas. He discussed how facilities systems effect yield and parametric control in the fab.

Just recently, his organization within Micron broke records working with M&W on the new flagship Fab 10X in Singapore—now running 3D-NAND—by going from ground-breaking to first-tool-in in less than 12 months, followed by over 400 tools installed in 3 months. "The devil is in the details across the board, especially for 20nm and below," said Armour. "Fabs are delicate ecosystems." Armour gave a few examples of component-level failures that caused major yield crashes.

Ultra-Pure Water (UPW) is critical for IC fab processes including cleaning, etching, CMP, and immersion lithography, and contamination specs are now at the part-per-billion (ppb) or part-per-trillion (ppt) levels. Use of online monitoring is mandatory to mitigate risk of contamination. International Technology Roadmap for Semiconductors (ITRS) guidelines for UPW quality (minimum acceptable standard) include the following critical parameters:

- Resistivity @ 25C >18.0 Mohm-cm,
- TOC <1.0 ppb,
- Particles/ml < 0.3 @ 0.05 um, and
- Bacteria by culture 1000 ml <1.

In one case associated with a gate cleaning tool, elevated levels of zinc were detected with lots that had passed through one particular tool for a variation on a classic SC1 wet clean. High-purity chemistries were eliminated as sources based on analytical testing, so the root-cause analysis shifted to the UPW system as a possible source. Then statistical analysis could show a positive correlation between UPW supply lines equipped with pressure regulators and the zinc exposure. The pressure regulator vendor confirmed use of zinc-oxide and zinc-stearate as part of the assembly process of the pressure regulator. "It was really a curing agent for an elastomer diaphragm that caused the contamination of multiple lots," said Armour.

UPW pressure regulators are just one of many components used in facilities builds that can significantly degrade fab yield. It is critical to implement a rigorous component testing and qualification process prior to component installation and widespread use. "Don't take anything for granted," advised Armour. "Things like UPW regulators have a first-order impact upon yield and they need to be characterized carefully, especially during new fab construction and fit up."

Photoresist filtration has always been important to ensure high yield in manufacturing, but it has become ultra-critical for lithography at the 20nm node and below. Dependable filtration is particularly important because industry lacks in-line monitoring technology capable of detecting particles in the range below ~40nm.

Micron tried using filters with 50nm pore diameters for a 20nm node process...and saw excessive yield losses along with extreme yield variability. "We characterized pressure-drop as a function of flow-rate, and looked at various filter performances for both 20nm and 40nm particles," explained Armour. "We implemented a new filter, and lo and behold saw a step function increase in our yields. Defect densities dropped dramatically." Tracking the yields over time showed that the variability was significantly reduced around the higher yield-entitlement level.

Airborne Molecular Contamination (AMC) is 'public enemy number one' in 20nm-node and below fabs around the world. "In one case there were forest fires in Sumatra and the smoke was going into the atmosphere and actually went into our air intakes in a high volume fab in Taiwan thousands of miles away, and we saw a spike in hydrogen-sulfide," confided Armour. "It increased our copper CMP defects, due to copper migration. After we installed higher-quality AMC filters for the make-up air units we saw dramatic improvement in copper defects. So what is most important is that you have real-time on-line monitoring of AMC levels."

Building collaborative relationships with vendors is critical for troubleshooting component issues and improving component quality. "Partnering with suppliers like Entegris is absolutely essential," continued Armour. "On AMCs for example, we have had a very close partnership that developed out of a team working together at our Inotera fab in Taiwan. There are thousands of important technologies that we need to leverage now to guarantee high yields in leading-node fabs." ◁▶

Semiconductors

High-volume processes for next-generation biotechnology devices

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Over the past several decades, miniaturization has significantly improved clinical diagnostics, pharmaceutical research and analytical chemistry. Modern biotechnology devices—such as biosensors, fully integrated systems for diagnostics, cell-analysis or drug discovery—are often chip-based and rely on close interaction of biological substances at the micro- and nanoscale. Thus, process technologies that enable the production of surface patterns and integration of fluidic components with small feature sizes are needed (**FIGURE 1**).

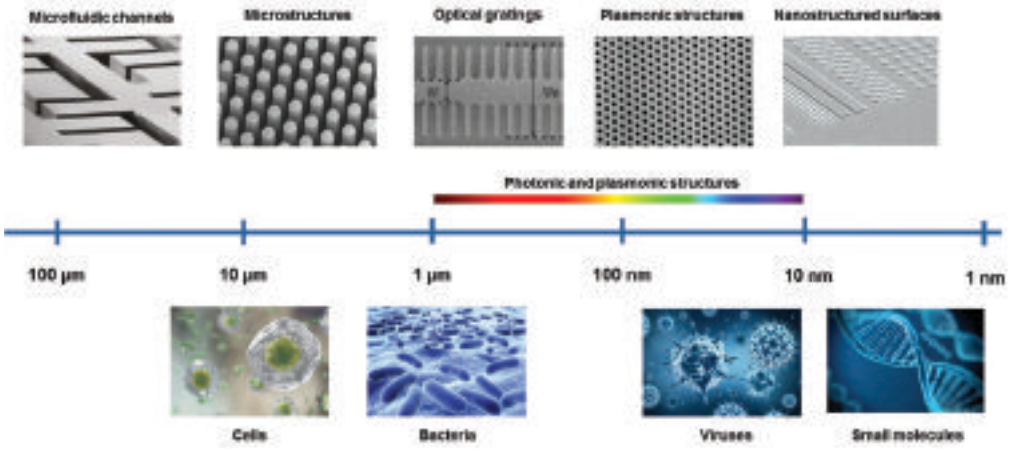

FIGURE 1. Biotechnology devices utilize a variety of structures at the micro- and nanoscale that interact with biological substances.

Today´s miniaturized biotechnology devices can be found in numerous applications, including fields related to human health as well as environmental and industrial sciences. For example, chemical sensors and biosensors are commonly used to analyze pH values, levels of electrolytes and blood-gas. Glucose sensors are a prominent example of highly successful commercial devices used for diabetes monitoring, where miniaturization has enhanced the development of implantable chips for continuous glucose level monitoring inside the human body. Fully integrated systems, including micro- and nanopumps for accurate insulin release, have also been shown. In general, such controlled drug delivery systems offer new opportunities for the treatment of common acute and chronic diseases. Moreover, microneedle arrays, which allow minimally invasive and painless delivery of drugs through the skin, neural electrodes for stimulation or monitoring signals inside the brain, or prosthetic devices such as artificial retinas, have also been developed.

Microfluidics plays a key role in the transport and manipulation of biological fluids in biotechnology devices. For example, laminar flow behavior can be overserved, which allows a well-defined control of liquids. Capillary forces can enable fluid flow without the need of active pumps. In addition, short distances reduce diffusion times of molecules, which lead to faster biological reactions. Overall, microfluidic devices offer a high degree of parallelization while using extremely-low-volume samples. Microfluidic devices that perform complete tasks or analysis, usually done in a laboratory, are referred to as lab-on-chip (LOC) devices. Other names include bio-chips or micro-Total-Analysis-Systems (µ-TAS). These systems are used in applications such as in-vitro diagnostics, high-throughput screening, genomics and drug discovery. LOC devices are also ideally suited for point-of-care testing (POCT), where they provide rapid diagnostics at the patient site.

Nanoimprint lithography

To successfully commercialize such products in a fast growing market with stringent requirements and high

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regulatory hurdles, precise and cost-effective microstructuring technologies are essential. Nanoimprint lithography (NIL) has evolved from a niche technology to a powerful high-volume manufacturing method that is able to serve today's needs and overcome the challenges of increasing complexity of microfluidic devices in particular, and biotechnology devices in general. NIL is a patterning technique capable of producing a multitude of different sizes and shapes on a large scale by imprinting either into a biocompatible resist or directly into the bulk material with resolutions down to 20 nm. NIL can be distinguished between three types of imprint technologies: hot-embossing or thermal NIL, UV-NIL, and microcontact printing (μ-CP).

Hot-embossing is a cost-effective and relatively simple process, well suited for the fabrication of polymer microfluidic devices with very high replication accuracy of small features down to 50 nm (**FIGURE 2**). A polymer sheet or spin-on-polymer is heated above its glass transition temperature, transforming the material into a viscous state. A stamp containing the negative copy of the structures is then pressed into the polymer with sufficient force to conformally mold the polymer. De-embossing is done after cooling the substrate below a certain temperature where the material retains its shape when removing the stamp. During hot-embossing, the structure is transferred by displacement of the viscous material. The process is characterized by short flow paths of the material, moderate flow velocities and imprinting temperatures. Residual stress is therefore low, especially when comparing the process to injection molding, which is an alternative production technique for microfluidics.

Because of the much higher process temperatures and pressures associated with injection molding, final products produced by this process usually experience higher internal residual stress, which easily results in significant deformation, such as warpage and shrinkage. In addition, a surface solidification layer is formed at the interface of the cold mold during the injection of the high-temperature molten polymer. This effect significantly influences the replication accuracy and optical quality. Extensive effort in process development and simulation is therefore often necessary for injection molding to replicate small features in an accurate manner. In contrast, hot-embossing allows precise replication of micro- and nanostructures with less effort and is superior when replicating high-aspect ratio features or when using very-thin substrates. Structures with high-aspect ratios are often needed in microfluidic chips for filtration elements, particle separation or cell sorting.

The ability to use very thin substrates enables the patterning of spin-on-polymer layers on top of other

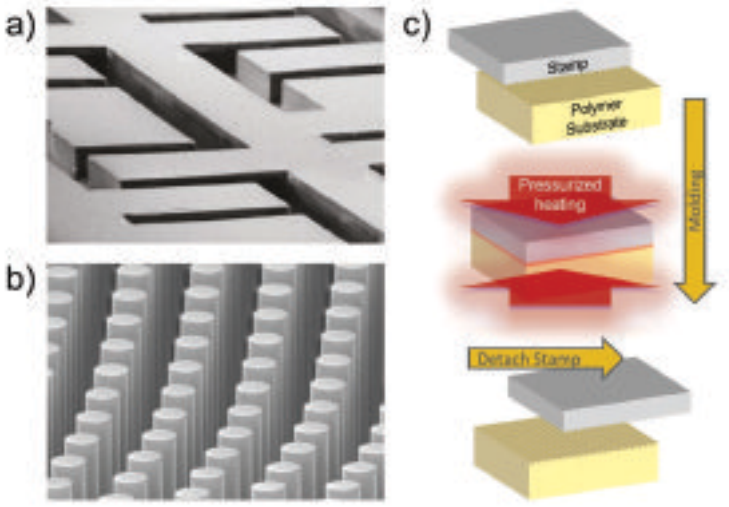

FIGURE 2: a) 200-μm wide microfluidic channels and b) 10-μm pillar arrays with high aspect ratios (7:1) fabricated by hot-embossing (Courtesy of National Research Council Canada). c) Schematic drawing of hot-embossing process flow.

materials or even roll-to-roll embossing using polymer foils for very-high-throughput production. Parallel wafer-based batch processing also enables fabrication of typical-sized microfluidic chips with throughputs comparable to or even higher than injection molding or similar techniques. Since master stamps for hot-embossing do not need to withstand the high temperatures and forces required for mold inserts for injection molding, they are less expensive to produce. Therefore, hot-embossing is also a well suited technology for R&D and allows easier design changes in volume-production.

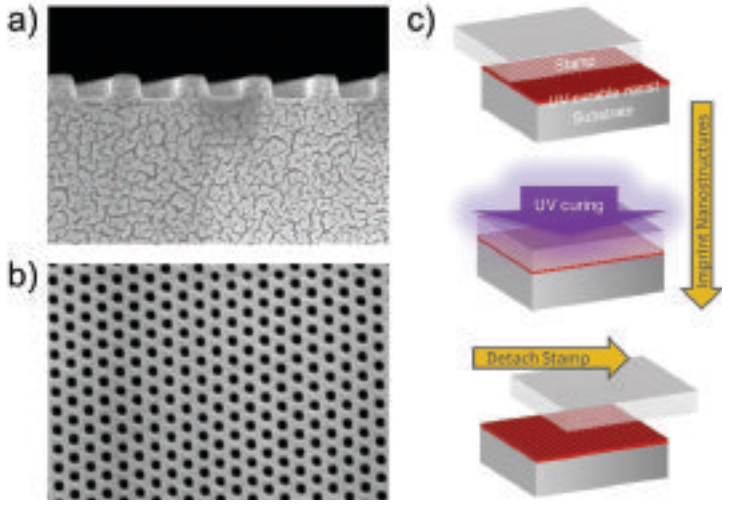

FIGURE 3: (a) 100-nm grating with residual layer <10 nm imprinted into 90 nm height resist on silicon substrate and (b) 350-nm photonic crystal fabricated by UV-NIL. c) Schematic drawing of UV-NIL process flow.

UV-NIL refers to a technique where a transparent stamp is pressed into a photo-curable resist and cross-linked by UV-light while still in contact (**FIGURE 3**). In biotechnology applications, the resist is usually coated onto silicon or glass substrates. Unlike hot-embossing, the UV-NIL stamp is brought in contact with the resist using minimum force to conformally join the stamp and substrate. The different mechanisms of curing and stamp attachment account for different advantages and fields of application of the respective technologies.

UV-NIL provides very-high-alignment accuracy, pattern fidelity, and throughput whereas hot-embossing is capable of imprinting higher aspect ratios and larger structures in the upper micron range as well as combinations of micro- and nanostructures. UV-NIL offers additional opportunities for biotechnology devices where features with ultra-high precision are needed. Examples include optical-based biosensors that often rely on noble metal nanostructures that influence properties of coupled light upon the binding of molecules onto the nanostructures. Regardless of what the sensing principle is based on (e.g. localized surface plasmon resonance or photonic band gaps), small changes in shape and size can significantly alter the properties of the sensing element.

In order to produce nanostructures made of metals, either additive or subtractive processes can be used. The former involves the deposition of a metal layer onto the patterned resist followed by a lift-off process, whereas the latter involves the transfer of the pattern into an underlying metal layer by etching processes. In both cases, the small residual layer must first be removed. Having a uniform residual layer is of high importance, especially for subsequent etching processes, and can be easily achieved with current equipment over large areas. Imprinted UV-NIL resists can also be used directly as functional layers. After many years of continuous resist development, a broad portfolio of optimized resist materials is available for various bio-applications. Another interesting aspect, especially for microfluidic devices, is the potential of nanostructures to influence surface properties. For

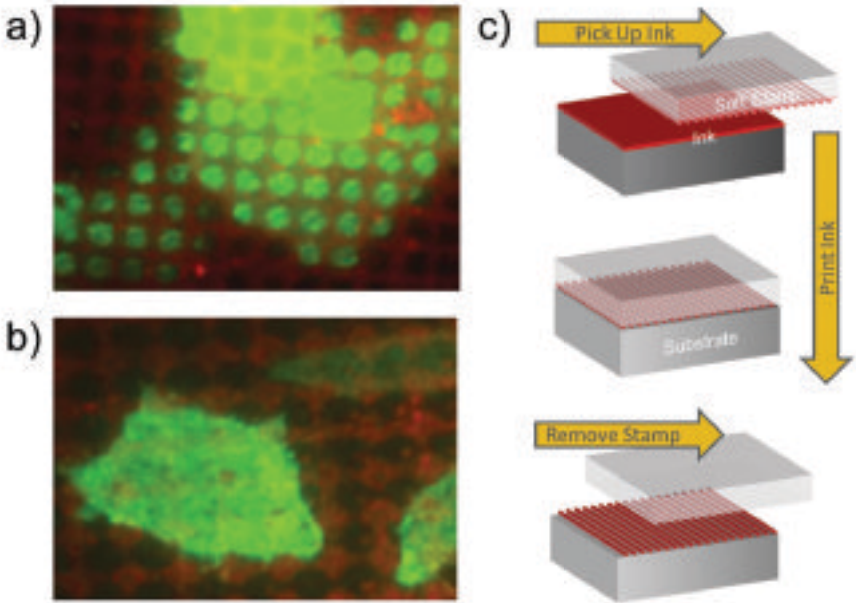

FIGURE 4: Bio-functionalized, micro-patterned array created by micro-contact printing for the detection of protein-protein interactions in live cells. a) Antibody-patterns induce the recruitment of two interacting proteins to micro-patterns, which is detected by fluorescence microscopy. b) Missing interaction of the two candidate proteins leads to homogenous distribution on the functionalized surface. c) Schematic drawing of micro-contact printing process flow. [Images adapted from Schwarzenbacher et al., 2008, Nature Methods; Weghuber et al., 2010, Methods in Enzymology].

example, nanostructures can change the surface behavior from hydrophilic to hydrophobic, which can be used to locally influence the fluid flow.

While UV-NIL is ideally suited for fabricating very small features, it is not well suited for features larger than several tens of micrometers. In cases where both highly-accurate nanostructures and large microfluidic channels are needed, hot-embossing can be used to imprint the channels on a separate substrate. The two substrates can subsequently be bonded together to produce the final device.

A third NIL option is μ-CP, where a pre-inked stamp is used to transfer materials such as biomolecules onto a substrate in a distinct pattern (**FIGURE 4**). Local modification of surface chemistry can, for example, be used to guide the growth of neurons on a chip. On the other hand, it can be used for the precise placement of capture molecules in biosensor fabrication. This technique is applicable on all common surfaces, such as silicon, glass or polymers with micro- and nanometer resolution and offers new possibilities for functionalization of biotechnology devices.

Although most current microfluidic devices do not follow the same degree of miniaturization in terms of chip-size compared to the microelectronics industry, large-scale parallel processing has a significant advantage in terms of costs and flexibility (**FIGURE 5**). Alternative fabrication techniques for microfluidic chips, such as injection molding, are principally serial processes and have limitations in up-scaling. Using nanoimprinting, 30 chips of the size of a microscopy slide (25 x 75 mm) can easily fit on a single 300-mm substrate. This format can be considered a good reference for an average-sized microfluidic chip. In terms of throughput, wafer-based batch processing is able to reach similar or better cycle times per device compared to alternative solutions, such as injection molding. UV-NIL has even been introduced on GEN2 substrates (370 x 470 mm). In addition, roll-to-roll processing can reach even higher throughput levels but is restricted to the structuring of flexible foils.

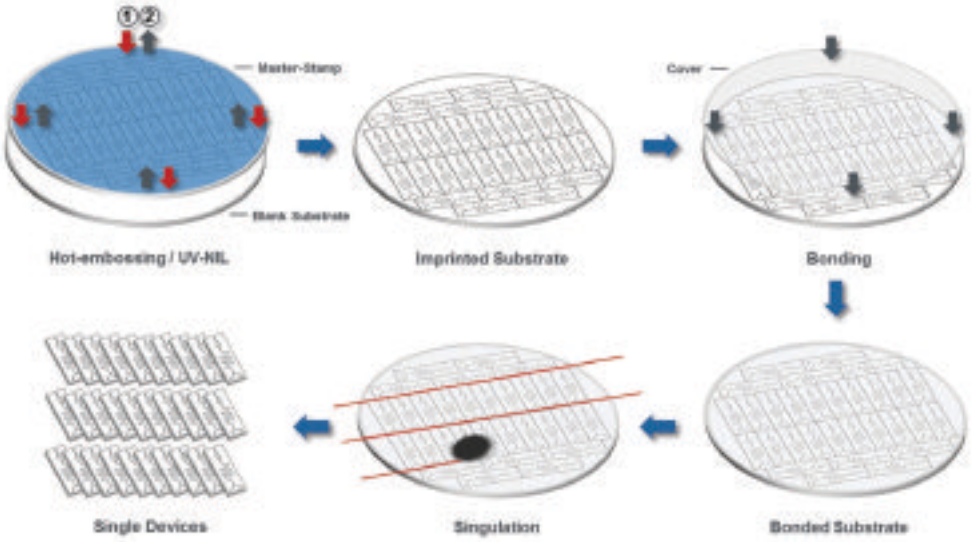

FIGURE 5: Large-area parallel processing offers significant advantages in terms of cost and flexibility. Additional processes, such as electrode fabrication or spotting of reagents, can also be efficiently integrated.

Wafer bonding

NIL has an additional advantage in terms of post-processing. Electrode fabrication, surface treatments or spotting of bio-reagents can be efficiently integrated in a large-area batch. The same is true for sealing and

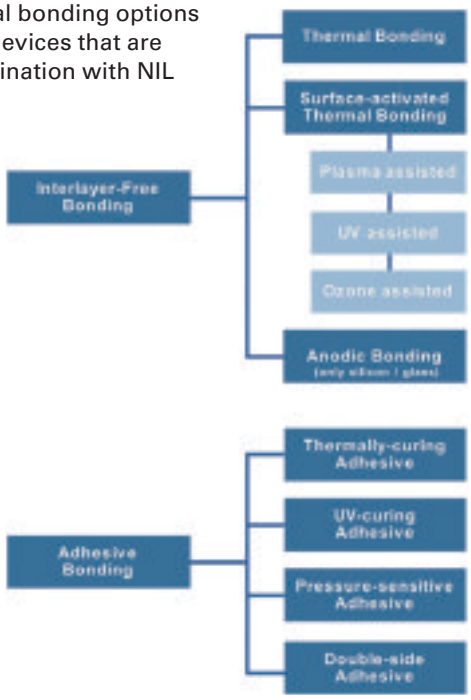

FIGURE 6: Typical bonding options for biotechnology devices that are well suited in combination with NIL processes.

encapsulation, an essential process step for all biotechnology devices. It is usually mandatory to close microfluidic channels, to fabricate a hermetic sealing for protection against environmental influences or even to provide packaging that is compatible for implantation into human bodies. In addition, interconnections to the outer world have to be incorporated, such as holes or fluidic connectors. Electronic connections or assembling the device together with an integrated microelectronic chip is also often necessary. Thus, bonding of different device layers, capping layers or interconnection layers is a key process that can be implemented together with NIL in a cost-effective large-area batch process. NIL has an additional advantage of providing a high surface quality that can significantly improve subsequent bonding of polymer devices. Surface roughness, total-thickness variation as well as warpage are usually lower than in devices fabricated by injection molding. In the following section, several well-suited bonding processes for sealing biotechnology devices are discussed (**FIGURE 6**).

A common requirement in biotechnology applications is optical transparency, at least from one side, since most devices rely on optical readouts. Glass is therefore often used as a capping layer for highly complex devices made of silicon. In such cases, anodic bonding can provide a high-quality hermetic seal, where bonding is achieved by high voltage and heat causing inter-diffusion of ions. Another process for joining glass or polymer devices is thermal bonding using high temperatures and pressures. Special attention has to be paid when using this technique for bonding polymer and, in particular, polymer microfluidic devices. Thermal bonding is performed by heating the substrate near or above the glass transition temperature, which softens the material. The additional pressure generates sufficient flow of polymer at the interface to achieve intimate contact and inter-diffusion of polymer chains. Pressure is removed after the substrate is cooled down to a specific value below the glass transition temperature. Un-optimized temperature and pressure can easily lead to deformation of microstructures. Plasma as well as UV and ozone treatment can be used to activate the polymer surface, which allows bonding at reduced temperatures and reduces the risk of deformation. Anodic and thermal bonding are interlayer-free processes and therefore do not introduce any additional material to the device.

Adhesive bonding is another process that found widespread use in sealing or encapsulating bio-technology devices. Many biocompatible adhesives are available today and high bond strength can be expected from this technique. Bonding with adhesives can be used to join many different materials. Often liquid adhesives are used, which can be cured thermally or by exposure to UV light. The latter offers a significant advantage that addresses another important issue in many pharmaceutical or diagnostic devices where bio-molecules have to be incorporated before sealing the device. UV-curing allows bonding at room-temperature whereas higher temperatures usually lead to denaturation or complete destruction of bio-molecules.

Adhesives usually have to be selectively deposited on the substrate, which can be achieved with μ-contact printing. Similar to bio-molecule printing, an adhesive can be transferred onto the substrate according to the pattern of the stamp. In contrast, however, an adhesive can be spin coated onto a transfer plate, which is then brought into contact with the substrate. By releasing the transfer plate, the adhesive will remain on the heightened structures. This production process is an elegant solution for microfluidic devices where micro-channels stay free of adhesive without the need for alignment. With these methods the adhesive can be coated as a thin layer (typically on the order of several microns) with very good uniformity over large areas. Commercially available adhesive tapes offer another solution, which can be easily laminated onto the microfluidic chips either in the form of double-side-adhesive tapes or pressure-sensitive-tapes. By using this process, the tape covers the top of microfluidic channels and can alter chemical or physical parameters of the channels, which can then influence the fluidic behavior or biological function of the device. Due to the availability of a variety of different tapes, however, such influences can be addressed and eliminated in many applications.

Summary

Micro- and nanotechnology combined with biotechnology has the potential to revolutionize many areas of healthcare, agriculture and industrial manufacturing. The market for miniaturized bio-devices is rapidly growing with technologies becoming increasingly complex. For successful translation of these technologies into new products, the availability of fabrication tools is key. Today´s NIL equipment offers a well suited solution, where complexity in design does not necessarily add manufacturing cost. Together with sealing and bonding processes that are well aligned with these structuring techniques, limitations of current fabrication methods can be overcome to enable the production for next-generation biotechnology devices.

Further reading

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Deep dive into the Intel/ Micron 3D 32L FG-NAND

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Key features of the cell structure, design and integration of the Micron 3D 32L FG-NAND device are discussed, and compared with Samsung's 32L and 48L V-NAND device.

The Intel/Micron 1st generation 3D TLC NAND with FG (floating gate) structure is finally on the market. TechInsights has torn down Micron's Crucial MX300 750 GB 2.5-inch SSD and reverse engineered Micron's 3D FG-NAND. The SSD has eight 3D NAND packages with 6FB22 NW852 package markings on the board, and two NAND dice in each package. We discuss some key features of the cell structure, design and integration of the Micron 3D 32L (32 layers or 32T, 32 Tiers) FG-NAND device, and compare with Samsung's 32L and 48L V-NAND device.

Die size and memory density

Micron's 32L 3D NAND die size (168.2 mm2) is much larger than Samsung's 32L (84.3 mm2) and 48L (99.8 mm2) 3D V-NAND devices. Micron's 32L 3D NAND memory size is 48 GB/die (384 Gb/die) which is more than 4 times Samsung 32L V-NAND (85.3Gb/die) and 1.5 times their 48L V-NAND (256 Gb/die). In other words, the memory density for the Intel/Micron 32L 3D NAND is 2.28 Gb/mm2, while Samsung's 32L V-NAND and 48L V-NAND are 1.01 Gb/mm2 and 2.57 Gb/mm2, respectively. **FIGURES 1 and 2** show comparisons of memory density and memory array efficiency for the Micron 32L, Samsung 32L and 48L 3D NAND memories. Micron's 2.28 Gb/mm2 memory density is the same as their announcement in 2015 at IEEE IEDM. They announced another 3D NAND with 768 Gb/die TLC (which is 4.29 Gb/mm2) earlier this year at ISSCC 2016. We can find a gap between the two announcements, including memory density difference (2.28 Gb/mm2 and 4.29 Gb/mm2). They might further shrink bitline pitch to 40 nm or expand to 48 layers. Comparing the 32L 3D NAND devices, the memory density on Intel/Micron's 1st generation 3D NAND is more than two times Samsung's 32L 3D NAND. Although Micron jumped into the 3D NAND race two years later than Samsung, Micron beat Samsung's 32L 3D NAND devices and came close to Samsung's 48L ones by using CMOS circuit under the memory array. We're looking forward to seeing their 2nd generation (either a modified 32L or a new 48L) FG-NAND.

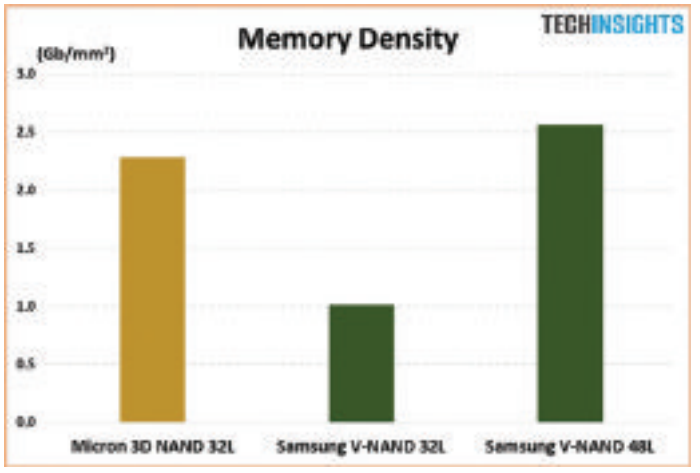

FIGURE 1. A comparison of memory density on Intel/Micron 3D 32L NAND, Samsung 3D 32L and 48L NAND.

3D memory cell architecture

As shown on **FIGURE 3**, the Intel/Micron 1st generation 3D FG-NAND (32L or 32T) has 4 planes with 32 tiles; while Samsung's 3D V-NAND, either 32L (2nd generation) or 48L (3rd generation), has 2 planes without a tile-like floor plan. An innovative technology from Micron is that CMOS decoders and sense-amps are sitting under the 3D FG-NAND memory array for high memory density (2.28 Gb/mm2). Referring to the memory tiles comprised of page buffer (PB), string drivers and CMOS circuits, the area of

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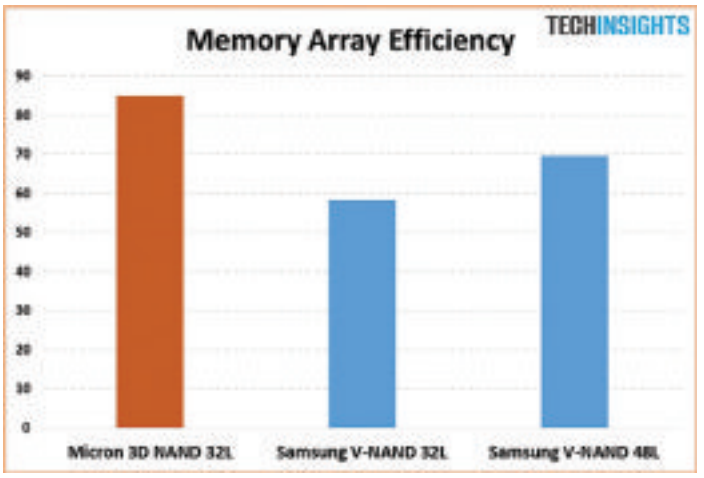

FIGURE 2. A comparison of memory array efficiency on Intel/Micron 3D 32L NAND, Samsung 3D 32L and 48L NAND.

unit memory tile is 4.12 mm2. The 1 kB page buffer, string drivers and other CMOS circuits on each memory tile have 2.20 mm2, 0.83 mm2 and 1.09 mm2 areas, respectively (**FIGURE 4**). As Micron mentioned at ISSCC 2016, placement of the wordline drivers under the array allows for the wordline lengths to be short.

Micron's 32L 3D FG-NAND uses a 4 metal CMOS plus FG-NAND array on common source plate technology. The FG-NAND array has 32 active wordlines, 6 dummy wordlines (3 on the top portion and 3 on the bottom portion), one source-side select gate and one drain-side select gate. All of the wordlines and select gates are on a Si/W-silicide-based common source plate. The NAND array has 40 gates (38 wordlines plus 2 select transistors), which is different from Samsung's 32L V-NAND which has 39 gates (36 wordlines plus 3 select transistors).

Micron's V-NAND uses a vertical Si-channel surrounded by a floating gate (FG) and a control gate (CG), termed a 'gate all around (GAA)' structure. The vertical Si-channel and control gate stacked memory cell structure is the same as Samsung's, however, Micron uses a silicon FG (floating gate) layer instead of Samsung's SiN charge trap

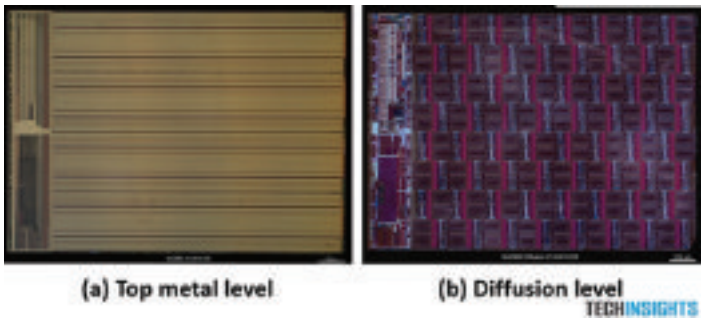

FIGURE 3. Top metal level and Diffusion level of Micron 3D 32L NAND die.

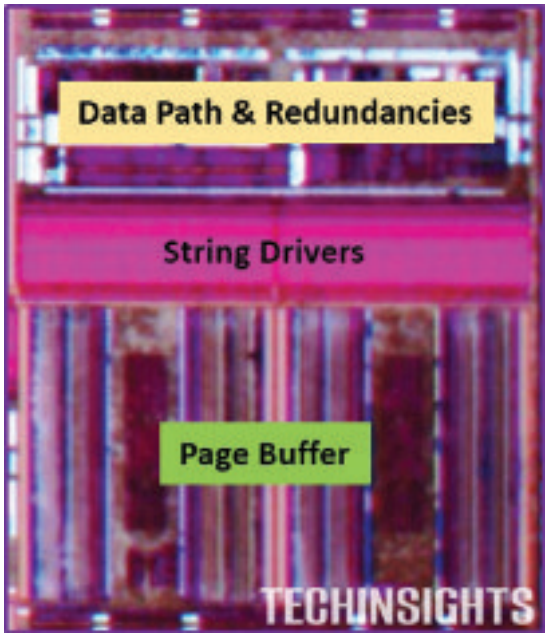

FIGURE 4. Memory tile layouts on Micron 3D 32L NAND die.

layer (CTL). The FG layer is far better way to store more electrons than a SiN layer. Micron's 52 nm 32L NAND array vertical cell gate pitch is less than Samsung's 60 nm 32L V-NAND vertical cell gate pitch. Micron's memory cell array (or Si-channel hole) height is 2.21 μm, which is 27% lower than that of Samsung 32L (2.9 μm).

Micron's 3D FG-NAND cell architecture has a 'CG/FG first, Channel last' scheme, while Samsung's 3D V-NAND cell integration has a 'Channel first, Gate last' scheme. Micron's process involves first making the control gate/dielectric stack. A recess etch would have been used to form cavities for the polysilicon floating gates (FG) and inter-poly dielectrics. The deposition of the tunnel oxide and polysilicon channel would complete then NAND string. An etch-back processes is applied for both CG and FG structures to recess and isolate the gates.

Micron's 2D 16 nm node planar thin-FG NAND Flash has a select gate with the same structure as the cell, which has a high-k dielectric stack and a thin polysilicon floating gate. To simplify the manufacturing of the 16 nm cell, the source and drain select gates are constructed in a similar manner as the cell. In contrast, Micron's 3D FG-NAND device has a select gate composition that is different from cell gate. Here, the source and drain select devices are single gate oxide transistors.

Placing the select gates and dummy wordlines under and on the memory cell gates looks reasonable from an integration perspective. Intel/Micron and Samsung have the same configuration of dummy wordlines near the select transistors, but Samsung has a SEG (Si epitaxial

growth) channel on GST (ground select transistor) structure. Micron uses a single select gate with a thick gate length (thickness) on the drain side, while Samsung has two thin SSTs (string select transistors). **FIGURE 5** shows a comparison of 3D cell gate structure on Samsung and Intel/Micron 32L NAND devices.

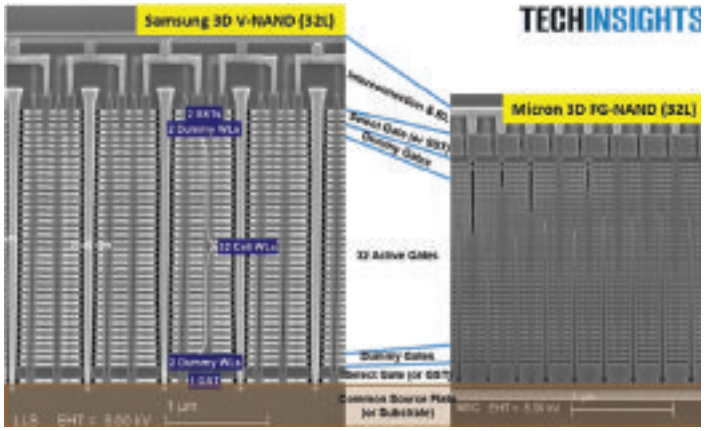

FIGURE 5. A comparison of 3D cell gate structure on Samsung and Intel/Micron 32L NAND devices.

3D NAND competition and roadmap

When Micron will produce 48L 3D FG-NAND commercial products is an open question. **FIGURE 6** shows a NAND roadmap for the major players of 3D NAND products (Samsung, Micron/Intel, Toshiba/SanDisk and SK-hynix). Samsung has 48L V-NAND SSD products and they are developing 64L for their next generation 3D V-NAND. Samsung has been more focused on 3D V-NAND development including yield improvement and 64L V-NAND than next generation 2D NAND (1z nm). Intel/Micron have just entered the V-NAND race with their 32L FG-NAND. Once they successfully release 48L and 64L, if in a timely manner, they may gain market share at the expense of Samsung, Toshiba and SK hynix. Toshiba and SanDisk are scheduled to release their 3D BiCS NAND products to compete in the 3D NAND sector soon.

Intel/Micron's 1st generation 3D FG-NAND devices with 32L (or 32T) are quite compatible with Samsung's 32L 3D V-NAND. Samsung and Toshiba use a CTL (charge trap layer), while Micron adopted thin-FG silicon layer as a storage between channel and CG. Although Micron's thin-FG layer contains more electrons than Samsung's CTL SiN layer, the etch-back process used to isolate the FG layers may result in non-uniform FG sizes and coupling ratios. Furthermore, the FG layer is getting smaller and may form nanowire-like or nanodot-like structures on the Si cylinder during the process integration creating performance non-uniformities. Samsung's CTL scheme does not suffer as much from process non-uniformities giving it an advantage. Additionally the CTL does not require isolation between each of the stacked cell gates.

Which is better? Intel/Micron's 32L 3D FG-NAND or Samsung's 32L (or 48L) 3D V-NAND? From the memory cell structure and process integration viewpoints, Samsung looks better than the Intel/Micron design due to the CTL scheme. From the die efficiency and memory density viewpoints, Intel/Micron's CMOS circuit layout under the memory array has an advantage over Samsung's conventional die floor plan. Should Micron scale down the bitline pitch from 80 nm to 40 nm, it would be a memory density advantage to them. We can discuss further after circuit, device and waveform analyses on Intel/Micron's 3D NAND devices. ◆

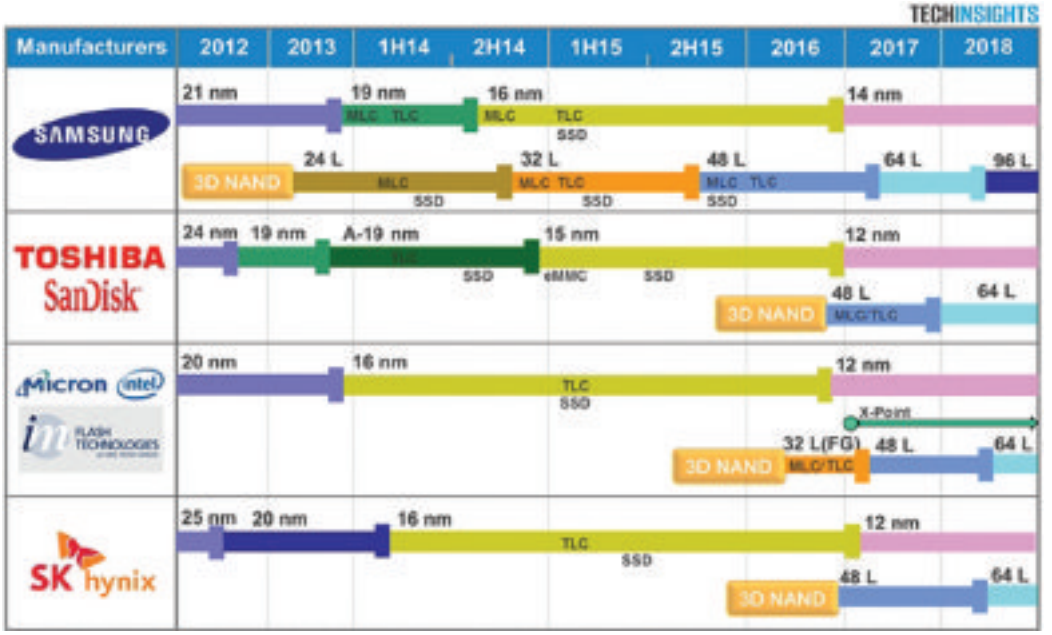

FIGURE 6. NAND technology roadmap.

CMP slurry optimization for advanced nodes

ADAM MANZONIE, **TODD BULEY**, **JIA-NI CHU** *and* **MIKE KULUS**, *CMP Technologies, Dow Electronic Materials, Newark, DE*

As advanced device manufacturers identify needs for new and additional CMP steps, new slurry solutions can deliver exceptional planarization and defectivity within a stable CMP process.

Advanced logic and memory device nodes demand significantly greater performance from chemical mechanical planarization/polishing (CMP) processes. Due to the fast growing number and increased diversity of non-metal CMP steps, new requirements are emerging, such as enhanced planarization efficiency, near-zero level defectivity and substantial reductions in process cost versus previous device nodes. Highly tunable and dilutable CMP slurries, in conjunction with matched CMP pads and processes are needed to achieve both technical and economic objectives. In advanced front-end-of-line (FEOL) processing, a variety of new CMP steps for different layer combinations, such as oxide, nitride and polysilicon, need to be polished and each layer requires different rates, selectivities and tight process control.

These varied requirements necessitate new slurry formulations. A new family of dielectric CMP slurries will be examined, which uses state-of-the-art colloidal silica abrasives paired with advanced additives to offer high removal rates, planarization efficiency and exceptionally low defect levels. These newly commercialized slurries are offered to customers in concentrate form to minimize overall cost-of-ownership (CoO). Point-of-use dilution minimizes abrasive concentration without sacrificing CMP performance and process stability.

CMP technical trends and challenges

The semiconductor industry continues to see growth in both logic and memory chip demand, driven by expanding applications in segments such as mobile, server, data processing, communications, consumer electronics, industrial and automotive. Scaling and cost reduction to extend Moore's Law continue to drive the needs for new transistor/device architectures and technologies like 3D FinFETs, 3D NANDs and 3D packaging. CMP is a critical enabler to deliver these technologies.

In advanced logic nodes, there are an increased number of CMP layers (e.g., 22-28 layers at 7nm compared to 12 layers

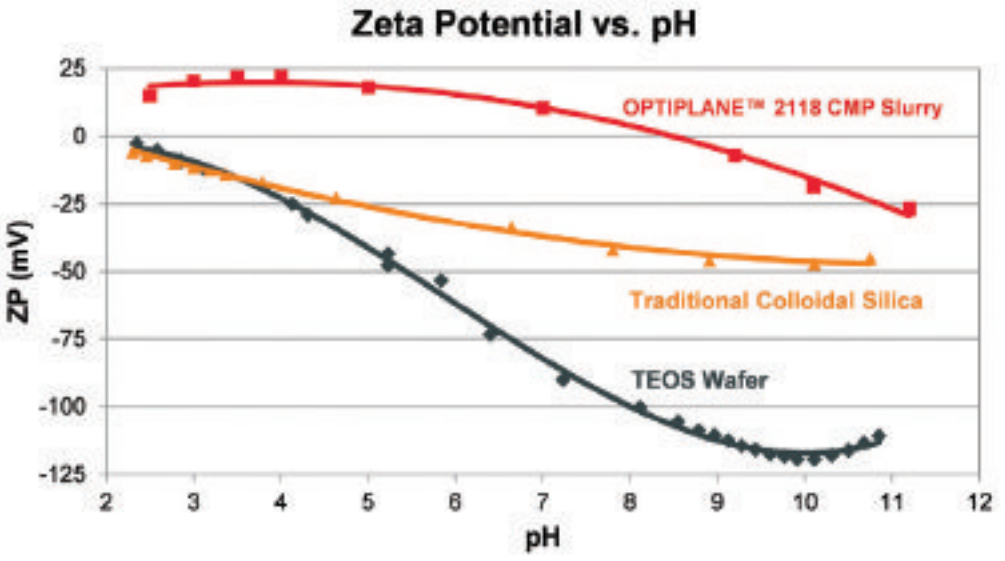

FIGURE 1. Zeta potential compared against pH for OPTIPLANE™ 2118 CMP slurry, traditional colloidal silica slurry and a TEOS wafer.

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for 45nm). New technologies and material layers have not only offered additional opportunities but also presented new challenges for CMP consumables and tool sets [1].

In addition to low defectivity and reduced cost-of-ownership, key performance drivers such as planarization efficiency (PE), erosion, and dishing must have tight process control with-in-die (WID) and with-in-wafer (WIW) uniformity. New innovations are needed for these emerging requirements.

In advanced logic processes, the Polysilicon Open Polish (POP) requires nitride and oxide removal to then stop on polysilicon [2]. There is a need for a tunable slurry and stable pad life to enable low gate height variation and dishing. Self-Aligned Contacts (SAC) processes require polishing nitride and stopping on oxide; this necessitates use of a highly-selective slurry (nitride: oxide selectivity > 50:1). Multiple buff steps may be needed to generate nitride residual free surfaces, making a tunable slurry a good solution. Polysilicon gate CMP polishes amorphous- or polysilicon and stops in the same film. Gate height variation across the wafer is critical. Managing final thickness requirements through end-pointing is very challenging; preferably, it requires a pad/slurry process with some level of self-stopping and with high planarization efficiency for gate height control and low surface roughness. With shallow trench isolation (STI), since the needle-like structure fins are getting thinner and taller, there is a need for slurry with extremely high selectivity (>100:1 Ox: SiN) to minimize the nitride loss. New flowable CVD (FCVD) films used for gap-fill (e.g., in STI processes) are sensitive to deposition and annealing, and could cause high defectivity (particles) and rate instability.

Advanced memory applications are also incorporating additional CMP process steps (e.g., buff steps may be performed in a one-platen process with hard pads for improved defectivity and global uniformity after an etch step). There are enormous technical challenges to enable further scaling of current DRAM cell size. With the need for additional CMP steps, DRAM processes continue to demand higher removal rates to enable greater throughput and reduce overall CoO.

For advanced nodes, one consistency is that there are additional new CMP steps for both logic and memory (primarily 3D-NAND). Slurries with significant, characterized tunability, enabling low defectivity and a lower CoO, are required for multiple applications.

New slurry formulations

Semiconductor manufacturers rely on strong collaboration with materials suppliers to identify or develop slurries that meet these new specific and stringent requirements. As an example, Dow has recently developed slurry options that address higher oxide removal, lower defectivity and lower cost-of-ownership in both ≤ 20nm DRAM and ≤ 28nm logic applications. For ≤ 14nm logic applications, different process requirements warranted an oxide slurry with high planarization efficiency and step height reduction combined with good polysilicon and nitride removal rates.

One of the commercial slurry products developed as a result of these requests is Dow's OPTIPLANE™ 2118 slurry, a low-abrasive, acidic pH silica slurry used for planarizing dielectric films in advanced CMP nodes. The enhanced CMP efficiency of this slurry is primarily enabled by a unique formulation that promotes favorable particle/wafer interaction. As demonstrated in the plot of zeta potential vs. pH (**FIGURE 1**), colloidal silica abrasives have the same negatively-charged surface as the polished TEOS films (throughout all measured pH ranges from pH 2 to pH 11) and thus exhibit undesirable electrostatic repulsion during

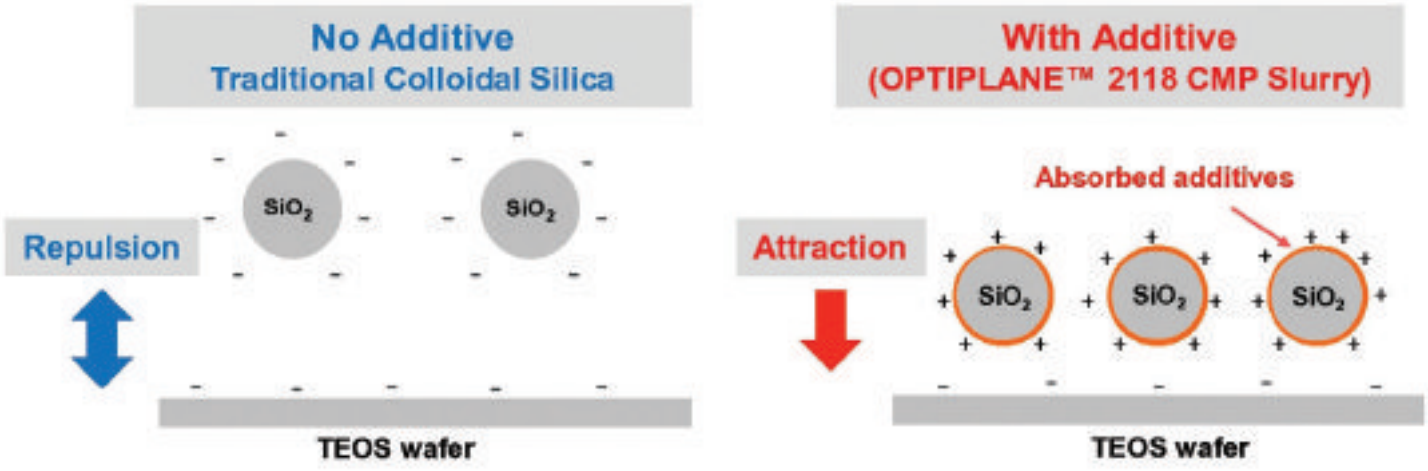

FIGURE 2. Silica abrasive-wafer interactions (a) without a charge modifying additive and (b) with a charge modifying additive.

polishing. With the introduction of proprietary additives in the formulation, the new slurry formulation possesses a significantly shifted isoelectric point (IEP) and creates a positively-charged surface at acidic pH via additive adsorption onto the silica particle surface. Under such conditions, the particles are intuitively attracted to the wafer surface such that the point-of-use (POU) abrasives can be significantly reduced without sacrificing removal rate performance (**FIGURE 2**). This optimized formulation reflects precise control of the particle-wafer interface in order to maximize the CMP benefit.

The slurry consists of spherical colloidal silica particles and a proprietary additive which adsorbs on to the abrasive particles and reverses the charge from negative to positive as illustrated in Fig. 2. The resulting electrostatic attractive forces between the abrasive particles (+ve) and dielectric film (-ve) leads to increased polishing efficiency (material removal rate/abrasive loading) as shown in **FIGURE 3**. For commercially available alkaline colloidal and fumed silica slurries, achieving high dielectric removal rates at low abrasive loading is extremely challenging, and hence they are generally used at >12 wt. % abrasive content for typical ILD applications. In comparison, this new slurry formulation can be used at 6 wt. % abrasive content at point of use (POU) for such applications.

A variety of defects are generated during oxide CMP processes, including scratches, particle residues, pad debris and roughness-related non-visible defects. Scratches are widely believed to be the most detrimental to wafer yields. The onset of scratch formation is often a result of an increased number of large particles in the polishing slurry.[2]

OPTIPLANE 2118 has been formulated with highly controlled spherical silica particles and produced with advanced filtration technology. This slurry exhibited ~ 45% scratch reduction when used on undoped silica glass (USG) wafers (**FIGURE 4**) and demonstrates > 70% scratch reduction on internal TEOS wafers compared to those polished with conventional fumed silica slurry under similar polishing processes. Such defect benefits, together with remarkably reduced pad wearing and polishing temperature, can be attributed to the use of low POU abrasive content and steric protection from additive adsorption on the polished surface.

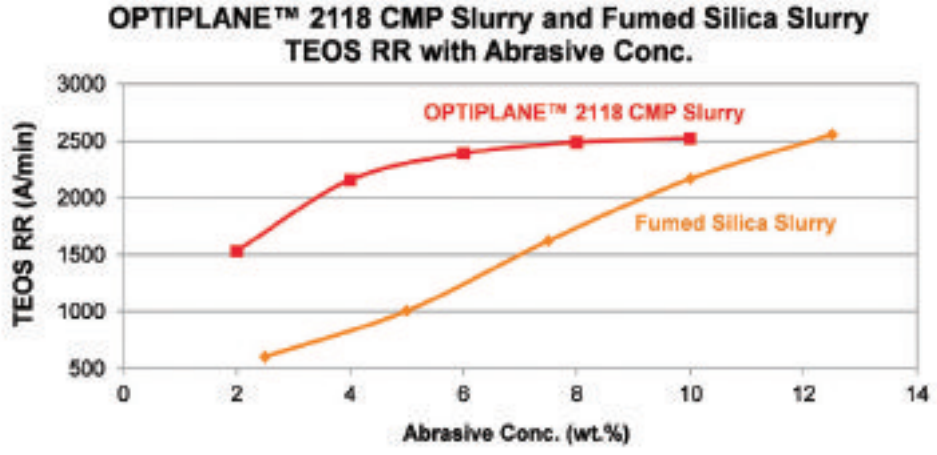

FIGURE 3. TEOS removal rate with silica abrasive loading for OPTIPLANE™ 2118 and fumed silica slurry.

While this new commercial slurry formulation is for dielectric applica-

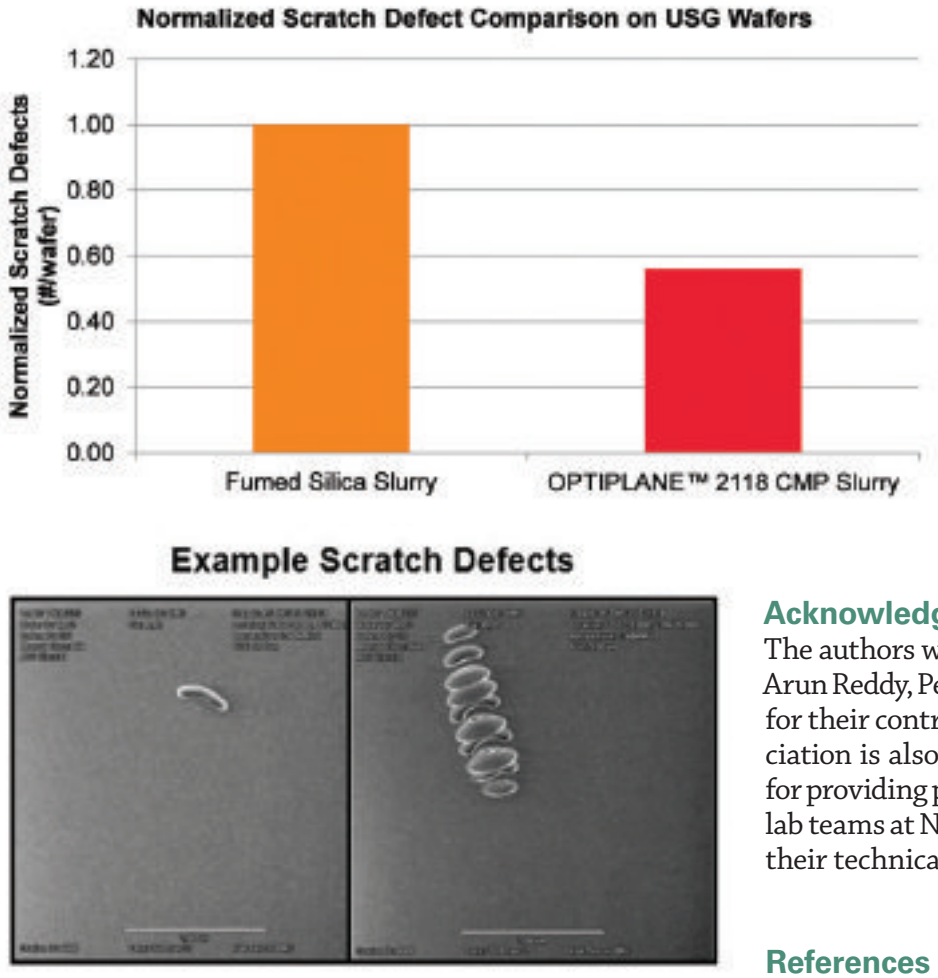

FIGURE 4. Normalized scratch defect comparison on USG wafers and examples of scratch defects.

tions, R&D teams are also developing and characterizing slurries with specific selectivities targeted at advanced FEOL CMP steps such as POP and SAC amongst others. Through internal development work and customer engagements, a wide range of rates and selectivities can be obtained from other formulations that will be commercialized in the OPTIPLANE 4000 series family.

Conclusion

As advanced device manufacturers identify needs for new and additional CMP steps, new slurry solutions can deliver exceptional planarization and defectivity within a stable CMP process. Advanced performance can be achieved while lowering process costs, through low point-of-use abrasive concentration, high removal rates and exceptional process consumable lifetime. New innovations in CMP slurries are helping to enable success at advanced nodes for next-generation manufacturing as the industry continues to move forward.

Acknowledgement

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Liquid to liquid ambient cooling systems for semiconductor tools

MARKO NIEMANN, *Regional Sales Director, Laird Engineered Thermal Systems, Cologne, Germany*

An overview of liquid-to-liquid cooling systems and their operating principles

Cooling and temperature control systems are used throughout semiconductor fabrication facilities. In fabrication facilities both large and small, hundreds to thousands of cooling systems are installed and operate continuously. The processes employed are usually setup as copy-exact, which means the process systems are developed and transferred from the OEM of the process tool. These crtitical production tools used in a semiconductor fabrication facilities are required to be reliable and easy to service to deliver minimum downtime. The same is required of the cooling systems that support them. Usually the cooling systems employed have a water-cooled evaporator instead of an air-cooled evaporator. A liquid-liquid unit is quieter than a liquid to air unit because a fan is not required. Even more important, the heat can be rejected by available general facility cooling water and the heat is not rejected into the air temperature conditioned environment. These cooling systems can be placed near the tool, hidden in a false floor or on the lower level in a sub-floor. Cooling systems are built to meet SEMI S2 or F47 standards. OEM customers vary in their demand according to their unique requirements, but compliance is mandatory and sometimes OEM customers ask to get certifications for SEMI S2 or F47, which includes for example seismic "protections." In these fabrication facilities a variety of liquid cooling systems are used including: compressor and thermoelectric based recirculating chillers.

Cooling systems

Liquid cooling systems are required to:

- Protect the tool process against chemical reaction by avoiding an unknown Wetted-Parts- Material-Mix
- Achieve a stable temperature, independent from facility water temperatures that can change
- Achieve a temperature below or above the facility water temperature
- Solve different temperature or fluid requirements at one tool with a multi-loop liquid cooling system

In semiconductor fabrication facilities, the required temperature control range varies from -80°C to +150°C. For the majority of applications, only one stable temperature set point is required. In the final chip test environment however, temperatures are required to vary in order to stress the chip. Here different temperature set points need to be reached with a single thermal management system. Due to the high-precision processes, tool manufacturers demand a very stable temperature environment. Typical of these requirements are +/-0.1K stability (e.g. for etching) to ±0.001K (e.g. for lithography) while cooling capacities can be up to several kilowatts.

In semiconductor fabrication facilities, custom multi-stage compressor based chillers are used to support cooling for very low temperature requirements. Most standard chillers utilized need some form of modification to meet semiconductor process facility requirements and may even require a water-cooled condenser. Some of the installation base also uses thermoelectric (19" rack) cooling systems, i.e. for etch applications, instead of compressor-based systems.

The cooling capacity demands and the range over which the system operates varies from a couple of hundred Watts (thermoelectric chiller and compressor based systems) to hundreds of Kilowatts (liquid-to-liquid cooling systems). The majority of the installed base uses liquid-to-liquid cooling systems that operate close to ambient and are based on a fluid-to-fluid heat-exchange principle.

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The cooling systems utilize facility water to prevent heat dissipation of the cooling unit from warming the cleanroom and destabilizing the process tool's thermal management system. These liquid-to-liquid systems keep the air quality level high by avoiding dust up introduced from the airflow of an air-to-air thermal management system. This consideration is independent of the location of the thermal management system. Due to the cyclic nature of the market, product requirements change and time to market is crucial. The cooling system solution developed is usually a custom product with a unique approach and design specific to the OEM.

Technical requirements

Cooling systems are often placed in the sub-fab, which means they are located one or two floors below the tool they are connected to. For cooling systems that use water as coolant, the height between the tool and the cooling system cannot exceed 10 meters, otherwise the height difference can cause the water to boil as the pressure is lower than the vapor pressure of water.

If the cooling system is placed at a lower level, the coolant circuit can function as a closed loop to the atmosphere. In this case, the cooling unit needs to incorporate a closed pressurized reservoir (7 PSI pressure cap) to minimize over flow conditions. The reservoir can be designed as a flow through reservoir or as a standpipe reservoir with a pressurized cap (**FIGURE 1**).

FIGURE 1. The reservoir can be designed as a flow through reservoir or as a standpipe reservoir with a pressurized cap.

A standpipe reservoir introduces additional fluid to the liquid circuit as required, whereas a flow-through reservoir continuously exchange fluid. It is important to know that the pump simply needs to overcome the height and pressure difference one-time during start-up in a closed loop system, as the supply and return lines will equilibrate given that they have the same length and diameter.

Material compatibility

In the semiconductor process environment, copper and brass are materials with limited compatibility due to their susceptibility to galvanic corrosion. Wetted parts, which come in direct contact with the medium (liquid), are typically made of stainless steel. These parts range from the complete plumbing circuit of the cooling unit to the process loop. Stainless steel is usually used in the process loop due its resistance to galvanic corrosion or because a special fluid is used that is not compatible with PVC, copper, and brass etc. When stainless steel is required, the heat exchanger, valves and the pumps will require special consideration. Occasionally, stainless steel may require additional passivation or a limited subset of stainless steel materials may be used.

If copper or brass is used to accomodate cost considerations, the material needs to be insulated to minimize the thermal impact on the system from outside thermal sources. Special particle free insulation may be required in this instance.

Special fluids used in the semiconductor environment include: di-electric fluids (Galden, 3M Novec), which are non-conductive. Special hoses and sealings need to be used for these fluids and special attention to handling is also required. These coolants run in a closed loop as the fluid vapor pressure is relatively low compared to water.

The use of de-ionized water is common. Copper or brass can be run up to 3 MOhm-cm resistivity if the set point temperature does not exceed 30°C for extended periods of time. However to ensure long lifetimes and for higher resistivity demands, the cooling system should be equipped with a nickel brazed or complete passivated stainless steel evaporator/heat-exchanger. The pumps should be stainless steel and all component parts in contact with the fluid should be made of passivated stainless steel to prevent corrosion. This is referred to as high-purity plumbing. In addition, a DI cartridge can be equipped with an indicator light or regulated through the cooling system and the DI level will be constantly measured and monitored keeping to a preset resistivity. The DI cartridge filters the ions out of the fluid and needs to be replaced to ensure its effectiveness.

Valves

If the unit is placed below the fabrication floor, an anti-siphoning package can be used to avoid backflow of the fluid and prevent overflowing the unit in event the

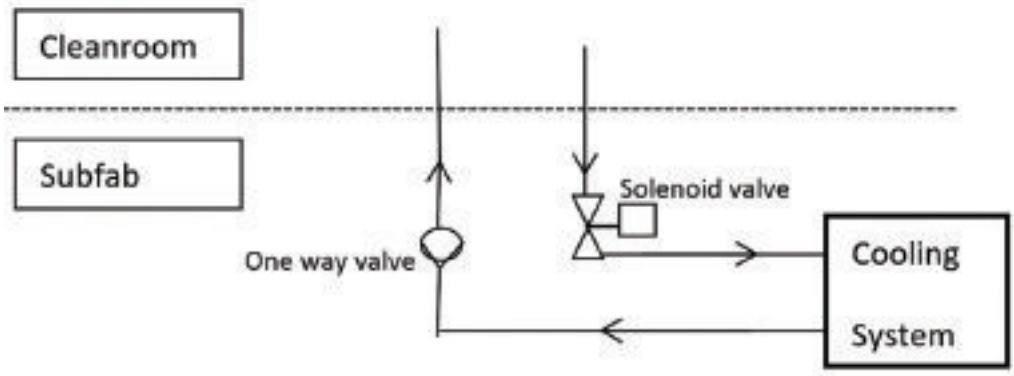

FIGURE 2. Instead of a one-way check valve, another solenoid valve can be used.

pump stops. The anti-siphoning package consists of a one-way check valve in the supply line and normally open solenoid valves triggered by the unit in the return line. The solenoid valve would close in case the pump stops and the one-way check valve allows for the flow in only one direction. Instead of a one-way check valve, another solenoid valve can be used, though this depends on the flow rate and size (**FIGURE 2**).

For a process facility, constant monitoring and control of the facility process water is required and modulating solenoid valves from Siemens or Bellimo need to be used. The valve diameter and actuating motor have to be sized correctly to achieve stable temperatures and trigger the correct switching cycles. Assuring this means the inclusion of a long-lasting actuator and facility water flowing through an acceptable pressure drop from the facility water supply and return. Sometimes three-way mixing valves are used. This allows for continuous flow into the facility water loop and adds cooling for the heat exchanger of the thermal management system when required. The constant flow back to the facility water loop avoids a water hammer in cases where it would close and reopen when cooling is required. Flow requirements can go be as high as hundreds of liters per minute.

Space consideration

Cleanroom costs can be up to $60,000 /m^2, therefore the chiller footprint is important and can have a costly impact. Semiconductor cooling systems should be stackable (stacked high) and preferable narrow to maximize space and minimize their impact on costs. Therefore the design of a cooling system's footprint needs to be closely examined. The system should also be located where it is easy to access from two sides. Routine maintenance on cooling systems is required to exchange components such as pumps, motors, valves and fans to maximize system uptime.

SEMI requirements

For a completed tool, OEMs require a SEMI S2 certification and sometimes a Semi F-47 certification in areas with high earthquake probability. As the SEMI S2 certification requires a high amount of documentation, subsystems like a cooling unit will finally be integrated into the tool. Most of the time it is sufficient to meet the intent of SEMI S2 and the OEM will do a full certification of the final tool with all sincorporated subsystems in their NRTL laboratory. Below are some items to consider when designing a cooling unit to meet SEMI S2 and F-47 standards.

SEMI S2:

- Drip tray must be large enough to hold 110% of the volume of the largest container in the cooling product
- EMO button and/or EMO connection
- Seismic brackets, seismic tie downs for standalone units
- A specific power connection setup depending on the power consumption

F-47:

- Continue to run during a power drop for a given time and fixed reduction of power

These requirements vary from customer to customer, but to some extent the certification is known to the manufacturer of the system.

If the unit is not placed below the fabrication facility flooring, the cooling system will instead be placed in the cleanroom or a grey room. Again, requirements here can vary drastically from customer to customer. If the cooling system, sub-assembly or any component is required to be in the cleanroom, then the entire assembly including each

component must be as clean as possible. This requires the entire manufacturing process to have a high level of attention to cleanliness. Debris, dust, burrs or chips occurring at every process step need to be examined and removed ideally after every fabrication step. The industry is quite sensitive to this.

After the final assembly, the cooling unit needs to go through a manual check with UV-light and wipe down for final cleaning with gloves. The unit is then double bagged and each bag needs to be labeled appropriately. There are suppliers who specialize in cleaning, to semiconductor standards, and this can be subcontracted. Since it contributes to the cost and lead-time, the level of detail used requires scrutiny.

Service

Selling a cooling unit into the semiconductor market requires long-term servicing agreements in the contract. If a product is qualified in one facility other facilities can take over the setup as a copy exact requirement and use the existing cooling solution. For this after-market service and support, full understanding of the end users demands is critical. Service and support needs to responsive. In the event a tool unexpectedly goes down, immediate support is required or the OEM can lose millions of dollars in revenue.

Once the tool is installed service needs to be done on-site on the same day of failure, as large cooling systems cannot be replaced easily or shipped back to manufacturer for repair. OEMs have moved away from purchasing redundant cooling systems as their processes are getting leaner and expenses are reviewed more closely. This puts the contractual emphasis on service and a global service infrastructure.

Ideally the manufacturer is aware of the service demands and support strategy of their customers. Systems today are designed to minimize the downtime and make use of hot swappable parts, such as pumps on rails or modular exchange of complete assemblies, including electrical control boxes.

Conclusion

A semiconductor fabrication facility's unique environment makes designing and building a liquid based cooling system one of the most challenging environments. Careful consideration is required not only for component selection, but also on the overall liquid cooling system unit and its integration with a semiconductor tool. Challenges designers face include the type of heat transfer mechanism utilized on the control and heat dissipation sides, material compatibility, valve control, cleanliness, space optimization, semi compliance and serviceability. These are all areas in need of attention to detail to properly ensure an optimized total cost of ownership. ◆

Light and sound: LEDs seen acoustically

By **TOM ADAMS**, *Sonoscan,Inc., Elk Grove, IL*

Many LED failures are the result of voids or other gap-type anomalies that block heat flow from the die.

A few years ago, the only commercial class of LED devices - HB-LEDs - was typically manufactured for applications requiring high reliability. The goal in most applications was to have few field failures, or at least few early-term field failures. Most HB-LED appliances were consequently fairly expensive.

Recently, however, the world of commercial LEDs has split into two parts: High power LEDs, which continue the tradition of reliability and high brightness in applications that require those characteristics, and mid power LEDs, which fill less demanding roles and tend to have lower initial costs. The principle behind mid power LEDS is that consumers will accept a somewhat higher failure rate in appliances having relatively large numbers of LEDs. The gradual loss of light output is balanced by the lower replacement cost.

Recent work has also shed light on the typical mechanisms of failure in both types of LEDs. Most failures in LEDs generally are related to power supply problems, but many failures are the result of voids or other gap-type anomalies that block heat flow from the die. Not surprisingly, there is good correlation between the total voided area beneath the die and the LED's junction temperature.

Acoustic micro imaging, usually in an automated format, is widely used to ensure LED quality, but with some changes to accommodate the new lower-price market. LEDs can be inspected acoustically in wafer form, as singulated devices before lens placement, and after lens placement by pulsing ultrasound into the heat sink at the bottom of the device (in failure analysis, they may also be inspected by grinding down much of the lens and pulsing ultrasound from above).

The primary change is that singulated mid power LEDs destined for lower-priced applications often need less intensive acoustic inspection. A percentage of such LEDs may be placed in trays and scanned by a system such as one of Sonoscan's C-SAM® tools, but this done as a non-destructive monitoring step to ensure that large numbers of defective devices are not slipping through rather than as 100% inspection to remove all defective devices. High power LEDs, however, may require 100% acoustic inspection.

The chief structural concerns in both mid power LEDs and high power LEDs are defects that are capable of blocking heat flow from the die. At a much lower power level, the situation is similar to that of IGBT modules, where heat from the die must reach a heat sink below the die to be dissipated. IGBTs generate far more heat than LEDs, but like IGBT modules both LED classes must dissipate heat downward. The lens above the LED is a very poor thermal transmitter.

In some designs the LED may be attached directly to the metal heat sink by a layer of solder. More often there is some type of printed circuit board between the die and the heat sink, with a thermal interface material (solder, grease, epoxy or an adhesive) between the die and the printed circuit board and between the printed circuit board and the heat sink.

Gap-type defects anywhere along the path from the die top the heat sink are the chief targets of acoustic imaging at these depths. A delamination or void as thin as 200Å will reflect virtually all of the ultrasound that strikes it; it is also a very efficient blocker of heat. The various gap-type defects have various somewhat overlapping names: a delamination suggests an interface that was once bonded but was somehow pulled apart; a void suggests a flattened (probably) air bubble; a non-bond suggests two surfaces that should have been bonded but never were, perhaps

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because of contamination of one of the surfaces. The actual etiology of a gap-type defect may more likely be revealed by knowledge of the processes used in packaging the LED than in observing the defect's structure.

FIGURE 1 is a high-resolution acoustic image of the solder layer between the substrate and the heat sink of an LED. The transducer of the acoustic micro imaging tool traveled back and forth just above this wafer at a speed that can exceed 1 m/s. Each second the transducer repeated its pulse-echo function thousands of times, pulsing ultrasound into the wafer and receiving the return echoes from material interfaces - homogeneous materials generate no echoes. The amplitude of each echo is recorded, and will determine the pixel color for that x-y location. Most material interfaces are between two solids, reflect roughly 20% to 80% of the ultrasound, and in monochrome images produce dark gray to light gray pixels.

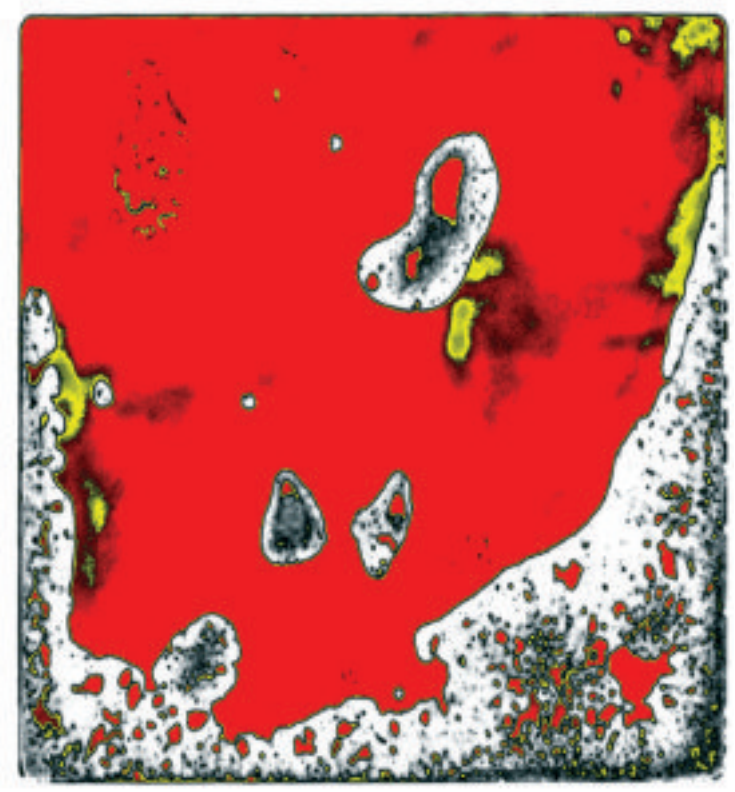

FIGURE 1. Red regions in this acoustic image are voids in the solder bonding the heat sink to an LED.

In the polychromatic color map used here, only in the white areas is the solder bonded to both the substrate and the heat sink. Red regions are not bonded, and thus contain an air gap and reflect virtually all of the ultrasound. More than half of the intended contact area is not bonded, a situation that might be acceptable for a mid power LED, but not for a high power LED. If the non-bonded area grows in size -- as they tend to do after thermal cycling -- this LED may overheat and fail. If it is a mid power LED assembly, though, the failure of some units may have been anticipated and overall performance may remain within acceptable limits.

When ultrasound and heat encounter the interface between a solid and a void, they react in somewhat different ways. A pulse of ultrasound is almost entirely reflected, with no change in its velocity. Essentially none of the pulse crosses the interface. Heat too is reflected, but also retarded. None of the heat crosses the the gap by conduction, although some heat may cross the gap by convection if the gap is filled with air. If the heat is reflected into a heat-retentive material, that material will heat up.

FIGURE 2 is the acoustic image of a single high power LED from which most of the lens above the die has been ground away to permit a less distorted acoustic view of the die and the die substrate. There is still some distortion caused by the remaining lens material; the die is actually rectangular, for example. But the critical depth - the interface between the lens and the die substrate - is clearly visible. In the color map used here, red indicates the very high reflection from a gap-type defect or delamination, in this case the interface between a solid (the lens) and the air in the gap. Like the red regions in Fig. 1, this delamination reflects nearly 100% of the ultrasound. What this image reveals, then, is that the lens is separated from the substrate by a gap. In itself, this

FIGURE 2. Removing part of the lens revealed the red delamination that could expand under the die.

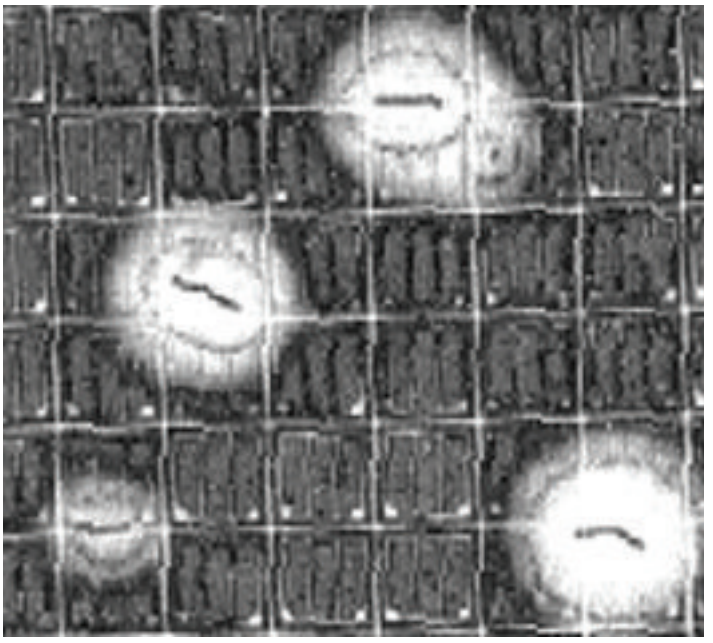

FIGURE 3. On this LED wafer, loose particles caused the rounded white voids.

delamination is relatively unimportant as a blocker of heat, because it lies beside and not below the die. But gaps such as this one tend to grow when exposed to thermal cycling; if this gap grows, it is likely to expand under the die and block significant heat. It if grows large enough, it can cause the die to overheat and fail.

Both high power and mid power LEDs are also imaged acoustically in wafer form in order to find widespread defects as early as possible. **FIGURE 3** shows one depth in one region of an HB-LED wafer. The circular or oval white areas formed as follows: at one point in the placing of layers on the wafer, small elongate structures broke free and moved away from their original positions. When the next layer was put down, these structures prevented some points on the layer from reaching the intended depth and thus caused a rounded air-filled void to form. The void is white where there is an interface between the air and the solid layer above. During later handling, smaller particles moved around in the free space of the void until they became trapped under the lower "ceiling" near the edge of the void. These particles form a broken ring around the particle that created the void. They are dark because the interface is between the solid "ceiling" and the solid particle. ◆

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Etch abatement needed to meet WSC goals

The World Semiconductor Council (WSC) is comprised of the semiconductor industry associations (SIAs) of the United States, Korea, Japan, Europe, China and Chinese Taipei. Its goal is to promote international cooperation in the semiconductor sector in order to facilitate the healthy growth of the industry from a long-term, global perspective. Formed in 1996, the WSC early on recognized the industry's obligation to responsibly manage its impact on the environment.

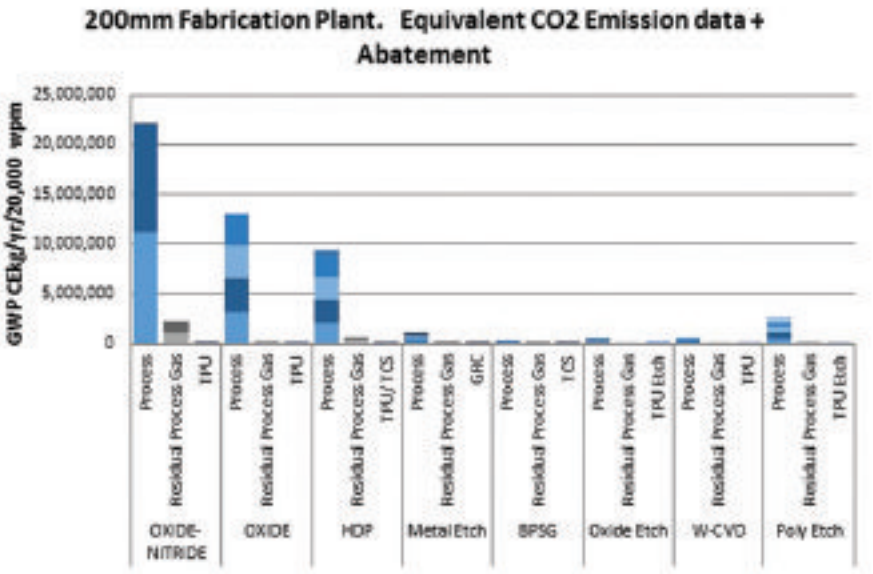

FIGURE 1. Global warming potential as carbon equivalent (in Kg) per year per 20,000 wafer starts per month. Etch processes are now the major opportunity to reduce harmful emissions in pursuit of WSC 2020 goals.

One of the council's first acts was the issuing of a voluntary industry target to reduce the emission of perfluorinated compounds (PFC) to 10 percent below their 1995 levels by 2010. PFCs are significant greenhouse gases (GHG) and many can persist for extended periods in the atmosphere. Given the significant growth of the semiconductor industry over this 15 year period, this was a very aggressive goal. By the end of the period, all member SIAs were able to report that they had met, and in many cases, significantly exceed the stated goal. This rather impressive achievement was accomplished by two key efforts. The first was the replacement of traditional CF4 and C2F6 CVD cleaning gases with NF3, which readily dissociates in a plasma to provide fluorine, an effective cleaning gas, which, though toxic, is not a greenhouse gas. The second was the widespread adoption exhaust gas abatement.

In 2011 the industry set new targets for 2020, which it summarizes as:

- The implementation of best practices for new semiconductor fabs. The industry expects that the implementation of best practices will result in a normalized emission rate (NER) in 2020 of 0.22 kgCO2e/cm2, which is a 30 percent NER reduction from the 2010 aggregated baseline.

- The addition of "Rest of World" fabs (fabs located outside the WSC regions that are operated by a company from a WSC association) in reporting of emissions and the implementation of best practices for new fabs.

- NER based measurement in kilograms of carbon equivalents per area of silicon wafers processed (kgCO2e/cm2), which will be the single WSC goal at the global level.

The original 2010 target focused primarily (and successfully) on emissions from chemical vapour deposition (CVD) processes. The main area for potential improvement now, as illustrated by the figure, is etch, especially in older 200mm fabs where etch processes may not have been fitted with PFC abatement devices. This is particularly true for etch processes making extensive use of CF4, which has a very high global warming potential over a 100-year timescale (GWP100) of 7350, due largely to its atmospheric half-life of 50,000 years. It is extremely stable.

Some are predicting a prolonging of the productive lifetimes of 200mm fabs in conjunction with projected growth as a result of the growing market for internet of things (IoT). Many IoT devices do not require cutting-edge production technology and can be economically produced in older fabs. In any case, the onus is on our industry to continue our efforts to reduce any adverse effects on the environment we all share. ◆

MIKE CZERNIAK, *Environmental Solutions Business Development Manager, Edwards*

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