

# Solid State TECHNOLOGY

**Insights for Electronics Manufacturing**

**How DSA and EUV Are  
Complementary**

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**Advancements in  
Spintronics**

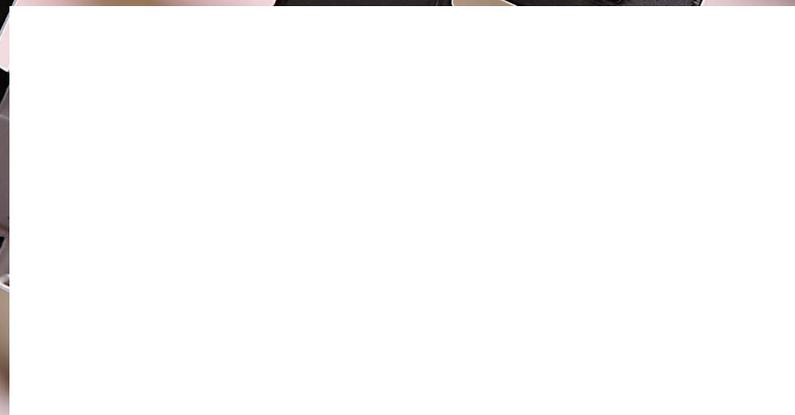
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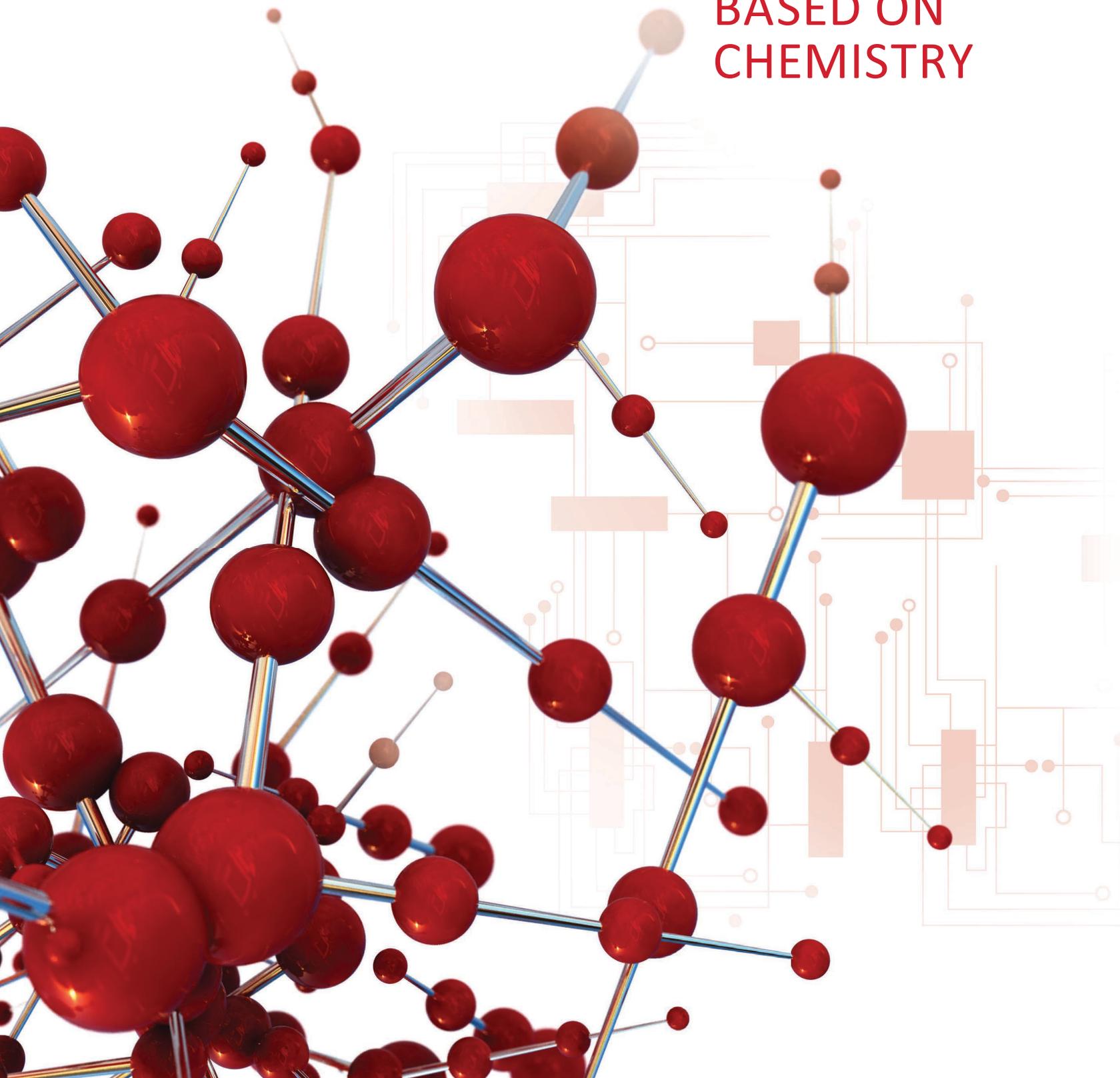
## Laser Marking Meets Diverse Challenges

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### LASER MARKING | Laser marking meets diverse challenges in fab and packaging

The basics of laser marking are reviewed, as well as current and emerging laser technologies.

*Dietrich Tönnies, Ph.D. and Dirk Müller, Ph.D., Coherent Inc., Santa Clara, CA*

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### LITHOGRAPHY | DSA and EUV: Complementary technologies to enable fine-pitch lithography

DSA and EUV should be envisioned as complementary, not competing, techniques that will eventually become mainstream for fine-pitch lithography.

*Douglas J. Guerrero, Ph.D., Brewer Science, Rolla, MO*

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### EMERGING DEVICES | Advancements in spintronics

Applications now include nanoscale Spintronics sensors that further enhance the areal density of hard disk drives, through MRAMs that are seriously being considered to replace embedded flash, static random access memories (SRAM) and at a later stage dynamic random access memories (DRAM).

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# Equipment forecast: \$49.4 billion

At a SEMICON West press conference, SEMI released its Mid-year Forecast. Worldwide sales of new semiconductor manufacturing equipment are projected to increase 19.8 percent to total \$49.4 billion in 2017, marking the first time that the semiconductor equipment market has exceeded the market high of \$47.7 billion set in 2000. In 2018, 7.7 percent growth is expected, resulting in another record-breaking year—totaling \$53.2 billion for the global semiconductor equipment market.

“It’s really an exciting time for the industry in the terms of technology, the growth in information and data and that’s all going to require semiconductors to enable that growth,” said Dan Tracy, senior director, IR&S at SEMI.

The average of various analysts forecast the semiconductor industry in general 12% growth for the year. “It’s a very good growth year for the industry,” Tracy said. “In January, the consensus was about 5% growth for the year and with the improvement in the market and the firmer pricing for memory we see an increase in the outlook for the market.”

The SEMI Mid-year Forecast predicts wafer processing equipment is anticipated to increase 21.7 percent in 2017 to total \$39.8 billion. The other front-end segment, which consists of fab facilities equipment, wafer manufacturing, and mask/reticle equipment, will increase 25.6 percent to total \$2.3 billion. The assembly and packaging equipment segment is projected to grow by 12.8 percent to \$3.4 billion

in 2017 while semiconductor test equipment is forecast to increase by 6.4 percent, to a total of \$3.9 billion this year.

“Based on the May outlook, we are looking at a record year in terms of tracking equipment spending. This is for new equipment, used equipment, and spending related to the facility that installed the equipment. It will be about a \$49 billion market this year. Next year, it’s going to grow to \$54 billion, so we have two years in a row of back to back record spending,” Tracy said.

In 2017, South Korea will be the largest equipment market for the first time. After maintaining the top spot for five years, Taiwan will place second, while China will come in third. All regions tracked will experience growth, with the exception of Rest of World (primarily Southeast Asia). South Korea will lead in growth with 68.7 percent, followed by Europe at 58.6 percent, and North America at 16.3 percent.

SEMI forecasts that in 2018, equipment sales in China will climb the most, 61.4 percent, to a total of \$11.0 billion, following 5.9 percent growth in 2017. In 2018, South Korea, Taiwan, and China are forecast to remain the top three markets, with South Korea maintaining the top spot to total \$13.4 billion. China is forecasted to become the second largest market at \$11.0 billion, while equipment sales to Taiwan are expected to reach \$10.9 billion.

—Pete Singer, Editor-in-Chief

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**Abstract Submission Deadline**  
October 31, 2017

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- CM01 Exploring Nanoscale Physical Properties of Materials via Local Probes
- CM02 *In Situ* TEM Characterization of Dynamic Processes During Materials Synthesis and Processing
- CM03 Investigating Nanostructures with X-Rays—Fundamentals and Applications
- CM04 *In Situ* and *Operando* Characterization of Materials and Devices by X-Ray and Neutron
- CM05 Strain Localization, Avalanches and Intermittent Deformation Mechanisms
- CM06 Frontiers in Functional Imaging in Aberration-Corrected Electron Microscopy

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- EP04 Reliability and Materials Issues of Semiconductor Optical and Electron Devices and Materials
- EP05 Emerging Light-Emitting Materials and Devices—Halide Perovskite and Low-Dimensional Nanoscale Emitters
- EP06 Materials, Devices and Systems for Machine Learning and Neuromorphic Computing
- EP07 Phase-Change Materials and Their Applications—Memories, Photonics, Displays and Non-von Neumann Computing
- EP08 Advanced Polymer Semiconductors—Key Properties and High-Performance Electronics

## ENERGY MATERIALS AND TECHNOLOGIES

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- EN02 Advances in Perovskite Solar Cell Devices and Applications
- EN03 Superconducting Materials—From Basic Science to Applications
- EN04 Advanced Materials for Carbon Capture and Other Important Gas Separations
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- EN06 Safer and More Energy-Dense Rechargeable Batteries
- EN07 Issues, Challenges and Opportunities in Actinide Materials
- EN08 Low-Cost Tandem Photovoltaic Cells
- EN09 Materials and Systems for Grid Energy Storage—Redox Flow Batteries
- EN10 Thermoelectric Materials, Devices and Applications
- EN11 Nanomaterials for the Water and Energy Nexus
- EN12 Hierarchical Materials for Nuclear Waste Management
- EN13 Capacitive Energy Storage—Fundamentals, Materials and Devices
- EN14 Materials Science and Device Engineering for Safe and Long-Life Electrochemical Energy Storage
- EN15 Novel Materials Physics of Perovskite Semiconductors
- EN16 Combining Materials, Technologies and Societal Awareness to Harvest Natural and Human-Made Energy Sources
- EN17 Fundamental Materials Science to Enable the Performance and Safety of Nuclear Technologies
- EN18 Multiscale Designing and Constructing Photocatalytic Materials for Solar Fuels
- EN19 Novel Inorganic Semiconductors for Optoelectronics and Solar Energy
- EN20 Deposition, Transformation and Reaction at Functional Interfaces for Electrochemical Energy Systems
- EN21 Next-Generation Solid-State Super Ion Conductors

## MANUFACTURING

- MA01 Advanced Materials for Analog and Digital Functional Printing
- MA02 Organic Electronics—Processing, Microstructure and Multifunctioning
- MA03 Directed Matter—Atom-by-Atom Assembly with Electron Beams and Scanning Probes
- MA04 Advances in Additive Manufacturing—Materials, Processes and Devices
- MA05 Dynamic Materials and Textiles for Next-Generation Clothing

## NANOMATERIALS

- NM01 Nanomaterials and Devices by Cluster Beam Deposition
- NM02 Active Colloids with Order
- NM03 Rational Designed Hierarchical Nanostructures for Photocatalytic Systems
- NM04 Porous Materials and Nanocomposites for Catalysis
- NM05 Colloidal Nanoparticles—From Synthesis to Applications
- NM06 Nanodiamonds—Synthesis, Characterization, Surface Chemistry and Applications
- NM07 Nanoscale Magnetic Structures and Materials
- NM08 Graphene Oxide Liquid Crystals and 2D Soft Material Systems
- NM09 Novel Approaches and Material Platforms for Plasmonics and Metamaterials
- NM10 Nanometallic Materials by Design
- NM11 Deformable Atomically Thin Materials—Mechanics, Materials and Devices
- NM12 Transitioning Quantum Dots from Benchtop to Industry
- NM13 Functionalization of Topological Materials

## SOFT MATERIALS AND BIOMATERIALS

- SM01 Soft Materials, Sensors, Electronics, Displays and Actuators—Functional Components for Soft Machines and Robots
- SM02 Immune Modulatory Materials—From Design to Translational Applications
- SM03 Engineered Functional Biointerfaces—From Electronics and Nanomaterials to Biocircuits and Bionanomaterials
- SM04 Understanding and Controlling the Structure and Function of Biomolecules at Material Interfaces
- SM05 Biomaterials for Tissue Interface Regeneration
- SM06 The Future of Neuroengineering—Relevant *In Vivo* Technology
- SM07 Functional (Bio)polymers in Energy and Environment Applications
- SM08 Smart Hydrogels and Living Materials

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### Don't Miss These Future MRS Meetings!

**2018 MRS Fall Meeting & Exhibit**  
November 25–30, 2018, Boston, Massachusetts

**2019 MRS Spring Meeting & Exhibit**  
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## Web Exclusives

### Latch up detection: How to find an invisible fault

Way back when, in the olden days (which, in the semiconductor industry, usually means last week), designers used visual inspections and manual calculations to check their layouts. The scale and complexity of today's designs mean that everything's changed now. Design margins have been driven to near-extinction by the market demand for lower power, higher reliability electronics. It doesn't really matter whether you're implementing a new design start at your current process node, migrating to your "next" node, or adding new functionality to a well-trusted design, meeting those time-sensitive tapeout schedules and tight time-to-market windows means you need more than a good eye and a quick hand on the calculator.

<http://bit.ly/2wvfkgc>

### Insights from the Leading Edge: ASE Embedded Packaging Solutions

At the recent IMAPS Carolina Chapter meeting, Rich Rice of ASE gave an update presentation on "Embedded Packaging Solutions." Specifically:

- SESUB- Semiconductor Embedded In Substrate
- aEASI -Advanced Embedded Active System Integration
- FOWLP- Fan Out Wafer Level Package

<http://bit.ly/2wvt6j0>

### Industry upswing: End of cycles?

This is an exciting year to be in the semiconductor industry as Ajit Manocha, president and CEO of SEMI highlighted at SEMICON West; semiconductor-related companies are trading at all-time highs, and record device shipments and revenues as well as equipment revenues are expected.

<http://bit.ly/2vociGM>



### Semiconductor industry capital spending forecast to jump 20% in 2017

IC Insights has revised its outlook for semiconductor industry capital spending and presented its new findings in the August Update to The McClean Report 2017. IC Insights' latest forecast is for semiconductor industry capital spending to climb 20% this year.

<http://bit.ly/2ipZWMx>

### Join us in 2018!

The ConFab 2018 is returning to Las Vegas. The ConFab will be held May 20-23, at THE COSMOPOLITAN of LAS VEGAS, a fabulous property, with state-of-the-art conferencing facilities. Regarding the conference program and agenda, we will be covering a lot of the emerging and leading-edge technologies, and applications that are driving the semiconductor Industry and related industries that are involved with solid-state electronics and device manufacturing.

<http://bit.ly/2gc1UiO>

### Insights from the Leading Edge: ASE Tech Forum at Nijmegen Part 1

At the recent ASE Tech Forum in Nijmegen chaired by John Marc Yannou, Ivanovik of Yole gave a nice overview of the industry presentation titled "Advanced Packaging Industry 2017."

<http://bit.ly/2wEXbNv>

### Mid-year global semiconductor sales up 21% compared to 2016

The Semiconductor Industry Association announced worldwide sales of semiconductors reached \$97.9 billion during the second quarter of 2017, an increase of 5.8 percent over the previous quarter and 23.7 percent more than the second quarter of 2016.

<http://bit.ly/2vwlEzw>



# CONNECT

## SEMICON Europa 2017:

# Empowering Innovation and Shaping the Value Chain

For the first time SEMICON Europa will co-locate with productronica in Munich, Germany creating the strongest single event for electronics manufacturing in Europe, and broadening the range of attendees across the electronics supply chain. The co-location with productronica embodies the SEMI global strategy to connect the breadth of the entire electronics supply chain.

SEMICON Europa events will expand attendee opportunities to exchange ideas and promote technological progress featuring the most advanced and innovative electronics manufacturing platform in Europe.

Convenient and central location in Europe, Munich will attract tens of thousands of international visitors: Together to connect for electronics business!

**Key Segments at SEMICON Europa 2017:** Materials, Semiconductor Front-end and Back-end Manufacturing, Advanced Packaging, MEMS/Sensors, Power and Flexible Electronics, applications such as the Internet of Things (IoT), automotive and MedTech.

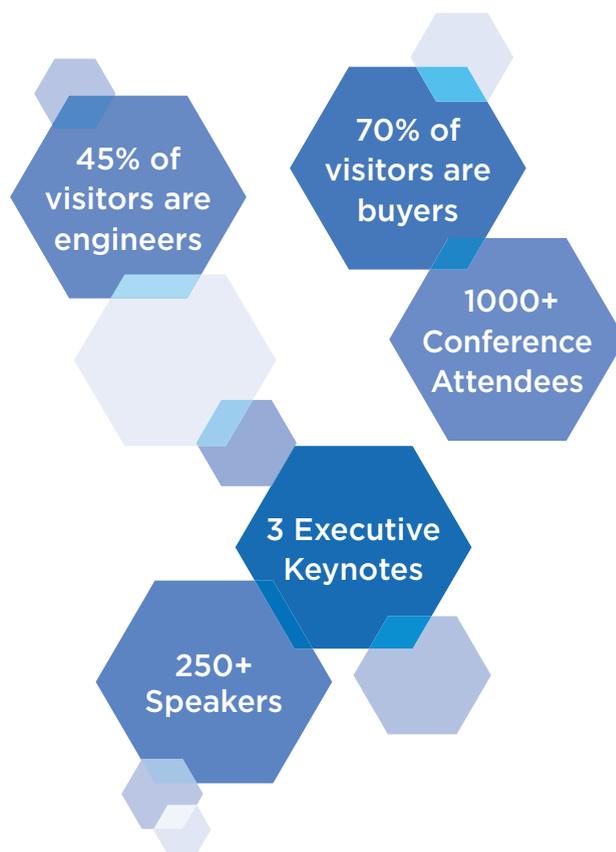
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## worldnews

**ASIA - TowerJazz and Tacoma** announced a partnership for a new 8-inch fabrication facility in Nanjing, China.

**USA - GLOBALFOUNDRIES** announced that it has demonstrated silicon functionality of a 2.5D packaging solution for its high-performance 14nm FinFET FX-14 integrated design system for application-specific integrated circuits (ASICs).

**ASIA - ROHM Semiconductor** announced the availability of the industry's smallest class (1608 size) of 2-color chip LEDs.

**USA - NanoString Technologies, Inc. and Lam Research Corporation** announced a strategic collaboration to develop NanoString's proprietary Hyb & Seq next-generation sequencing platform.

**ASIA - Samsung Electronics Co., Ltd.** announced a new V-NAND (Vertical NAND) memory solutions and technology that will address the pressing requirements of next-generation data processing and storage systems.

**EUROPE - HEIDENHAIN** announced the offering of a new angular positioning system for metrology and micromachining.

**USA - NXP Semiconductors N.V.** announced a \$22 million dollar program that expands its operations in the United States.

**ASIA - Rudolph** announced it is expanding its presence in China for AMOLED display lithography.

**EUROPE - University of Groningen** scientists led by physics professor Bart van Wees have created a graphene-based device, in which electron spins can be injected and detected with unprecedented efficiency.

**USA - Covalent Metrology** announced that it has consolidated operations in a larger facility located in Santa Clara, CA.

## Silicon wafer shortage starts in 2018

TECHCET CA, an advisory service firm providing electronic materials information, announced that the silicon wafer supply for semiconductor device fabrication is forecasted to appreciably lag demand starting next year, and could remain in shortage through the year 2021 despite investments in China. Silicon wafer area demand is forecasted to steadily increase at a CAGR of ~3.1% over the 2016-2021 period to reach over 13,000 million square inches (MSI). Executives of silicon wafer suppliers have stated that average selling prices have remained too low to allow for investment in 300mm expansions, as detailed in a quarterly update to the TECHCET Critical Materials Report, "Silicon Wafers Market & Supply-Chain."

The silicon wafer supply-chain is dominated by two suppliers—Shin-Etsu Handotai and SUMCO—combining to capture almost two-thirds of the global wafer market in 2016, and the top five representing over 92% of total revenues. The silicon wafer market is maturing as evidenced by recent mergers and acquisitions, the two most notable being the

acquisition of SunEdison Semi by GlobalWafers (Taiwan) and the assumption of majority ownership of LG Siltron by SK Holdings (Korea).

"Over the last five years, the average selling price per square inch of semiconductor-grade silicon wafers has declined by about a third and more than a half from the 2007 level," explained Michel Walden, lead author of the report and senior technology analyst with TECHCET. "However, current tightness in the supply-chain has led to greater stability and even price increases in some cases, all of which is likely needed for the long-term health of the wafer suppliers."

Over the past few years, silicon suppliers decommissioned roughly 25% of the peak capacity for 200mm wafers. Of the remaining 200mm capacity, roughly 65% of the total demand is for epitaxial (epi) wafers, and a series of epi service companies have embraced this opportunity and provide a variety of layer configurations for their customers.

## What is the status of III-N technology?

The III-N semiconductor family has attracted significant research attention over the last 25 years, resulting in intensive patenting activity, with a substantial increase during the past decade. More than 80,000 patents and patent applications related to III-N technology have been published worldwide since the early 1990s, announce KnowMade's analysts. In such a dynamic III-N market, it is essential to understand the technology challenges and the market needs as well as to track related patents. Therefore, industrial companies need to anticipate changes, quickly detect business opportunities, mitigate risks, and make strategic decisions.

KnowMade, System Plus Consulting and Yole Développement, all part of Yole Group of Companies combine their expertise to develop relevant services and high-added value reports dedicated to the III-N technology. Based on

technology changes, market evolution and IP strategy, the group is covering the overall GaN industry from LED, diode and laser to RF applications as well as other III-N materials. What is the status of the III-N semiconductor field? Yole Group of Companies proposes an overview of this industry.

The Technology Intelligence & IP strategy consulting company, KnowMade presents a new service to follow the industry evolution and get a comprehensive understanding of the technical challenges and company's market positioning through an IP approach. III-N Patent Watch service is monthly updates dedicated to the III-N related patents. With a useful Excel database presenting the latest patent applications, newly granted patents, expired or abandoned, patent transfers and

Continued on page 9

# Lam Research takes uniformity control to the edge

Chipmakers want every part of the wafer to produce, or yield, good die. Advances in process technologies over the years have just about made this a reality, even as feature dimensions continue to shrink and devices grow ever more complex. Now, the last frontier is improving yields at the edge of the wafer – the outer 10 mm or so – where chemical, physical, and even thermal discontinuities are simply much harder to control. Complicating matters, current strategies used to manage these edge issues involve tradeoffs between yield and manufacturing costs that result in less than ideal fab economics.

## Edge challenges

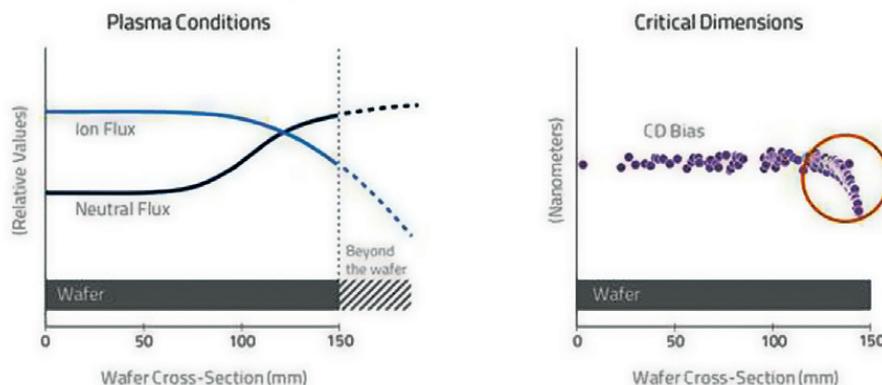
Taking a closer look at the wafer's edge, where up to ~10% of the die may be located, there are several issues at play that can impact yield. In all plasma etch reactors, the abrupt end of the wafer surface creates inherent electrical discontinuities at the edge region, forming voltage gradients that bend the plasma sheath. This, in turn, changes the direction of the plasma's components (ions and neutrals), which impacts etch results and causes unwanted variability. In the case of 3D NAND devices, for example, this change in the plasma conditions at the wafer's edge can cause tilted etch profiles or prevent features from being completely etched. In addition to affecting tilt angle, these edge effects can result in non-uniform critical dimensions (CDs) or changes in local overlay metrics.

Another challenge is that process drift creates CD uniformity and selectivity problems over time. As a way to manage this, chipmakers often add more chamber wet cleans to restore the equipment to a standard condition. However, this approach significantly reduces productivity because the chamber is not available for processing wafers during this maintenance. In addition, as process margins get tighter, more frequent wet cleans are required, which increases operational costs.

## Corvus solution

Lam's new Corvus technology provides a novel capability to smooth out extreme edge discontinuities and enhance edge performance. It offers the ability to tune the plasma sheath at the edge to produce a constant, user-defined etch rate and ion angle. For example, etch rate can be tuned to be faster or slower at the edge relative to the rate over the rest of the wafer. With 3D NAND applications, Corvus technology has demonstrated the ability to minimize plasma sheath drift, preventing detrimental feature tilting at the wafer's edge. Tuning to within 1.5 mm of the edge, the new technology

## Edge Discontinuities Lead to Variability



can correct for inherent process variation in the edge region as well as for incoming film variations to optimize die yield. Furthermore, with Corvus, every wafer sees the same edge conditions for optimal yield, eliminating previously seen systematic wafer-to-wafer yield variability.

Corvus technology not only improves across-wafer uniformity, it also greatly reduces wafer-to-wafer and chamber-to-chamber variability and eliminates the historical tradeoffs among yield, operational flexibility, and cost. Customers have reported die yield improvements of 0.5-2% per wafer, which can be a significant advantage – especially when you consider how many thousands of wafers chipmakers process every day. Additionally, Corvus has demonstrated the ability to provide higher and more consistent yield over a longer period. It also greatly enhances productivity and lowers overall fab operating costs for high-volume manufacturing by requiring fewer chamber wet cleans. The new technology is being used for advanced patterning, mask open, and other challenging conductor etch applications where reducing variation in CD, profile, or selectivity and improving productivity helps enable continued scaling.

The new capability provided by Corvus complements Lam's Hydra® technology, which enables fine tuning of within-wafer uniformity and actively compensates for incoming variation. Together, these advanced process control technologies are reducing variability across the entire wafer surface, improving yield, and enabling the production of next-generation logic and memory devices.

Welch Foundation, the Army Research Office and the National Science Foundation supported the research.

That kind of tool could be commercially available within about two years, and health monitoring and diagnostic tools could be available within about five years, Javanmard said. ◀

## New ultrathin semiconductor materials exceed some of silicon's "secret" powers

The next generation of feature-filled and energy-efficient electronics will require computer chips just a few atoms thick. For all its positive attributes, trusty silicon can't take us to these ultrathin extremes.

Now, electrical engineers at Stanford have identified two semiconductors – hafnium diselenide and zirconium diselenide – that share or even exceed some of silicon's desirable traits, starting with the fact that all three materials can "rust."

"It's a bit like rust, but a very desirable rust," said Eric Pop, an associate professor of electrical engineering, who co-authored with post-doctoral scholar Michal Mleczko a paper that appears in the journal *Science Advances*.

The new materials can also be shrunk to functional circuits just three atoms thick and they require less energy than silicon circuits. Although still experimental, the researchers said the materials could be a step toward the kinds of thinner, more energy-efficient chips demanded by devices of the future.

### Silicon's strengths

Silicon has several qualities that have led it to become the bedrock of electronics, Pop explained. One is that it is blessed with a very good "native" insulator, silicon dioxide or, in plain English, silicon rust. Exposing silicon to oxygen during manufacturing gives chip-makers an easy way to isolate their circuitry. Other semiconductors do not "rust" into good insulators when exposed to oxygen, so they must be layered with additional insulators, a step that introduces engineering challenges. Both of the diselenides the Stanford group tested formed this elusive, yet high-quality insulating rust layer when exposed to oxygen.

Not only do both ultrathin semiconductors rust, they do so in a way that is even more desirable than silicon. They form what are called "high-K" insulators, which enable lower power operation than is possible with silicon and its silicon oxide insulator.

As the Stanford researchers started shrinking the diselenides to atomic thinness, they realized that these ultrathin semiconductors share another of silicon's secret advantages: the energy needed to switch transistors on – a critical step in computing, called the band gap – is in a just-right range. Too low and the circuits leak and become unreliable. Too high and the chip takes too much energy to operate and becomes inefficient. Both materials were in the same optimal range as silicon.

All this and the diselenides can also be fashioned into circuits just three atoms thick, or about two-thirds of a nanometer, something silicon cannot do.

"Engineers have been unable to make silicon transistors thinner than about five nanometers, before the material properties begin to change in undesirable ways," Pop said.

The combination of thinner circuits and desirable high-K insulation means that these ultrathin semiconductors could be made into transistors 10 times smaller than anything possible with silicon today.

"Silicon won't go away. But for consumers this could mean much longer battery life and much more complex functionality if these semiconductors can be integrated with silicon," Pop said.

### More to do

There is much work ahead. First, Mleczko and Pop must refine the electrical contacts between transistors on their ultrathin diselenide circuits. "These connections have always proved a challenge for any new semiconductor, and the difficulty becomes greater as we shrink circuits to the atomic scale," Mleczko said.

They are also working to better control the oxidized insulators to ensure they remain as thin and stable as possible. Last, but not least, only when these things are in order will they begin to integrate with other materials and then to scale up to working wafers, complex circuits and, eventually, complete systems.

"There's more research to do, but a new path to thinner, smaller circuits – and more energy-efficient electronics – is within reach," Pop said.

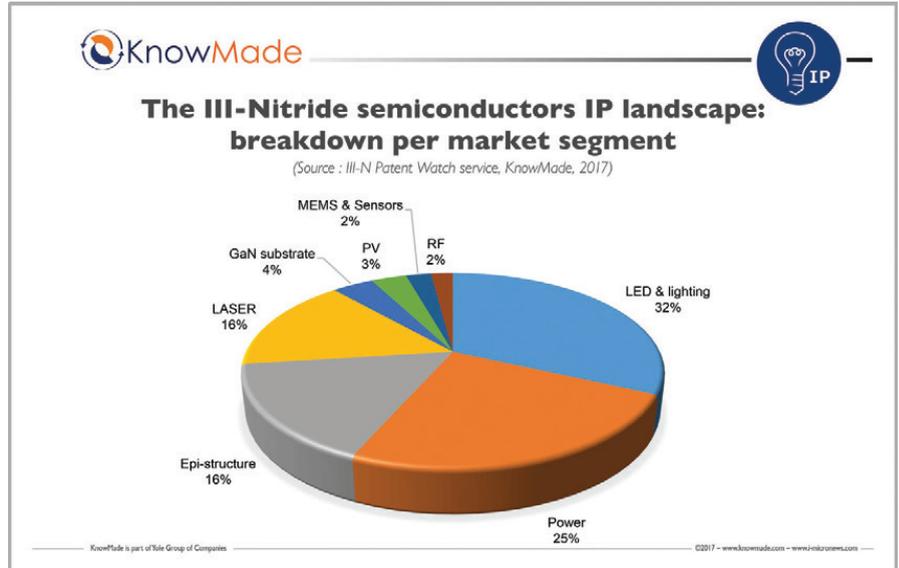
Additional Stanford contributors to this research include: Chaofan Zhang, Hye Ryoung Lee, Hsueh-Hui Kuo, Blanka Magyari-Köpe, Robert G. Moore, Zhi-Xun Shen, Ian R. Fisher, and Professor Yoshio Nishi.

The work was supported by the Air Force Office of Scientific Research (AFOSR), the National Science Foundation, Stanford Initiative for Novel Materials and Processes (INMP), the Department of Energy (DOE) Office of Basic Energy Sciences, Division of Material Sciences, and an NSERC PGS-D fellowship. ◆

patent litigation and more, the Patent Watch service is a powerful tool of strategic analysis to track competitors, partners and customers and identify new entrants. Patent Watch also allows companies to identify business opportunities as well as analyze the risks for business development.

Under this service, the technology intelligence and IP strategy consulting company is tracking the IP of more than 100 players involved in the III-N sector. The take-off of patenting activity took place in the 2000s with a first wave of patent publications. A second wave started in 2010 while first commercial GaN products, collaborations, mergers, and acquisitions emerged... III-N Patent Watch service from KnowMade help the companies to get a clear view of the market evolution, understand the IP strategies, and anticipate the industry changes and much more.

In parallel, System Plus Consulting and Yole Développement are strongly involved in the GaN industry, representing the biggest market of the III-N semiconductor materials family. Both companies propose a huge collection of reverse



engineering and costing analyses and technical and market reports to highlight the technology innovations, markets adoption and give a quantification of these markets. According to Yole Développement, the global GaN market including LED, RF, Power and laser, was estimated to be worth US\$16 Billion in 2016 and should reach US\$20 Billion by 2020 at a 5% CAGR between 2016 and 2020. Indeed the overall GaN industry is today mainly boosted by newly emerging markets. ◀

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# Sony's stacked image sensor



PHIL GARROU,  
Contributing Editor

It has been nearly a decade since Toshiba announced the use of backside TSV's to miniaturize CMOS image sensors. More recently, In Feb 2017 at the IEEE International Solid-State Circuits Conference (ISSCC), Sony announced the Industry's first 3-Layer Stacked CMOS Image Sensor (90nm generation back-illuminated CIS top chip, 30 nm generation DRAM middle chip, and a 40nm generation image signal processor (ISP) bottom chip for Smartphones. Sony further revealed that that the CIS is made in a 90 nm, 1 Al, 5 Cu technology, the DRAM is a 1 Gb, 30 nm (3 Al, 1 W) part, and the ISP is a 40 nm, 1 Al, 6 Cu device.

This newly developed sensor with stacked DRAM delivers fast data readout speeds, making it possible to capture still images of fast-moving subjects with minimal focal plane distortion as well as super slow motion movies at up to 1,000 frames per second (approximately 8x faster than conventional products) in full HD (1920x1080 pixels).

At the recent Mobile World Congress, Sony announced adoption of this technology their Xperia XZ Premium and XZs phones, with the Motion Eye camera system capable of 960 fps.

Dick James, writing in EE Times, reports on cross-sections of the rear-facing camera chip which contains the 3 layered stack. The CMOS image sensor (CIS) is

mounted face-to-back on the DRAM, which is face-to-face with the image signal processor (ISP). The cross section below is direct for Sony. Since the DRAM is sandwiched between the CIS and the ISP, the high-speed data has to go through the memory chip to the ISP, and then back-and-forth until it is output through the I/F (interface) block of the ISP, at a conventional speed suitable for the applications processor" reports James who then adds that since the DRAM die also has the CIS row drivers on it, it must be "designed as a custom part, and is not one of the TSV-enabled (TSV = through-silicon via) commodity DRAMs."

James has also shown the TSV layer connections between the two chips (see below). The cross section below shows two layers of TSVs connecting a 6-metal stack in the CIS to the M1 of the DRAM die. They did not have a cross-section of extended TSVs joining the CIS directly to the ISP, though there are TSVs through the DRAM to the top metal of the ISP.

In an interesting article by Ray Fontaine of TechInsights he notes that "the development of low-temperature wafer bonding and various wafer-to-wafer interconnect techniques have been key enablers for stacked image sensors. Two-die stacks, comprising a back-illuminated CIS and mixed-signal image signal processor (ISP), have emerged as the dominant configuration for leading smartphone camera chips. The CIS portion can be considered a 'dumb' chip carrying only an active pixel array. Most of the signal chain and digital processing is partitioned onto the ISP and systems application processor."

The table compares technologies that have been implemented since 2013.

With Sony's inclusion of DRAM into the CIS stack, I can safely predict that Omnivision and Samsung will not be far behind. ◀

Chip Vendor	Year	Stacked CIS Foundry/Gen.	Stacked ISP Foundry/Gen.
Sony	2013	Sony 90 nm	Sony 65 nm
Sony	2014	Sony 90 nm	TSMC 40 nm
Sony	2016	Sony 90 nm	TSMC 28 nm
Omnivision	2015	XMC 65 nm	XMC 65 nm
Omnivision	2016	TSMC 65 nm	TSMC 65 nm
Samsung	2015	Samsung 65 nm	Samsung 65 nm
Samsung	2016	Samsung 65 nm	Samsung 28 nm HKMG
Sony	ISSCC 2017	90 nm CIS*	30 nm DRAM* 40 nm ISP*

\*announced Feb 2017

Table 2. Noteworthy Stacked Chip CIS/ISP Configurations

## Packaging



# How low can we go?

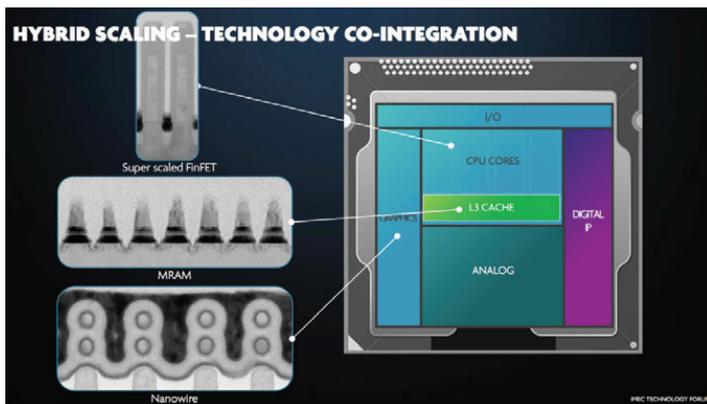


ED KORCZYNSKI,  
Sr. Technical Editor

In the advanced CMOS technology programs ongoing in the Belgium city of Leuven, IMEC works to extend the building-blocks of integrated circuits (IC). On the day before the opening of SEMICON West 2017, the invitation-only IMEC Technology Forum provided an update on the emerging opportunities in semiconductor technology and smart electronics systems. An Steegen, Executive VP Semiconductor Technology & Systems, provided the update on how small we can scale CMOS devices over the next 5-10 years. Taller finFETs will likely be used along with nano-wire FETs (NW-FET) by industry, and researchers see ways to cost-effectively combine both in future optimized System-on-Chips (SoC).

with forming fins and so could be relatively easily integrated with finFETs for co-integrated hybrid CMOS.

“Today, this SoC is processed in one technology which means it’s sub-optimal for certain blocks on the SoC,” explained Steegen. “So imagine a future where you can choose the preferred technology for each block. I would choose finFETs for those blocks that need drive current, while I would choose nano-wire-FETs for those blocks that need more density and lower power. I would for example choose a magnetic RAM to replace my cache memory. I can optimize each sub-block for a preferred technology. Now I can do more, like sprinkle in low-energy devices like tunnel-FETs or spin-devices or 2D-materials as low-energy switches.”



System-Technology Co-Optimization (STCO) for future System-on-Chip (SoC) designs could integrate finFETs with Nano-Wire FETs (NW-FET) and Magnetic Random Access Memory (MRAM) for optimized performance. (Source: IMEC)

## Super-vias and Rutherford rails

Design-Technology Co-Optimization (DTCO) is IMEC’s term for new interconnect technologies to allow for simpler or more-compact designs. IDTCO process-scaling boosters are needed to stay with the pace of aggressive design rule targets. “We’re working on super-vias that connect more than one metal to the other and can jump a number of levels, and buried rails to support finFETs in standard-cell libraries,” explained Steegen during ITF2017.

Super-vias could be cobalt plugs that connect more than two metal levels within on-chip multi-level interconnects. The cobalt plugs would be nominally 20nm diameter and 105nm deep, and connected to a dual-damascene upper metal line. Low-k dielectric of  $k=2.55$  uses thin silicon carbon nitride (SiCN) for definition between the damascene levels.

Ruthenium rails (Rutherford rails) would be buried in a front-end dielectric layer to provide electrical contacts below finFETs for 42nm CGP and 21nm MP needed for IMEC 3nm-Node (I3N) devices. Ruthenium rails 30nm deep and 10nm wide do not need complex barrier layers and should provide sufficient current flow for either finFETs or NW-FETs.

IMEC is also working on materials R&D to extend the performance of 3D-NAND. Steegen said,

“At IMEC we are working on improving the performance of that Flash device by introducing high-mobility channels, also by engineering the dielectric trapping layer with a barrier that can help improve the erase window and also the retention.” ◀

“Existing finFET technology can scale to the 5nm-node,” explained An Steegen at ITF 2017 in Antwerp, Belgium. “However, at the 3nm-node it looks like the nano-wire is comparable in performance to the finFET, but it has an additional advantage in that the nanowire is a better electro-statically controlled device so it enables gate-length scaling more than the finFET. So the contacted gate pitch (CGP) of a nano-wire can scale further than a finFET, because below ~40 nm CGP a finFET loses electro-static control which a nano-wire does not.”

While it is given that a nanowire has better electro-static control compared to a finFET, the basic trade-off is that of reduced drive current. The **Figure** shows that IMEC sees the possibility of System-Technology Co-Optimization (STCO) of future system-on-chip (SoC) designs using hybrid semiconductor technologies. IMEC’s basic process flow for NW-FETs starts

## Semiconductors



# Laser marking meets diverse challenges in fab and packaging

**DIETRICH TÖNNIES**, Ph.D. and **DIRK MÜLLER**, Ph.D., Coherent Inc., Santa Clara, CA

*The basics of laser marking are reviewed, as well as current and emerging laser technologies.*

Laser marking is established at multiple points in semiconductor production and applications continue to diversify. There are several laser technologies servicing the application space. This article reviews the basics of laser marking and the current and emerging laser technologies they utilize. It is intended to give a clear sense of what applications parameters drive the choice of laser (speed, cost, resolution, etc.), and provide those developing a new application some guidance on how to select the optimum technology.

## Laser marking basics

Laser marking usually entails inducing a visible color or texture change on a surface. Alternatively, although less commonly, marking sometimes involves producing a macroscopic change in surface relief (e.g. engraving). To understand what laser type is best for a specific marking application, it is useful to examine the different laser/material interactions that are generated by commonly used laser types.

Most frequently, lasers produce high contrast marks through a thermal interaction with the work piece. That is, material is heated until it undergoes a chemical reaction (e.g. oxidation) or change of crystalline structure that produces the desired color or texture change. However, the particulars of this process vary significantly between different materials and laser types.

CO<sub>2</sub> lasers have been employed extensively for PCB marking because they provide a fast method of producing high contrast features. However, they are rarely selected when marking at the die or package level. This is because the focused spot size scales with wavelength due to diffraction. CO<sub>2</sub> lasers emit the longest infrared (IR) output of any marking laser. Additionally, IR penetrates

far into many materials, which can cause a substantial thermal impact on surrounding structures. Consequently, CO<sub>2</sub> laser marking is limited to producing relatively large features where a significant heat affected zone (HAZ) can be tolerated.

Fiber lasers, which offer high power output in the near IR, have emerged over the past few years as one of the most cost effective tools for high-speed marking. Furthermore, the internal construction of fiber lasers renders a compact footprint, facilitating their integration into marking and test handlers. Cost and space savings are further enhanced when the output of a single, high power fiber laser is split, feeding two scanner systems.

But fiber lasers have disadvantages, too. One reason for the low cost of many fiber lasers is that they are produced in high volumes with designs meant for general-purpose applications. For example, they usually produce a high quality beam with a Gaussian intensity profile. This is



**FIGURE 1.** PowerLine Pico 10-532 IC, a short-pulse laser for marking ultra-shallow and ultra-small features.

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advantageous for many material processing applications, but not always for laser marking. In fact, a more uniform beam intensity distribution, called a flat-top profile, is sometimes more useful since it produces marks with a sharper, more abrupt edge (rather than a smooth transition from the marked to the unmarked region). Coherent recently introduced a new type of fiber (NuBEAM Flat-Top fiber technology) which enables efficient conversion of single-mode laser beams into flat-top beam profiles, specifically to address this issue.

Other quality criteria, such as high-purity linear polarization, and stability of pulse energy and pulse width, are difficult to achieve with low-cost fiber lasers. This limits their use in more stringent or sensitive marking applications. From a practical standpoint, most fiber lasers cannot be repaired in the field, but are replaced as a whole. This leads to longer equipment downtime and increased maintenance efforts as compared to traditional marking lasers based on diode-pumped, solid-state (DPSS) technology (specifically, DPSS is used here to refer to lasers with crystal resonators).

DPSS lasers also emit in the near infrared. Generally, these lasers are more expensive than a fiber laser of the same output power level. So, infrared DPSS lasers are most commonly used in applications having

technical requirements that cannot be met by fiber lasers, such as high volume production of more advanced and expensive semiconductor devices.



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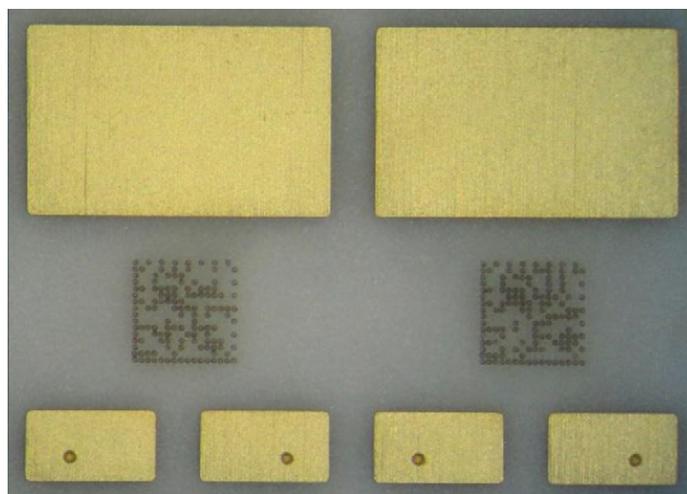


**FIGURE 2.** Standard thickness molded IC package marked with 30 W, near IR DPSS laser (PL E Air 30 D IC).

One advantage of DPSS laser technology is that it can be configured to directly produce a multi-mode beam profile which is essentially flat-top. The Coherent | RoFin PowerLine E Air 30-1064 IC is an example which has found extensive use in semiconductor marking, since it provides an efficient way to rapidly produce very high contrast marks.

Another useful feature of DPSS lasers, which produce pulsewidths in the nanosecond regime, is that their output is much more stable than that of fiber lasers. This makes it much easier to reliably frequency double or triple their infrared light within the laser head, giving a choice of output in the green or ultraviolet (UV). Output at these wavelengths provides two significant benefits. First, they offer additional options in matching the absorption of the material to the laser wavelength. Stronger absorption generally yields higher marking efficiency and reduced HAZ, since the laser light doesn't penetrate as far into the material. The second benefit of shorter wavelengths is the ability to focus to smaller spot sizes (because of their lower diffraction) and produce smaller, finer marks.

However, frequency multiplied DPSS lasers are generally more costly and voluminous than either fiber lasers or infrared DPSS lasers with comparable output power. Lower power translates into reduced marking speed.



**FIGURE 3.** Ceramic LED substrate marked with a nanosecond pulsewidth fiber laser (PowerLine F 20 Varia IC).

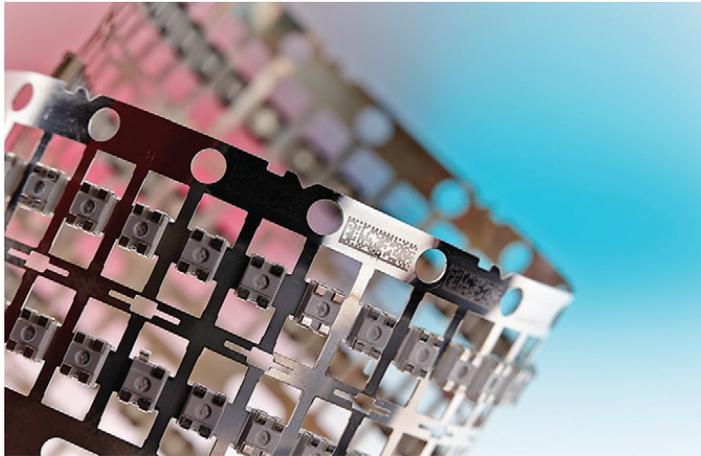
Therefore, green and UV DPSS lasers are typically employed when they offer a significant advantage due to the particular absorption characteristics of the material(s) being marked.

Another emerging and important class of marking lasers has pulsewidths in the sub-nanosecond range. Due to the nature of the laser/material interaction at short pulsewidths, these lasers tend to produce the smallest possible HAZ with excellent depth control.

There are just a few products currently on the market that exploit this property. One example is the PowerLine Pico 10 from Coherent | RoFin which generates 0.5 ns laser pulses in either the near IR (8 W total power) or green (3 W total power), at pulse repetition rates between 300 kHz and 800 kHz. This combination of output characteristics makes it capable of high speed marking of a wide range of materials where mark penetration depth must necessarily be shallow because of low material thickness, or to minimize HAZ.

### Laser marking today

Typically, the first consideration in choosing a laser for a specific application is matching the absorption characteristics of the material with the laser wavelength. Similarly, desired feature size is also driven by laser wavelength, as well as by the precision of the beam scanning system. Next, HAZ constraints usually determine the maximum pulsewidth which can be used (although this choice is again highly material dependent). To see how these parameters interact in practice, it's useful to review some real world applications.



**FIGURE 4.** Metal ledframe marked with a near IR fiber laser (Coherent PL F 20-1064 IC).

### Epoxy-based molding compounds

The most commonly used molding compounds absorb very well in the near IR. Specifically, the near IR laser transforms the usually black molding compound into a gray/white powder, yielding high contrast marks. Plus, many IC packages have mold compound caps thick enough to easily tolerate a marking depth of 30  $\mu\text{m}$  to 50  $\mu\text{m}$ . As a result, many marking systems based on near IR lasers, both fiber and DPSS, are currently in use.

However, some semiconductor devices with small form factor have only thin mold compound caps to protect wire bonded silicon dies, and a marking depth of only 10  $\mu\text{m}$  or less is required. Increasingly, green lasers are used for this type of shallow marking because of a stronger absorption at this wavelength by the epoxy matrix.

### Ceramics

The process window when marking ceramics, such as used in packaging power semiconductors, high-brightness LEDs, RF devices, saw filters or MEMS sensors, is relatively narrow. Accurate focus and high pulse energy are critical to ensure reliable marking results, and ideally, the laser marker should have the capability to adjust the focus of the laser beam onto the ceramic surface in real time, in order to compensate for package height variations. Because of their more reliable interaction with ceramic materials, DPSS lasers based on Nd:YAG, which offer high pulse energies and relatively long pulses, are often still used for marking ceramic lids and substrates. Coherent | Rofin has also developed a special fiber laser (the PowerLine F 20 Varia IC), which offers adjustable pulse widths up to 200 ns, specifically to improve process windows for marking applications of this type.



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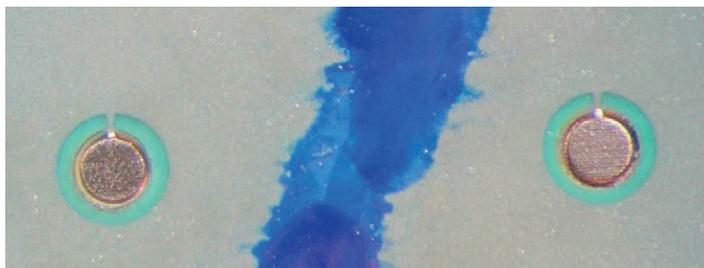
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**FIGURE 5. a)** Gold pad marked on flexible IC substrate



**FIGURE 5. b)** IC substrate marked white



**FIGURE 5. c)** backside of silicon wafer marked with characters <math>< 150 \mu\text{m}</math> in height

The ceramic substrates used with high-power LEDs often require tiny marks to identify individual devices. IR lasers are the preferred lasers for marking these ceramic substrates, providing their spot size is not too big for the layout to be marked. For very small marking features a green laser or UV laser is often required.



**FIGURE 5. d)** leadframe mark

### Organic substrates

IC substrates or interposers are marked during production with traceable data matrix codes. The thin green solder resist layer on top of the substrate has to carry the mark, and care has to be taken that the copper underneath the solder resist is not exposed. Moreover, data

matrix codes can be quite small, with cell sizes of only  $125 \mu\text{m}$  or even less. Since the spot size of the focused laser beam must thus be much smaller than the cell size, the final spot diameter must be significantly less than  $100 \mu\text{m}$ .

Defective IC substrates often are identified by marking large features (e.g., a cross) into the solder resist layer. Although the part is defective, the properties of the mark are still important. This is because it has to be reliably recognized by subsequent processing tools, and also, because any delamination of the solder resist layer might cause problems during succeeding processes.

IC strips have gold pads along their periphery which are used to identify parts found to be defective after die attach and wire bonding. For defective parts, the gold pad is marked by converting its color from gold to black or to dark grey.

Ideally, it is desirable to have one laser marker that can accomplish all three of these marking applications tasks. The green DPSS laser has become the standard laser marker for these applications, with UV lasers occasionally employed for high-end substrates.

### Semiconductors

The growing demand for flip-chip devices, wafer-level packaging and defective die identification drives the need for direct marking of silicon, GaAs, GaN/sapphire or other semiconductors. Silicon is partially trans-

parent in the near IR, and lasers at this wavelength are used whenever deep marks into silicon are required, such as placing wafer IDs near the wafer edge. Near IR laser markers are also selected for marking molded fan-out wafer level packaging wafers.

However, for marking either flip-chips or the backside of wafers, green lasers are preferred because of the strong absorption of this wavelength in silicon. Wafer backside marking requires only very shallow marks and the shallow laser penetration avoids potential damage to the circuitry on the reverse side of the flip-chip or wafer. The need for shallow marking also minimizes the laser power requirement. For example, Coherent | Rofin provides a 6 W green laser (the PowerLine E 12 SHG IC) that is well suited for wafer backside marking, and can also mark the wafer through the tape whenever the wafer is mounted on a film frame.

### Metals

Near IR lasers are widely used for marking the metal lids used with microprocessors and other high power consumption ICs.

Leadframes, which are plated with tin, silver or gold, are marked either before or after plating. Since leadframes are used for cost sensitive devices, capital investment is critical, and economical fiber lasers are often chosen for this reason.

### Laser marking tomorrow

As packages get thinner and smaller, they will require shallower, higher resolution marks. Sub-nanosecond lasers are the most promising method for producing these types of marks, and are compatible with a wide range of materials. The diverse capabilities of this technology are shown in **Figure 5**, which depicts marking results on four different materials using a sub-nanosecond laser (Coherent | Rofin PowerLine Pico 10-532 IC).

The first image is a flexible IC substrate; very thin solder resist layers and metal coatings make it important that the laser does not cause delamination. Here, the circular gold pad has been converted to black without delamination. In the next image, an IC substrate has been given a white mark, again without delaminating the solder resist.

The third image shows very small characters (< 150  $\mu\text{m}$ ) marked on the backside of a silicon wafer containing

hundred thousands of tiny discrete semiconductor devices. Producing marks of this resolution through the film would be difficult to accomplish with a nanosecond pulsewidth laser.

The final image is a copper leadframe coated with thin silver film. Here, the goal is to produce a shallow mark with high contrast without engraving the underlying material, which has been accomplished with the sub-nanosecond laser.

### Conclusion

Semiconductor fabrication and packaging represent challenging marking applications, often requiring small, fine marks produced without a significant effect on surrounding material. An overall trend towards smaller and thinner device geometries will drive increased use of higher precision laser tools, such as those utilizing green and UV nanosecond lasers, and even sub-nanosecond lasers, while cost-sensitive applications will continue to utilize inexpensive fiber lasers.  $\blacktriangleright$

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# DSA and EUV: Complementary technologies to enable fine-pitch lithography

**DOUGLAS J. GUERRERO**, Ph.D., Brewer Science, Rolla, MO

*DSA and EUV should be envisioned as complementary, not competing, techniques that will eventually become mainstream for fine-pitch lithography.*

**A**dvances in lithography have always been critical in the drive toward each subsequent semiconductor node. Anticipating limitations in the scaling ability of immersion lithography, the industry has been pursuing next-generation lithography techniques. Several techniques have been proposed, including extreme ultraviolet (EUV) lithography, multibeam electron-beam lithography, nanoimprint lithography and directed self-assembly (DSA) of block copolymers.

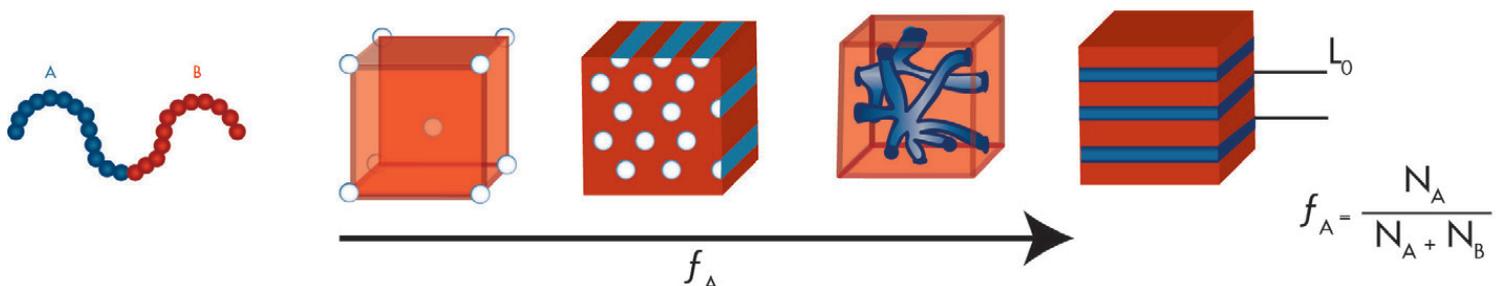
DSA attracted a great deal of interest from major semiconductor manufacturers for several years, following its initial development in the early 2000s. However, it has since fallen out of favor to some extent, in part because of advances in EUV lithography as a result of focused investment in that technology. Recent developments in DSA materials and processing

promise to overcome concerns that have delayed its implementation.

Choosing an appropriate lithography technique does not need to be an either-or proposition. The greatest opportunity may lie in leveraging both EUV lithography and DSA. Although these two technologies are sometimes seen as competing, it makes more sense to envision them as complementary. This article explains how lithography may benefit by taking advantage of both EUV and DSA, and why previously existing roadblocks may no longer pose obstacles.

## The material defines the pattern

Unlike most lithography techniques, where the mask defines the pattern, in DSA the pattern exists in the material itself. The original block copolymers (BCPs)



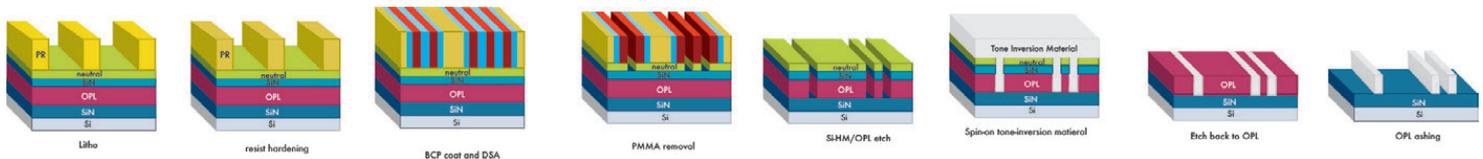
**FIGURE 1.** Morphology of generic BCP as a function of composition. As the fraction of component A increases, the configuration changes from spheres to cylinders to lamellae.

Legend:

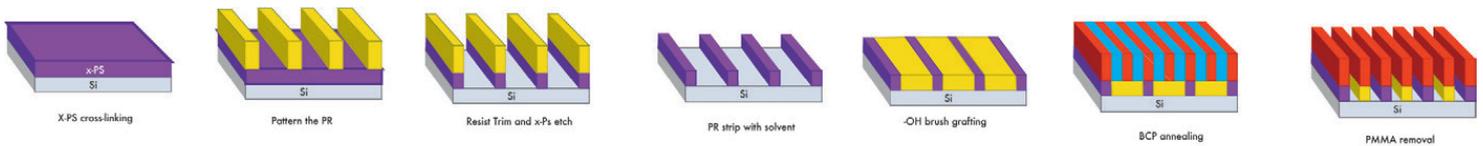
L<sub>0</sub>: Characteristic domain length scale

N: Number of chain segment

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**FIGURE 2.** Example process for tone-inverted graphoepitaxy (TIGER), including lithography, DSA deposition and etch that employs a silicon-containing anti-reflective coating (Si-HM) layer.



**FIGURE 3.** Liu-Nealey (LiNe) process flow for chemoepitaxy of DSA materials.

for DSA combine polystyrene (PS) and poly(methyl methacrylate) (PMMA), two polymers that naturally segregate themselves into separate phases. Adjusting the relative proportions of PS and PMMA in the PS-b-PMMA material changes the morphology from spherical to cylindrical to lamellar (**FIGURE 1**). The product of the Flory interaction parameter,  $\chi$ , and the segment length determine the spacing of the ordered structure. The higher the value of  $\chi$ , the finer the pitch of the resulting structure.

Standard PS-b-PMMA materials have relatively low  $\chi$ , which limits the pitch to 20nm or larger. Some materials manufacturers are considering chemistries other than PS-b-PMMA to produce high- $\chi$  BCPs, replacing the PMMA component with polydimethylsiloxane or polyhydroxystyrene. Modifying PS-b-PMMA is another approach to increase  $\chi$ . In this manner, it is possible to tune  $\chi$ , the molecular weight and the glass transition temperature to achieve lamellar spacing between 14nm and 40nm under various annealing conditions.

The process flow for BCP deposition is straightforward. A neutral layer spin-coated onto the substrate allows for the BCP to separate into its individual domains during the thermal annealing process. The neutral layer allows for domain separation because it does not have affinity for either of the polymer chains in the BCP. Polymer domain separation is responsible for pattern formation.

### Processing Considerations

The DSA deposition process uses one of two basic approaches (**FIGURES 2 and 3**). Graphoepitaxy leverages topography to align the BCPs, depositing them into relatively deep trenches. Guide patterns define the trenches, confining the BCPs into configurations

in which they align in a preferred direction. Chemical epitaxy, or chemoepitaxy, is based on a chemical pattern on a flat substrate, on top of which the BCPs self-align.

The semiconductor industry is pursuing both graphoepitaxy and chemoepitaxy approaches, favoring the former



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for producing fine-pitch vias and the latter for creating arrays of parallel lines.

Annealing temperatures are in the range of 250°C to 275°C, making them compatible with standard semiconductor processing. The annealing step can be lengthy—up to two hours to create structures with sufficiently low defect rates—adding cost to the process.

PS-b-PMMA BCPs are being manufactured in high-volume quantities. Worldwide, 1.1 million tons of the material are currently in use for a variety of applications. This quantity is greater than the needs of the entire semiconductor industry. Therefore, although no commercially produced DSA materials are currently targeted for semiconductor applications, the infrastructure is in place to scale up production of suitable materials when the industry is ready.

### Why DSA is attractive now

DSA was added to the ITRS roadmap in 2007. Major semiconductor industry players originally believed DSA would enter commercial production anywhere between the 14nm and 7nm logic nodes, and even sooner for DRAM; but so far that has not come to pass. A survey at the 2016 DSA Symposium suggested that the technology is still not ready for the mainstream and won't be for several years. But some IDMs would like to accelerate the process, and there are reasons to believe this is not only possible, but desirable.

Decreasing the wavelength to 193nm immersion lithography has enabled line width and spacing down to 80nm. Techniques such as self-aligned quadruple patterning (SAQP) can create even smaller features through multiple lithography/etch iterations, but at the expense of adding lithography steps, each requiring a custom mask.

Immersion lithography is reaching its limits, providing an opportunity for next-generation lithographic techniques. Designs with critical dimensions (CD) in the range of 10nm to 30nm create a sweet spot for these state-of-the-art techniques.

Advances in EUV lithography are one factor that has led the industry to favor it over DSA. Today's EUV materials have greater sensitivity compared with older-generation products, therefore requiring lower UV doses; and line roughness has improved as well. EUV

lithography can create vias with 30nm or 40nm spacing that are not feasible with immersion lithography.

DSA enables even finer resolution than the semiconductor industry currently demands. Feature sizes are just now approaching a level where DSA can be especially effective. If these trends continue, the technique is poised to be widely adopted before the end of this decade.

### DSA and EUV: Better together?

The most effective solution may lie in leveraging EUV and DSA technologies to take advantage of the strengths of each. Both methods can achieve resolution levels that are compatible with the N7 and N5 logic nodes. EUV lithography is well-suited to patterning designs with multiple different pitches, down to line width and spacing around 30nm. For such fine pitches, however, the number of mask steps required may make the technique prohibitively expensive. Local CD uniformity (LCDU) can also be a concern, especially at high throughput rates.

The initial hard-mask lithography process is the same for both EUV and DSA, but they diverge during pattern processing. Once the BCPs are deposited, DSA can achieve 30nm feature size without requiring additional masks. Annealing naturally separates the two phases into the correct morphology. The DSA process, however, is best suited to designs with a single pitch.

EUV can be used to pattern lower-resolution features on a chip, plus create spacers for subsequent DSA deposition. This combination provides the greatest design flexibility while streamlining the fabrication process, eliminating processing steps and reducing mask costs. LCDU is also better than with EUV alone.

DSA is best suited for devices with multiple repeating, regular fine-pitch features. Therefore, it likely will first be implemented in DRAM storage, later migrating to use in via layers on logic devices. Graphoepitaxy, especially using EUV to deposit the spacers, can enable more complex designs using DSA, where different regions of the chip require different pitches. This will presumably be the approach of choice for logic chips.

Despite the promise that leveraging both DSA and EUV offers, the semiconductor industry will only migrate to this approach once suppliers can convince IDMs that

the materials have overcome their technical limitations. DSA has suffered from several challenges that have delayed its adoption: Primary issues are defectivity, pattern placement accuracy, ease of integration into manufacturing flows, and cost. But there is reason to be optimistic, as advances in chemistry and processing methods are improving all these metrics.

### Overcoming technical challenges

The 2016 DSA Symposium survey identified defectivity as the greatest technical challenge. Defectivity and cost are related, in that the lowest defect levels are seen with the longest annealing times. While annealing for as little as five minutes causes the two phases to separate, the resulting material contains far too many defects to be suitable for commercial use.

Wafers are typically annealed one at a time, which can make the cost of annealing prohibitive. However, recent research using batch annealing in a vertical furnace showed great promise for reducing cost. By annealing 150 wafers in parallel for 30 minutes, researchers were able to demonstrate sufficiently low defect levels at a cost lower than that of SAQP.

Using both DSA and EUV has the potential to alleviate the problem of pattern placement errors. For example, EUV lithography can create prepatterned holes for doublet vias. The two vias may merge during the EUV process but will then automatically separate during DSA. Without DSA, an additional lithography step may be required to avoid merged vias.

This approach of leveraging EUV and DSA for fine-pitch vias is most reliable when the via shape is optimized. Studies have shown that a peanut shape, rather than an elliptical one, is ideal for creating doublet vias with minimal risk for pattern placement errors, even at the challenging N5 node.

### Collaborating to advance DSA adoption

The semiconductor industry has extensive experience with lithography, but DSA requires a shift in mindset. BCP materials are not something that the industry is used to, and revolutionary rather than evolutionary changes in materials and processes can face resistance. DSA needs to be demonstrated on real devices before it can achieve traction in the semiconductor market.

Collaborative efforts between semiconductor industry materials suppliers and chemical companies with deep experience in BCPs are one route to bridge this gap. One such collaboration is currently underway. Brewer Science has teamed up with Arkema, a company with two decades of experience producing BCPs, but little leverage with the semiconductor industry. The partnership, begun in 2015, has led to pilot production of DSA materials, paving the way for the technique to move out of the laboratory and into commercial semiconductor products.

DSA and EUV should be envisioned as complementary, not competing, techniques that will eventually become mainstream for fine-pitch lithography at the N7 node and beyond. Partnerships between materials and chemical companies are poised to enable this transition, unlike previous efforts by single organizations. ◀

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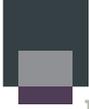
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# Advancements in spintronics

**HIDEO OHNO, MARK STILES, and BERNARD DIENY, IEEE**

*Applications now include nanoscale Spintronics sensors that further enhance the areal density of hard disk drives, through MRAMs that are seriously being considered to replace embedded flash, static random access memories (SRAM) and at a later stage dynamic random access memories (DRAM).*

**S**pintronics is the concept of using the spin degree of freedom to control electrical current to expand the capabilities of electronic devices. Over the last 10 years' considerable progress has been made. This progress has led to technologies ranging from some that are already commercially valuable, through promising ones currently in development, to very speculative possibilities.

Today, the most commercially important class of devices consists of magnetic sensors, which play a major role in a wide variety of applications, a particularly prominent example of which is magnetic recording. Nonvolatile memories called magnetic random access memories (MRAMs) based on magnetic tunnel junctions (MTJs), are commercial products and may develop into additional high impact applications either as standalone memories to replace other random access memories or embedded in complementary metal-oxide-semiconductor (CMOS) logic.

Some technologies have appealing capabilities that may improve sensors and magnetic memories or develop into other devices. These technologies include three-terminal devices based on different aspects of spin-transfer torques, spin-torque nano-oscillators, devices controlled by electric fields rather than currents, and devices based on magnetic skyrmions. Even further in the future are Spintronics-based applications in energy

harvesting, bioinspired computing, and quantum technologies.

But before we get into detail about where Spintronics is today, we need to cover the history of Spintronics.

## The history of spintronics

Spintronics dates to the 1960s and was discovered by a group at IBM headed by Leo Esaki, a Japanese physicist who would later go on to win a share of the Nobel Prize in 1973 for discovering the phenomenon of electronic tunneling. Esaki and his team conducted a study which showed an antiferromagnetic barrier of EuSe sandwiched between metal electrodes exhibits a large magnetoresistance.

Subsequent advances of semiconductor thin film deposition techniques such as molecular beam epitaxy led to the development of semiconductor quantum structures, which prompted studies of magnetic multilayers. Ensuing studies of magnetic multilayers resulted in the discovery of giant magnetoresistance (GMR) in 1988. This effect was used to make magnetic sensors, which boosted the areal density of information stored on hard disk drives and led to the 2007 Nobel Prize in Physics awarded to Albert Fert and Peter Grunberg.

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Since then rapid progress has continued to enhance both the role and the potential of Spintronics. So, let's take a look at where we are now.

### Where we are now

Applications now include nanoscale Spintronics sensors that further enhance the areal density of hard disk drives, through MRAMs that are seriously being considered to replace embedded flash, static random access memories (SRAM) and at a later stage dynamic random access memories (DRAM). Applications also include devices that utilize spin current and the resulting torque to make oscillators and to transmit information without current.

Now let's look at those applications and more in-depth.

**Modern Hard Disk Drives:** Two breeds of Spintronics sensors have replaced traditional anisotropic magnetoresistance (AMR) sensors. Those sensors include giant magnetoresistance (GMR) sensors (used in hard disk drives between 1998 and 2004) and tunnel magnetoresistance (TMR) sensors (used since 2004).

Those sensors are part of the technology development that enabled the increase of storage density of hard disk drives by several orders of magnitude, laying the foundation of today's information age in the form of data centers installed by the cloud computing industry.

**Magnetoresistive Random Access Memory (MRAM):** MRAM and particularly spin-transfer torque MRAM (STT-MRAM) is a nonvolatile memory with very high endurance and scalability. The current STT-MRAM technology uses an array of MTJs with an easy axis of magnetization oriented out of the plane of the layers. These MTJs utilize interface perpendicular anisotropy at the CoFeB-MgO interface, along with the large TMR of the system, for reading the state of magnetization. The spin-transfer torque exerted by a spin polarized current is used to change the magnetization direction, offering an efficient way of rewriting the memory. **FIGURE 1** show the main families of MRAM that have evolved since 1995.

**Three Terminal Magnetic Memory Devices:** Recent physics developments raise the prospect of three-terminal spintronic memory devices. These devices

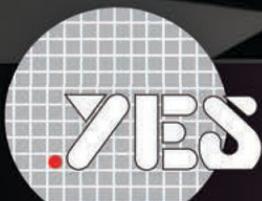
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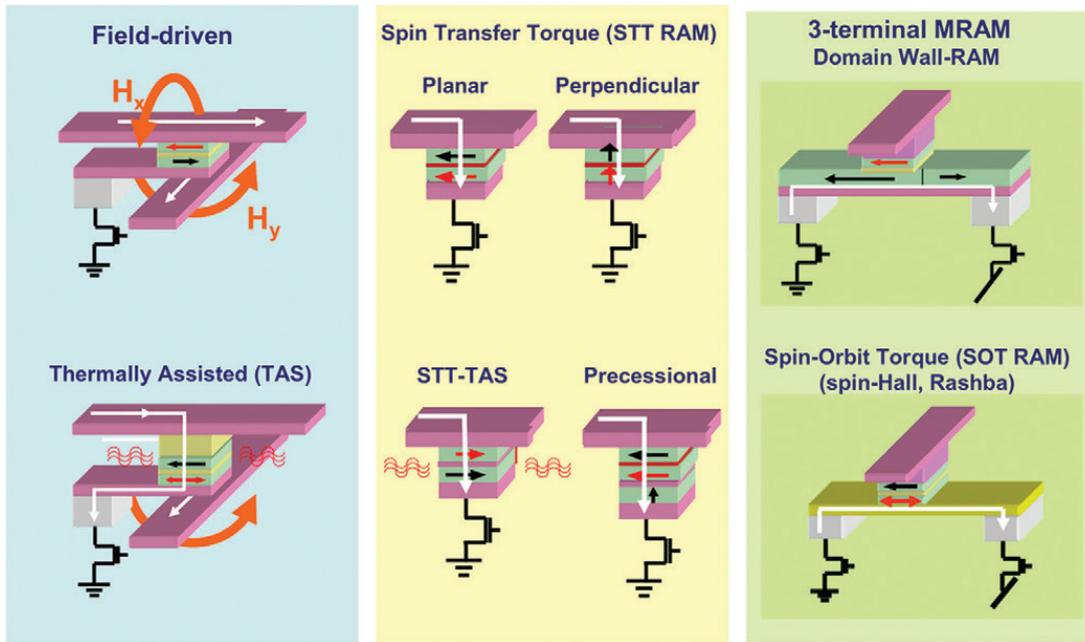


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**FIGURE 1.** Various families of MRAM developed since 1995. Left: First MRAM generation based on field writing. Center: Various flavors of STT-MRAM with in-plane and out-of-plane magnetization, with thermal assistance (TAS) or orthogonal polarizers (precessional or OST-MRAM). Right: 3-terminal MRAM using current-induced domain wall propagation or spin-orbit-torque (SOT) effects (Rashba or spin Hall effects).

have an advantage over the standard two-terminal devices used in memory applications such as MRAM in that separating the read and write functions potentially overcomes several future roadblocks in the development of MRAM. There are two writing schemes: one is based on spin currents generated by an electrical current running through a heavy metal adjacent to the free layer of the MTJ. The current causes a spin current both in the bulk of the heavy metal and at the interface; this spin current then exerts a torque, called the spin-orbit torque, on the magnetization. In this scheme, the write current does not pass through the MTJ, separating the write and read functions. The other scheme uses current-induced domain wall motion to move a domain wall in the free layer of the MTJ from one side of the fixed layer to the other. In this scheme, the current passes through the free layer, but not the tunnel barrier, again separating the read and write functions.

**Standby-Power-Free Integrated Circuits Using MTJ-Based VLSI Computing:** Spintronic-based nonvolatile embedded working memory used in conjunction with CMOS-based logic applications is a crucial first step toward standby-power-free logic circuits that are much needed for Internet of

Things (IoT) applications. MRAM based logic-in-memory reduces the overhead of having memory and logic apart and gives both minimized interconnection delay and nonvolatility.

**Security:** These devices have shown great promise for logic and memory applications due to their energy efficiency, very high write endurance, and nonvolatility. Besides, these systems gather

many entropy sources which can be advantageously used for hardware security. The spatial and temporal randomness in the magnetic system associated with complex micromagnetic configurations, the nonlinearity of magnetization dynamics, cell-to-cell process variations, or thermally induced fluctuations of magnetization can be employed to realize novel hardware security primitives such as physical unclonable functions, encryption engines, and true random number generators.

**Spin-Torque and Spin-Hall Nano-Oscillators:** Spin-torque nano-oscillators (STNO) and spin-Hall effect nano-oscillators (SHNO) are in a class of miniaturized and ultra-broadband microwave signal generators that are based on magnetic resonances in single or coupled magnetic thin films. These oscillators are based on magnetic resonances in single or combined magnetic thin films where magnetic torques are used to both excite the resonances and subsequently tune them. The torques can be either spin-transfer torques due to spin-polarized currents (STNOs) or spin Hall torques due to pure spin currents (SHNOs). These devices are auto-oscillators and so do not require any active feedback circuitry with a positive gain for their operation. The auto-oscillatory state is strongly nonlinear, causing phase–amplitude coupling, which governs a wide range of properties, including frequency tunability, modulation, injection locking, mutual synchronization, but also causes significant phase noise. STNOs and SHNOs can, in principle, operate at any frequency supported by a magnetic mode, resulting in a potential frequency range of over six orders of magnitude, from below 100

MHz for magnetic vortex gyration modes to beyond 1 THz for exchange dominated modes. Since STNOs and SHNOs can also act as tunable detectors over this frequency range, there is significant potential for novel devices and applications.

Beyond the applications listed, the spin degree of freedom is also being used to convert heat to energy through the spin Seebeck effect, to manipulate quantum states in solids for information processing and communication, and to realize biologically inspired computing. These may lead to new developments in information storage, computing, communication, energy harvesting, and highly sensitive sensors. Let's take a look at these new developments.

**Thermoelectric Generation Based on Spin Seebeck Effects:** The study of combined heat and spin flow, called spin caloritronics, may be used to develop more efficient thermoelectric conversion. Much of the focus of research in spin caloritronics has been the longitudinal spin Seebeck effect, which

refers to spin-current generation by temperature gradients across junctions between metallic layers and magnetic layers. The generated spin current in the metallic layer gets converted into a charge current by the inverse spin Hall effect, making a two-step conversion process from a thermal gradient perpendicular to the interface into a charge current in the plane of the interface. This process can be used for thermoelectric conversion. Device structures using the spin Seebeck effect differ significantly from those using conventional Seebeck effects due to the orthogonality of the thermal gradient and resulting charge current, giving different strategies for applications of the two effects.

**Electric-Field Control of Spin-Orbit Interaction for Low-Power Spintronics:** Control of magnetic properties through electric fields rather than currents raises the possibility of low energy magnetization reversal, which is needed for low-power electronics and Spintronics. One specific way to accomplish this low energy switching is through electric-field

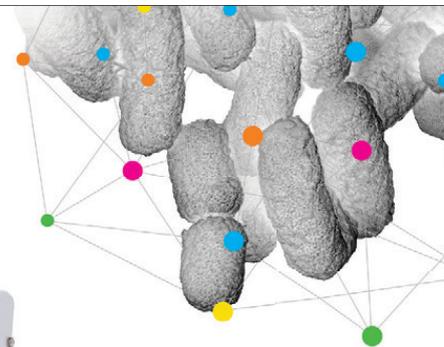
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control of electronic states leading to modification of the magnetic anisotropy. By applying a voltage to a device, it is possible to change the anisotropy such that the magnetization rotates into a new direction. While such demonstrations of switching alone are not sufficient to make a viable device, voltage controlled reversal is a promising pathway toward low-energy nonvolatile memory devices.

**Control of Spin Defects in Wide-Bandgap Semiconductors for Quantum Technologies:** The spins in deep level defects found in diamond (nitrogen-vacancy center) and in silicon carbide (divacancy) have a quantum nature that manifests itself even at room temperature. These can be used as extremely sensitive nanoscale temperature, magnetic-field, and electric-field sensors. In the future, microwave, photonic, electrical, and mechanical control of these spins may lead to quantum networks and quantum transducers.

**Spintronic Nanodevices for Bioinspired Computing:** Bioinspired computing devices promises low-power, high-performance computing but will likely depend on devices beyond CMOS. Low-power, high performance bioinspired hardware relies on ultrahigh-density networks built out of complex processing units interlinked by tunable connections (synapses). There are several ways in which spin-torque-driven MTJs, with their multiple, tunable functionalities and CMOS compatibility, are very well adapted for this purpose. Some groups have recently proposed a variety of bioinspired architectures that include one or several types of spin-torque nanodevices.

**Skyrmion-Electronics: An Overview and Outlook:** The concept of skyrmions derives from high energy physics. In magnetic systems, skyrmions are magnetic textures that can be viewed as topological objects. Theory suggests that they have properties that might make them useful objects in which to store and manipulate information. Many of the ideas are similar to ideas that were developed decades ago for bubble memory or, more recently, racetrack memory. There are several possible advantages for skyrmion devices as compared to other related devices. They are potentially higher density and lower energy, although the arguments for these remain to be experimentally verified.

So, what does the future of spintronics have in store?

## The future

Spintronics will continue to have increasing impact, but the future is somewhat uncertain. The importance of magnetic sensors is likely to remain important while the importance of the magnetic sensors in hard disk drives appears to depend on the economics of mass storage in the cloud.

MRAM seems likely to play an increasing role both as standalone memory and embedded in CMOS. The degree of adoption still depends on a few technical and many economic considerations. The acceleration, over the past few months, of announcements and demonstrations related to STT-MRAM produced by major microelectronics companies, seems to indicate that large volume production of STT-MRAM is getting quite close. If the adoption of this technology by microelectronics industry becomes a reality, the whole field will be strongly boosted.

In the future, Spintronics can play a critical role in areas such as IoT, ultralow-power electronics, high-performance computing (HPC). Besides, in the next 10 to 15 years, we are likely to see a much greater role played by alternative forms of computing. The role that Spintronics plays in those technologies is likely to be strongly influenced by the success of MRAM. If MRAM is successful, we will have developed the ability to manufacture it making it easier to import into other technologies.

Some of the recent technical developments that have significant virtues for applications will likely play a role in technology 10 to 15 years from now but many will not. Research on many of these ideas will continue and will spawn related areas. Material research is key along this road.

Innovative materials allowing efficient charge to spin and spin to charge current conversion, or good control of magnetic properties by voltage, or efficient injection/manipulation/detection of spins in semiconductors can play major roles. Along with this idea, the use of oxide materials in spintronic devices can become quite important. Oxides share crystallinity with semiconductors in distinction to metallic magnetic devices. Will the greater control that comes with crystallinity give advantages to oxides in future devices? These are some of the many topics that are likely to be addressed in the coming years. ◀

# Measuring metals, dielectrics, resists and CDs in advanced packaging

**CHEOLKYU KIM**, Director of Metrology Product Management, Rudolph Technologies, Inc.

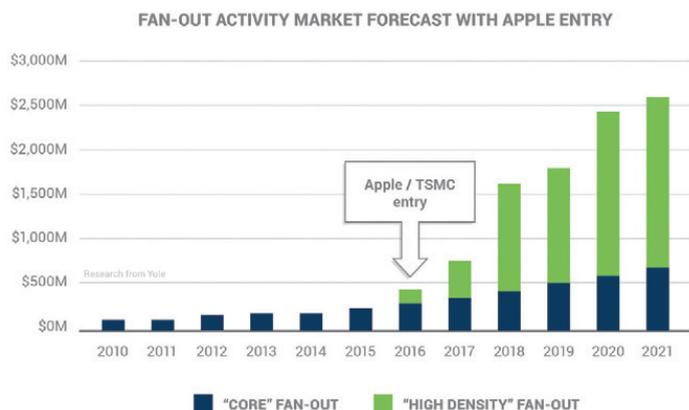
*A new system combines acoustic, optical and reflectometric techniques to enable measurement of metals, dielectrics, resists and critical dimensions on a single platform.*

**R**apid growth in the mobile device market is generating demand for advanced packaging solutions with higher levels of system integration and increased I/Os and functionality. This demand is driving 2.5D/3D integration of IC devices, which in turn requires sophisticated packaging technologies. Among various approaches, fan-out is gaining traction as outsourced semiconductor assembly and test (OSAT) houses and wafer foundries roll out their own technologies. As illustrated in **FIGURE 1**, the adoption of fan-out technology accelerated significantly in 2016, and is projected to reach \$2.5 billion by 2021, a more than 10X increase from 2015.

First generation “core” fan-out was geared toward mobile applications and had RDL lines that were typically 10/10 $\mu$ m (line/space) and larger. Second generation

HDFO processes, which were developed to integrate multiple chips in a single package, use more RDL lines at smaller width and tighter pitch, down to 2/2 $\mu$ m and smaller. Growth in HDFO accelerated with the entry of Apple and TSMC in 2016 and accounts for the bulk of the fan-out growth projected through 2021 [2-4].

As design rules for HDFO approach those of front-end processes, so too will requirements for process control and, in consequence, the need for more accurate and repeatable metrology. Until now, manufacturers have characterized metal films, such as RDL and under bump metallization (UBM), using semi-automated measurement tools, such as contact profilometers, which are easy to use and relatively inexpensive. However, these tools are not the best solution for measuring a variety of products with varying topographies in high volume production.

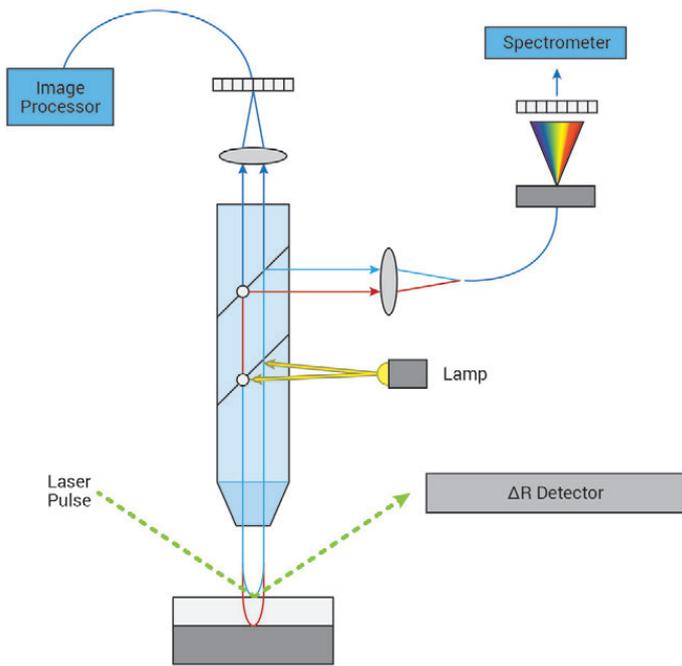


**FIGURE 1.** Fan-out activity revenues forecast breakdown by fan-out market type. [1]

## High Density Fan-Out process control

HDFO processes include one or more RDL, the number depending on the application. Like front-end processes, HDFO processes use additive and subtractive technologies to create patterns of conductive metal lines isolated by dielectric materials. As RDL lines become smaller, controlling line resistance with appropriate dimensional control has become essential. For an RDL process, the most important parameters to monitor are dielectric thickness, Cu seed layer thickness, Cu thickness and line width (CD). In general, the process must operate inside a window that varies within 10% of the target value. This, in turn, requires measurement tools with a gauge

**CHEOLKYU KIM** is Director of Metrology Product Management, Rudolph Technologies, Inc.



**FIGURE 2.** Schematic of MetaPULSE AP system's optics configuration.

capability ( $3\sigma$  repeatability + reproducibility) of 10% of the variability, or 1% of the target value. In addition to delivering accuracy and repeatability, the metrology system must be able to operate on product wafers and, therefore, 1) be able to measure test structures smaller than  $50\mu\text{m}$ , 2) be non-contact/non-destructive/non-contaminating, 3) be fast enough to support high volume production and 4) be able to handle the significant surface topography and substrate/wafer warpage that are induced by the HDFO process.

As shown schematically in **FIGURE 2**, the metrology system described here (MetaPULSE<sup>®</sup> AP, Rudolph Technologies), combines picosecond ultrasonic laser sonar (PULSE<sup>™</sup>), automated optical microscopy and reflectometry to meet all the requirements for RDL process control in a single system. The acoustic technique, well proven and widely accepted for metal film metrology in front-end applications, is a first principle technology that provides accurate measurements of metal film thickness for UBM and RDL.

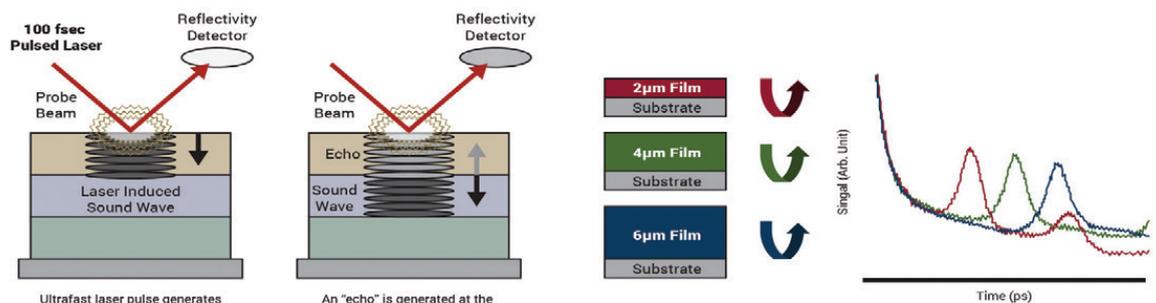
Measurements of RDL thickness with this technique on dense line arrays, pads and bumps have shown excellent correlation to cross sectional scanning electron micro-

scope (X-SEM) results. The precision and gage capability of the technology have been validated down to  $2\mu\text{m}$  and meet OSAT and foundry RDL roadmap requirements.

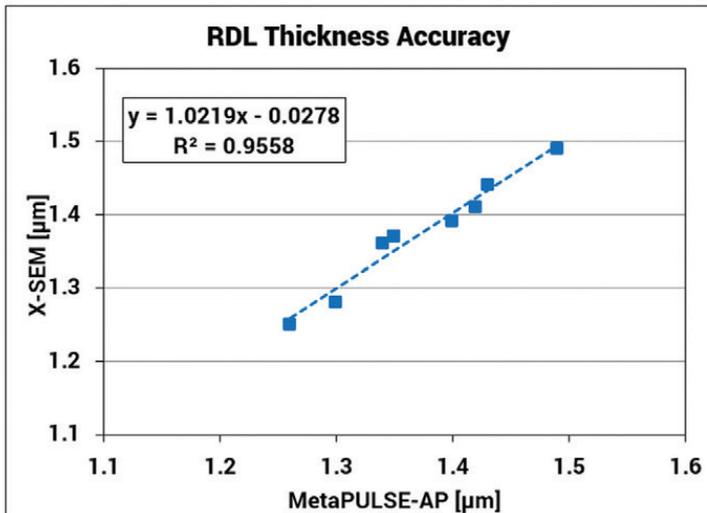
The integration of a high-resolution reflectometer provides accurate measurements of dielectric and resist thickness, ranging from a few  $1000\text{\AA}$  to  $60\mu\text{m}$ , on product wafers. The incorporation of an automated optical microscope/high-resolution camera provides gage-capable CD measurements. CD measurements can be made simultaneously with thickness measurements. The addition of optical CD measurements and reflectometer-based transparent film thickness measurements to the acoustic platform provides an efficient and comprehensive in-line RDL metrology solution that eliminates the need to route wafers to multiple measurement tools.

**PULSE acoustic thickness measurements on opaque films**

**FIGURE 3** illustrates the principles of the PULSE acoustic measurement technology. An extremely short laser pulse is focused onto a small spot on the sample surface where the energy of the laser pulse is absorbed by the film surface. This causes a sudden increase of surface temperature, and rapid thermal expansion launches a sound wave on the surface that travels into the film. When the sound wave reaches an interface with an underlying film, it is partially reflected back to the surface as an echo. Upon arrival at the surface, the echo causes a change in optical reflectivity, which is detected to measure the round-trip travel time of the sound wave. Film thickness can be calculated from the travel time of the sound wave and the speed of sound in the material. Some of the energy from the original sound wave is transmitted through the interface. In a multi-layered stack, the progressing sound wave returns a distinct echo from each interface. An analysis



**FIGURE 3.** (left) Measurement principle of the PULSE acoustic technique. (right) Acoustic signal plotted against time, note that the peak position moves to the right as thickness increases.



**FIGURE 4.** PULSE correlation with cross-sectional SEM.

of the round-trip travel time for each successive echo permits the calculation of the thickness of each layer. Typical data acquisition times vary from 1s to 4s per site. Repeatability is < 0.1% of target thickness, meeting the 10% GR&R requirement.

**FIGURE 4** shows the correlation between X-SEM and PULSE measurements for RDL in the 1.25μm-1.5μm thickness range. The excellent correlation clearly demonstrates the accuracy of PULSE thickness measurements.

### Reflectometer thickness measurements on transparent films

**FIGURE 5** (left) demonstrates the strong correspondence between a measured reflectometer signal and a model fitted curve for 5μm polyimide on Si. The figure also shows the correlation between reflectometer measurements and a fab reference metrology tool. The excellent correlation with the reference tool confirms the accuracy of reflectometer measurements. Data collection time for reflectometer measurements is typically less than 1s. The reflectometer has excellent sensitivity with Å level resolution and gage-capable R&R.

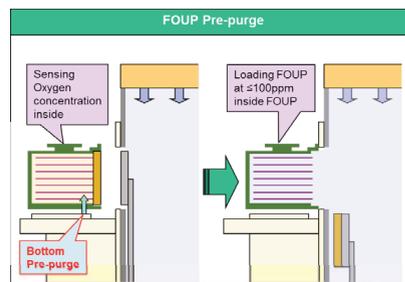
### Automated optical CD measurements

Using the optical microscope/ high resolution camera system, users can define multiple regions of interest

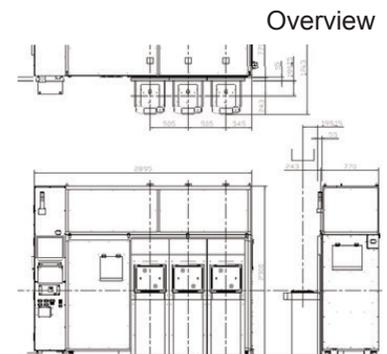
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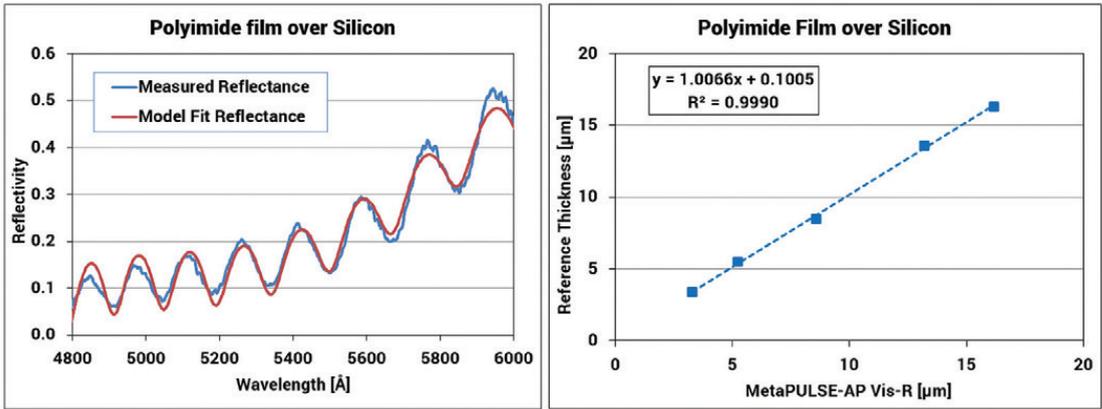


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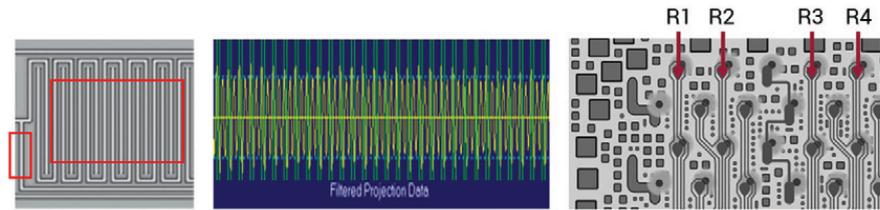
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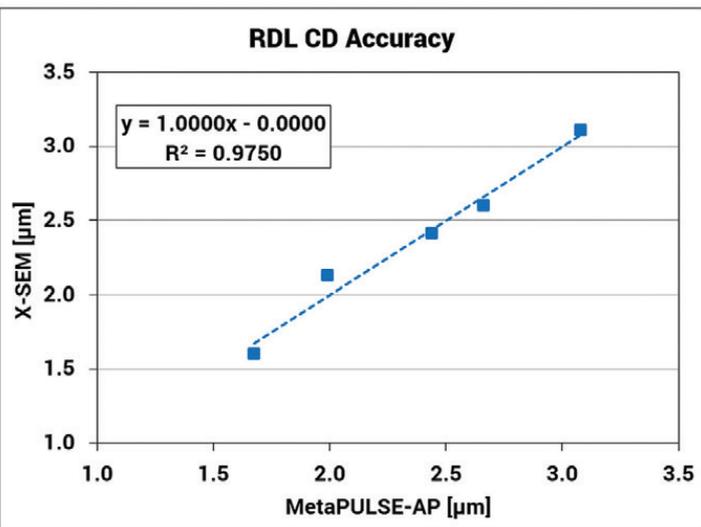
**FIGURE 5.** (left) Measured vs model fitted curves of 5µm Polyimide on Si. (right) Correlation with transparent film reference metrology tool.

arrays. The strong correlation between optical CD and X-SEM measurements (**FIGURE 7**) validates the accuracy of the technique. CD measurement with the optical microscope is limited by the microscope’s resolution, typically 1µm or larger. Since SEM resolution is typically on the scale of nanometers, the correlation requires proper calibration. The results shown in Fig. 7 are after calibration.



**FIGURE 6.** (left) ROI can be defined (red boxes) for single lines or multiple line arrays. (middle) Raw data across multiple lines shows the variations of the brightness signal, from which the algorithm detects edges and calculates CDs. (right) Example image with multiple regions of interest: R 1-4 (red arrows).

(ROI) for CD measurements, including single line and multi-line arrays. The built-in measurement algorithms can report individual or average values. Extension of the CD technique to also measure overlay has shown promising results and additional work is in progress to fully characterize the capability. **FIGURE 6** shows images and signals from CD measurements on lines and



**FIGURE 7.** Correlation between calibrated MetaPULSE AP and X-SEM.

### Multi-layered stacks

Most of RDL plating requires prior deposition of a Cu seed layer, the thickness of which must also be tightly controlled. **FIGURE 8** (left) shows examples of the acoustic signals acquired from three Cu/Ti stacks of varying thickness. The first positive peak of each signal gives the

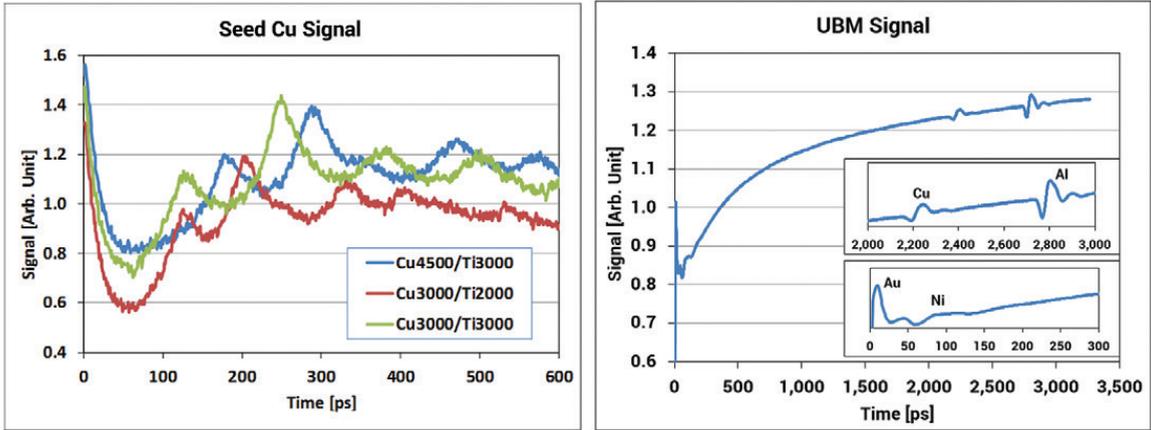
round-trip travel time of the sound wave in the Cu film, while the spacing between first and second positive peaks gives the round-trip travel time through the Ti layer. The echo positions are used to calculate the thickness of Cu and Ti layers simultaneously. **Figure 8** (right) shows the signal of an Au/Ni/Cu/Al stack measured on UBM. The echo from each layer is distinct. Knowing the arrival times of the echoes and the speed of sound in the materials, the system calculates the thickness of all four layers simultaneously, with 3σ repeatability less than 1% for each of the layers.

### Warped wafer handling

The thin wafers/substrates used in HDFO processes can be warped significantly at several different steps in the process, most significantly by the mismatch between thermal expansion coefficients of the molding compound and the die. Warpage of 2mm or more poses a major challenge to handling and measurement systems. A specially designed vacuum chuck has three concentric vacuum zones. Applying vacuum to the zones sequentially, starting with the innermost zone and working out, the chuck pulls and holds warped wafers flat against itself to allow accurate measurements.

### Conclusions

High density fan-out packaging is essential for advancing growth in mobile and networking applications. The integration of multi-chip modules in fan-out processes requires complex processing using tools and



**FIGURE 8.** (left) Example signals of seed Cu with Cu/Ti stack. (right) Example signal of UBM with Au/Ni/Cu/Al stack.

materials that are significantly more expensive than traditional packaging lines. We have described an automated metrology solution that combines acoustic measurements with high resolution reflectometry and optical microscopy to provide comprehensive, gage-capable measurements for characterizing critical process steps in high volume production applications. Simultaneous measurement of multiple parameters

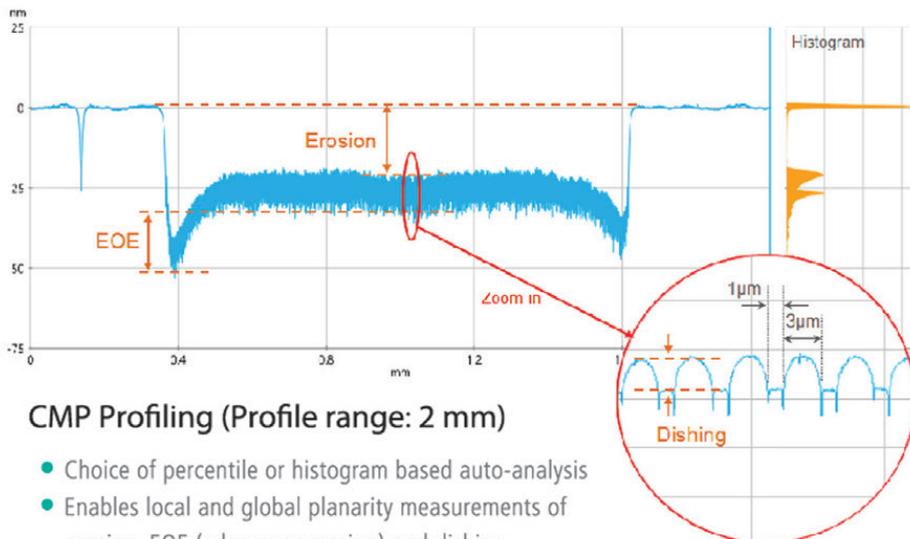
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# It's gonna be a bright, bright sun-shiny day

**ARABINDA DAS** and **JUN LU**, TechInsights, Ottawa, ON

Last year was a great year for photovoltaic (PV) technology. According to Renewable Energy World magazine, since April 2016, 21 MW of solar PV mini-grids were announced in emerging markets [1]. The exact numbers of installed solar grids for 2016 has not been published yet but looking at the data for 2015, the PV industry is growing, helped by the \$/watt for solar panels continuing to drop. The \$/watt is obtained by taking the ratio of total cost of manufacturing and the number of watts generated. According to the Photovoltaic Magazine, the PV market continued to grow worldwide in 2015. The magazine also makes reference to the newly published report by the International Energy Agency Photovoltaic Power System (IEA PVPS) programme's "Snapshot of Global Photovoltaic Markets 2015," which also states that the total capacity around the globe has crossed the 200 GW benchmark and is continuing to grow [2]. This milestone of 200 GW in installed systems is a remarkable achievement and makes us think of the amazing journey of PV technology. The technology was born in Bell Labs, around 1954, with a solar cell efficiency of just 4% [3]. By the end of the 20th century, the overall solar cell efficiency was close to 11% and the worldwide installed capacity of PV was only 1 GW [3]. Today, seventeen years later, it has soared to 200 GW, with single junction cells having efficiencies around 20% [2].

## Si-based solar cells

To celebrate this important milestone, we put TechInsights' analysis and technical databases to work to investigate the structure of solar cells of two leading manufacturers and compare them to earlier technologies. We chose to analyze Si-based solar cells only, as they represent over 85% of the global market. According to the 2016 IHS Markit report, the top three PV module suppliers in the world are Trina Solar, SunPower, and First Solar [4]. We procured panels from Trina Solar, a Chinese based company, and SunPower, an American company, and carried out a structural analysis

of these panels. These analyses helped us take a snapshot of current PV technology. We compared these two types of panels with an older panel from our database. This panel is about eight years old and was made by Kaneka (Japan). We will provide an overview of each panel and their underlying structure.

Manufacturer	Kaneka	Trina Solar	SunPower
Model	GSA-type	TSM-260PD05.08	SPR-X20-250-BLK
Technology	Thin Film	Multi-Crystalline	Mono-Crystalline
Substrate	NA	P-type substrate	N-type substrate
Nominal Power	60 W	260 W	250 W
Voltage of Open Circuit (Voc)	92 V	38.2 V	50.9 V
Short Circuit Current (Isc)	1.19A	9.00A	6.20 A
Weight	13.7 kg	18.6 kg	15 kg
Dimensions of a panel	0.99 m x 0.99 m x 0.040 m	1.65 m x 0.99 m x 0.040 m	1.6 m x 1 m x 0.046 m
Area of panel	0.98 m <sup>2</sup>	1.63 m <sup>2</sup>	1.6 m <sup>2</sup>
Efficiency	7-10%	15.9%	20.5%

**TABLE 1.** Specifications of three Si-based solar panels from three manufacturers.

**Table 1** consolidates some of the important parameters of the three panels. The SunPower panel is based on monocrystalline silicon and the Trina solar panels are based on polycrystalline silicon. The older Kaneka panel is based on amorphous Si thin film technology. The panel from Kaneka is an earlier product; their recent products are made using hybrid technology, a combination of amorphous films and polycrystalline substrates. The Kaneka panel complements very well the other two products which are based on Si crystalline wafers. The technology to fabricate the solar cells (thin film, multi-crystalline or mono-crystalline) has a direct impact on the efficiency of the cells and on their electrical parameters like

the open circuit voltage ( $V_{oc}$ ) and the short circuit current ( $I_{sc}$ ), as can be seen in Table 1. This table also shows that the Kaneka thin-film based panel has the lowest nominal power among the three. The ratio of nominal power to the light power that is received by the PV panel is indicative of its efficiency. It can be seen also that Kaneka's thin film panel has the highest open circuit voltage which is the maximum voltage available from the solar cell without any load connected to it.

Table 1 indicates that SunPower is the only one among the three that uses an n-type substrate and has the highest solar efficiency. SunPower has the lowest weight per meter-square of all the panels assessed (9.3kg).

Unlike SunPower panels, most installed Si solar panels employ a p-type substrate, even though the first silicon-based solar cells developed at Bell Labs were based on n-type Si substrates [3]. Researchers J. Libal and R. Kopecek posit that the industry transitioned to p-type substrates because the initial usage of solar cells was in space applications and p-type wafers demonstrated less degradation in the presence of cosmic rays. They suggest that for terrestrial applications there is growing evidence that n-type based solar panels are preferred over p-type based panels [5]. The reasons for choosing n-type Si substrates rather than p-type substrates are because the former are less sensitive to metallic impurities and thus are less expensive to fabricate. In general, the minority carrier diffusion lengths in n-type substrates are higher than p-type Si substrates. Also, n-type Si substrates can withstand higher processing temperatures than p-type substrates, which are prone to boron diffusion. According to the International Technology Roadmap for Photovoltaic (ITRPV), n-type based substrates will increase in prevalence and may eventually replace the p-type monocrystalline Si cells [6].

Thin film based solar panels are very different from monocrystalline Si cells. Thin film cells have the lowest efficiency and yet they too have a role to play in the PV industry. They are the most versatile; they can be coated on different substrates such as glass, plastic or even flexible substrates. The other big advantage of amorphous solar films is that they can be manufactured in a range of shapes, even non-polygonal shapes, thus they can be used in various applications. Also, thin film solar panels are not affected by high temperatures, unlike crystalline solar panels. Thin film based panels made from amorphous Si are more effective for wavelengths between 400 nm to 700 nm, which is also the sensitive spectrum of the human eye; thus they can be used as light sensors [7]. Usually, thin film panels are almost half the price of monocrystalline panels.

Amorphous silicon solar cells only require 1% of the silicon used in crystalline silicon solar cells [7].

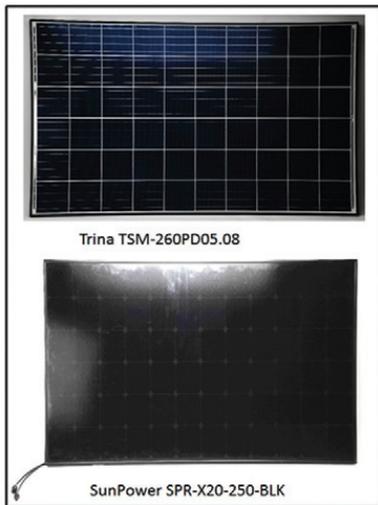
Multi-crystalline (MC) solar panels are also cheaper than monocrystalline solar panels. MC panels are made by melting raw silicon and confining them into square molds, where they are cooled. This MC-Si process does not require the expensive Czochralski process. In the early days, the cost of fabrication of MC-Si panels was higher than thin film based panels. Now, due to the major advances in fabrication technologies, these panels often have the best \$/watt, which represent the ratio of cost to manufacture to energy output [8]. It is difficult to compare \$/watt directly from different manufacturers and different types of solar panels as the technology is manufacturing is changing rapidly and often the most recent products of a manufacturer are not compared. A more sensible factor of comparison would be the ratio of total kilowatt-hours the system generates in its lifetime divided by the cost per square unit of the panel. To make a detailed estimation even the installation cost and tolerance to shade, overall reliability must be included in the calculations, which is beyond the scope of this article.

### Solar panel overview

**FIGURE 1** shows the panel from Kaneka. It indicates that the Kaneka solar panel cells are long strips that run across the whole length of the panel. The color of the panels is a shade of purple. The Kaneka Solar which is amorphous Si-based, has a very uniform color. The inherent structure of amorphous Si-films has many structural defects because they are not crystalline and thus are tolerant to other defects like impurities during manufacturing, unlike crystalline based panels [7]. The color of the thin film panels is strongly thickness dependent because thickness affects the light absorption. A solar cell's outward appearance can range from blue to black and is dependent on the absorption and reflectivity of their surface. Ideally,



**FIGURE 1.** Kaneka Solar panels from three leading Si-based PV manufacturers.



**FIGURE 2.** Solar panels from Trina Solar and SunPower.

if the cell absorbs all the light impinging on the surface it should be black. **FIGURE 2** shows the panels from Trina solar and Sunpower. The Trina Solar panel has a blueish color and each cell is perfectly square. The SunPower SPR-X20-250-BLK solar cell has a uniform blackish color. The spacing between the cells, the interconnect resistance, the top contacts

and the materials used for the connections affect the overall performance of the panel. All three manufacturers connect their cells within a PV module and PV modules within an array in a series configuration.

Manufacturer	Kaneka GSA-60W	Trina Solar TSM-260PD05.08	SunPower SPR-X20-250-BLK
# Cells in the panel	108	60	72
Rows	1	6	6
Columns	108	10	12
Spacing between cells	0.55 mm	3 to 5 mm	5 mm
Cell length	95 mm	156 mm	128 mm
Cell width	8.30 mm	156 mm	128 mm

**TABLE 2.** Cell specifications of three Si-based solar panels from three manufacturers

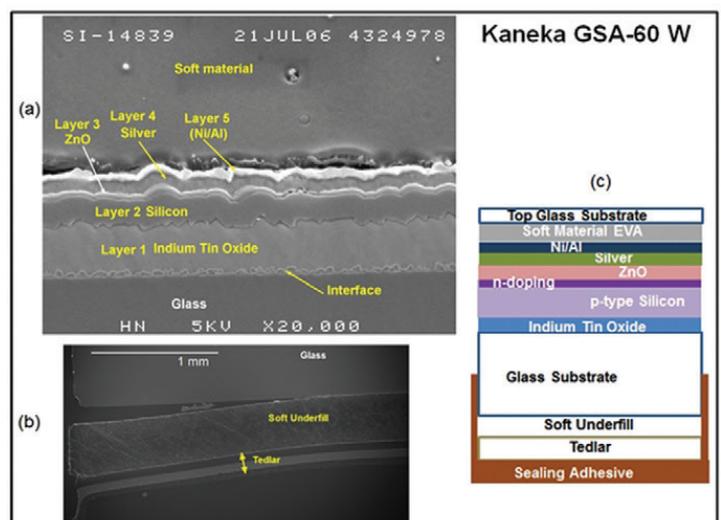
**Table 2** summarizes the cell dimensions for the three manufacturers. Kaneka panels have the narrowest space (0.55mm) between the cells. The Trina solar panel has a 3 mm wide gap and a 5 mm gap, between two adjacent solar cells, in the horizontal and vertical direction respectively. These gaps are used for bus electrodes. In the SunPower solar panel, the metal grid is placed on the back surface eliminating metal finger width as a layout constraint. This design significantly reduces the finger resistance and improves the series resistance.

For all panels, interconnects are made between the cells. The metallization and interconnects between the cells is a field of technology on its own. There are various techniques like lithography, laser grooving and printed contacts and these details are discussed more in detail elsewhere [9, 10, 11].

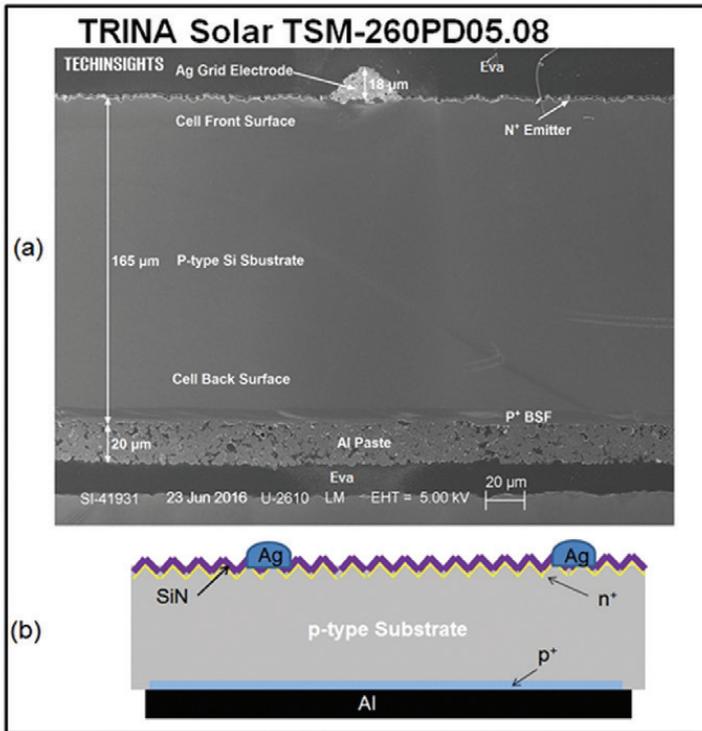
## Solar panel cross-sections

In this section, we look into the layers deposited on the substrates. Cross-sectioning these big panels is not a trivial feat. These panels are covered with tempered glass and shatter during sawing and cross-sectioning. To extract a small rectangular piece requires patience and involves sawing and grinding processes. In most cases, the glass was removed before doing the cross-section. **FIGURE 3** illustrates two SEM cross-sectional images and one schematic drawing. The SEM cross-sectional images show the top and bottom part of the Kaneka solar cell. In figure 3(a), the active layers comprise indium-tin-oxide, an amorphous silicon layer capped with zinc oxide, silver and a very thin layer of Ni-Al. On top of the Ni-Al film, solder is deposited. Ni-Al provides better adhesion to solder. Two electrical contacts are made between the cells, one to the indium-tin-oxide for the back contact and the other to the Ni-Al layer. Figure 3(b) exposes the layers under the glass substrate. The rear surface of the glass substrate is covered by a soft material such as EVA (ethyl-vinyl-acetate), which in turn is covered by a rear Polyvinyl Fluoride (PVF) layer called the backsheet (Tedlar or similar). EVA is also used on the top surface (figure 3(a)). The usage of these layers is standard practice in the PV industry. The main function of these layers is that they are impervious to moisture and are stable under prolonged exposure to sunlight. On the front side, EVA also helps to reduce reflection and provides good adhesion between the top glass and the solar panels. Figure 3(c) shows the complete stack in the Kaneka solar cell.

**FIGURE 4** presents the stack of materials on the multi-crystalline substrate of the Trina Solar panel. The



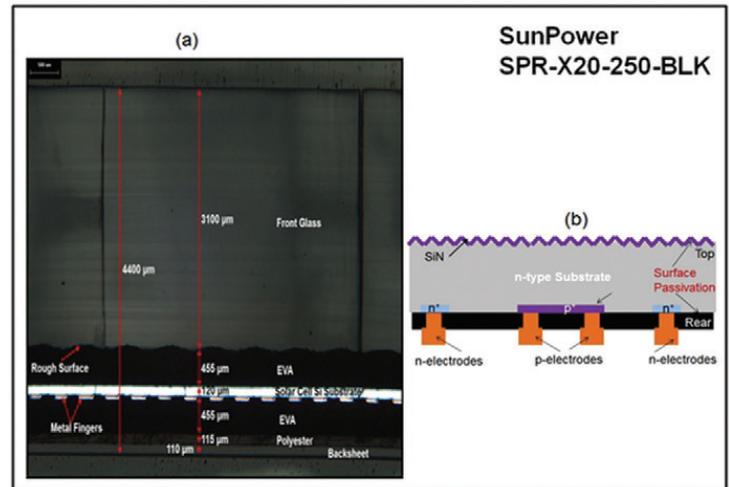
**FIGURE 3.** Cross-section of Kaneka solar panels; a) top portion of the solar panel, b) bottom portion of the solar panel, c) representative schematic of the cell.



**FIGURE 4.** Cross-section of Trina solar panel; a) layers in the solar panel, b) representative schematic of the cell.

substrate is p-type and has a very thin phosphorous doped region near the top surface. This n-doped region forms the PN junction. A silicon nitride anti-reflective coating layer is deposited on top of the substrate and in designated areas the passivation is opened and silver is deposited to make electrical contact to the n-doped regions. At the bottom of the multi-crystalline substrate, there is also a thin region of high p-doping concentration and this forms the back surface field layer. This solar cell module is fabricated using passivated emitter and full metal back-surface-field (BSF) technology. BSF technology is implemented to mitigate rear surface recombination and this is done by doping heavily at the rear surface of the substrate. This high doping concentration keeps minority carriers (electrons) away from the rear contact because the interface between the high and low doped areas of same conductivity acts like a diode and restricts the flow of the minority carriers to the rear surface. Passivated emitters in the front side and BSF layer on the rear side improve the efficiency of the cells. Figure 3(b) is the schematic representation of the cell without the EVA and PVF layers.

**FIGURE 5** shows an optical cross-section of the SunPower cell. Figure 5(a) shows that SunPower employs a backside junction technology with interdigitated backside p-emitter and n-base metal. This means that both the contact's n and p-electrodes are at the bottom of the substrate and are placed in an alternating manner. Having all the metal contacts on the rear side has two big advantages:

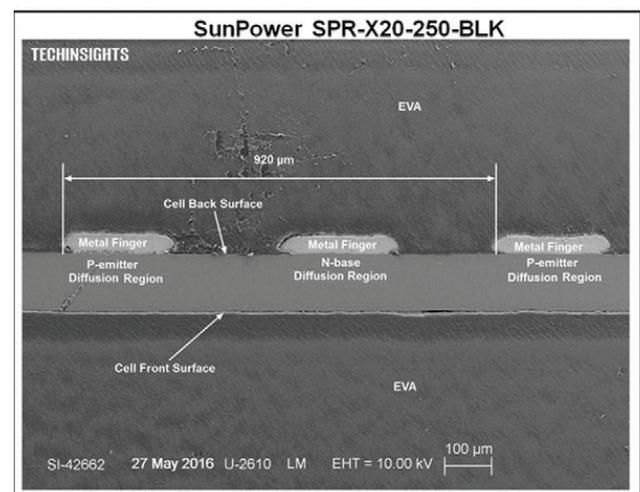


**FIGURE 5.** Cross-section of SunPower solar panel; a) Layers in the solar panel, b) representative schematic of the cell.

1. Metallic contacts are reflective and occupy space that can be used to collect more sunlight; transferring these contacts to the rear side improves the cell efficiency and also leaves the front surface with a uniformly black color, which is more aesthetic for the home users.
2. It reduces bulk recombination. The mono-crystalline substrate is only 120 μm thick. It is designed so that the carrier is generated close to the junction. The substrate is n-type and p-electrodes are formed by localized doping on the bottom part of the substrate.

Figure 5(b) illustrates the general structure of the cell.

**FIGURE 6** depicts a SEM cross-section of the metal fingers that connect to the interdigitated electrodes. The pitch between the metal fingers is 920 μm and repeats over the entire back surface of the panel.



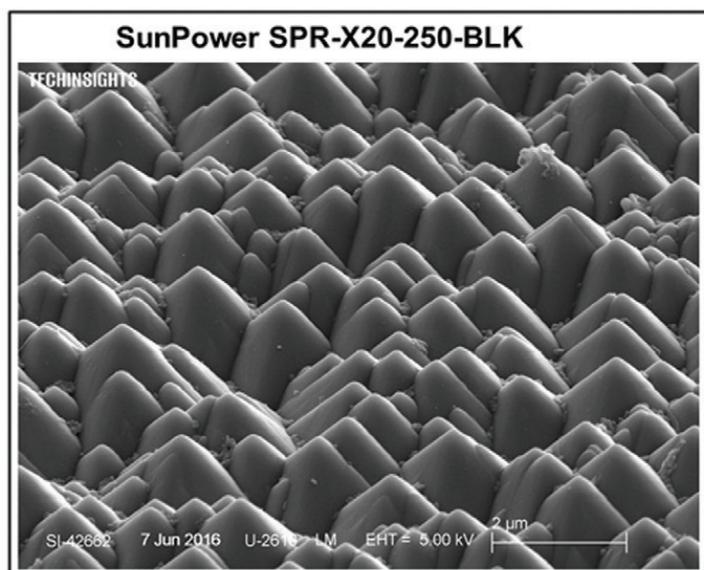
**FIGURE 6.** Cross-section of SunPower solar panel showing interdigitated contacts at the rear part of the panel.

All three manufacturers employ some sort of surface texturing along with anti-reflective coatings to reduce reflection but SunPower uses the most advanced technology for surface texturing. **FIGURE 7** illustrates a SEM topographical image of the front surface texture of the monocrystalline substrate having pyramids, which are etched into the silicon surface. These faceted surfaces increase the probability of reflected light entering back to the surface of the substrate. A similar concept is also applied to the back surface.

### The future is sunny and bright

Of the three panels we analyzed, SunPower solar panels employ the most advanced technologies and they illustrate how the solar cell has evolved over the ages. It started from a simple PN junction, then passivated emitters were introduced along with local back-surface-field (BSF) technology, which came to be known as Passivated-Emitter with Rear Locally (PERL) diffused technology. In contrast, today the most advanced technology is interdigitated back contacts along with passivated contacts.

In addition to these advances, there is great progress in tandem cells and multi-junctions to capture the different wavelength regions of the sun's rays. A recent article in IEEE spectrum magazine presented the state of art of record-breaking PV cells made with different techniques such as thin film, crystalline Si, single junction, multi-junction cells. PV cells especially the multi-junction cells, have now crossed the 50% efficiency barrier [12]. Similarly, a publication from the alterenergy.org has collected all the major advances made in PV technology and discusses concepts like colloidal quantum dots and GaAs for cell technology,



**FIGURE 7.** Topographical image of the front surface of the SunPower solar panel.

along with new applications [13]. Today, we regularly read about new materials (like perovskites) and come across new techniques that improve solar panel efficiencies, including new manufacturing methods to reduce the overall cost of fabrication. Moreover, PV cells are used in an innovative manner. The installation of PV panels is no more restricted to isolated rooftops or solar farm. An article in the Guardian made a reference to a solar panel road in Normandy, France [14]. At TechInsights, we will continue to keep an eye on emerging solar cell technologies.

The efforts emerging from various organizations all over the world are very encouraging. There are indeed many challenges for renewable energy to overcome before fiscal parity with fossil fuels is achieved; particularly for PV energy. Nevertheless, there is an increased focus on climate change issues. This has resulted in a significant amount of resources being allotted to PV technology in many countries, especially in developing countries such as China, India, and Brazil [1, 2]. This optimistic scenario reminds us of the song “I Can See Clearly Now” by the 1970s American singer Johnny Nash, where the refrain runs optimistically, “It’s gonna be a bright, bright sun-shiny day.”

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# Understanding the impact of valve flow coefficient (Cv) in fluid systems

**STEPHANE DOMY**, Saint-Gobain Performance Plastics,

## *Understanding the impact of valve flow coefficient (Cv) in fluid systems for microelectronics manufacturing*

**W**hen scaling up, or down, a high-purity liquid installation – many complex factors need to be considered from ensuring the integrity of the transported product to the cleanliness of the environment for both the safety of the process and the operator [1]. In my 15 years working in the semiconductor fluid handling component industry, I've learned that the Cv is a bit misunderstood. Given the Cv formula can be used for any flow component in a fluid line, most are familiar with it, yet few consider how it relates to their specific installation. Therefore, this article will focus on factors that pertain to achieving a specific flow performance and specifically the flow coefficient (Cv) as it relates to valves.

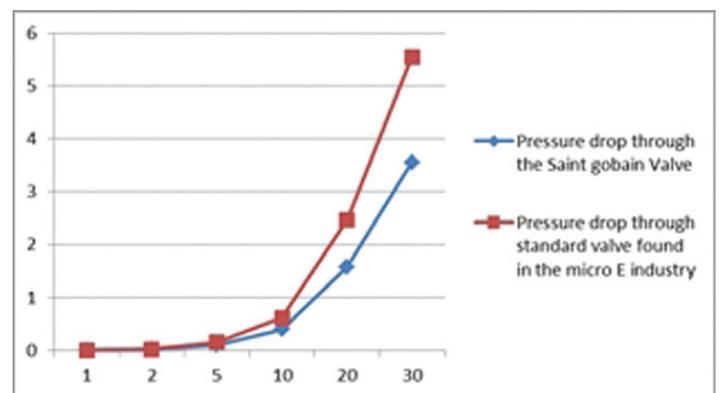
### **Cv empirical explanation and more**

As we know, when working on a turbulent flow the Cv formula is:  $Cv = Q\sqrt{SG / \Delta P}$  where Q is the flow going through the valve in gallons per minute (GPM), SG is the specific gravity of the fluid and  $\Delta P$  is the pressure drop in PSI through the component. In the semiconductor industry, due to the low velocity of the transported fluid the high purity chemistry and slurries are mostly in a semi-turbulent state or a laminar state. Yet you'll notice there is not a single link to the viscosity of the transported product in the Cv formula. This is significant given the viscosity directly impacts the Cv value when the flow is in a semi-turbulent or laminar mode. Consider that if you calculate the pressure drop in your system with the formula above you could end up with a result that is 4 to 5 times lower. No doubt this inaccuracy can cause significant issues in your installation.

To take this further, let's analyze how pressure drop based on flow evolves through a valve by comparing a Saint-Gobain Furon® Q-Valve (½" inner flow path and ½" pipe connection) to a standard semiconductor industry valve

of the same size. The Saint-Gobain valve, which meets the requirements of the semiconductor industry (metal free, 100% fluoropolymer flow path and so on), has a Cv of 3.5 – one of the best for its dimensions. To ease the calculation, we will use deionized (DI) water, which will free us of the specific gravity or impact of the viscosity if we are not in the right state.

As we can see on the graph in **FIGURE 1**, at a normal flow rate used in micro-e for ½" 5 to 10 lpm; the pressure drop difference between a standard valve and a Saint-Gobain valve is in the range of 0.1 to 0.3 PSI. At first glance, this does not appear to be much. However, let's factor in a viscous product and that you have a number of these lines in your flow line -- now the numbers start to accumulate. And by moving from a standard valve to a Saint-Gobain valve, as described above, you start to see a significant difference in pressure drop, which could occur across your installation. That being said, up to a certain limit (defined by another component in your installation, such as your pump pressure capability or some more delicate device) an "easy" counter is to increase the pressure through put of your pump but it is at the expense of wasting energy and adding the potential for additional shearing or particle



**FIGURE 1.**

generation in your critical fluid. Now that we have reviewed, the impact of the Cv on our flow and how this could impact our installation, let's see what can potentially impact the Cv.

### Design impact on Cv and resulting trade-off

The first impact that may come to mind is a larger orifice – and it's correct. The size of the orifice can benefit flow through and directly relates to the volume of your valve. However there are trade-offs for this improved Cv. The first is cost increase. A higher volume requires a larger valve, which can cost up to 50% more than the initial valve due to specific material and process requirements. Additionally, as highlighted in "Design Impact for Fluid Components" by increasing the size of the component (due to the specific micro-e material requirements), you could lose pressure rating performance [1]. Also when increasing the inner volume of your valve, you potentially increase volume retention as well as particle generation, given that using larger actuation systems results in more points of contact and creates a hub for generating particles. Another possible drawback is significant velocity loss, but that will have to be addressed in another article. The critical point to be taken here is the importance of choosing the right size orifice – too small and flow can be restricted too much and too big and you may end up paying for other problems.

Another potential impact to Cv is the difference in valve technology. Though there more, I'll specifically cover stopcock/ball valves, weir style valves; and diaphragm valves. Other valve technologies, such as the butterfly valve, will not be discussed because their construction materials are generally not used for fluid handling components for the semiconductor industry.

Starting with the simplest design, the stopcock/ball valve provides by far the best Cv of the three technologies mentioned. Considering the premium Cv achieved, you would assume they are expensive. Instead they are generally the cheapest of the three values mentioned. One drawback in using stopcock valves is the need for a liquid oring on the fluid path which may create compatibility issues. The exception is the Furon® SCM Valve, a stopcock valve that employs a PFA on PTFE technology and allows for oring-free sealing. Additionally, stopcock valves can lower pressure/ temperature ratings and have a tendency to generate a great deal of particles when actuated. This occurs when the key or ball is rotating inside the valve body. Both drawbacks are related to the PTFE/PFA construction materials required for the flow path by the micro-e industry.

The weir style valve, if done properly, should provide a very good Cv – perhaps not as good as a stopcock/ball valve, but still very good. And although liquid orings are not an issue,

these valves have other drawbacks. In a weir style valve the diaphragm is generally a sandwich structure consisting of a thin layer of PTFE that is backed by an elastomeric component in which a metal pin is embedded to connect the membrane to the valve actuating system. It is the sandwich materials that generate a number of potential issues when used on critical, high purity chemistry. Specifically, the delamination of the sandwich creates the possibility of multiple points of contamination to the liquid (metal & elastomer). In addition, the significant surface contact between the membrane and the valve seat, which is necessary to secure a full seal, generates a lot of particles – though significantly less than a stopcock/ball valve.

The diaphragm valve is the most commonly used valve in the semiconductor industry as it offers a great balance in terms of the issues previously identified: potential contamination, materials and particle generation. The trade-off is that the construction of these valves is more complex and as a result they are priced higher than the average cost of the other valves. Additionally, the Cv performance is well below a stopcock/ball valve and slightly below a weir style valve. However, by using Saint-Gobain's patented rolling diaphragm technology this does not have to be an issue. In fact, with this technology, we can offer the equivalent Cv of a weir style valve in combination with premium pressure and temperature capabilities as well as the cleanest valve technology – all of which allows for a system design with the lowest impact possible on the transported fluid.

As demonstrated in this document, understanding the Cv rating and the impacts that could affect that rating as it relates to valves is critical when optimizing an installation for fluid and energy efficiency. Cost aside, there are a number of issues that are unique to the semiconductor industry that ultimately guide and often restrict installation choices, such as: dead volume, particle generation, cleanliness as well as the physical and mechanical properties of appropriate polymers. Additionally, choosing the appropriate valve for your installation goes far beyond the simple notion that if "I need more flow, I will get a larger valve." Most likely the residual effect of that choice will affect the performance of the system, particularly regarding cleanliness. Instead critical adjustments to your valve actuation mechanism and valve flow path designs as well as to your valve technology may allow you to achieve the required results – even if the installation still uses the same ½" valve...but more on this point in another article.

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# The ConFab 2018 will be held May 20-23

The ConFab 2018, to be held May 20-23 in Las Vegas at THE COSMOPOLITAN of Las Vegas, will take a close look at the new applications driving the semiconductor industry, the technology that will be required at the device and process level to meet new demands, and – perhaps most importantly – the kind of strategic collaboration that will be required. It is this combination of business, technology and social interactions that make The ConFab so unique and so valuable. Here are six key trends that will each have a huge impact in the near future:

- The semiconductor industry is on the cusp of a new era of growth, driven by a diverse array of applications. Much of the growth will come from the need for better connectivity and more intelligent data analysis.
- In the Internet of Things (IoT), data is captured by sensors and transferred via the appropriate networks, stored in data centers and analyzed. This creates demand for high performance computing, including artificial intelligence and “deep learning.” New computational methods are emerging, such as neuromorphic methods that mimic how the brain works.
- Faster communication with higher bandwidth will be required. 5G wireless communication is coming, as is improved WiFi, near-field communication, Bluetooth and satellite communication.
- Huge opportunities exist in automotive electronics, as autonomous driving moves closer to reality.
- Virtual reality will be combined with artificial intelligence to create a truly immersive experience that mankind has never experienced.
- Semiconductors will play an increasingly important role in the healthcare industry, as diagnostic tools and patient monitoring.

To meet the demands of these diverse applications, much innovation will be required on the technology side. Huge efforts are also needed to reduce the overall cost. Since the beginning, the economics of semiconductor manufacturing has been a focal point of The ConFab. In 2018, we will be including insights into the emerging and rapidly growing new markets and what semiconductor device manufacturers need to know to successfully tap into those markets.



**PETE SINGER**, *Editor-in-Chief*



New technology needed in manufacturing will be another focal point of The ConFab. EUV is finally entering volume production, ushering in a new era of patterning for the 7 and 5nm generations. Many new materials are being considered, transistors are evolving from FinFETs to gate-all-around nanowires, on chip communication with silicon photonics will soon emerge, and advanced packaging/heterogeneous integration is ever more critical.

There is a strong need for strategic collaboration across the entire supply chain. Empowering that collaboration is a high priority goal for The ConFab 2018. We do that through private, pre-arranged meetings among interested parties. The ConFab also includes well-attended evening receptions plus breakfasts, lunches and refreshment breaks. These offer exceptional networking opportunities for people to meet in a relaxed environment.

In 2018, we expect heightened interest and involvement as we explore how businesses, people and technology must all work together to meet the world’s insatiable demand for new electronics.

To inquire about participating – if you represent an equipment, material or service supplier, contact Kerry Hoffman, Director of Sales: [khoffman@extensionmedia.com](mailto:khoffman@extensionmedia.com). To inquire about attending as a VIP, contact Sally Bixby, Events Director: [sbixby@extensionmedia.com](mailto:sbixby@extensionmedia.com). ◀

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### Start Planning Now to Attend The ConFab 2018:

- Blending a focus on the economics of semiconductor manufacturing and design, The ConFab 2018 will go beyond and connect-the-dots to the end semiconductor application space, such as: **IoT, AI, 5G, VR, and automotive**
- We'll look closely at new applications, technology required at the device and process level, and strategic collaboration needed to leverage **emerging opportunities** and **critical market trends**
- A distinctive combination of business, technology and social interactions makes this a **uniquely valuable conference and networking event** that industry leaders and decision-makers can't afford to miss

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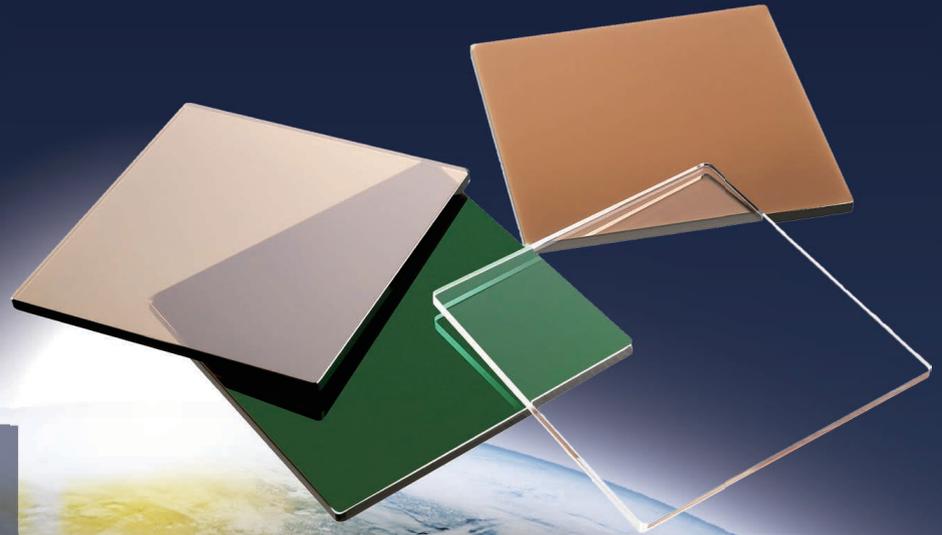
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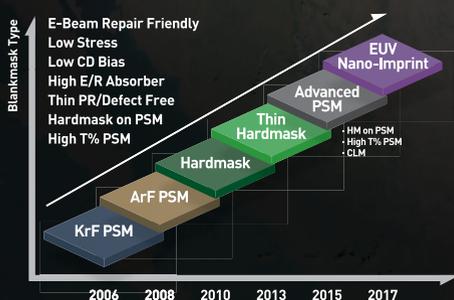
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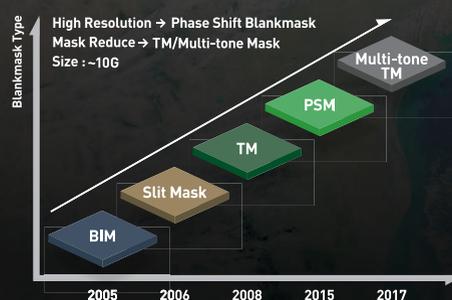
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