SEMICONDUCTORS • PACKAGING • MEMS • LEDS • DISPLAYS

NOVEMBER 2012

Solid State TECHNOLOGY®

Insights for Electronics Manufacturing

IEDM Preview: 20nm and Below P. 14

www.solid-state.com

PennWell

SEMICONDUCTORS • PACKAGING • MEMS • LEDS • DISPLAYS

NOVEMBER 2012

Solid State TECHNOLOGY®

Insights for Electronics Manufacturing

IEDM Preview: 20nm and Below P. 14

www.solid-state.com

PennWell

ADVANCED PACKAGING SINGLE WAFER WET PROCESSING

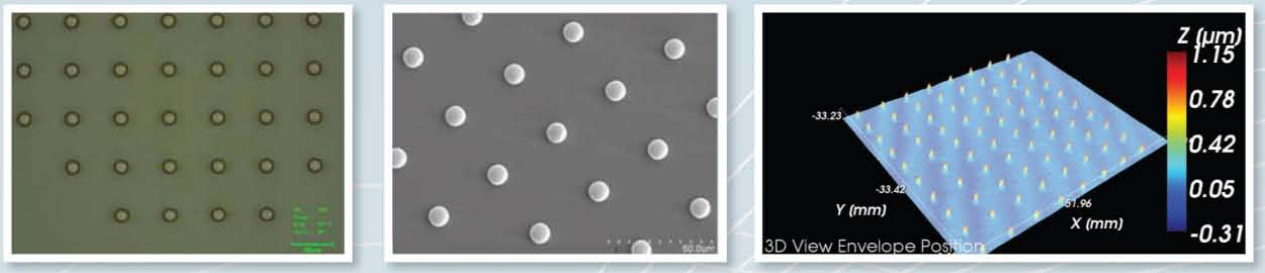
Solid State Equipment LLC

ADVANCED PACKAGING
SINGLE WAFER
WET PROCESSING

TSV RESIST STRIP AND CLEAN

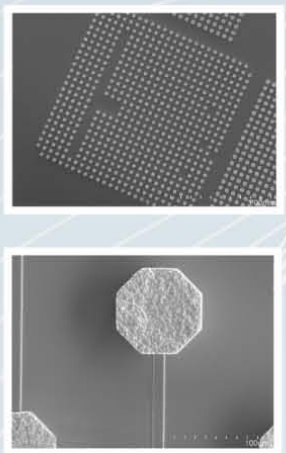
As received – post DRIE | After SSEC Cleaning | As received – post DRIE | After SSEC Cleaning | As received – post DRIE | After SSEC Cleaning

Si ETCH TO REVEAL Cu TSV

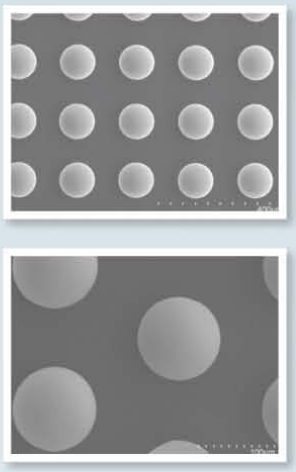


Optical | SEM | ISIS 3D

DRY FILM STRIP



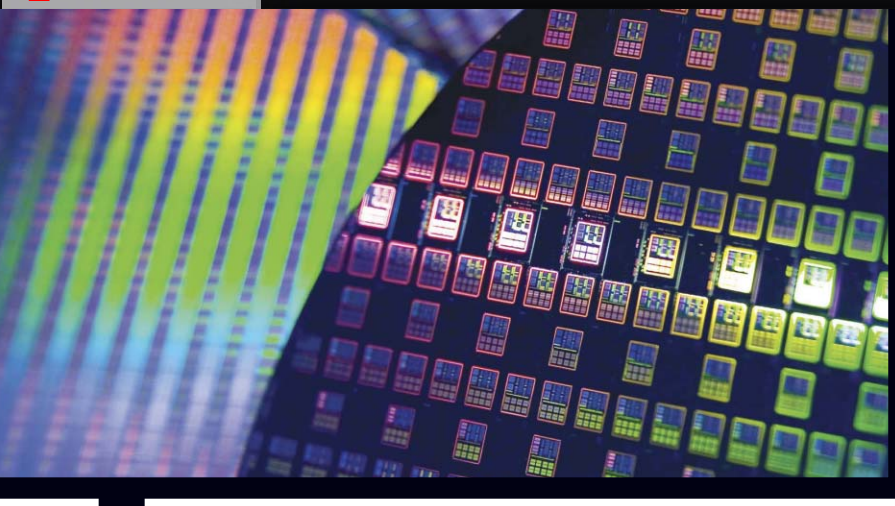
FLUX CLEANING



UBM AND RDL METAL ETCH

UBM Post Etch | UBM Post Strip

ssecusa.com



Solid State TECHNOLOGY®

NOVEMBER 2012 VOL. 55 | NO. 9

Processed wafers add a near-magical quality to reflected light. Source: TSMC.

COVER

FEATURES

COLUMNS

DEPARTMENTS

online@ www.solid-state.com

Web Exclusives

EUV Symposium takeaways

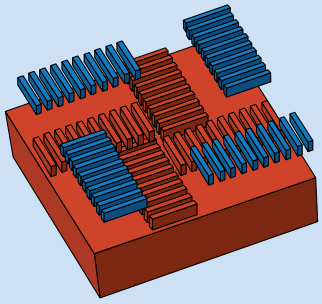
Reporting from the International Symposium on Extreme Ultraviolet Lithography, industry analysts and host imec gauge the pace of improvements in EUV lithography and its long march toward production readiness. Bottom line: Progress is still slow and steady, but much improvement is expected in early 2013 with the next generation of tools. **http://bit.ly/SPoip9**

European consortia, ASML, supplier network plan for 450mm transition

At SEMICON Europa, European government representatives, consortia, and suppliers discussed programs to support and participate in the 450mm wafer-size transition — including a comprehensive presentation from ASML about its roadmap for 450mm EUV platforms. **http://bit.ly/Ve840o**

Process Watch:

Taming the overlay beast



Experts from KLA-Tencor discuss overlay registration and new capabilities to align to buried layers. **http://bit.ly/PIWxts**

LED industry shifting production to 6-inch wafers

Driven by market demand and cost-savings goals, the semiconductor industry is progressing toward consensus on building-block standards for automating LED production on 6-in wafers, writes Paula Doe in *SST*'s sister magazine *LEDs Magazine*. **http://bit.ly/PKsoQp**

n&b news and blogs

Moving forward with Moore's Law: Throughput of EUVL scanners

Dr. Vivek Bakshi asks: How much do we need to increase EUV throughput, what must be done to accomplish that, and how quickly can it be achieved? **http://bit.ly/SPMoQA**

Insights from the Leading Edge

Dr. Phil Garrou takes a closer look at some of the 3D and advanced packaging papers presented at the recent 45th Symposium on Microelectronics (IMAPS 2012). **http://bit.ly/QdGRo8**

MEMS in medical, quality-of-life

Karen Lightman from the MEMS Industry Group talks with Freescale Semiconductor's Jeannette Wilson about a panel discussion at the MEMS Executive Congress. **http://bit.ly/RNxbmy**

GlobalFoundries' 14nm finFET "eXtreme Mobility" process

Chipworks' Dick James digs into the technical details of GlobalFoundries' 14nm finFETs, and how they stack up against what Intel and TSMC will be offering. **http://bit.ly/QR5OZ0**

Residual Gas Analyzers ...

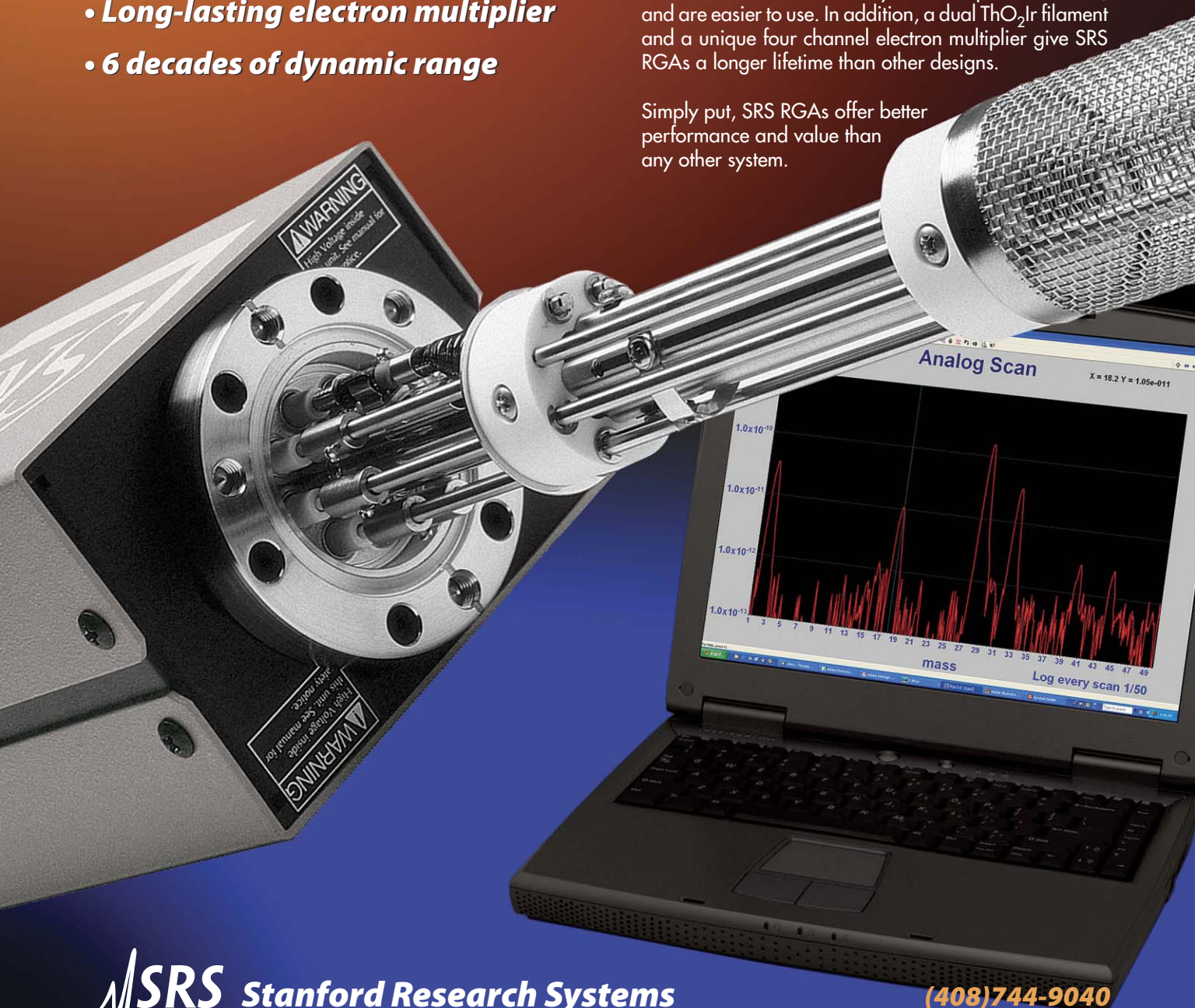
... starting at $3750

- 100, 200, 300 amu models
- Sensitivity to 5 x 10^{-14} Torr
- Better than ½ amu resolution
- Dual ThO_2Ir filament
- Long-lasting electron multiplier
- 6 decades of dynamic range

Residual Gas Analyzers from SRS are designed to handle the toughest environments from basic research to semiconductor process monitoring. Thousands of SRS RGAs are in use worldwide, and have earned us a reputation for producing quality vacuum instrumentation at reasonable prices.

Our RGAs have greater dynamic range, higher resolution and better linearity than competitive models, and are easier to use. In addition, a dual ThO_2Ir filament and a unique four channel electron multiplier give SRS RGAs a longer lifetime than other designs.

Simply put, SRS RGAs offer better performance and value than any other system.



SRS Stanford Research Systems

(408)744-9040
www.thinkSRS.com

editorial

Forecast for 2013

Nobody can predict the future, of course, but 2013 is shaping up to be a good year for the semiconductor industry and its suppliers. According to SEMI, total fab spending for equipment needed to ramp fabs, upgrade technology nodes, and expand or change wafer size could increase 16.7 percent in 2013 to reach a new record high of $42.7 billion. The estimate includes new equipment, used equipment, or in-house equipment but excludes test assembly and packaging equipment (which, if included, would bring the number up to about $50 billion). The market for semiconductor manufacturing materials, which was $48.6 billion this year, is expected to grow 4% to more than $50 billion in $2013.

There's been some hand-wringing in 2012 about continued consolidation and the number of companies that will be moving to 450mm: most pundits guess that only 5-7 companies will be able to make the move. However, that's a limited view of the industry, since there are hundreds of facilities around the world cranking out chips, LEDs, optoelectronics, power devices, MEMS and other components. The latest edition of the SEMI World Fab Forecast lists over 1,150 facilities (including 300 opto/LED facilities), with 76 facilities starting production in 2012 and in the near future.

> I'm bullish on opportunities in healthcare, such as body area sensor networks

There's sure to be much talk in 2013 about technology requirements at the leading edge, including the 450mm transition, progress in EUV, 3D integration and FinFET optimization. Sustainability will be key, with an emphasis on reducing power consumption, which means lower leakage currents and reduced Vdd.

The demand for semiconductors will never be higher, particularly as the middle class rise on dominance in places such as Brazil, Russia, India and China. First on the wish list it seems, after shelter, food and clothing, is a smart phone.

After a trip to imec in Leuven, Belgium, I'm particularly bullish on opportunities in healthcare, which range from body area sensor networks to amazingly advanced labs-on-a-chip that can screen 20 million blood cells per second to find a single tumor cell in 5 billion blood cells. It is these kinds of applications that could lead to a new revolution in how electronics are designed and manufactured.

—Pete Singer, Editor-in-Chief

Solid State TECHNOLOGY®

Susan Smith, Group Publisher
Ph: 603/891-9447, susans@pennwell.com

Pete Singer, Editor-in-Chief
Ph: 603/891-9217, psinger@pennwell.com

James Montgomery, News Editor
Ph: 603/891-9109, jamesm@pennwell.com

Robert C. Haavind, Editor-at-Large
Ph: 603/891-9453, bobh@pennwell.com

Julie MacShane, Copy Editor

Phil Garrou, Contributing Editor

Michael Fury, Contributing Editor

Justine Beauregard, Marketing Manager

Cindy Chamberlin, Presentation Editor

Katie Noftsger, Production Manager

Dan Rodd, Illustrator

Debbie Bouley, Audience Development

Marcella Hanson, Ad Traffic Manager

EDITORIAL OFFICES

PennWell Corporation,
Solid State Technology
98 Spit Brook Road LL-1,
Nashua, NH 03062-5737;
Tel: 603/891-0123; Fax: 603/891-0597;
www.ElectroIQ.com

PennWell®

CORPORATE OFFICERS

1421 South Sheridan Rd., Tulsa, Ok 74112
Tel: 918/835-3161
Frank T. Lauinger, Chairman
Robert F. Biolchini, President and CEO
Mark Wilmoth, Chief Financial Officer

TECHNOLOGY GROUP

Christine A. Shaw, Senior Vice President and Publishing Director

For subscription inquiries:
Tel: (847) 559-7500; Fax: (847) 291-4816;
Customer Service e-mail: sst@omeda.com;
Subscribe: www.sst-subscribe.com

CONNECT. COLLABORATE. CREATE.

CONNECT *with the right people.*
COLLABORATE *in the right environment.*
CREATE *alliances, partnerships and strategies for a stronger future.*

The ConFab®

Presented by: Solid State TECHNOLOGY Insights for Electronics Manufacturing

CONNECT… It's remarkable what can happen when you get the right people together.

That's why CEOs, CTOs, VPs of Operations and Manufacturing, Fab Managers and other executives from companies like Intel, GLOBALFOUNDRIES, Texas Instruments, Samsung, Broadcom, IBM, TSMC and more attend The ConFab.

Don't miss the 9th Annual ConFab, presented by Solid State Technology!

Coming to the Encore at the Wynn in Las Vegas from June 23 to 26, 2013.
Visit **www.theconfab.com** today to learn more and pre-register or to apply to attend as our VIP guest.

Owned & Produced by: PennWell®

www.theconfab.com

Please send news articles to jamesm@pennwell.com

news

worldnews

USA | **Tezzaron Semiconductor** is taking over **SVTC Technologies'** wafer fab in Austin, TX.

USA | Devan Iyer, director of Semiconductor Packaging in **Texas Instrument**'s Manufacturing Group, has joined the advisory board of The ConFab.

WORLD | **Imec** plans to start construction of a 450mm pilot line next year, with early production focused on sub-10nm devices starting at the end of 2016.

WORLD | **Imec**, Holst Centre, and **Panasonic** have developed a new prototype of a wireless EEG (electroencephalogram) headset.

USA | **Solvay Specialty Polymers USA** has extended its line of high-performance polyester compounds with a new version targeting light-emitting diode (LED) TVs with higher heat and light stability.

WORLD | **ON Semiconductor** has joined imec to collaborate on the development of next-generation GaN-on-Si power devices.

WORLD | The market for semiconductor magnetic sensors used in industrial and medical applications expanded by 6% in 2011 to $118.2 million, with green energy initiatives acting as a major growth driver, according to **IHS iSuppli**.

ASIA | **GaN power device developer Transphorm Inc.** has secured a $35M Series E financing round led by the Japanese government-backed Innovation Network Corporation of Japan (INCJ), and Nihon Inter Electronics Company with whom it has signed a second-source manufacturing deal.

Analyst: Fab spending softness 2012 extending into 2013

Fab equipment spending continues to soften in 2012, but don't hope for a reprieve until later in 2013.

Worldwide wafer fab equipment (WFE) spending is projected at $31.4 billion in 2012, a -13.3% decline from 2011, according to Gartner. But counter to some other industry watchers, the firm now thinks there won't be a big rebound in 2013 — it's now forecasting a -0.8% slip next year to $31.2B, before finding its footing again and bouncing back in 2014 with 15.3% growth to $35.9B.

Earlier this summer Gartner foresaw an -8.9% decline in 2012, followed by 7.4% growth in 2013. In September SEMI predicted 2013 could be a "golden year" with nearly 17% growth in fab spending.

"The outlook for semiconductor equipment markets has deteriorated as the macro economy has weakened," stated Bob Johnson, research VP at Gartner. After starting the year strong thanks to sub-30nm production ramps at foundries and other logic manufacturers, demand for new equipment logic production will soften as yields improve, leading to declining shipment volumes for the rest of the year."

Fab utilization rates will erode to the low 80% range by the end of this year, slowly increase to about 87% by the end of 2013. (That's less optimistic than Gartner's June outlook which saw mid-80% in mid-2012 and 87% by the end of the year.) Leading-edge capacity will recover slightly better, hitting the high-80% range by year's end and gradually getting into the low-90% range as 2013 progresses.

Increased demand combined with less-than-mature yields at the leading edge had been hoped to consume extra capacity and raise utilization rates. In leading-edge logic that has in fact helped create inventory shortages, Johnson noted, but "not enough to bring total utilization levels up to desired levels. In the memory segment, some suppliers are even cutting production in an attempt to shore up weak market fundamentals."

Memory is expected to be weak through 2012, with strong declines in DRAM investments and a virtually flat NAND market, the firm notes. Foundry spending has been revised downward for both 2012 and 2013; some foundries have improved their 28nm yields, but mainly for SiON technology, as 28nm high-*k*/metal gate (HKMG) processes are still yielding below normal. Longer-term, Gartner thinks foundries will ratchet up their spending more in future years due to aggressive development of EUV lithography and 450mm wafer processing. **— J.M.**

TV makers expanding low-brightness LED backlit models into entry-level market

When LCD TVs were first competing against plasma TVs, one key differentiating argument was their brightness. Typical TVs have brightness measuring around >400 nits (1 nit is roughly 1 candela per m^2), which is deemed suitable for TVs typically viewed in a living room and at a distance. Plasma TVs' full-white brightness is typically sub-200 nits; <300 nits is more typical of computer/laptop screens.

However, the trend in LCD TVs is now swinging toward lower brightness, according to DisplaySearch senior analyst Jimmy Kim. Most existing low-brightness TV models were small and targeted the secondary market, but earlier this year first trials began for low-brightness TV models, with low-cost direct LED backlighting, in the main segment of large TVs, he notes. The tradeoff is sacrificing design and picture quality for cost — lower brightness for the LED component, and a thinner light guide plate. These efforts have reduced the cost gap between LED and CCFL backlights to <1.3×, so pricing is similar. (A spike in CCFL materials prices is another reason for the shrinking cost difference.)

Consumers have responded enthusiastically, and low-brightness LED-backlit TVs accounted for more than 10% of total LCD TV shipments in 2Q12. So TV makers are now planning more models with low brightness, even those using edge LED backlights. Most mainstream TV models are now being designed with ~350 nits, and some entry-level models will be as low as 250 nits, to fend off the charge of low-cost backlight TVs (300-350 nits). Soon the only 400-nit LCD TVs will be high-end models, Kim predicts.

Getting edge-lit backlight TV brightness down to 250 nits narrows the cost gap between them and CCFL models from 2× to 1.5×, which is still a bit higher than aforementioned gap between CCFL and direct LED backlighting. But the goal here, Kim notes, isn't to offer another CCFL alternative — it's targeting the same entry segment as low-cost low-brightness direct LED backlight TVs. **— J.M.**

news cont.

Europe to unite research efforts in Silicon Europe cluster alliance

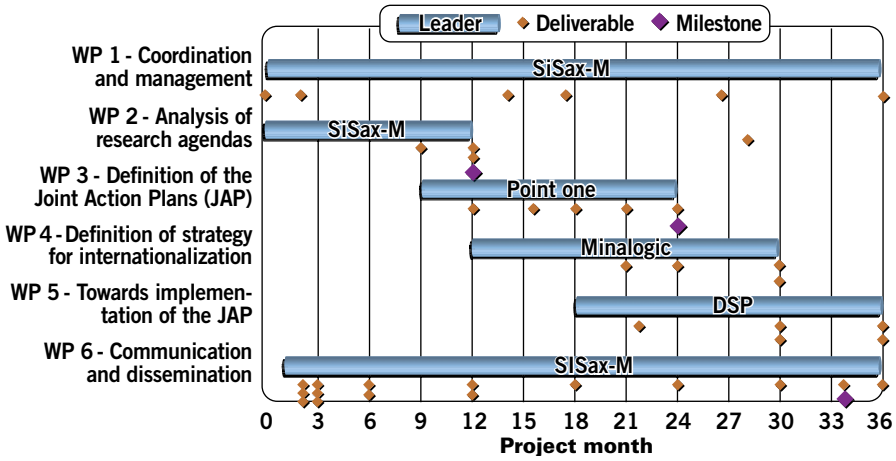
A cluster of partners from across Europe are forming a new cluster alliance to cooperate in research, development, and business and reassert Europe's position as a leading world center for energy-efficient micro-/nanoelectronics, and information/communications technology.

The new collective organization, dubbed "Silicon Europe," brings together Europe's four leading micro- and nanoelectronics regions: Silicon Saxony (Dresden/Germany), DSP Valley (Belgium), Minalogic (Grenoble/France), and Point One (Eindhoven/Netherlands). They claim to represent about 800 research institutes and companies, including global leaders Philips, NXP, Globalfoundries, Infineon, STMicroelectronics, Schneider Electric and Thales — though more than 75% of all their partners are small and medium-sized businesses.

"Global competition is tough and investments into European microelectronics are declining," acknowledged Jean Chabbal, chief representative and CEO at the French Cluster Minalogic (Grenoble/France). Only 10% of all worldwide investments into microelectronics (~€28 billion) went to Europe, less than a quarter of the funds (48%) that went to Asia. Since 2000, Europe's market share in the semiconductor industry has dwindles from 21% to 16%.

Still, the region employs 135,000 workers directly and another 105,000 in supplier sectors, the group notes. "Europe is home to a number of the world's best-known, and most active regions in the micro- and nanoelectronics industry and the semiconductor industry, more specifically," with regional clusters consolidating work from industry, research, and government partners, Chabbal stated. "The European micro- and nanoelectronics sector must take advantage of this leading position and further expand upon it. This is the only way for Europe to maintain its role as a world-renowned leader in technology research and development."

This is a three year effort, as shown in the diagram above. "We want to set up a joint action plan that is organized between the four clusters," said Frank Bösenberg, in charge of administration of Silicon Europe, speaking at a press conference in Dresden. "In the third year, we also want to start implementing this action plan. It's not only about creating paper, but doing some action. In addition to this, we want to involve if possible additional European players."



Details are not clear on precisely how the micro/nanoelectronics work will be shared and portioned out; the groups say they are currently analyzing each cluster's main research topics, identifying ways to synchronize activities and unearth and utilize previously unused synergies. In a published executive summary, the groups do identify three key objectives: promote the strategic importance of micro/nanoelectronics as a key enabling technology; secure European know-how across research institutes, design houses, and system integrators; and open up new markets

by improving innovation and technology transfer from research to commercialization and internationalization.

Plans also are underway to develop a strategic technology roadmap, with the hope that it can be a template for future European Commission programs, explained Thomas Reppe, general manager of the German Cluster Silicon Saxony. The group also has identified a goal of making "a substantial contribution" to the European Union's "Europe 2020" growth strategy, which aims to advance R&D as a basis for improving European society. "With their activities, the European Commission aims at a digital and resource-efficient development [because] both of these core goals micro- and nanoelectronics are a decisive factor," noted Eelco van der Eijk, contact person for the high-tech industry at the Dutch Ministry of Economic Affairs.

Obtaining political support is key in the Silicon Europe's mission. Peter Simkens, managing director at the Belgian Cluster DSP Valley, called for a pan-European micro/nanoelectronics summit in the style of Germany's IT summit: "We are appealing to all national governments to increase the synchronization of their economic and innovation policy with the European Commission and its guidelines," he said. "Silicon Europe stands for the common interest of the European microelectronics industry [...] The European economy needs to expand on its strengths now, if it wants to remain competitive in the global market for the long run."

Some of that government support is already coalescing. "The Europe-Cluster of the micro- and nanoelectronics sites is a very important signal for both German and European politics. Together and across national borders we have to ensure that this key technology still has a home in Europe in the future," stated Michael Kretschmer, vice-chairman of the CDU Parliamentary Group at the German Bundestag, member of the German Bundestag, and member of the Committee on Education, Research and Technology Assessment. While acknowledging that previous European clusters haven't worked together, "I appreciate the Silicon Europe initiative and wish for it to find numerous supporters and advocates also in the German Bundestag and the German government. The high-tech nation Germany can simply not forego these technologies that by enabling innovations in various industries create jobs and prosperity." **— P.S., J.M.**

news cont.

Laser spike anneal for photoresists outperforms hotplate bake

Researchers at Cornell University have developed a new laser-based method for ultra-fast anneal of thin photoresist films. The research, sponsored by Semiconductor Research Corporation (SRC), has shown that the new anneal outperforms a state-of-the-art hotplate bake for both 193nm and EUV lithography applications.

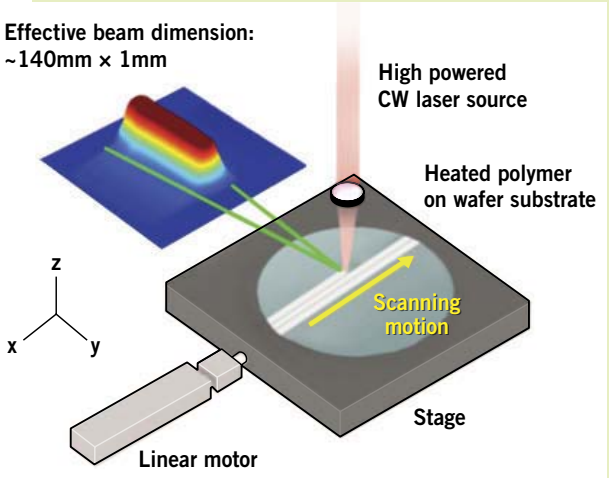


Figure 1: Using a continuous wave laser focused to a line and scanned over the surface, laser-spike annealing heats up a silicon substrate to its melting temperature in millisecond time frames.

Laser spike annealing is already in use for dopant activation in silicon (see J. Hebb et al., "Dual-beam laser spike annealing for advanced logic applications," http://bit.ly/VLRWCg). Now, Professors Michael Thompson and Christopher Ober from Cornell are perfecting the unique advantages of laser heating vs. current state-of-art hotplate bake used in chip patterning processes.

Historically, wafers required a lengthy bake at low temperatures to avoid degradation of the photoresist properties. Heating at much higher temperatures for millisecond times using continuous wave lasers not only activates the necessary photoresist chemical reactions at higher throughput, the researchers have determined, but also improves the pattern fidelity and line-edge roughness by limiting the chemical diffusion.

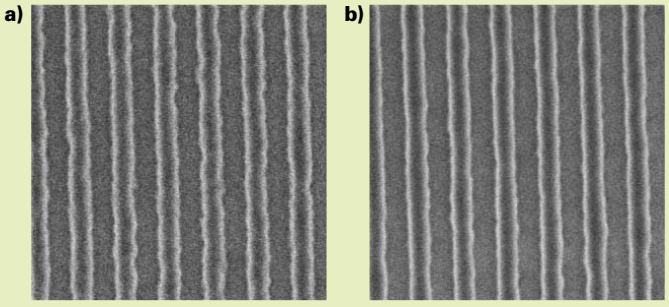


Figure 2: Patterns generated under 13.5nm EUV exposures using a) hot-plate PEB and b) laser PEB on a commercially available EUV resist. Critical dimensions were 52.1nm and 47.8nm for hot-plate and laser patterns respectively, with a target half pitch of 50nm. For these comparable SEM images, laser patterns show ~15% enhancement in sensitivity and ~15% reduction in linewidth roughness compared to hot-plate patterns. PEB temperatures and durations were 85°C for 60 sec (hot-plate) and 72W (~225°C) for 2ms (laser). (SEM image courtesy of GlobalFoundries)

"This new laser method can deliver a breakthrough in thermal processing for the industry," said Ober. "Until now, lithography progress has been held back by the traditional methods for heating the resist that were regarded by many as already optimized. The laser proves otherwise."

As one of the key benefits of the laser-based bake process, Cornell Ph.D. candidate Byungki Jung has shown significant improvements in line-edge roughness for both current 193nm immersion lithography as well as for next-generation 13nm EUV lithography.

Currently, photoresists are exposed and then baked on a hot plate at low temperatures (80-150°C) for approximately 1min to activate the resist chemistry and create a solubility differential between exposed and unexposed parts of the resist, which delineates the post-develop pattern. Prolonged heating, especially at higher temperatures, causes excessive chemical diffusion which degrades the image quality.

The novel application of laser spike heating — for a duration of milliseconds only — preserves the polymer integrity at much higher temperatures (up to 800°C) and provides a means to maximize resist sensitivity while minimizing pattern roughness, thereby facilitating enhanced scalability. **— P.S.**

CONNECT. COLLABORATE. CREATE.

CONNECT *with the right people.*
COLLABORATE *in the right environment.*
CREATE *alliances, partnerships and strategies for a stronger future.*

The ConFab®

Presented by: Solid State TECHNOLOGY
Insights for Electronics Manufacturing

COLLABORATE… It's impressive how the right environment can foster powerful collaboration.

"The ConFab is a great experience. The way that the conference is organized, the level of participation and the level of the participants are truly excellent. Going to a lot of these events, for me, the ConFab is the preeminent conference in the industry right now."

- IT Solutions Manager at Intel

Don't miss the 9th Annual ConFab, presented by Solid State Technology!

Coming to the Encore at the Wynn in Las Vegas from June 23 to 26, 2013.
Visit **www.theconfab.com** today to learn more and pre-register or to apply to attend as our VIP guest.

Owned & Produced by: PennWell®

www.theconfab.com

IMAPS 2012: A review

The 45th Symposium on Microelectronics (IMAPS 2012) was held September 9-13 in San Diego. Here's a quick review of some of the 3D and advanced packaging papers presented at the meeting.

Dr. Phil Garrou, Contributing Editor

Gu and co-workers at **Qualcomm** reported on a memory on logic 3DIC stack consisting of a two-chip-wide IO memory stack bonded to a 28nm logic chip. TSV are 6µm, wafers are thinned to 50µm, TSV connection is to M1 of the 7-layer copper/low-k interconnect stack. The memory stack has 1200 IO on 40µm pitch. The bottom memory die has TSV, the top die does not need them. Thinned die are shipped either on their carrier (the OSAT removes the carrier) or after removal from the carrier on a flex frame.

A negligible shift in electrical parameters is observed after optimizing TSV formation and determining the need for a 5µm keep-out zone (KOZ). No change in bump resistance is seen after 1000 hrs at 150°C and 1000 cycles of temp cycling.

Xilinx has been releasing information on its 2.5D FPGA module for the past two years. In the latest presentation, Banijamail and co-workers examine the reliability of their 2.5D Virtex-7 H580T, which consists of a transceiver chip and two FPGA slices. Interposer TSVs are 10-20µm and 50-100µm deep. FPGA chips are bumped on 30-60µm pitch using Cu pillar bump technology.

Different substrate sizes and designs, lid designs, lid materials, and underfills were examined to minimize warpage and maximize microbump and c4 bump reliability. Control of these variables resulted in packages that met JEDEC warpage spec and minimized BGA fatigue.

Packaging

With the recent announcements by **Xilinx**, **Altera** and others the commercial production of 2.5D products on "high density" interposers is entering the realm of commercial reality. While it is clear that fine featured interposers will come from foundries like TSMC, there have been questions, about "coarse featured" interposers in terms of who will make them and what applications they will be used in.

Shinko and **CEA Leti** now describe integration and electrical characterization of such a "coarse featured" 3D silicon interposer demonstrator for a SiP application. This demonstrator consists of (4) 10x10mm chips mounted on a 26x26mm Si interposer with 25µm microbumps on 50µm pitch and underfilled. TSV diameter are 10µm and interposer thickness is 100µm for an Aspect Ratio (AR) of 10. We are told that RDL on both sides of the interposer are done with a "semi additive process" although we are not given line width or pitch.

In their paper "Stacking Aspects in the View of Scaling," **imec** points out that when pitch goes below 40µm, "stacking accuracy is one of the main drivers to ensure yielding devices." It is shown that stacking can be made less sensitive to in plane misalignment by the obvious options of increasing the pad size or decreasing the solder bump size

In a second presentation, "Small pitch microbumping and experimental investigation for underfilling 3D stacks," they report on 3D stacking characterization when using pre-applied underfill (UF).

For 3D stacking, capillary underfilling has clear limits in terms of the gap between die and the bump pitch. This limits high density integration and therefore shifts focus onto pre-applied underfill where the material is dispensed on the landing die before stacking. Pre-applied UF does have concerns such as transparency for alignment marks and UF/filler entrapment between bumps.

imec's studies reveal that both NUF/NCP (define) and WUF (wafer underfill) have commercial products that result in >90% electrical yield after underfilling, although issues such as delamination of WUF films was observed.

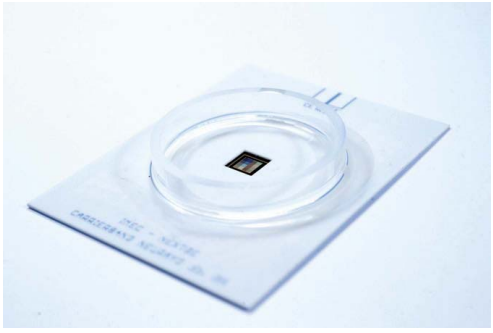
Semiconductors and healthcare converging

Semiconductor technology is increasingly being implemented in a variety of healthcare applications.

Pete Singer,
Editor-in-Chief

At the recent imec International Technology Forum Press Gathering in Leuven, Belgium, imec CEO Luc Van den hove outlined uses in blood cell sorting, mobile apps for personalized medicine (such as brain monitoring of EEG activity), and advanced bio research.

"The cost of healthcare is exploding," he said, noting that one in three people will develop diabetes in their lifetime. It is estimated that the cost of treating diabetes patients will exceed $500 billion 20 years from now (for U.S. and Europe).



CMOS chip with a matrix of micronails with various dimensions, packaged in a dish suitable for cell cultures.

Van den hove believes the healthcare system will soon see the kind of evolution of that the semiconductor industry has witnessed. "We have created this fabulous revolution in compute power. We went from mainframe to desktop type systems to a computer in our pocket that is more powerful than a mainframe computer we were using 20 years ago. We're convinced that we will see a similar revolution in the domain of medical diagnostics," said Van den hove. "We are clearly at a turning point and we will go from these very sophisticated clinical labs with big medical analysis tools to tools that will be implemented on a doctor's desk, eventually to tools we will be using in our homes which are add-ons to our smart phones, which will allow us to do part of the analysis at home. We are convinced that if you combine the capabilities of semiconductor technology with the know-how that is available in the medical profession, we can come up with solutions that are more sustainable."

One cornerstone of such a medical system will be early diagnostics. One example is the early detection of cancer cells in blood. "Typically today, when you have a primary tumor, it will spread out tumor cells that will circulate through the blood and will create secondary tumors that are usually the more fatal ones. If we can find a way to detect those circulating those tumor cells in the blood in an easy way, then we can come up with a way to detect cancer at an early stage," Van den hove said.

The challenge is huge: one has to have the ability to detect one bad tumor cell in 5 billion blood cells. This equate to a requirement to detect 20 million cells per second. "This is a real challenge, but the parallelism that can be realized with semiconductor technology is a tremendous opportunity. We can fabricate thousands of those parallel circuits on one device. This will allow us to create this kind of sensitivity," he said. "The system we are building here is a combination of very sophisticated microfluidics, electronics and very sophisticated on-chip imaging. We also require a lot of compute power because we have to analyze 20 million images per second. It will become possible to realize these kinds of detection systems."

The second pillar of a sustainable healthcare system, according to imec, is mobile diagnostics that will allow patients to be monitored in their homes and also better access to healthcare in places that are difficult to reach. A third pillar of such a sustainable healthcare system will be personalized therapy which could lead to the discover of cures of illnesses that are now uncurable.

MEMS

TRANSISTORS

IEDM preview: 20nm and below

PETE SINGER, *Editor-in-Chief*

As the industry works to perfect 28nm devices in volume manufacturing and early 20nm processes, attention is focusing on next-generation 14nm and below technologies.

There have been three primary drivers in the semiconductor industry for the last four decades: Area, power/performance and cost. The well-known push to cram more functionality onto a single chip through continued scaling -- or into a single package through 3D integration and other advanced packaging techniques -- has been well documented. Today, with the exception of Intel, the industry's leading edge devices in high volume manufacturing have critical dimensions of 28nm. Intel, racing ahead, introduced the 22nm IvyBridge chip in 2011 and has announced plans to have 14nm by the end of 2013. How long this kind of scaling can continue is the subject of some debate, with most recognizing the EUV lithography will be required at some point, most likely for the 10nm generation (Intel has said it doesn't need it for 14nm).

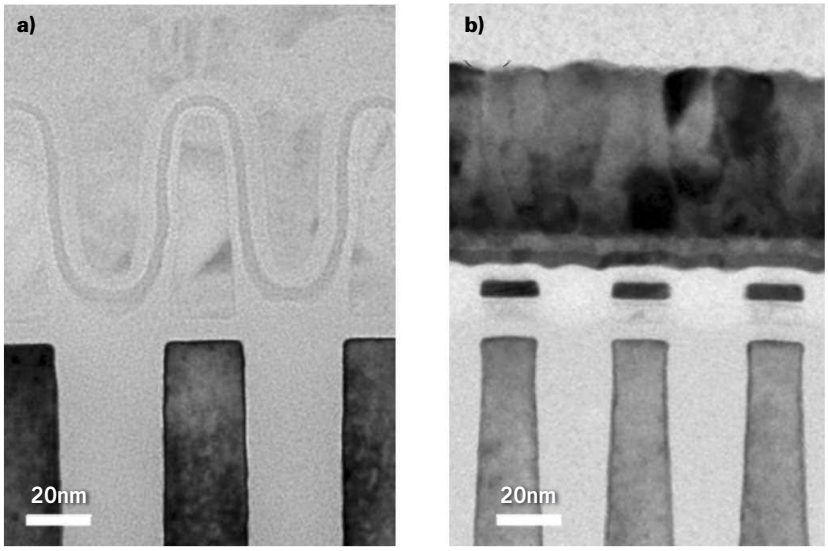


FIGURE 1. A wrap FG cell (left) and a planar FG cell (right). Source: Micron, Intel.

It's clear, though, that continued scaling is running out of steam, and that the industry most look for other means by which to say on the path defined by the proverbial "Moore's Law." Those advances are one of the primary focal points of the upcoming 58th annual IEEE International Electron Devices Meeting (IEDM), which will take place December 10-12, 2012 at the San Francisco Hilton Union Square. The conference will be preceded by a day of short courses on Sunday, Dec. 9 and by a program of 90-minute afternoon tutorial sessions on Saturday, Dec. 8.

As reported in last month's issue, highlights of the IEDM 2012 technical program, which comprises some 220 presentations, include Intel's unveiling of its industry-leading trigate manufacturing technology; a plethora of advances in memory technologies from numerous companies; IBM's demonstration of high-performance logic technology on flexible plastic

substrates; continuing advances in the scaling of transistors to ever smaller sizes, and breakthroughs in many other areas that will continue to move electronics technology forward.

Following, we've assembled a list of the "be sure not to miss" papers and sessions slated for IEDM 2012.

Invited papers

In the plenary session, imec's Luc Van den hove, will describe how ultimate transistor and memory technologies are the core of a sustainable society. He says that several key societal challenges in domains such as healthcare, energy, urbanization and mobility call for sustainable solutions that can be enabled by combining various technologies. These solutions will be backboned by wireless sensor systems, smart mobile devices and huge data centers and servers, the key constituents of a new information universe. They will require extreme computation and storage capabilities, bound by (ultra)low-power or heat dissipation constraints, depending on the application. This drives the need, he says, to keep on scaling transistor technologies by tuning the three technology knobs: power/performance, area and cost. To get to ultra-small dimensions, advanced patterning integration, new materials such as high-mobility Ge and III-V materials, and new device architectures such as fully depleted devices are being introduced. This comes along with an increasing need for process complexity reduction and variability control. Equally important are the continued R&D efforts in scaling memory technologies. NAND Flash, DRAM and SRAM memories are now approaching the point where new scaling constraints force exploration of new materials, cell architectures and even new memory concepts. This opens opportunities for resistance based memories such as resistive RAM, phase-change RAM or spin-torque transfer magneto resistive RAM.

In another invited paper, in the regular sessions, researchers from Micron and Intel will discuss scaling

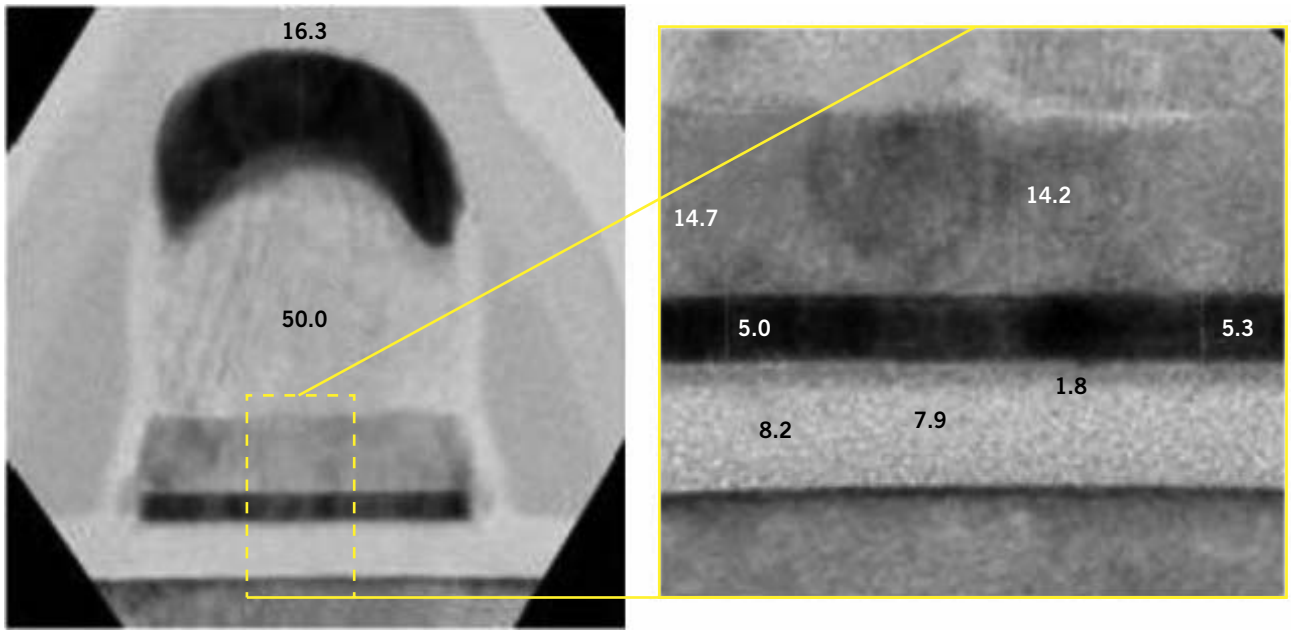


FIGURE 2. A TEM image of a polysilicon/TiN HFG cell perpendicular to the CG direction. Source: imec.

directions for 2D and 3D NAND Cells. They note that many 2D NAND scaling challenges are addressed by a planar floating gate (FG) cell, which has a smaller aspect ratio and less cell to cell interference. **Figure 1** compares a wrap FG cell (left) and a planar FG cell (right). The wrap cell is limited by a required aspect ratio of >10 for both the wordline and the bitline direction in a sub-20nm cell. The planar cell eliminates this limitation.

Of course, not all IEDM presentations are focused on leading-edge logic and memory. In the plenary session, John Rogers from the University of Illinois at Urbana-Champaign, will talk on bio-integrated electronics. He notes that biology is curved, soft and elastic, while silicon wafers are not. Semiconductor technologies that can bridge this gap in form and mechanics will create new opportunities in devices that require intimate integration with the human body. He plans to cover ideas for electronics, sensors and actuators that offer the performance of state-of-the-art, wafer-based systems but with the "mechanical properties of a rubber band." He'll explains the underlying materials science and mechanics of these approaches, and illustrate their use in bio-integrated, 'tissue-like' devices with unique diagnostic and therapeutic capabilities, when conformally laminated onto the heart, brain or skin.

In the third plenary talk, Joo-Tae Moon of Samsung Display will give a talk titled "State of the Art and Future Prospects in Display Technologies." There are two parts which satisfy this vision, he notes. One is the picture quality and the other is design of the display. From picture quality point of view, bigger screen size and higher pixel density are the main factors. The need for a bigger screen size requires expediting technologies with lower RC delay and higher transistor performance. Higher pixel density mandates a smaller unit pixel area and each unit pixel has the dead space for the transistor and metal line which is protected from the light by the black matrix. Clearly, the design factor is the one of the main driving forces for the changes from CRT era to flat panel display era, he says.

Notable papers

imec, in a paper titled "Ultra Thin Hybrid Floating Gate and High-k Dielectric as IGD Enabler of Highly Scaled Planar NAND Flash Technology," will describe -- for the first time -- a demonstration of ultra-thin hybrid floating gate (HFG) planar NVM cell performance and reliability. Results not only confirm the high potential of the HFG thickness scaling down to 4 nm with improved performance, but also show

excellent post cycling data retention and P/E cycling endurance. The optimized ultra-thin HFG planar cells show potential for manufacture and scalability for high density memory application. **Figure 2** is a TEM image of a polysilicon/TiN HFG cell. The stack consists of an ISSG tunnel oxide, a dual layer FG (PVD polysilicon + PVD TiN), a high-k IPD (ALD Al_2O_3) and an n-type polysilicon CG.

In a paper jointly authored by GLOBALFOUNDRIES and Samsung, titled "Stress Simulations for Optimal Mobility Group IV p- and n-MOS FinFETs for the 14 nm Node and Beyond," researchers provide calculations of stress enhanced mobilities for n- and p-FinFETs with both Si and Ge channels for the 14 nm node and beyond. Results indicate that both for

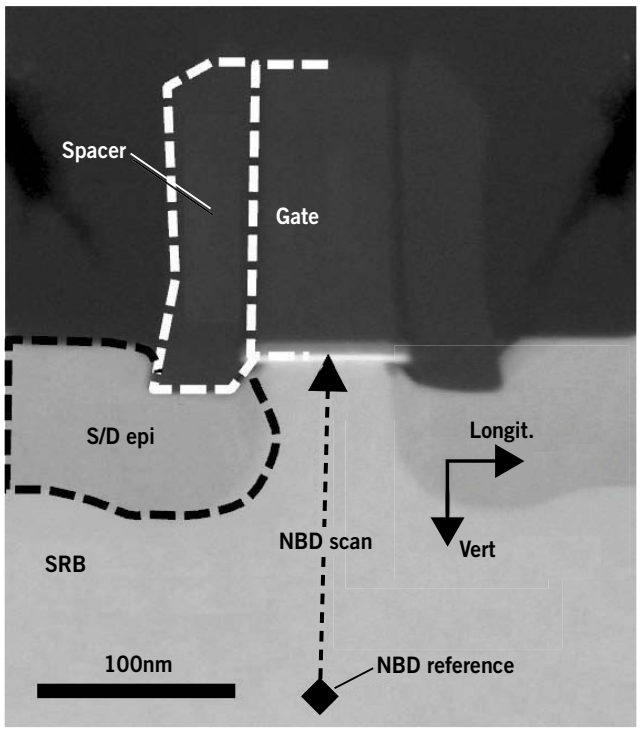


FIGURE 3. XTEM of a Ge-channel FET with SiGe source/drain. Source: GLOBALFOUNDRIES, Samsung.

nFETs and pFETs, Ge is "very interesting," provided the correct stressors are used to boost mobility. **Figure 3** is a XTEM of a Ge-channel FET with SiGe source/drain. They conclude that strained channels grown on a strain relaxed buffer is effective for 14nm nodes and scalable to future nodes. TCAD simulation trends are experimentally confirmed by nano-beam diffraction (NBD).

Luncheon presentation

Ajit Manocha, CEO, GLOBALFOUNDRIES, Inc. is sure to provide an interesting luncheon talk on Tuesday, December 11th, addressing some recent jabs from Intel's Mark Bohr. The title of Manocha's talk: "Is the Fabless/Foundry Model Dead? We Don't Think So. Long Live Foundry 2.0!"

Manocha says that industry experts and observers have predicted for a long time that the fabless model has some cracks in it, and may in fact be headed for extinction at some point. "We in the foundry industry dismissed such chatter as we continue to enjoy growth rates that outpace the overall semiconductor industry," he notes in his pre-conference abstract. "But it wasn't until an executive from – surprise – Intel – officially declared the fabless model is collapsing recently that many of us really got our feathers ruffled. We firmly believe that the rumors of its death are greatly exaggerated. Evidence would seem to support that it is actually the IDM model which is dead, survived only by a very small number of anomalies that have either the financial wherewithal or stubbornness to continue down this path."

The foundry-based fabless model is not going away, and moreover it is driving manufacturers and device designers closer together, says Manocha. But like all living organisms, especially those in electronics, we have to continue to evolve. There are warning signs, both technical and economic, emerging in the foundry business that warrant our attention, and in fact require a re-thinking of how best to apply our resources and energy. Recent talks of fabless companies investing in their own fabs, and of foundries developing 'single company fabs' underscore the sense of urgency. "Clearly, we must change - Call it Foundry 2.0," he says.

Unprecedented technical and business challenges have driven semiconductor manufacturing to this new fork in the road. On the one side is the option to 'go it alone', an option available to less than a handful of companies. The temptation here is to circle the wagons, dig deep into the bank and develop an optimized, but

Continued on page 29

LED MANUFACTURING

Automated data analysis improves yield of MOCVD epitaxial process in LED manufacturing

MIKE PLISINSKI, *Data Analysis & Review Business Unit, Rudolph Technologies Inc., Tewksbury, MA*

Integration of collection and analysis are vital

LED manufacturers invested heavily in production equipment in 2010–2011, driven primarily by demand for backlighting for flat panel displays in TVs and computers. Although this driver has moderated and there is currently an oversupply of metal organic chemical vapor deposition (MOCVD) capacity, LED manufacturers are anticipating a new round of demand for general lighting applications. Growth in this segment is highly dependent on achieving further reductions in cost per lumen, so while forecasts for additional MOCVD capacity have softened, there is strong pressure to improve the efficiency and yield of existing process equipment.

The MOCVD process is the most critical determinant of LED performance. With long process times and complex dynamics, it is inherently difficult to control, resulting in yield losses as high as 50%. Moreover, MOCVD processing occurs early in the process flow, and there is no opportunity to rework the wafers or eliminate low or non-performing die from further processing. Although LED manufacturers are making significant progress in reducing costs in subsequent process steps, particularly packaging, improving MOCVD processing remains the single largest opportunity to increase the yields and economic performance of the manufacturing process.

MOCVD equipment manufacturers have incorporated in situ measurement capabilities into their tools. Device manufacturers have also increased the amount of data they collect throughout the manufacturing process. However, much of the process knowledge that could be derived from this data remains hidden and its value unrealized.

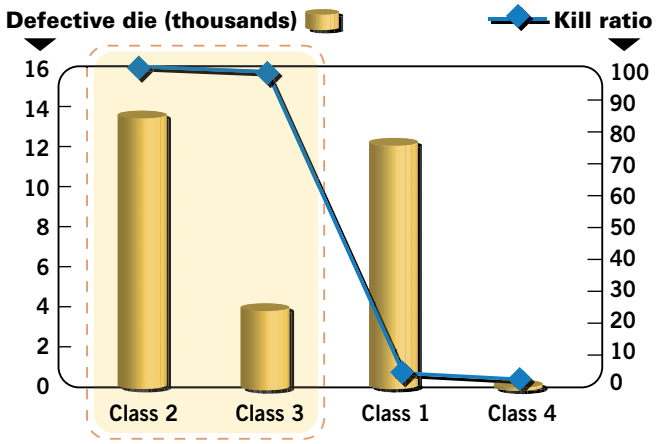


FIGURE 1. The power of ADC to identify defects with the greatest impact on yield.

Automated data analysis can reduce the difficulty of finding actionable information in the overwhelming volume of raw data, contributing significantly to improvements in process performance by shortening reaction times to process excursions and focusing engineering resources on solutions and innovation. Yield management systems can provide process insights to increase both yield and throughput. Automatic defect classification can help direct engineering resources to defects that are having the

MIKE PLISINSKI *(Mike.plisinski@rudolphtech.com) is VP and GM of the Data Analysis & Review Business Unit of Rudolph Technologies Inc. (www.rudolphtech.com).*

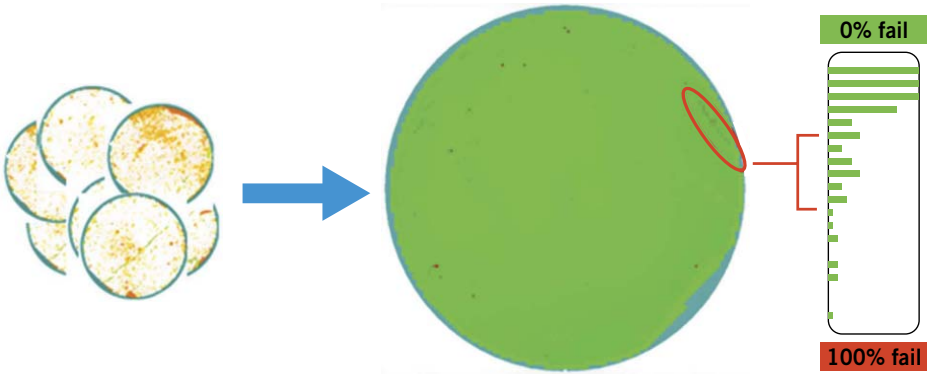


FIGURE 2. When detected, spatial patterns can often lead to rapid identification of the defect's root cause.

greatest impact on yields. Spatial pattern recognition can identify and eliminate wafer scale systemic defects. Automated fault detection and classification can sift through terabytes of sensor data to identify equipment parameters that impact yield and anticipate equipment failures. Advanced process control techniques can be applied to narrow process windows.

MOCVD process

Modern LEDs are multilayered structures of semiconducting materials in which the thickness and composition of the various layers determine the color and brightness of the emitted light and the energy efficiency of the device. The layers are deposited sequentially using MOCVD, where the crystalline structure of each new layer is epitaxially aligned with that of the underlying layer. In the MOCVD process, precursor gases flow over the heated substrate surface, where they interact and decompose to deposit the desired material layer. Gas composition and flow rates, substrate temperature, and many other parameters must be precisely controlled to ensure the quality of the device.

THE MOCVD process is time-consuming (6–12 hours) and largely determines the value of the final device, but the actual performance of the device cannot be measured until it has incurred the significant added costs of assembly and packaging. Yields of devices meeting the required performance specifications may be as low as 50%.

MOCVD equipment manufacturers have steadily improved the physics and technology of their tools. Innovative reactor designs have improved the uniformity of the deposition process across the substrate surface. Clustering of multiple chambers, engineered substrates, and higher growth rates have increased throughput. In situ metrology and diagnostics generate copious data on tool and process performance. The most cost-effective opportunity for improving the economic performance of the manufacturing process lies in the effective collection and analysis of available data to enhance process yields.

Yield management systems

Over decades of experience, manufacturers of integrated circuits (ICs) have developed sophisticated, automated yield management systems (YMSs). While there are many similarities among the processes used for IC and LED manufacturing, there are also significant differences. Although an LED is a simple device compared to an IC containing millions of transistors and many layers of interconnecting circuitry, analysis tools optimized for IC manufacturing do not natively meet the demands of the LED manufacturers. Challenges in data collection and analysis—such as the large number of devices per wafer, long MOCVD runs that generate vast amounts of valuable sensor data, or the need to "stack" hundreds of PLM maps and then correlate the stacked data with final test results on a device by device basis—can easily

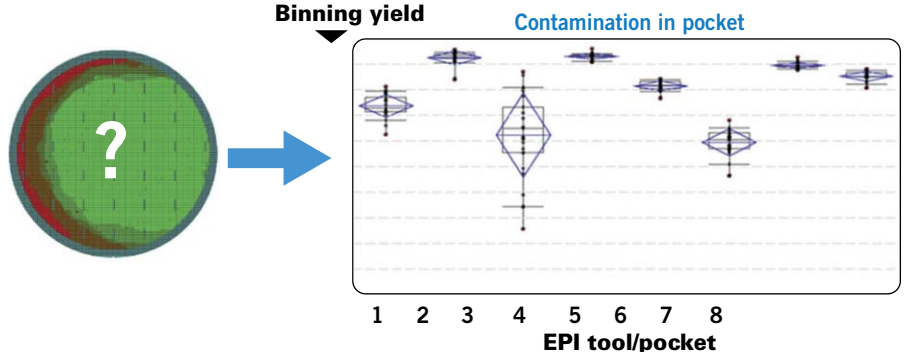


FIGURE 3. In MOCVD applications, FDC can provide traceability down to the individual reactor chamber and even the specific substrate pocket.

overwhelm systems not designed specifically for LED applications. Other barriers to effective LED yield management are more cultural than technical, such as the relative isolation of various process areas and the lack of consistent and comprehensive data collection and sharing throughout the process. It is not uncommon for the epitaxial process area to be both physically and digitally isolated, located separately with little or no network connectivity to the chip fab.

Yield management generates the greatest benefits when it operates on information gathered across the entire process, from incoming materials to final test, to identify causes of yield loss and opportunities for yield improvement. One of the most important benefits of automated yield management is its ability to eliminate much of the tedium involved in collecting and analyzing process data by generating automated reports that convert data into actionable information and allow process engineers to focus their efforts on innovations and solutions.

Automatic defect classification

Automatic defect classification (ADC) categorizes defects based on multiple characteristics, including size, shape, and color. The conventional approach to defect characterization relies on size alone, or some parameter, such as the amount of scattered light, that is presumed to be correlated to size. It further assumes that size correlates to kill ratio, i.e. the larger the defect, the more likely it is to result in a defective device. Neither of these assumptions is universally true. Figure 1 illustrates the power of ADC to identify defects with the greatest impact on yield. Defects in classes 2 and 3 have high kill ratios. Although class 2 defects are more common, both types of defect have a significant impact on yield. Defects in class 1, though numerous, are not usually deadly. Defects in class 4 are both uncommon and non-lethal. Clearly the most effective defect reduction strategy in this example will prioritize class 2 first, then class 3, ignoring classes 1 and 4.

Spatial pattern recognition

Spatial pattern recognition (SPR) looks for relationships among defect locations on the substrate surface. When detected, spatial patterns can often lead to rapid identification of the defect's root cause (Fig. 2). The green map is a composite of 589 individual defect maps. The scratch readily apparent in the composite map was invisible in the individual maps. Further analysis revealed that the scratch killed 14–28 die 35% of the time, representing over US$500,000 / year for this issue alone.

Automated fault detection and classification

Engineers are alerted of the occurrence and type of failure conditions using automated fault detection and classification (FDC), which monitors process equipment. In MOCVD applications, FDC can provide traceability down to the individual reactor chamber and even the specific substrate pocket (Fig. 3). Bin yield data (right) indicated low yield for die from substrates processed in pocket 6. Further analysis revealed a spatial pattern with the defective die located near the edge of the substrate on one side. Engineers traced the problem to contamination in pocket 6 that was missed by photoluminescence mapping and other in-line monitoring.

Predictive maintenance

Predictive maintenance improves productivity by avoiding the unscheduled downtime that occurs with run-to-fail approach to equipment maintenance, while also reducing unnecessary scheduled downtime that occurs with strictly periodic maintenance. Predictive maintenance requires a precise and reliable indicator of imminent failure. In Fig. 4, the pressure differential across a filter is used to predict the need to change out the filter. In Fig. 5, the frequency and amplitude of spikes from a mass flow controller

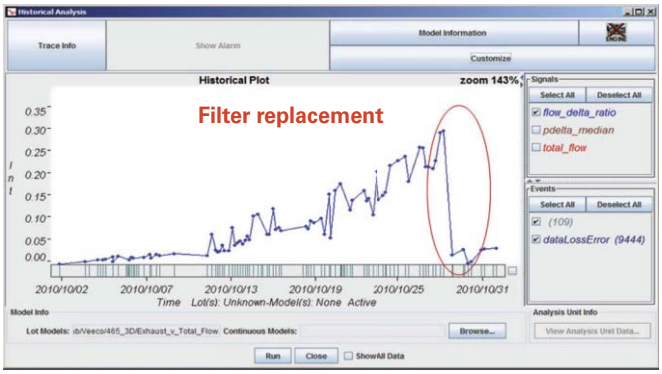


FIGURE 4. Increasing pressure differential across a filter can be used to predict the need for maintenance. After changing the filter, the pressure differential drops back to a baseline level.

indicate the need for maintenance. Automated FDC can monitor these and other equipment parameters to alert engineers of the need for maintenance.

A case study

Figure 6 illustrates the combination of various techniques to detect and resolve a problem in an LED production line. The problem was initially detected as a yield loss due to excessive variability in the wavelength of emitted light. Commonality analysis isolated the problem to a specific reactor. Spatial pattern recognition and pocket-level traceability showed the defects concentrated near the edge of the susceptor. Analysis of sensor data from the reactor indicated a radial non-uniformity in susceptor temperature. Possible causes to be investigated include miscalibration of the outer zone pyrometer and insufficient RF power to the outer zone.

With an integrated approach to data collection and analysis, manufacturers can quickly and easily detect and isolate a process issue, ultimately saving millions of dollars per year through increased yields and more efficient use of precious process engineering time.

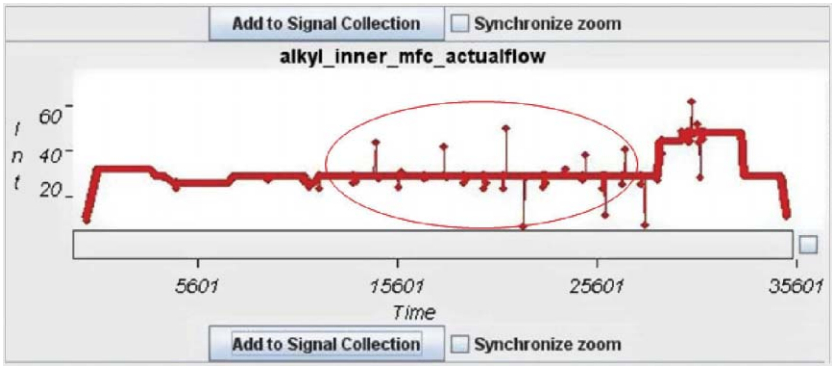


FIGURE 5. The frequency and amplitude of spikes from a mass flow controller may predict the need for maintenance.

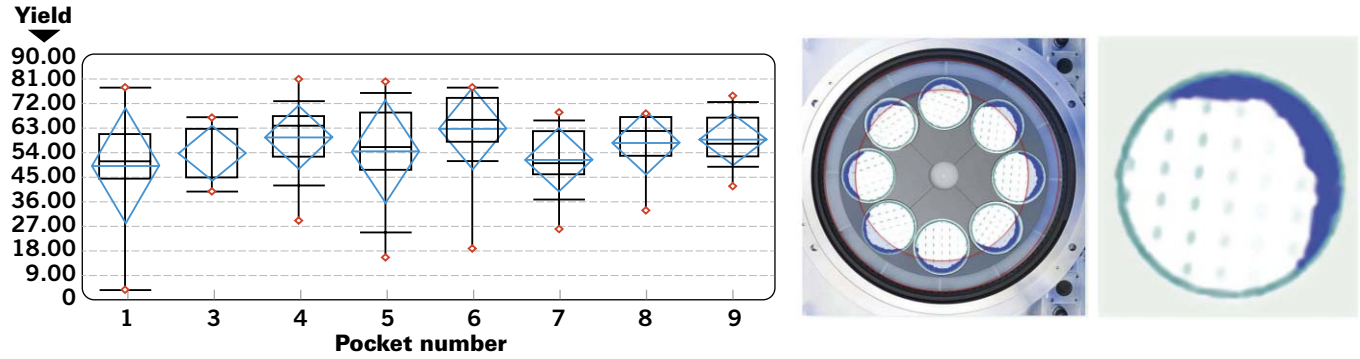


FIGURE 6. The combination of yield analysis, spatial pattern recognition, and fault detection classification identified non-uniform radial temperature in a specific reactor as the cause of yield loss.

Future opportunities

By narrowing process windows and increasing yields, advanced process control has the potential to significantly reduce the cost per unit area of MOCVD epitaxial processing, which is the most costly process in LED manufacturing. Improving bin yields also reduces assembly and packaging costs for defective die. Additional benefits may accrue from increases in die size that would be enabled by decreases in defect density. Finally, higher yields of more valuable devices can drive increases in average selling price and profitability.

Conclusion

Process control software is providing leading LED manufacturers with higher yields and better control of their manufacturing processes. By focusing yield management and process control strategies on the MOCVD process, these manufacturers are achieving significant reductions in the largest contributor to their manufacturing costs. Moreover, since process control systems scale inexpensively with changes in production capacity, technology, materials, or geographies, the investments of early adopters will be highly leveraged by future growth.

EMERGING TECH

New CMP process holds promise of lower costs, improved efficiencies

CHRISTOPHER ERIC BANNON, *Texas Instruments Inc., Richardson, TX*

Implementing third-generation low-abrasive copper slurry

There is a certain amount of inertia involved in making a decision to deploy a new manufacturing process. However, lowering the total cost of ownership and improving the overall efficiency often provide sufficient impetus to take the first step, even when the process is so integral to semiconductor fabrication as is the chemical-mechanical polishing (CMP) of wafers. Of course, following the correct steps to discover, evaluate, qualify, and deploy the optimum materials as well as the most effective process parameters and procedures are essential to successfully migrating to a new CMP process.

Reducing costs, improving processes

The market for third-generation copper slurries has matured to the point where the cost of such slurries has reached a new low. This gets the attention of semiconductor manufacturers, but selecting, qualifying, and deploying a new consumable material is only part of the challenge. Third-generation slurries are typically less abrasive and more selective in the materials they remove than previous formulations. As a result, switching slurries would also require an array of design experiments to discover how the CMP process would be affected by changing a critical component in the process. In addition, the control parameters for the equipment performing the process would have to be modified to achieve an optimum level of production with high yields.

Still, the benefits that evolve from migrating to a new slurry would be far reaching. Specifically, the manufacturer could expect a slurry with the following characteristics: low abrasion, high copper removal rate, highly selective to the oxide, and low dishing and erosion of the wafer. At the same time, the CMP process could have increased pad/puck life, head life and tool throughput, as well as a

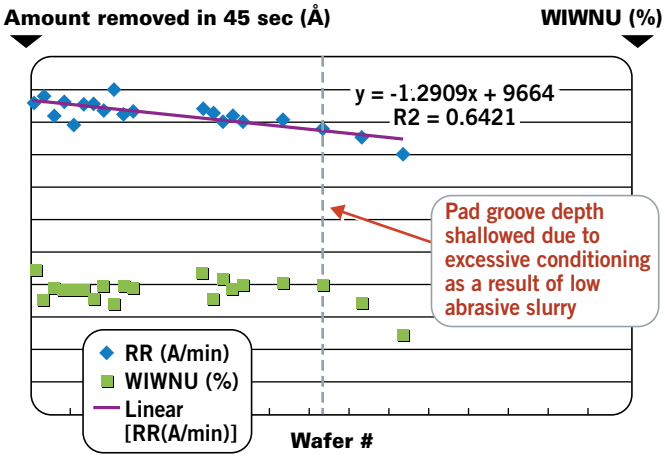


FIGURE 1. Results of removal rate tests on a third-generation slurry.

CHRISTOPHER ERIC BRANNON *(cbrannon@ti.com) is a member of technical staff at Texas Instruments (www.ti.com) and currently holds a position at TI's DMOS5 factory as a copper CMP manufacturing engineer.*

world-class mean-time-between-failures (MTBF) of approximately 48 hours.

Evaluating slurries

Integral to choosing a new copper slurry would be evaluating its compatibility with the manufacturer's existing machine tooling. A best case scenario would be to leverage existing pads, conditioning pucks, and heads. Moreover, for maximum throughput, wafers would need to be processed through the current processing equipment's onboard scrubber and dry station as quickly as possible.

Surveying commercial slurries on the basis of slurry/solid makeup and type, chemical composition, pH level, oxidizer (H_2O_2) costs, and compatibility with the current barrier slurry should reduce the number of appropriate candidates to be evaluated on an experimental basis. First, the performance properties of each material would be evaluated and second, experiments would be performed by varying process control parameters to determine the optimum slurry to deploy and how it should be deployed on the machine tooling.

The initial criteria for testing wafer performance and thereby judging each slurry should involve: removal rate, nominal removal profile, removal profile turnability in relation to certain sets of recipe alternatives, and defect rates. Following these types of tests, experiments with process controls and the candidate slurries should compare: carrier speed, table speed, down force exerted on the wafer, carrier positioning, carrier oscillation, and slurry flow. Candidate slurries advancing beyond this point could also be evaluated on the basis of patterned wafer tests to discover removal rate behaviors, the ability of each slurry to detect endpoints, and the over-polishing window. In addition, slurry recipe parameters could be manipulated to eliminate residual copper, especially at the wafer's edge, and to achieve uniform and reasonable dishing and erosion performance. Lastly, slurry vendors should be asked to perform and provide the results from lifetime experiments with consumables.

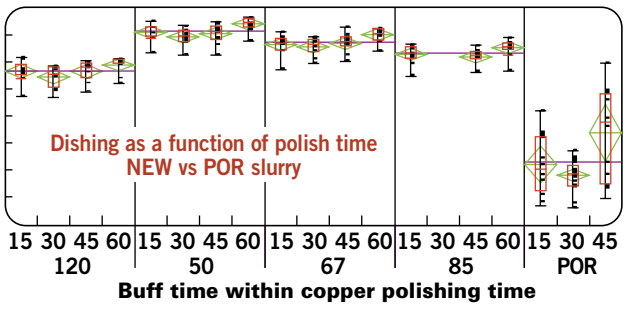


FIGURE 2. A third-generation slurry's polish time as a function of short-loop dishing.

Second- vs. third-generation slurries

Throughout this type of process, manufacturers will become aware of the differences in second- and third-generation slurries.

Second-generation slurries are high in abrasive solid content and have chemical additives to help stop the removal process as it reaches the tantalum nitride (TaN) layer. Overall, the results of such a slurry would be limited to a very mechanical process, one that would rely heavily on F.W. Preston's venerable equation that defined how quickly material would be removed from a surface as a result of mechanical polishing. Although experiments performed by TI have shown a second-generation slurry likely would be selective enough with regards to the materials removed, the tool's pad would probably degrade after approximately 400 wafers. This could cause increased dishing and erosion as a result of temperature spikes and reduced consumable performance.

> Once the benefits of a new slurry have been identified, the actual processes in the manufacturing line must be re-developed

In contrast, third-generation slurries are low in abrasives and have a different chemical composition than second-generation slurries. Third-generation slurries could be just as selective as second generation slurries, meaning they would also remove materials to the TaN layer, but they typically produce less dishing and erosion, and achieve higher copper removal rates at lower process parameters.

Experiments performed by Texas Instruments (TI)

with one third-generation slurry compared to a currently deployed first-generation slurry showed that there could be a problem with premature balding of the machine's pad (**Fig. 1**). The removal rate for the polishing process decreased as wafers were processed and as the grooves on the machine's pad became shallower due to excessive conditioning required because of the third-generation slurry's nonabrasive nature.

Further experimentation revealed that this could be overcome by reducing the conditioner's down-force and time. Since the third-generation slurry was low-abrasive, it would not wear down the conditioner diamonds, which caused the degrading of the cut rate of the pad. **Figure 2** shows the performance of a third-generation slurry with regard to the removal of dishing over several polishing times and compares this to the same results of a first-generation slurry. This clearly demonstrates the superior performance of the third-generation slurry.

Process development challenges

Once the benefits of a new slurry have been identified, the actual processes in the manufacturing line where the slurry will be deployed must be re-developed to take into account the new material. With a CMP process, these challenges often involve identifying and correcting any defects the new process may introduce. Issues such as photo-induced corrosion can usually be resolved quickly, while others like residual copper and micro-scratching, may require adjustments in the process.

Residual copper can have a devastating effect on yields, but polish and plate engineers can usually produce custom film depositions based on the requirements of the process. In addition, wafer-level inspections on every lot processed will also help. Micro-scratching is particularly problematic with first-generation slurries which incorporate fumed silica. These processes typically lack a final table conditioner and, as a result, the machine's soft pad will become embedded with slurry until it effectively becomes a fine-grain sandpaper. Nonabrasive, third-generation slurries which employ colloidal silica avoid this problem entirely.

Replacement costs

Even though experiments demonstrated the benefits of a third-generation slurry, these advantages must outweigh the cost of replacing a process that is currently in place. This involves benchmarking consumable costs and the wafer yield rate with a new CMP process versus the old CMP process. The benchmark results performed at TI were quite

Continued on page 31

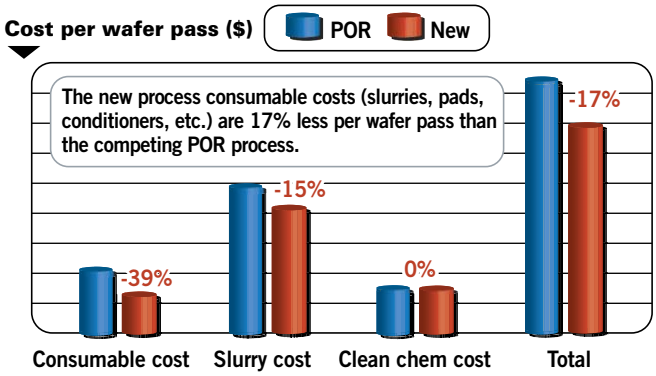


FIGURE 3. Consumables cost savings of third-generation slurry CMP process over first-generation slurry CMP process.

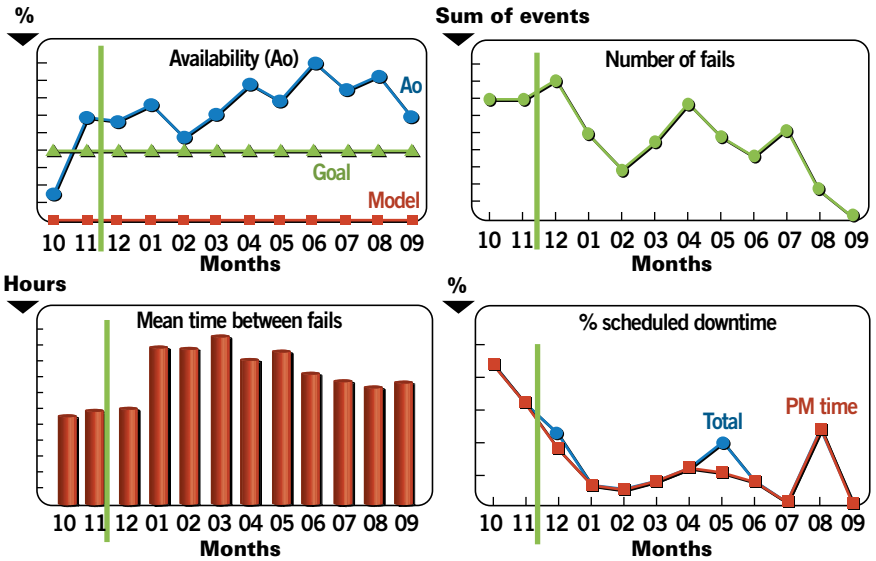


FIGURE 4. Sample copper tool availability with the new third-generation slurry process.

CONNECT.
COLLABORATE.
CREATE.

CONNECT *with the right people.*
COLLABORATE *in the right environment.*
CREATE *alliances, partnerships and strategies for a stronger future.*

The ConFab®

Presented by: Solid State TECHNOLOGY Insights for Electronics Manufacturing

CREATE… It's amazing what the right people in the right environment can accomplish together.

Alliances
Partnerships
Strategies for a Stronger Future

CONNECT, COLLABORATE, CREATE @ THE CONFAB

Don't miss the 9th Annual ConFab, presented by Solid State Technology!

Coming to the Encore at the Wynn in Las Vegas from June 23 to 26, 2013.
Visit **www.theconfab.com** today to learn more and pre-register or to apply to attend as our VIP guest.

Owned & Produced by: PennWell®

www.theconfab.com

FORECAST

The scare of overcapacity

CHRISTIAN GREGOR DIESELDORFF, *SEMI Industry Research & Statistics, San Jose, CA*

How changes in capex affect fab capacity

Reports have surfaced recently that indicate companies including TSMC, Samsung, and Intel may change their capital expenditure plans for 2013. A number of market research firms have revised their economic scenarios and forecasts, including updates for both semiconductor industry revenues and fab spending.

For example, TSMC may increase its 2013 capex by about US$ 2 billion — to a robust $10 billion. Another media report in September indicated that Samsung may reduce 2013 spending, perhaps even significantly. Historically, Samsung cut capex in 2002 (by -30%), 2008 (-22%), and 2009 (-44%) — all years of economic depression. But can Samsung maintain its market share with a -30% or even -50% cut in capex?

Other media reports speculate that Intel may cut 2013 capex by about -10%. Intel's equipment spending for 2012 was actually a bit lower than the year before. If Intel does cut its 2013 capex, SEMI's data suggest that front-end equipment spending could be affected only marginally.

The question remains: How will changes in capex affect capacity? An increase in installed capacity may lead to oversupply, which will then drive down average selling prices and subsequently revenue.

Capex affects capacity

If significant changes in capex occur, installed capacity is likely to be affected. Since the last economic downturn in 2009, the industry has seen a change in paradigm. The average yearly growth rate from 2003 to 2007 (before the downturn) was 16%. From 2010 to 2015 (after the worst of the downturn), it is expected to range from 6% to 7%. Before the downturn, most

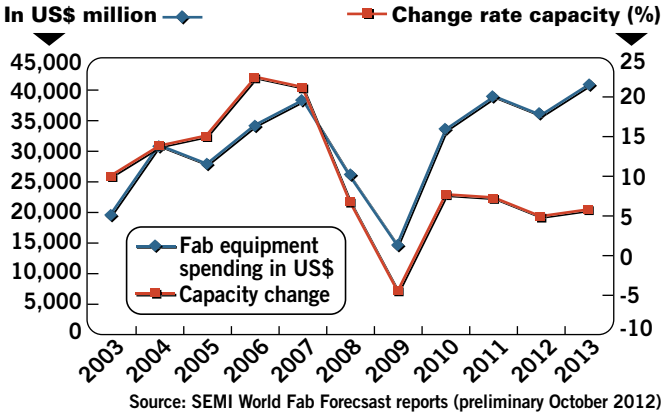


FIGURE 1. Fab equipment spending vs. change of installed capacity.

fab spending went into new installed capacity; however, more money is now being spent to upgrade existing facilities (**Fig. 1**).

Except for foundries and system LSI (SLSI), almost all segments of the industry have seen a decrease in the rate of new capacity additions in 2012 (**Fig. 2**). The foundry industry segment has greater installed capacity — both in absolute terms and in the rate of growth in comparison to other segments. Given industry consolidation and as more IDMs change to a fab-lite or fabless business model, foundries become even more important to the supply chain that provides manufacturing technology. The dedicated foundry sector has added capacity at greater than a 10% rate year-over-year (YoY) since 2010, and this trend will continue going into 2013.

Most current spending for the MPU sector goes into existing fabs. While no new capacity is planned for 2012, a couple of new fabs will begin ramping in 2013, pushing installed capacity up by 4%.

Cutbacks were made in NAND flash memory production in 2012 — by companies including Sandisk, Toshiba, Samsung, and Micron — in order to improve average selling prices. Anticipating higher demand,

CHRISTIAN GREGOR DIESELDORFF *(cdieseldorff@semi.org) is senior industry analyst at SEMI Industry Research & Statistics (www.semi.org), San Jose, CA.*

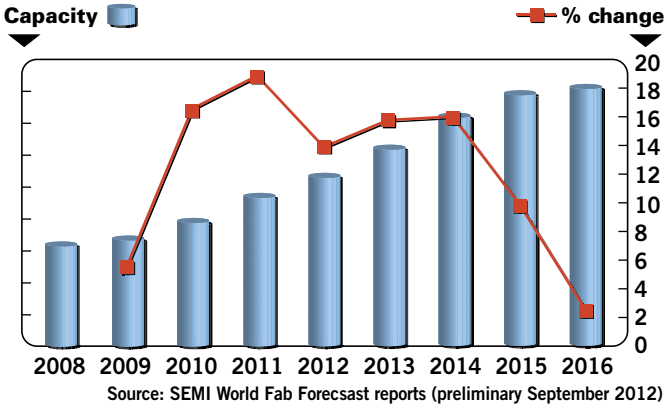


FIGURE 2. Except for foundries and system LSI (SLSI), almost all segments of the industry have seen a decrease in the rate of new capacity additions in 2012.

companies will likely need to increase flash capacity in 2013. While flash growth will increase only 4% YoY in 2012, it's expected to double in 2013 to 8%.

More consolidation is predicted in the DRAM market. Nanya is expected to exit the PC DRAM market, and Micron may acquire Elpida by 1H13. Ultimately, only three major DRAM makers will remain; no noticeable increase of installed capacity is expected in 2012 and into 2013.

Samsung's heavy investments in system LSI will singlehandedly spike overall SLSI capacity. One example is the recently announced $4 billion conversion of its Austin, TX, fab from flash to 28nm SoC logic devices. Installed capacity for system LSI shows healthy growth since 2010 — about 20% every year, with an expected repeat performance in 2013.

Samsung has begun an aggressive conversion of up to four existing memory lines to system LSI. A transition from flash to system LSI is not easy to manage, so a drop in memory capacity is expected. The company is expected to compensate for this memory capacity by continuing to ramp its Line 16 fab and constructing a new fab in Xian, China, with a massive investment of $7 billion; construction started in mid-September 2012. SEMI's World Fab Forecast gives more detail about the ramping phases of this leading-edge flash fab with huge potential capacity.

Needed: More 300mm fabs?

Merely shrinking die may not compensate for increasing demand for chips, such as for mobile and automotive applications. Volume production for the first 450mm fabs may not occur until 2018; it may take even longer until the cost-benefit ratio for 450mm volume fabs makes it an attractive option for all potential chipmakers. While 450mm production catches up to demand, the industry will still need additional 300mm fabs, especially for system LSI and flash. Of the 300mm NAND flash fabs currently in construction, ramping, or still planned, all are expected to reach full capacity by 2016 (**Fig. 3**).

The industry has a changed paradigm in that more fab equipment spending is allocated to upgrade existing capacity rather than adding new capacity. The industry reacts quickly to changes in average selling prices by reducing capacity outputs and slowing down expansion. In the five years before the economic downturn, capacity growth rates were in the double-digits. However, since the downturn, growth YoY has been more moderate, in the low single-digits.

The assumptions in any forecast are related to macroeconomic and political factors, like the Eurozone debt crisis, China's economy, the U.S. fiscal situation,

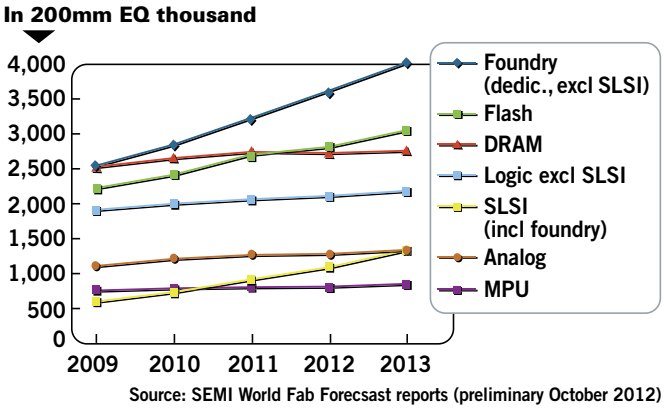
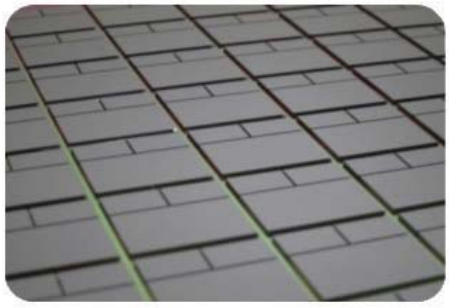


FIGURE 3. Installed capacity of 300mm volume flash fabs. Actual data available in World Fab Forecast report.

turmoil in the Middle East, and the U.S. election. At this point, worldwide GDP for 2013 is expected to be higher than in 2012, while semiconductor revenue is expected to be heading for the upper single-digits in 2013. While some data suggests that 2013 front-end fab equipment growth could be as high as 17%, a range of 12% ($40.3 billion) to 14% ($41.1 billion) is more likely, in light of recent changes in the marketplace.

PACKAGING

CoWoS process cuts power, boosts performance, shrinks footprint



JERRY TZOU, *TSMC, Hsinchu, Taiwan*

Converging the IC package and system board into one device package

A new integrated process technology, CoWoS (chip-on-wafer-on-substrate) by TSMC, uses a silicon wafer with through-silicon vias (TSVs) as a carrier to integrate multiple chips in a single device to reduce power, improve system performance, and reduce form factor. The process attaches silicon chips to the TSV'ed wafer through a CoW bonding process and then attaches the subsystem to the substrate to form the final component (Fig. 1).

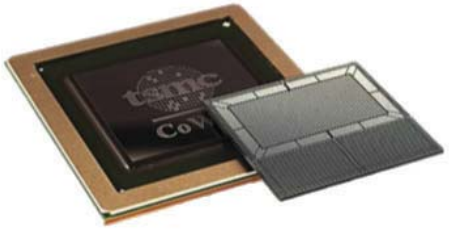


FIGURE 1. CoWoS die and finished package.

Shortens distance

This architecture enables higher-density interconnects and decreases global interconnect length and associated RC loading, resulting in enhanced performance, reduced power dissipation, and smaller form factor. As high performance applications need greater bandwidth between advanced processors and memory, and become I/O and bandwidth limited, CoWoS integration can effectively address the need by shortening the distance between them, providing the added benefit of reducing power consumption. In addition, convergence of the IC package and system board into a single device package minimizes the number of packages on printed circuit boards (Fig. 2).

CoWoS also allows designers to partition large die into a few smaller ones or partition subsystems by packaging multiple chips manufactured on different process technologies in one device. For example, a designer may choose an advanced technology for critical parts such as CPUs and use mainstream technology alongside it to optimize cost.

Shipments begun

TSMC has successfully qualified CoWoS technology using its first test vehicles and has started shipping risk production CoWoS units to customers. TSMC will build an infrastructure that encompasses DRAM manufacturers, EDA vendors and IP suppliers to facilitate CoWoS access.

TSMC uses DRAM with its CoWoS technology to produce integrated chips featuring lower power consumption, smaller form factor, and higher system bandwidth. These devices will prove ideal for networking equipment, high-performance computing (HPC) applications, smartphones, tablets and Ultrabooks.

TSMC, along with its EDA and IP infrastructure

JERRY TZOU *is deputy director of the backend business division of TSMC, Hsinchu, Taiwan.*

partners, has created multiple CoWoS design solutions through test chip and reference flow collaboration over the past year. Cadence has provided implementation for bump assignment, redistribution layer and interposer routing. CoWoS implementations also use Cadence Wide-I/O Controller IP to enable chip-to-chip connections that increase bandwidth between DRAM and logic.

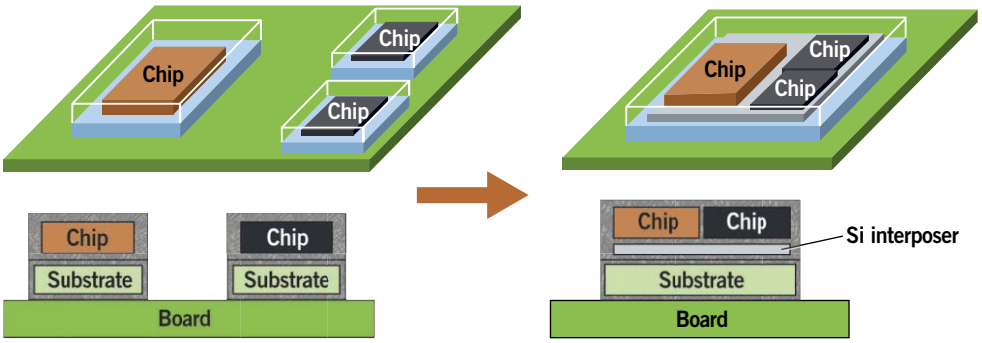


FIGURE 2. Converging the IC package and system board into a single device package minimizes the number of packages on printed circuit boards.

EDA partners

Several other EDA companies are involved in these efforts. Mentor has supplied multi-die physical verification of DRC, LVS, and extraction. Apache/Ansys can be used for IR-drop and electro migration power integrity analysis, and Sigrity can be employed for substrate extraction.

These tools, along with others in development or evaluation, will be included in TSMC's recently introduced Reference Flow for 3D design. TSMC's integrated CoWoS process provides turnkey, end-to-end manufacturing that includes the front-end process as well as backend assembly and test.

Continued from page 17

relatively closed, solution that will hopefully work for most every need. Manocha said a second option, ironically, is a move toward a more IDM-like model. Strategic collaboration that creates a 'virtual IDM-like interface' to chip design companies will help further close the gap between process teams at the manufacturing companies and design teams at the fabless companies. "With daunting technical challenges like 3D stacking, 450mm fabs, new transistor architectures, multi-patterning, and the long-term viability of extreme ultraviolet (EUV) lithography, collaboration – early, often and deep – is really the only practical approach given the cost and complexities involved," he said.

Evening panel

One of the two evening panels on Tuesday at 8pm is titled "The Mighty Little Transistor: FinFETs to the *Fin*ish or Another Radical Shift?" The moderator will be Suresh Venkatesan of GLOBALFOUNDRIES. He notes that the 22nm node spelled the dawn of the fullly-depleted device architecture – with the implementation of FinFETs as the workhorse of the technology. However – projecting out to the 10nm node and beyond – the scalability of the FinFET architecture, the materials systems used to create it, and the fundamental electrostatics and parasitic components associated with the transistor once again loom large as significant challenges that need to be overcome.

Please send new products to peters@pennwell.com

New Products

Gas sampling system

SEMI-GAS Systems, a division of Applied Energy Systems Inc., now offers an automatic gas sampling system that eliminates operator touch time while certifying cylinders of blended gas mixtures. The Samplex, a gas sampling system from the Xturion product line, can sample any gases that can be detected using a Fourier transform infrared (FTIR) analyzer. The system is useful for EPA protocol analysis and for gas suppliers and gas companies that make EPA-approved blended mixtures. It enables more efficient sampling and certification of cylinders, ensuring that certain EPA specifications and requirements, like the EPA Traceability Protocol for Assay and Certification of Compressed Gas Calibration Standards, are being met. Samplex confirms the accuracy of constituent gases within a gas mixture, enables batch analysis, and can display up to six samples. Samplex features a workstation PC with LabView interface and a color touch screen controller. **Applied Energy Systems Inc., SEMI-GAS Systems,** Malvern, PA, www.semi-gas.com.

Defect inspection system

Nanotronics Imaging has announced new capabilities to its nSPEC semiconductor inspection system. nSPEC now detects and categorizes defects on semiconductor wafers after photolithographic patterning and other chip processing steps. nSPEC has been proven effective for inspection of blank wafers (substrates and epitaxial) across a full range of compound semiconductor materials, e.g., SiC, GaN, GaAs, and InP. The patterned wafer inspection feature gives nSPEC the capability to track wafer quality through the whole chip manufacturing process from bare substrate all the way to fully processed devices. Software has been developed in collaboration with Microsemi Corp. of Aliso Viejo, CA, and supported by funding from the US Air Force. Commercial release of the patterned wafer inspection software for new and existing nSPEC systems is expected in 1Q13; it is currently available for evaluation as a beta version. **Nanotronics Imaging**, Cuyahoga Falls, OH, www.nanotronicsimaging.com.

Ultrasonic spray system

Spraying Systems Co. has introduced the AccuJet Ultrasonic Spray System, which delivers a precise, extremely fine spray that is good for micron coating, high-precision coating, vaporization, spray drying, and humidification.

The Ultrasonic spray nozzle will operate at flow rates that range from 0.5 to 10 cc/min. The high vibration frequency generates fine droplets. Air assist shapes spray pattern and allows adjustment of droplet velocity.

Shaping air pressure as low as 0.1psi will affect spray velocity. Spray velocity adjustments can be made to optimize coverage with minimal overspray, resulting in savings on materials and maintenance costs. The spray controller allows for power adjustment to the nozzle and maintains the nozzle at resonant frequency. Applications for ultrasonic spray include: coating of medical devices, (stents, catheters), solar panels and semiconductors; spray drying; humidification (glove boxes); and applications in nanotechnology. **Spraying Systems Co.**, Wheaton, IL, www.accujet.com.

Continued from page 24

positive in favor of a third-generation slurry. The cost of consumables, such as pads, conditioners, the slurry itself and other materials, revealed a 17 percent cost savings with the new process over the old (**Fig. 3**.) The useful life of pads and conditioner was 50 percent greater with the third-generation process because of low abrasiveness and lower conditioning down-force. Moreover, the life cycle of equipment heads nearly doubled, increasing by 98 percent. This was caused by the lower process parameters required by the third-generation slurry, which reduced wear on the retaining ring. Longer head life cycles reduced the number of failures resulting from loading and unloading heads, lengthening the tool's MTBF to a range of 30 to 40 hours. In addition, wafer yield comparisons showed that the new process achieved slightly better yields than the old process.

Figure 4 benchmarks the availability performance of a new third-generation slurry CMP process versus an older first-generation process. The point of switch-over from the old process to the new is indicated by a vertical green line in each of the four plots. In every case, the performance of the new process significantly surpassed that of the old.

Conclusion

Qualifying, developing, and deploying a new copper polishing process with a third-generation low-abrasive copper slurry presents certain challenges, but the opportunity to lower costs and achieve an equivalent or better wafer yield outweighs the challenges. In the end, leveraging the manufacturer's engineering, maintenance, and operational talent ,as well as that of supply chain vendors will be essential for a successful transition to a new process.

Solid State TECHNOLOGY

EXECUTIVE OFFICES
PennWell, 98 Spit Brook Rd, Nashua, NH 03062-5737
Tel: 603/891-0123

ADVERTISING
Marcella Hanson—Ad Traffic Manager
Justine Beauregard—Marketing Communications Manager

ADVERTISING SALES OFFICES

Group Publisher
Susan Smith
98 Spit Brook Rd, Nashua, NH 03062-5737;
Tel: 603/891-9447;
Fax: 603/891-9328;
e-mail: susans@pennwell.com

Sales Manager
Kerry Hoffman
98 Spit Brook Rd. Nashua, NH 03062-5737
Tel: 603/891-9118;
Fax: 603/891-9328;
e-mail: kerryh@pennwell.com

The ConFab
Sabrina Straub
98 Spit Brook Rd. Nashua, NH 03062-5737
Tel: 603/891-9118;
Fax: 603/891-9328;
e-mail: sabrinas@pennwell.com

Europe
Holger Gerisch
Hauptstrasse 16, D-82402 Seeshaupt, Germany;
Tel: 49/(0)8856-802022;
Fax: 493(0)8856-8020231;
e-mail: holgerg@pennwell.com

United Kingdom & Scandinavia
Kerry Hoffman
98 Spit Brook Rd. Nashua, NH 03062-5737
Tel: 603/891-9118;
Fax: 603/891-9328;
e-mail: kerryh@pennwell.com

Israel
Dan Aronovic
Allstar Media Inc., 3/1 Hatavas St., Kadima, 60920, Israel
Tel / Fax: 972/9-899-5813
e-mail: aronovic@actcom.co.il

Japan
Masaki Mori
ICS Convention Design, Inc., Chiyoda Bldg., Sarugaku-cho 1-5-18, Chiyoda-ku, Tokyo 101-8449, Japan
Tel: 3-3219-3641;
Fax: 3-3219-3628;
e-mail: mori-masaki@ics-inc.co.jp

Taiwan
Diana Wei
Arco InfoComm, 4F-1, #5 Sec. 1 Pa-Te Rd. Taipei, Taiwan R.O.C. 100
Tel: 866/2-2396-5128 Ext. 270
e-mail: diana@arco.com.tw

China, Hong Kong
Adonis Mak
ACT International, Unit B, 13/F, Por Yen Building, 478 Castle Peak Road, Cheung Sha Wan, Kowloon, Hong Kong
Tel: 852/2-838-6298;
Fax: 852/2-838-2766;
e-mail: adonism@actintl.com.hk

List Rental
Kelli Berry
1421 South Sheridan Rd., Tulsa, OK 74112;
Tel: 918/831-9782; Fax: 918/831-9758;
e-mail: kellib@pennwell.com

November 2012, Volume 55, Number 9 • ***Solid State Technology*** ©2012 (ISSN 0038-111X) Periodicals postage paid at Tulsa, OK 74112, & additional mailing offices. Published 9x per year (Jan, Mar, Apr, May, Jun, Jul, Sep, Oct and Nov) by PennWell Corp., 1421 S. Sheridan Rd., Tulsa, OK 74112. **Subscriptions:** Domestic: one year: $258.00, two years: $413.00; one year Canada/Mexico: $360.00, two years: $573.00; one-year international airmail: $434.00, two years: $691.00; Single copy price: $15.00 in the US, and $20.00 elsewhere. Digital distribution: $130.00. You will continue to receive your subscription free of charge. This fee is only for air mail delivery. Address correspondence regarding subscriptions (including change of address) to: *Solid State Technology*,, PO Box 3425, Northbrook, IL 60065-9595, sst@omeda.com, ph 847-559-7500 (8 am – 5 pm, CST). PRINTED IN THE USA. GST NO. 126813153. Publication Mail Agreement No. 40052420. **POSTMASTER:** Send address changes to *Solid State Technology*, PO Box 3425, Northbrook, IL 60065-9595. Return Undeliverable Canadian Addresses to: P.O. Box 122, Niagara Falls, ON L2E 6S4.

ad index

industryforum

New level of repeatability required for 3D NAND

Historically, manufacturers have increased memory density by packing more cells together in a single plane. As traditional dimensional shrinks become increasingly difficult, the industry is transitioning from planar to 3D NAND architectures by stacking memory cells onto the same silicon substrate. This approach is made cost efficient by fabricating numerous memory levels simultaneously and using standard semiconductor processes and materials.

In 3D NAND, critical dimensions for deposition and etch processes can be roughly five times larger than those used in planar devices. While this relaxes scaling challenges due to shrinking, it would be misleading to suggest that fabrication is trivial. Making trillions of identical memory cells requires outstanding repeatability on every wafer, wafer to wafer, chamber to chamber, and fab to fab. In addition, 3D NAND stacking introduces an entirely new dimension of process repeatability control—level to level. This new requirement is especially challenging because errors are magnified by the sheer number of levels, and chipmakers are driving more memory levels to increase product value. As a result, the precision requirements for many 3D NAND processes can far exceed those of their planar counterparts.

JEFF MARKS, *global product group chief technology officer, Lam Research Corp.*

The magnification of error effect in 3D NAND stacking is evident in several critical steps, and here we consider a vertical channel architecture. In the case of deposition, the gate stack of a 30-level memory device requires depositing 60 repeatable thin film layers at a time, compared with only one to two layers for planar devices. For the plasma-enhanced CVD process, this means that any minor imperfections (e.g., defects or surface roughness) in the first few layers can propagate into subsequent layers, compounding with each added film. Dielectric film stress is also additive and can result in wafer bowing. Film distortion is a concern because every other layer of the 3D NAND stack will become an electrically active part of the device. Furthermore, undulations in the film stack can interfere with pattern transfer, which then makes subsequent process steps more difficult. One solution approach is to optimize the properties of the alternating film layers to neutralize distortion.

> Equipment suppliers need to optimize performance from individual processes and leverage coupled effects between process steps.

Looking at an etch example, the hole etch is critical because it forms the cell channel for all of the levels by "punching" a hole through the stack of alternating film layers in a single pass. Although the aspect ratio for an individual level may only be 1:1, the net aspect ratio of the hole can reach 40:1 in a 30-level device. This is a difficult etch because a nearly perfectly straight profile is required in order to keep the channel size the same at each level. Even a 0.5-degree deviation from vertical can cause the channel dimension at the top level to be ~20% larger than at the bottom. One strategy to minimize this variability is to modify the hardmask properties to enhance etch precision.

Magnification of error concerns also exist for the "stair" etch, which forms the landing pads for each level's contact. This process requires multiple mask trims in a single pass to create features that look like steps of all the same size. Any systematic error in step size is magnified by the number of levels in each pass, shifting the contact placement with each successive step. Considering a 500nm step, only a 5% incremental error would cause the contacts to completely miss the pad after eight levels. The challenge for this process is to etch at high throughput without losing level-to-level precision.

As described, manufacturing 3D NAND devices requires a new level of repeatability driven by a unique compounding effect. Equipment suppliers will need to continue working closely with customers to deliver the precision needed—including optimizing performance from individual processes and leveraging coupled effects between process steps.

Previous Page | Contents | Zoom in | Zoom out | Refer a Friend | Search Issue | Next Page

MAGAZINE

WEBSITE

SIX E-NEWSLETTERS

EVENT

Solid State TECHNOLOGY®

Insights for Electronics Manufacturing

Semiconductors | Packaging | Displays | MEMS | LEDs

Solid State Technology, the leading independent media resource covering semiconductor manufacturing and packaging technology, equipment and materials for more than 50 years, also provides in-depth coverage of MEMS, displays and LED manufacturing topics.

Request a FREE subscription to our magazine and email newsletters, visit our comprehensive website and attend our annual executive conference, The ConFab, to see for yourself why manufacturing decision makers rely on Solid State Technology.

SUBSCRIBE

Scan the QR code on the right to subscribe to Solid State Technology Magazine

To learn about advertising and sponsorship opportunities, contact us.

The ConFab | 半導體科技 先進封裝測試 | 半导体科技 制造 封装 测试 Solid State TECHNOLOGY Advanced Packaging CHINA

www.solid-state.com

PennWell® MEDIA FOR STRATEGIC MARKETS SINCE 1910