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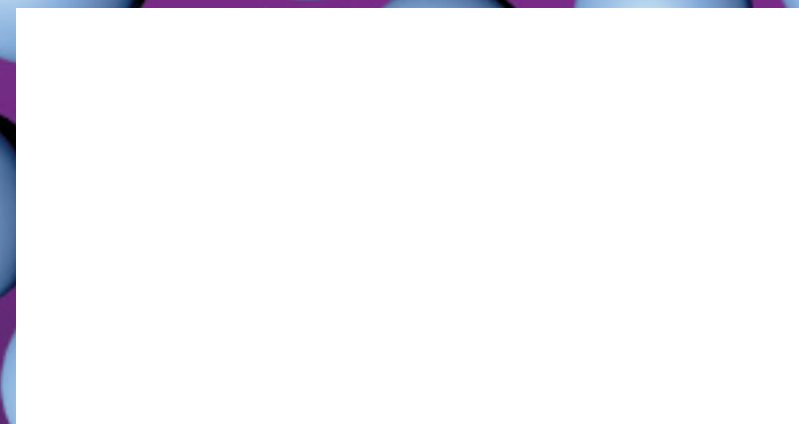
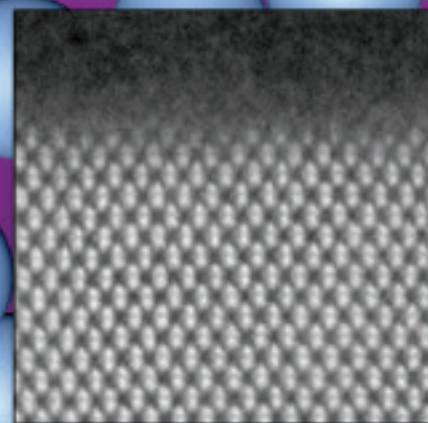
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Atomic layer processes introduce the reactants sequentially through a set of repeated self-limiting cycles. Source: Lam Research Corp.

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### **ETCH** | [Moving atomic layer etch from lab to fab](#)

A new plasma-enhanced atomic layer etch method delivers atomic-level etch precision with process times that are practical for use in a manufacturing environment. *Keren J. Kanarik, Samantha Tan, John Holland, Aaron Eppler, Vahid Vahedi, Jeff Marks, And Richard A. Gottscho, Lam Research Corporation, Fremont, CA USA*

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### **FinFETs** | [FinFET evolution for the 7nm and 5nm CMOS technology nodes](#)

In addition to extending the fin-based design investments, augmenting the FinFET for improved performance allows an evolution of the process infrastructure for a few more nodes. *Aaron Thean, imec, Leuven, Belgium*

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## Web Exclusives

### **SemiMD** More than Moore – manufacturing challenges for MEMS

Semiconductor Design & Manufacturing discussed 'More than Moore' (MtM) standardization topics and challenges with Peter Himes, VP of marketing and strategic alliances at Silex Microsystems, Dr Eric Mounier, senior analyst, MEMS devices and technologies at Yole Développement, Tom Morrow, chief marketing officer at SEMI and Mike Rosa, senior global product strategic marketing manager – emerging technologies, 200mm components and systems group at Applied Materials.

### **SemiMD** Design For Yield (DFY) moves closer to the foundry/manufacturing side

SemiMD discussed the trend for design for yield (DFY) moving closer to the foundry/manufacturing side with Dr Bruce McGaughy, Chief Technology Officer and Senior Vice President of Engineering, ProPlus Design Solutions, Ya-Chieh Lai, Engineering Director, Silicon and Signoff Verification, Cadence and Michael Buehler, Senior Marketing Director, Calibre Design Solutions, Mentor Graphics, and Amiad Conley, Technical Marketing Manager, Process Diagnostics and Control, Applied Materials.

### **SemiMD** Pervasive Computing: Are You Ready?

Pervasive computing is changing the landscape of the microelectronics industry, fragmenting the future of both Moore's Law and More-than-Moore technologies. At the leading edge, we have FinFETs versus FD-SOI; in memory, every roadmap involves novel devices and novel material sets; in 3D stacking, we have foundries, OSATs and IDMs developing alternative paths. In markets, the smart phone and tablet boom is moderating, China and India are cooling, but new markets, such as the all-connected Internet of Things, have the potential to create an entire new ecosystem of buyers, technologies and business models, Karen Savala, president of SEMI North Americas, presents her views on pervasive computing, which is also the focus of the upcoming SEMI Industry Strategy Symposium meeting.



### **Can Intel beat TSMC?**

Zvi Or-Bach, president and CEO of Monolithic 3D, blogs about a recent announcement by Intel CEO Brian Krzanich on company expansion focused on a foundry plan. Or-Bach said that if Intel could keep the traditional 30% cost reduction per node from 28nm to 10nm, and the foundry's cost per transistor is staying flat, then Intel would be able to provide their foundry customers SoC products at a third of the other foundries cost, and accordingly Intel should be able to do very well in its foundry business.

<http://tinyurl.com/q9nf6v6>

### **EUV Source Workshop**

Vivek Bakshi, EUV Litho, Inc. reports on work presented at the 2013 Source Workshop (Nov 3-7, 2013, Dublin, Ireland), including data on the readiness of 50 W EUV sources to support EUVL scanners. At the meeting, keynoter Vadim Banine of ASML said that 50 W EUV sources have now demonstrated good dose control and are now available for deployment in the field.

<http://tinyurl.com/phegnrq>

### **Apple in NY?**

Dick James of Chipworks says that 28-nm samples they have seen from GLOBALFOUNDRIES and Samsung are remarkably similar, and ponders the possibility of Apple's A7 chips being fabricated in New York in the not too distant future.

<http://tinyurl.com/po5fboc>





# Semiconductors that detect cancer

As exciting as it is to watch the semiconductor industry push to sub-10nm dimensions, 450mm wafers, finFETs, 3D ICs and the like, what's even cooler is the potential of semiconductor technology to make a real difference in medicine. I firmly believe that a mobile health revolution is in the making, where people will be able to use their smart devices to monitor their personal health through an array of body sensors.

The next step is to build thousands of channels on a single chip.

Semiconductor and related technologies such as microfluidics will also play an increasingly important role in medical diagnostics. This was brought home to me at the recent imec International Technology Forum Press Gathering in Leuven, Belgium, where imec CEO Luc Van den hove provided an update on blood cell sorting technology that combines semiconductor technology with microfluidics, imaging and high speed data processing to detect tumorous cancer cells. Similar technologies are slated to be presented at IEDM this month as well.

Cancer spreads throughout our body through circulating tumor cells that originate from the primary tumors, and create secondary tumors. Usually those are the most fatal ones. "If we can develop a system that can detect those circulating tumor cells in a very early phase, we develop an early warning system for cancer," Van den hove said.

Today, single cell analysis requires a lot of manual operations, sophisticated (and expensive) tools that require a lot of time to generate the results. Very often those results are not accurate enough or not sensitive enough. "What we actually need is a much more engineering type approach where we start from the clinical samples directly, and one that is much more automated. At imec, we are developing a high content, high throughput cell sorter, which is much more compact than any cell sorter ever made," he said.

Imec has so far demonstrated all the building blocks of this technology and demonstrated proof of principle with a single channel. The next step is to build thousands of channels on a single chip. "With silicon technology, we can very easily integrate thousands of those channels on one chip and in this way, realize the enormous sensitivity that is needed in order to detect these bad tumor cells in a billion cells.

—Pete Singer, Editor-in-Chief

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## worldnews

**ASIA | Dongbu HiTek** began volume production of 5.0 Megapixel CMOS Image Sensor (CIS) devices for **Superpix Micro Technology Co., Ltd.**, a fabless customer based in Beijing.

**EUROPE | SUSS MicroTec** installed an ELP300 excimer laser stepper to support next generation advanced packaging and 3D IC laser debonding applications at the **Fraunhofer Institute for Reliability and Microintegration (IZM)**, Berlin.

**USA | AMD** was selected for an award of \$3.1 million for a research project associated with the **U.S. Department of Energy (DOE)** Extreme-Scale Computing Research and Development Program, known as "DesignForward."

**EUROPE | STMicroelectronics** and **Yogitech**, a provider of functional safety solutions, have signed an agreement to create a comprehensive package that will simplify the development and certification of safety-critical applications based on STM32 microcontrollers.

**USA | Spansion Inc.** launched a family of microcontrollers addressing high performance and low power needs for industrial applications such as factory automation, building management, inverter drives, smart meters, home appliances and medical devices.

**WORLD | FlipChip International** acquired **Millennium Microtech**, a provider of fully integrated semiconductor packaging and testing services situated in the Zhang Jiang Hi-Tech Park, Pudong New Area, Shanghai, China.

## Status update on logic and memory roadmaps

The way in which logic and memory technology is likely to evolve over the next six years was provided at imec's recent International Technology Forum in Leuven, Belgium. An Steegen, senior vice president process technology at imec, said that FinFETs will likely become the logic technology of choice for the upcoming generations, with high mobility channels coming into play for the 7 and 5nm generation (2017 and 2019). In DRAM, the MIM capacitor will give way to the SST-MRAM. In NAND flash, 3D SONOS is expected to dominate for several generations; the outlook for RRAM remains cloudy.

The 14nm node (which imec calls the "N" node") is in development today, heading toward early production in 2013/2014. That will be followed by the N10 node in production at the end of 2015 and beginning of 2016. Then N7 and N5 will follow in 2017 and 2019.

The most notable evolution in the logic roadmap is that of device architecture, where planar devices are being replaced by fully depleted devices. There are two main flavors of fully depleted devices: fully depleted SOI (FDSOI) and finFETs. Imec sees FDSOI as an option for 14nm, which is "actually a speed push option from 20nm," Steegen said. "What's happening is that in the 14-16 generation, speed push knobs are implemented on the technology roadmaps to get the extra performance boost for that node." That's partly driven by the readiness (or really unreadiness) of EUV. "Scaling is not necessarily the .7X one dimensional scaling that you expect node to node," Steegen said. That's why, in the 16-14nm

generation, planar devices are being replaced by a higher performing fully depleted device. "When you push this to 10 and 7nm that we believe that the finFETs are going to have a long lasting life," she added, which means that we will see finFETs on the roadmap for at least three generations.

Steegen said imec is now mainly focused on assessing processes for 7nm and trying to figure out when the ultimate finFET scaling limit will be hit. At that point, expect to see what imec calls "local SOI," which is a slight undercut of the bulk silicon fin to provide better isolation in the well. A more extreme version gate all-around device, which could be based on silicon nanowires.

To boost performance in the past, external source/drain stressors were used to increase electron and hole mobility in the device. The problem moving forward, in the N10 and N7 generations, is that there's no space to do that. Instead, expect to see replacement of the silicon channel with a high mobility material. "When you look at what material that could be, germanium is a good candidate to push hole mobility, so the PFET. And III-V, InGaAs, is a good material for NFET devices to push the electron hole mobility," Steegen explained.

Beyond high mobility designs, efforts are underway to reduce VDD supply voltage as well as the subthreshold slope in transistors, and to optimize multi-Vt designs. Eventually, lateral finFETs built from silicon nanowires may be required. Steegen said power was a concern in both high performance logic devices, which are thermally



limited, and in mobile devices, which are battery limited. "What we've been trying to do at all our technology nodes is to try to step down that power curve, mainly by trying to lower the Vdd," she said. The trick, she said, was to lower the power, but still retain performance, and the best way to do that is to make the subthreshold slope of the device steeper. She said the target was 16mv/decade, which is the limit of conventional transistors.

There's a tradeoff, however, in that reduced Vdd often means increased variability, depending on the threshold voltage of the devices. "On the High Vt device, when you go low Vdd, you're so close to the threshold voltage of your device that the spread becomes enormous. What you could do is switch to a low Vt device. That's better for variability but your leakage is going to increase," she said.

At imec, their research is focused on bulk silicon finFETs (others are exploring fully depleted SOI) with a replacement gate and high k. Work is still underway on ways to best integrate a replacement metal gate, and on multi-Vt devices. "That's still work we are executing," she said. She noted that imec has worked on high-k metal (HKMG) gates for more than 15 years, and is now looking at how to implement a replacement metal gate on a finFET device and engineer the Vts. "You also need to make sure your reliability comes together," she said.

One way in which they have enabled multi-Vt tuning (range up to 600mV) is with controlled Al diffusion in metal gate stack. "You want to make sure you can offer the designers a low Vt device, a standard Vt device and a high Vt device, which means that you need to be able to tweak the materials in your gate to cover that entire range of Vt scaling," Steegen said.

She added that, for the 10nm node, they are engineering an entire silicon finFET platform. "That means we work on every single module going in, from scaling to the N10 dimensions, control of the fin height, making sure you get conformal doping in the fin, and source/drain engineering because you still want to get some form of stress from your source/drain."

For the 7nm node, Steegen believes the channel materials will need to be replaced with higher mobility materials, germanium for PFETs and InGaAs for NFETs. To integrate these materials, a technique known as Aspect Ratio Trapping (ART) is used. This technique uses high aspect ratio sub-micron trenches to trap threading dislocations, greatly reducing the dislocation

density of lattice mismatched materials grown on silicon. "You have engineer your dislocations and defects," Steegen said.

ART is shown to be very effective for a wide variety of materials including Ge, GaAs and InP. It has been combined with epitaxial lateral overgrowth to create long, 18 micron wide strips of low dislocation density material. ART has been used to integrate many types of Ge and III-V devices on silicon including GaAs MOSFETs, GaAs lasers, GaAs tunnel diodes and a silicon infrared imager chip with monolithically integrated Ge photodiodes.

For PFETs, the technique involves, "recessing the silicon, growing silicon germanium buffer back and then



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strained germanium on the top. The STI is then going to be recessed and you have a strained germanium fin on the top," Steegen explained. The same integration scheme is used for NFETs, but "it's a little more complex to try to get to a strained InGaAs NFET channel because the lattice mismatch with silicon is larger. You have to use more buffers here and go a little bit deeper to grow all these buffers through the trench," she said. "Aspect ratio trapping makes sure all the defects -- and you're going to have them in that strained/relaxed buffer -- are trapped at the sidewalls of the STI so that they don't reach the top silicon."

This added complexity appears to be worth the effort based on modeling, which shows a net gain of 25% more performance at constant power, compared to a bulk silicon finFETs. "There is still a lot of benefit you're going to get in one node by replacing these channel materials," Steegen noted.

Beyond 7nm, imec is looking at higher mobility materials such as graphene, and also looking at new device architectures such as tunnel FETs. "At this point, we are looking at germanium source tunnel FET to overcome the tunneling barrier with a lower bandgap material at the source," Steegen said. "We truly want to try to break that 60mv/decade subthreshold slope." She said lots of progress has

been made but there was more work to do to understand band-to-band tunneling mechanisms. The team is also looking at "2D" materials such as molybdenum disulfide and tungsten diselenide.

As far as standalone memory (vs embedded memory) goes, STTMRAM is now being pushed forward to basically replace the MIMCAP on the DRAM roadmap. That's because it's very challenging to get an EOT of 0.3 (see table) and maintain acceptable leakage of the MIM capacitor.

For NAND flash, Steegen said the two-dimensional hybrid floating gate integration flow is definitely being pushed to a 15 and 13nm half pitch. "Scaling is one challenge you're going to encounter here. The other one is the charge you can trap on the floating gate itself. It becomes so discrete there's hardly any charge left. The variability you're going to have on the hybrid floating gate concept is likely getting too big. That is why 3D SONOS is definitely getting it's way in on the NAND flash replacement roadmap and also we forecast that to have quite a long lifetime: two or three generations," she said.

Steegen said the outlook for RRAM was cloudy. It could be the eventual successor to 3D SONOS, but "if you want to replace 3D SONOS, you're getting to need 3D RRAM because you're going to use the same 3D configuration. Also, for NAND flash replacement, you always need that select

element to make sure you only select that one cell you want to turn on. How to integrate the selector with the RRAM element in

a 3D configuration is going to be the trick of how RRAM can enter this NAND flash roadmap at the end," she said. ♦ P.S.

## GLOBALFOUNDRIES, Open-Silicon and Amkor demo 2.5D test vehicle

GLOBALFOUNDRIES, Open-Silicon and Amkor Technology have jointly exhibited a functional system-on-chip (SoC) solution on a 2.5D silicon interposer featuring two 28nm logic chips, with embedded ARM processors. The jointly developed design is a test vehicle that showcases the benefits of 2.5D technology for mobile and low-power server applications. The companies recently demonstrated the functioning SoC at ARM TechCon in Santa Clara, CA.

The test vehicle features two ARM Cortex-A9 processors manufactured using GLOBALFOUNDRIES' 28nm-SLP (Super Low Power) process technology. The processors are attached to a silicon interposer, which is built on a 65nm manufacturing flow with through-silicon-vias (TSVs) to enable high-bandwidth communication between the chips.

Open-Silicon provided the processor, interposer, substrate, and test design, as well as the test and characterization of the final product. GLOBALFOUNDRIES provided the PDKs (process design kits), interposer reference flow and manufactured both the 28nm ARM processors and the 65nm silicon interposer with embedded TSVs. Amkor provided the package-related design rules and manufacturing processes for back-side integration, copper pillar micro-bumping, and 2.5D product assembly. GLOBALFOUNDRIES and Amkor collaborated closely throughout the project to develop and validate the design rules, assembly processes, and required material sets.

The companies developed the custom SoC to help overcome some of the challenges associated with bringing 2.5D technology to market. The 2.5D system features the following characteristics:

- Logic die including dual-core ARM Cortex-A9 CPUs, as well as DDR3, USB and AXI bridge interfaces
- A special EDA reference flow designed to address the additional requirements of 2.5D design, including top-level



interposer design creation and floor planning, as well as the increased complexity of using TSVs, front-side and back-side bumps, and redistribution layer (RDL) routing

- Support for additional verification steps brought on by 2.5D design rules
- Custom die-to-die IO for better area and power characteristics providing a maximum of 8GB/s full-duplex data-rate across the two die through the silicon interposer
- A development board with memory, boot-ROM, and basic peripherals to demonstrate the die-to-die interface functionality through software running on the CPUs embedded in the logic dies
- A test methodology consisting of Boundary Scan and Loopback modes
- Package-related design rules, back-side integration, copper pillar micro-bumping, and 2.5D product assembly by Amkor Technology, a leading supplier of outsourced semiconductor packaging and test services.

GLOBALFOUNDRIES said this demonstrates the value of its open and collaborative approach to delivering next-generation chip packaging technologies, which it calls "Foundry 2.0," which is aimed at enabling an open supply chain through collaboration with ecosystem partners and customers. This approach allows GLOBALFOUNDRIES' customers to choose their preferred supply chain partners, while leveraging the experience of ecosystem partners who have developed deep expertise in design, assembly and test methodologies. This open and collaborative model is expected to deliver lower overall cost and less risk in bringing 2.5D technologies to market.

"As the fabless-foundry business model evolves to address the realities of today's dynamic market, foundries are taking on increasing responsibility for enabling the supply chain to deliver end-to-end solutions that meet the requirements of the broad range of leading-edge designs," said David McCann, vice president of packaging R&D at GLOBALFOUNDRIES. "To help address these challenges, we are driving our 'Foundry 2.0' collaborative supply chain model by engaging early with ecosystem partners like Open-Silicon and Amkor to jointly develop solutions that will enable the next wave of innovation in the industry."

The companies demonstrated first-time functionality of the processor, interposer, and substrate designs, and the die-to-substrate (D2S) process used by the supply chain resulted in high yields. The design tools, process design kit (PDK), design rules, and supply chain are now in place and proven for 2.5D interposer products from GLOBALFOUNDRIES, Amkor, and Open-Silicon.

"This project is a testament to the value of an open and collaborative approach to innovation, leveraging expertise from across the supply chain to demonstrate progress in bringing a critical enabling technology to market," said Ron Huemoeller, senior vice president of advanced product development at Amkor Technology. "This collaborative model will offer chip designers a flexible approach to 2.5D SoC designs, while delivering cost savings, faster time-to-volume, and a reduction in the technical risk associated with developing new technologies."

"We are pleased to be at the forefront of making 2.5D a reality with our foundry and OSAT partners," said Dr. Shafy Eltoukhy, vice president of technology development at Open-Silicon. "This approach will allow designers to choose the right technology for each function of their SoC while simultaneously enabling finer grain and lower power connectivity than traditional packaging solutions along with reduced power budgets for next-generation electronic devices." ◀

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## EUV is late but on the way for 10nm; DSA is promising

EUV lithography is late, but it is on the way and will be ready for insertion into the 10nm node, which is slated to go into production in late 2015/early 2016. Meanwhile, results from early work into directed self-assembly (DSA) is quite promising. DSA could be used in conjunction with EUV for the 7nm node, scheduled to go into production in the 2017/2018 timeframe. These were some of the conclusions from the imec International Technology Forum for the press earlier this month, where the latest results from EUV and DSA work were presented. Imec and ASML also announced an advanced patterning center that will be based at imec's Leuven campus focused on EUV. Luc Van den hove, president and CEO of imec, described EUV as a cost-effective lithography approach that is "absolutely needed." He said: "We realize that EUV is late. There are challenges here. But I have to say over the last couple of months, significant and steady progress has been realized." In terms of imaging performance, imec has been characterizing some of the latest hardware together with ASML and have showed very good resolution performance of 13nm half pitch and 22nm contact holes. "With

double patterning, we have even demonstrated 9nm half pitch," Van den hove said. "Who would have thought a couple of years ago that this would be realizable with lithography?" Adequate source power, which directly determines throughput, is one of the challenges. "We are seeing a steady increase quarter by quarter," Van den hove said. "We see that we get the improvements and I'm very convinced that very soon EUV will be ready to enter manufacturing."

An Steegen, senior vice president of process technology at imec, provided some more details: "The stand-alone Cymer source has been demonstrated at 55Watt. The next checkpoint is the 80W by the end of 2013. That is on the assembled system, source and scanner, and [throughput] should be approximately 58 wafers/hour. The goal is by the end of 2014, about 126 wafer/hour," she said.

Steegen said ASML's 3300 system has already been verified. "We definitely and clearly can see the resolution benefits as well as overlay capability," she said (the demonstrations were done in at ASML's facilities in Veldhoven; imec has a 3000

system installed, but won't get a 3300 until February 2014).

The ideal entry point for EUV is the 10nm node (or N10 using imec's terminology). "If you look at the cost calculation, the best entry point for EUV is actually at N10 because you can replace triple patterning layers in immersion with a single patterning layer in EUV," Steegen said. Since that will come relatively soon with early production occurring toward the end of 2015 and in early 2016, that means that likely the whole development phase will have already been built on immersion and multi-patterning. "Likely you will see on the most difficult levels, a swap, an introduction of EUV at the most critical levels later on in manufacturing for N10," Steegen said. "That is still what the forecast is today. You would also see a benefit later on inserting EUV in N10."

When you move to N7 and do multi-patterning, it's getting even more complicated, since almost every level is going to be triple patterning. "If you replace that with EUV, will still be going to try to have single patterning on most of the levels, but there's some complexity coming in even with EUV, that you would have to go to multi-patterning for N7 to get to those dimensions," Steegen added. However, she acknowledged that more work needed to be done. She

noted that defectivity in mask and the reticles was still a challenge, particularly those defects embedded in the multi-layered films. "Between those multi-layers in the reticle, you might have embedded defects that you can't see today with any inspection tool. You actually need an actinic inspection tool that also runs at the wavelength of the EUV tool to really see those embedded defects on the reticle. Today, the only way we find those is by printing the wafer and see the printable defects in your patterns," she said.

Van den hove added: "Now that the tool is really progressing tremendously and becoming ready for manufacturing, you also have to make sure that the rest of the infrastructure is ready. In our program, we are now focusing very much also on how to handle defects – defectivity on the mask is one of the big challenges."

In an earlier interview, Veeco's Tim Pratt, Senior Director, Marketing, said that indeed the next major roadblock to progress in the ongoing push to develop EUV lithography for volume production is the availability of defect-free mask blanks. He said that the tools in place today are not capable of producing mask blanks with the kind of yield necessary to support a ramp in EUV. Imec is also evaluating the use of a pellicle on EUV reticles. Pellicles are used to



keep particles from falling on the reticle during exposure and transport, but since EUV masks are reflective instead of transparent, it's not clear how a pellicle would work. "For years, we have been thinking that pellicles would be impossible in EUV, and whether we can use a pellicle or not," Van den hove said. But he said there were some options that are being evaluated at this moment. Steegen said: "We're looking into would it make sense to avoid added defects during scanning to introduce a pellicle on these EUV reticles."

Steegen also said they have also seen good progress with the resists needed for EUV for the 22/20nm contact hole and line space range, including improved line edge roughness (LER) and local critical dimension uniformity (LCDU). "We see quite some improvement in LER post-etch and also in LCDU post-etch where we combined the exposures on the 3300 with etch and basically try to improve our line edge roughness and local CDU," she said. Imec has integrated litho and etch together in such a way that the resulting dimensions are improved after etch. "What you can see is that you cannot only shrink your holes after etch, but you also improve your line edge roughness and local CDU after etch," Steegen said. "That's pretty significant because basically you can shrink the nominal dimension of the hole by about 14% and the local variation of that CD,

we can improve about 30% post etch."

Here's how imec summed up EUV's readiness:

- NXE-3300 resolution benefit and overlay capability demonstrated.
- CH and LS resist materials for NXE-3300 selected, based on CDU, LER/LCDU and defectivity; good progress in resist process down-selection towards 16nm LS (@ 0.33NA)
- 4.2nm of CH CD reduction for 26 nm HP post etch (14%); 1.4nm LCDU reduction for 26nm HP post etch (30%)
- Source power and mask defectivity remain key challenges:
- ASML/Cymer demonstrated 55W power on standalone Cymer source, outlook 80W (58wph) by YE13, 250W (126wph) by YE14.
- Introduction of actinic inspection tools by 2015 for mask blank embedded defect detection and of pellicle to reduce mask defect adders.
- Expectation that EUV will be introduced at a few critical levels in N10 manufacturing (replace LE3) with cost reduction benefit. Potential EUV area benefit from tip-to-tip and tip-to-line and pitch scaling, with redesign.

Van den hove described direct self-assembly (DSA)

as "very promising" and Steegen said work there has largely focused on reducing defectivity. In DSA, resists that contain block copolymers are deposited on top of guiding structures. The self-directed nature of the process results in very regular patterns with very high resolution.

The trick with DSA is that it requires a double exposure to take away the random patterns at the edge of the device, and the resolution needed for this "cut mask" is also very high. "We're convinced that it's not a replacement for EUV or any high resolution lithography technique. We are very convinced it will be used in conjunction with EUV," Van den hove said. "It certainly keeps the pressure on EUV very high."

Steegen described DSA as a complimentary litho technique that is having quite some momentum. The process starts with a "relaxed" guiding pattern on your wafer. Then, depending on the polymer length in the block copolymer, the space in between the guiding structure is replicated into multiple lines and spaces. "The defectivity of these materials are going to be key to bring the defects down. Our year end target is 60 defects/cm<sup>2</sup> and this needs to go down even further next year," she said.

Work at imec has shown that the polymers, with a hard mask on top, are robust enough to enable the etching of the patterns into silicon. "That's fairly new data and very promising," Steegen said. Imec is already looking at where DSA levels could be inserted into the logic N7 flow, with fins and spacers being primary targets. Steegen said the Metal1 level would be a challenge due to its irregular pattern. "That makes it not easy to be replaced with DSA, but we're looking into techniques to do that," she said.

Here's how imec summed up DSA readiness:

- Good progress in material selection and integration flow optimization for line-multiplication down to 14nm, pattern transfer into bulk Si demonstrated.
- First templated DSA process available using SOG/SOC hard mask stack.
- Focus on defectivity reduction & understanding, currently at 350 defects/cm<sup>2</sup>, YE13 target 60 def/cm<sup>2</sup>
- Alignment and overlay strategy needs to be worked out
- First N7 implementation levels identified: Finfet (replace SADP EUV or SAQP 193i) and Via (replace EUV SP/DP or 193i LE3).

◆ P.S.

# Substrate impact on 2.5/3D IC costs

*At the recent Georgia Tech Global Interposer Technology (GIT) Workshop in Atlanta, the pervasive theme appeared to be whether a change in substrate is required to lower overall costs and help drive HVM (high volume manufacturing) applications. Certainly conference chair Rao Tummala, industry visionary whose name is synonymous with microelectronic packaging, feels the time is right to take a serious look at glass interposers both for their superior electrical performance and their promise of lower costs. The PB substrate manufacturers are also taking a serious look at this market and proposing that they can drive their technology to the required dimensions and electrical performance, though many skeptics (including me) are taking a "show me" attitude about these claims.*

The Yole Developpement presentation pointed out that while 2.5D silicon interposer technology was fully underway at TSMC and GLOBALFOUNDRIES, UMC and SPIL supposedly are near initiation, all of the rumored "driver applications," like the Apple A7, the next gen Qualcomm phone, the Sony PS4, ST Micro's "Wioming" application processor, wide IO memory and the next generation Altera FPGA (see discussion below) have been, at the very least, postponed. While no one would openly reveal what the current and proposed future costs are, it is believed that all of these postponements are due to cost which certainly is not yet meeting the mobile phone requirements of less than 1 cent per sq mm proposed by Qualcomm's Matt Nowak (i.e., this is roughly \$550 for a 300mm wafer of interposers).

While Yole has identified at least 10 products moving towards commercialization, all of them currently require so called high density interposers (i.e. 1  $\mu$ m L/S and as small as 10  $\mu$ m TSV). Currently these dimensions can only be fabricated using front end dual damascene type processing available only at silicon foundries and more recently the OSAT, SPIL.

## Packaging

While Yole is still projecting a greater than \$1B in revenue from 2.5D TSV activity by 2017 (activity revenues including TSV etching, filling, RDL, bumping,

wafer test & wafer level assembly), these projections only hold if the current "postponed applications" are quickly commercialized.

During the Amkor presentation Ron Huemoeller indicated that lowering cost could come from elimination of backside RDL on the interposers by arranging pin out on the top side high density interconnect.

Huemoeller sees high end applications being dominated by silicon, mid end applications like graphics possibly using glass and the low end applications (yet unidentified) being wide open. He sees GPU + HBM (high bandwidth memory) being adopted in 2015 and tablets and processors adopting interposer solutions the following year.

In terms of organic "interposers" he indicates that Shinko and Semco are in limited sampling of 2/2 (L/S) and Kyocera 5/5. He labels Unimicron as in "early development."

After making the standard argument that 2.5/3DIC was needed to combat the costs of continued scaling and that system level cost savings could pay for interposer costs, Dave McCann of GLOBALFOUNDRIES indicated that GF was achieving near 100% yields with reticle sized interposers having 4 layers of high density interconnect.

McCann predicted we would see voltage regulator function on future interposers. He also described a program between Global (chip and silicon interposer), Open-Silicon (design), Cadence (EDA tools) and Amkor (assembly and test), which produced a functional processor vehicle featuring two 28nm ARM Cortex-A9 processors connected on a 2.5D silicon interposer built on a 65nm manufacturing flow. The program demonstrated first-time functionality of the processor, interposer, substrate and the die-to-substrate assembly process. The design tools, process design kit (PDK), design rules, and supply chain are now in place for other activities.

Inherently most believe that all things being equal, glass should be a lower cost interposer solution since it can be processed in large format. However, one interesting question from the audience was "Why are silicon and glass wafer the same price?"

Although the data from experts like Professor Kim from KAIST confirms that glass is a better electrical performance solution, especially for RF applications, the major issue is that a complete infrastructure is not yet in place to manufacture such glass interposers. ◀



**Dr. Phil Garrou,**  
Contributing Editor





# Progress on 450mm at G450C

*At Semicon Europa, Paul Farrar, general manager of G450C, provided an update on the consortium's progress in demonstrating 450mm process capability. He said 25 tools will be installed in the Albany cleanroom by the end of 2013, progress has been made on notchless wafers with a 1.5mm edge exclusion zone, they have seen significant progress in wafer quality, and automation and wafer carriers are working.*

G450C is an initiative by five big chip makers — Intel, TSMC, GLOBALFOUNDRIES, IBM and Samsung — partnered with New York state and CNSE. The main goal is to develop 10nm capability on 450mm wafers in 2015 or 2016. “What we have to demonstrate is that a film on 300mm, when we scale it up to 450mm, we can do it with the same capability and, more importantly, at a very significantly reduced cost per process area. In other words \$/cm<sup>2</sup> need to go down significantly. That's how you hit the scaling that we've typically seen in a wafer transition which is in the 30% range,” Farrar said.

Farrar said the facility looks quite different now than it did in March, when it was fairly empty. 18 tools have been installed so far, with a total of 25 tools delivered into the Albany complex by the end of 2013. “2013 is the year that I call install and debug,” Farrar said. “We'll have approximately 50% of the toolset in the facility by the year end. It doesn't mean that they'll all be up and running but they will be placed in Albany or virtually at the suppliers, with about 35% of the toolset coming in 2014 and the last little bit that will be delivered will be the lithography tool in early 2015.” The program is organized around unit processes, including: film deposition and growth, wafer clean and strip, CMP and

other processes, inspection and metrology, etch and plasma strip, and lithography.

In call cases, G450C will have at least one process that will be required for the 14nm flow. In most cases (about 70%) they will have multiple suppliers, at least two and sometimes three. “At the end, we'll have both unit process and what I would call modules – 2 or three step processes – demonstrated. And then our member companies will take those building blocks and they will put their devices and their IP and then go build out factories,” Farrar said.

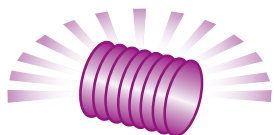
G450C is also trying to take advantage of having a clean slate to make a switch from notched wafers – which provide a useful indicator regarding the crystal orientation of the silicon – to notchless wafers, which are perfect circles. “If you think about the physics around a notch, it really makes it difficult to get uniform films,” Farrar said. “A circle is a lower stress form. We get 1-1.5% better in getting closer to the edge. Using chips around the notch and perhaps getting to 1.5mm edge exclusion. We won't get there if we don't have notchless wafers. Our goal is to collaborate with our IC makers, our tool suppliers and materials suppliers, along with our facilities group.”

Probably the most critical part of the 450mm puzzle is lithography. Farrar said the consortia has been working with Nikon. “We were able to work with Nikon so that we now have immersion capability, in Japan, starting in June of 2014 and we'll then have that tool installed in Albany at the end of the first quarter of 2015. We will have a true lithography capability which will enable us to get the efficient and actual process recipes that the deposition supplier will need to see so that they can demonstrate the capabilities at the 450 wafer form factor,” he said. “In the interim, we're working on DSA (directed self assembly). We're starting to see some pretty good results. I don't think this will be a high volume technique but it's a way that we can get something that works started in the early process modules in 2013 and early 2014.”◆



**Pete Singer,**  
Editor-in-Chief

## Semiconductors



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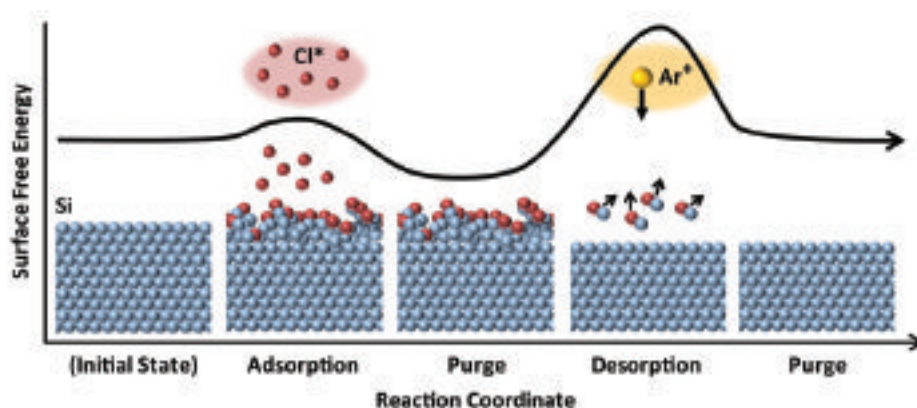


# Moving atomic layer etch from lab to fab

**KEREN J. KANARIK, SAMANTHA TAN, JOHN HOLLAND, AARON EPPLER, VAHID VAHEDI, JEFF MARKS,**  
and **RICHARD A. GOTTSCHO**, Lam Research Corporation, Fremont, CA USA.

*A new plasma-enhanced atomic layer etch method delivers atomic-level etch precision with process times that are practical for use in a manufacturing environment.*

Extending Moore's Law will rely increasingly on high-precision processes to form minuscule device features with high-quality film surfaces. At the sub-14nm technology node, transistor performance will be highly sensitive to process variations, which can significantly impact current leakage and battery power loss. To give some perspective on the reality of the challenges, within the next 10 years, transistor gate dimensions are expected to be less than 50 atoms wide, and feature size variations will be measured in atoms, including contributions from surface roughness. Atomic layer processes are the most promising path for delivering the precision needed at this scale. Atomic layer deposition (ALD) has been in production for over a decade in the semiconductor manufacturing industry. However, it has been difficult making the etch counterpart -- atomic layer etch (ALE) -- productive enough for cost-effective manufacturing, and a commercially viable system has not been available. Here, we report on a plasma-enhanced ALE method using a commercial plasma reactor that provides atomic-level precision with process times that are suitable for high-volume device manufacturing.

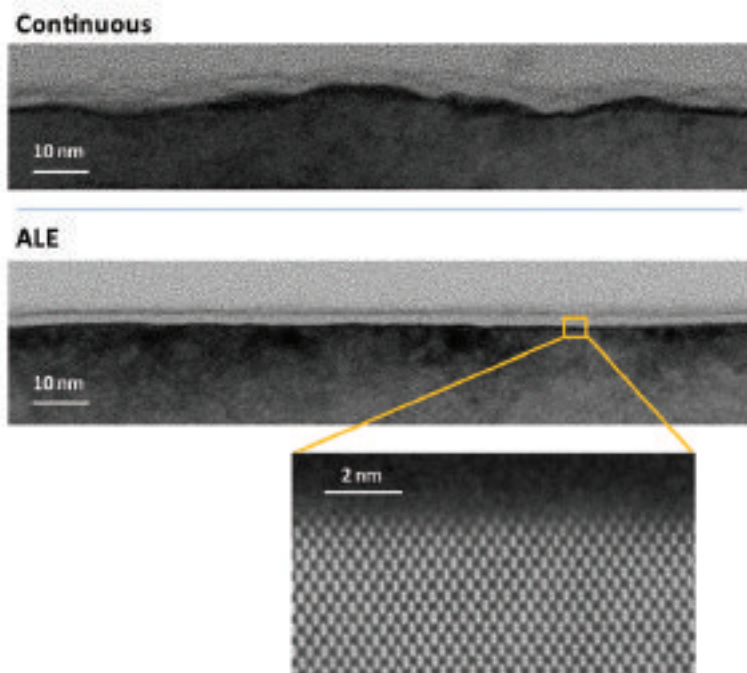


**FIGURE 1.** Illustration of the process steps in a plasma-enhanced ALE cycle for a silicon film etched by chlorine and argon.

## Promise of atomic-layer processes

Although used in the semiconductor industry for nearly 40 years, continuous deposition and etch processes are inherently imprecise due to how they are executed. Typically, all of the reactants are introduced into the process chamber simultaneously, where they interact concurrently and continuously with the exposed film surfaces. As a result, the film thickness is often strongly dependent upon parameters such as reactant flux, which can vary locally as well as across the wafer. While continuous processes can be optimized to be more precise, for example in terms of uniformity and film smoothness, it is often difficult to compensate for all factors simultaneously.

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**FIGURE 2.** High-resolution TEM images of blanket epitaxial silicon after removal of ~400 atomic layers by continuous and ALE methods under comparable process conditions.

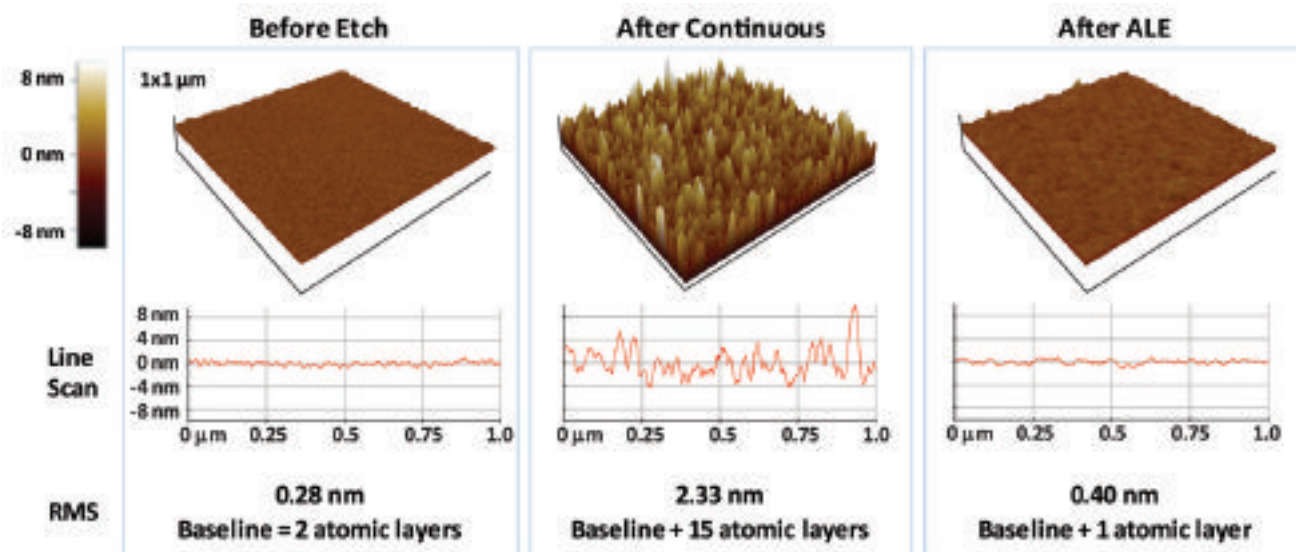
In contrast, atomic layer processes introduce the reactants sequentially through a set of repeated self-limiting cycles. In this case, the amount of film added or removed is controlled by the number of these cycles. The reactions stop when the limited reactants are consumed, and the film surface “resets” to a common state after each cycle. This results in an inherently smooth surface and uniform film.

The challenge in implementing atomic layer

processes in high-volume semiconductor manufacturing is that their rates tend to be very slow, up to several orders of magnitude less than continuous processes. In the case of ALD, fab adoption came after nearly half a century of laboratory work and commercial applications in other industries such as flat panel display. Today, ALD is a mainstream technique used for depositing both metals and dielectrics in production. Although rates are still slower than some chemical vapor deposition (CVD) continuous processes, the associated benefits from ALD are attractive, especially for very thin films or when alternative processes fail to meet requirements. With ongoing improvements in productivity, ALD is expected to be used on an increasing number of emerging films.

### Making ALE faster

Lagging behind its deposition counterpart, ALE was first demonstrated in the laboratory in the early 1990s and has remained a subject of ongoing important research ever since [1]. Unfortunately, achieving productivity levels sufficient for high-volume manufacturing has been challenging. To give a sense of the process times involved, consider the most studied ALE case of etching a silicon (Si) film. Reported cycle times typically vary from ~1 minute to over 5



**FIGURE 3.** AFM data of blanket epitaxial silicon surfaces showing surface roughness before etch, after a continuous etch, and after ALE.

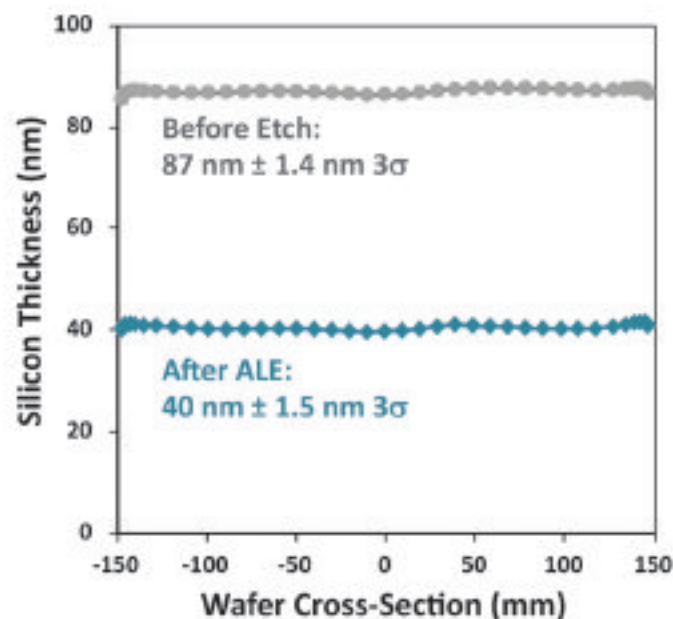


minutes with corresponding etch rates of  $\sim 0.1$  to  $0.01$  nm/min. These long process times are largely due to using thermal adsorption methods and specialized equipment such as ion beam systems for desorption, which are also undesirable from a cost perspective. An attractive alternative is to use a conventional etch reactor and enhance the ALE rate through specific plasma techniques.

To understand how plasma enhancement improves process cycle times, it is useful to consider the individual steps involved in a single ALE cycle. **FIGURE 1** illustrates these steps for the case study of etching silicon with chlorine ( $\text{Cl}_2$ ) and argon (Ar). First, chlorine reactants are adsorbed onto the silicon film surface, and then excess reactants are purged. Next, argon ions are introduced to desorb the silicon chloride byproduct via directional ion bombardment, followed by purging the excess gas. This cycle is then repeated until the desired amount of film has been removed.

The adsorption step has historically been done using thermal methods, in which adsorption occurs spontaneously at room temperature and follows Langmuir kinetics. The time needed to completely saturate the surface has been reported to take  $\sim 30$  seconds. The speed of this step is limited by the time needed for the  $\text{Cl}_2$  molecules to dissociate, which must occur before chlorine can react with a dangling silicon bond at the film surface. With the plasma-enhanced ALE method, chlorine gas is ignited into a plasma, which readily dissociates  $\text{Cl}_2$  to produce radicals that quickly react with the silicon surface. It is worth pointing out that the plasma needs to operate in a regime that minimizes ions and photons with energies above the etch threshold in order to prevent premature, uncontrolled etching.

For the desorption step, bombarding particles are used to provide enough energy to break the Si-Si bonds that have been weakened by adsorbed chlorine. However, bombarding the surface to remove material is somewhat inefficient, and calculations have indicated that it takes  $\sim 10$  particles to remove just one silicon chloride molecular byproduct [2]. This step can be accelerated by applying a high flux of bombarding ions, generated by the same plasma reactor used for the adsorption step. By combining these adsorption/desorption improvements with fast



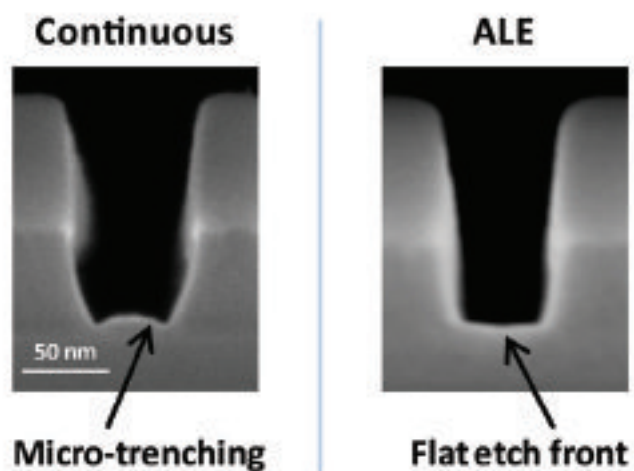
**FIGURE 4.** Uniformity across a blanket silicon wafer before and after the ALE process.

gas-switching capabilities, significantly faster cycle times can be achieved.

### Application of plasma-enhanced ALE

This ALE technique was evaluated on blanket epitaxial silicon wafers along with a continuous plasma process under comparable conditions. The etch rate of the ALE process is found to be significantly faster than has been typically demonstrated. To verify that the ALE process is not simply the sum of physical sputtering and spontaneous chemical surface reactions, these rates were measured and found to contribute insignificantly to the overall etch rate. It was also confirmed that the plasma-enhanced ALE process is self-limiting, with the reactive layer reaching a self-limiting thickness of a few atomic layers. Note that analogous with ALD, the ALE process benefits occur not because each cycle removes exactly one atomic layer, but because each cycle is self-limiting.

To evaluate the surface conditions after etch, blanket wafers were processed by continuous or ALE methods to remove  $\sim 400$  atomic silicon layers ( $\sim 50$  nm) and evaluated with high-resolution transmission electron microscopy (TEM) (**FIGURE 2**). The continuous process produces a rough surface, while the ALE process leaves the surface smooth. Quanti-



**FIGURE 5.** SEM images of polysilicon trenches etched under comparable process conditions.

tative analysis of surface roughness was determined in terms of root mean squared (RMS) using atomic force microscopy (AFM). Prior to etching, the surface roughness was 2 atomic layers (**FIGURE 3**). The data show that the continuous process added 15 atomic layers of roughness due to accumulative effects. In contrast, the ALE process contributed only 1 additional atomic layer of roughness, thus preserving the atomic smoothness of the film. This is attributed to the self-limiting nature of ALE, where the film's surface state resets after each cycle.

The ALE process is also found to be precise on the macroscopic scale. The amount of silicon removed by ALE was measured across the full diameter of a 300mm wafer (**FIGURE 4**). Even though the ALE process was not optimized, the process demonstrates excellent uniformity, indicating relative insensitivity to variations in neutrals and ions across the wafer. This implies relatively high process stability and repeatability, which is an important requirement for high-volume manufacturing.

To characterize performance on patterned features, polysilicon trenches were used to examine etch profiles. As shown by the scanning electron microscope (SEM) images in **FIGURE 5**, the etch front for

the continuous process is micro-trenched, which is a well-known phenomenon that occurs in chlorine/argon plasma chemistries. This effect is attributed to ion scattering from the feature sidewalls, causing the trench side corners to be etched faster than the center [3]. In contrast, the ALE process shows a flat etch front. This is attributed to the self-limiting nature of the process: once the adsorbed reactants are exhausted, the argon sputter rate is too slow to be significant. The overall result is the desired flat etch front with an atomically smooth surface that is uniformly repeated across the wafer.

## Conclusion

A plasma-enhanced ALE method has been presented that delivers atomic-level etch precision with process times that are practical for use in a manufacturing environment. Addressing historical productivity barriers while maintaining self-limiting behavior was achieved by enhancing the adsorption and desorption steps with plasma using a commercially available etch reactor. With this new capability, production-ready ALE is becoming a reality, and this is a significant and exciting milestone for extending Moore's Law.

## Acknowledgments

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# FinFET evolution for the 7nm and 5nm CMOS technology nodes

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*In addition to extending the fin-based design investments, augmenting the FinFET for improved performance allows an evolution of the process infrastructure for a few more nodes.*

With 14nm CMOS technology node soon to be ready for production and the leaders in the industry busy with 10nm development, our R&D focus shifts to scaling devices for the 7nm and 5nm technology nodes. In the post-planar transistor era, chip power continues to be a major challenge and the need for low-voltage transistors is ever more important. With a goal to reduce close to 50% of the supply voltage ( $V_{dd} < 0.5-0.6V$ ) relative to today's most advanced microprocessors in production, significant improvements of transistor short-channel electrostatics as well as performance are sought. It remains hard to tolerate a lackluster performance with density scaling, especially when process cost rises significantly.

"Souping-up" the FinFET is the order of the day. Besides extending the fin-based design investments, augmenting the FinFET for improved performance allows us to gently evolve the process infrastructure for a few more nodes. However, to do better than today's FinFET performance is no easy feat. Just to maintain the sub-threshold swing close to ideal (65 mV/dec-70 mV/dec), a measure of transistor switching quality (important for low  $V_{dd}$ ) (FIGURE 1), fin thicknesses have to be scaled to 7nm or thinner, for gate length of 20nm and 15nm, targeted for 7nm and 5nm, respectively (FIGURE 2). The new paradigm is here, where we have a transistor feature (fin) that needs to be patterned more aggressively than the gate length, while rivaling the device's high-k gate

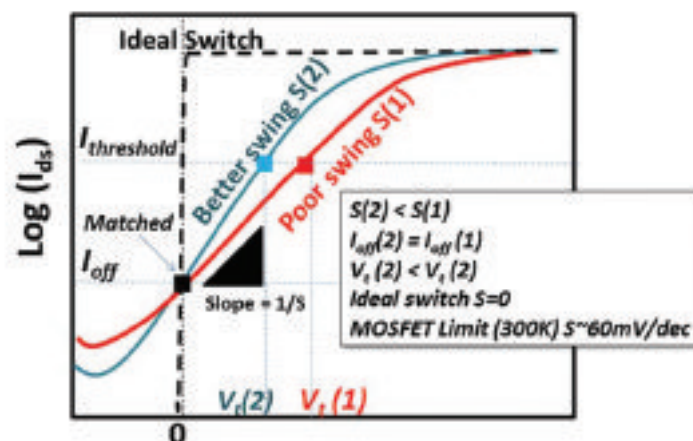


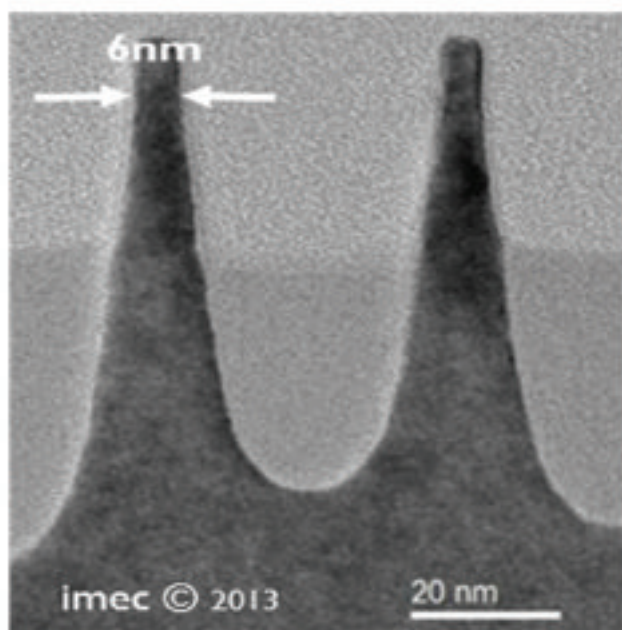
FIGURE 1. Sub-threshold Swing (S) of a MOSFET.

dielectric (typically ~2nm), already in the order of 4 atomic lattices. Moreover, the aggressively-tight gate pitch (~40-48nm by 7nm node) and tiny device volume make doping, and strain engineering for performance very tricky.

Fortunately, we are not at the end of the road yet, and there are options. The first is to extend good-old silicon channel, by focusing on improving electrostatics, leakage isolation issues and strain engineering. Options like gate-all-around (nanowires), steep retrograde wells (ground planes), and Si:C/Ge stressors are being investigated.

We reach for a new bag of tricks as well. Why not replace the Si channel by non-Si high-mobility materials? I mean literally etch out Si and epitaxially re-grow non-Si materials of desired properties. Several





**FIGURE 2.** Cross-sectional TEM images of Si FinFET targeting 10nm CMOS.

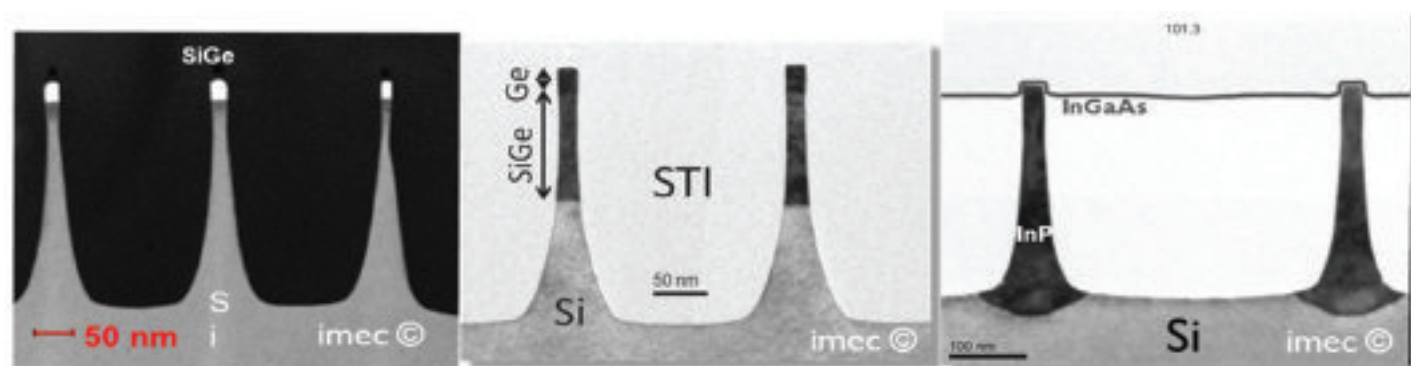
desired high mobility materials are being considered because the effectiveness of conventional stressors, like source/drain stressors, strongly reduces when transistors shrink. We also investigate SiGe, Ge and III-V replacement fin process (**FIGURE 3**).

The learning curve to master these materials (for FinFETs) is steep. For example, introducing Ge into a fin is not a trivial process when it agglomerates easily with higher process temperatures. On the device side, leakages due to narrow band gap, gate-stack passivation, and defectivity are on-going hurdles. Moreover, any technique employed to integrate Ge in the pFET must be CMOS compatible, which means that it must allow a co-integration with materials for nFETs, like Si, III-V materials. For all these challenging options, it is our goal to identify, for our technology partners, the promising options, innovate on the solutions, and

work-out the design/system impact.

Recent work on novel devices that have Ge as a pFET channel material (6x gain in mobility wrt Si) in combination with III-V materials like InGaAs for nFETs, has turned out very promising. For the Ge-channel based pFET, strain boosting technologies are mandatory in order to outperform the conventional strained Si FinFET devices. Imec researchers have found a way to implement strain on Ge pMOS devices by using a Si<sub>1-x</sub>Ge<sub>x</sub> strain relaxed buffer (SRB) that epitaxially-replaced Si. The epitaxial buffer not only helps reducing the mismatch in atomic spacing, it also provides a way of introducing strain in the Ge layer. Besides being an efficient stressor, additional electrostatic benefit arises from the Ge/SiGe quantum well confinement. Some major optimizations in terms of doping and passivation allowed us to achieve good performance characteristics, as will be shown at the upcoming IEDM conference. The co-integration of this first strained Ge-based pFET device with alternative nMOS channel materials however still comes with major integration challenges.

Obviously, there is still much work to do. Also, it has become clear that scaling the transistor into the 7nm and 5nm nodes is no longer 'business as usual'. But looking back at the last ten years, CMOS scaling hasn't been usual either, while still enabling good business. Since the days we replaced Si source-drain with embedded SiGe stressors, we are working our way towards heterogeneous material integration. Exciting possibilities for CMOS and beyond are ahead of us and we need to make it happen through early collaboration on various aspects of the technology: materials, tools, patterning and process integration. Now, we just need to figure our way out of that pesky variability issue. ♦



**FIGURE 3.** Cross-sectional TEM images Left: SiGe on Si Fins, Middle: strained Ge/SiGe on Si, Right InGaAs/InP on Si Fins.

# Advances in back-side via etching of SiC for GaN

**ANTHONY BARKER, KEVIN RIDDELL, HUMA ASHRAF** and **DAVE THOMAS**, SPTS Technologies, Newport, UK. **CHIA-HAO CHEN, YI-FENG WEI, I-TE CHO** and **WALTER WOHLMUTH**, WIN Semiconductors Corp, Hwaya Technology Park, Taiwan.

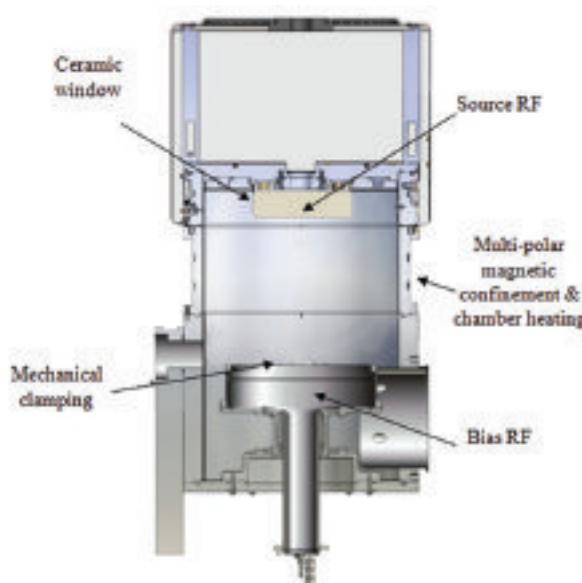
*The development of an 85 $\mu$ m diameter, 100 $\mu$ m deep SiC back-side via etch process for production is described.*

**T**he high breakdown voltage and high electron mobility of GaN make it an attractive material for high power device applications [1]. GaN is typically grown on SiC substrate wafers. Therefore the implementation of back-side vias involves the deep etching of SiC to form conducting pathways to the front-side circuitry [2,3].

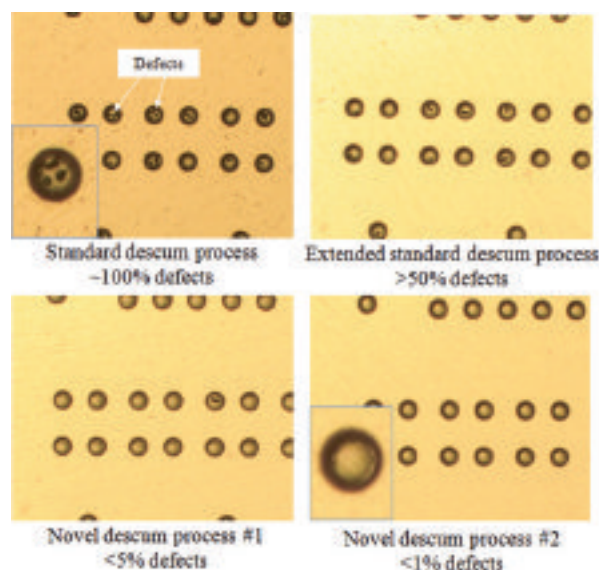
Compared to GaAs the material properties of SiC and GaN make them much more challenging to plasma etch. Energetic plasma processes are required to deliver productive SiC etch rates whilst maintaining high enough selectivity to the masking layer and low enough wafer temperature to preserve the bonding and prevent de-lamination. This requires metal masks and careful attention to the method of wafer clamping and temperature control. Due to the ground finish of the pre-etched SiC surface descum break-through steps are essential in minimising defects within the vias to maximise device yields. In such an energetic plasma environment it is challenging to maintain smooth enough SiC walls for subsequent seed metal deposition/electro-plating and to preserve selectivity to the GaN. The build up of relatively low volatility etch by-products within the via and upon the surfaces of the plasma reactor requires effective wet cleans to be developed for both the wafer and the reactor.

## Experimental

Substrates for etching were prepared by WIN Semiconductors. The 100mm diameter GaN/SiC wafers were temporarily bonded face down to a 100mm carrier.



**FIGURE 1.**



**FIGURE 2.**

**DAVE THOMAS** is etch marketing director at SPTS Technologies, Ringland Way, Newport NP18 2TA, UK, e-mail: dave.thomas@spts.com.

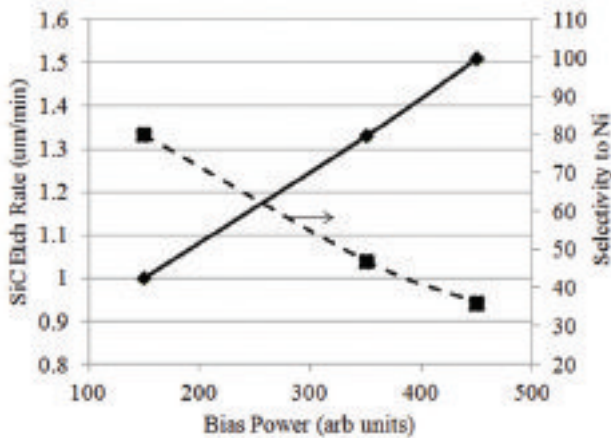


FIGURE 3.

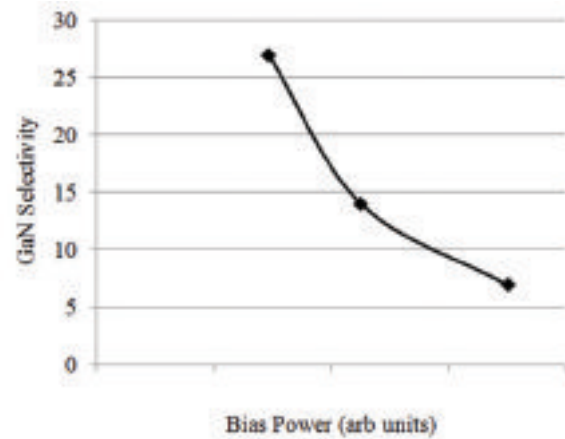


FIGURE 4.

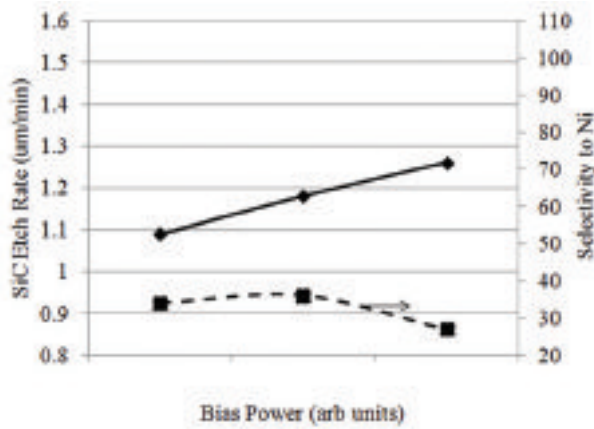


FIGURE 5.

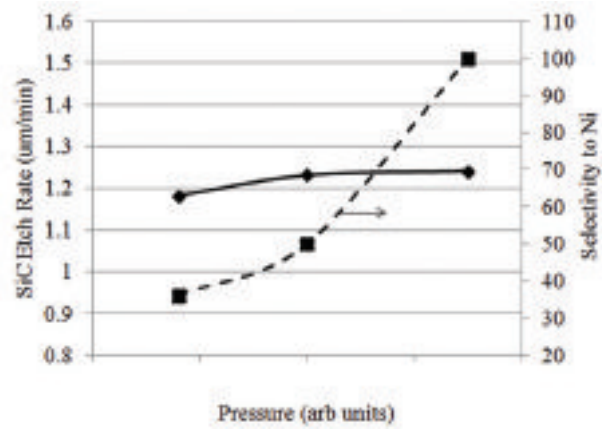


FIGURE 6.

After SiC grinding to  $\sim 100\mu\text{m}$  thickness an electroplated Ni mask was patterned ready for the SiC via etch. Following via etching the wafers were wet cleaned to strip the mask and clean the via of polymer. The GaN layer was then etched, using the SiC via as the mask, stopping on the front-side Au metal. All etching was carried out in an SPTS APS process module. A schematic of the module is shown in **FIGURE 1**.

The reactor is designed with a doughnut-shaped source RF coupling ceramic (13.56MHz at up to 2.2kW), and a heated chamber (set to 50-60°C) with multi-polar magnetic confinement. This arrangement delivers plasma densities in the range  $10^{12}$ - $10^{13}\text{cm}^{-3}$ , typically 10x higher than conventional ICPs. The etch processes used  $\text{SF}_6/\text{O}_2/\text{He}$  and  $\text{Cl}_2/\text{BCl}_3$  chemistries for the SiC and GaN, respectively. A proprietary descum process was developed as part of the SiC via etch in order to reduce/eliminate the formation of pillar defects. Mechanical clamping was used to ensure reliable temperature control during the SiC and GaN etch steps. The platen temperature was set to 10°C. Optical emission spectroscopy (OES) was used to

end-point the GaN etch. Wet chemical via cleaning was also investigated. Processed wafers were analysed using optical microscopy, cross-sectional SEM, profilometry and temperature label measurement.

## Results

Wafer temperature was assessed using '4 level microstrips' (RS Components). These temperature stickers record the peak temperature. Table I summarises the peak temperatures for various wafer types for a 5 minute etch time when the platen is set to 10°C.

Wafer type	Wafer temperature (°C)
Sapphire carrier	100
Bulk SiC	80
SiC bonded to carrier	116

**TABLE 1.** WAFER TEMPERATURES FOR SILICON CARBIDE VIA ETCHING



Process conditions	Etch rate	Selectivity to Ni	Selectivity to GaN	Uniformity	Sidewall quality
Bias power	▲▲	▼▼	▼▼	▲ improves	◀ ▶
Dilution with He	▼	▼	▼	▲▲ improves	▲ improves
Pressure	▲	▲▲	▲	▼ degrades	▲ improves
Ar addition	▲	▼▼	▼▼	◀ ▶	▼▼ degrades

**TABLE 2. PROCESS TRENDS FOR SILICON CARBIDE VIA ETCHING**

These temperatures are safely below the the maximum allowable (dictated by the temporary bonding layer) which is 130°C in this case.

Due to the wet chemical etches of the metal seed layers and the SiC grinding that take place prior to the SiC via etch it is necessary to introduce a descum step as part of the via etch process. Optical images of SiC vias are shown in **FIGURE 2** after partial etching with a range of descum conditions. Standard descums are ineffective, resulting in defectivity levels of 50-100%. A proprietary approach has been developed that substantially reduces pillar defectivity to <1%.

**FIGURE 3** shows the SiC etch rate and the Ni mask selectivity for the main etch conditions as a function of bias power. The wafers were run with the optimized descum but the impact of the descum on the etch rate and selectivity has been subtracted.

The data clearly shows that there is a balance required between maximizing the etch rate and conserving sufficient Ni mask by optimizing the selectivity.

**FIGURE 4** shows selectivity to the GaN underlayer across a similar bias power range. The improvement in selectivity with reducing bias power makes a 2 step (soft landing) approach appropriate for this application.

Having investigated the etch rate and selectivity trends it was necessary to focus on improvements to the sidewall roughness of the via. **FIGURE 5** shows the impact of chemical dilution on the SiC etch rate and mask selectivity. Here the He flow was increased so as to be the primary process gas. There is a corresponding reduction in the slopes of the graphs. Lower etch rates result under these conditions but the selectivity becomes a softer function of bias power which

can help in tuning the process. Dilution was found to improve sidewall quality and improve within wafer etch rate uniformity. The next stages of the development saw a move to higher pressure to drive the SiC etch rate and selectivity up whilst maintaining sidewall quality. **FIGURE 6** shows the SiC etch rate and selectivity trends with process pressure.

Table 2 summarises the process trends for the SiC Via etch tuning.

SEM cross sections for a 100µm deep SiC via etched using a two step optimized process stopping on the GaN underlayer are shown in **FIGURE 7**. The GaN loss has been measured to be <0.35µm for this process.

**FIGURE 8** shows the via base following GaN etching using a Cl<sub>2</sub>/BCl<sub>3</sub> chemistry in the same APS module. This process takes place after the Ni mask has been stripped and the via wet cleaned of polymer. Selective etching of the GaN to the Au metallisation is achieved.

End-point traces for the GaN etch are shown in **FIGURE 9**. The intensities of the Ga\* emissions at 417nm for 2 consecutive wafers show that the total etch times agree within 3 seconds.

The ability to clean the via of etch polymer using a 20% HNO<sub>3</sub> solution at room temperature for 15 minutes is shown in **FIGURE 10**. The trenching observed at the base of these partially etched vias is typical for an energetic process of this type. The trenching disappears when etching is continued to the GaN layer.

The substrate vias were then coated with a sputtered metal seed layer and electro-plated with Au metal resulting in a nominal via resistance slightly below 6E-3Ω.

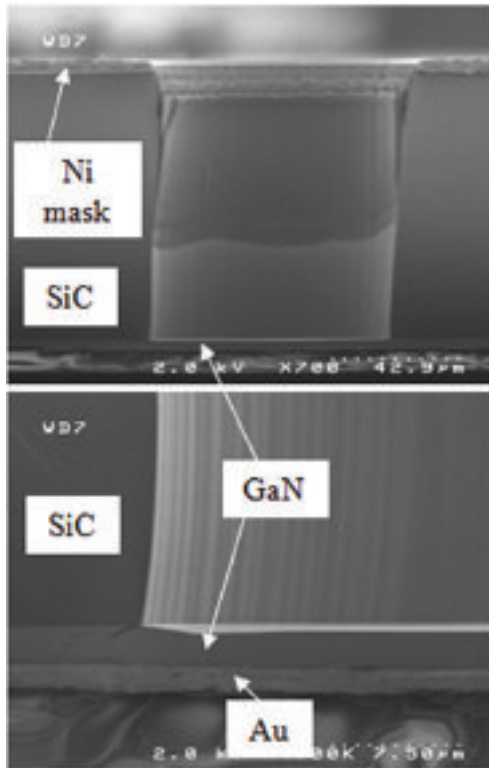


FIGURE 7.

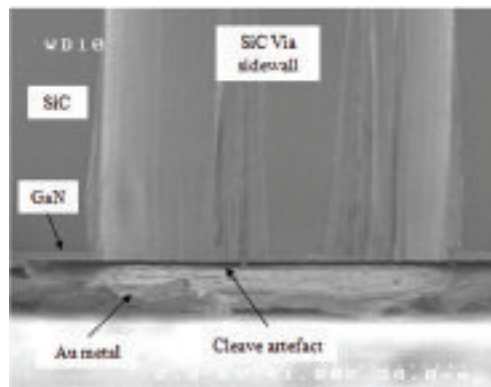


FIGURE 8.

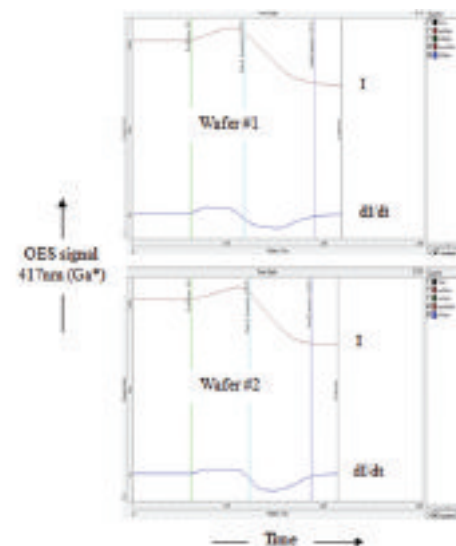


FIGURE 9.

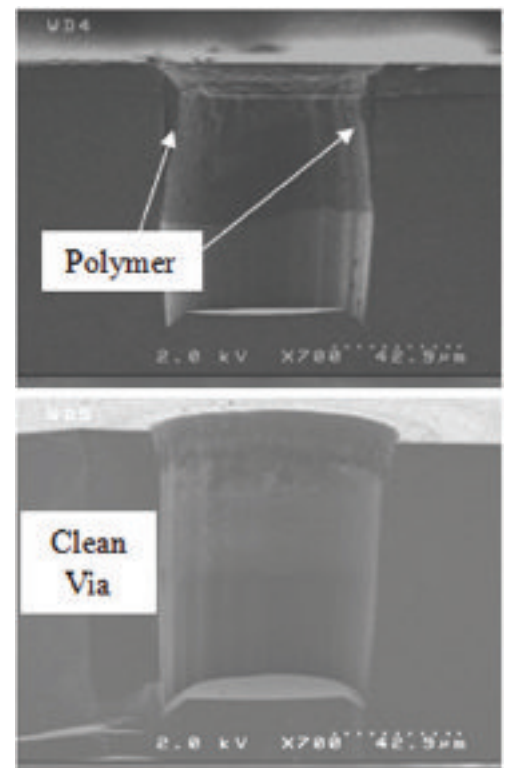


FIGURE 10.

## Conclusions

A manufacturable SiC back-side via process has been developed for high power device applications. Etch rates  $>1.3\mu\text{m}/\text{min}$  with cross-wafer uniformities of  $<\pm 5\%$  have been achieved along with Ni mask selectivity in the range 30-40:1. The use of a unique descum process has resulted in pillar defect levels  $<1\%$  and the vias are easily cleaned of polymer using  $\text{HNO}_3$  solutions. The same module hardware has been used to etch the GaN stopping on Au metal with automated end-point detection control. Via resistances  $<6\text{E}-3\Omega$  have been achieved.

## Acknowledgements

The authors would like to thank Tony Barrass and Brian Kiernan at SPTS for their help in designing and implementing the weighted clamp hardware for the APS module and all of the staff at WIN Semiconductors who supported the GaN technology development.

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# Applying leading-edge non-visual defect inspection to a mainstream 200mm fab

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**ROBERT NEWCOMB, BILL USRY** and **JOEL HICKSON**, Qcept Technologies, Atlanta, GA.

*Improving economic competitiveness through cost reduction, cycle time improvement and more eco-friendly processing.*

Leading-edge semiconductor device manufacturers utilize advanced inspection technologies to detect and reduce the impact of yield-critical defectivity issues. This is especially true during the development of a new technology node and the subsequent ramp to high-volume manufacturing. Traditionally, the defect inspection focus was on physical defects, but the proliferation of new materials, new processes and new device structures has resulted in the need to detect yield-critical non-visual defects (NVDs), including sub-monolayer residues and process-induced charging of dielectric films. Leading-edge fabs are utilizing a scanning probe system that detects changes in surface work function or charge build-up of a dielectric film to detect and reduce the impact of yield-critical NVDs [1-5].

There are numerous mainstream semiconductor fabs, including 200mm and trailing edge 300mm fabs that have established high yielding processes. Applying a leading-edge technology for NVD inspection to a mainstream fab would typically face a significant barrier to entry given their end of line (EOL) yields and the challenge of justifying higher cost new equipment

from a return on investment perspective. Mainstream fabs must therefore focus engineering resources on more than just yields in order to maintain the economic competitiveness of their products. They must also focus their efforts on cost reduction through lower materials usage, higher tool utilization through more optimized processes and fab capacity management through mix and match of equipment from different vendors. Additionally, the fabs look for more eco-friendly processes that reduce overall use and disposal of chemicals, deionized water and other effluents.

In this paper, we present data on how a 200mm mainstream analog fab achieved significant economic benefit from using an advanced ChemetriQ NVD inspection system manufactured by Qcept Technologies [6-7]. The highlighted case studies provided an annual savings of US \$3.0M per year – and a further US \$3.5M one-time savings in capital expenditures for a new wet process tool due to higher capacity with their existing tools.

## Reduced packaging costs

For certain devices, the analog process flow required the insertion of an additional back end of line (BEOL) process

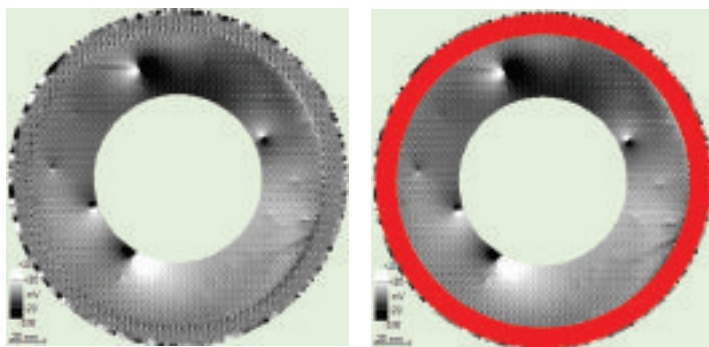
**COURTNEY HAZELTON** is a senior surface preparation engineer, **JOSH ROBERGE** is a senior product engineer, and **ALLEN PAGE** is a senior BEOL cleans and plasma etch engineer at Texas Instruments, email: c-hazelton1@ti.com

**ROBERT NEWCOMB** is an executive vice president, **BILL USRY** is a senior applications engineer, and **JOEL HICKSON** is product marketing manager at Qcept Technologies, Atlanta, GA, email: robert.newcomb@qceptech.com



Edge Residues (1a)

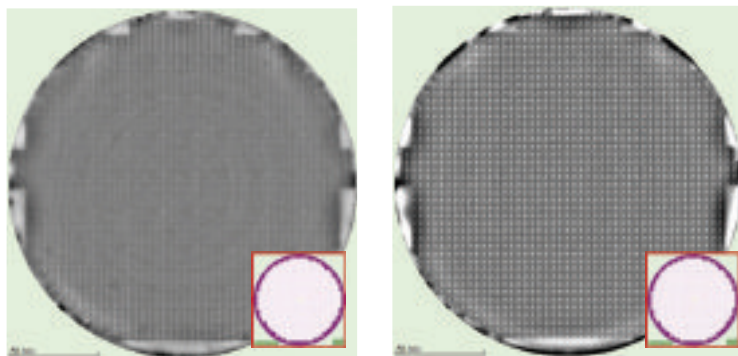
Defect Map (Bad Die) (1b)



**FIGURE 1.** NVD inspection results with (1a) highlighting the edge residue in the outer regions of the wafer; and (1b) automatically flagging this wafer as bad and providing feed forward data to ink mark the known bad die.

1st Lot

10th Lot



**FIGURE 2.** NVD inspection results show that the wafers from the 10th production lot using the IPA reuse process are residue free, and thus the new process has low risk for yield loss due to residues.

loop in order to deliver the requisite device capabilities. Based on EOL yield data and failure analysis, it was determined that this additional loop was leaving a thin edge residue that was not detectable by existing optical inspection tools. This residue affected 15% of lots in the production line. In addition to the sunk cost of assembling these defective die, the failure rate for the bad lots resulted in delayed revenue from the good die and higher incurred costs to perform extensive failure analysis to prove the yield loss was attributed to the edge residues and not a different reliability risk.

Fab engineers determined that the ChemetriQ NVD inspection tool was the only system capable of detecting the thin edge residue in the fab. An inline NVD inspection was subsequently implemented on 100% of production wafers after the plasma etch and clean process. **FIGURE 1A** provides an example of a bad wafer where the edge residue is detected in the

outer region of die. It was determined that this residue failure mode was isolated to die near the edge and so the inspection recipe was optimized for this specific NVD. In **FIGURE 1b**, threshold analysis was used to automatically flag wafers as bad if they had the edge residue, and the data enabled the fab to determine how far the residue encroaches into the wafer interior.

The inline inspection data from the NVD inspection tool was then used to feed forward the region with known bad die so that these die can be ink marked post fab and no longer packaged. Eliminating the packaging of known bad die has resulted in a recurring US \$900,000 per year savings. Additionally, the customer reject rate was reduced from 15% to 0% after implementing this new inline inspection protocol – resulting in an additional recurring savings of US \$900,000 by eliminating the need for failure analysis.

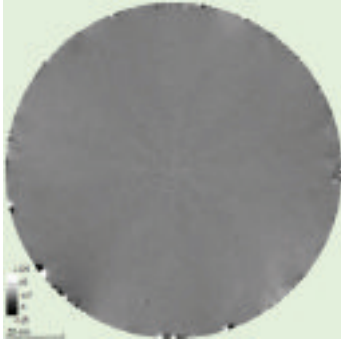
### Reduced Chemical Costs

The second use case involves a BEOL solvent clean process where the process of record used back-to-back isopropyl (IPA) baths where the IPA chemicals are changed after every ten production lots. Fab engineers had previously proposed a process change that would reduce IPA chemical usage by 50%, but the change was not approved because the fab lacked a method to detect non-visual residues that could have a negative impact on yield or even worse, result in reliability failures in the field.

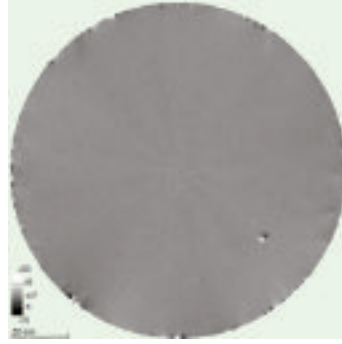
The proposed process change was re-evaluated with the ChemetriQ NVD inspection tool to demonstrate the process robustness and latitude. The new process reused IPA chemicals from the second (clean) bath to the first (dirty) bath resulting in each batch of IPA to be used for twenty production lots for a 50% reduction in chemical usage. **FIGURE 2** shows two residue free NVD inspection results for a wafer from the 1st production lot and 10th production lot while implementing the IPA reuse approach from the second bath to first bath.

The new process was implemented after this second study because the fab was confident that the new process would be robust based on the combination of the NVD inspection results, which showed that the wafers were residue free, with data such as particle checks and electrical split lot qualification. The 50% reduction in IPA usage for this back end of line solvent clean process resulted in US \$720,000 per year savings

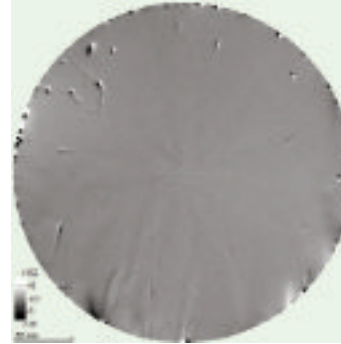
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Goal



Process Marginality



Standard Rinse Time (3a) 50% Reduced Rinse Time (3b) 90% Reduced Rinse Time (3c)

**FIGURE 3.** NVD inspection results for a rinse time reduction study indicate that the 90% reduced rinse time (in 3c) is incapable of efficiently removing the cleaning chemistries from the surface.

for this one process step.

### Higher throughput and more eco-friendly process

The final use case involves optimizing the process throughput for a FEOL RCA clean process by reducing the total deionized water (DIW) rinse time. The RCA process used a two-step final rinse with a Quick Dump Rinse (QDR) technique. The goal was to reduce the total rinse time by 50% from the process of record while ensuring that the shorter rinse was thorough enough to remove the clean chemistries without leaving residues.

The design of experiments for the proposed process change used multiple inspection tools and electrical qualifications, including NVD inspection, optical inspection, electrical gate oxide integrity (GOI) and

electrical EOL probe results. For the NVD inspection portion, wafers were processed through the two-step QDR tanks ranging from 10% to 100% of the standard rinse time using increments of 10%. The goal was to determine at which point the rinse time was no longer effectively removing the cleaning chemistry.

**FIGURE 3** shows the NVD inspection results for

three wafers from this study including the 100%, 50% and 10% splits. The results indicate that the efficacy of the 10% QDR split is very poor as a significant level of surface residues are detected on the wafer in **FIGURE 3C**. The 50% QDR split provided effective rinsing of the wafer, which was verified with numerous confirmation runs. Electrical qualification lots were run comparing the 100% QDR process to the 50% QDR process and both the GOI data and final probe data as shown in **FIGURE 4** showed good electrical performance for the proposed process.

The new 50% QDR rinse time process was approved, which resulted in numerous benefits for the fab,

PROJECT	INLINE INSPECTION	COST REDUCTION	ECO-FRIENDLY PROCESS	FAB CAPACITY & UTILIZATION	YIELD IMPROVEMENTS	BENEFIT STATEMENT	ANNUAL ECONOMIC BENEFIT
Edge Residue	✓	✓			✓	Reduced packaging costs; fewer customer rejects	\$1,800,000
IPA Reclaim		✓	✓			50% reduction in IPA use; lower costs, less effluent	\$ 720,000
ESC Charge				✓	✓	Resolved issue to enable tool qual for production	N.D.
Wet Hood Monitor	✓	✓			✓	Inline yield excursion monitor for wet bench	\$ 250,000
Litho Rework					✓	Resolved NVD yield issue at litho rework	\$ 500,000
DIW Rinse		✓	✓	✓		14M liter/year reduction in DIW; capital avoidance	\$ 3,500,000 capital avoidance

**TABLE 1.**

including (a) a 14,000,000 liter reduction in DIW usage for this one RCA clean process; (b) a 25% increase in the wafers per day throughput of the wet bench system; which in turn resulted in (c) the fab cancelling a planned \$3.5M expenditure for a new wet bench system because the existing tools could now meet the higher wafer start levels without the need of more tools.

## Summary

Table 1 summarizes the economic benefits achieved from the three case studies covered in this article as well as three other examples. These include (a) resolving a charge induced yield issue on a “new” used tool where the fab had to mix-and-match different tools from different vendors for the same process; (b) implementing an inline NVD inspection step to detect yield excursions due to ozone generator reliability issues and high water content in the process bath; and (c) optimizing a litho rework process to eliminate non-visual BARC residues that resulted in lower yields for lots that were reworked as compared to lots that were not reworked.

In summary, both 200mm and trailing edge 300mm mainstream fabs face many challenges, including how to improve their economic competitiveness. In this article we have presented use cases from a 200mm mainstream analog fab that utilized advanced NVD inspection technology to reduce costs, provide higher throughput for process tools and deliver more eco-friendly processing. The economic benefit of the use cases shown in Table 1 exceeds US \$3.0M per year of recurring savings plus a one time savings of US \$3.5M in capital.

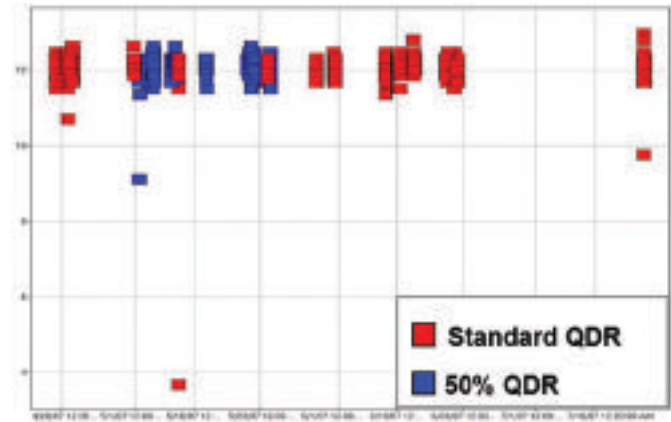
## Acknowledgements

This article is based on an oral presentation given at the 2013 SEMICON West TechXPOT Productivity Innovation track focused on reducing cost and improving performance at 200/300mm wafer fabs. ◀▶

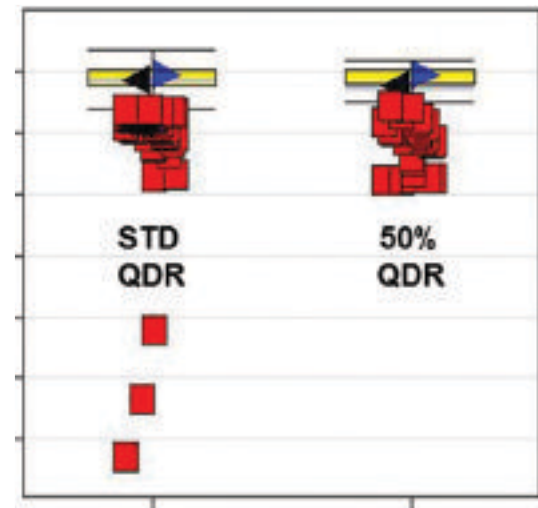
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## GOI Failures



## Final Probe



**FIGURE 4.** Electrical results for gate oxide integrity failures and EOL final probe data showing a favorable comparison between the 100% rinse time process versus the new 50% rinse time process.

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# A bilayer temporary bonding solution for 3D-IC TSV fabrication

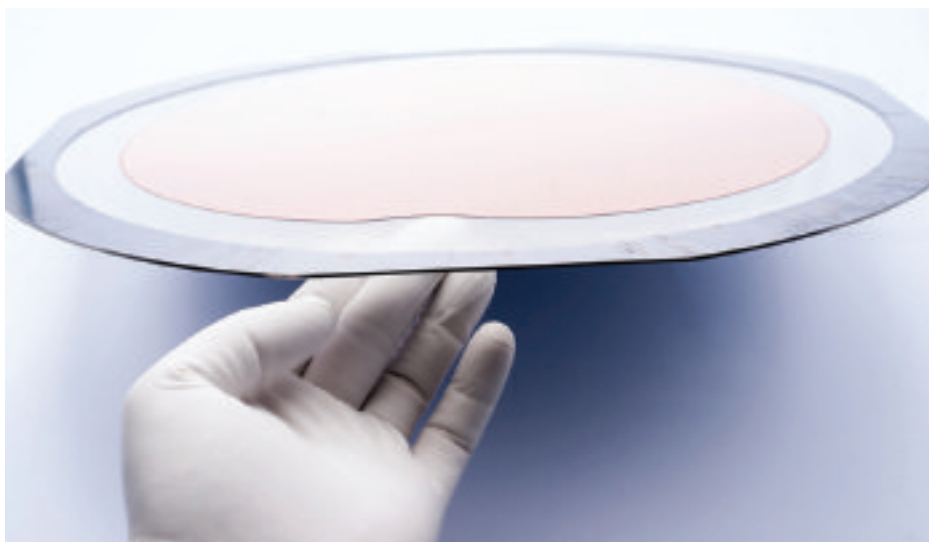
**ANDREW HO**, Global Industry Director, Advanced Semiconductor Materials, Dow Corning, Hong Kong.

*New technology eliminates the need for specialized equipment for wafer pre- or post-treatment.*

**A**dvances in three-dimensional (3D) through-silicon via (TSV) semiconductor technology promise to significantly improve the form factor, bandwidth and functionality of micro-electronic devices by enabling once-horizontal chip structures to be fabricated as vertical architectures. The challenges to implementing 3D-IC TSV integration are not trivial, and the search for a solution has prompted exploration of several schemes. These are frequently labeled as via-first, via-middle or via-last depending on the position where the 3D TSV fabrication takes place.

In via-first integration, TSVs are formed before processing the front-end-of the line (FEOL) layers, which enables high thermal budget processing for TSV insulation and filling. In via-middle schemes, TSVs are added between FEOL and back-end-of-the-line (BEOL) stacking to allow several copper-based interconnections. In a via-last approach, fabrication of TSVs occurs after completion of FEOL and BEOL processing, either from a wafer's front or back side. This approach generally addresses applications in which low density 3D interconnections are adequate.

In all these approaches, however, TSV fabrication is problematic without thinning the active silicon wafer down to 50µm or less (**FIGURE 1**) – about half the



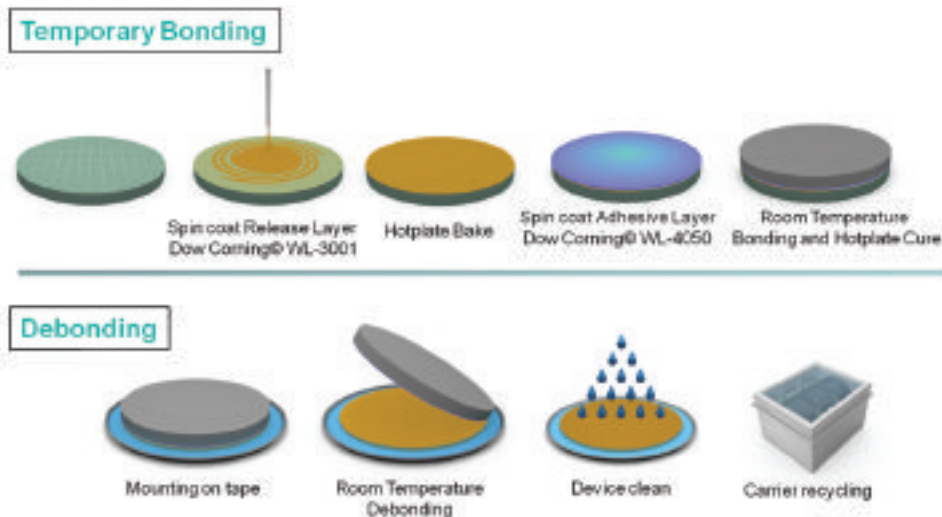
**FIGURE 1.** A thin silicon wafer on dicing frame after successful debonding from a silicon carrier wafer at imec, using Dow Corning's silicone-based temporary bonding solution. Image courtesy of and copyright owned by imec.

thickness of a standard piece of printer paper – and therein lies the challenge. In order to handle such ultra-thin wafers, the industry requires solutions that can easily, cost-effectively and temporarily bond and debond active wafers to carrier wafer systems for subsequent wafer thinning and TSV fabrication.

## Temporary bonding solutions: A primer

Wafer thinning is already widely applied for IC manufacturing, as well as the manufacture of power devices and image sensors. Depending on process requirements and applications, wafer bonding can be divided into several

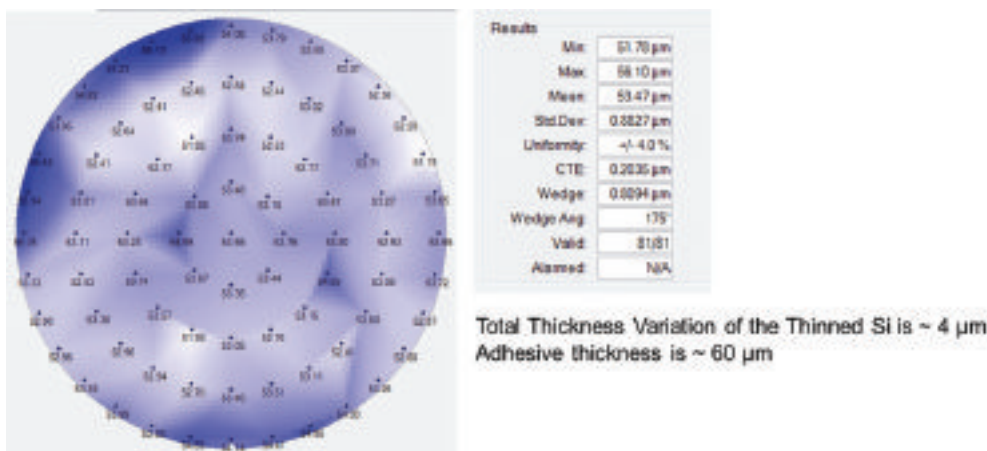
**ANDREW HO** is the Global Industry Director, Advanced Semiconductor Materials, Dow Corning. E-mail: Andrew.ho@dowcorning.com.



**FIGURE 2.** A typical process flow for temporary bonding and debonding solutions.

techniques including direct bonding, anodic bonding and thermo-compression adhesive bonding and others. For 3D-IC integration, however, the most commonly explored approach is attaching device wafers to a carrier wafer for support with the use of polymer-based temporary adhesives. As shown in **FIGURE 2** A typical process flow for the use of such temporary bonding solutions first applies a release and an adhesive layer, either on the device or the carrier wafer. After this the device and carrier wafers are bonded together. Subsequent steps, in sequence, involve wafer thinning, TSV reveal or fabrication, formation of redistribution layers and wafer interconnect fabrication, debonding and cleaning of the processed ultra-thin device wafer and, lastly, 3D stacking of the thinned device wafers.

Central to the success of this approach is the

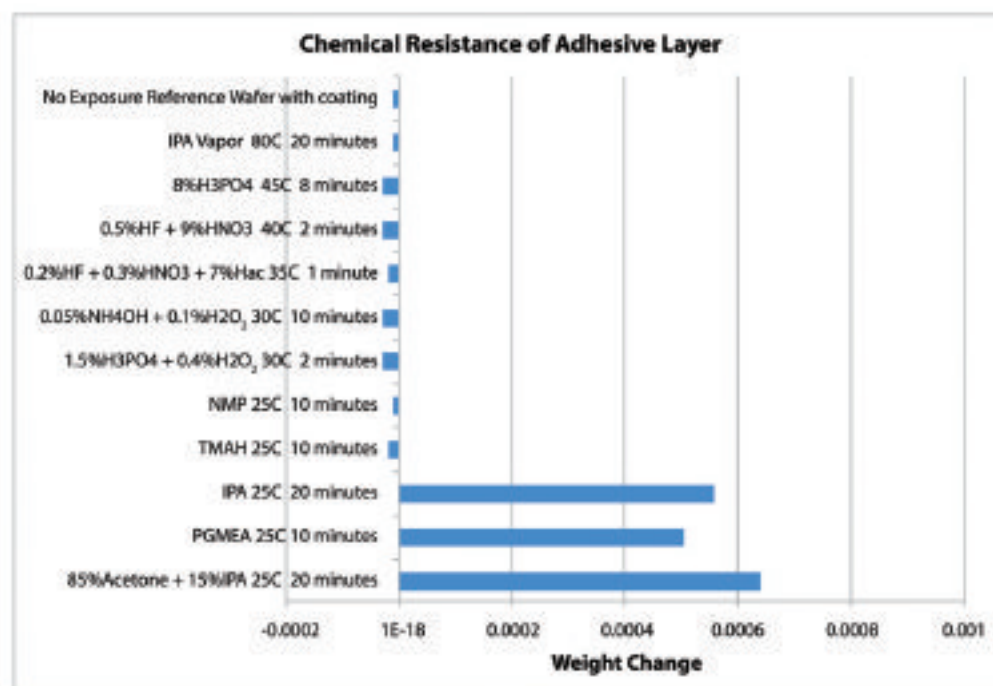


**FIGURE 3.** Measurements of a temporarily bonded active wafer (post-thinning) show total thickness variation to be approximately  $4 \mu\text{m}$ .

polymer adhesive, which must protect the ultra-thin wafer while withstanding the harsh chemicals and thermal stresses imposed by wafer thinning and 3D-IC TSV integration processes. Specifically, temporary bonding/debonding (TB/D) solutions must demonstrate excellent thermal and chemical stability to withstand the plasma processes as well as the solvents, bases and acids used by 3D-IC TSV processes. In addition to delivering excellent adhesive properties to withstand the mechanical stress of the wafer

thinning process, temporary adhesives must also be able to maintain global high uniformity of the adhesive layer as characterized by a low total thickness variation (TTV) across the device wafer through all processing steps to reach a typical target of  $2 \mu\text{m}$  TTV on the thin device wafer (**FIGURE 3**). In addition, these materials must enable low-temperature debonding compatible with different interconnect technologies using solder bumps or copper pillars, and offer a simple wafer cleaning process that will damage neither the underlying layers of the processed device wafer nor the tape on which the thinned wafer stands after debonding.

The potential of polymer-based TB/D solutions has prompted exploration of several material technologies coupled with various equipment platforms and wafer treatments. As development of these and other TB/D solutions advance, 3D-IC TSV integration has yet to become a mainstream technology due to its additional costs and challenges on thin wafer handling. These costs derive not only from the sophisticated materials used, but also the multiple pre-treatment steps that temporary bonding and debonding processes have traditionally required. While these painstaking steps help to ensure high yields and protect the high value of fully functional device



**FIGURE 4.** Wafers spin-coated with the temporary adhesive and then cured tested the material's chemical resistance by soaking it in phosphoric acid, nitric acid, organic solvents and other chemicals familiar to TSV fabrication. The temporary bonding material showed negligible weight loss or gain for all chosen chemicals.

wafers, they also hinder 3D-IC TSV integration from moving to volume production and, ultimately, they contribute to a higher total cost of ownership.

Minimizing total cost of ownership is essential for all semiconductor manufacturing applications. But it is a critical enabler for next-generation technologies, such as 3D-IC TSV integration. Recent innovations by Dow Corning and industry collaborators have shown promising development of a simpler, more cost-effective temporary bonding solution based on silicone adhesive and release layers. Importantly, this new solution enables room-temperature bonding and room-temperature mechanical debonding of active and carrier wafers using conventional, high-volume manufacturing methods.

### A new bilayer temporary bonding/debonding concept

At the center of this new approach is a simple bilayer concept based on two silicone materials that serve as the temporary bonding materials during the fabrication of thin wafers for 3D-IC TSV integration. It applies a process flow that greatly simplifies the temporary bonding/debonding process, and reduces costs associated with

special equipment for pre- or post-process treatments of the device wafer such as plasma, ultra-violet, preferential zone treatment and others.

The first step in the process flow is the spin coat of the temporary bonding materials. This step is critical to minimizing delays in process time, as the total thickness variation (TTV) of the spin coated material can contribute to the TTV of the bonded pair and, later, transfer to the thin wafer during the wafer thinning and post processing of bonded wafer pairs. Thus it is important to start with a low TTV for spin coated films. Notably, the process described here targets TTV for coatings on the device wafer to a range of within 1 percent.

The spin coat step first applies a continuous release layer onto the front side of the device wafer, ensuring the layer entirely covers any micro-structures present. Next, comes spin coat application of a silicone-based adhesive layer of a few tens of microns in thickness – depending on the device wafer's topography – on top of the release layer. The adhesive layer developed for this process is designed to obtain excellent uniformity and planarization over high bump topographies. It allows single-layer thicknesses between 10 and 110  $\mu\text{m}$  to provide process simplicity.

After application of both layers, the device and carrier wafer are bonded. The carrier wafer can be either silicon or glass, and it does not require any particular pre-processing. Prior to the bonding step, application of vacuum assures no air bubbles are trapped in the adhesive, which is viscous. After degassing, the carrier is dropped onto the device wafer.

Importantly, bonding occurs at room temperature, which greatly improves the opportunity for increased throughput. Also, the silicone-based adhesive is still in its wet state at this point. So, no force is required to bond the pair. Thus, this technology offers the



potential to accommodate fragile ultra-low dielectric constant materials used within advanced copper interconnects that are very sensitive to the application of force. The total time for this step takes a couple of minutes, followed by a post-bonding bake on a hotplate – typically at 150° C for a few more minutes – to cure the adhesive layer.

Wafer processing now proceeds with backgrinding and associated process control. Following post-bonding, the bonded pair is mechanically debonded at room temperature along the release to adhesive layer interface. The thinned device wafer remains on a tape on a frame, available for release layer cleaning followed by dicing, pick-and-place and stacking steps. The carrier wafer, still covered with adhesive, is processed for chemical recycling.

### **Able to withstand real-world processes**

Candidate TB/D materials must deliver excellent thermal stability to ensure that the bond remains strong during the various processing steps involved in the copper nail reveal step and formation of redistribution layers on the device wafer. It is also critical that candidate materials do not outgas during post-bond processing, as this can lead to voids or delamination that, ultimately, can contribute to device failures.

Thermal analysis of both the release and adhesive materials used in this new approach heated the thinned bonded pair to 200° C on a hot plate in air for 20 minutes; and then to 200° C in air for three hours, where it passed solder bump reflow conditions at 260° C for 10 minutes; and finally to 200° C for three hours under vacuum. Scanning acoustic microscopy analysis after each test showed no voids or delamination.

These results underscore that both TB/D materials developed for the approach described above can not only hold up under the rigors of conventional backgrinding processes, they can also deliver the thermal stability necessary to withstand the plasma processes applied to the wafer pair during the fabrication of 3D-IC TSV architectures.

Strong chemical resistance is also critical for candidate TB/D materials to ensure they can perform reliably without delaminating or swelling when exposed to the several wet processes that thinned wafers undergo. Testing of the release and adhesive

layer materials began by spin coating a wafer with the temporary adhesive, curing it using described protocols and then soaking it in phosphoric acid, nitric acid, organic solvents and other chemicals familiar to TSV fabrication. The temporary bonding material showed negligible weight loss or gain for all chosen chemicals (**FIGURE 4**).

One of the most important enablers of broader adoption of TB/D solutions is the ability to debond thinned device wafers from carrier wafers, and clean any residues from the device wafer without adversely affecting device yields. The new bilayer TB/D concept described above leverages a room-temperature peel debond, and has been demonstrated on several conventional, commercially available debonding platforms from leading equipment providers.

The process begins by first mounting the thinned wafer pair onto a dicing tape and holding it in place on a vacuum chuck while peeling off the thick carrier wafer. Because the solvent dissolvable release layer is applied to the thin device wafer with dicing tape exposed, no harsh silicone removers or other strong acids need be applied. The entire debond process takes less than five minutes, including clean-up of the device wafer.

### **Conclusion**

While TB/D materials and equipment continue to evolve in sophistication, broader adoption of this technology and the 3D-IC TSV integration that it enables cannot advance at the expense of simple processing, device yields or total cost of ownership. The emergence of Dow Corning's simple, bilayer TB/D bonding solution achieves all these goals by eliminating the need for specialized equipment for wafer pre- or post-treatment.

Comprising an adhesive and release layer, the technology has demonstrated excellent spin coating and room temperature bonding performance with low TTV, even for very thick layers up to 110 µm. Proven on commercially available high-volume production equipment, it has shown excellent chemical stability when exposed to phosphoric acid, nitric acid, organic solvents and other chemicals familiar to TSV fabrication. In addition, the bonding solution and paired wafers showed good thermal stability when exposed to the 300° C temperatures common to post-bonding 3D TSV processes. ♦

# Design for yield trends

**SARA VER-BURGGEN**, contributing editor, SemiMD

*Should foundries establish and share best practices to manage sub-nanometer effects to improve yield and also manufacturability?*

**D**esign for yield (DFY) has been referred to previously on this site as the gap between what the designers assume they need in order to guarantee a reliable design and what the manufacturer or foundry thinks they need from the designer to be able to manufacture the product in a reliable fashion. Achieving and managing this two-way flow of information becomes more challenging as devices in high volume manufacturing have 28 nm dimensions and the focus is on even smaller dimension next-generation technologies. So is the onus on the foundries to implement DFY and establish and share best practices and techniques to manage sub-nanometer effects to improve yield and also manufacturability?

‘Certainly it is in the vital interest of foundries to do what it takes to enable their customers to be successful,’ says Mentor Graphics’ Technology Communications Manager, Gene Forte, adding, ‘Since success requires addressing co-optimization issues during the design phase, they must reach out to all the ecosystem players that enable their customers.’

Mentor refers to the trend of DFY moving closer to the manufacturing/foundry side as ‘design-manufacturing co-optimization’, which entails improving the design both to achieve higher yield and to increase the performance of the devices that can be achieved for a given process.

But foundries can’t do it alone. ‘The electronic design automation (EDA) providers, especially ones that enable the critical customer-to-foundry interface, have a vital part in transferring knowledge and automating the co-optimization process,’ says Forte. IP suppliers must also have a greater appreciation for and involvement in co-optimization issues so their IP will implement the needed design

enhancements required to achieve successful manufacturing in the context of a full chip design.

As they own the framework of DFY solutions, foundries that will work effectively with both the fabless and the equipment vendors will benefit from getting more tailored DFY solutions that can lead to shorter time-to-yield, says Amiad Conley, Applied Materials’ Technical Marketing Manager, Process Diagnostics and Control. But according to Ya-Chieh Lai, Engineering Director, Silicon and Signoff Verification, at Cadence, the onus and responsibility is on the entire ecosystem to establish and share best practices and techniques. ‘We will only achieve advanced nodes through a partnership between foundries, EDA, and the design community,’ says Ya-Chieh.

But whereas foundries are still taking the lead when it comes to design for manufacturability (DFM), for DFY the designer is intimately involved so he is able to account for optimal trade-off in yield versus PPA that result in choices for specific design parameters, including transistor widths and lengths.

For DFM, foundries are driving design database adjustments required to make a particular design manufacturable with good yield. ‘DFM modifications to a design database often happen at the end of a designer’s task. DFM takes the “ideal” design database and manipulates it to account for the manufacturing process,’ explains Dr. Bruce McGaughy, Chief Technology Officer and Senior Vice President of Engineering at ProPlus Design Solutions.

The design database that a designer delivers must have DFY considerations to be able to yield. ‘The practices and techniques used by different design teams based on heuristics related to their specific application are therefore less centralized. Foundries recommend DFY

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**SARA VER-BURGGEN** is a contributing editor for Semiconductor Manufacturing and Design, [www.semimd.com](http://www.semimd.com).

reference flows but these are only guidelines. DFY practices and techniques are often deeply ingrained within a design team and can be considered a core competence and, with time, a key requirement,' says McGaughy.

### In the spirit of collaboration

Ultimately, as the industry continues to progress requiring manufacturing solutions that increasingly tailored and more and more device specific, this requires earlier and deeper collaboration between equipment vendors and foundry customers in defining and developing the tailored solutions that will maximize the performance of equipment in the fab. 'It will also potentially require more three-way collaboration between the designers from fabless companies, foundries, and equipment vendors with the appropriate IP protection,' says Conley.

A collaborative and open approach between the designer and the foundry is critical and beneficial for many reasons. 'Designers are under tight pressures schedule-wise and any new steps in the design flow will be under intense scrutiny. The advantages of any additional steps must be very clear in terms of the improvement in yield and manufacturability and these additional steps must be in a form that designers can act on,' says Ya-Chieh. The recent trend towards putting DFM/DFY directly into the design flow is a good example of this. 'Instead of purely a sign-off step, DFM/DFY is accounted for in the router during place and route. The router is able to find and fix hotspots during design and, critically, to account for DFM/DFY issues during timing closure,' he says. Similarly, Ya-Chieh refers to DFM/DFY flows that are now in place for custom design and library analysis. 'Cases of poor transistor matching due to DFM/DFY issues can be flagged along with corresponding fixing guidelines. In terms of library analysis, standard cells that exhibit too much variability can be systematically identified and the cost associated with using such a cell can be explicitly accounted for (or that cell removed entirely).'

'The ability to do "design-manufacturing co-optimization" is dependent on the quality of information available and an effective feedback loop that involves all the stakeholders in the entire supply chain: design customers, IP suppliers, foundries, EDA suppliers, test vendors, and so on,' says Forte. 'This starts with test chips built during process development, but it must continue through risk manufacturing, early adopter experiences

and volume production ramping. This means sharing design data, process data, test failure diagnosis data and field failure data,' he adds.

A pioneer of this type of collaboration was the Common Platform Consortium initiated by IBM. Over time, foundries have assumed more of the load for enabling and coordinating the ecosystem. 'GLOBALFOUNDRIES has identified collaboration as a key factor in its overall success since its inception and been particularly open about sharing foundry process data,' says Forte.

TSMC has also been a leader in establishing a well-defined program among ecosystem players, starting with the design tool reference flows it established over a decade ago. Through its Open Innovation Platform program TSMC is helping to drive compatibility among design tools and provides interfaces from its core analysis engines and third party EDA providers.

In terms of standards Si2 organizes industry stakeholders to drive adoption of collaborative technology for silicon design integration and improved IC design capability. Forte adds: 'Si2 working groups define and ratify standards related to design rule definitions, DFM specifications, design database facilities and process design kits.'

Open and trusting collaboration helps understand the thriving ecosystem programs that top-tier foundries have put together. McGaughy says: 'Foundry customers, EDA and IP partners closely align during early process development and integration of tools into workable flows. One clear example is the rollout of a new process technology. From early in the process lifecycle, foundries release 0.x versions of their PDK. Customers and partners expend significant amounts of time, effort and resources to ensure the design ecosystem is ready when the process is, so that design tapeouts can start as soon as possible.'

DFY is even more critically involved in this ramp-up phase, as only when there is confidence in hitting yield targets will a process volume ramp follow. 'As DFY directly ties into the foundation SPICE models, every new update in PDK means a new characterization or validation step. Only a close and sustained relationship can make the development and release of DFY methodologies a success,' he states. ♦



# Synthetic diamond's role in thermal management

**ADRIAN S. WILSON,** Element Six Technologies Ltd., Berkshire, U.K.

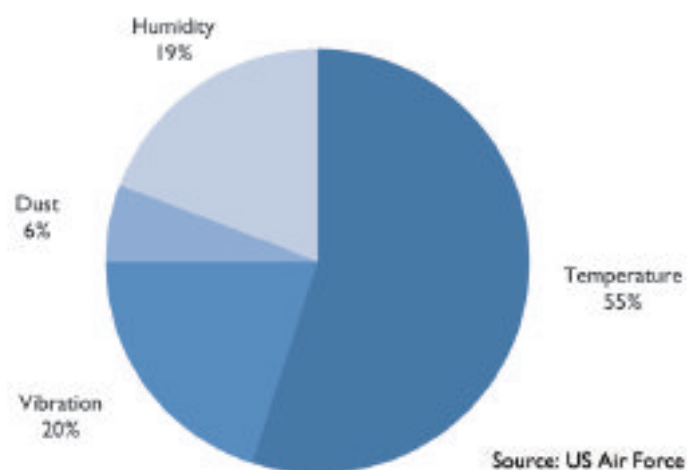
*Synthetic diamond is ideally suited for thermal management of semiconductor packaging, as it combines exceptionally high thermal conductivity with electrical isolation.*

Studies have shown that when it comes to the reliability of packaged chips, most failure processes follow a temperature dependent behavior. Every 10°C of increase in junction temperature represents a 2x decrease in device lifetime. In fact, more than half of failures in today's electronic systems are due to temperature (**FIGURE 1**).

This thermal challenge is at the forefront of package designers' minds as they struggle to design packages to meet today's thermal requirements. What's more, this trend is only going to get worse.

Device power densities are on a trajectory to be well above 100 W/cm<sup>2</sup> at 14 nm (according to the ITRS Roadmap). When combined with the need for higher power solid state switching devices for power converters and high frequency components for military, cellular, and satellite communications, the need to manage higher power densities and the associated heat is an issue spanning all major segments of the industry.

Higher thermal conductivity materials are being explored to provide better heat extraction as compared to incumbent materials such as copper. Synthetic diamond is ideally suited for thermal management of semiconductor packaging, especially for today's advanced electronic systems driving towards higher and higher power density, as it combines exceptionally high thermal conductivity with electrical isolation. Diamond's thermal conductivity at room temperature is an amazing five times that of copper. In addition,



**FIGURE 1.** Failure modes in electronic systems.

for mobile and aerospace applications, diamond has the advantage of low density (3.52 g/cm<sup>3</sup>), which combined with its high thermal conductivity, enables small heat spreader dimensions for a very low-weight thermal management solution. For rugged applications, the high Young's modulus of diamond (1000 to 1100 GPa) helps increase the reliability of the entire package or module.

## Industry adoption

Widespread industry adoption of diamond in IC packaging has been slow, however some sectors are recognizing its benefits. It is being effectively integrated into packages for high power, LED and RF devices. However, the economics of diamond synthesis only really work if you can create high quality, thick

**ADRIAN S. WILSON** is the Head of Technologies Division, Element Six Technologies Ltd., Berkshire, U.K.



**FIGURE 2.** CVD synthetic diamond wafer, up to 140 mm in diameter and 3 mm in thickness.

diamond plates in high volume, which has only been achievable in the last 5-10 years. New materials to the semiconductor industry take anywhere from 5-15 years to be adopted. Synthetic diamond is now moving from the “early adopter” stage to the “early majority” stage of its lifecycle, yet further awareness is critical to fully transition through the product lifecycle model to full-scale use.

Addressing the criteria above, synthetic diamond, by way of microwave chemical vapor deposition (CVD) delivers:

- **High quality:** High quality is relevant since the method of heat transfer within diamond is by lattice vibration, i.e. the transport of phonons. Any material impurities will hinder this lattice vibration and thus reduce the thermal conductivity. Synthetic diamond manufacturers understand this need and have patented such methods as using a microwave source that creates high energy atomic hydrogen which strips away impurities in synthetic diamond during growth.
- **Thick diamond plates:** Thermal conductivity is a three dimensional problem. As such the diamond needs to be of sufficient thickness to rapidly dissipate localized semiconductor heat spots and optimally transfer the heat effectively from the semiconductor to the heat sink. Microwave-assisted CVD is a scalable technology which deposits

diamond over large areas and thicknesses (**FIGURE 2**) at a cost similar to semi-insulating SiC wafers.

- **High volume:** With an uptick in adoption, more manufacturers will look to expand capacity, as some have already done. Expanded capacity enables the industry to synthesize diamond at the appropriate scale to meet the price points required for both high power and RF device packages.

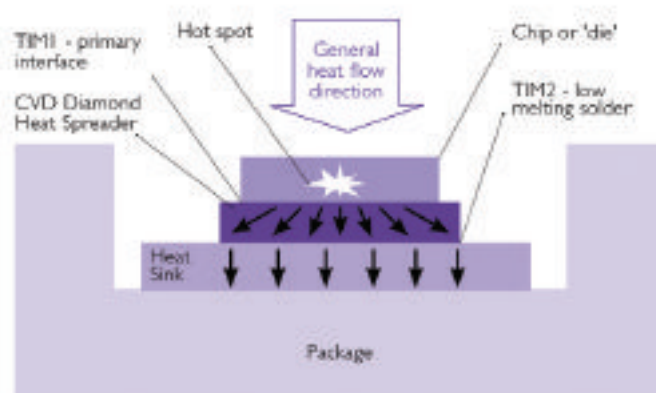
### Integrating Synthetic Diamond in IC Design

Thermal conductivity alone is not the whole story. The effectiveness of CVD diamond as a heat spreader in electronic packages depends very much on how it is integrated into the module.

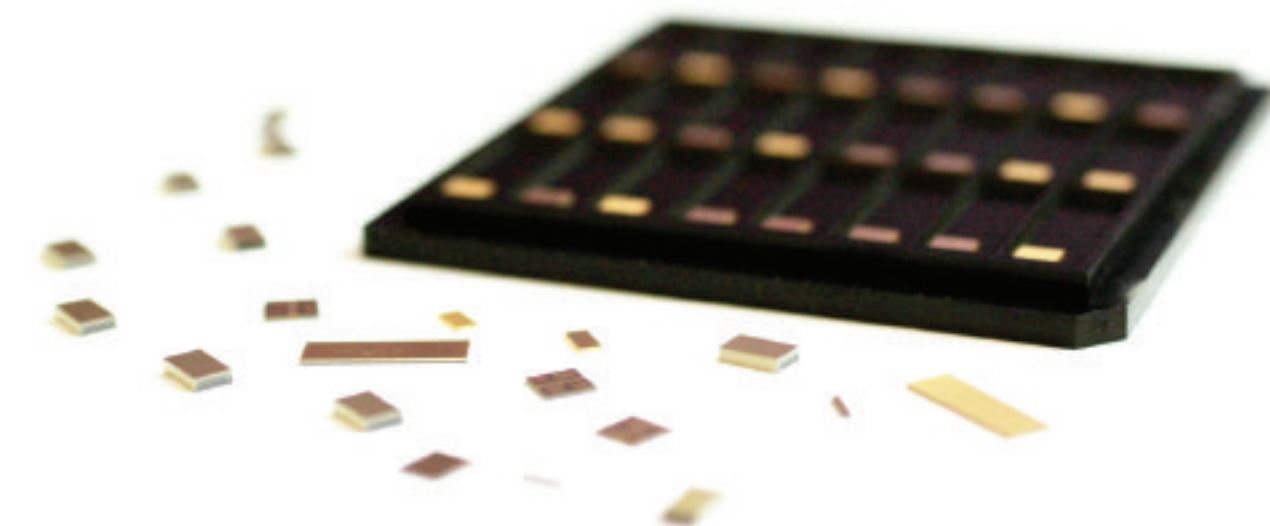
To optimize the thermal-management solution, engineers must consider carefully how the die and heat spreader will be attached, device operating requirements, the dimensions and surface conditions of the heat spreader, thermal expansions mismatch, and cost.

- **Die attach requirements:** thermal barrier resistance of the TIM1 interface (**FIGURE 3**) between the die and heat spreader must be minimized to optimize diamond heat spreader effectiveness. A metallic bond to the die, such as a solder joint, typically creates the least thermal barrier

### TYPICAL PACKAGE GEOMETRY WITH CVD DIAMOND MOUNTED IN MODULE



**FIGURE 3.** Diagram of heat spreader in LED package.



resistance. Because diamond is a chemically inert material, carbide forming materials must be used to metalize diamond with sufficient adhesion. A commonly used metalization scheme of Ti/Pt/Au ensures carbide formation at the Ti/diamond interface to achieve the best results.

- **Device requirements:** a heat spreader can be electrically conductive or insulating, and both options are possible using CVD diamond. The diamond itself is electrically insulating, but can be made conductive by means of covering the side faces with metals or laser drilling vias, with metal fillings, through the diamond.
- **Heat spreader characteristics:** apart from choosing the grade of diamond to be used (from 1000 to 2000W/mK), the size of the heat spreader must also be determined. Heat spreaders are typically sized 50-100  $\mu\text{m}$  longer than the die in each lateral dimension to ensure good solder fillets. Typical spreader thickness varies from 350 to 400  $\mu\text{m}$  for a wide range of devices (FIGURE 4).

### The Future for synthetic diamond

The combination of the semiconductor industry roadmap for increasing power densities and the increasing availability and affordability of synthetic diamond will result in a rapid increase in the adoption of this engineering material.

Synthetic diamond will be used with a broad range of semiconducting materials, such as SiC, GaAs and GaN.

As adoption increases, so will the desire to optimize TIM1 – the primary interface between die and diamond. No doubt new interface materials will be explored and potentially direct methods of bonding. In fact, making

diamond heat spreaders easy to integrate into semiconductor packages and modules, through the implementation of standard package components for instance, will be a key element to the industries increasing adoption of this thermal management solution.

To this end, synthetic diamond manufacturers such as Element Six, in combination with its acquisition of the assets and IP of Group4 Labs, is bringing a GaN-on-diamond substrate to market. This substrate provides a highly optimized TIM1 interface and is already in use by U.S. defense contractors, and such early adopters indicate an increase in its use for the defense sector. Synthetic diamond technology will also reach into telecom infrastructure applications such as satellite communications and mobile base stations. For these applications, synthetic diamond enables higher power density, thus lowering system costs or increasing performance, and allows operation in hotter ambient environments, thus lowering cooling costs and/or increasing lifetimes.

The unique combination of properties synthetic diamond possesses makes it one of the most exciting supermaterials in the world. In a few years, perhaps diamond will become the semiconductor material itself for applications requiring extremely high breakdown voltages. The list of applications for synthetic diamond is only expected to grow, making synthetic diamond manufacturers well-positioned to collaborate with industry partners to ensure future innovative applications for the material. ♦



## Non-contact lithography system

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**EV Group**, St. Florian, Austria, [www.evgroup.com](http://www.evgroup.com).

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**Dow Corning**, Midland, MI, <http://www.dowcorning.com/content/etronics/>

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**Multitest**, Rosenheim, Germany, [www.multitest.com](http://www.multitest.com).

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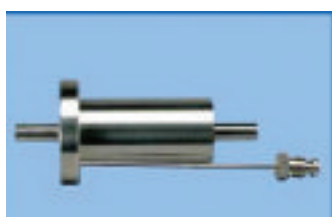


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## Green manufacturing: What you need to know

Green is the color for the decade and future decades as each country is developing its own standards for energy consumption and implementing its green initiatives. At one time considered a passing trend, green initiatives are now mandatory and force manufacturers to not only maintain corporate responsibility, but to positively impact the bottom line. As a result, high-volume manufacturers must work with vendors and suppliers that will help enable their overall cost and green manufacturing goals. Tracking and managing total operational costs is critical for sustaining a cost-effective, high-volume manufacturing (HVM) environment. Effective partners are already engaged in and developing systems on 'green' platforms using technology and services that balance performance with environmental impact, all within the barriers of cost. It includes companies that are designing systems using innovative techniques and new technologies that not only reduce the cost of energy, but also look at ways to reduce the cost of consumables, and the cost of downtime for HVM. By taking a total cost-of-operation approach when considering vendors and suppliers in a green manufacturing strategy, the resulting energy and environmental improvements can significantly lower fab operating costs.



**TATSUO ENAMI**  
Executive Officer &  
General Manager of  
Sales, Gigaphoton, Inc.

When considering light sources, the power consumption of excimer lasers will continue to increase, as high-power lasers grow in demand especially for 450-mm processes, it has increased 4.5x over the past 6 years. As these processes gear up for HVM, the environmental impact cannot be ignored. The estimated cost for utilities for lasers, which includes electricity consumption, gas consumption and heat management, will be approximately 30% of the total cost-of-operation. Clearly, reducing utility costs is critical. As a result, the true value of a laser for HVM weighs heavily on its effectiveness in controlling utility costs. To address this issue, several companies are working to find solutions. Gigaphoton is currently developing a new hybrid laser system that utilizes a solid-state laser chamber. This system will require a maximum power of only 36kW compared to 60kW on the current system. When considering costs, the use of a hybrid laser system for HVM can result in approximately 40% less overall power consumption from the laser system alone. As there are others in development by other companies, this is an example of one solution that is in development to reduce energy and help enable HVM.

Energy and environmental improvements can significantly lower fab operating costs.

Keep in mind, a successful partner in your green manufacturing strategy will develop wider technology solutions that also include reducing the cost of consumables and the cost of downtime. Companies that have invested time and considerable resources to develop eco-friendly systems will provide the most effective all-around solutions. For example, to further reduce the overall cost-of-operation and maintenance, determine if your potential partner has a roadmap to develop longer-life consumables, or develop a system that removes some of the consumables all together. In the case with hybrid lasers, this would be the Line-Narrowing Module (LNM) and the Enhanced Front Mirror (EFM). Gas is another consumable that also affects downtime. New techniques for system optimization have been developed that reduce the amount of gas needed by 50% and minimize the down time for maintenance by half compared to existing laser systems.

There are many companies that are working to provide 'green' solutions for its customer. Gigaphoton has been leading the 'green' concept since 2007. By working with our customers to identify technology, performance and cost models for HVM, Gigaphoton has developed the EcoPhoton program. When considering a green manufacturing strategy for HVM, to significantly reduce the overall cost-of-operation partner companies need to provide solutions that reduce energy consumption, and also a roadmap to develop longer-life consumables, gas modules with less volume and refill requirements, all of which contribute to minimizing down time for maintenance. The right partner can make the environment greener as well as your bottom line. ◀

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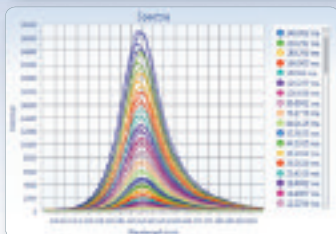
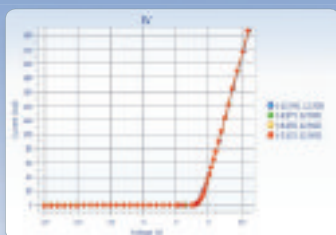


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