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Wafer stage at load position of an Ultratech LSA201 laser spike anneal system with ambient control.

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The ConFab 2015: Time for Collaboration

The future of the semiconductor industry continues to shine brightly. Smart phones have become an everyday part of life the world over, and we will soon see a new explosion of demand brought about by the "internet of things," cloud computing, digital television, biomedical sensors and many other types of advance electronics. Many believe this capability is leading to the 4th industrial revolution.

> "The goal of The ConFab is to spark discussions"

The semiconductor industry's ability to pack more and more functionality onto a single chip, many challenges remain. Some argue that we will soon reach the end of the road defined by Moore's Law, pointing to higher costs per transistor. More complex device structures, such as the FinFET and Vertical NAND, have become mainstream, 3D integration with TSVs continue to make slow progress, and a wide variety of new materials are being put into play. The IoT could drive the need for low power, low cost and high levels of integration of diverse components.

The path forward is far from clear. But what is clear is that the need for collaboration has never been greater. That's what The ConFab 2015 is all about. We bring together executives from all parts of the supply chain for three days of thought provoking talks and panel discussions, networking events and in-depth, pre-arranged meetings. In 2015, we'll be back at The Encore at The Wynn in Las Vegas, May 19-22. See www.theconfab.com for more information.

The goal of The ConFab is to spark discussions that will lead to faster resolution of problems, faster and broader industry expansion, and long-term collaborations among organizations of all types. In other words, our goal is to help The ConFab attendees "connect, collaborate and create"

Whenever we get together at The ConFab – which is now in its 11th year – I'm always reminded of a quote by Margaret Mead, "Never doubt that a small group of thoughtful, committed citizens can change the world; indeed, it's the only thing that ever has." Join as at The ConFab 2015 and you, too, can change the world.

—Pete Singer, Editor-in-Chief

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Technifab Keeps Cold Liquids Colder

Technifab specializes in the storage, transfer, and control of cryogenic fluids. Technifab designs, builds and installs cryogenic liquid systems along with providing the assistance customers need to make a cryogenic delivery system work. Cryogenic liquids used in Technifab equipment include liquid nitrogen, helium, hydrogen, oxygen, CO_2, LNG and others.

Technifab's products have been used throughout the semiconductor manufacturing and testing industry. Cryogenic liquids can remove heat from the manufacturing processes and also may be used to purge unwanted gases or create inert environments in critical process areas. Another common use is with environmental chambers, which often use liquid nitrogen to achieve and maintain desired temperatures. Recirculating chillers can use Technifab lines to circulate their cold fluids.

Although cryogenic delivery system installation and design are a key service provided by Technifab, they began as a manufacturing firm and still produce their own products today.

Technifab's product line includes:

Techflex Transfer Hoses

Durable, efficient, and maintenance free, Techflex transfer hoses deliver liquid quicker. The outer surface remains at room temperature and is safe to touch with bare hands.

Techniguard Vacuum Jacketed Pipe

Lower cryogenic liquid losses, more consistent liquid flow, and a significant lifetime savings occur with Techniguard vacuum insulated pipe. Technifab's bayonet connections between pipe sections simplifies installation and allows easier assembly - even reconfiguration. Vacuum jacketing significantly lowers heat transfer giving a significant reduction, often elimination, of the dripping and sweating, along with improved durability versus other forms of cryogenic insulation.

Techflow Cryogenic Valves

Technifab makes vacuum insulated pipe and tube size valves from 1/2" to 2" IPS with and without actuators. Designed for solid closure at cryogenic temperatures, vacuum insulation reduces heat ingress and can reduce valve cavitation. They also offer standard unjacketed cryogenic valves.

Liquid Helium Equipment

Technifab makes a variety of standard and custom equipment for ultra cold helium. From manifolds to specialty hoses and helium stingers, their helium equipment outperforms the competition in independent testing.

Custom and Laboratory Dewars

Technifab manufactures vacuum insulated dewars for many varied applications. Technifab dewars are used in labs for liquid nitrogen. Other custom OEM applications for low noise electromagnet sensors and delivering medical vaccines include remote African villages.

Liquid Nitrogen Phase Separators

Phase separators provide saturated, lower temperature liquid nitrogen with lower gas content and more consistent temperatures. Technifab offers four different models to meet customer application needs.

Technifab has grown from its inception in 1992 to an operation with global distribution. Since moving to the existing Indiana location in 1995, the building has been expanded four times to meet customer needs. The California regional office was added in 2010 and a third facility in Houston, Texas was added in 2013. A separate division and new facility, Exactifab, was opened in 2014 in response to the demand for precision machining that other firms found challenging to meet.

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Web Exclusives

Air gaps in copper interconnects for logic

The good people at ChipWorks have released some of the first public data on Intel's new 14nm-node process, and the results indicate that materials limitations in on-chip electrical interconnects are adding costs. Additional levels of metal have been added, and complex "air-gap" structures have been added to the dielectric stack. Flash memory chips have already used air-gaps, and IBM has already used a subtractive variant of air-gaps with >10 levels of metal for microprocessor manufacturing, but this is the first known use of additive air-gaps for logic after Intel announced that a fully-integrated process was ready for 22nm-node chips. (From SemiMD, part of the Solid State Technology network)

http://bit.ly/10b67Wa

RF and MEMS technologies enable the IoT

The "Internet of Things" (IoT) has been seen as the next major market that will demand high volumes of integrated circuits (IC). The IoT can be loosely defined as a network of small, low-cost, ubiquitous electronic devices where sensing data and communicating information occurs without direct human intervention. Each device would function as a "smart node" in the network by doing some low-level signal processing to filter signals from noise, and to reduce the bandwidth needed for node-to-node communications. The nodes will need to communicate up to some manner of a "cloud" for secure memory storage and to bounce actionable information down to humans. (From SemiMD, part of the Solid State Technology network)

http://bit.ly/1wBU4hj

Insights from the Leading Edge: STATS acquisition, Will SLIT replace TSV?

Contributing Editor Dr. Phil Garrou discusses acquisition rumors and presentations from the 2014 IMAPS Packaging meeting in this edition of Insights from the Leading Edge.

http://bit.ly/10P62ZI

n&b news and blogs

China's LED fabs to install more than 1,000 MOCVD tools from 2014 to 2018

SEMI China believes that the general lighting market will replace the LCD TV backlight market as the largest application market for LEDs in 2014, and general lighting market will continue to drive the LED industry over the next several years.

http://bit.ly/1zATu63

Intel's 14nm parts are finally here!

Dick James, senior analyst at Chipworks, deconstructs Intel 14nm parts in this edition of Chipworks' blog. Chipworks' analysis is ongoing, and the blog provides some excellent images.

http://bit.ly/1nWQNaH

Pittsburgh IMAPS Workshop

Packaging means a lot of different things to a lot of different people. Webster's dictionary defines package as a "group or a number of things, boxed and offered as a unit." But if you are in the microelectronics/MEMS industry, when you hear the word packaging your mind goes to the various MEMS packages that can contain a multitude of electrical and mechanical components that are inter-connected to the outside world for devices such as MEMS microphones, airbag accelerometers, gyros, RF MEMS and the list just goes on and on.

http://bit.ly/115lXBf

IMAPS Award Winners for 2014

At the IMAPS (International Microelectronics & Packaging Society) meeting in October, several of their key annual awards were given out.

http://bit.ly/1sN69KN

SACHEM
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SACHEM Reveals Innovations in IGZO and TSV Reveal Processing

SACHEM is a global chemical science company specializing in designing and manufacturing ultrapure chemistries for the microelectronics manufacturing industries.

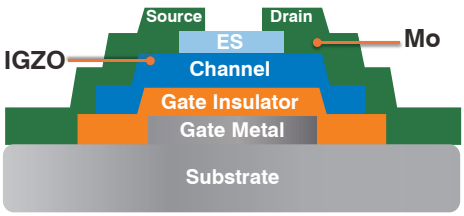
SACHEM is a leading supplier of high purity chemicals used in photoresist developers, selective etchants, wafer cleaners and chemical strippers for applications in Integrated Circuit, Advanced Packaging, Flat Panel Display and Printed Wiring Board manufacturing.

Development of these products requires collaboration with both formulators and end-users. From this process we often discover innovative solutions and make them directly available to our customers.

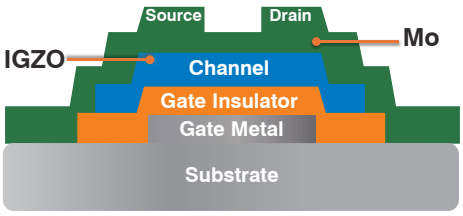
IGZO Processing Solution

In recent months, SACHEM technologists released a new formulation that enables etch-stop free IGZO processing without damaging IGZO properties.

- High Metal Etch Rates
- High Selectivity to Oxides
- Minimal Effect on IGZO Properties



Current IGZO-based TFT Integration



TFT Integration utilizing SACHEM's Chemistry


TSV wafer bonded to carrier


TSV wafer backside grinding


SACHEM TSV Reveal Etch™


RDL processing

SACHEM's TSV Reveal Etch™ Solution

TSV Reveal Etch™ is a formulation designed to enable all wet silicon etch in the TSV reveal process. This novel solution, developed in collaboration with Solid State Equipment Corporation, combines fast silicon etch rate with high selectivity to metals and oxides. In addition, the process yields reduced silicon surface roughness, potentially eliminating the need for CMP.

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news

worldnews

USA | Intel CEO Brian Krzanich was elected chairman of the **Semiconductor Industry Association**.

ASIA | **Texas Instruments** announced it will expand its manufacturing capacity in Chengdu, China, with a 300mm wafer bumping facility.

USA | **mCube** was named Start Up of the Year at the MEMS Executive Congress in November.

ASIA | **Applied Materials** announced it collaborated with **Samsung Electronics** and **PSK Inc.** to develop an advanced patterning solution for the manufacture of future generations of NAND and DRAM device designs.

USA | The **Semiconductor Industry Association** presented its University Research Award to professors from University of California, Berkeley and University of Texas at Dallas in recognition of their outstanding contributions to semiconductor research.

ASIA | Researchers at **Drexel University** and **Dalian University of Technology** in China have chemically engineered a new, electrically conductive nanomaterial that is flexible enough to fold, but strong enough to support many times its own weight.

EUROPE | **STMicroelectronics** announced it has shipped 5 billion MEMS sensors.

ASIA | **MegaChips** signed an agreement to acquire SiTime, a MEMS and analog semiconductor company, for $200M.

IBM to pay GlobalFoundries $1.5B to take over chip fabs

IBM and GLOBALFOUNDRIES announced that GLOBALFOUNDRIES will acquire IBM's global commercial semiconductor technology business, including IBM's intellectual property, technologists and technologies.

IBM will pay GLOBALFOUNDRIES $1.5 billion in cash over the next three years to take the chip operations off its hands. The cash consideration will be adjusted by the amount of working capital, which is estimated to be $200 million.

GLOBALFOUNDRIES will also become IBM's exclusive server processor semiconductor technology provider for 22nm, 14nm and 10nm semiconductors for the next 10 years.

It its official statement, IBM said the agreement will enable the company to further focus on fundamental semiconductor research and the development of future cloud, mobile, big data analytics, and secure transaction-optimized systems. IBM will continue its previously announced $3 billion investment over five years for semiconductor technology research to lead in the next generation of computing. GLOBALFOUNDRIES will have primary access to the research that results from this investment through joint collaboration

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Experts at the Table: Focus on Semiconductor Materials *By Jeff Dorsch*

The cutting edge in semiconductor manufacturing has meant not only big changes in IC design and process technology, but also in semiconductor materials. What follows are responses from Linde Electronics; Kate Wilson of Edwards Vacuum; David Thompson, Technology Director, Process Chemistries, Silicon Systems Group, Applied Materials; and Ed Shober, General Manager, Advanced Materials, Air Products and Chemicals.

1. What changes are being made in materials in fabrication of FinFETs, gate-all-around transistors, vertical NAND and fully-depleted silicon-on-insulator processes? Are there other new developments and trends in semiconductor materials (in interconnects, for example)?

Kate Wilson: We are seeing an increase in MOCVD precursors, low-temperature precursors and switching of process gases for ALD and multilayer films.

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Wearable sensor market to expand sevenfold in five years

Driven by rising demand for fitness and health monitoring features as well as by improved user interfaces, shipments of sensors used in wearable electronic devices will rise by a factor of seven from 2013 through 2019, according to IHS Technology.

The worldwide market for sensors in wearables will expand to 466 million units in 2019, up from 67 million in 2013.

Shipments of sensors will climb much more quickly than the market for the wearable devices themselves. Wearable devices will increase to 135 million units in 2019, less than three times the total of 50 million in 2013.

"Wearables are a hotbed for sensors, with market growth driven by the increasing number of these components in each product sold," said Jérémie Bouchaud, director and senior principal analyst, MEMS & Sensors, at IHS Technology. "The main factor propelling this phenomenon is a transition in market share away from simple products like pedometers and toward more sophisticated multipurpose devices such as smartwatches and smartglasses. Instead of using a single sensor like the simpler devices, the more complex products employ numerous components for health and activity monitoring, as well as for their more advanced user interfaces."

The average wearable device shipped in 2019 will incorporate 4.1 sensor elements, up from 1.4 in 2013.

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at the Colleges of Nanoscale Science and Engineering (CNSE), SUNY Polytechnic Institute, in Albany, N.Y.

Through the acquisition, GLOBALFOUNDRIES will gain substantial intellectual property including thousands of patents, making GLOBALFOUNDRIES the holder of one of the largest semiconductor patent portfolios in the world.

GLOBALFOUNDRIES will acquire and operate existing IBM semiconductor manufacturing operations and facilities in East Fishkill, New York and Essex Junction, Vermont, adding capacity to serve its customers and thousands of jobs to GLOBALFOUNDRIES' workforce. GLOBALFOUNDRIES plans to provide employment opportunities for substantially all IBM employees at the two facilities who are part of the transferred businesses, except for a team of semiconductor server group employees who will remain with IBM. After the close of this transaction, GLOBALFOUNDRIES will be the largest semiconductor technology manufacturing employer in the Northeast.

GLOBALFOUNDRIES will also acquire IBM's commercial microelectronics business, which includes ASIC and specialty foundry, manufacturing and related operations and sales. GLOBALFOUNDRIES plans to invest to grow these businesses.

IBM took a related pre-tax charge of $4.7 billion in its third quarter. It also reported a 4 percent drop in revenue on Monday.

What the analysts are saying

In terms of its 14nm FinFET collaboration with Samsung, the acquisition and the sudden influx of top talent from IBM will certainly help get GLOBALFOUNDRIES up to speed, Robert Maire of Semiconductor Advisors LLC reported.

"Even though Samsung still holds the keys and most of the cards in their relationship, the addition of the IBM horsepower does help even things a little bit even though IBM hasn't been a serious player in the semiconductor business for quite a while it still has a deep well of expertise," said Mr. Maire.

Currently, analysts at Summit Research Partners are not concerned about the long-term financial impact of the acquisition.

"We think that at present, when the transfer of IBM's chip manufacturing assets to GLOBALFOUNDRIES is done, this is a non-event to the semiconductor industry for the most part," said Srini Sundararajan, Semiconductor, Semi-cap Equipment Analyst at Summit Research Partners. "That is sad considering that there were times in the 90s that IBM and Intel competed with one another over bragging rights for technological advancements."

"In terms of potential impact to semiconductor equipment companies, there would likely be minimal to no impact as potential capex spend would be absorbed within the capex spend of Global Foundries," Mr. Sundararajan concluded.

news cont.

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Linde Electronics: These devices will be implemented at aggressive nodes, e.g., 14/16 nm and below. Due to the unavailability of EUV lithography in HVM for at least the next 2—3 years, chip makers are forced to use multiple patterning techniques, which have led to several additional deposition and etch steps being incorporated relative to previous generations.

Of the devices mentioned, FinFETs and vertical NAND are becoming or will soon become mainstream in leading-edge logic and NAND fabs. Given that key parts of the device structures are approaching dimensions that are tens of atoms across, the tolerance for variability in the manufacturing process is significantly reduced, which in turn imposes special demands on materials suppliers to control variation in the quality of the electronic materials (EM) products supplied to a fab. This requires additional metrology and quality control techniques to be used across the EM supply chain, from incoming raw material to in-process material to finished product. In addition, these advanced devices are more sensitive to any unspecified species in the EM products, and it is crucial to measure trace levels of unspecified impurities and understand their potential interactions with the thin films and interfaces involved in these devices. Collaboration across all the supply chain participants is thus key. Looking ahead, novel channel materials such as germanium and III-V compound semiconductors will be required, which bring their own set of challenges in deposition and etch.

David Thompson: For all these architectures the big trends are the introduction of new materials to enable scaling and the increasing criticality of interfacial materials. Consistently meeting new material innovation and interface engineering requirements is what we call precision materials engineering. Numerous new materials are being used today to enable low-power, high-performance foundry/logic devices. Selective epitaxy and metal gate films deliver >2 nodes of performance scaling with no litho-scaling. The introduction of CVD Cobalt liner and selective Cobalt cap layers in interconnect improves device reliability by 80x by completely encapsulating interconnect with Cobalt. More potential new materials are being evaluated at 10nm and beyond in transistors and interconnect. In 3D NAND, SiN film is used to store electrons using charge trap storage technology, compared to planar NAND where polycrystalline Si film is used using floating-gate MOSFET technology.

Interface engineering is also becoming increasingly critical. Whether it's the transistor metal films, the interconnect cladding, or 3D NAND, there are essential

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enabling films that require sub-angstrom uniformity control across the wafer that have thicknesses between 10 and 40 angstroms – that's less than the diameter of an atom. Additionally, while the bulk properties of materials are a useful roadmap, developing an understanding of how barrier, electrical, and other properties are impacted when the material is so thin that it doesn't exhibit bulk properties is the challenge of the day. In many cases, a very particular pretreatment is required to enable the specific material interface to tune these properties. We're finding that increasingly these steps need to be carried out sequentially within a vacuum environment with no air breaks.

Ed Shober: For logic devices and the adoption of 3D transistors, such as FinFETs, there are many needs for new chemical precursors to deposit — for example, silicon nitride and silicon oxide at temperatures far lower than previously required. In earlier nodes the thermal budget was in the 450 to 600C range, now the budget has been reduced to the 250 to 400C range, and the expectation is that it will go lower in the future. The shallow dopant profiles around the fin structure is one of the reasons for this drive to lower temperatures. Atomic layer deposition (ALD) is playing a greater role in depositing films. Thus, the chemistries employed must adsorb and react on the surface quickly and allow for deposition of highly conformal films over high aspect ratio features. More metal precursors are being employed in the FEOL for logic in order to tune the work function of the transistors. In the BEOL the biggest metal change has been the adoption of cobalt as a copper capping film and as a barrier liner film.

Needs for CMP are also increasing with 3D transistor structures. There are at least three new CMP steps that need to be performed to fabricate the fin. Finally, cleaning continues to play a major role in preparing the structures for the next deposition step.

Vertical NAND is moving memory off the lithography road map and onto a track that is driven by number of SiO/SiN films in a stack. The material needs here are again ALD-based precursors for lining and filling the channels etches into these film stacks. A major driver in cleans is products that limit particles left on the wafer and the scale of these particles must be in the nm size range.

For all devices, but especially DRAM and logic, the delays in adopting EUV are driving the need for self-aligned double, triple and quadruple patterning. These patterning strategies require new materials for forming the structures needed to reduce the pattern dimensions.

2. What changes are necessary in pumps and abatement?

Wilson: Increased variety of precursors requires flexible product operating range and tailored set-ups by process. Collaboration with semiconductor tool manufacturers, collaborative research organizations and end-customer development facilities is becoming more critical to ensure best known methods are applied.

Shober: Compatibility with the chemical precursors which can be highly reactive is one necessary requirement. Particle generation by the components is also a major concern and must be addressed by the suppliers to the same scales as discussed in the above answer around semi materials.

3. What are the risks involved with certain materials? Can they be disposed of safely? What about EPA regulation of these materials?

Wilson: Metal byproducts can be very toxic and containment of them can be challenging. Special care needs to be applied to their capture and disposal. Many of the new precursors are flammable and pyrophoric as well as being highly toxic so abatement is essential. Safe handling of new flammable or pyrophoric deposition precursors puts additional challenges on the process equipment and its maintenance – leaks of material out of, and air leaks into, process equipment can have serious consequences and therefore have to be diligently avoided to prevent accidents. It's essential that sub-fab equipment designed to support advanced CVD processes should be designed from the outset with safe operation and servicing in mind. Better yet, an integrated sub-fab system design and a single point of ownership for the whole sub-fab system provide some assurance that the system can be operated with the minimum risk of accidents due to inadequate maintenance. Advanced integrated dry-pump/exhaust system/abatement/thermal management

systems are available from at least one reputable equipment supplier to support such advanced processes, and have been widely adopted by several top-tier device manufacturers to provide exactly such assurance of maximized risk reduction in their advanced CVD processes.

Shober: With the drive to lower thermal budget there is a trend to using chemical precursors that are more reactive and stable. Thus, how they are produced, packaged, shipped and used by the customers are risks that we must address as new products are introduced. Shipping is especially a concern because there are more limitations on what materials can be flown from one point to another. This is driving for more localization of production/purification to shorten supply chains. BCP is of course another concern. Customers are looking for multiple and secure supply of materials.

5. How are advanced processes, such as atomic-level deposition, affecting materials use?

Wilson: Diverting precursor and low utilization rates in the process cause higher unreacted material and waste.

Linde Electronics: Both atomic layer deposition (ALD) and atomic layer etch (ALEt) are key new processes required in leading-edge device manufacture because of the new elements being incorporated and the aggressive geometries being adopted to keep Moore's Law on track. Several new EM products are now used in ALD, e.g. organometallic molecules. For ALEt, quite a few traditionally used EM products (e.g. chlorinated gases) are currently being evaluated.

The selection of process materials becomes very challenging when multiple films are in close proximity, e.g. requiring high selectivity for etching one thin film without affecting two or more nearby materials.

Thompson: What we find is that the deposition technique or specific chemistries employed strongly impact material properties. There are almost no situations where when we migrate from one technology to another – say PVD to ALD – where we don't see significant change in materials properties associated with the technique.

Additionally, in many cases the materials that the industry is accustomed to using are no longer available for a new technique. Usually, there's a ripple effect on retuning other materials or processes to enable the new material. It's an exciting time – there's a renaissance of metallurgy in both the front end and back end.

Shober: ALD does have a tendency to reduce material consumption, but not to the degree one may expect as a result of the process itself. The biggest impact ALD is having is on chemical costs. Materials capable of being deposited by ALD are oftentimes novel and there only use is within the semi industry. Thus, the cost on a gram basis can be much higher than what the industry has come to expect from use of materials like TEOS.

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Smartphone brands are increasingly aware that wearables are a better platform for some types of sensors than mobile handsets. IHS expects components like humidity sensors and pulse sensors to move from handsets to wearable devices, such as new smartwatches introduced by Samsung, Apple and others. This will further boost shipments of sensors in wearables.

This information is derived from the new IHS report entitled "MEMS & Sensors for Wearables Report – 2014" from the IHS MEMS & Sensors service.

Sensor scan

The types of sensors used in wearables are motion sensors, microelectromechanical systems (MEMS) and sensors for user interfaces, health sensors and environmental sensors.

Motion sensors represent the dominant technology in the wearables segment and comprise the component categories of accelerometers, gyroscopes, magnetometers, pressure sensors and combo motion sensors. MEMS sensors for user interfaces include MEMS microphones, proximity sensors and MEMS displays.

The health sensor area is represented by pulse, pulse-oximeters, hydration and skin temperature sensors. Environmental sensors include humidity, temperature and ultraviolet (UV) components.

Sensing opportunity

Wearables increasingly are employing sensors for fitness monitoring, using motion sensors or health sensors. The wearable devices also are implementing fitness and health monitoring using motion sensors or health sensors like pulse sensors. On the user interface front, wearables use MEMS microphones for voice command and motion sensors for tap command.

"The use of these types of sensors reflects consumer preferences that are propelling the growth of the wearables market," Bouchaud said. "Users want health and fitness monitoring, and they want wearable devices that act as extensions of their smartphones. However, there's no real demand from consumers for environmental sensors. Instead, the rising adoption of environmental sensors such as humidity and UV devices is being pushed by both sensor suppliers and wearable original equipment manufacturers (OEM)."

Watching the market

The market for sensors in wearables will undergo a major acceleration next year as shipments of the Apple Watch commence. Overall wearable sensor shipments will double next year; shipments of sensors for smartwatches will surge by nearly 600 percent.

The Apple Watch not only employs an accelerometer, but also a gyroscope, a microphone and a pulse sensor.

"Similar to the iPhone and iPad, IHS expects the Apple Watch will set a de facto standard for sensor specifications in smartwatches," Bouchaud said. "Most other wearable OEMs will follow Apple's lead in using these four devices—or will add even more sensors to differentiate."

Fitness and heart rate monitors and foot pods and pedometers lead the wearable market in terms of sensor shipments in 2013.

However, smartwatches will take the top position starting next year and will maintain dominance through 2019.

STMicroelectronics dominates sensors

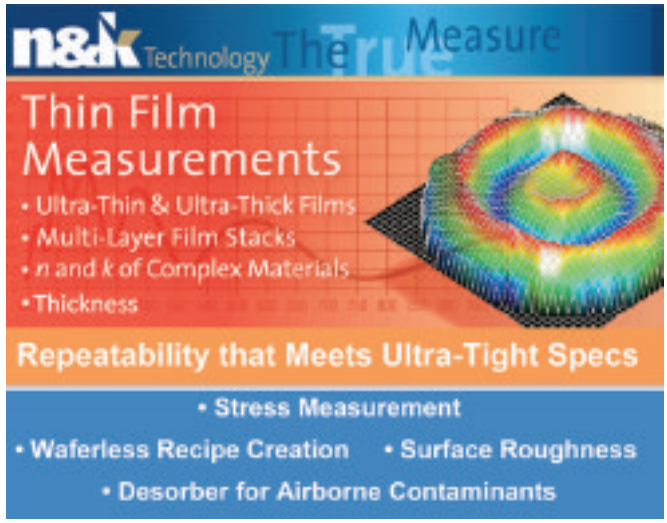
STMicroelectronics is by far the top MEMS and sensor supplier for the wearable market. The company consolidated its leadership position in 2013 with a 26 percent share of revenue, up from 20 percent in 2012.

Beside its leadership in the discrete accelerometer market, STMicroelectronics' success with wearable sensors is because of its strong bundling strategy. The company often sells its sensors as part of a packaged deal along with its other semiconductor offerings, such as 32-bit microcontrollers and wireless chips. ◆

n&k Technology, Inc. (n&k) designs, manufactures, and sells optical metrology systems with exceptional capabilities and wide ranging applications for the control of thin-films and critical dimensions. The company offers a wide portfolio of fully-and semi-automated systems for production control and R&D in Semiconductor, Photomask, Data Storage, and Flat Panel Display industries. n&k is a privately held company headquartered in San Jose, California, with customers around the world, and was founded 22 years ago by Dr. Rahim Forouhi and Dr. Iris Bloomer.

The origins of the company were in the 1980s when the founders deduced equations for n (refractive index) and k (extinction coefficient) of thin films based on first principles of quantum mechanics and solid state physics, an account of which can be found in Wikipedia under, "Refractive index and extinction coefficient of thin film materials." The company developed hardware with patented all-reflective optics to produce the strongest signal:noise possible. When the industry required optical critical dimension (OCD, also known as "scatterometry") control technology, the company responded with algorithms to perform Rigorous Coupled-Wave Analysis (RCWA) of trenches, holes, and other periodic structures.

n&k systems use polarized broadband spectrophotometry, measuring either the reflected or the reflected plus transmitted signals. Depending on n&k's system configuration and its applications, the wavelength range covers from Deep UltraViolet to Near InfraRed (190-1000nm), or the extended range to InfraRed (190-1500nm).



n&k's key products have features and measurement capabilities that are unique:

OptiPrime family of systems use the 190-1000nm range for measurements of thin films and trenches, and can be configured for either automated or manual wafer handling, and are available for either 200mm-/300mm- or 300mm-/450mm-diameter wafers.

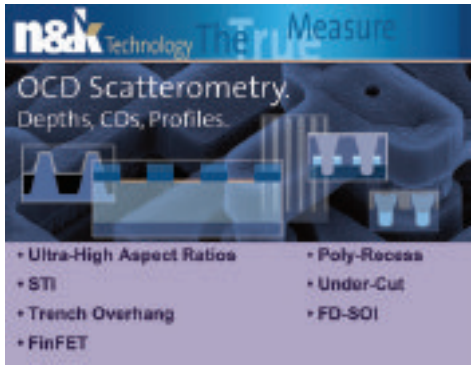
LittleFoot has similar capability to OptiPrime with the smallest footprint in the industry for a fully-automated system.

Olympian systems use the broader 190nm-15000nm range, enabling measurement of very thin and very thick films, Epi-Si, very rough and thick Poly-Si, as well as high aspect-ratio trenches. This family includes the manual loading **Olympian-M**, and the **Olympian-450** for 450mm-diameter wafers.

Gemini is offered for controlling the production of both conventional (transmissive) and EUV (reflective) photomasks. This unique system will simultaneously measure both reflectance and transmittance spectra for thin film and OCD measurements of photomasks.

EclipSE is the newest system from n&k, combining spectroscopic reflectometry with ellipsometry to unambiguously determine thickness, n and k spectra of thin films, plus depths, CDs, and profiles of trenches and holes. The tool measures film stress and provides waferless recipe creation. A desorber to remove airborne contaminants is also available.

With unmatched measurement capabilities, n&k's systems are acknowledged as the go-to solutions to characterize and control today's most challenging thin-films and periodic structures. n&k, located in the heart of silicon valley, has 15 Sales and Support offices worldwide.



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A Little More Patience Required for 2.5/3D

Dr. Phil Garrou,
Contributing Editor

There is an old proverb that states "All things Come to Those Who Wait." I personally am not the waiting type wanting to get things done ASAP but most civilizations look at patience as a virtue.

We've discussed the leading edge before. The leading edge is where the money is made. So while you don't want to be too early, you certainly don't want to sit back and wait to see if something is going to happen and let others drain all the profit from that early period of introduction.

Now having said that, let me counter by saying that "All things don't come to those who wait". I waited for thin film MCMs to take off in the 90's and early 2000's and they never did. A lot of us gambled and, in that case, lost. Life is a gamble!

TSV technology and 2.5/3D has had its own dichotomy. We couldn't sit back and allow others to get there first so we all anteed up our time and money without any assurance that there is big money to be made on this technology. Like the cat, we have been waiting (some more patiently than others) for 2.5/3D to enter HVM when in fact there has been no assurance that the mouse wasn't going to exit from another wall (i.e another technological solution as happened in thin film MCMs).

Anyone who understood what TSV technology could bring to the party, knew that HVM and actually new product design itself could not expand until foundry technology was available (since TSV were/are clearly going in during chip fabrication) and memory stacks were available, since foundries don't make DRAM. Of course it all has to be at the right price, but if it's not even available, what matters the price?

In terms of foundries TSMC was the first to announce and GlobalFoundries is not far behind, so those at the leading edge can now design in 2.5D. But what about memory?

While UMC and a few others have made noise about entering the 3D market space they appear to be significantly further behind.

The status of memory

The DRAM industry has been undergoing significant consolidation in the last few decades. The recent acquisition of Elpida by Micron has left 3 major players in the DRAM: Samsung with 38%, Hynix with 29% and Micron with 28% (according to Gartner).

Moving forward. the main roadmaps for DRAM suppliers all address: (1) reduce power consumption, (2) satisfy bandwidth requirements and (3) satisfy density requirements , all while maintaining low cost.

With DDR architecture running into a brick wall the memory suppliers have been focusing on new architectures that will deliver lower power, higher bandwith memory solutions. As shown in the Table, these include wide IO-2, HBM (high bandwidth memory) and HMC (hybrid memory cube).

Definition, standardization and scale up of these memory technologies has simply taken longer than any of us would have liked, but these are the new architectures what will take advantage of TSV stacking technology.

As we head into the fall of 2014 the last probably most important of the big three memory suppliers, Samsung has now announced production of TSV based memory stacks. This means we are about to have HBM for graphics modules, wide IO-2 for mobile products and HMC for HPC and high end servers. Now there can be no more excuses.

Within the next 18 months if we do not see product introductions announced 2.5/3D will begin to fade away until it is only remembered as another one of the bad bets we made attempting to stay on the leading edge.

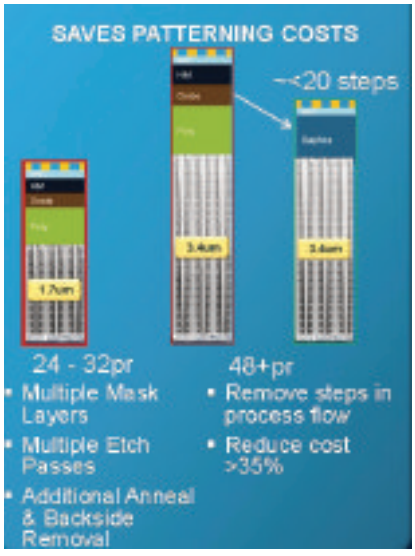
Packaging

A New Hardmask Process, Saphira

Pete Singer,
Editor-in-Chief

A new hardmask material and process was introduced this month by Applied Materials. Designed for advanced logic and memories, including DRAM and vertical NAND, the hardmask is transparent, which simplifies processing. It also exhibits very high selectivity, low stress and good mechanical strength. It's also ashable, so that it can be removed after etching is completed. Called Saphira, the process was developed in conjunction with Samsung and other customers. An Applied Materials-developed process for stripping the hardmask was licensed to Korea-based PSK.

Hardmasks are used for etching deep, high aspect ratio (HAR) features that conventional photoresists cannot withstand. Applied Materials first introduced an amorphous carbon hardmask in 2006, and now has a family of specialized films. The Advanced Patterning Films (APF) family now includes APFe, which enables deposition of thicker layers than APF (e.g., in capacitor formation and metal contacts for memory devices), and APFx, design to address patterning of metal lines and contacts at 5xnm and beyond.



The new Saphira APF process – which runs on the Applied Materials Producer XP Precision CVD chamber and works with PSK's OMNIS Asher systems -- introduces new film properties that include greater selectivity and transparency. The Saphira APF deposition and resolve major issues to improve patterning of more complex device structures at advanced technology nodes. "It's a materials solutions," said Terry Lee, vice president of strategy and marketing for the dielectrics systems and modules group at Applied Materials. "It's delivered with the patterning film itself, Saphira, as well as the combination of technologies and processes, whether it's in the CVD chamber or etch chamber, reducing process steps and simplifying process complexity.

Applied Materials isn't saying exactly what the Saphira hardmask is composed of, but a recent patent filing describes it as boron-rich amorphous carbon layer. The patent notes that, compared to carbonaceous masking layers, boron-doped carbonaceous layers, which include between 1 wt. % and 40 wt. % boron provide even greater etch resistance.

Lee said the Saphira film "In general behaves very much like a ceramic. But unlike most ceramics, it's ashable. It's structurally hard like a ceramic, but it's ashable like our standard carbon hard mask," he said.

In general, the selectivity of Saphira is twice the conventional masking materials on the open market, Lee said.

The new process reduces process complexity and cost in a couple of different ways. Because it's transparent, no extra step is needed to open the mask to find the alignment mark. And because the film has high selectivity, fewer masking steps are required. That all reduces the process complexity. Lee said that with conventional masks, in order to mask these high aspect ratio features, a thicker mask material is often needed. "When you have a thicker mask and you need to etch fine features, what you wind up with is a very narrow mask. In order to prevent the mask itself from collapsing or titling, you need very strong mechanical strength. With Saphira, we have that high mechanical strength and it resists the deformation," he said.

Saphira can also reduce the need for multiple hardmasks. "Instead of having the hardmask, oxide and poly (see figure), it drops down to a one mask that's thinner because the selectivity is higher," Lee explained. "What we're seeing is that we can reduce around 20 steps. When you reduce steps, you reduce cost. What we're seeing based on our calculations is something like 35% reduction in cost of this one module. Across multiple modules, that adds up to a lot of money," he added. ◆

Semiconductors

Laser Spike Annealing Resolves Sub-20nm Logic Device Manufacturing Challenges

YUN WANG, *Ph.D., Ultratech, San Jose, CA*

LSA technology plays an enabling role to overcoming manufacturing challenges for sub-20nm logic devices.

Sub-20nm system-on-chip and FinFET devices have specific manufacturing challenges that can be resolved with laser spike annealing (LSA) technology. Over the last decade, new process technologies and materials have emerged, such as strained silicon, high-k/metal gate (HKMG) and advanced silicide. Meanwhile transistor structures have evolved significantly, from bulk planar and PDSOI to 3D FinFET. With dimensions approaching atomic scales, the need for low thermal budget processes offered by millisecond annealing (MSA) becomes more important to precisely control the impurity profiles and engineer interfaces. This article will explain how LSA technology plays an enabling role to overcoming manufacturing challenges for sub-20nm logic devices.

LSA and MSA

The European semiconductor equipment market is expected to grow along with the world market. Global capital spending on semiconductor equipment is projected to grow 21.1 percent in 2014 and 21.0 percent in 2015. According to the August edition of the SEMI World Fab Forecast, semiconductor equipment spending will increase from $29 billion in 2013 to $42 billion in 2015.

In this article the terms LSA and MSA are used interchangeably. MSA can be implemented either by a scanning laser or a bank of flash lamps (**FIGURE 1**). In both cases, a reduced volume of substrate is heated to high temperature by a powerful light source, which results in fast temperature ramping compared to conventional RTP. Surface cooling in the millisecond time scale is dominated by conductive heat dissipation through the lower temperature substrate, which is several orders of magnitude faster than radiation heat loss or convection cooling through surfaces. The wafer backside is typically heated by a hot chuck or lamps to reduce the front surface peak temperature jump, and in some cases, to reduce the flash lamp power requirement or facilitate laser light absorption. Flash usually requires higher backside heating temperature than the laser option.

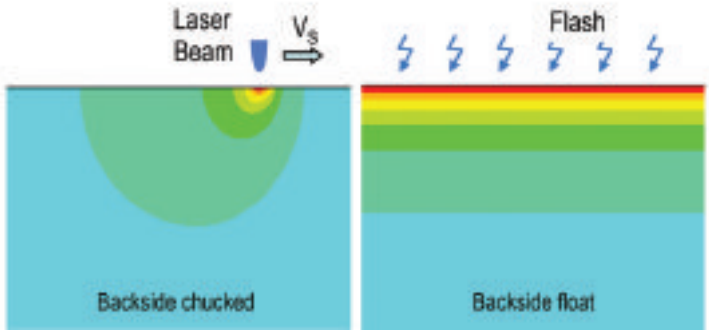


FIGURE 1. Simulated temperature distribution in silicon substrate by millisecond nonmelt scanning laser (left) and flash lamp heating (right).

There are important differences between flash and laser approaches. The flash system provides global heating where the top surface of the entire wafer is

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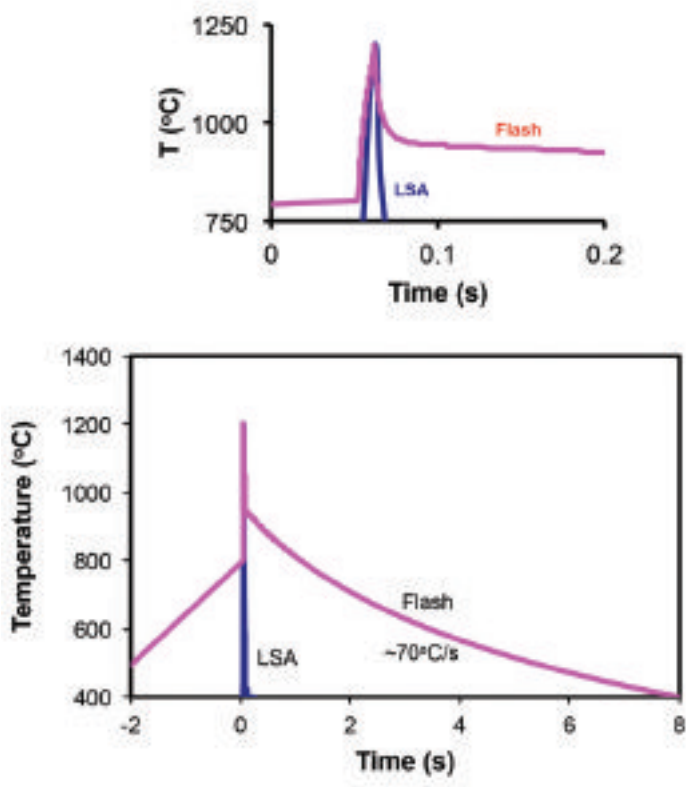

FIGURE 2. Comparison of simulated temperature profiles between long dwell laser and flash annealing. Tpk = 1200°C, dwell time = 10ms, preheat T = 800°C for flash. Inset shows details magnified around peak temperature.

heated at the same time. Hence heat dissipation occurs only in one dimension (1D - vertical direction). In addition, the backside needs to be floated to relieve the stress caused by global wafer bending due to the vertical thermal gradient. The laser system, on the other hand, provides localized heating around the scanning beam. The heat dissipation is between two-dimensional (2D) and three-dimensional (3D) (2D for an infinitely long line beam, and 3D for a point source). Since the thermal stress is localized, the backside can be chucked to facilitate heat sinking.

The difference in heat dissipation has a significant impact on the cooling rate, in particular, when long annealing or high intermediate (preheat) temperature is used. **FIGURE 2** compares the temperature (T) profiles between laser and flash systems for the same peak surface temperature (T_{pk}) and dwell time (t_{dwell}—defined as the full-width-half-maximum duration when a fixed point on the wafer sees the laser beam or flash pulse). The latter shows much slower ramp down. This is because once the flash energy is dissipated through the wafer thickness, the cooling is limited by the same radiation loss mechanism as in RTP. For applications relying on non-equilibrium dopant activation, the extra thermal budget due to the slow ramp down could be a concern for deactivation.

LSA technology uses a long wavelength p-polarized CO2 laser with Brewster angle incidence. Previous studies have shown that such configuration has benefits of reduced pattern density effect compared to short wavelength with near normal incidence. A second beam can be added to form a dual beam system that allows more flexibility to adjust the temperature profiles, and expands the process capability to low T and long dwell time.

FIGURE 3 shows different LSA annealing temperature-time (T-t) regimes that can be used to meet various application needs. Standard LSA used in front-end applications has Tpk ranging from 1050~1350°C and t_{dwell} from 0.2~2ms. Short dwell time is beneficial for reducing wafer warpage and litho misalignment, especially for devices with high strain. Long dwell time (2~40ms) adds more thermal budget for defect curing. It can also be used to improve activation and fine tune the junction depth. The low T regime enables applications that require lower substrate and peak annealing temperatures, such as annealing of advanced silicide or new channel/gate stack materials that have poor thermal stability.

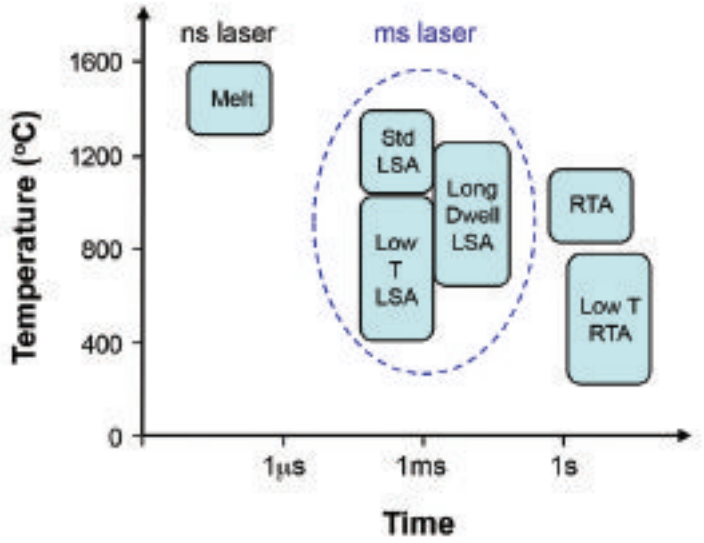

FIGURE 3. LSA extended process space. For comparison, T-t regimes of conventional RTA and nanosecond melt laser annealing are also shown.

High-k/metal gate (HKMG)

The impact of MSA on HKMG is thinner equivalent oxide thickness (EOT) due to reduced interfacial layer growth from a lower thermal budget. Lower leakage and better surface morphology are also observed in hafnium-based, high-k films when annealed by a laser.

Incorporating nitrogen into a high-k dielectric film can improve thermal stability, reliability, and EOT scaling. Post nitridation anneal with MSA provides opportunities to stabilize the film with a more precisely controlled nitrogen profile, which is important since excessive nitrogen diffusion can increase interface trap and leakage.

Oxygen has a strong impact on the characteristics of HKMG and it is important to control the ambient environment during the gate annealing. Full ambient control capability has been developed for LSA to accommodate this need. **FIGURE 4** shows the schematics of our patented micro-chamber approach that allows ambient control to be implemented in a scanning system using non-contact gas bearing. Different process gas can be introduced to accommodate various annealing and material engineering needs.

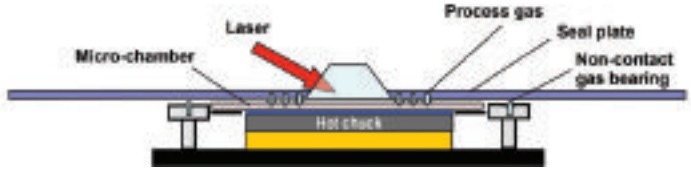

FIGURE 4. LSA extended process space. For comparison, T-t regimes of conventional RTA and nanosecond melt laser annealing are also shown.

Advanced silicide

Conventional NiSi processing involves two RTA steps. The 1st RTA (200~300°C) forms Ni-rich silicide, and the 2nd RTA (400~500°C) after selective etch of un-reacted Ni forms the desired low resistance NiSi phase. By replacing the 2nd RTA with a high temperature MSA (700~900°C), it can reduce leakage as well as improve performance. The improvement in leakage distribution results from the statistical reduction of Ni pipe defects due to the low thermal budget of MSA.

High temperature promotes phase mixing of Si-rich Ni silicide at the silicide/Si interface and lowers Schottky barrier height (SBH). In conventional RTA, this requires T > 750°C; such high T would lead to morphology degradation, excess diffusion, and higher resistivity. With MSA, because of the short duration, agglomeration does not occur until ~900°C.

To maximize the performance gain, anneal at high T close to the agglomeration threshold is desired. In such a case, minimizing within-die pattern effects and implementing within-wafer and wafer to-wafer temperature control becomes very important.

FinFETs

As FinFETs shrink, interface contact resistance, Rc, becomes more critical (**FIGURE 5**). A promising path to lower Rc is interface engineering by dopant segregation using pre or post silicide implantation. Thermal annealing is necessary to repair implant damage and activate dopants in pre silicide implantation scheme, and to drive-in dopants in post silicide case.

Using MSA instead of RTA results in more precise dopant profile control, higher dopant concentration at the interface and less potential silicide defectivity, due to the lower thermal budget.

Recently, Ti re-emerged as an option for contact metal because of better thermal stability and potential lower SBH. LSA can be applied to form low Rc Ti/Si contact. In advanced FinFET flow where contacts are formed after source/drain activation and gate stack, low thermal budget process is beneficial to minimize dopant deactivation and unintentional gate work function shift.

In-situ doped selective epitaxial growth is increasingly used to form the raised source/drain for FinFET. There is, however, a limitation in the maximum activation level it can achieve. Activation can be improved using MSA in combination with additional implantation. Drastic FinFET performance improvement has been achieved with co-optimization of conformal doping, selective epitaxial growth, implantation and MSA. In addition to front-end and middle-of-line applications, there are also opportunities at the back-end. One example is low-k curing. For FinFET, low-k is important not only as an inter-Cu dielectric, but also as a transistor-level dielectric to minimize the parasitic capacitance arising from 3D topography. The modulus and hardness of the low-k films can be improved without adversely impacting the k value using MSA.

New channel materials

Below the 10nm technology node, new materials with enhanced transportation, such as SiGe/Ge and III-V compounds, may be needed to meet the performance requirements. These materials have low thermal stability and are lattice mis-matched with the Si substrate, as a result physical integrity during thermal annealing is a very big concern. Low thermal budget processing by MSA provides a way to alleviate this issue. For example, studies on SiGe/Si heterostructures have shown that MSA can enable a higher annealing temperature than RTA, without strain relaxation or structural degradation. This results in improved activation. With MSA, junctions with enhanced activation and reduced diffusion can be obtained.

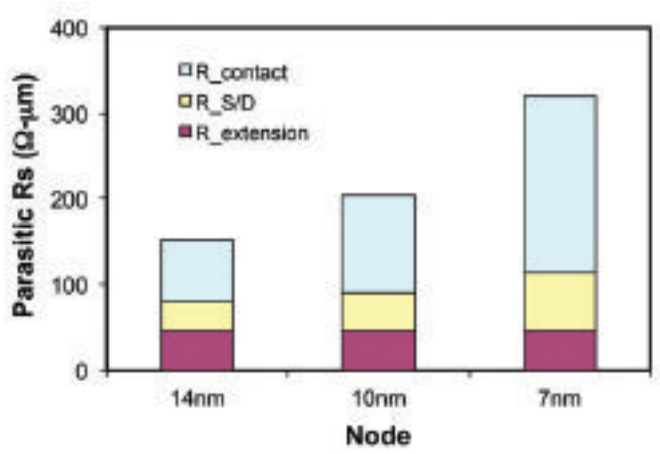

FIGURE 5. Parasitic resistance components for different nodes of FinFET, calculated using an analytical model. ρ_c of 10^{-8} Ω-cm² is used.

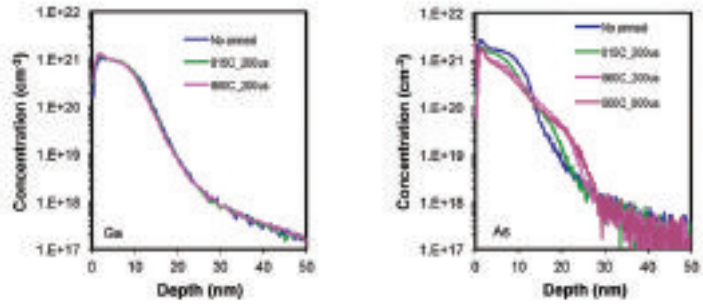

FIGURE 6. SIMS profiles of Ga-doped (left) p+/n and As-doped (right) n+/p Ge junctions annealed by LSA. For Ga, no diffusion is observed. For As, concentration enhanced diffusion is observed but can be reduced with short dwell time.

Summary

We have reviewed various applications of millisecond annealing for advanced device fabrication. As new materials emerge and device dimensions approach the atomic scale, precise thermal budget control becomes critical. This opens new opportunities for short time scale annealing. In addition to the traditional dopant activation and impurity profile control, MSA can also be used for interface engineering and material property modifications (structural, electrical, chemical, and mechanical). In general, if a desired process has higher thermal activation energy than an undesired process, application of high temperature, short duration annealing is beneficial. ◆

From Transistors to Bumps: Preparing SEM Cross-Sections by Combining Site-specific Cleaving and Broad Ion Beam Milling

J. TESHIMA, *LatticeGear, Beaverton, OR and* **JAMIL J. CLARKE,** *Hitachi High Technologies America, Inc., Clarksburg, MD*

Cross section sample preparation is demonstrated using a workflow that combines High Accuracy Cleaving (HAC) and Broad Ion Beam (BIB) milling.

In order to develop and manufacture new materials and processes, the cross section is essential (**FIGURE 1**). Cross sections allow one to visualize, measure, and characterize the chemistry of the film stack or device structures. This allows engineers to verify the integrity of devices and to make critical decisions about the process. To be able to provide this data, manufacturers and equipment suppliers invest close to a billion dollars annually [1] to purchase equipment for off-line use and out- of-fab support labs.

Because such labs are not considered a "make wafer" function, lab managers are under constant pressure to reduce costs, both per sample and for lab operations. This paper demonstrates cross section sample preparation using a workflow that combines High Accuracy Cleaving (HAC) and Broad Ion Beam (BIB) milling. Coupling these techniques, which are relatively low in cost when compared to Focused Ion Beam (FIB) or automated polishing or cleaving [2], reduces sample preparation time, complexity, and cost without sacrificing cross-section quality. The LatticeAxTM HAC and the Hitachi IM4000 BIB milling tools were used to demonstrate this process and are also described.

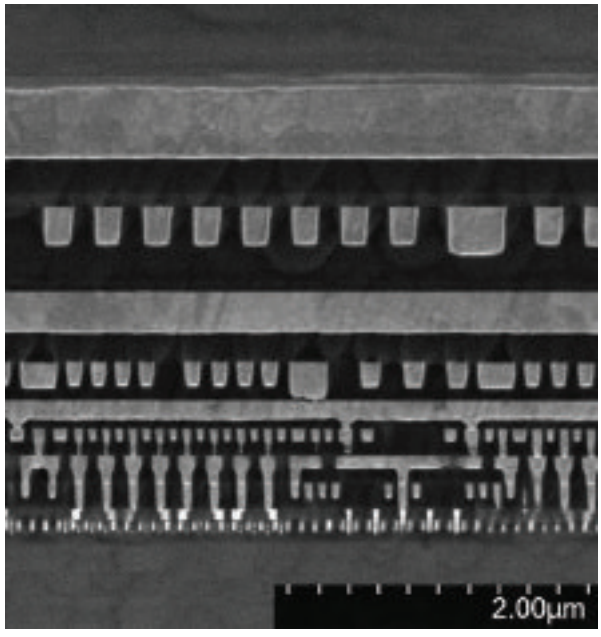

FIGURE 1. Cross section of a fully processed microprocessor prepared by high accuracy cleaving and flat milling

Preparing cross sections for SEM analysis

Characterization of semiconductor structures and material properties commonly begins with sample preparation. Semiconductor samples are inspected

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FIGURE 2. Wafers and wafer pieces enter a cross-section workflow that starts with cleaving and then follows a single- or multi-tool sample preparation process.

either as a cross section or "top down." Cross-section samples are needed to inspect layers of subsurface features. As shown in **FIGURE 2**, if a cross-section view is required and the original sample is a wafer or a die, cleaving is typically the first step in the sample preparation procedure.

In many cases, the sample can proceed directly to the Scanning Electron Microscope (SEM) as shown in the Single-Tool workflow. For fully processed devices and those with large metal structures, improving surface quality with another method enhances the results (see Multi-Tool workflow).

Advanced techniques used in the multi-tool workflow, such as FIB and automated polishing, have benefits in terms of submicron—or in the case of FIB, nanometer—targeting accuracy, but the tradeoff is high cost, long cycle time, and the need for skilled operators.

Methods

The following sections describe the techniques used to perform multi-tool, cross-section sample preparation workflow using HAC and BIB milling.

High Accuracy Cleaving An accurate and high quality cleave is critical to preparing a cross section for SEM imaging regardless of whether it follows the single- or multi-tool workflow. Manual cleaving, in which you scribe a line and then break the sample along the fracture over a raised edge or pin, has inherent problems with accuracy and repeatability. In addition, because the user handles the sample with

FIGURE 3a. Hand tools commonly used for cleaving semiconductor materials

fingers that are often gloved, great skill is required to achieve good results. **FIGURE 3a** shows traditional scribing hand tools used in manual cleaving. Cleaving results using these tools are obviously dependent on the hand-eye coordination of the operator.

The LatticeAx process overcomes these disadvantages by controlling the indent location and depth, as well as the cleaving operation, with fine-positioning knobs on the LatticeAx high magnification digital microscope. This new machine-assisted Indent and Cleave[3] approach bridges both manual scribing and fully automated cleaving or polishing, and increases success rates while keeping costs down.

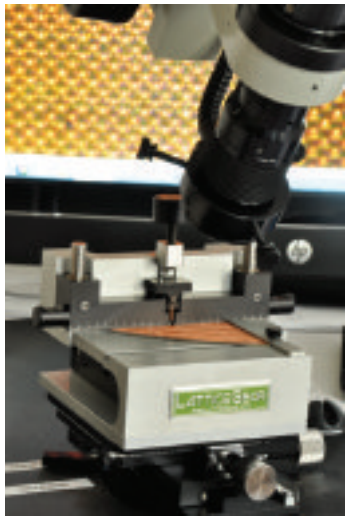

FIGURE 3b.

The accurate, repeatable indent and slow, controlled cleaving that results from this hybrid tool (**FIGURE 3b**) speeds preparation time and produces high accuracy, quality results—regardless of user experience—and with greater flexibility of sample size and dimensions.

Broad Ion Beam Milling The BIB milling system is a specimen preparation device (**FIGURE 3c**) for SEM and surface analysis (EDX[4], EBSP[5], etc.). The device uses a defocused beam of argon ions that sputter material from the target specimen at a

FIGURE 3c. Hitachi IM4000Plus broad ion beam milling system

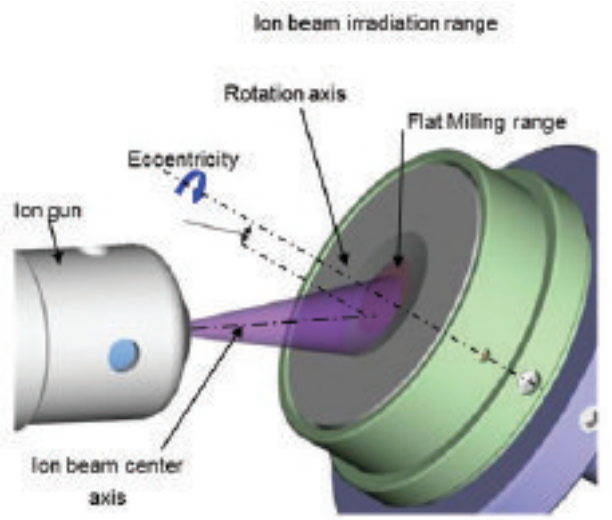

FIGURE 3d.

rate up to 2-500µm/hour, depending on the mode used. The BIB milling system uses a simple, repeatable process to remove surface layers of a specimen and for final finish of specimens in cross section. It is advantageous compared to mechanical polishing methods, which require well-trained operators to polish the specimen to a flat and mirror-like surface and hit a specific target. In addition, complex material composites that contain materials varying in hardness pose challenges when mechanically prepared using polishing wheels and compounds. This mechanical approach can lead to cracks, stress, relief (pull-out effects), and smearing. These adverse effects are minimized when using the low voltage (0-6kV) argon beam to remove material.

Flat Milling Mode Using the BIB's "Flat Milling" mode yields a high quality cross section in a short amount of time. It requires the initial high accuracy cleave to be through or within a few 100nms of the area of interest and the face of the cross section to be at 90 degrees to the sample surface. With a high quality cleave, the BIB's Flat Milling mode quickly polishes the cross-section face. Material is removed at a rate of 2µm/hr. Using the flat milling holder, the milling process can uniformly sputter an area approximately ~5mm across around the center of rotation of the specimen (**FIGURE 3d**). Typical operating parameters for the Hitachi IM4000Plus are 3kV accelerating voltage and a tilt of 70 degrees, with sample stage oscillation set to ±90 degrees and 10rpm. The best quality surface is achieved with a minimum mill time, thus the importance of cleaving through, or very close to, the region of interest. Otherwise, variations in the milling rates of different materials produce artifacts, often called "curtaining."

Cross-section Mode When more than a few microns of material need to be removed, the BIB system is operated in "Cross-section" mode. This is commonly used when exposing a sub-surface target structure. Mechanical grinding causes mechanical artifacts and deformation from stress, making it difficult to obtain a smooth surface for SEM analysis. When using the cross-section milling holder, the BIB IM4000Plus shields part of the argon ion beam with the mask arranged on the specimen, and produces a cross section along the trailing edge of the mask into the sample. For Cross-section mode, targeting accuracy is approximately +/- 15µm.

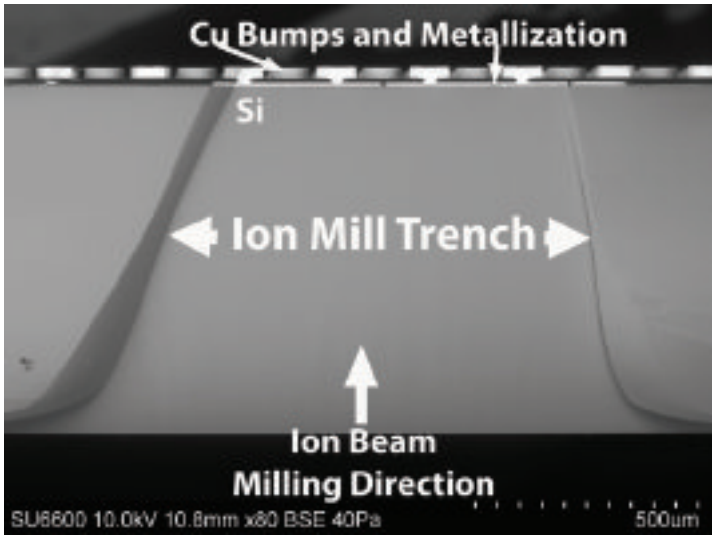

FIGURE 4. Copper bump after backside milling shows both the milling direction and the trench created by the ion beam

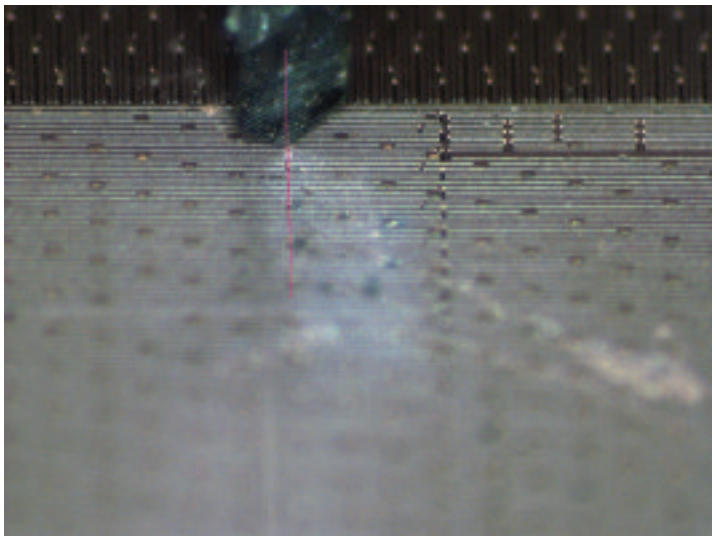

FIGURE 5a. Case Study 1 –HAC and flat milling processes for cross section final polish

Backside Milling Backside (as opposed to topside) milling mode can be used in both flat milling and cross-section modes. Backside milling is effective and necessary to alleviate curtaining effects[6] that can occur when traditional top-down ion milling induces striations. These striations are caused by the milling differential from neighboring materials that are atomically denser than the surrounding area. **FIGURE 4** shows the direction of the ion beam during backside milling and the trench milled by the ion beam.

Case Study 1. Quick 5-minute HAC and Flat Milling for Cross Section Final Polish

In this example, a cross section was prepared of an Intel microprocessor removed from its package. The size of the sample available after deprocessing was 8 x 8mm. To prepare the cross section, the sample was cleaved parallel to 15µm contacts visible on the sample surface. The Hitachi IM4000 was then used to prepare the final surface using flat milling mode. Approximately 100nm of material was removed in 10 minutes to achieve the polished surface of the final cross section.

The cross-section process included:

1. Indenting the 15µm area of interest (AOI) with the LatticeAx (**FIGURE 5a**) (3 min)
2. Cleaving through the AOI using the small sample cleaving accessory[7] (2 min) (**FIG 5b-c**)
3. Mounting the sample for the IM4000Plus and backside milling using flat milling mode (15 min)

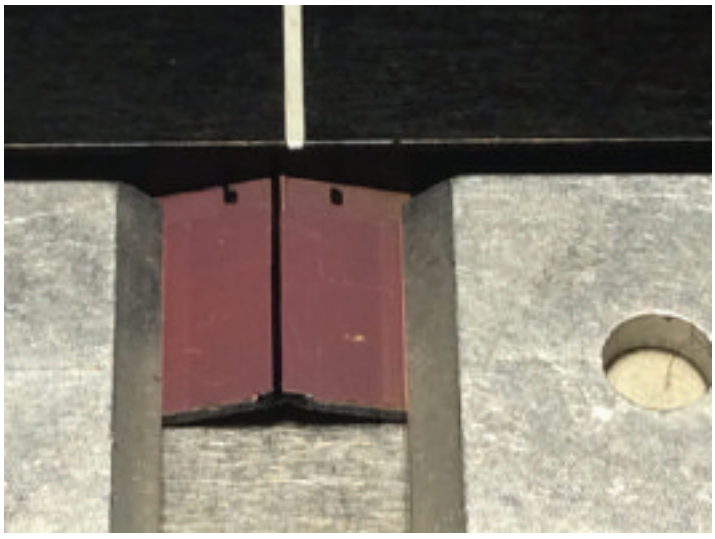

FIGURE 5b. View of sample after cleaving with the small sample cleaver

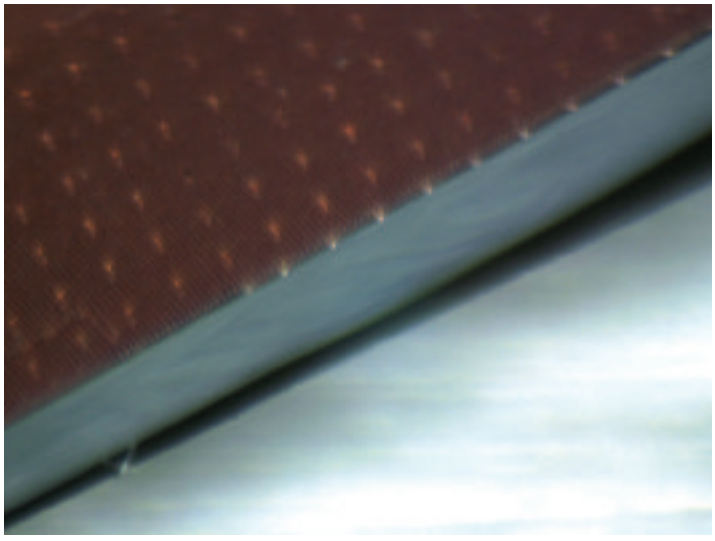

FIGURE 5c. Optical view of the cross section after cleaving

Results

This demonstrates a rapid (15-minute) method to obtain a damage-free cross section from a fully processed microprocessor over a very large area (5mm in diameter). A comparison of the results before and after milling shows the clear improvement in surface quality and SEM imaging results (**FIGURE 5d and e**). Using other methods such as mechanical polishing or FIB can take several hours to achieve a comparable size produced by the large flat-milled region. The best results were obtained when removing a minimum of material (nms), demonstrating the importance of an accurate, high quality cleave prior to BIB milling. **FIGURE 5f** shows a high-magnification view of the resulting cross section after flat milling that is high quality and without curtaining.

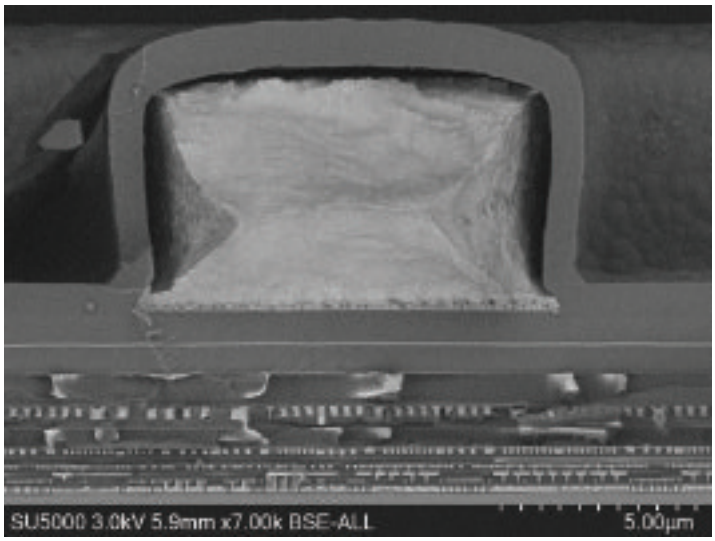

FIGURE 5d. SEM image of the microprocessor after cleaving

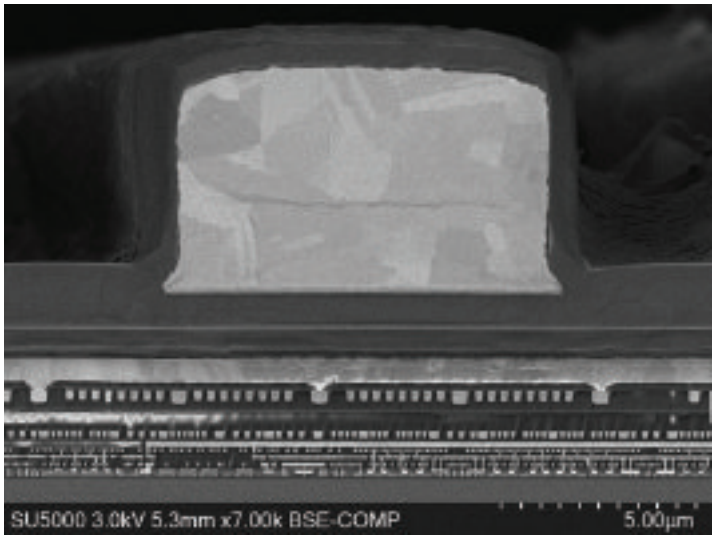

FIGURE 5e. SEM image of the microprocessor after 10 minutes of BIB milling using flat milling mode

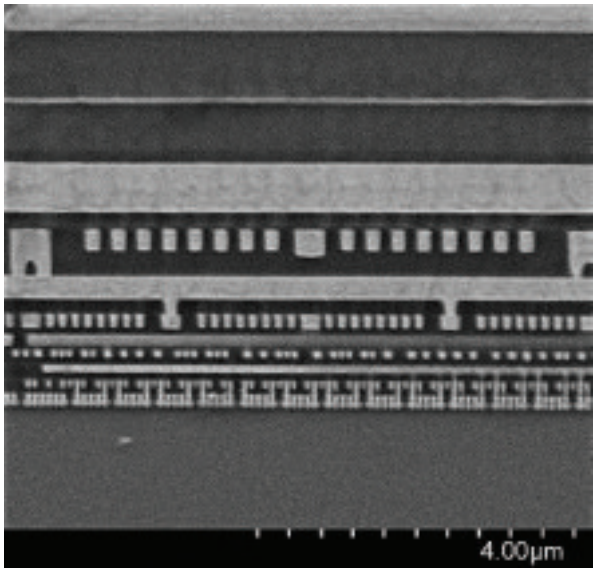

FIGURE 5f. SEM image showing planar cross section after flat milling

Case Study 2. Using HAC and BIB Milling in Cross-section Mode to Prepare Cross Sections of Solder Bumps

Cross sections are required to inspect solder bump reliability for interconnect problems during development and production, or for electromigration failure after aging. Creating these cross sections in a targeted location is critical for effective fault isolation and SEM analysis. With the advent of large Through-Silicon-Via (TSV) and solder bump structures—often 100µm in depth or width—high throughput methods are necessary to make cross sections efficiently and effectively.[8]

In this case study, the solder bumps were prepared for SEM in a two-step process. In step 1, the LatticeAx cleaver was used to cleanly cross-section close to, and parallel to, a specific row of copper bumps. The copper bumps had a diameter of 85µm and were cleaved 30 µm from the center of a bump. Time to cleave was 5 minutes and yielded the results shown in **FIGURE 6a and FIGURE 6b.**

In step 2, a broad argon ion beam instrument, the Hitachi IM4000, was used to prepare the final imaging surface within the copper bump. The backside milling method was used; no further preparation was performed.

Results

FIGURES 6c and 6d, taken after ion milling, plainly show the improved surface quality and copper grain structures, as well as fine details at the interface between the bump and adjacent structures. By cleaving close to the center of the copper bumps, the milling time on the BIB was reduced to less than 2 hours versus tens of hours for large cross-section areas (multiple bumps).

This two-step sample preparation process described has been implemented in production by a large semiconductor manufacturer. The technique described reduces turn-around time and repeatedly results in artifact-free cross sections of copper solder bumps.

Conclusion

For "off-line" laboratories, using HAC and BIB together for creating high quality cross sections is a compelling, low-cost alternative to investments in

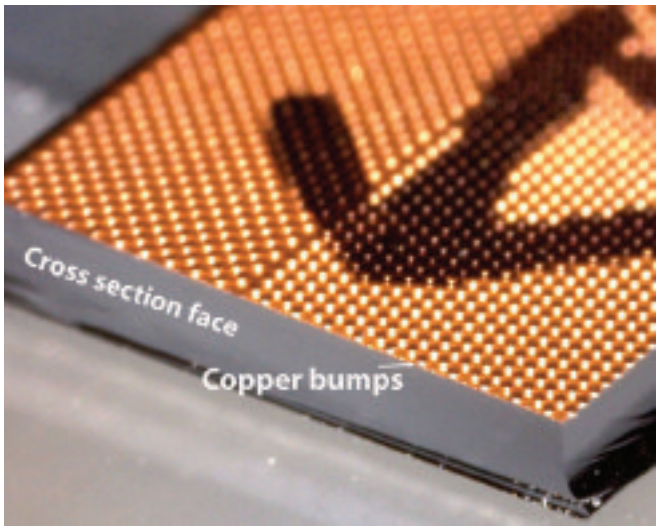

FIGURE 6a. SEM image of the microprocessor after cleaving

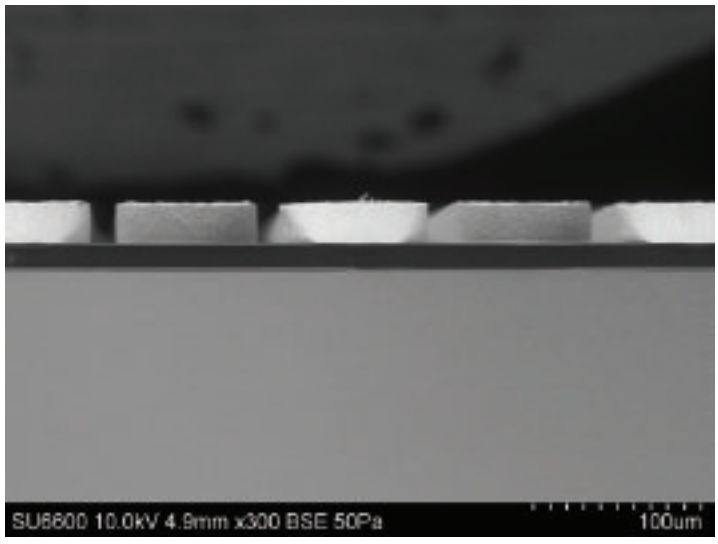

FIGURE 6b. SEM image of the microprocessor after cleaving

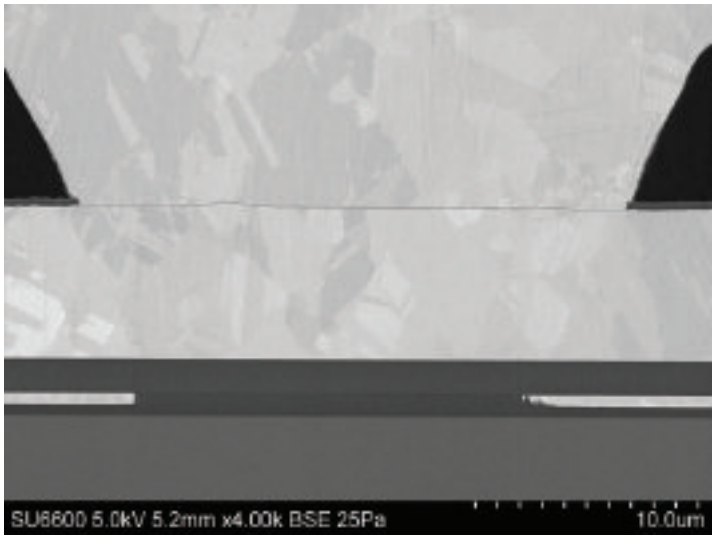

FIGURE 6c. SEM image of the microprocessor after cleaving

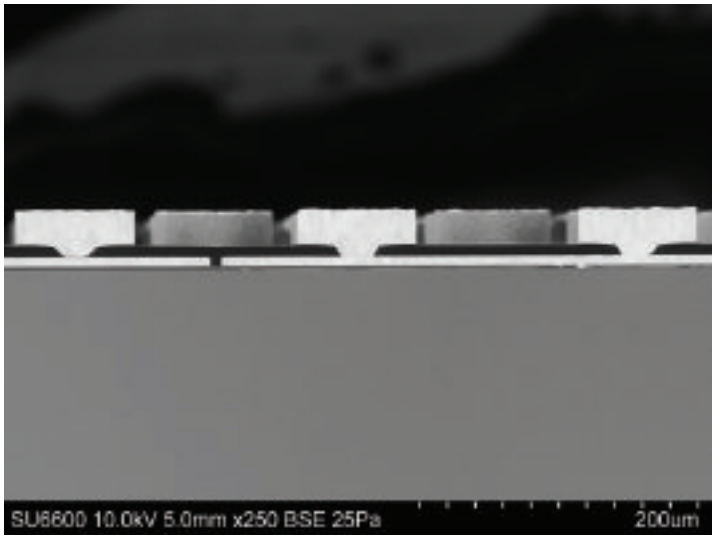

FIGURE 6d. SEM image of the microprocessor after cleaving

FIBs or automated polishing or cleaving equipment. High accuracy cleaving reduces sample preparation time, complexity, and cost without sacrificing cross-section quality. Combining this with a broad argon ion beam instrument for quick removal of minimal amounts of material or for milling of large flat areas, HAC presents effective, accurate results critical to product or failure analysis, while keeping both equipment and per- sample costs low.

Whether for final polish or in sample preparation of solder bumps, the results from the machine-assisted high accuracy Indent and Cleave approach combined with broad ion beam milling rival those of fully automated cleaving or polishing systems.

References

1. Per industry sources
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3. Cleaving Breakthrough: A New Method Removes Old Limitations, E. Moyal, E. Brandstädt, EDFAAO (2014) 3:26-31
4. Energy-dispersive X-ray spectroscopy
5. Electron backscatter pattern
6. CAVolkert and AM Minor, MRS Bull 32(5) (2007) 389–99.
7. The small sample cleaving accessory is used to clamp samples as small as 4mm wide for indenting with the LatticeAx and cleaving using a separate cleaving base.
8. Sample Preparation of Semiconductor Materials with a New Site-specific Cleaving Technology, Microscopy Today, September 2013, Teshima et al., 56-59.

LED Manufacturing with NMP-free Resist Stripping

NIK MUSTAPHA *and* **DR. GLENN WESTWOOD**, *Avantor Performance Materials, Inc.*
MARKUS TAN, JOACHIM NG, *and* **YANG MING CHIEH**, *Philips Lumileds Singapore*

The use of a semi-aqueous organic film stripper and residue remover that does not contain N-Methyl-2-pyrrolidone (NMP) is compared with current NMP-based chemistry.

Philips Lumileds collaborated with Avantor™ Performance Materials, a global manufacturer of high-performance chemistries, to evaluate one of Avantor's post-etch residue remover and photoresist stripper products as a replacement for a current chemistry.

Avantor's J.T.Baker® ALEG™-368 organic film stripper and residue remover is an engineered blend of organic solvents and semi-aqueous components suitable for bulk photoresist removal and post-etch/ash residue and sidewall polymer removal. Designed to provide broad process latitude in terms of processing times and temperatures, ALEG™-368 organic film stripper and residue remover is completely water soluble, requires no intermediate solvent rinse, and contains no hydroxylamine (HA), NMP, or fluoride elements.

The authors worked together to assess whether a change to Philips Lumileds' process of record (POR), using this product, could be accomplished without impacting yield or device quality, and with the desired cost savings.

NMP replacement challenges

Pending changes in environmental, health, and safety regulations in key manufacturing locations around the world may prohibit the use of NMP-based post-etch residue and photoresist removal products in LED manufacturing. The shift can already be observed in Europe and in some parts of Asia and the United States, where companies are moving toward NMP-free manufacturing environments. In today's competitive environment, it is vital for companies to find alternative chemistries that are not only effective and emphasize good performance, but also provide better cost of ownership. Philips Lumileds is taking a significant step to be part of this change.

Critical Substrates		Baseline	J.T. Baker® ALEG™-368
Etch Rate (A/min)	Oxide	<1	<1
	Al	<7	<7
	Nitride	<1	<1
	Ag	<5	<5
	TiWN	<0.5	<0.5
	III/V Nitride	<5	<5

TABLE 1. Comparable etch rate data (A/min) shown by baseline and ALEG™-368 product on critical substrates.

NIK MUSTAPHA *is a Principal Applications Engineer, Avantor™ Performance Materials, Inc.* **MARKUS TAN** *is Chief Process Engineer, JOACHIM NG is Senior Manager-Process Engineering, and* **YANG MING CHIEH** *is a Process Engineer at Philips Lumileds Singapore.* **DR. GLENN WESTWOOD**, *Senior Research Scientist, Avantor™ Performance Materials, Inc.*

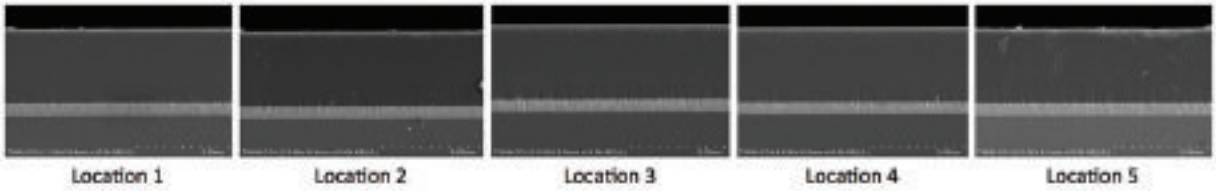

FIGURE 1. Cross-sectioning images showing resist on top of III/V metal surface before ALEGTM-368 process step.

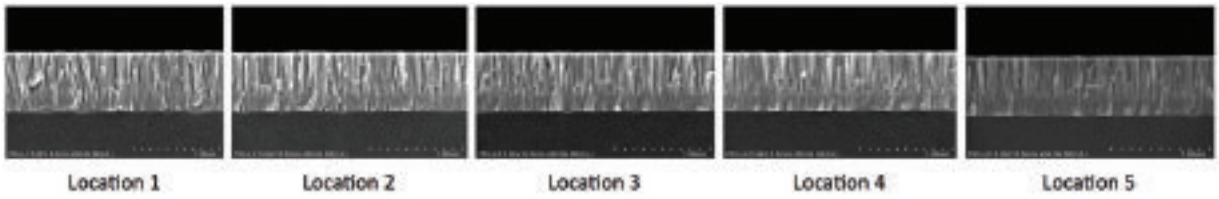

FIGURE 2. Cross-sectioning images showed no resist on top of III/V metal surface after processing in ALEGTM-368.

Initial verification tests of NMP-free product

As part of the process verification, several wafers were used to check etch rate on critical substrates such as III/V Nitride, Al, Ag, and Au. These wafers were also used to verify the effectiveness of the ALEG™-368 product to remove photoresist. Data were then compared with the current POR (**TABLE 1**).

It was important to confirm the effectiveness of the ALEG™-368 product in stripping capability of negative photoresist. A wafer with 5 µm thickness was used as an experiment. The wafer was dipped in the ALEG™-368 product at 75 °C followed by a water rinse step. To ensure uniformity of chemical performance, five locations were inspected by a scanning electron microscope (SEM) before and after treatment with the NMP-free product (**FIGURE 1**).

Post-treatment images after dipping the wafer in the ALEG™-368 product indicated that no resist remained on top of the metal surface (**FIGURE 2**). This supports the effectiveness of the ALEG™-368 product; it is capable of stripping photoresist completely, without visible damage to the metal surface.

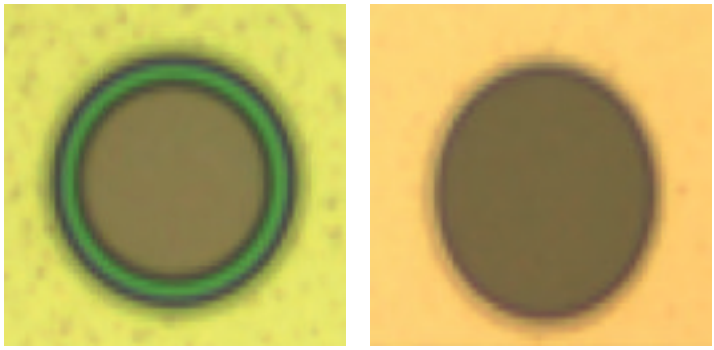

FIGURE 3. Post-treatment for POR material. No photoresist remained under high-magnification confocal microscope inspection.
POR material showed good stripping capability on patterned wafers.

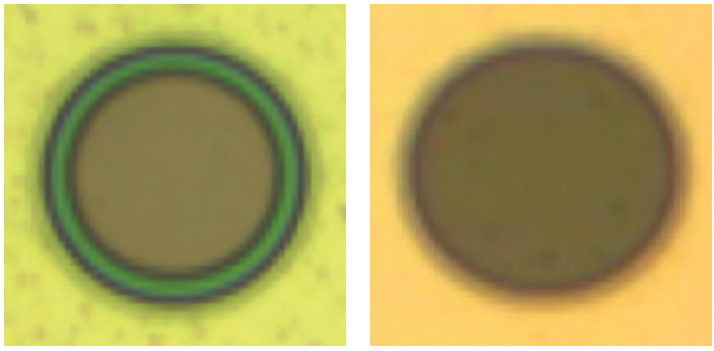

FIGURE 4. Post-treatment using the ALEG™-368 product. No resist remained under high-magnification confocal microscope inspection. POR material showed good stripping capability on patterned wafers.

Resist stripping and residue remover verification test on pattern wafers

Further tests were conducted on pattern wafers comparing POR and the ALEG™-368 product at 75 °C, for 30 minutes. Wafers were then cleaved and subjected to SEM inspection.

High-magnification images were obtained to verify cleaning performance and stripping capability of the ALEG™-368 product and POR wafers. For top-view inspection, a high-magnification confocal microscope was used to verify complete removal of photoresist. Results are shown in **FIGURES 3 and 4**.

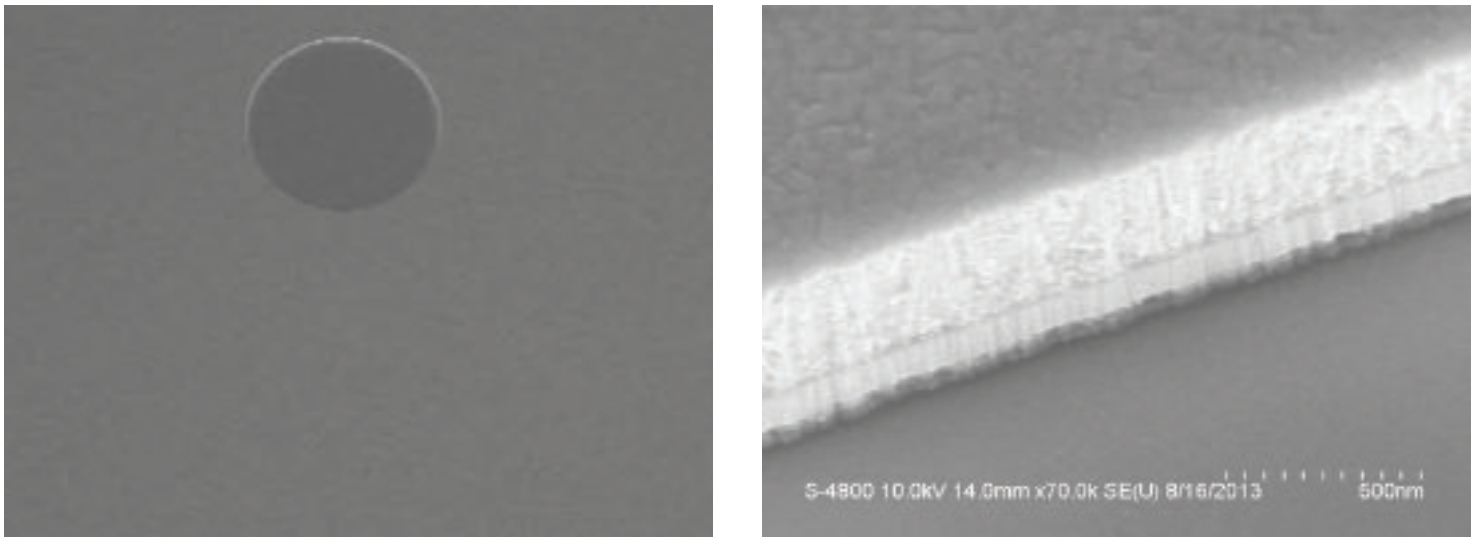

FIGURE 5. SEM images showing post-treatment for POR.

Both the POR and the ALEG™-368 product showed equal performance in terms of cleaning polymer residues and stripping photo resist on patterned wafers (**FIGURES 5 and 6**). The next critical step was to verify electrical performance for both the POR and the ALEG™-368 product.

Electrical performance for engineering lots

Wafers were sampled from several production lots before being split into two groups, one group using the baseline and the other using the ALEG™-368 product. Both groups were processed in an automated tool following the recommended process condition at an operating temperature of 75 °C and a processing time of 30 minutes. To achieve wafer uniformity, the tool was equipped with a mega-sonic function and recirculation to ensure effective cleaning of post-etch residues and stripping of negative photoresist.

After chemical treatment, the wafers were given an intermediate rinse using an IPA solvent to remove any remaining traces of the ALEG™-368 product from the surface of the wafer. Without this step, chemical left on the surface of the wafer could cause corrosion, water marks, or other device defects. Wafers were then subjected to a QDR (quick dump rinse) to remove all remaining solvent on the wafers. This step normally takes five to ten minutes, with noticeable CO2 bubbling to serve as extra protection from corrosion of exposed metal. Finally, all wafers were subjected to a nitrogen dry for five minutes, a vital process since any remaining moisture could cause severe corrosion and impact electrical performance and final yield.

Once all process steps were performed, both groups were subjected to electrical tests to ensure

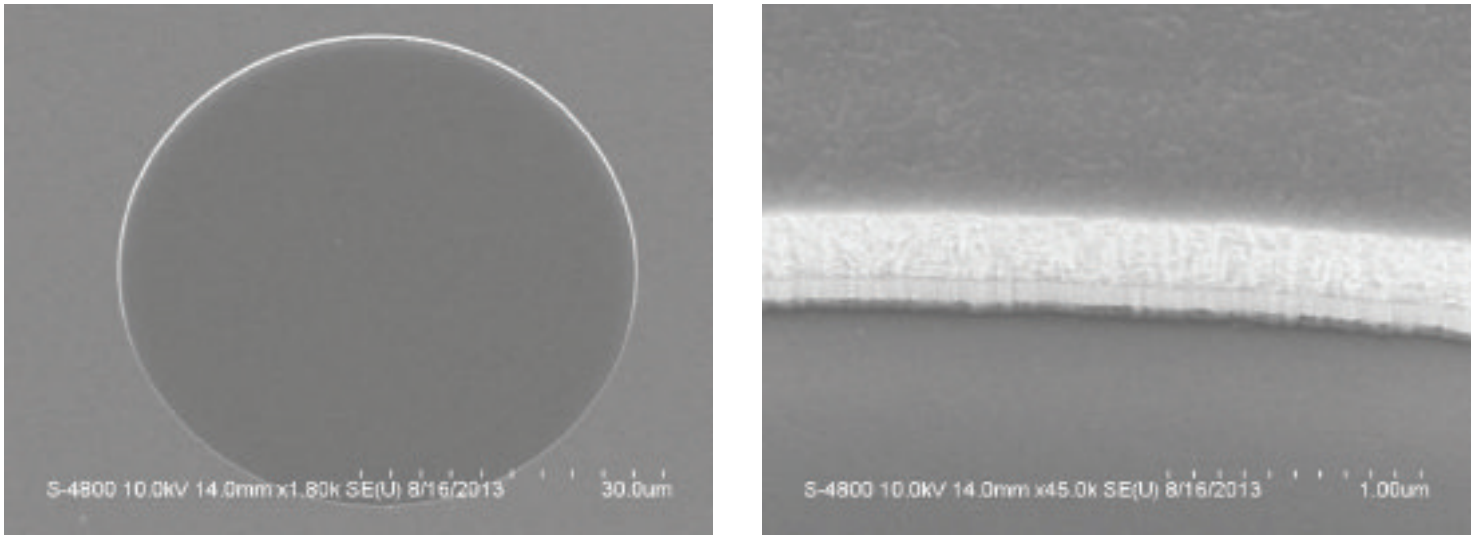

FIGURE 6. SEM images showing post-treatment for the ALEG™-368 product.

the chips on the wafers were functioning well and within specifications. Results, as indicated in **FIGURE 7**, showed no significant differences in term of electrical performance for both the baseline and the ALEG™-368 product. All wafers met specification and were subject to final yield probe.

Comparable Performance in Final Yield

The same production wafers which were processed using the ALEG™-368 product at 75 °C were then subjected to final yield analysis and compared to current POR.

There was slight improvement in the standard deviation for the ALEG™-368 product when compared to baseline chemistry. Overall, both products showed comparable final yield at 98 percent (**FIGURE 8**).

Reduced Cost of Ownership

It is undeniable that operating cost is a major consideration in LED manufacturing. Prior to adopting the current POR chemistry, Philips Lumileds tried both HA-based and NMP-based chemistries. Using the HA-based chemistry, a pre-treatment process was needed to soften the photoresist prior to stripping, followed by a solvent intermediate rinse. A strip process with the ALEG™-368 product eliminated this step and resulted in significant cost savings and increased throughput due to process simplification (**TABLE 2**).

Summary

The NMP-free ALEG™-368 product was comparable to POR when tested in various steps of the LED manufacturing process, including: substrate compatibility on critical layers, electrical performance on actual device, and final yield. In terms of process simplification, use of the ALEG™-368 product also showed similar technical benefits as POR, in which a significant reduction of the number of steps and chemicals used in the process leads to improved cost of ownership.

This collaboration demonstrates how a manufacturer can translate its commitment to environmental, health, and safety improvements and reduction of cost of ownership into the commercialization of a new cleaning process which can bolster its competitive position in the global LED manufacturing industry.

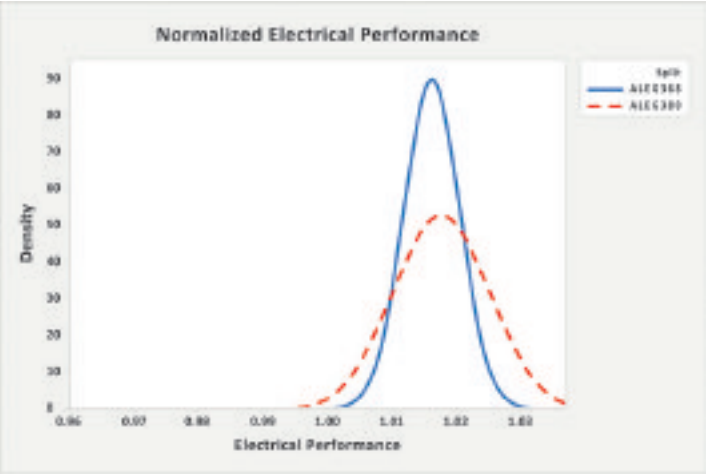

FIGURE 7. Electrical performance comparing ALEG™-380 and ALEG™-368 products for real production wafers.

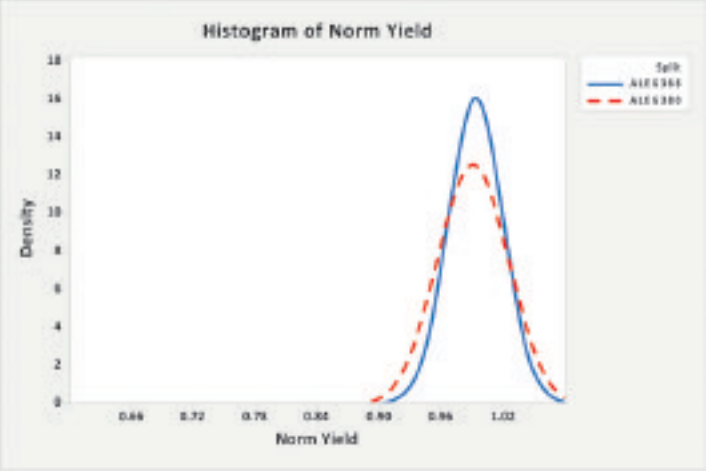

FIGURE 8. Yield distribution for ALEG™-380 and ALEGTM-368 products on real production wafers.

Strip Process	HA-based	NMP-based (POR)	NMP-free ALEG™-368
Process A	# of process steps: 4 # of chemicals: 4	# of process steps: 3 # of chemicals: 3	# of process steps: 3 # of chemicals: 3
Process B	# of process steps: 4 # of chemicals: 4	# of process steps: 3 # of chemicals: 3	# of process steps: 2 # of chemicals: 2

TABLE 2. Higher throughput and better cost of ownership due to a reduction in process steps.

The most expensive defect

DAVID W. PRICE *and* **DOUGLAS G. SUTHERLAND**, *KLA-Tencor, Milpitas, CA*

Defects that aren't detected inline cost fabs the most.

Defect inspection tools can be expensive. But regardless of the cost of the inspection tool needed to find a defect, the fab is almost always better off financially if it can find and fix that defect inline versus at the end of line (e.g., electrical test and failure analysis). Here, we are referring to the term defect in a general sense—the same concepts also apply to metrology measurements.

The third fundamental truth of process control for the semiconductor IC industry is:

The most expensive defect is the one that wasn't detected inline.

FIGURE 1A (top) shows an imaginary SPC chart for a factory experiencing a baseline shift in defectivity (an excursion) beginning at Lot #300. **FIGURE 1B** (bottom) shows the same scenario except the fab has an effective inline monitor at the point of the excursion. In this case, the excursion is quickly identified and the offending process tool is taken offline for process tuning or maintenance. The excursion is contained and relatively few lots are impacted by the resulting yield loss.

The difference between these two scenarios is that in the top chart, the fab is unable to detect the excursion inline so the baseline shift continues unabated until the first affected lots hit end of line test. For a foundry process with a 60-day cycle time, this delay could easily exceed 20 days.

In our experience working with IC manufacturers, the majority of financial impact does not come from large excursions that cause significant yield loss to every affected wafer—those problems are usually

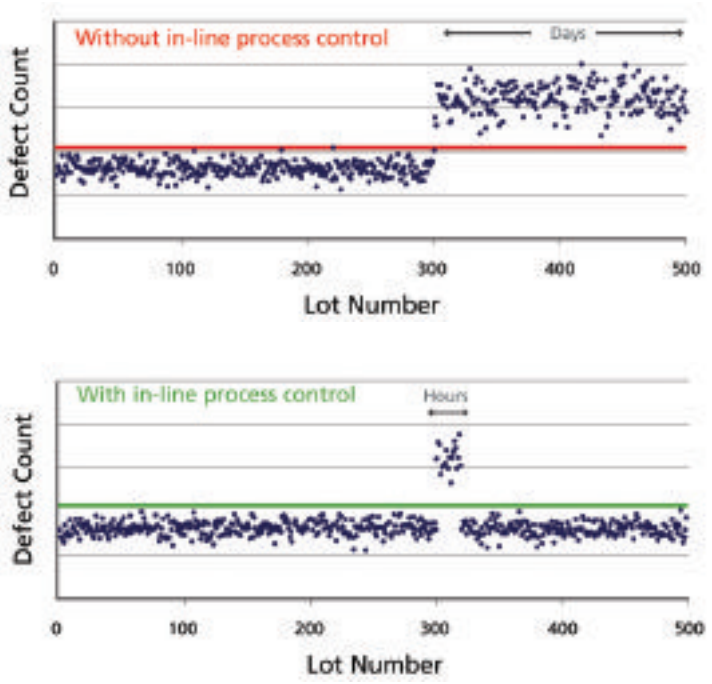

FIGURE 1. It is always better to find and fix problems inline versus at the end of line. 1a. Problem identification and correction does not occur until bad wafers reach end-of-line test. 1b. Problem identification and correction occurs immediately.

identified and rectified very early on. Rather, the largest losses usually come from small excursions that are difficult to detect. They cause relatively low levels of yield loss but persist for prolonged periods of time. It is not uncommon to see thousands or even tens of thousands of wafers exposed to these low level excursions.

The culprit is nearly always a process control capability issue that can be traced back to one or more possible problems. The following list is not meant to be exhaustive, but is instead, representative of the most common causes:

DR. DAVID W. PRICE *and* **DR. DOUGLAS SUTHERLAND** *are senior director and principal scientist, respectively, at KLA-Tencor Corp., Milpitas, CA.*

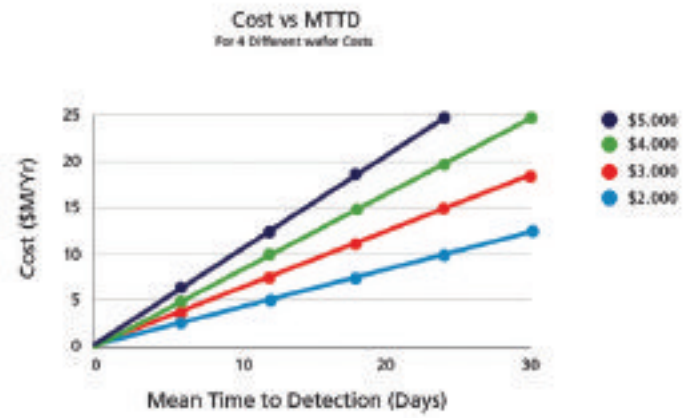

FIGURE 2. Cost vs. mean time to detection (MTTD) of finding a defect inline. The curves are drawn for 4 different wafer costs in a fab with 100k WSPM. It is assumed that the excursion takes place at a single step in the process and happens once per year to each of the process tools at that step. The yield loss is assumed to be 20% during the excursion.

Insufficient number of inspection points to allow effective isolation of the defect source

- Failing to use a sensitive enough inspection tool or recipe (pixel size is too large, wrong wavelength, etc.)
- Inspected area of wafer is too low
- Review sample size is too small

Often, the original inspection strategy was carefully designed, but as time passed, changes were made to reduce costs. As new sources of noise are introduced in the SPC chart, the fab becomes less sensitive to small excursions.

FIGURE 2 shows the economic impact to the fab for the two scenarios shown by the SPC chart in **FIGURE 1**. Imagine an excursion which results in a net 25 percent yield loss (e.g., one out of four wafers must be scrapped). Finding that excursion at end-of-line (+30 days) versus inline (greater than one day) would amount to a staggering $21 million loss per occurrence for an average size run rate of 25k wafer starts per month. Given that this value only represents the cost of re-manufacturing the scrapped wafers it could actually be a conservative estimate. The true cost could easily be double that amount for a fab that is running at the limit of their capacity since it would directly impact revenue.

Even if the situation requires the use of a relatively expensive inspection tool to find, monitor and resolve the problem, it is nearly always in the factory's best interest to do so. One of the implications of this truth is that if an important defect type can only be detected by a certain inspection tool, then that inspection tool is almost always the most cost-effective solution for that layer. Rather than modifying process control strategies to save costs, it is nearly always in the factory's best interest to maintain capable, inline process control strategies that prevent the financial impact of 'the most expensive defect.'

Author's Note: This is the third in a series of 10 installments that explore fundamental truths about process control—defect inspection and metrology—for the semiconductor industry. Each article introduces one of the 10 fundamental truths and highlights their implications.

Eliminating electrostatic discharge: Protecting tomorrow's technology

KNUT BEEKMANN, *Precision Polymer Engineering, Blackburn, Lancashire, U.K.*

A new range of dissipative materials based on fluoroelastomer and perfluoroelastomer polymers is designed for wafer processing and wafer handling applications.

All industries are now focusing on creating increasingly innovative products at a greatly reduced cost, providing customers with new cost efficient solutions. As new technologies are being produced, there is a need for an improved supply chain, providing new materials, improving wafer throughputs and lowering defects – all resulting in reduced costs for manufacturers.

When dealing specifically with the electronics industry, there is a particular focus for all major manufacturers on electrostatic charge reduction and elimination of electrostatic discharge (ESD). Electrostatic discharge is something we all experience on a regular basis – when walking across a carpeted floor and then touching a door handle, for example, or during a lightning storm. Although in everyday situations it is unlikely that any real lasting damage will be sustained, it is possible for electronic devices to be damaged by ESD events that are imperceptible to the human body. Even relatively low electrostatic voltages can have a huge impact on sensitive electrical devices, impacting yield, quality and reliability. It is suspected that ESD events occur hundreds of times a day. Although these are often not seen, they can have a significant impact on electrical equipment, resulting in a huge cost to manufacturers. In fact, it has been estimated that the cost of static associated damage ranges up to 33% for the electronic industry and between an average of 16 to 22% for component manufacturers [1] - a number which all would like to see dramatically reduced.

The principle of ESD

The initial creation of electrostatic charge requires energy to be transferred to a material which can occur when two materials repeatedly come into contact and separate. This is referred to as triboelectric charging. During this process a chemical bond is formed between the two surfaces as they come into contact, allowing charges to move from one material to the other to equalize their electrochemical potential. This creates a net charge imbalance between the objects. When separated, some of the bonded atoms keep extra electrons, while others give them away, though the imbalance will be partially destroyed by tunnelling or electrical breakdown (usually corona discharge). In addition, some materials may exchange ions of differing mobility, or exchange charged fragments of larger molecules.

When objects at different electrostatic potentials are brought together, the result is a rapid transfer of charge between the objects – the spark or 'shock' we commonly recognise as static electricity.

The triboelectric effect is not very predictable, and only broad generalizations can be made. However, materials such as glass or silica, plastics and elastomers, all of which are a fundamental requirement of semiconductor device manufacturing,

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either as a handling material or as part of the device, can each be a source of electrostatic charge. Once a material has become charged, the electrostatic field can also induce a charge distribution in nearby ungrounded conducting materials.

The level and sign of charge will mostly depend on the types of material, as summarized in **TABLE 1**.

The impact of electrostatic charging

ESD has been an issue across multiple industries for as long as manufacturing has been taking place. Military forts in the 1400s were using static control procedures and devices trying to prevent inadvertent electrostatic discharge ignition of gunpowder stores. By the 1860s, paper mills throughout the U.S. employed basic grounding, flame ionization techniques, and steam drums to dissipate static electricity from the paper web as it travelled through the drying process [2].

As electronic device technology has progressed, we have seen reduced voltage tolerances and lower capacity for heat dissipation. The age of electronics brought with it new problems allied to electrostatic discharge. Today, ESD impacts productivity and product reliability in virtually every aspect of the global electronics environment and emphasis on minimizing electrostatic charging and ESD has become hugely important [2].

When flowing through an integrated circuit, electrostatically induced charge can generate sufficient heat to break down the gate structure, cause spiking in contacts, junction breakdown and burn the interconnects. ESD events can also create a weakness that can lead to reliability issues or premature failure [3]. Damage from ESD on semiconductor devices can be immediate and catastrophic and can be blamed for millions of dollars of product failures a year.

ESD events may also interfere with the control electronics of the process tool. ESD creates electromagnetic energy transmitted in the form of waves in the radio frequency range, leading to electromagnetic interference (EMI) [4].

Example Materials in the Triboelectric Series	
+	Glass
Positive	Mica
	Human Hair
	Nylon
	Wool
	Fur
	Lead
	Silk
	Aluminium
	Paper
	Cotton
	Steel
	Wood
	Amber
	Sealing Wax
	Nickel, Copper
	Brass, Silver
	Gold, Platinum
	Sulfur
	Acetate Rayon
	Polyester
	Celluloid
Negative	Silicon
-	Teflon

TABLE 1. Example materials in the triboelectric series.

Finally, electrostatic charging of materials can also lead to attraction and subsequent adhesion of particles from the ambient or from within the process tools. Electrostatic attraction will not distinguish between material types and create potential yield reducing damage, as both insulating and ungrounded conducting matter can be equally influenced.

The failures can all have a dramatic impact on manufacturers, especially when we consider the cost of repairing equipment that has been exposed to ESD – especially if such failures happen once the component has been installed into a system. While a simple piece of electronic technology may cost only $10 to replace and retest on its own, when it fails in the field it could mean a cost of hundreds or thousands of dollars. Recent approximations propose that the cost of repairing an ESD-damaged product

increases tenfold at every level between individual component to system [1].

Semiconductor manufacturing

Modern semiconductor production plants have become significantly more automated, especially as wafer sizes have increased to 300mm. Wafers can undergo more than 1000 process steps and multiple robotic wafer handling cycles per process step, providing opportunities for static charges to accumulate and discharge. To a large extent, therefore, static build up is inevitable. In order to counteract this risk, system manufacturers have a responsibility to monitor the environment and use appropriate materials and equipment, as well as ensuring grounding and controlled leakage paths in order to control ESD.

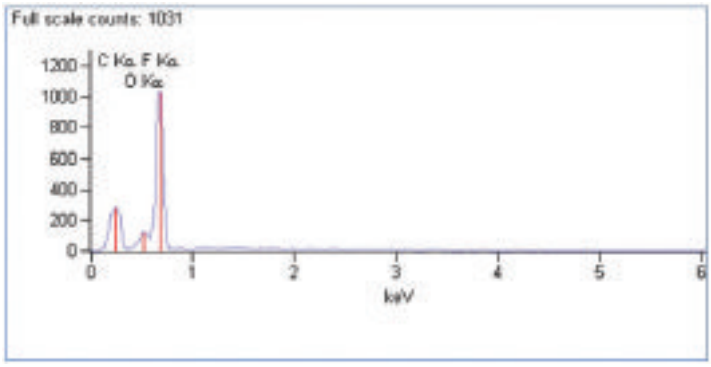

FIGURE 1. EDX spectra of electrostatically dissipative perfluoroelastomer.

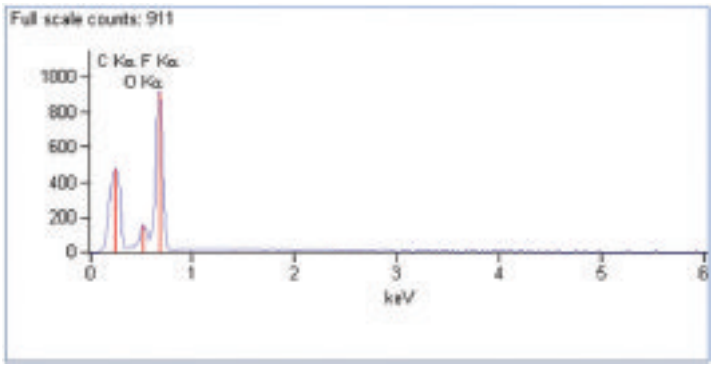

FIGURE 2. EDX spectra of electrostatically dissipative fluoroelastomer.

Plastics and elastomers are commonly used to contact or support substrates through production lines. They serve their main purpose in several ways; substrates do not slide as they move and they should potentially be able to withstand raised temperatures without creating adhesion issues. However, these contact materials are primarily insulators. Whenever a substrate is in contact with a handling device and subsequently separates, triboelectric charging will take place. This increases the likelihood of a subsequent ESD event or induced charging of materials.

Rather than using insulators to contact the substrates, these materials should be electrostatically dissipative and have a low resistance path to ground. To ensure this, electrostatically dissipative materials need to have a volume or surface resistance between that of insulating and conducting materials at between $1x10^4$ and $1x10^{11}$ ohms [2].

In addition to the properties previously mentioned, materials need to be compatible with semiconductor devices and not contribute to already sensitive levels of contamination. Elastomeric materials such as ethylene-propylene polymers (EPD/EPDM) can be obtained in dissipative variants; however these invariably contain metallic elements. Dissipative elastomer materials for semiconductor processing or handling should have controlled constituents and avoid common metallic filler.

Dissipative elastomers

Particular properties of fluoroelastomers and perfluoroelastomers, such as chemical resistance, higher temperature compatibility and low levels of contaminants, make them particularly suitable for semiconductor applications. Finding materials with additional electrostatic dissipative properties, however, often proves a challenge.

To meet this need, a completely new range of dissipative materials based on fluoroelastomer and perfluoroelastomer polymers has been specifically designed for wafer processing and wafer handling applications. **FIGURES 1 and 2** show an energy dispersive X-ray spectroscopy (EDX) analysis carried out on both polymer types and demonstrates a complete absence of metallic based filler and an entirely organic composition. This is summarized in **TABLE 2**. Despite avoiding the use of metallic

EDX Compositional Analysis in Weight %			
Material	C-K	O-K	F-K
Perfluoroelastomer	15.21	7.89	76.90
Fluoroelastomer	22.71	8.06	69.22

TABLE 2. EDX compositional analysis in weight.

based additives, volume resistance values can be obtained that are well within the dissipative range (**FIGURES 3 and 4**).

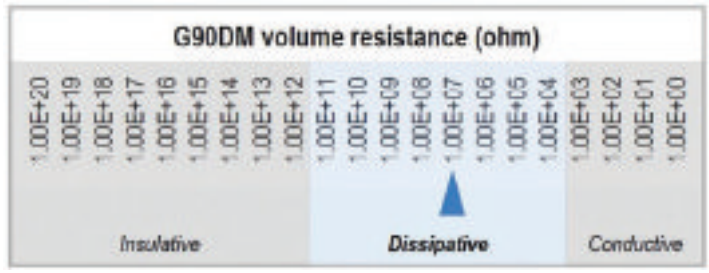

FIGURE 3. Perfluoroelastomer volume resistance.

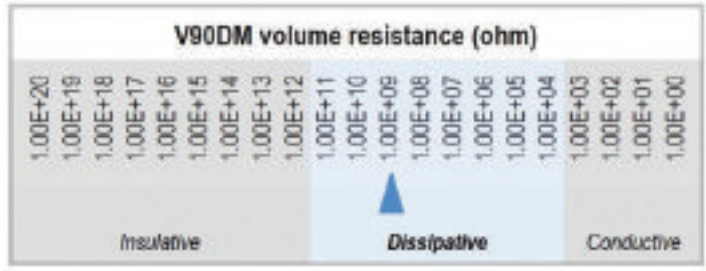

FIGURE 4. Fluoroelastomer volume resistance.

Conclusion

Technological progress within the semiconductor industry brings with it greater yield sensitivity, along with a common desire to reduce costs. These two factors are also related to defects and hence, how well those defects are controlled throughout an increasingly automated manufacturing process. An important part of reducing defects, both during and after production, includes management of electrostatic charging in order to avoid damage from ESD events. Greater use of dissipative materials is an obvious way of minimising charge build-up and reducing ESD events

However, it is also essential to ensure these materials are compatible with the process environment and the devices themselves. With the correct material and precautions in place, it is possible to avoid damage from static charge, particle contamination through electrostatic attraction and process tool interference through EMI.

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Delivering new Liquid Metalorganic Precursors to Epi and CVD

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The case is made for delivering liquid precursors from a central delivery system to the epi/dep tool as a vapor of precisely-controlled composition.

The epi and deposition processes for silicon-based semiconductor devices have used gaseous and liquid precursors. Gaseous precursors are compounds whose vapor pressure at room temperature is higher than 1500 torr (2000 mbar), which is sufficient to drive a mass flow controller (MFC). Using only one MFC, gaseous precursors can conveniently be metered to the process. Silane and dichlorosilane (DCS) have been used with that method. The industry has also used Trichloro silane (TCS) that boils at around 33°C and can be directly metered to a low pressure epi process using an appropriate MFC. For the epi of SiGe, germane, which is a gas, has been used. Tetraethylorthosilicate (TEOS) has long been used for the deposition of SiO2 and has mostly been delivered using direct liquid injection (DLI). DLI meters the flow of the liquid precursor to a flash evaporator and provides good control, but flash evaporation requires high temperatures and care must be taken that the precursor compound does not break up prematurely. This can be a challenge for precursors that work at lower deposition temperatures.

More recently, trisilane (Si3H8) has been used for low temperature Si epi and deposition. The delivery of trisilane to the process uses the carrier-gas-assisted delivery method. In the most common implementation, it employs an on-board evaporation ampoule dedicated to one reactor. The same setup has been used for III-V compound semiconductor and LED epi with good success. Driven by cost pressure, however, the LED epi industry is moving from dedicated onboard ampoules to a central delivery system for high-volume precursors like trimethylgallium (TMGa). One part of the cost reduction simply comes from the economies of scale. Another aspect comes from the elimination of excessive hardware, such as thermal baths and pressure controllers, and their maintenance. Most importantly, a substantial part of the cost reduction comes from yield increases due to improved process control. The same central delivery system can be used for trisilane and other liquid CVD precursors for silicon-based CVD for similar cost reduction.

Carrier-gas-assisted precursor delivery

Liquid compounds with an RT vapor pressure between 1 and 400 mbar require carrier-gas-assisted delivery. Many liquid compounds within that vapor pressure range are excellent precursors for CVD and epi processes. For such compounds, the difference between the vapor pressure and the process pressure is too small to drive an MFC for straight metering. Adding a carrier gas increases the pressure to between approximately 760 and 1500 torr (1000 and 2000 mbar). The selection of a good delivery pressure depends primarily on the desired concentration. The carrier-gas-assisted delivery method has long been used for trimethylgallium (TMGa) and trimethylaluminium (TMAl) for the growth of GaAs and GaN. For the growth of GaAlN and GaInN for LEDs, the composition ratio of the two group III

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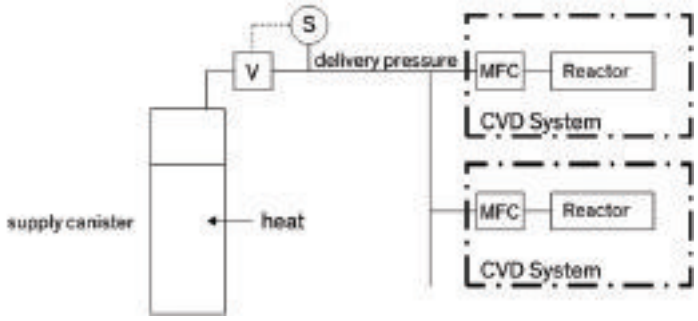

FIGURE 1a. High vapor pressure precursor, straight vapor delivery. S: pressure sensor, V: metering valve. S and V are normally integrated into a pressure regulator. MFC meters neat vapor.

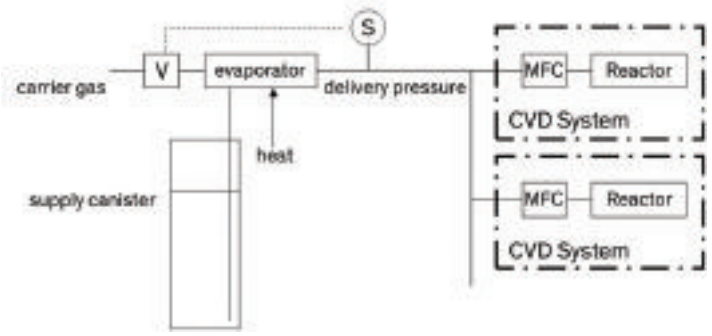

FIGURE 1b. Low vapor pressure precursor, carrier gas assisted delivery in Dow's VAPORSTATION™ Central Delivery System. S: pressure sensor, V: metering valve. MFC meters diluted precursor vapor. Pressure and temperature control guarantee high precision concentration.

precursors is extremely critical for the performance of the final product. Therefore, the precision of the evaporation and the metering has always been a concern.

FIGURE 1a shows the setup for a straight gas delivery and **FIGURE 1b** shows the setup for a carrier-gas-assisted delivery. The design shown in Figure 1b requires no modification of the epi/dep tool in order to accept a normally liquid precursor. From an epi/dep tool perspective, the design shown in Figure 1b behaves just like the straight gas delivery of Figure 1a. As such, it allows the use of the gas mixture from one delivery system at several points of use, i.e. the output of the delivery system can be subdivided. In Figure 1b the precursor vapor is made on demand. While the output (mol flux of precursor per time) is theoretically unlimited, there are practical limits that restrict the output to approximately 20 standard liters per minute (slm). The main limitation is the dynamic range of the metering valve: the best units have a dynamic range of 1 in 104, which means that they can reliably control a flow between 0.002 and 20 slm. This is important for the mol flux precision at smaller flows, i.e. when only one or two tools draw precursor.

On-board ampoules and central delivery system

There are several designs of carrier-gas-assisted delivery sources. The traditional design meters carrier gas into the ampoule rather than the mixture into the process chamber. Such a delivery system is dedicated to one reactor because the mass flow is metered upstream of the evaporation vessel and the associated MFC is controlled by the epi/dep tool. The ampoule serves two functions: (1) as the transport vessel and (2) as an evaporation device. For cost reasons, the ampoule should be of simple design. This means that trade-offs for the evaporation performance have to be made. The trade-offs result in line-to-line delivery rate variations and a noticeable change of delivery rate over the life of the ampoule. For some products, such changes require run-to-run recipe adjustments. In some cases the on-board ampoule is connected to a central dispense unit that transfers liquid precursor into the on-board ampoule. The result is a complex system that is still subject to delivery rate shifts requiring recipe adjustments.

A new central delivery system design is shown in Figure 1b. The task-optimized evaporator is fitted with temperature, pressure and level sensors that hold the precursor output variation at less than +/-0.4% by use of special stability algorithms. The evaporator is a permanently-installed part of the central delivery system. It is fed from a supply canister and features two precision thermometers inside the precursor liquid and gas distribution baffles and strainers for entrained droplets. Once calibrated, the system delivers a precisely known rate to a number of epi/dep reactors in the fab.

FIGURE 2 shows the output concentration of two calibrated central delivery units under various loads [1]. The curve that is alternately dotted and solid represents the signal of the binary gas sensor, which was alternately connected to one or the other unit. The other curves represent the output of the two units in standard liters per minute. The results show that proper calibration of the temperature and pressure

sensors results in error of the delivery of less than +/- 0.4%. This precision cannot be achieved with ordinary on-board ampoules.

Recently, the application of the VAPORSTATION Central Delivery system has been expanded to deliver $SnCl_4$ to a new process for the deposition of GeSn. It was fitted to a gas delivery line that was available on a mainstream silicon epi tool.

GeSn epi using a $SnCl_4$ as new precursor

There has been increasing interest in GeSn and SiGeSn as alternative Group IV semiconductor material for electrical and optical device applications. The continuing expansion of traditional silicon with Sn and Ge offers additional design options for band gap and stress engineering. Over the past years, stress engineering using Ge made a major contribution to the improvement in Si-CMOS device performance. More recently the use of GeSn as a stressor for Ge-CMOS and relaxed GeSn as a virtual substrate, which is used to create tensile strain in a Ge epitaxial film, have been considered. The creation of tensile strain in an epitaxial Ge film is expected to result in germanium with a direct band gap [5] for photonic devices. Epitaxial $Ge_{1-x}Sn_x$ itself has also been considered as a promising candidate material for lasers and photodetectors. It has been predicted that, for sufficiently high Sn content, relaxed $Ge_{1-x}Sn_x$ turns into a direct band gap semiconductor [6,7]. Recent work of imec and its partners describe the active functionality based on the heterogeneous integration of strained GeSn/Ge on a Si platform providing photodetection in the mid-infrared [8].

Due to the poor solubility of Sn in the Ge matrix of less than 1%, the epitaxial growth of (Si)GeSn is very challenging. Low solubility demands out-of-equilibrium growth conditions and, from epitaxial growth point of view, extremely low growth temperatures. Until recently, GeSn was grown by molecular beam epitaxy — a technique that is not suited for mass production. More recently, deuterated stannane, SnD_4 has been used as Sn precursor for a CVD process, but the practical application is questionable due to the instability of SnD_4.

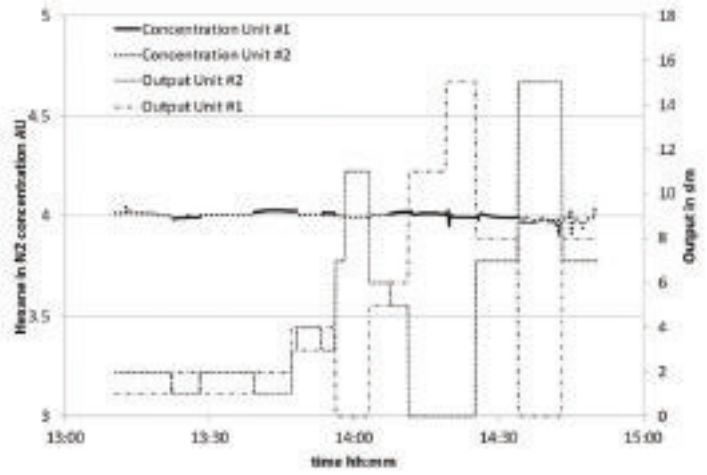

FIGURE 2. Output and concentration of two calibrated VAPORSTATION™ Central Delivery Systems. Concentration remains within +/- 0.4% of set point regardless of load.

To eliminate the problems posed by SnD_4, imec chose to investigate stannic chloride $SnCl_4$, a stable, benign, abundant and commercially-available liquid Sn compound. Currently though, most of the CVD reactors for SiGeSn epi are not designed to use liquid precursor sources. In order to facilitate the use of liquid CVD precursors at imec, Dow Electronic Materials provided an R&D version of the central delivery system. It features the output stability and other benefits described above. The use of one of these units enabled imec to use $SnCl_4$ and develop a groundbreaking new CVD process using digermane (Ge_2H_6) and $SnCl_4$ to grow GeSn epitaxial films in a production-compatible CVD reactor. The films are metastable GeSn alloys with up to 13% substitutional Sn [10,11].

FIGURE 3 shows a typical cross section transmission electron microscope (TEM) picture with associated (224) x-ray diffraction reciprocal space mapping (XRD RSM) of a fully strained GeSn layer, grown on top of a relaxed Ge virtual substrate. The deposition temperature for the GeSn growth was kept low (320°C) in order to allow Sn incorporation in Ge lattice without Sn precipitation or agglomeration.

The TEM picture in Fig. 3(a) exhibits a defect-free and high crystalline quality for the 40-nm-thick GeSn layer. Furthermore, the surface quality of the as-grown Ge0.92Sn0.08/Ge/Si heterostructure was investi-

gated by reflection high-energy electron diffraction (RHEED) analysis after ex-situ transfer to a MBE system. An annealing in ultra-high vacuum up to 420°C resulted in an oxide-free GeSn surface showing a strong (2x1) surface reconstruction as seen on RHEED pattern along the [110] azimuth (Fig. 3(b)). Finally, the XRDRSM around the (2 2 4) Bragg reflections (Fig. 3(c)) demonstrates that the grown GeSn layer is fully strained on Ge/Si (001) substrate.

Conclusion

The use of an improved delivery system for liquid CVD precursors allowed the use of stannic chloride for the growth of GeSn. The new process developed by imec produces metastable GeSn with concentrations of substitutional tin of 13%.

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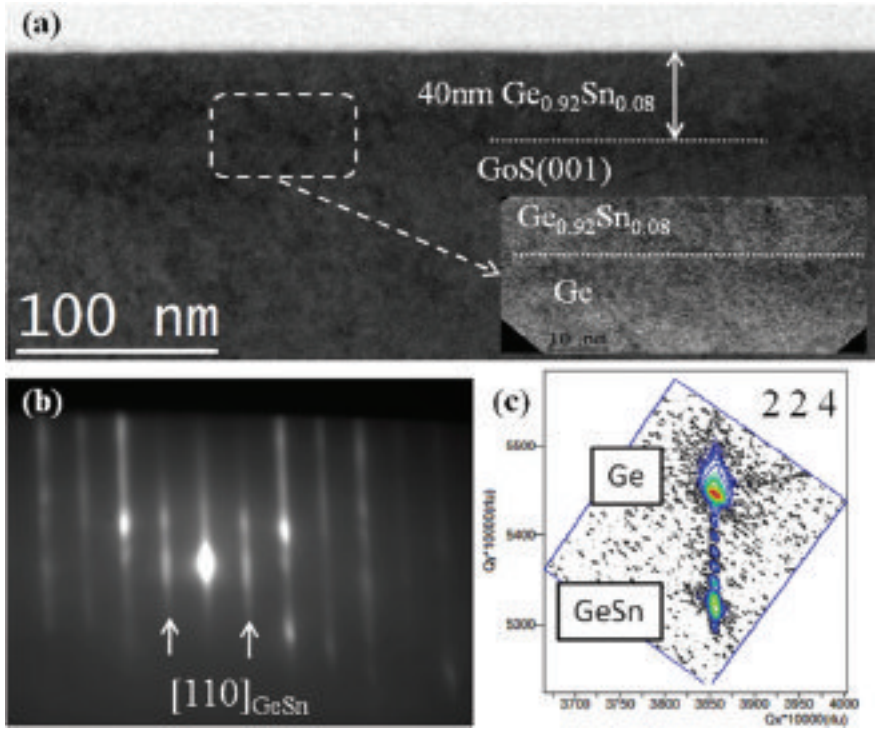

FIGURE 3. (a) Cross-section TEM of a 40 nm fully strained defect free GeSn layer on 1 lm Ge/Si buffer substrate with 8% Sn grown with AP-CVD using combination of Ge2H6 and SnCl4. (b) RHEED diagram of the Ge0.92Sn0.08 surface after deoxidation in UHV at 420°C. The pattern exhibits a strong (2x1) surface reconstruction along the [110]Ge direction. (c) (224) XRD-RSM of the 40 nm Ge0.92Sn0.08/Ge bilayer showing that GeSn is fully strained on Ge.

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IoT's Divergent Needs Will Drive Different Types of Technologies

Given the current buzz around the Internet of Things (IoT), it is easy to lose sight of the challenges – both economic and technical. On the economic side is the need to cost-effectively manufacture the trillions of sensors used to gather data, while on the technical side, the challenge involves building out the infrastructure. This includes enabling the transmission, storage, and analysis of volumes of data far exceeding anything we see today. These divergent needs will drive the semiconductor equipment industry to provide very different types of manufacturing solutions to support the IoT.

In order to fulfill the promise of the IoT, sensor technology will need to become nearly ubiquitous in our businesses, homes, electronic products, cars, and even our clothing. Per-unit costs for sensors will need to be kept very low to ensure the technology is economically viable. To support this need, trailing-edge semiconductor manufacturing capabilities provide a viable option since fully depreciated wafer processing equipment can produce chips cost efficiently. For semiconductor equipment suppliers, this translates into additional sales of refurbished and productivity-focused equipment and upgrades that improve yield, throughput, and running costs.

DAVE HEMKER, *Senior Vice President and Chief Technology Officer, Lam Research Corp.*

In addition to being produced inexpensively, sensors intended for use in the IoT will need to meet several criteria. First, they need to operate on very low amounts of power. In fact, some may even be self-powered via MEMS (micro-electromechanical systems)-based oscillators or the collection of environmental radio frequency energy, also known as energy harvesting/scavenging. Second, they will involve specialized functions, for example, the ability to monitor pH or humidity. Third, to enable the transmission of data collected to the supporting infrastructure, good wireless communications capabilities will be important. Finally, sensors will need to be small, easily integrated into other structures – such as a pane of glass, and available in new form factors – like flexible substrates for clothing. Together, these new requirements will drive innovation in chip technology across the semiconductor industry's ecosystem.

The infrastructure needed to support the IoT, in contrast, will require semiconductor performance to continue its historical advancement of doubling every 18-24 months. Here, the challenges are a result of the need for vast amounts of networking, storage in the Cloud, and big data analysis. Additionally, many uses for the IoT will involve risks far greater than those that exist in today's internet. With potential medical and transportation applications, for example, the results of data analysis performed in real time can literally be a matter of life or death. Likewise, managing the security and privacy of the data being generated will be paramount. The real-world nature of things also adds an enormous level of complexity in terms of predictive analysis.

Implementing these capabilities and infrastructure on the scale imagined in the IoT will require far more powerful memory and logic devices than are currently available. This need will drive the continued extension of Moore's Law and demand for advanced semiconductor manufacturing capability, such as atomic-scale wafer processing. Controlling manufacturing process variability will also become increasingly important to ensure that every device in the new, interconnected world operates as expected.

With development of the IoT, semiconductor equipment companies can look forward to opportunities beyond communications and computing, though the timing of its emergence is uncertain. For wafer processing equipment suppliers in particular, new markets for leading-edge systems used in the IoT infrastructure and productivity-focused upgrades for sensor manufacturing are expected to develop. ◆

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