Insights for Electro Ifacturing

High-aspect Ratio Cu Pillars P. 12

Practical Limits for Metallization Scaling

P. 20

Feed-forward Overlay Control P. 22

How Variations in Substrate Layers Impact Board-level Reliability P22

> Extension E DI

A

THE POVER of TVO.

two lasers | one station

higher efficiency greater flexibility lower cost of ownership

the X-280-ML Multi-laser Micromachining System

to learn more about how the IX-280-ML can benefit you call +1 (603) 518-3200 IPG Microsystems will be happy to set up an individual meeting to discuss specific projects in more detail or host product demonstrations at our facility in Manchester NH.

www.ipgphotonics.com

sales.ipgm@ipgphotonics.com

PHOTONICS

The Power to Transform[®]



Solid State TECHNOLOGY.

NOVEMBER/DECEMBER 2015 VOL. 58 NO. 8

Dr. Michael Liehr (left) of SUNY Polytechnic Institute's CNSE and Bala Haran (right) of IBM Research inspect a wafer of 7nm test chips.

FEATURES



PACKAGING | Variation in build-up substrate layer thicknesses and its impact on FCBGA BLR performance Subtleties in thicknesses between the alternating Cu metal and dielectric layers within a build-up substrate can impact BLR performance.



SOVER

performance. Texas Instruments, Dallas, TX

LITHOGRAPHY Advanced lithography and electroplating approach to form high-aspect ratio copper pillars

It is possible to fabricate copper pillars more than 100µm in height, with aspect ratios up to 6:1, using advanced packaging stepper lithography in conjunction with electroplating. *Keith Best, Rudolph Technologies, Wilmington, MA and Phillip Holmes, TEL NEXX, Billerica, MA*



INTERCONNECTS | Practical limits for metallization scaling in fabs

Beyond economic limits due to litho limitations, the inherent need for a physical barrier an electrical limit on the ability to scale.

Ed Korczynski, Senior Technical Editor



LITHOGRAPHY | Feed-forward overlay control in lithography processes using CGS

Feed-forward can be applied for controlling overlay error by using Coherent Gradient Sensing (CGS) data to reveal correlations between displacement variation and overlay variation. Doug Anberg and David M. Owen, Ultratech, San Jose, CA



PROCESS WATCH | The Most Expensive Defect; Part 2

Because yield and reliability defects stem from the same source, reducing the source of yield defects will have the side benefit of also reducing reliability defects. Increasing process steps and the tyranny of numbers. David W. Price and Douglas G. Sutherland, KLA-Tencor, Milpitas, CA



RELIABILITY When front-end-of-line and back-end-of-line reliability meet

Due to the further scaling and increasing complexity of transistors, the boundaries between back-end-of-line and frontend-of-line reliability research are gradually fading. Imec's team leaders Kristof Croes and Dimitri Linten give their vision on the future of reliability research.

COLUMNS

- 2 Editorial Are you ready for Industry 4.0? Pete Singer, Editor-in-Chief
- 10 Packaging GINTI's via-last backside TSVs, Phil Garrou, Contributing Editor
- **11 Semiconductors** Transistor-level challenges get squeaky wheel results, *Dr. Lianfeng Yang, ProPlus Design Solutions*
- 32 Industry Forum Security by Design, Chowdary Yanamadala, ChaoLogix

DEPARTMENTS

- 4 Web Exclusives
- 5 News
- 31 Ad Index



editorial

Are you ready for Industry 4.0?

The semiconductor industry is sure to benefit by the "digitization" of manufacturing in that it's an important component of the IoT explosion, along with smart homes, smart cities, smart health, etc. But is the semiconductor manufacturing industry – already one of the most advanced in the world – ready for the Industry 4.0 revolution? Will the cobbler's children get new shoes?

"There's a long way to go for the semiconductor industry to realize the kind of data sharing embodied in the Industry 4.0 concept."

I believe it will, but there are some major roadblocks that need to be overcome.

New innovation is required for a couple of reasons. First, the path to continued cost reduction through scaling has come to an end. The industry will continue to push to smaller dimensions and pack more functionality on a single chip because the world will always need superadvanced electronics for data servers, cloud computing and networking. But it's looking to be an increasingly expensive proposition. At the same time, the industry is looking to the Internet of Things explosion as the "next big thing." The two most important aspects of IoT devices will be low power and low cost. Speaking at a press conference at Semicon Europa in October, Rutger Wijburg, Senior VP and General Manager Fab Manufacturing for GlobalFoundries said a typical figure of merit in the mobile space is \$0.25/mm2. "My estimation is that the massive volume going into the Internet of Things has to be delivered for ASPs (average selling price) between \$0.05 and \$0.10/mm2," he said.

Could the Industry 4.0 movement enable a dramatic reduction in costs? Proponents say greater connectivity and information sharing — enabled by new capabilities in data analytics, remote monitoring and mobility — will lead to increased efficiency and reduced costs. There will also be greater efficiency across the supply chain.

Sadly, there's a long way to go for the semiconductor industry to realize the kind of data sharing and "digitization" embodied in the Industry 4.0 concept. The main challenge is that the semiconductor industry has been so secretive, especially when it comes to process recipes and yield data, that 4.0-type of data sharing is almost impossible. What's needed? A whole new strategy for looking at IP and deciding what is critical and what can be shared.

-Pete Singer, Editor-in-Chief

Solid State TECHNOLOGY.

Pete Singer, Editor-in-Chief Ph: 978.470.1806, psinger@extensionmedia.com

Shanon Davis, Editor, Digital Media Ph: 603.547.5309 sdavis@extensionmedia.com

Ed Korczynski, Senior Technical Editor, edk@extensionmedia.com

Jeff Dorsch, Contributing Editor

Phil Garrou, Contributing Editor

Dick James, Contributing Editor

Vivek Bakshi, Contributing Editor

Sara Ver-Bruggen, Contributing Editor, Semiconductor Manufacturing & Design CREATIVE/PRODUCTION/ONLINE LS Jerrett, Production Traffic Coordinator Nicky Jacobson, Senior Graphic Designer Simone Bradley, Graphic Designer Slava Dotsenko, Senior Web Developer Jon Franke, Media Coordinator

MARKETING/CIRCULATION Jenna Johnson, jjohnson@extensionmedia.com

CORPORATE OFFICERS

Extension Media, LLC Vince Ridley, President and Publisher vridlev@extensionmedia.com

Clair Bright, Vice President and Publisher Embedded Electronics Media Group cbright@extensionmedia.com

Melissa Sterling, Vice President, Business Development msterling@extensionmedia.com

For subscription inquiries

Tel: 847.559.7500; Fax: 847.291.4816; Customer Service e-mail: sst@omeda.com; Subscribe: www.sst-subscribe.com

Solid State Technology is published eight times a year by Extension Media LLC, 1786 Street, San Francisco, CA 94107. Copyright © 2015 by Extension Media LLC. All rights reserved. Printed in the U.S.



1786 18th Street San Francisco, CA 94107

November/December 2015, VOL. 58 NO. 8 • *Solid State Technology* ©2015 (ISSN 0038-111X) *Subscriptions:* Domestic: one year: \$258.00, two years: \$413.00; one year Canada/Mexico: \$360.00, two years: \$573.00; one-year international airmaii: \$434.00, two years: \$681.00; Single copy price: \$15.00 in the US, and \$20.00 elsewhere. Digital distribution: \$130.00. You will continue to receive your subscription free of charge. This fee is only for air mail delivery. Address correspondence regarding subscriptions (including change of address) to: *Solid State Technology*, 1786 18th Street, San Francisco, CA 94107-2343. (8 am – 5 pm, PST).



Conference & Networking Event

MEET OUR NEW ADVISORY BOARD MEMBERS



Robert Cappel KLA-Tencor



Dr. Bill Chen ASE



L.T. Guttadauro Fab Owners Association



Dr. Li Li Cisco Systems



Dr. Pinyen Lin G450C and TSMC



Ariel Meyuhas The MAX Group



Dr. Gary Patton GLOBALFOUNDRIES



Elton Peace Lam Research www.theconfab.com

REGISTRATION IS OPEN Register by Dec. 31st to Save!



2016 CONFERENCE TOPICS

How the IoT is Driving the Semiconductor Industry

Filling the Fabs of the Future: A Guide to Hot New Applications

MEMS Sensor Fusion and More then Moore

The Limits of Scaling: Understanding the Challenges of sub-10nm Manufacturing

Fabless, Foundries and OSATs: Optimizing the Supply Chain

System Integration, Advanced Packaging and 3D Integration: How They All Fit Together

China's New Role in the Global Semiconductor Industry

The Impact of Continued Consolidation Across the Supply Chain

Wearables and Bioelectronics: The Cusp of a Revolution?

Tackling Rising R&D Costs in the Semiconductor Industry

Register by Dec. 31st to Save on Your Total Access Pass



www.theconfab.com

Produced by: Extension MEDIA

Online@www.solid-state.com

Web Exclusives

Slideshow: 2015 IEDM Preview

This year marks the 61st annual IEEE International Electron Devices Meeting (IEDM). As usual, Solid State Technology will be reporting insights from bloggers and industry partners during the conference. This slideshow provides an advance look at some of the most newsworthy topics and papers that will be presented at this year's meeting, which will be held at the Washington, D.C. Hilton from December 7-9, 2015.

http://bit.ly/1kriYi2

Historic era of consolidation for chip makers

One thing seems clear about the semiconductor market: consolidation is showing no signs of slowing down. To help readers follow this constantly changing situation, Solid State Technology is keeping a running scorecard of all the significant transactions in the semiconductor market here.

http://bit.ly/10GbKTT

2015 Source Workshop – What we expect to hear

EUV Sources remain the key enabler to move EUVL into manufacturing, and we look forward to the upcoming 2015 Source Workshop (November 9-11, 2015, Dublin, Ireland) for the latest developments and status of EUV Source technology. Both high-volume manufacturing (HVM) level and metrology EUV sources are needed for chip manufacturing using EUVL. For HVM sources, power level and availability are needed to generate cost effective throughput. We expect to hear from the user (Intel) as well as source makers (ASML and Gigaphoton) on the latest performance of these sources.

http://bit.ly/1Y6ulKt

ARM CEO celebrates 500 years of connectivity

"Realize that everything connects to everything else," Leonardo da Vinci said some five centuries ago. Simon Segars, chief executive officer of ARM Holdings, took that quotation as the theme for his ARM TechCon keynote address on Wednesday morning (November 11), which was entitled "Building Trust in a

Connected World." (From SemiMD) http://bit.ly/1NsZEaC

MEMS, sensors poised for growth in the Internet of Things era

The microelectromechanical system (MEMS) devices and sensors market is evolving as demand for low-power connected devices continues to rise. The Internet of Things has MEMS/sensors vendors somewhat giddy about growth prospects, yet veteran executives realize the victories will go to the suppliers with

the lowest cost of manufacturing and the best prices. (From SemiMD) **http://bit.ly/1GYmSJc**



Is the semiconductor industry ready for Industry 4.0 and the IIoT?

An industrial revolution is in the making, equivalent some say to the introduction of steam power at the tail end of the 18th century. Known as smart manufacturing, Industry 4.0 (after the German initiative Industrie 4.0), the industrial internet of things (IIoT), or simply the fourth industrial revolution, the movement will radically change how manufacturing is done. http://bit.ly/1PDYLk4

Insights from the Leading Edge: IMPACT Taiwan 2015 – Altera, iNEMI, SPIL

The IMPACT conference claims to be the largest gathering of packaging and PCB professionals in Taiwan. It is organized by IEEE CPMT, ITRI, IMAPS Taiwan and the Taiwan Printed Circuit Association. The Technical Chair for IMPACT 2015 is CT Liu, of ITRI. Contributing Editor Phil Garrou reviews conference presentations in this blog post. http://bit.ly/1WONK5d

Check out the finalists for MEMS & Sensors Technology Showcase at MEMS Executive Congress 2015

Karen Lightman, Executive Director of the MEMS Industry Group, gives readers a review and insider's perspective on the products shown at the MEMS & Sensors Technology Showcase at the 11th Annual MEMS Executive Congress 2015 on November 4.

http://bit.ly/1LbMc9l

Nowhere near room temp superconductors

On-chip metal interconnects limit IC speed in many advanced design today, and with signal delay proportional to the product of the resistance (R) of wires and the capacitance (C) of dielectric insulation, wires with R lower than that of copper (Cu) metal would significantly improve IC performance. We know of superconductors materials with zero resistance to electrical current flow but only at "critical temperature" (Tc) well below 77°K, and so there has been an ongoing quest by scientists to find a material with Tc above room temperature of 298°K. (From SemiMD)

http://bit.ly/1MM9pjA

It's all about packaging – in this material world, who is your partner?

With the recent release of Apple's 6s and the form factors of internet enabled mobile devices and the emergence of the IoT (Internet of Things), advanced packaging is clearly the enabling technology providing solutions for mobile applications and for semiconductor devices fabricated at 16nm and below process nodes. SEMI and TechSearch International are once again partnering to prepare a comprehensive market analysis of how the current packaging technology trend will impact the packaging manufacturing materials demand and market. http://bit.ly/1MZ2Nol

Please send news articles to sdavis@extensionmedia.com

worldnews

USA - GlobalFoundries announced the availability of FX-14, an applicationspecific integrated circuit offering built on the company's next-generation 14nm FinFET process technology.

EUROPE - imec and CMST unveiled the development of a novel technology for thermoplastically deformable electronics enabling low-cost 2.5D free-form rigid electronic objects.

USA - FEI announced agreement to acquire DCG Systems, Inc.

ASIA - Toshiba announced the sale of its image sensor business to Sony.

USA - IMT announced a partnership with Silicon Catalyst to provide MEMS technology and manufacturing.

EUROPE - CEA-Leti announced that it has joined the GLOBALSOLUTIONS ecosystem as an ASIC provider, specifically to support **GLOBALFOUNDRIES' 22FDX** technology platform.

ASIA - Applied Materials, Inc. announced it plans to establish a new R&D laboratory in Singapore in collaboration with A*STAR. The S\$150 million joint investment will focus on developing advanced semiconductor technology to fabricate future generations of logic and memory chips.

USA - Soraa announced that it will open a new semiconductor fabrication plant in Syracuse, New York.

ASIA - Tsinghua Unigroup Ltd., a Chinese government-owned chipmaker, will make a \$600 million investment in Powertech Technology of Taiwan.

USA - Ultratech introduced superfast 4G+ low-cost in-line inspection system for patterned wafers.



Reports: TI, STMicro to add to semiconductor acquisitions spree

One thing seems clear about the semiconductor market: consolidation is showing no signs of slowing down.

On the heels of two additional acquisitions in the space around semiconductors LAM Research acquiring KLA-Tencor and Western Digital buying SanDisk - rumors have abounded this week that there is more to come.

First, Bloomberg reported that Texas Instruments, the world's largest maker of analog chips, is in talks to buy Maxim Integrated. TI is said to have competition for Maxim from a competitor in the analog chip space, Analog Devices.

According to the Bloomberg report, Maxim may be holding out for a hefty premium, if it does, in fact, sell.

"When asked on an Oct. 22 conference call about a possible takeover by a larger company such as Texas Instruments, Maxim Chief Financial Officer Bruce Kiddoo said the company is big enough and profitable enough to survive on its own," Bloomberg reported. "Maxim also has the resources to do its own acquisitions," he said.

Arrownied	Balag Salid or Acquisition Target*	Barger	Purchase Price (SWG)	Yape of Transaction	Throng of Purchase
April any	Silicon Image (M/83	Lamine (M. 6.)	SAUE	Gash.	Completer
February	Laintig Otiermanal	terrent Eld S.B.	1944	thick;	Completeid
February	Entropic Contrinundantians (U.S.)	Mandument (NJ 5.1	1287	Carls & Shiek	Completed
March	freescale (U.S.)	NOP Pietherlandsi	\$11,800	Cash & Stock	2415
March	Write saw (bulls 3	Microsofti (u) 5.3	\$349	Call	Completed
Manuh	(BM (V.B.)	Uphill Investment (China)	1731	Cash	9009
depend	Constitutions (U.S.)	Has Capital, investors (China)	\$1,900	Cash	By 5494
May	INARCENT PULS 3	Microchip (MS-)	58.99	Canth an Sames	Completeid
May	Broadian (U.S.)	Avago Chingspond	\$87,000	Carb & Noch	Ro Apr. 2018
intray .	tast of power seet (Actionization)	and Capital Divising	\$4,800	Rack.	2155
(Aurilean)	Alberta 0.2 3.2	1 mile 1 (01.0.0	34.0,700	-Carb	No only 2218
daring.	Caseman Invaluances (CLULE)	Panaste Technologies (Talacard)	63-00	Cash	9006
Status .	Mictory* 2015.3	Tuingheat Unignousy (Dhina)	\$23,000	-Cash-	Proposed
(Autor)	MACOM subamotive on # 10.5.5	Autoini (Sweden)	\$300	Carb	By Sept. 2025
July .	100P CM05 sensor unit (Notherlands)	AMD (Awarris)	19.4	TNA.	Completed
Instantos	ASHIELDU S.1	Distant R/K)	54,600	Carls & Stock	1006
The second secon	of coffeet many located int make 20024			which party and state	Frank int. Doors

Semiconductor Market Consolidation. (Slide from: Dr. Rutger Wijburg, Sr. Vice President and General Manager, GLOBALFOUNDRIES; keynote at Semicon Europa)

Lam Research to acquire KLA-Tencor

Lam Research Corporation (LRCX) and "This is just what the doctor ordered," Srini KLA-Tencor Corporation (KLAC) announced that they have entered into a definitive agreement for Lam Research to acquire all outstanding KLA-Tencor shares in a cash and stock transaction. The move, unanimously approved by the boards of directors of both companies, will create a combined company with approximately \$8.7 billion in pro forma annual revenue.

The combined company expects to realize \$250 million in cost savings within 18 to 24 months of closing, and anticipates gaining approximately \$600 million in incremental revenue by 2020 through improved differentiation of each company's products and creation of new capabilities.

Sundararajan, Semiconductor and Semicaps Analyst for W.R. Hambrecht + Co./Summit Research, wrote in an analysis of the move. "It removes excessive dependence of LRCX on memory and excessive dependence of KLAC on foundry/logic."

According to the LRCX press release, "the combination will create unmatched capability in process and process control, delivering optimized results in partnership with its customers by reducing variability and accelerating yield, ultimately helping the semiconductor industry extend Moore's Law and performance scaling generally."

"The pairing of Lam Research and KLA-Tencor brings industry leadership in process and

Continued on page 8

Continued on page 8

GLOBALFOUNDRIES achieves 14nm finFET technology success for next-generation AMD products

GLOBALFOUNDRIES announced it has demonstrated silicon success on the first AMD products using GLOBALFOUNDRIES' most advanced 14nm FinFET process technology. As a result of this milestone, GLOBALFOUNDRIES' silicon-proven technology is planned to be integrated into multiple AMD products that address the growing need for high-performance, power-efficient compute and graphics technologies across a broad set of applications, from personal computers to data centers to immersive computing devices.

AMD has taped out multiple products using GLOBALFOUNDRIES' 14nm Low Power Plus (14LPP) process technology and is currently conducting validation work on 14LPP production samples. Today's announcement represents another significant milestone towards reaching full production readiness of GLOBALFOUNDRIES' 14LPP process technology, which will reach high-volume production in 2016. The 14LPP platform taps the benefits of three-dimensional, fully-depleted FinFET transistors to enable customers like AMD to deliver more processing power in a smaller footprint for applications that demand the ultimate in performance.

"FinFET technology is expected to play a critical foundational role across multiple AMD product lines, starting in 2016," said Mark Papermaster, senior vice president and chief technology officer at AMD. "GLOBALFOUNDRIES has worked tirelessly to reach this key milestone on its 14LPP process. We look forward to GLOBALFOUNDRIES' continued progress towards full production readiness and expect to leverage the advanced 14LPP process technology across a broad set of our CPU, APU, and GPU products."

"Our 14nm FinFET technology is among the most advanced in the industry, offering an ideal solution for demanding high-volume, high-performance, and power-efficient designs with the best die size," said Mike Cadigan, senior vice president of product management at GLOBALFOUNDRIES. "Through our close design-technology partnership with AMD, we can help them deliver products with a performance boost over 28nm technology, while maintaining a superior power footprint and providing a true cost advantage due to significant area scaling."

GLOBALFOUNDRIES' 14LPP FinFET is ramping with production-ready yields and excellent model-to-hardware correlation at its Fab 8 facility in New York. In January, the early-access version of the technology (14LPE) was successfully qualified for volume production, while achieving yield targets on lead customer products. The performance-enhanced version of the technology (14LPP) was qualified in the third quarter of 2015, with the early ramp occurring in the fourth quarter of 2015 and full-scale production set for 2016.

Light goes infinitely fast with new on-chip material

Electrons are so 20th century. In the 21st century, photonic devices, which use light to transport large amounts of information quickly, will enhance or even replace the electronic devices that are ubiquitous in our lives today. But there's a step needed before optical connections can be integrated into telecommunications systems and computers: researchers need to make it easier to manipulate light at the nanoscale.

Researchers at the Harvard John A. Paulson School of Engineering and Applied Sciences (SEAS) have done just that, designing the first on-chip metamaterial with a refractive index of zero, meaning that the phase of light can travel infinitely fast.

This new metamaterial was developed in the lab of Eric Mazur, the Balkanski Professor of Physics and Applied Physics and Area Dean for Applied Physics at SEAS, and is described in the journal Nature Photonics.



In this zero-index material there is no phase advance, instead it creates a constant phase, stretching out in infinitely long wavelengths. (Credit: Peter Allen, Harvard SEAS)

"Light doesn't typically like to be squeezed or manipulated but this metamaterial permits you to manipulate light from one chip to another, to squeeze, bend, twist and reduce diameter of a beam from the macroscale to the nanoscale," said Mazur. "It's a remarkable new way to manipulate light."

Although this infinitely high velocity sounds like it breaks the rule of relativity, it doesn't. Nothing in the universe travels faster than light carrying information — Einstein is still right about that. But light has another speed, measured by how fast the crests of a wavelength move, known as phase velocity. This speed of light increases or decreases depending on the material it's moving through.

When light passes through water, for example, its phase velocity is reduced as its wavelengths get squished together. Once it exits the water, its phase velocity increases again as its wavelength elongates. How much the crests of a light wave slow down in a material is expressed as a ratio called the refraction index — the higher the index, the more the material interferes with the propagation of the wave crests of light. Water, for example, has a refraction index of about 1.3.

When the refraction index is reduced to zero, really weird and interesting things start to happen.

In a zero-index material, there is no phase advance, meaning light no longer behaves as a moving wave, traveling through space in a series of crests and troughs. Instead, the zero-index material creates a constant phase — all crests or all troughs — stretching out in infinitely long wavelengths. The crests and troughs oscillate only as a variable of time, not space.

This uniform phase allows the light to be stretched or squished, twisted or turned, without losing energy. A zero-index material that fits on a chip could have exciting applications, especially in the world of quantum computing.

"Integrated photonic circuits are hampered by weak and inefficient optical energy confinement in standard silicon waveguides," said Yang Li, a postdoctoral fellow in the Mazur Group and first author on the paper. "This zero-index metamaterial offers a solution for the confinement of electromagnetic energy in different waveguide configurations because its high internal phase velocity produces full transmission, regardless of how the material is configured."

The metamaterial consists of silicon pillar arrays embedded in a polymer matrix and clad in gold film. It can couple to silicon waveguides to interface with standard integrated photonic components and chips. "In quantum optics, the lack of phase advance would allow quantum emitters in a zero-index cavity or waveguide to emit photons which are always in phase with one another," said Philip Munoz, a graduate student in the Mazur lab and co-author on the paper. "It could also improve entanglement between quantum bits, as incoming waves of light are effectively spread out and infinitely long, enabling even distant particles to be entangled."

"This on-chip metamaterial opens the door to exploring the physics of zero index and its applications in integrated optics," said Mazur.

The paper was co-authored by Shota Kita, Orad Reshef, Daryl I. Vulis, Mei Yin and Marko Loncar, the Tiantsai Lin Professor of Electrical Engineering.

YES-VERTA SERIES PROCESS OVENS



For Demanding MEMS & Semiconductor Applications

VertaCURE - Curing Polyimide/PBO/BCB

VertaCOAT - Deposition Chemical Vapor Phase for Adhesion Promotion or Anti-Stiction Layers

VertaVAC - High Vacuum Vacuum Packaged MEMS Outgassing



www.yieldengineering.com

newscont

Reports: TI, STMicro, Continued from page 5

For Texas Instruments' part, CFO Kevin March weighed in on potential acquisitions on October 21. Bloomberg quotes him as saying: "If we were to look at an acquisition, it would probably be a company that's going to be broad in catalog, have a diverse customer base, have a large percentage of its revenue coming from industrial and automotive, probably have a very talented R&D team. So we really do focus on the numbers that that acquisition might lead us to."

Following the Bloomberg story, the Chicago Tribune issued a report saying STMicroelectronics is considering a bid for Fairchild Semiconductor. STMicro is Europe's biggest chipmaker, and would be looking to "increase growth and shore up its digital products business" with the purchase, according to the report.

For its part, Fairchild, which is one of the oldest chipmakers in the US, has hired Goldman Sachs to help it find a buyer. In recent months the company has conducted talks with ON Semicondor and Infineon Technologies about being purchased, according to the Tribune.

It is still uncertain whether anything will come of either report, but it seems clear that the merger madness in the semiconductor industry is far from over.

To help readers follow this constantly changing situation, Solid State Technology is keeping a running scorecard of all the significant transactions in the semiconductor market, available here: http://bit.ly/10GbKTT.

Lam Research, Continued from page 5

process control together, accelerating our capability to address our customers' most difficult challenges as they scale to meet the market demands of lower power, higher performance, and smaller form factors," said Martin Anstice, Lam's president and chief executive officer. "Lam Research and KLA-Tencor's shared commitment to collaboration and building strong customer trust, along with our respective track records of innovation, product leadership, and operational excellence, position us as a combined company to deliver the higher levels of technology differentiation and speed to solutions that are critical to our customers' long-term success."

"I strongly believe that this transaction represents a great outcome for all of KLA-Tencor's key stakeholders," said Rick Wallace, president and chief executive officer of KLA-Tencor. "The combined company will be uniquely positioned to work collaboratively with our customers to help them meet the challenges of FinFET, multipatterning and 3D NAND development. Given the complementary nature of the two companies' product offerings and technologies as well as the lack of product overlap, the combination will create an industry leader with greater opportunities for our respective employees for professional development and growth. Lastly, this transaction will benefit our stockholders who will receive compelling upfront value, in addition to the opportunity to own a meaningful stake in an industry leader and participate in the upside potential created by the combination."

According to the press release, the transaction is expected to close in mid-calendar year 2016, pending customary regulatory approvals. The transaction is also subject to customary closing conditions, including the adoption by KLA-Tencor's stockholders of the merger agreement and the approval by Lam Research's stockholders of the issuance of shares in the transaction. Given their complementary product lines and the industry benefits the transaction will enable, the companies believe that they will be able to obtain the requisite regulatory approvals on a timely basis. Analyst Sundararajan agrees: "We expect minimal opposition to this deal from the various jurisdictions, rather easily handled."

However, Robert Maire of Semiconductor Advisors thinks approval could potentially be more difficult. "We think this is going to be the obvious biggest issue after the failed AMAT & TEL merger. We think there will likely be opposition in the semi industry but probably less so than we heard the screaming related to AMAT/TEL," he wrote. "While maybe not overjoyed, the combination makes a lot of sense for customers and feels a lot less negative than the failed AMAT/TEL."

According to the press release, some of the benefits the combined company expects to see are:

- Creates Premier Semiconductor Capital Equipment Company: Strengthened platform for continued outperformance, combining Lam's best-in-class capabilities in deposition, etch, and clean with KLA-Tencor's leadership in inspection and metrology
- Accelerated Innovation: Increased opportunity and capability to address customers' escalating technical and economic challenges
- Broadened Market Relevance: Comprehensive and complementary presence across market segments provides diversity, scale and value creating innovation opportunities
- Significant Cost and Revenue Synergies: Approximately \$250 million in expected annual on-going pre-tax cost synergies within 18-24 months of closing the transaction, and \$600 million in annual revenue synergies by 2020
- Accretive Transaction: Increased non-GAAP EPS and free cash flow per share during the first 12 months post-closing
- Strong Cash Flow: Complementary memory and logic customer base, operational strength, and meaningful installed base revenues strengthen cash generation capability

According to Sundararajan, the move could have negative impacts for some other companies in the industry. "This deal is quite negative for Applied Materials (AMAT) and Hermes Microvision and perhaps for ASML also," he wrote. "In the case of AMAT, their process diagnostics and control division being based in Israel does not allow of meshing of capabilities, and product synergies really don't exist. In the case of Hermes Microvision, since etch is the pre-dominant user of e-beam inspection due to testing of contacts, a combination of KLAC and LRCX with both e-beam and etch capabilities can be lethal."

Maire also foresees difficulties for competitors: "The combined LAM and KLA creates a powerhouse in the semicap industry, which is looking a lot more like a duopoly."

Lam president and CEO Anstice concluded, "We have tremendous respect for the company KLA-Tencor employees have built over nearly 40 years — their culture, technology, and operating practices. I have no doubt that our combined values, focus on the customer, and complementary technologies will create a trusted leader in our industry, capable of creating significant opportunity for profitable growth and in turn delivering tremendous value to all of our stakeholders. This is the right time for the right combination in our industry."

A MEASURE OF CONFIDENCE

Particle Counting Solutions for Cleanroom Environments

The smallest particles have the ability to cause big issues in cleanroom environments. TSI has dedicated over 45 years to measuring these small particles and providing measurement solutions trusted by national and standards labs worldwide. Whether you are certifying a cleanroom, monitoring a process or tracking down a root cause, TSI offers a suite of products that ensure you get the perfect measurement – every time, all the time.

TSI particle counting solutions include:

- + Handheld, Portable and Remote Particle Counters
- + Accurate detection down to 0.100 μm at 1 CFM
- + Facility Monitoring Systems

Learn more at tsi.com/electronics



UNDERSTANDING, ACCELERATED



GINTI's via-last backside TSVs

One of the plenary presentations at this year's IEEE 3DIC conference was "Advanced 2.5D/3D Hetero-Integration Technologies at GINTI, Tohoku University" by KW Lee, Koyanagi-san and co-workers, detailing the activities at the University and the prototyping spin-out.

The Global Integration Initiative (GINTI) is 8/12-inch R&D foundry fab for the R&D of 2.5D/3D integration technologies and applications. GINTI provides a process development infrastructure in a manufacturing-like fab environment and "low cost", prototyping of proof of concepts using commercial/customized 2D chip/wafer, and a base-line process.

State-of-the technologies include design, layout and mask making to wafer thinning, forming of TSV on chip/wafer (front side/backside TSV), redistribution routing, both side micro-bump formation, chip/wafer stacking, failure analysis, and reliability testing.



FIGURE 1.

GINTI can provide 3D prototype LSI stacking using commercial 2D chips by die-level 3D hetero-integration, backside TSV formation and various stacking (C2C C2W, W2W, and self-assembly) technologies.

GINTI mainly focuses on a via-last backside TSV approach, because they feel it is a better solution for heterogeneously integrating different function, size,

Packaging



and material devices, with better flexibility for commercial chip/ wafers.

PHIL GARROU, Contributing Editor

Their process flow for via-last backside TSV fabrication is shown in **FIGURE 1**. The incoming LSI device wafer with metal bumps is temporarily bonded onto a support wafer. Then the Si substrate is thinned to target thickness from the backside by grinding and CMP. After via patterning on the ground surface, the deep Si trench is formed from the backside by RIE processing until the first level metallization layer (M1) is exposed. Oxide liner is deposited into via holes and the bottom oxide liner in via hole is selectively etched by dry etching to re-expose the M1 layer. Next, the deep trench is filled with Cu by electroplating after dep of barrier and seed metal layers. Re-distribution layer (RDL) is then formed on the backside and metal bumps are formed on the RDL by electroplating. Finally, the support wafer is de-bonded from the thinned LSI wafer.

To create new 3D hetero-integrated systems they have developed die-level 3D integration technology. Commercially available 2D chips with different functions and sizes such as those of sensor, logic, and memories which were fabricated by different technologies, are processed to form TSVs and metal micro-bumps and integrated to form a 3D stacked chip in die level. **FIGURE 2** shows a 3D stacked image sensor chip comprising three layers of CIS, CDS, and ADC chips for high speed image sensor system. ◆



FIGURE 2.

Transistor-level challenges get squeaky wheel results

The squeaky wheel gets the grease, or so it seems in the semiconductor industry, as the high level of the design process seems to get the most attention. Meanwhile, the transistor level appears to have been largely forgotten.

With increasing complexities and scale of electronic system, design and verification have moved up the abstraction level from register transfer level (RTL) to the electronic system level (ESL) with help from high-level synthesis software and other new EDA technologies. Portable stimulus is available at ESL to test specifications and virtual platforms enable early software consideration, for example.

Throughout, transistor-level challenges are ongoing but appear to be largely forgotten. New process technologies, such as FinFET, increasingly stress transistor-level verification tools, in particular, SPICE and FastSPICE simulators, and designer needs are greater. Highly accurate and reliable verification and sign-off tools for large post-layout simulation is one of many.

When designers move to 16/14 nanometer and beyond with FinFETs, accuracy is a priority and essential for characterization, verification and signoff, due to reduced Vdd and the impact of process variations. Device characteristics and physical behavior is more complicated with these process nodes. Circuit size is increasing and design margins are shrinking. Every aspect that contributes to leakage and power must be measured and accurately modeled. The entire circuit, including all parasitic components, has to be simulated accurately.

While circuit designers may not be squeaky wheels, they do need to be confident of their designs, as they're under the pressure from ever-increasing design and manufacturing complexities and cost. FastSPICE simulators used in final verification and signoff do not offer enough accuracy. This is true for small currents critical to low-power design and achieving sufficient noise margins. Often, FastSPICE simulations rely on special, fine-tuned options and start with non-converged DC, further challenging accuracy.

Semiconductors



Designers use FastSPICE to verify timing and power before tapeout. Unfortunately, they can't be sure of the results, risk expensive respins and missing market windows, for



VP of Marketing, ProPlus Design

applications sensitive to small current or noise elements, such as advanced memory designs. This is an all-toofamiliar scenario where wheels should be squeaking.

What sends the situation out of control is FastSPICE's lack of a golden to refer. FastSPICE provides many options for designer to tune to trade-off accuracy and speed, which worked in past generations. Such an option tuning strategy, however, becomes unreliable for advanced designs where designers have much less design margin than before. Designers now see more and more failure or inaccurate cases due to fundamental accuracy limitations of FastSPICE.

Traditional SPICE simulators were the "golden" simulator to validate FastSPICE, but only for small blocks as no commercially available SPICE simulator can offer simulation capacity for verification and signoff that FastSPICE used. And such validation can't automatically scale up. The circuit size continues to increase and giga-scale designs are common. At 16nm and beyond, 3D device structures add greater capacity and accuracy challenges. FastSPICE simply doesn't offer enough confidence and may introduce unpredictably inaccurate or wrong verification results, which designers don't want to risk for tapeout.

Well, circuit designers may not be squeaking, but help is on the way nevertheless. A new type of SPICE simulator known as giga-scale SPICE simulators or GigaSpice, is able to support giga-scale circuit simulation and verification with a pure SPICE engine. It features SPICE accuracy and FastSPICE-like capacity and performance through advanced parallelization technology. It does not require option tuning and always converges on DC, making it easy for designers to adopt and offering accurate and reliable results for designers. GigaSpice can be a golden reference for FastSPICE and a replacement for memory characterization, large block simulation and full-chip verification.

The squeaky wheel may be noisy, but a few clever developers have been paying attention to the new developments for transistor-level verification and signoff and are responding. Giga-scale SPICE simulators are fast becoming part of circuit-level design flows for squeaky wheel results. \blacklozenge

PACKAGING

Variation in build-up substrate layer thicknesses and its impact on FCBGA BLR performance

JAIMAL WILLIAMSON, Texas Instruments, Dallas, TX

Subtleties in thicknesses between the alternating Cu metal and dielectric layers within a build-up substrate can impact BLR performance.

anaging an organization in an orderly and disciplined manner is known as "running a tight ship." This mentality and discipline cannot be understated with build-up substrate supplier capability and manufacturing tolerances as it relates reliability and margin in a flip chip ball grid array (FCBGA) device. Build-up substrate technology is the backbone for flip chip packaging due to its ability to bridge high density interconnects and functionality enabling improved electrical performance in tandem with the semiconductor chip. Alternating metal and dielectric layers build up the substrate into the final composite structure. The range of thicknesses of the aforementioned metal and dielectric layers are dependent on associated substrate manufacturer design rules, which can have an impact on board level reliability (BLR). Having a keen awareness of substrate supplier design rules can aid not only troubleshooting, but improve understanding of reliability margin from a chip to package interaction standpoint for any array of commercial and automotive FCBGA applications.

Influence of copper and dielectric layers on reliability

To better understand the thickness variation impact of bottommost substrate copper (Cu) metal (15 +/- 5μ m) and dielectric (30 +/- 6μ m) layers as it relates to strain energy density of BGA solder joint at die shadow area

and package corner, a 3x3 factorial design of experiments (DoE) approach (**FIGURE 1**) was pursued. Through the use of finite elemental modeling, outputs of the study included both strain energy density under -40°C to 125°C and 0°C to 100°C BLR temperature cycle conditions and changes in coefficient of thermal expansion (CTE) as Cu metal and dielectric thicknesses varied. For the remainder of the article, results from the more stringent -40°C to 125°C BLR temperature cycle condition will be discussed.

Leg #	Pattern	Cu thickness	ABF dielectric thickness
1	21	15	24
2	11	10	24
3	33	20	36
4	22	15	30
5	13	10	38
8	32	20	30
7	31	20	24
8	12	10	30
9	23	15	36

FIGURE 1. 3x3 factorial DoE.

Rationale of the study was based on a striking difference in BLR performance from two FCBGA daisy chain test vehicles having an identical substrate design, but manufactured at two different substrate suppliers (noted as supplier A and B in this article). The FCBGA daisy chain

JAIMAL WILLIAMSON is a packaging engineer responsible for development and qualification of Embedding Processing FCBGA devices within Texas Instruments' Worldwide Semiconductor Packaging group.





FIGURE 2. Example of FCBGA package.

test vehicle comprises the following package attributes (see **FIGURE 2** for a side view example):

- 40mm x 40mm body size
- 8-layer build-up stack (3/2/3)
- 400µm core thickness
- 1mm BGA pitch

Weibull analysis was generated from empirical BLR results at 5 percent and 63.2 percent cycles to failure. Specifically, at 5 percent cycles to failure supplier A exhibits ~25 percent reduced BGA solder joint fatigue life than counterparts from supplier B (as illustrated in **FIGURES 3** and **4**).

In a similar study focusing on component level reliability (CLR), it was observed that bottommost substrate Cu layer thickness can impact stress underneath die shadow area. For these reasons, a more detailed examination was done to measure bottommost substrate Cu layer thickness from daisy chain units of suppliers A and B. Based on package construction analysis, supplier A was found to target the nominal value of 15μ m; whereas supplier B targeted the high end of specification at 20μ m. These Cu thickness differences would play a significant role in the BLR results.



FIGURE 3. Weibull plot of supplier A.



FIGURE 4. Weibull plot of supplier B.

Stress modeling results

Outputs of the finite elemental modeling are revealed in FIGURE 5 based on inputs from the aforementioned 3x3 factorial DoE illustrated in Fig. 1. Based on the combination of various Cu and dielectric layer thicknesses evaluated, thicker dielectric and Cu layers yield higher macroscopic CTE values. This is an expected trend based on CTE material properties of Cu and dielectric layers in relation to the substrate core material. Simulation results confirmed CTE in ascending order is: dielectric layer > Cu layer > substrate core. Comparing Weibull analysis from supplier A and B (figures 3 and 4), DoE legs 4 and 6 match best, respectively, to the empirical BLR results. In addition, DoE legs 4 and 6 align with the bottommost substrate Cu layer thickness values from the aforementioned package construction analysis measurements. It is noted that based on modeling results, an approximately 2 percent change in CTE can swing the cycles to failure at 63.2 percent by ~11 percent. DoE leg 4 focuses on nominal Cu thickness of 15µm; whereas leg 6 focuses on the high end of the Cu thickness tolerance at 20µm. Dielectric thickness is nominal value of $30\mu m$ in both DoE cases. Improved BLR performance from supplier B is attributed to the thicker Cu providing a better CTE match to the BLR test board.

Use of JMP for statistical perspective

As a supplemental tool for data interpretation, JMP statistical analysis was performed to illustrate how nominal and extreme values of the metal and dielectric layer thickness specification affect FCBGA BLR perfor-

mance. Analyzing the strain energy data outputs, the model fit well to the predicted values as shown in **FIGURE 6.** Similarly, CTE correlated well with predicted values as illustrated in **FIGURE 7.** Use of the prediction profiler function, as illustrated in **FIGURE 8**, shows CTE is proportional to increase in metal and dielectric thickness, which correlates with the stress modeling results.

De£ leg≢	Cu thick name	ABP mickness jan	Simulation results			
			40-C to 125-C			
			Strain energy density	63.2% fair	CTE	
4	15	24	0.268	5,493	13.24	
2	10	24	4.307	1.373	12.82	
8	20	21	0.249	2,028	34,82	
4	15	30	0.278	1,685	13.52	
\$	10	36	0.284	1,744	13.52	
6	20	30	0.260	1,812	19.77	
1	20	24	0.272	1.811	13.51	
8	10	30	0.786	1,550	13.23	
	15	26	9.265	1,889	13,79	

FIGURE 5. Finite elemental modeling results.

Summary

Subtleties in thicknesses between the alternating Cu metal and dielectric layers within a build-up substrate can impact BLR performance. Two identical daisy chain substrate designs manufactured by different suppliers were compared head to head. A detailed package construction analysis revealed differences in bottommost Cu thickness layer within the substrate. This Cu thickness delta between the two substrate designs caused a change in CTE with supplier B (higher value) than supplier A due to thicker copper. Finite element modeling demonstrated relatively small macroscopic changes in CTE on the order of less than 2 percent can affect cycles to failure by 11 percent.

The key takeaway found from the head to head evaluation was supplier A producing a more stable process as it was able to meet the center point of the Cu thickness specification as compared to supplier B, which was off target. However, in essence, supplier A lost the head to head BLR comparative study with supplier B as its



FIGURE 6. JMP model of SED predicted vs. actual.



FIGURE 7. JMP model of CTE predicted vs. actual.



FIGURE 8. CTE prediction as a function of metal and dielectric thickness

accuracy in meeting the Cu thickness target caused reduced solder joint fatigue life. The typical corrective action would be to work with supplier B to establish better tolerance control in their Cu plating process to stabilize Cu thickness at the center or nominal value like supplier A. However, the lesson learned was to tailor and control the Cu thickness at the higher end of the specification to improve reliability performance. Typically, in any setting the criteria of success is to hit the bullseye or target, which supplier A achieved. Conversely, supplier B missed this mark with results that were skewed to the right. Ironically, because of the skewed results off-target reliability margin was obtained. In reflection of these findings, the adage "success is in the eyes of the beholder" has never been more poignant. ◆

Advanced lithography and electroplating approach to form high-aspect ratio copper pillars

KEITH BEST Rudolph Technologies, Wilmington, MA, and PHILLIP HOLMES, TEL NEXX, Billerica, MA

It is possible to fabricate copper pillars more than $100\mu m$ in height, with aspect ratios up to 6:1, using advanced packaging stepper lithography in conjunction with electroplating.

ecent years have seen rapid development in the area of advanced packaging. In general, advanced packaging processes are concerned with the interconnection of multiple chips in a single package to provide increased functionality and performance in a smaller volume. System Scaling Technologythe combination of front-end, middle-end and back-end to advance microelectronic systems—utilizes many different advanced packaging approaches, one of which is known as 2.5D packaging. The term "2.5D packaging" has not always been used consistently in literature. The definition used for the purpose of this paper can be summarized as follows: a 2.5D package utilizes an interposer between multiple silicon die and a systemin-package (SiP) substrate, where this interposer has through vias connecting the metallization layers on its front and back surfaces (FIGURE 1).

The development of these new packaging schemes is being driven primarily by the rapid growth in mobile handheld devices such as smartphones. Often, the manufacturing processes used are adaptations of wellestablished front-end processes. A number of different approaches are in development or already in production, including wafer-level chip scale packaging, copper pillar bumps on through silicon vias (TSVs), fan-out wafer level processing, and many more. Of particular interest is the



FIGURE 1. A 2.5D IC/SiP using an interposer and through vias.

replacement of solder bumps by fine pitch copper pillar bumps, which has been the subject of many new systemin-package designs. Here we investigate the lithography and plating of copper pillars, with focus on heights in excess of $100\mu m$ and diameters of $25\mu m$, in anticipation of future SiP requirements.

The increase in the number of I/O channels required by multi-chip system designs has exceeded the density and pitch capabilities that traditional solder bump processes can deliver, so that an alternative connection scheme is required. For interposers, the key enabling technology has been the development of fine pitch copper pillar bumps to provide the high-density interconnection between the interposer and the die. Copper pillar bumps provide a number of advantages over the solder bumps they are

KEITH BEST is director applications engineering at Rudolph Technologies, Wilmington, MA. **PHILLIP HOLMES** is director of technology at TEL NEXX, Billerica, MA

supplanting. They can deliver finer pitches, 40μ m and less have been demonstrated. They also provide superior electromigration performance in applications where high current-carrying capacity is required. However, lithography and electroplating for fine pitch copper pillar bumps can be particularly challenging. The pillars are electroplated into openings in a thick layer of photoresist which exceeds the capability of most front-end tools. Typically, today's copper pillars range from 30-50 μ m in height, with height to width aspect ratios from 1:1 to around 2:1 Here we describe the lithography, resist, and electroplating systems and processes required to create 5:1 aspect ratio copper pillars with heights in excess of 100 μ m.

Photoresist

A negative tone photoresist (JSR THB-151N) was chosen for this work. Its acrylate groups cross-link on exposure and are developed in industry standard 2.38% TMAH developer. The photoresist was spun to a thickness of 120 μ m on 300mm silicon wafers with an under bump metallization (UBM) prepared seed layer. To reach the 120 μ m photoresist film thickness, two coatings of photoresist were required, soft baked at 130C, 300secs and 130C, 360secs respectively. After coating, the photoresist film was allowed to rehydrate for one hour prior to exposure on a wafer stepper (Rudolph Technologies' JetStep System).

Lithography

We used a customized test reticle that included a wide range of sizes and pitches to expose the wafer. When processing a thick photoresist, well-controlled sidewall angles are a critical requirement, especially when electroplating tall copper pillars. Most front-end tools have high numerical aperture (NA) lenses with low depth of focus (DOF) that prevent adequate exposure of thick films with sufficient image contrast to meet the sidewall angle and resolution requirements. Mask aligners also struggle with high aspect ratio imaging, not because of their NA, but because they are unable to provide the necessary focus offset required to expose the film at high resolution, ultimately limiting their aspect ratio and sidewall angle control. Although photoresist sidewall angles are primarily a function of the photoresist material and its processing (pre-bake, post-bake, developing, etc.), the exposure system plays an important role. Accurate focus control across the wafer or substrate is

required to achieve consistent and accurate CD control with straight and perpendicular sidewalls.

The lithography stepper employed in this study refocuses for each exposure to ensure optimal focal plane height on advanced packaging substrates that are frequently warped by film stress and thermal cycling. The system's 0.1 NA provides a large depth of focus to maintain image integrity and CD control through thick films. The stepper lens is achromatized and the installed "filter wheel" provides a choice of illumination wavelengths to expose the photoresist layers: "broadband" ghi (350-450nm), gh (390 to 450nm) or i-line (365nm). This study, with a photoresist thickness of 120 μ m, required high energy illumination of >1000 mJ/cm², so broadband illumination (g,h,i wavelengths) was employed to maintain high throughput.

The coated wafers were exposed using a focus exposure matrix wafer layout which provided a large number of programmed focus and exposure conditions at a fixed stepping distance to enable quick and efficient characterization of the lithography process window for any pillar CD. After exposure, the wafers were developed for a total time of 180 secs, using 6 puddles in 2.38% TMAH. A number of wafers were processed in this way to provide images of the resist structures prior to the electroplating process. The SEM micrograph in **FIGURE 2** shows a cross section of the photoresist via mold structures, the CD limit appears to be $25\mu m$ with this process, since the via is not open to the seed metal beyond this resolution.

It is interesting to note how the sidewall angle of the photoresist changes with decreasing CD suggesting that the plating will generate a "pedestal" type of copper pillar



FIGURE 2. SEM micrograph of photoresist via mold structures.



QuantumClean®: Process Improvement Through Consistently Cleaner Parts®

QuantumClean is the global leader in high-purity outsourced process tool parts cleaning, performance coatings, refurbishment and analytical & engineering services to the semiconductor, solar and LED industries. QuantumClean operates on the frontier of the sub-20nm high-purity semiconductor parts cleaning market through leading-edge technologies, resources and expertise.



Global Locations

We operate innovative Advanced Technology Cleaning Centers® around the globe, built on the premise of providing customers process improvement through consistently cleaner parts that meet today's demanding sub-28nm requirements, dramatically reducing our customers' total cost of ownership. With 19 Advanced Technology Cleaning Centers located in 9 countries, QuantumClean provides unsurpassed cleaning capability worldwide. Our Advanced Technology Cleaning Centers are designed, constructed and managed for the specific purpose of providing exceptional semiconductor tool part cleaning, coating, surface treatment and restoration services.



Capabilities

As a global partner to semiconductor wafer fabs, OEMs & OPMs, we provide process enabling solutions including:

- Ultra-clean parts new & recycle
- Global leader in high purity diffusion Quartz/SiC Cleaning
- · Cleaning to an end-point specification
- Quartz repair and fabrication
- Proprietary life-extending coatings
- Texturing to optimize performance
- Complete copper segregation
- · Part refurbishment & kitting
- Precious metal recovery
- Failure analysis
- On-site support
- Dedicated MBE chamber cleaning facility and expertise
- · Logistics and specialized packaging
- Sophisticated, customer-accessible parts tracking and data collection system
- Alignment of our technology roadmap with customers
- Extensive R&D and applications engineering support resources

Fab areas served include:

• ALD, CVD, Diffusion, Etch, Implant, Photolithography, PVD

QuantumClean is the only parts cleaner validated by analytical data generated by ChemTrace[®] laboratories.

Partner/Solution

QuantumClean continues to develop innovative process ideas and methods for customers' unique part cleaning challenges. We are committed to providing solutions to help achieve cost savings, rapid turnaround times and the highest quality finished products possible. We look forward to collaborating with you to define additional methods for continuous improvement.

QUANTUM CLEAN

QuantumClean

Corporate Headquarters 1900 AM Drive, Suite 200 Quakertown, PA 18951 www.quantumclean.com info@quantumclean.com

Global Locations

USA

Fremont, CA San Jose, CA Phoenix, AZ Hillsboro, OR Irving, TX Carrollton, TX Colorado Springs, CO Scarborough, ME

Europe/Middle East

Glenrothes, Scotland Celbridge, Ireland Son, Netherlands Kiryat Gat, Israel

Asia

Hsinchu, Taiwan Tainan, Taiwan Pyeongtaek-si, Republic of Korea Hwaseong-si, Republic of Korea Pal-tan, Republic of Korea Singapore Xi'an, China



FIGURE 3. SEM cross section micrograph of 25μ m vias in 120μ m of negative resist at 1215mJ dose.

base at larger CDs, becoming progressively more vertical at smaller CDs. However, upon closer inspection of the smallest CDs, a slight "footing" can be observed at the base of the via (**FIGURE 3**), and this could result in slight undercut of the final copper pillar. The footing effect was most likely the result of our unoptimized develop process.

Electroplating

After the lithography processing, the wafers were sent to TEL NEXX for electroplating. The plating process employed the TEL NEXX Stratus P300 System, a fully automated electrochemical deposition system for advanced wafer-level packaging applications. The system deposits thick metal layers for wafer bumping, redistribution layers, TSVs, integrated passives, and MEMS.

In this study, we used a methanesulfonic acid copper chemistry with organic additives. The bath composition, operating temperature and current waveform were



FIGURE 4. SEM micrograph of electroplated copper pillars after photoresist strip.



FIGURE 5. SEM micrograph showing $20\mu m$ CD copper pillar with 6:1 aspect ratio.

optimized for high speed copper plating into very thick resist features with flat bump profiles. After plating the photoresist was stripped using an immersion bath with EKC162 solution at 60 degrees. To preserve the profile of the photoresist mold the seed layer was not etched. The final copper pillar structures exhibit the inverse photoresist mold profile (**FIGURE 4**).

The electroplating process successfully deposited copper in the photoresist via "molds" that were open to the copper seed material, producing good quality copper pillars with a final minimum copper pillar CD of $20\mu m$, indicating a process bias of $5\mu m$. This bias enabled the final copper pillar to reach a 6:1 aspect ratio as shown in **FIGURE 5**.

The final copper pillars exhibit excellent sidewall angle, 90 degrees for the smaller CDs. The profiles correlate well with the profiles observed in the photoresist SEM cross sections. The change in profile at the base of the



FIGURE 6. SEM micrograph of larger copper pillars showing same base profile as photoresist images.



FIGURE 7. SEM micrograph of copper pillar top.

photoresist for the smaller CDs did result in a slight undercut of the final copper pillar. The removal of this photoresist foot could be achieved by either increasing the de-scum time or modifying the develop recipe. The larger copper pillars tended to flare out slightly at the base (**FIGURE 6**) compensating for any undercut. This will benefit the structure during the removal of the copper seed layer.

The rheology of the copper pillar surface is very important for bonding reliability and the uniform plating of Sn solder, which was not performed during this particular study since it was not the primary objective. **FIGURE 7** shows the flat top surface of a copper pillar which is free of voids and defects. For advanced packaging applications, precise copper pillar height control is essential, and lithography CD control plays an important part in the plating process since CD variation directly affects plated height. The electroplating rate is proportional to current per unit area, i.e. the open area at the bottom of the photoresist openings at the beginning of the process, and the area of the evolving metal surface during deposition. Variation in CD or sidewall angle across the wafer will result in a corresponding change in copper pillar height. For example, in the case of copper pillar features a 5% change in CD can cause a 10% change in plated height.

Conclusion

The results of this study prove that it is possible to fabricate copper pillars more than 100μ m in height, with aspect ratios up to 6:1, using advanced packaging stepper lithography in conjunction with electroplating. As advanced packaging requirements continue to evolve, the ability to create smaller copper pillar CDs at finer pitches in thick films will provide increased I/O density opportunities for SiP designers. Furthermore, it is clear that achieving high yield and reliability in the final package requires precise CD control throughout the entire photoresist profile to ensure consistent copper pillar height.

INTERCONNECTS

Practical limits for metallization scaling in fabs

ED KORCZYNSKI, Senior Technical Editor

Beyond economic limits due to litho limitations, the inherent need for a physical barrier puts an electrical limit on the ability to scale.

n-chip interconnects for ICs have evolved to meet different exacting needs, and the most advanced chips require multiple levels of copper (Cu) metal lines and via connections between transistors. When scaling Cu lines to the finest dimensions possible to interconnect local transistors in advanced manufacturing nodes, there are economic limits due to lithography technology. Also, the inherent need for a physical barrier to surround Cu and prevent poisonous out-diffusion imposes an electrical limit on the ability to scale. Best practices today include an explicit hierarchy of dimensions and a stacking-order for on-chip interconnects: local between nearby transistors, global between functional blocks, as well as input/output (I/O) and power/ ground connections. With advanced logic chips having >12 levels of on-chip copper metallization, only the

Level 14nm FET	MemoryiLogic	Pitch (nm)
Chip I/O	L3 external DRAM	40,000
Globel	L2 SRAM or DRAM	5,000-10,000
Intermediate	L1 SRAM date bus	600-3,000
Locel	L1 SRAW bit/word-line	140
Gate	L1 SRAM transistor	42

TABLE 1



FIGURE 1. (LEFT) Fraction of the copper (Cu) wire thickness used by the barrier/liner coating within the trench, and (RIGHT) SEM cross-section of a damascene Cu trench where half the width is used by the barrier/liner. (Source: ITRS 2012)

bottom-most are at the tightest pitch. **Table 1** (courtesy of imec) shows the hierarchy of interconnect signals for a 14nm-node finFET logic chip, and the tightest pitch is 42nm as used for the vertical gate contacts as well as for the metal-1 (M1) and metal-2 (M2) levels. The last published International Technology Roadmap for Semiconductors (ITRS) chapter for Interconnects that included detailed tables of on-chip metal specifications was published in 2012. In the ITRS 2012 Interconnect chapter Table 2 on microprocessor (MPU) requirements, the "Intermediate Wires" specification for Metal 2 (M2) is the same as for Metal 1 (M1) level and shows 32nm halfpitch is manufacturable, which is used with MPU physical gate lengths of 22nm.

FIGURE 1 shows the fraction of the intermediate wire volume that is Cu depending on the thickness of the barrier for succeeding generations of high-performance (HP) MPUs. Note that in the SEM cross-section on the right that the 10nm of Cu is only 50% of the line thickness, and that such a line would be extremely susceptible to current-crowding and premature circuit failure due to electro-migration (EM).

In minimally-scaled Cu wiring, resistivity increases arise due to electron scattering from the sidewalls and grain boundaries. Tricky process integration involving

> electro-chemical deposition (ECD) of the Cu along with careful thermal annealing is already being used to grow large columnar grains across the trench—resembling bamboo when cut in cross-section—to minimize the volume of grain-boundaries. Forming columnar lines of single Cu grains after ECD requires control of barrier atomic-layer deposition (ALD) parameters, along with chemical-mechanical planarization (CMP) and rapid-thermal annealing (RTA) processes.

When engineering materials, first-order parameters to be controlled include composition and uniformity, while second-order parameters include internal structure such as crystal orientation or average crystal grain-size in multi-crystalline structures. In general, it is more difficult and far more expensive to control second-order parameters in manufacturing, and when engineering at the atomic scale it is yet more difficult to control thirdorder parameters such as grain boundary orientation.

Since the industry must control third-order parameters to continue using Cu metal, there has been ongoing R&D of non-metallic materials that could be integrated into ICs

as on-chip conductors. Superconductors have been found that can exhibit zero resistance to electric current flow, but only when they are frozen to extremely low temperatures such that phonon vibrations within their lattices settle out. Recently, a team of six Japanese research groups tested nearly 1000 materials over a four year period and found no superconductors with critical temperatures (Tc) above the 298°K of room temperature.

The rapid increase in resistivity when Cu lines are scaled to minimal dimensions motivates the search for "ballistic"

conductors which are immune from electron scattering effects. While R&D into graphene and Carbon Nano-Tubes (CNT) as on-chip conductors continues, there are inherent issues with integrating any such technologies into high-volume manufacturing (HVM) to achieve superior performance compared to legacy Cu. The ITRS 2012 Interconnects chapter summarizes the issues:

Ballistic transport in one dimensional systems, such as silicides, carbon nano tubes, nanowires, graphene nanoribbons or topological insulators offers potential solutions. While ballistic transport has many advantages in narrow dimensions, most of these options incur fundamental, quantized resistances associated with any conversions of transport media, such as from Cu to CNTs. In addition to the quantum resistance, the technological problems of utilizing an additional conduction medium with its interface, substrate and integration issues, pose substantial barriers to the implementation of ballistic transport media.



FIGURE 2. Simplified 3D schematic of Macronix's new single-gate vertical channel (SGVC) 3D NAND Flash architecture. (Source: IEDM 2015)

Imec recently published preliminary "7nm-node" finFET specifications for logic ICs having 14nm gate lengths, with expectation that delays in the implementation of EUV lithography call for use of multiple-patterning using 193-immersion (193i). M1 layer patterning at 18nm half-pitch can be done with self-aligned doublepatterning (SADP) technology, while Litho-Etch-Litho-Etch (LELE) patterning with two masks allows for 24nm half-pitch patterning of more arbitrary 2D shapes for easier routing. Going to tighter half-pitches will require Litho-Etch-Litho-Etch-Litho-Etch (LELELE) with three masks, or self-aligned quadruple patterning (SAQP) schemes, which is why the number of metal levels for logic continues to increase with each successive node.

> In memory chips with regular bit arrays for storage and orthogonal bit:word architectures, leading 3D architectures use similar metal interconnect half-pitches. FIGURE 2 shows a new 3D stacked NAND Flash memory architecture that will be shown at the 2015 IEEE International Electron Device Meeting (IEDM) in presentation 3.2, "A Novel Double-Density, Single-Gate Vertical Channel (SGVC) 3D NAND Flash That Is Tolerant to Deep Vertical Etching CD Variation and Possesses Robust Read-disturb Immunity," by Hang-Ting Lue et al. of Macronix.

The Metal Level 2 Bit Line (ML2 BL) half-pitch of ~25nm in parallel lines in this 3D NAND structure can be formed with SADP litho. Since SADP has been used in HVM of 2D NAND cells, presumably the complex SADP integrated process flow has already been established. Imec has shown ability to reach 18nm half-pitch with SADP 193i, so this new 3D NAND structure might be able to be shrunk by a "half-node" without having to re-engineer the ML2 BL fab process flow.

Even if the lithographic cost of scaling metal lines to <18nm half-pitch could be managed, the Cu barrier provides a functional limit as shown in Fig. 1. Assuming that Cu multi-level interconnects will be current-limited and will require ~3nm barriers—to prevent out-diffusion from the line as well as EM-induced diffusion within the line—the industry is already considering atomic limits. The barrier would be ~1/3 of 18nm, ~1/2 of 12nm, and ~2/3 of 9nm wide Cu lines. ◆

LITHOGRAPHY

Feed-forward overlay control in lithography processes using CGS

DOUG ANBERG and DAVID M. OWEN, Ultratech, San Jose, CA

Feed-forward can be applied for controlling overlay error by using Coherent Gradient Sensing (CGS) data to reveal correlations between displacement variation and overlay variation.

s the semiconductor industry is fast approaching 10nm design rules, there are many difficulties with process integration and device yield. Lithography process control is expected to be a major challenge requiring overlay control to a few nanometers. There are many factors that impact the overlay budget that can be broadly categorized as those arising from the reticle, the lithography tool and wafer processing. Typically, overlay budget components associated with the reticle and lithography tool can be characterized and are relatively stable. However, as published elsewhere, process-based sources of surface displacement can contribute to the lithography overlay budget, independent of the lithography process (e.g., etch, anneal, CMP). Wafer-shape measurement can be implemented to characterize process-induced displacements. The displacement information can then be used to monitor specific processes for excursions or be modeled in terms of parameters that can be fed-forward to correct the lithography process for each wafer or lot.

The implementation of displacement feed-forward for overlay control requires several components, including: a) a system capable of making comprehensive surface displacement measurements at high throughput, b) a characterization and understanding of the relationship between displacement and overlay and the corresponding displacement variability, c) a method or system to integrate the displacement information with the lithography control system. The Coherent Gradient Sensing (CGS) technique facilitates the generation of high-density displacement maps (>3 million points on 300 mm wafers) such that distortions and stresses induced shot-by-shot and process-by-process can be tracked in detail. This article will demonstrate how feed forward can be applied for controlling overlay error by using CGS data to reveal correlations between displacement variation and overlay variation.

High-speed, full-wafer data collection

Historically, patterned wafer surface inspection was limited to monitoring topography variations within the die area and across the wafer with the use of pointby-point measurements with low throughput, typically limiting measurements to off-line process development. Surface inspection of patterned wafers involving transparent films (e.g. SiO2 deposited films) was typically further limited to contact techniques such as stylus profilometry.

With CGS interferometry, a high-resolution front-surface topography map of a full 300 mm patterned wafer can be obtained for product wafers with an inspection time of a few seconds. Transparent films can typically be measured successfully without opaque capping layers due to the self-referencing attribute of the CGS interferometer. Essentially, CGS technology compares the relative heights

DOUG ANBERG currently serves as Ultratech's Vice President of Advanced Lithography Applications; **DAVID M. OWEN** has been the Chief Technologist for Surface Inspection at Ultratech since 2006. Prior to joining Ultratech, Dr. Owen spent nearly a decade as a research scientist at the California Institute of Technology (Caltech) in Pasadena, and was the Founder and Chief Technology Officer for Oraxion Diagnostics.





FIGURE 1. Example of the analysis of the uniform and non-uniform stress components of the displacement field: (a) total displacement computed from the x-direction slope, (b) uniform stress component of the displacement field determined from the best-fit plane to the data in (a), (c) nonuniform stress component of the displacement field.

of two points on the wafer surface that are separated by a fixed distance. Physically, the change in height over a fixed distance provides slope or tilt information and the fringes in a CGS interference pattern are contours of constant slope. In order to reconstruct the shape of the surface under investigation, interference data in two orthogonal directions must be collected. The slope data derived from the interference patterns is integrated numerically to generate the surface shape or topography. In-plane surface displacements in the x- and y-directions can then be computed from the surface topography using fundamentals of plate theory (FIGURE 1).

To best utilize the capabilities of CGS technology for determining stress-induced displacement impacting critical layer overlay budgets, a "Post minus Pre" inspection strategy is typically employed, where two measurements of a wafer are taken: one prior to the process step or module of interest (the pre-process map), and a second measurement is taken on the same wafer after completing the process step or module (the postprocess map). The pre-process topography map is then



FIGURE 2. Example of "Post minus Pre" topography CGS measurement.

mathematically subtracted post-process from the topography map, providing detailed, high resolution information about the topography variation in the process step or module of interest. A series of topography maps illustrating the "Post minus Pre" process is shown in **FIGURE 2**.

The surface displacements

directly impact the relative position of all points on the wafer surface, leading to potential alignment errors across the wafer at the lithography step. By measuring the evolution of process-induced stresses and displacement across multiple steps in a process flow, the overlay error due to the accumulated stress changes from those process steps can be evaluated, and the cumulative displacement can be calculated. The displacement error can then be fed forward to the lithography tool for improved overlay correction during the exposure process.

In the simplest implementation of this approach, the pre-process or reference measurement would be made following the prior lithography step, whereas the postprocessing measurement would be made just before the lithography step of interest. In this manner, the total displacement induced between two lithography steps can be characterized and provided to the lithography system for overlay correction.

Stress and displacement process fingerprinting

By using CGS-based inspection to generate full-wafer topography, displacement and stress, detailed information can be provided for both off-line process monitoring (SPC), or in-line, real-time monitoring

> (APC) of process steps with significant process induced stress and displacement. A key consequence of the monitoring flexibility afforded by the measurement is the ability to characterize and compare withinwafer displacement and stress fingerprints of individual process chambers in a manufacturing line.

Target-based overlay metrology systems have historically been used as the only metrology tool to measure overlay error at critical lithography layers. Overlay data from the targetbased overlay tools is collected after the wafer exposure step and is fed-backward to correct for the measured overlay error for subsequent wafers. As processinduced displacement errors are becoming a significant percentage of the layer-to-layer overlay budget, this post processing feed-back approach for overlay correction may not be sufficient to meet critical layer overlay specifica-



FIGURE 3. Vector displacement map showing process-induced edge distortion.

tions. Furthermore, overlay errors are often larger near the edge of the wafer where traditional overlay metrology target densities are typically low, providing only limited data for overlay correction.

The implementation of displacement feed-forward overlay correction can be

used to account for wafer-to-wafer and within-wafer distortions prior to lithography. The displacements can be characterized using an appropriate model and the model coefficients, or correctables, can be provided to the lithography tool for adjustment and control on a wafer-by-wafer basis. As shown in **FIGURE 3**, the CGS technique has the additional advantage of providing high-data density near the edge of the wafer (typically > 75,000 data points beyond 145 mm, sub-sampled in the Fig. 3 vector map for clarity), such that more accurate corrections can be determined where the overlay errors tend to be largest. As a result, lithography rework can be reduced and productivity increased. Case studies have revealed that a significant improvement in overlay can be achieved using this approach.

For each critical lithography step, a correlation is typically generated by comparing the traditional overlay measurement tool results to the surface displacement measured by the CGS measurement tool. Recognizing that displacement is only one component of the total overlay measurement, correlation of overlay to displacement requires effort to model or characterize the non-displacement components of the measured overlay. As a result, the appropriate correlation is derived by comparing total overlay to displacement plus the non-displacement overlay sources.

FIGURE 4 shows plots of total overlay versus displacement plus modeled non-displacement overlay sources for multiple locations on a single wafer processed in a leading-edge device flow. **Figure 4a** shows the x-direction data, whereas **Fig. 4b** shows the y-direction data. The data is presented in arbitrary units, however the same reference value in nanometers was used to normalize each set of data. The displacement data was evaluated at the same locations as the overlay target positions. For both the x-direction and y-direction data, the point-to-point correlation indicates good correlation with the correlation coefficients of 0.70 and 0.76, respectively. The RMS of the residuals of the linear fit to each data set are on the order of 1.5 to 2.0 nm.

FIGURE 5 similarly shows the wafer-to-wafer variation for overlay and displacement for the x-direction (**Fig. 5a**) and y-direction (**Fig. 5b**). The data in Fig. 5 are from multiple lots for the same lithography process evaluated

to generate the data in Fig. 4. As with the point-to-point data, the wafer-to-wafer data shows strong correlation with correlation coefficients of 0.94 and 0.90 for the x-direction and y-direction, respectively.

The data in Figs. 4 and 5 illustrate key points regarding the correlation of overlay to displacement. First, the inherent variability of an advanced lithography process



FIGURE 4. Within-wafer (point-to-point) correlation of conventional overlay data and displacement data for the (a) x-direction and (b) y-direction.





FIGURE 5. Wafer level correlation between conventional overlay, |mean|+3 sigma and displacement, |mean|+3 sigma for a leading-edge process in the (a) x-direction and (b) y-direction.

is typically on the order of 1 to 2 nm. As a result, it is reasonable to conclude that the most of the scatter shown in Fig. 4 is likely associated with the variability in non-displacement sources of overlay variation. Second, the modeling or empirical characterization of non-displacement overlay sources is useful to the extent to which those non-displacement sources are constant. Consequently, if such modeling is part of the displacement feed-forward scheme in an effort to predict overlay, the model must account for known variations in the lithography process. A simple example is variations in overlay performance due to differences between lithography chucks.

Displacement feed forward

It has been shown elsewhere that stress induced displacement can account for a significant fraction of the overlay error for certain critical layers at the 40 nm node and below. It is therefore critical to develop the tools necessary for utilizing the measured displacement data for real-time in-line feed forward overlay correction to the scanner. One approach to this solution is to develop a system that allows the user to define the level of correction to be applied to the scanner for each lot, wafer or within-wafer zone.

FIGURE 6 shows a simplified schematic for a combined displacement feed-forward and image placement error feed-back approach. Once the process induced displacement for a specific set of process steps has been measured and correlated to overlay error, the measured displacement can be "fed forward" to the scanner in combination with traditional image placement error

feedback techniques to further improve critical layer scanner overlay results. This approach is currently being implemented in leading-edge memory fabs to further reduce overlay errors on critical lithography levels and improve overall device yield.

Summary

The measurement of processinduced surface displacement can be an effective part of the overlay control strategy for critical layers

at leading edge process nodes. CGS technology provides a method to comprehensively measure these displacements at any point in the process flow. Using a full-wafer interferometer, this system measures the patterned wafer surface in a few seconds and provides a map with up to 3,000,000 data points. This enables 100% in-line monitoring of individual wafers for in-situ stress and process induced surface displacement measurements. Its self-referencing interferometer allows the inspection to be made on any type of surface or films stack, and does not require a measurement target. This capability is currently being employed in numerous leading-edge memory and logic processes. ◆



FIGURE 6. Simplified schematic for a combined displacement feed-forward and image placement error feed-back approach.

PROCESS WATCH

The Most Expensive Defect; Part 2

DAVID W. PRICE and DOUGLAS G. SUTHERLAND, KLA-Tencor, Milpitas, CA

Because yield and reliability defects stem from the same source, reducing the source of yield defects will have the side benefit of also reducing reliability defects.

he December 2014 edition of Process Watch suggested that the most expensive defect is the one that goes undetected until the end of line. Indeed, undetected excursions typically result in the scrap of millions of dollars per year of defective semiconductor chips.

But many electronics suppliers and OEMs would argue that the consequences of field failures (reliability defects) are much worse than those of non-functioning devices detected at electrical test (killer defects). Reliability defects result in angry customers, expensive failure analysis, the possibility of lost business, or worse. Consider all the IC devices in places such as automobiles, airplanes, and medical diagnostic and treatment equipment. Reliability in these applications is critical devices simply cannot fail out in the field. Hence, many fabs place a high priority on reducing the potential for reliability defects.

A fundamental truth of process control for the semiconductor IC industry is:



FIGURE 1. The same defect types that impact yield also affect reliability. They are distinguished primarily by their size and where they land on the die structure.

Improving Yield Also Improves Device Reliability

For a well-designed process and product, early-life factory reliability issues are dominated by random defectivity. This correlation has been confirmed by numerous researchers over the last two decades [1-6]. More recently, the authors interviewed the quality managers at multiple automotive OEMs who confirmed that the vast majority of reliability failures were ultimately traced to random defectivity in the fab.

Latent vs killer defects

By definition, a killer defect (a.k.a. yield defect) is a defect that causes the device to fail at t = 0 (electrical test). We use the term "latent defect" (a.k.a. reliability defect) to refer to a defect that causes the device to fail at t > 0 (burn-in to ~6 months).

The relationship between yield and reliability stems from the observation that the same defect types that impact yield also impact reliability. The two are distinguished primarily by their size and where they land on the device structure, as shown in **FIGURE 1**.

Experiments conducted at multiple device manufacturers have shown that for every 100 killer defects that cause yield loss, there are approximately 1-2 latent defects that will result in a reliability failure. This relationship between killer and latent defects is unequivocal and applies to a broad spectrum of defect types. Furthermore, the preponderance of these defects also correlates with overall defectivity. In other words:

- Lots with poor yield also have poor reliability
- Wafers with poor yield also have poor reliability
- Die locations with poor yield also have poor reliability

DR. DAVID W. PRICE is a Senior Director and DR. DOUGLAS SUTHERLAND is a Principal Scientist at KLA-Tencor Corp, Milpitas, CA.

For this reason, many fabs will ink out a good die if it is in a suspicious neighborhood on the wafer. These good dies, located in neighborhoods where the surrounding dies fail (**FIGURE 2**), have a higher probability of a latent defect, which may activate in the field and create a reliability problem.

Reliability defect reduction strategies

IC makers who supply the automotive industry have long adopted the following strategy: The best way to reduce the possibility of latent

(reliability) defects is to reduce the fab's overall random defectivity levels. This is accomplished through the following:

- Increased investment in process control in order to achieve higher baseline yields and fewer excursions for the entire fab (both automotive and non-automotive flows; See FIGURE 3)
- 2. Dedicated automotive process flows that utilize only the most stable process equipment
- 3. Use of screening inspections on a few layers in which every wafer is scanned for defects. This is typically accomplished using high speed inspection tools, such as KLA-Tencor's 8-Series (or 8900 – final TBD) systems

Conclusion

Because yield and reliability defects stem from the same source, reducing the source of yield defects will have the side benefit of also reducing reliability defects. Depending on the nature of the product, this could play a significant role in the fab's determination of the costoptimal investment in process control. For more information on the correlation of random defectivity and reliability, please contact the authors or refer to the papers listed below.



FIGURE 2. A good die in a bad neighborhood. Even though the highlighted die may pass final test, there is an elevated likelihood that this die represents a potential reliability problem. Many device manufacturers would ink out such a die at final test.





References

- Shirley, Glenn and Johnson, Scott. "Defect Models of Yield and Reliability." Published lecture #13 for Quality and Reliability Engineering ECE 510 course at Portland State University, 2013. http://web.cecs.pdx.edu/~cgshirl/Quality%20 and%20Reliability%20Engineering.htm
- Roesch, Bill. "Reliability Experience." Published lecture #12 for Quality and Reliability Engineering ECE 510 at Portland State University, 2013. http://web.cecs.pdx.edu/~cgshirl/Quality%20 and%20Reliability%20Engineering.htm
- Kim et al. "On the Relationship of Semiconductor Yield and Reliability." IEEE Transactions on Semiconductor Manufacturing, Vol. 18, No. 3 (2005).
- Riordan et al. "Microprocessor Reliability Performance as a Function of Die Location for a .25um, Five Layer Metal CMOS Logic Process." 37th Annual International Reliability Physics Symposium Proceedings (1999): 1-11. DOI (http://dx.doi. org/10.1109/RELPHY.1999.761584).
- Barnett et al. "Extending Integrated-Circuit Yield Models to Estimate Early-Life Reliability." IEEE Transactions on Reliability, Vol. 52, No. 3. (2003).
- Kuper et al. "Relation between Yield and Reliability of Integrated Circuits: Experimental results and Application to Continuous Early Failure Rate Reduction Programs." Proceedings of the International Reliability Physics Symposium (1996): 17-21. ◆

RELIABILITY

When front-end-of-line and backend-of-line reliability meet

Due to the further scaling and increasing complexity of transistors, the boundaries between back-end-of-line and front-end-of-line reliability research are gradually fading. Imec's team leaders Kristof Croes and Dimitri Linten give their vision on the future of reliability research.

n April 2015, the 53rd edition of the IEEE International Reliability Physics Symposium (IRPS) took place, a top conference where experts in reliability of micro- and nanoelectronics meet. With 16 contributions as either an author or a co-author, imec was prominently present. Dimitri Linten: "Our contributions to conferences such as IRPS highlight the unique role that imec plays in the field of reliability. And they show the importance of reliability research at imec for the development of new transistor and memory concepts. As scaling continues, a whole range of new technology options is being researched. New materials and architectures with often unknown failure mechanisms are being introduced. Reliability is one of the factors that determine which concept will finally have a chance. For example, one of the options is to replace silicon in the transistor's channel by germanium or a III/V material since these materials provide a higher charge carrier mobility. But until now, these materials pose important challenges to the reliability of the transistors that are made of these materials. Or, researchers look at introducing either air gaps or ultralow-k materials as spacers between the transistor's gate and drain in order to keep the capacity as low as possible. The integration of all these new materials is important, but their reliability is crucial as well: reliability before performance."



FIGURE 1. Advanced sample preparation is required to perform accurate failure analysis.

Kristof Croes: "10 years ago, reliability was tested only in a final stage of a technology development. But due to the ever decreasing reliability margins, the reliability is now being tested from the very beginning. And this starts with an understanding of the physics behind the failure, for which we often collaborate with universities. Once we understand the failure of e.g. new materials, we can model our findings and predict the lifetime of the device."

Front-end-of-line vs back-end-of-line

Traditionally, CMOS process engineers classify the semiconductor process in two main parts: the front-end-of-line (FEOL) and the back-end-of-line (BEOL). The FEOL comprises all the process steps that are related to the transistor itself, including the gate of the transistor. The BEOL comprises all subsequent process steps. In the BEOL, the various transistors are being interconnected through metal lines. The same classification is being used in reliability research. Consequently, FEOL and BEOL reliability is tested independently.

Kristof Croes: "This historical separation is being applied at imec as well, where reliability research within the process technology division is distributed among several groups. One group looks into the reliability of FEOL and memory chips. Another group investigates the BEOL reliability and chip packaging interaction. Today, in BEOL processes, electromigration (the movement of metal atoms as a result of an electric current), stress migration, time dependent dielectric breakdown (TDDB) and thermomechanical stress are the main failure mechanisms. We also look into 3D structures, where the impact and reliability of through-Si vias are important issues. In a 3D-stacked structure, for some applications, the Si wafer needs to be thinned down to about 5 micrometer. And this impacts the reliability. And there are thermal and thermo-mechanical influences related to the assembly of materials with completely different mechanical properties. All these failure mechanisms in the BEOL will become increasingly important for future technology nodes."

Dimitri Linten: "We look into the time dependent breakdown (TDDB) of the gate stack, and into stressinduced leakage current (SILC) and hot carrier stress (HC). The bias temperature instability (BTI) is important as well, as it causes a shift of the threshold voltage (VT) of the transistor during the lifetime of the circuit. We also investigate memory elements, by testing and modelling the retention and endurance of the memories. ESD or electrostatic discharge is still one of the main important failure mechanisms at the level of the final ICs in a certain technology. In order to intercept the current that is released during an electrostatic discharge, protecting ESD structures are implemented in the FEOL."

FEOL and BEOL reliability: fading boundaries

As the dimensions of the transistor shrink, the impact of the FEOL on the BEOL reliability – and vice versa – increases. Kristof Croes: "A well-known example is self-heating in FinFETs. In planar CMOS processes, the heat that is released during the transistor's operation is dissipated mainly through the Si substrate. But in a FinFET architecture, we have to take into account a higher thermal coupling towards the metal interconnects. The FinFETs warm up and heat the metal lines. And this impacts the reliability of the BEOL structure. In 3D technology, we thin down wafers with TSVs. After opening the TSVs, we can stack them on top of another wafer. The integration of the TSVs, the thinning and stacking of the wafers influence both the FEOL and the



FIGURE 2. Finite element modelling is a crucial step in order to understand complex electrical/thermomechanical/thermal behavior of chips.

BEOL performance and reliability."

Dimitri Linten: "Also the introduction of new architectures brings the reliability of FEOL and BEOL closer to each other. Think about vertical nanowires, potential successors of the FinFET because they promise a better electrostatic channel control. One of the challenges in terms of reliability is to provide these structures with an ESD protection. While in more conventional structures, the FEOL is most sensitive to electrostatic discharge, the impact of electrostatic discharge on the BEOL becomes critical in vertical nanowires. In these 3D structures, we have to connect all the vertical nanowires through local interconnects and interconnects that will be located very close to each other. And these interconnects will put other requirements to the ESD



FIGURE 3. Acquiring a large amount of statistical data sets is crucial for BTI, HC, TDDB and SILC analysis.

protection circuit than we are used to. A possible solution is to consider a 3D stacking of ESD protection circuits on top of the transistor architecture."

Another consequence of further scaling is an increase in the variability of the transistor parameters. In FEOL, variability is a well-known phenomenon. Dimitri Linten: "Time dependent variability of BTI is a relatively new challenge for reliability research. For large transistors - the older generations - BTI translates into an average shift of the circuit's threshold voltage of e.g. 50mV, the spec for BTI. But upon further scaling, there is no average shift anymore. Instead, there will be a static distribution of shifts. The variability becomes time dependent and the lifetime of the circuits will be spread. The imec FEOL reliability group is a world leader in this domain: we have developed a defect centric BTI model that has been adopted by market leaders in the semiconductor industry. On time dependent BTI, we closely collaborate with the design group in order to develop methodologies that take into account the time dependence." Kristof Croes: "Also in BEOL, variability becomes increasingly important. Think about via misalignment or line edge roughness of increasingly smaller metal lines. These issues degrade the reliability and the lifetime of the BEOL. To deal with the increasing variability, a powerful

statistical toolbox is required. And this toolbox can be deployed for BEOL as well as for FEOL reliability research."

When BEOL meets FEOL reliability

As dimensions are shrinking, the boundaries between FEOL and BEOL reliability are gradually fading. Kristof Croes: "We are convinced that we should optimally attune the activities and tools used for reliability research. We have to bring the people from BEOL and FEOL reliability closer together. And we want to unite the researchers outside these groups that work on reliability. Reliability is a field of expertise and sharing problems often provides part of the solution. For future technology nodes and for developments beyond scaling, this will increase the operational efficiency of reliability research. To strengthen this idea, we will on September 4 an internal workshop at

organize on September 4 an internal workshop at imec, with the help of our predecessors and colleagues Guido Groeseneken and Ingrid De Wolf. This will help our researchers to gain more insight into each other's work and into the tools they use. Hopefully, this idea will be adopted outside of imec as well."

Additional reading

Technical program of the 2015 IRPS conference with abstracts (http://www.irps.org/program/technical-program/15-program.pdf)

"New test allows to visualize in real-time crack formation of BEOL" March issue of imec magazine (http://magazine.imec.be/data/57/ reader/reader.html#preferred/1/package/57/pub/63/page/2) ◆

Solid State Product Showcase



ADVERTISEMENT

Die Bumping and QFN Advanced Packaging Solutions

CVI provides advanced packaging and assembly solutions including solder bumping single die, gold stud bumps, overmolded and open cavity QFN packages, and wafer bumping (including redistribution, RDL). CVI has a selection of substrate, die and PCB repair kits (pads and traces). Reball services are available for CSP and BGA.

www.covinc.com





Looking for a Custom Valve?

From Concept to Completion From Idea to Implementation From Engineering to Execution From Prototype to Production

You Visualize it, We'll Make it Happen!

> Quality Vacuum Valves Since 1973

www.highvac.com



Dry, High Performance Leak Detection

The Pfeiffer Vacuum ASM 380 dry, mobile leak detector is optimized for rapid pump down and short response times for ultra-clean maintenance of process chambers and large test systems. It features a 360° degree color touch display, an easy to navigate menu, SD card storage for remote analysis and extremely long maintenance intervals.

www.pfeiffer-vacuum.com



Solid State Technology

For over 50 years, Solid State Technology has been the leading independent media resource, covering:

- Semiconductors
- Advanced Packaging
- MEMS
- Displays
- LEDs

Request a **FREE** subscription to our magazine and e-Newsletters today at <u>www.solid-state.com/subscribe</u>

EXECUTIVE OFFICES

www.solid-state.com

ad index

Advertiser	Pg
ClassOne Technology	C4
The ConFab	3
CV, Inc	31
HVA	31
IPG Photonics	C2
Pfeiffer Vacuum	31
QuantumClean	
SEMI	C4
TSI	9
Y.E.S.	7

The Advertiser's Index is published as a service. The publisher does not assume any liability for errors or omissions.

Solid State TECHNOLOGY

Extension Media 1786 18th Street, San Francisco, CA 94107-2343.

ADVERTISING

Sales Manager Kerry Hoffman 1786 18th St. San Francisco, CA 94107-2343 Tel: 978.580.4205; e-mail: khoffman@extensionmedia.com

North America Kerry Hoffman Tel: 978.580.4205 khoffman@extensionmedia.com

Germany, Austria, E. Switzerland & E. Europe

Holger Gerisch Tel: +49.0.8856.8020228 holgerg@pennwell.com China, Hong Kong Adonis Mak Tel:+852.90182962 adonism@actintl.com.hk

Taiwan Diana Wei Tel: +886.2.23965128 ext: 270 diana@arco.com.tw

Rest of World Kerry Hoffman Tel: 978.580.4205 khoffman@extensionmedia.com

The ConFab and Webcasts Sabrina Straub Tel: 603.770.6569 sstraub@extensionmedia.com

industry forum

Security by Design

TThe advent of Internet-connected devices, the so-called Internet of Things (IoT), offers myriad opportunities and significant risks. The pervasive collection and sharing of data by IoT devices constitutes the core value proposition for most IoT applications. However, it is our collective responsibility, as an industry, to secure the transport and storage of the data. Failing to properly secure the data risks turning the digital threat into a physical threat.

Properly securing IoT systems requires layering security solutions. Data must be secured at both the network and hardware level. As a hardware example, let's concentrate, on the embedded security implemented by semiconductor chips.

Authentication and encryption are the two main crypto functions utilized to ensure data security. With the mathematical security of the standardized algorithms (such as AES, ECDSA, SHA512, etc.) is intact, hackers often exploit the implementation defects to compromise the inherent security provided by the algorithms.

One of the most dangerous and immediate threats to data security is a category of attacks called Side Chanel Analysis attacks (SCA). SCA attacks exploit the power consumption signature during the execution of the crypto algorithms. This type of attack is called Differential Power Analysis (DPA). Another potent attack form of SCA is exploiting the Electromagnetic emanations that are occurring during the execution of the crypto algorithm – or Differential Electromagnetic Analysis attacks (DEMA).

Both DPA and DEMA attacks rely on the fact that sensitive data, such as secret keys, leaks via the power signature (or EM signature) during execution of the crypto algorithm.

DPA and DEMA attacks are especially dangerous, not only because of their effectiveness in exploiting security vulnerabilities but also due the low cost of the equipment required for the attack. An attacker can carry out DPA attacks against most security chips using equipment costing less than \$2,000.

There are two fundamental ways to solve the threat of DPA



and DEMA. One approach is to address the symptoms of the problem. This involves

CHOWDARY YANAMADALA, Senior Vice President of Business Development, ChaoLogix adding significant noise to the power signature in order to obfuscate the sensitive data leakage. This is an effective technique. However, it is an ad-hoc and temporary measure against a potent threat to data security. Chip manufacturers can also apply this technique as a security patch, or afterthought, once and architecture work is completed

Another way (and arguably a much better way) to solve the threat of DPA is to address the problem at the source. The source of the threat derives from the leakage of sensitive data the form of power signature variations. The power signature captured during the crypto execution is dependent on the secret key that is processed during the crypto execution. This makes the power signature indicative of the secret key.

What if we address the problem by minimizing the relation between the power signature and the secret key that is used for crypto computation? Wouldn't this offer a superior security? Doesn't addressing the problem at the source provide more fundamental security? And arguably a more permanent security solution?

Data security experts call this Security By Design. It is obvious that solving a problem at the source is a fundamentally better approach than providing symptomatic relief to the problems. This is true in the case of data security as well. In order to achieve the solution (against the threat of DPA and DEMA) at the source, chip designers and architects need to build the security into the architecture.

Security needs to be a deliberate design specification and needs to be worked into the fabric of the design. Encouragingly, more and more chip designers are moving away from addressing security as an afterthought and embracing security by design.

As an industry, we design chips for performance, power, yield and testability. Now it is time to start designing for security. This is especially true for chips used in IOT applications. These chips tend to be small, have limited computational power and under tight cost constraints. It is, therefore, difficult, and in some cases impossible, to apply security patches as an afterthought. The sound approach is to start weaving security into the building blocks of these chips.

In sum, designing security into a chip is as much about methodology as it is about acquiring various technology and tools. As IoT applications expand and the corresponding demand for inherently secure chips grows, getting this methodology right will be a key to successful deployment of secure IoT systems. ◆



Date January 27 - 29, 2016 Venue Hall A·B·C·D COEX, Seoul Organizer SEMI

www.semiconkorea.org 82-2-531-7800



Pre-register Now for complimentary admission

November 16 to January 20

Co-located with

















ADVANCED PLATING For the rest of US – A total package



YES, IT INCLUDES World-Class Process Development!

Performance, price — and unbeatable process development support

You've probably heard how much performance ClassOne's \leq 200mm electroplating systems deliver — for roughly *half* the prices you'd pay elsewhere. Well, that's just the start. Where ClassOne *really* shines is in helping you develop your plating processes.

Get serious help from world-class plating experts

Some users tell us they want to start electroplating for process improvement, but they're not sufficiently experienced in it. That's OK, because our team has literally hundreds of combined years of experience in developing ECD processes and processing equipment; and we *love* to help our customers!

Some equipment makers just drop off your new tool and wish you luck! But at ClassOne, our most important job is helping you to get up and running — and get your processes optimized!

We've got you covered, start to finish

Our new Applications Lab in Atlanta is world class and fully equipped with all the right tools. It's not only for showing plating systems in operation — it's where we help you set up processes, start to finish.

We can support you in putting together new processes from scratch. We can process wafers and measure results. We can help you screen and select the right chemistries. And we can advise you on options and integration each step of the way — to dial in your processes exactly the way you want them.

Come see for yourself

We're here to help you succeed, and world-class process development support is a key part of that plan. Visit our Atlanta apps lab and see what we mean! Call us: (406) 407-7814. Or email: info@classone.com.

* * * * * *

Classone TECHNOLOGY

Advanced Plating For the Rest of Us

Learn more about all of our systems at www.ClassOne.com
