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JANUARY 2013

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Insights for Electronics Manufacturing

Taking Imagers to a Higher Level P. 14

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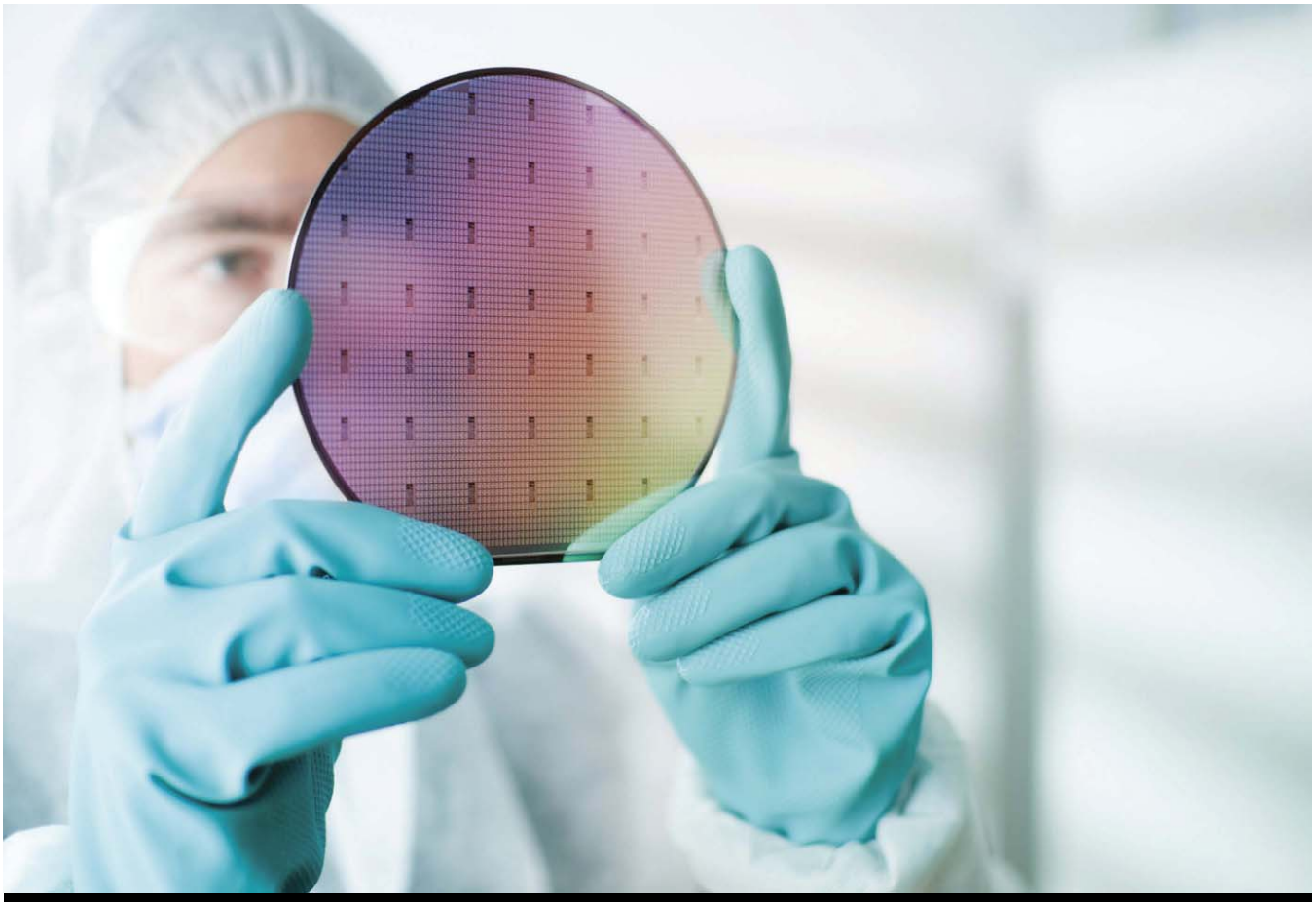

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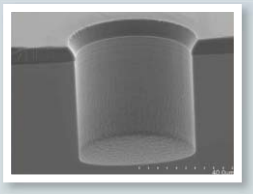
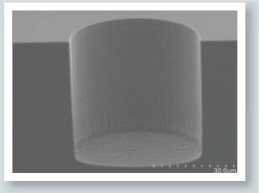
TSV CLEAN AND RESIST STRIP

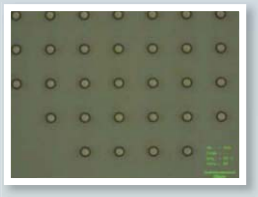


After DRIE

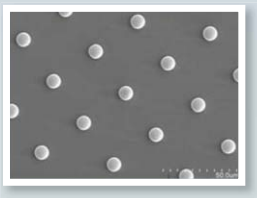


After SSEC Cleaning

Si ETCH TO REVEAL Cu VIAS



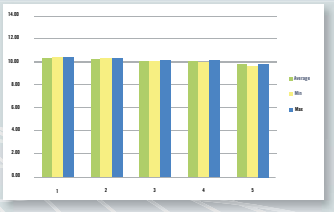
Optical



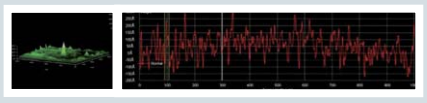
SEM

WET ETCH WAFER THINNING AND STRESS RELIEF

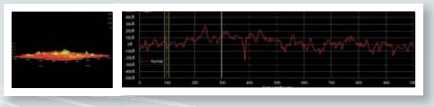
Wafer Thinning



≤ 2% Uniformity of Etch with TTV Unchanged

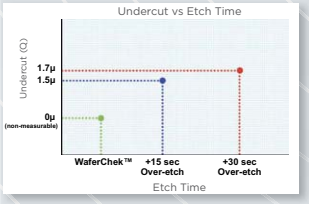


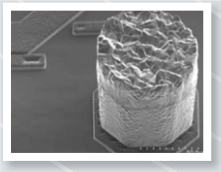
Before Etch (Surface Roughness)



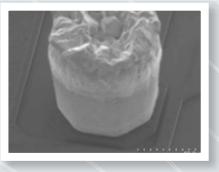
After Etch (Surface Roughness)

UBM AND RDL METAL ETCH



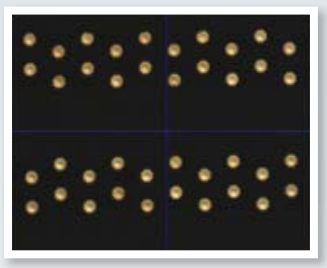


Before Etch

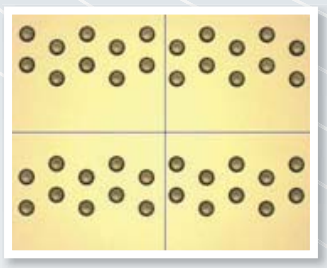


After Etch

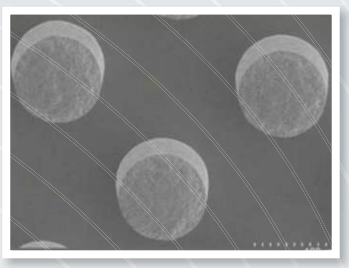
PHOTORESIST AND DRY FILM STRIP

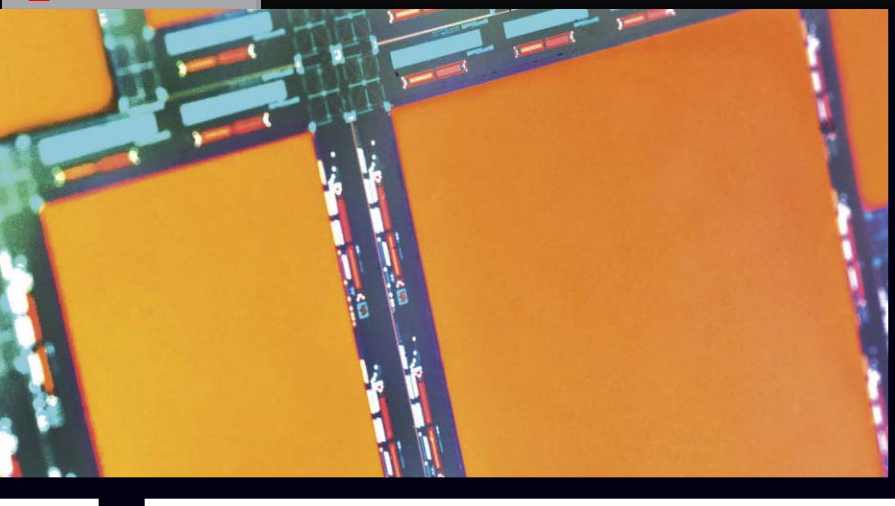


Pre-strip



Post Dry Film Strip





Solid State TECHNOLOGY®

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A flexible fab is required to make innovative imaging systems. Source: imec.

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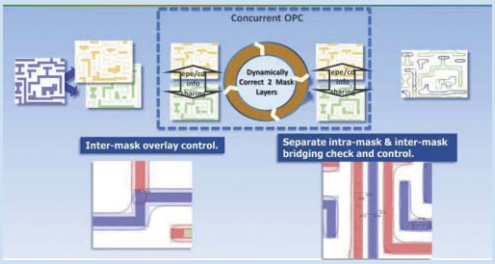
Web Exclusives

Innovations in computational lithography for 20nm

Several innovations in computational lithography have been developed in order to squeeze every possible process margin out of the lithography/patterning process. Gandharv Bhatara, product marketing manager for OPC technologies at Mentor Graphics, describes two specific advances that are currently in deployment at 20nm, in the areas of double patterning and OPC. http://bit.ly/ULXhXW

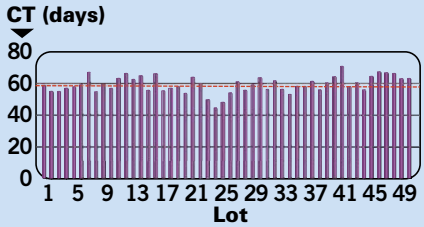


CES 2013: The brains behind smart devices are front and center

Todd Traylor, Vice President of Global Trading for Smith & Associates, reports that consumer devices and cutting-edge tech made the Consumer Electronics Show (CES) exciting. Traylor reviews Qualcomm's Snapdragon 800 and 600 series, Nvidia's Tegra 4, Samsung's Exynos 5, Intel's Bay Trail, AMD's Temash and Kabini chips, and Broadcom's Gigabit DOCSIS SoC, among others. http://bit.ly/XoTWyv

Cycle time's paradoxical relationship to inspection

Because of its rich benefits, reducing cycle time is nearly always a value-added activity. However, reducing cycle time by eliminating inspection steps may be a short-sighted approach, writes KLA-Tencor's Doug Sutherland and Rebecca Howland, in this installment of the Process Watch series. http://bit.ly/13X2xgk



n&b news and blogs

Questions and answers on FD-SOI

Our newly added ability to comment on articles triggered an interesting exchange on fully-depleted silicon-on-insulator between a reader and an executive from ST Microelectronics. http://bit.ly/10zhwgL

Insights from the Leading Edge

Dr. Phil Garrou reports on the Research Triangle Institute-sponsored Architectures for Semiconductor Integration and Packaging Conference, and takes issue with CFLs in an entertaining "Lester the Lightbulb" series. http://bit.ly/10hZRFu

IBM surprises with 22nm details at IEDM

Chipworks' Dick James reports on IBM 22nm SOI high-performance technology, aimed at servers and high-end SoC products. http://bit.ly/WAJoLy

MEMS new product development

MEMS-developer David DiPaola kicks off his first blog, which will discuss the critical factors needed for success in the early stage of new product development. http://bit.ly/13Z1ifE

editorial

450mm progressing

One of the highlights of SEMI's Industry Strategy Symposium — held in January in Half Moon Bay, California — was the first public presentation of a fully patterned 450mm silicon wafer.

Intel's Robert E. Bruck, corporate vice president and general manager of Technology Manufacturing Engineering asked Mario Abravanel, Intel 450mm Equipment Program Manager, to join him on stage. Abravanel appeared from behind the stage, carrying the wafer with gloved hands. "It's real," Bruck said, noting that the wafer was patterned with 26nm features using nano imprint lithography. Bruck singled out wafer-supplier SUMCO, Dai Nippon Printing for partnering in the mask area, and Molecular Imprints for imprint technology. "It shows that a true partnership can move this thing forward," he said. Bruck said that Intel will be producing thousands of 450mm wafers in the next few quarters for their equipment partners to use in their own equipment development.

> "The triumvirate of Intel, Samsung and TSMC is telling us 2017."

Bruck, during his presentation, noted that fewer companies are capable of delivering Moore's Law -- and fewer capable of 450mm production. He showed that about 20 semiconductor companies have the $3-5 billion revenue "threshold" (measured in 2011 dollars) to build a 200mm fab. Only nine have revenue, in the $9-12 billion range, which is the threshold for a 300mm fab (those being Intel, Samsung, TSMC, Toshiba, TI, Renesas, ST Micro, Qualcomm and Hynix). "In 300mm configurations, there's a much smaller group that can afford a reasonable capital cost as a percentage of revenue," Bruck said. "If you extend this 300mm model out a few more years, anticipating the next few nodes that come, the list of participants who can afford to build these factories gets even smaller. Somewhere beyond 2015 will be a 450 number which suggests even further concentration."

The exact timing of 450mm production was explored at ISS in a panel session hosted by Alix Partners. Chris Danely, Managing Director, Semiconductor Equity Research, JP Morgan, said: "From the Wall Street perspective, the triumvirate of Intel, Samsung and TSMC is telling us 2017. 2018 is when it starts to ramp."

—Pete Singer, Editor-in-Chief

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USA | **Ziptronix** signed a licensing agreement with **Novati Technologies Inc.** for the use of its patented direct bonding technologies.

ASIA | **Samsung** grabbed the No.3 foundry spot as a result of dominance in smartphones, according to IC Insights.

USA | An **IBM Research** team won the Feynman Prize for scanning probe microscopy.

WORLD | **SEMI**'s HB-LED Standards Committee has approved its first standard, specifying sapphire wafers used in making high-brightness light-emitting diode (HB-LED) devices.

WORLD | **SK Hynix** has entered into new eight-year patent licensing agreements with **Tessera Inc.** and Invensas, making it the first DRAM maker to gain access to both companies' patents, according to the firms.

USA | **Ultratech** has acquired the assets of **Cambridge Nanotech**, a developer and supplier of atomic-layer deposition technology with hundreds of installed systems in the field.

WORLD | **Oxford Instruments** acquired **Asylum Research**, a maker of scanning probe microscopes.

USA | **Axcelis** and **Lam Research Corp** announced a strategic collaboration agreement focusing on the interrelationship between ion implantation, etch processes, and photoresist strip applications.

World's most complex 2d laser beamsteering array demonstrated

RADAR works by reflecting RF waves off of a target, which return to the RADAR system to be processed. The amount of time it takes to return correlates to the object's distance. In recent decades, this technology has been revolutionized by electronically scanned (phased) arrays (ESAs),

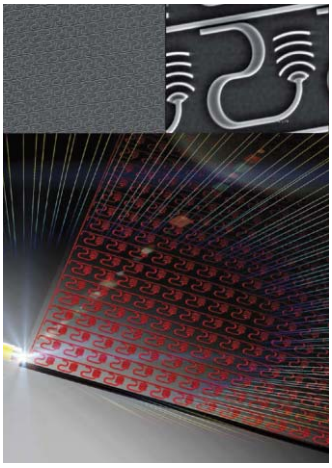

Photo: DARPA researchers used nanoantennas to fabricate the LADAR array. Source: MIT.

which transmit the RF waves in a particular direction without mechanical movement. Each emitter varies its phase and amplitude to form a RADAR beam in a particular direction through constructive and destructive interference with other emitters.

Similar to RADAR, laser detection and ranging, or LADAR,

Continued on page 9

Semi execs see a bright 2013, says survey

In its annual study, KPMG found three quarters of semiconductor executives polled believe they will see revenue growth in the next fiscal year — that's up from 63% in the previous survey. Two-thirds expect to hire more workers (vs. 48% in 2011), and 71% say annual industry profitability will increase in 2013. Overall their sentiment is for a recovery that builds up steam especially heading into the second half of the year.

KPMG's Global Semiconductor Survey, conducted in September, surveyed 152 semiconductor industry business leaders (primarily senior-level execs) at device, foundry, and fabless manufacturers, half of whom have annual revenue of $1 billion or more. Overall, its "Semiconductor Business Confidence Index" climbs to 57, stepping across the 50/50 threshold into optimism vs. the index of 46 recorded a year ago. Among its other findings:

— **More activity, inside and out.** Seventy-three percent of respondents expect to increase capital spending over the next

Continued on page 10

news cont.

Semiconductor leaders see massive industry transformation

The semiconductor industry is undergoing massive transformation as the rise in mobile computing, changes to the fabless-foundry model, uncertainties in technical innovation, and global macroeconomic trends become the dominant forces in 2013 and beyond, according to industry leaders speaking at the SEMI Industry Strategy Symposium (ISS).

Ajit Manocha, CEO of GlobalFoundries, during his keynote presentation discussed the dynamic technology and economic needs of mobile computing that is driving new approaches to the chip design-to-production cycle. Calling it "Foundry 2.0," he sees outsourced semiconductor manufacturing moving toward a more IDM-like model, creating new collaboration models and techniques to close the gap between process teams at foundries and design teams at the fabless companies. With daunting technical challenges like 3D stacking, 450mm fabs, new transistor architectures, multi-patterning, and the uncertainties to lithography-based scaling, product development paths with virtual teams will evolve and adapt rapidly in the coming months and years.

With new fabs now costing upwards of $8 billion and leading-edge manufacturing investments expected to exceed $40 billion this year alone, global economic trends and forces — increasingly influenced by uncertain consumer spending in both developed and emerging markets — have never been important to the semiconductor ecosystem. Dr. John Williams, president and CEO of the Federal Reserve Bank of San Francisco, said "Many businesses are locked into a paralyzing state of anxiety."

Williams used the ISS conference to lessen uncertainty and anxiety in the capital markets, pledging to keep interest rates near zero until the unemployment rate drops to 6.5%, as long as inflation expectations do not climb above 2.5%.

Bruce Kasman, chief economist and managing director of global research at JP Morgan, shared a positive economic outlook, especially in the second half of the year, that is "bumpy, better and less risky." He sees Asia leading the economic rebound, as China demand accelerates with the change in leadership and improved access to credit. University of Texas Austin Churchill scholar, Matthew Gertken, however, discussed the simmering "Asian cold war" developing as territorial disputes with China generate an emerging "containment policy" by many of China's neighbors.

GlobalFoundries adding R&D facility to NY fab campus

GlobalFoundries says it plans to build a $2 billion R&D facility at its Fab 8 campus in Saratoga County, NY. The new Technology Development Center (TDC) will span more than 500,000 sq. ft of "flexible space" for various technology development and manufacturing activities, including cleanroom and lab space. Construction is planned to begin in early 2013 and completed in late 2014.

The TDC will focus on a variety of semiconductor development and manufacturing work "to support the transition to new technology nodes," and development of "innovative capabilities to deliver value to customers beyond the traditional approach of shrinking transistors," according to the company. Broadly speaking, the TEC is planned to be a collaborative space to develop "end-to-end solutions covering the full spectrum of silicon technology," from EUV lithography photomasks to new interconnect and packaging technologies enabling 3D chip stacking, "and everything in between."

Fabless IC sales rise

IC Insights says fabless IC suppliers saw sales rise 6% in 2012, compared with a -4% decline by IDMs (those with their own IC fabs), and the overall market's -2% decline for the year.

Since 1999, the firm tracks, fabless company IC sales have outpaced IDMs (or the decline has been less severe) in every year except 2010. That year was an outlier largely because of strength in DRAM and NAND flash memory, areas in which fabless companies don't have a presence, the firm points out.

Since 1999, fabless IC sales started out as roughly 7% of IDM sales, but have steadily risen and now make up about 27% of total IC sales. And fabless IC market CAGR from 1999-2012 was 16% vs. the overall industry's 5% CAGR. More comparison metrics: fabless IC sales are at levels 7× what they were in 1999, vs. 50% for IDM IC sales, and IDM IC sales are now only 10% higher than 2000 and actually lower than they were in 2007.

By 2017, fabless IC companies will command a full third of the total IC market, IC Insights predicts, and this could be easily attained especially if larger companies (e.g. IDT, LSI Logic, Agere, and AMD) become entirely fabless. "Over the long-term, IC Insights believes that fabless IC suppliers, and the IC foundries that serve them, will continue to become a stronger force in the total IC industry," the firm notes.

news cont.

SRC, DARPA unveil university research center network

Semiconductor Research Corporation (SRC) and the Defense Advanced Research Projects Agency (DARPA) announced that $194 million will be dedicated during the next five years to six new university microelectronics research centers to support the continued growth and leadership of the U.S. semiconductor industry.

The new Semiconductor Technology Advanced Research network (STARnet) includes:

- the Center for Future Architectures Research (C-FAR) at the University of Michigan;
- the Center for Spintronic Materials, Interfaces and Novel Architectures (C-SPIN) at the University of Minnesota;
- the Center for Function Accelerated nanoMaterial Engineering (FAME) at the University of California, Los Angeles;
- the Center for Low Energy Systems Technology (LEAST) at the University of Notre Dame;
- the Center for Systems on Nanoscale Information fabriCs (SONIC) at the University of Illinois at Urbana-Champaign; and
- the TerraSwarm Research Center at the University of California, Berkeley.

"STARnet is a collaborative network of stellar university research centers whose goal is to enable the continued pace of growth of the microelectronics industry, unconstrained by the daunting list of fundamental physical limits that threaten," said Gilroy Vandentop, the new SRC program executive director.

STARnet is funded by the DARPA as part of the Department of Defense and U.S. semiconductor and supplier industries as a public-private partnership. Annually, $40 million is dedicated to the program, with each center receiving about $6 million.

Singapore IME launches 2.5D silicon interposer MPW

Singapore's Institute of Microelectronics (IME), a research institute of the Science and Engineering Research Council of the Agency for Science, Technology and Research (A*STAR), has launched a new multipro-ject wafer service (MPW) for 2.5D through-silicon interposers, to provide a cost-effective platform for R&D prototyping and proof-of-concept in the technology.

The 2.5D interposer MPW service, supported by IME's 3D through-silicon via (TSV) engineering line, includes the following modules:

- Leveraging industry standard Electronic Design Automation (EDA) tools to perform 2.5D TSI design, extraction and verification;
- TSV with critical dimension (CD), e.g. 10-50μm;
- Chip-to-wafer (C2W) interconnects with micro-bump;
- Front and backside redistribution layers (RDL) with thin wafer handling (for thickness down to 100μm and below) with bonding and debonding;
- Under-bump metallurgy (UBM); and
- Chip-to-wafer stacking.

It comes with comprehensive design kits, via and redistribution/bumping technology, as well as packaging and assembly capabilities. It is for academic, research and industrial customers wanting to develop 2.5D research test vehicles with leading-edge designs, materials, and processes to be used in smart phones, tablets, networking and sensors and bio-medical applications.

"Through our MPW platform, our partners will be able to overcome cost and technical hurdles and significantly reduce development time and cost as they transit to mass production," stated Prof. Dim-Lee Kwong, executive director of IME.

IME and Tezzaron teamed up to develop 2.5D silicon interposers in 2011. "Early work from the IME 300mm interposer line has already provided detailed insight into the performance benefits offered by 2.5D interposers," noted Tezzaron CTO Robert Patti.

2d *Continued from page 5*

scans a field of view to determine distance and other information, but it uses optical beams instead of RF waves. LADAR provides a more detailed level of information that can be used for applications such as rapid 3-D mapping. However, current optical beam steering methods needed for LADAR, most of which are based on simple mechanical rotation, are simply too bulky, slow or inaccurate to meet the full potential of LADAR.

DARPA researchers have recently demonstrated the most complex 2-D optical phased array ever. The array, which has dimensions of only 576µm x 576µm is composed of 4,096 (64 x 64) nanoantennas integrated onto a silicon chip. Key to this breakthrough was developing a design that is scalable to a large number of nanoantennas, developing new microfabrication techniques, and integrating the electronic and photonic components onto a single chip.

"Integrating all the components of an optical phased array into a miniature 2-D chip configuration may lead to new capabilities for sensing and imaging," said Sanjay Raman, program manager for DARPA's Diverse Accessible Heterogeneous Integration (DAHI) program. "By bringing such functionality to a chip-scale form factor, this array can generate high-resolution beam patterns — a capability that researchers have long tried to create with optical phased arrays. This chip is truly an enabling technology for a host of systems and may one day revolutionize LADAR in much the same way that ESAs revolutionized RADAR. Beyond LADAR, this chip may have applications for biomedical imaging, 3D holographic displays and ultra-high-data-rate communications."

news cont.

STMicro: 28nm FD-SOI is ready for manufacturing

STMicroelectronics is getting out of the JV chip business with Ericsson, but it's still full-steam ahead for its use of fully-depleted silicon-on-insulator (FD-SOI) technology with its partners.

The "feature-complete and silicon-verified" 28nm planar FD-SOI Technology Platform, now open for preproduction from the Crolles 300mm manufacturing facility, encompasses a full set of foundation libraries (std-cells, memory generators, I/Os, AMS IPs, and high speed interfaces), and a design flow ideally suited for developing high-speed and energy-efficient devices. Measurements on a multi-core subsystem revealed a maximum frequency exceeding 2.5Ghz and delivering 800 MHz at 0.6V, according to Jean-Marc Chery, EVP/GM, digital sector, and CTO/chief manufacturing officer of STMicroelectronics.

"Post-processing wafer testing has allowed us to prove the significant performance and power advantages of FD-SOI over conventional technologies, building a cost-effective industrial solution that is available from the 28nm node," he stated. ST-Ericsson will use the FD-SOI technology in its future mobile platforms demanding high performance yet low power consumption.

Porting libraries and physical IPs from 28nm bulk CMOS to 28nm FD-SOI is "straightforward," and the process of designing digital SoCs with conventional CAD tools and methods in FD-SOI is identical to bulk, due to the absence of MOS-history-effect, ST says. FD-SOI enables production of highly energy-efficient devices (dynamic body-bias allows instant switch between high-performance mode and a very-low-leakage state), transparently for the application software, operating system, and the cache systems. FD-SOI also can operate at significant performance at low voltage with superior energy efficiency versus bulk CMOS.

Semi *Continued from page 5*

fiscal year, up from 51% a year ago — and 24% expect to increase spending by 10% or more, vs. 10% of respondents in late 2011. Just 6% of respondents expect capital spending cuts, s. 18% a year ago. Similarly, 77% of execs expect semiconductor-related R&D spending to increase in 2013, up from just 65% a year ago. And two thirds of execs expect more merger and acquisition deals in fiscal 2013, up from 62% a year ago looking into 2012's crystal ball.

— **The US is tops again.** Execs placed the US ahead of China in the most important geographic markets for semiconductor revenue growth three years out — for a third consecutive year, fewer see China as their most important market. Next in priority are Europe, Korea, and then Taiwan — which two years ago was ranked 2nd and slightly ahead of the US, but might be losing favor due to exposure to softer Japanese and Chinese economies, according to Gary Matuszak, global chair of KPMG's Technology, Media and Telecommunications practice. Also, "significantly" fewer chip execs viewed China as a top-three hiring market in 2013; it's still in first place, but the US and Europe are gaining favor.

— **Consumer is king, redux.** Consumer applications are officially the most important revenue driver, as viewed by the chip execs over the next fiscal year; computing now ranks third, behind wireless. "Unlike past recoveries, this one won't be driven by wireless handsets and wireless communications alone," said Matuszak. Other revenue-driving apps — industrial, medical, automotive (with many sub-applications in body electronics, communications convergence, and safety), and power management (a big feature in wireless devices) — were emphasized by more chip execs in this year's survey than in the past three years. That's a clear indication how semiconductors have proliferated beyond traditional wireless and computing applications, such as mobile commerce and various automotive functionalities, added Ron Steger, global chair of KPMG's Semiconductor practice. Also getting a big push from semi execs: "renewal energy" such as battery technologies, listed by 53% of execs as an important revenue driver over the next three years, up from just 36% a year ago.

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450mm is the next big opportunity

A major challenge facing the industry in the coming year is how to deliver products faster without affecting budgets or compromising safety and quality.

The continued technology innovations will still support investment, and the ongoing move to mobile computing is a major driver in everyone's forecast. The bottom line is that the industry will continue to advance, with Moore's Law and economics driving market opportunity. From a US standpoint, we must continue to invest in emerging technologies and maintain our leadership status as an R&D center of excellence -- driving investment is important. At the same time, we can't continue to afford to just innovate here then provide incentives to drive manufacturing overseas. We must find a way to keep heavily IP-weighted manufacturing in the US. What has happened in New York is a great example. Previously known for high labor rates, now some of the top manufacturers in the industry are bringing their manufacturing there, proving the US is not only an innovator, but a viable producer of a quality product at a lower total cost.

Most notably, in semiconductor manufacturing, 450mm is the next big opportunity. Issues of economic scale and complexity will force fab designers, OEMs and process integrators to investigate all open avenues in the search for solutions to the huge challenges that accompany 450mm. Next generation fabs present new challenges with respect to the design of the facilities, substrate handling, tool connection, chemical distribution, water and electrical systems and other areas. A transition to a bigger wafer size will bring many opportunities – some of which include helping to evolve the way we fabricate devices, introducing different chemistries, supporting greener, more sustainable builds and improving the efficiency of the entire process infrastructure.

Joe Cestari, Total Facility Solutions

The general idea that was used to develop 300mm equipment was to simply scale 200mm tools. From a cost and physical size standpoint, this approach simply won't be adequate to achieve success for 450mm. We must innovate in terms of process technology, substrate handling/transport and process flexibility. "Point of Process" sensing and control technology will be critical, since remote subsystems (in the sub-fab) will not be sufficient for 450mm -- the tool will really need to be an integrated process line. In short, we need to understand the 450mm impact to the fab facility infrastructure

Right now, with 450mm in its infancy, no one really knows what to expect, especially with regards to tool installation and hook up as design packages aren't ready yet and in some cases the tools don't even exist. The transition faces numerous challenges, as is the nature of the business.

Given the industry's pressures on profitability and the challenges of the current economic climate, there is significant incentive for a collaborative supply chain. Collaboration has become essential even in the earliest stages of the planning and building of any semiconductor manufacturing facility, but given the enormity of the 450mm opportunity, a high quality, cost-effective supply chain performance becomes even more important. In addition, the consortia model or the Japanese Koretsu model will also be necessary. The number of manufacturers and suppliers in the 450mm ecosystem will be small, so standardization, joint investment or joint development will be of paramount importance. It won't work to simply give a supplier a spec and price target and say, "make this for me asap."

Semiconductors

Printed, flexible electronics scaling up

Excitement is building in the world of printed and flexible electronics. Recent announcements of flexible and curved displays for mobile phones, TVs and other consumer devices will push technologists to solve scale-up challenges in manufacturing, helping migrate products from prototypes to mass production.

Printed electronics are not limited to consumer goods either. The medical device market, estimated at over $300 billion, also benefits from advancements being made in printed electronics. According to Lux Research, the overall value proposition of printed, flexible and organic electronics revolves primarily around lower-cost replacements for non-printed devices, and flexible devices that will enable increased wearability.

Many materials manufacturers, capital equipment providers, and product integrators are hard at work reducing materials costs, improving device performance and increasing the reliability of printed electronic devices in an attempt to create these lower cost replacements for non-printed devices.

For example, there has been a lot of innovation in display manufacturing. E Ink is mass producing a plastic active matrix electrophoretic reflective display that has been launched for a cell phone product incorporating the best of both display worlds: a daylight readable low power EPD full display on one side and a video color LCD on the other side. LIM Liquids in Motion GmbH uses low power flexible front-planes with full-color and bistable features that can be built based on electrowetting principles.

Displays

Denise Rael,
FlexTech Alliance

UCLA has developed a new transparent composite electrode technology that can match the transparency and sheet resistance of ITO. OLEDs that can be reversibly stretched by up to 50% strain, twisted, and folded have been demonstrated.

On the production front, several advancement s have been made to enable full manufacturing scale-up . Applied Materials has a variety of different web handling & coating technologies that take into account the principal challenges inherent to R2R device manufacture such as choice of substrate, thermal budget, layer stack stress, patterning, and defects. PARC has developed design rules used for lab-scale, ink-jet printed multi-layer complimentary circuits. They are currently translating these designs rules to production scale equipment. AIXTRON has commercialized the principle of organic thin film deposition utilizing an inert carrier-gas for the transport and controlled condensation of small molecules to meet the scale up challenges of high performance devices.

Material providers are also making strides to reach the low-cost promise of printed electronics. DuPont Electronics and Communications is focused on efforts to address cost-centered concerns with a new family of printed conductor materials. Brewer Science has developed a novel method for achieving stable solutions of largely pristine carbon nanotubes without the need for surfactant. Solar Press is developing robust, high throughput roll-to-roll fabrication processes and ink formulations for high performance OPV module production, including low cost production techniques for active layer materials.

The latest developments, applications, and research in printed electronics—including manufacturing technology—will be featured at the 12th annual Flexible & Printed Electronics Conference & Exhibition, to be held January 29-February 1, 2013, in Phoenix, AZ. Hosted by the FlexTech Alliance, the 2013 Flex Conference features over 95 technical papers in 18 sessions on a broad range of topics covering the latest developments in flexible and printed materials, tools, and processes (www.flexconference.org) .

PACKAGING

Interdisciplinarity takes imagers to a higher level

ELS PARTON, PIET DE MOOR, JONATHAN BORREMANS *and* **ANDY LAMBRECHTS**, *imec, Leuven, Belgium*

Specialty processing steps for different apps.

Belgian research institute imec shows the opportunities for imagers when teams of designers, software engineers, technologists, and system designers collaborate. A flexible fab is also a requirement for making innovative image systems. The recipe? Take a 0.13µm CMOS technology and add some back-side illumination technology, specialty processing steps and coatings, 3D stacking, embedded CCD, hyperspectral filters, ... and leverage system-on-chip and technology codesign as well as dedicated software development to open up unprecedented image sensor application fields. Some examples of projects that are the result of this multidisciplinarity are presented.

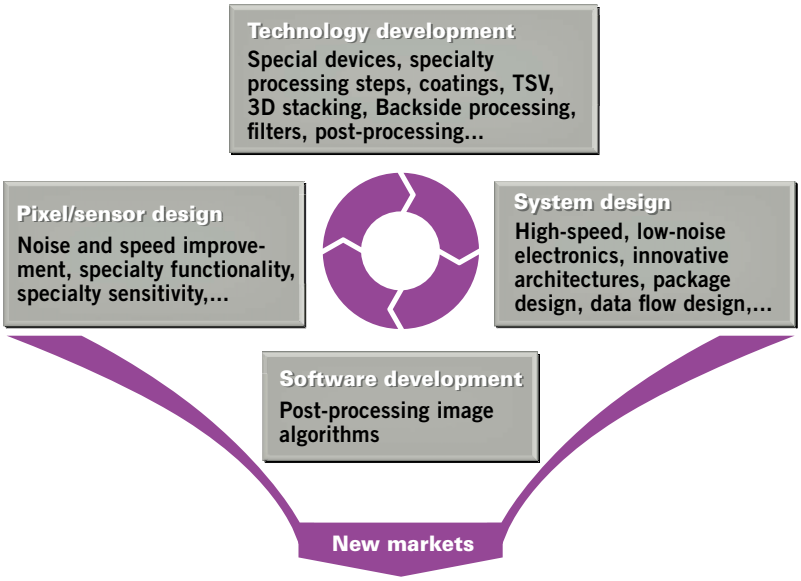


FIGURE 1. Only when technology and design challenges are met together can the image sensor target the application field.

The market

The most widespread imagers today are the ones in our cameras and cell phones. These are standard imagers made in large volumes. However, there is also a market for specialty imagers. For these, no standard solution is available. Often, these imagers have special requirements depending on the application. For example, wafer and mask inspection tools for advanced semiconductor processing require imagers that are sensitive to extreme ultraviolet (EUV) wavelengths; and lab-on-chip solutions require miniaturized microscopes that can recognize cells at a high speed.

The market for specialty imagers is broad—ranging from high-end scientific, space, earth observation, medical imaging, high-end consumer, and machine vision and instrumentation. There is a growing demand from semiconductor equipment manufac-

ELS PARTON *is editor-in-chief of imec's Dutch magazine InterConnect, which highlights trends, technologies, and collaborations with Flemish SMEs.* **PIET DE MOOR** *focuses his current research on advanced CMOS imagers such as back-side illuminated and hybrid imagers suitable for high-end imaging applications.* **JONATHAN BORREMANS** *leads the Imager Design Group at imec.* **ANDY LAMBRECHTS** *leads the Integrated Imaging team and is working on hyperspectral imaging, lens-free microscopy, and other activities.*

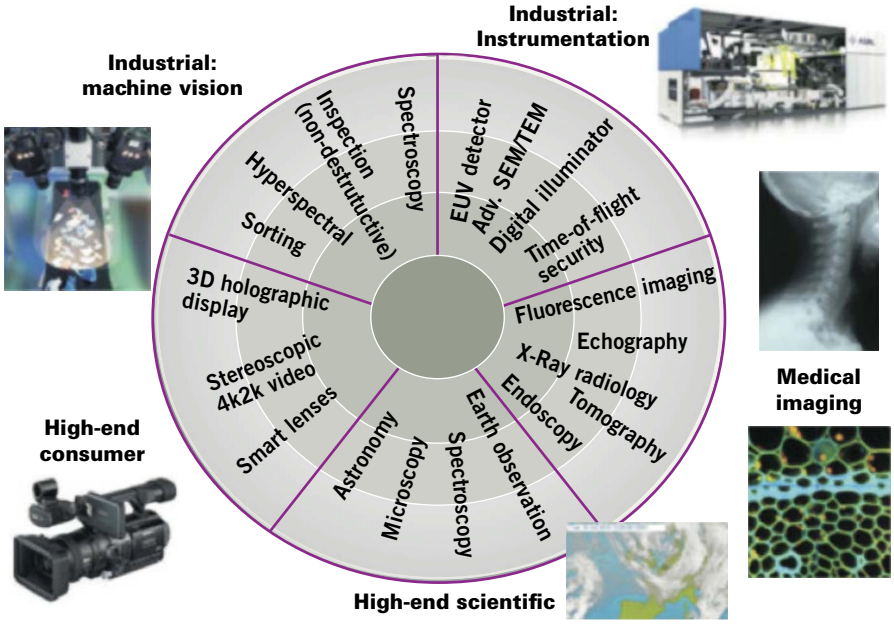


FIGURE 2. The market for specialty imagers is varied. Applications typically require custom-made solutions with a combination of many technologies and expertises.

turers for specialty imagers, and the medical imaging market segment is growing enormously.

New markets come with unprecedented noise, speed, and integration requirements, for example, for advanced high-end industrial tools. These unprecedented specifications necessitate innovative system-on-chip (SoC) design solutions in close collaboration with technology development and software post-processing development. Only when technology and design challenges are met together can the image sensor target the application field.

When analyzing the needs in the market for specialty imagers there is a clear trend towards imagers for non-visible wavelengths (e.g. UV, EUV). Also full SoC imager solutions are hot in the market today. Imec, as a research institute that closely collaborates with industry, has tackled some specific projects for industry. One by one, these projects are a clear illustration of the potential for imagers when bringing together different expertises. Below, we give a few examples of such realizations.

Microlens arrays for e-beam lithography

Reflective electron beam lithography (REBL) uses a beam of electrons to do lithography. The goal is to extend semiconductor manufacturing to the 16nm technology node and beyond. Electron beam lithography exists, but suffers from long writing times because this is essentially a serial technique. The advantage of the current development is that it enables writing of 1 million electron beams in parallel, leading to fast throughput.

A process for the fabrication of an electrostatic micro-lens (lenslet) array for the REBL tool has been developed. The lenslet device consists of an array of holes with a diameter of 1.4µm on a 1.6µm pitch. These holes are patterned through a stack with a total thickness of 4µm. This stack, consisting of electrode and insulating layers, acts as an electrostatic lens. By applying different voltages to the electrodes, electric fields are created that focus and either absorb or reflect an incoming electron beam.

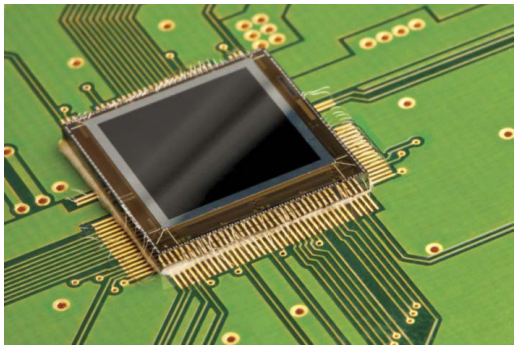


FIGURE 3. Back-side-illuminated hybrid imager (1 Mpixel) connected to a CMOS readout circuit. Back-side-illuminated imagers show an improved light sensitivity as compared to conventional frontside-illuminated CMOS image sensors.

The development of the lenslet structures together with the interconnects poses many design and processing challenges. A litho and etch process was developed to pattern the high aspect ratio devices with good overlay to underlying electrode layers. Bond pad and via design were done using some unconventional integration approaches

in order to remain compatible with the lenslet processing steps.

EUV sensors

EUV detection is needed for EUV lithography tools and wafer and mask inspection equipment. The imagers for these applications require detection of light with an extremely short wavelength. Such light typically has a very limited penetration depth in silicon and dielectrics. Also, lithography equipment requires high doses, which cause reliability issues in the EUV sensors.

Photodiodes were fabricated with a special structure. Key is a dedicated passivation that enables EUV penetration from the top to reach the sensitive silicon. These detectors can be used to sense the EUV dose in lithography tools. However, to check the uniformity, a 2D array is needed. For this reason, future work will focus on developing a complete imager. To do this, concepts like back-side illumination (BSI) become important.

Most imagers today use front-side illumination. The light has to go through the back-end-of-line with the metals and dielectrics. These materials reflect the light and even absorb part of the light. When you go to light beyond the visible spectrum, this becomes a problem. For this reason, it is better to use in this case the back-side illumination concept for the imager. By applying the BSI concept, EUV imagers become possible for applications such as monitoring the exposure dose, and calibrate, align, and focus the lithography tool's lens systems.

FIGURE 4. Wafer containing hyperspectral filter structures. These spectral filters are based on the principle of the Fabry–Pérot filter. Processed on a camera sensor, this structure can be used for hyperspectral imaging applications.

Hyperspectral filters on top of an imager

Hyperspectral imaging exists today as large, expensive tools typically used in research environments. However, innovative integration of filters and image sensors can turn this around and can enable high-speed, low-cost, and compact hyperspectral cameras. Such cameras could be used for industrial inspection, anti-counterfeiting, food quality control, and medical applications such as screening of skin cancer.

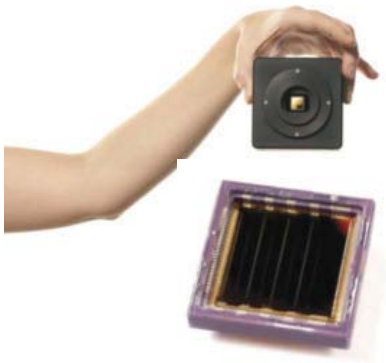
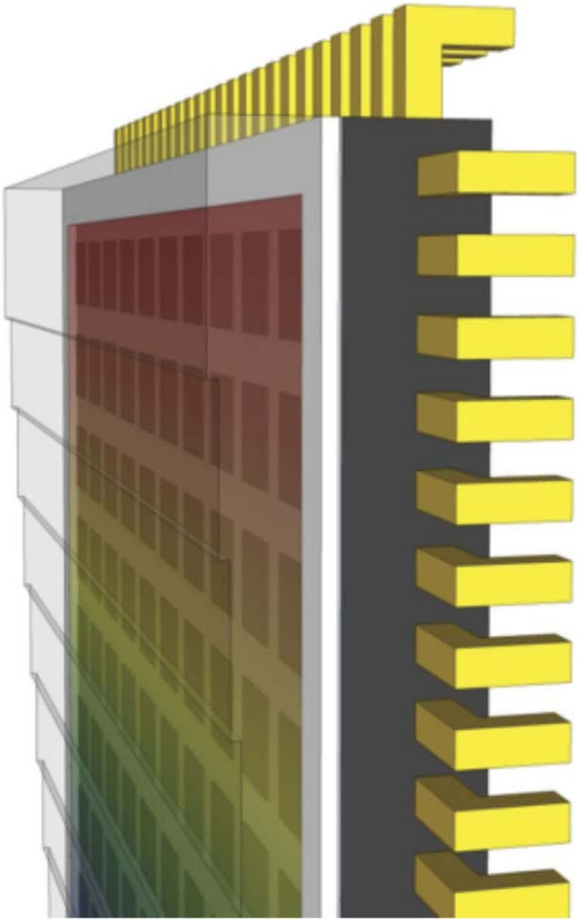


FIGURE 5. Compact hyperspectral camera and hyperspectral image sensor based on the integration of dedicated filters on top of image sensors.



A hyperspectral imager was developed by integrating a group of 100 spectral filters, arranged in the shape of a wedge, on top of

FIGURE 6. Hyperspectral filter structure (stepwise wedge consisting of Fabry–Pérot interferometers) that is directly post-processed on top of the image sensor.

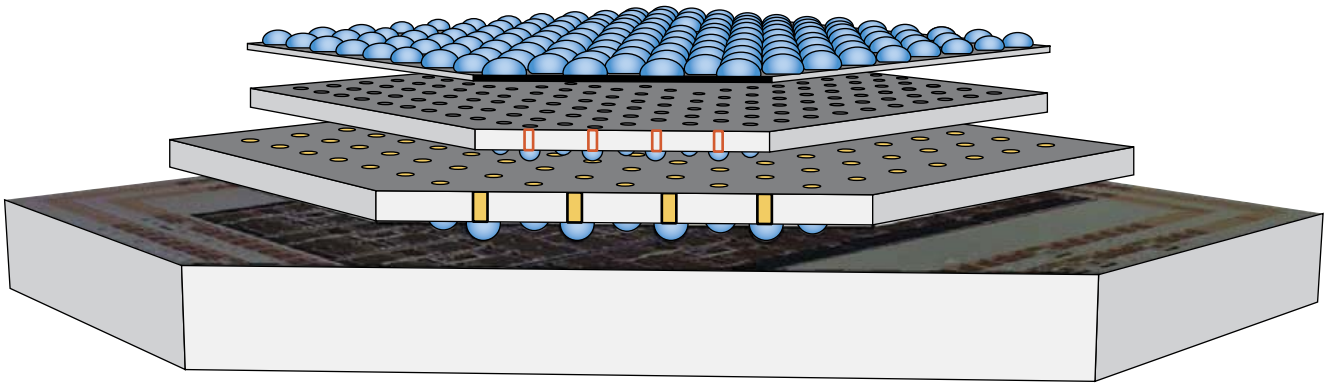


FIGURE 7. Concept of a 3D-stacked imaging system with different active layers for the different functionalities of a smart imaging system

a commercial CMOS imager. To enable the low-cost processing of such a microscopic wedge filter, imec introduced a design that is able to compensate for process variability. The result is a compact and fast hyperspectral camera made with mass-producible and fully CMOS-compatible process technology.

The integrated spectral filters are narrow banded Fabry–Pérot interference filters. The Fabry–Pérot filter is typically made of a transparent layer (called cavity) with a mirror at each side of that layer. The length of the cavity defines the central wavelength of the optical filter and the reflectivity of the mirrors defines the full width half maximum (FWHM) of the filter. Using these filters, different hyperspectral imager designs can be realized. As an example, a line scan hyperspectral imager can record a full 3D cube (i.e. an image in all the different wavelengths) for a linear moving object.

The hyperspectral filters can be processed in principle on any image sensor to match different application specs. Similarly, the spectral range can be tuned, and currently an extended spectral range of 400–1000nm is under development.

System-on-chip imagers

High-end imagers require a lot of intelligence to be integrated in the imager: just think about the complex and fast read-out circuitry needed. The solution is a CMOS-based SoC approach for the imagers. The CCD approach often used for specialty imagers cannot handle this need for integrated intelligence.

For example, analog-to-digital conversion for imagers pushes the boundaries of frame rate and resolution to meet new performance requirements from the application side. A prototype was developed with fast and low-power ADCs for each column on the imager. For high-performance SoC imagers, the co-design of technology, design, and system is essential, as well as a flexible CMOS platform with add-ons such as back-side illumination, embedded CCD, or hyperspectral filters.

3D stacking in imagers

In addition to system-on-chip technology, 3D stacking technology can also be used to make imagers smarter. During the last few years, a lot of development effort has been spent on through-Si vias (TSVs), enabling 3D stacking of active Si dies. The main driver for this technology is memory stacking and memory on logic stacking. This technology is now becoming mature (at the R&D level), and the implementation in industry is expected to happen in the future.

Also for imagers, 3D stacking creates opportunities. A first advantage is the decoupling of functions of different layers in an imager: sensing layer, analog ROIC, ADC, and digital system. Each of the different layers can be optimized separately in the most adequate technology and subsequently stacked. A second advantage is the enhancement of the read-out structure using a vertical interconnect scheme in terms of speed (massive parallel processing), and performance (complex image processing). Thirdly, 3D application mapping allows us to distribute the functionality of a specific sensor in an optimized way over the heterogeneous layers to obtain a cost-efficient realization.

3D INTEGRATION

Laser debonding enables advanced thin wafer processing

THOMAS UHRMANN, *EV Group, St. Florian, Austria, and* **RALPH DELMDAHL**, *Coherent GmbH, Göttingen, Germany*

An economically viable method for delivering throughput in fab equipment.

Thin wafers represent an important technological advance in achieving power devices with higher efficiency, as well as enabling the use of through-silicon-vias (TSV), a critical tool in greater device miniaturization. However, the mechanically delicate nature of thin wafers makes it largely impossible to handle them using existing process equipment and techniques. Temporary bonding of wafers to a thick carrier has emerged as a viable method for back thinning and subsequent backside processing. The processed thin wafers are then debonded from this carrier just prior to stacking.

There are several techniques for performing this debonding, including chemical, thermal, and laser-based methods. This article reviews the basics of the laser debonding process, and some of the practical considerations related to its implementation

Process basics

Figure 1 provides a schematic of the key process steps for thin wafer processing using a temporary carrier wafer. Specifically, a wafer is front-side patterned, and then bonded to a carrier substrate. The wafer is then

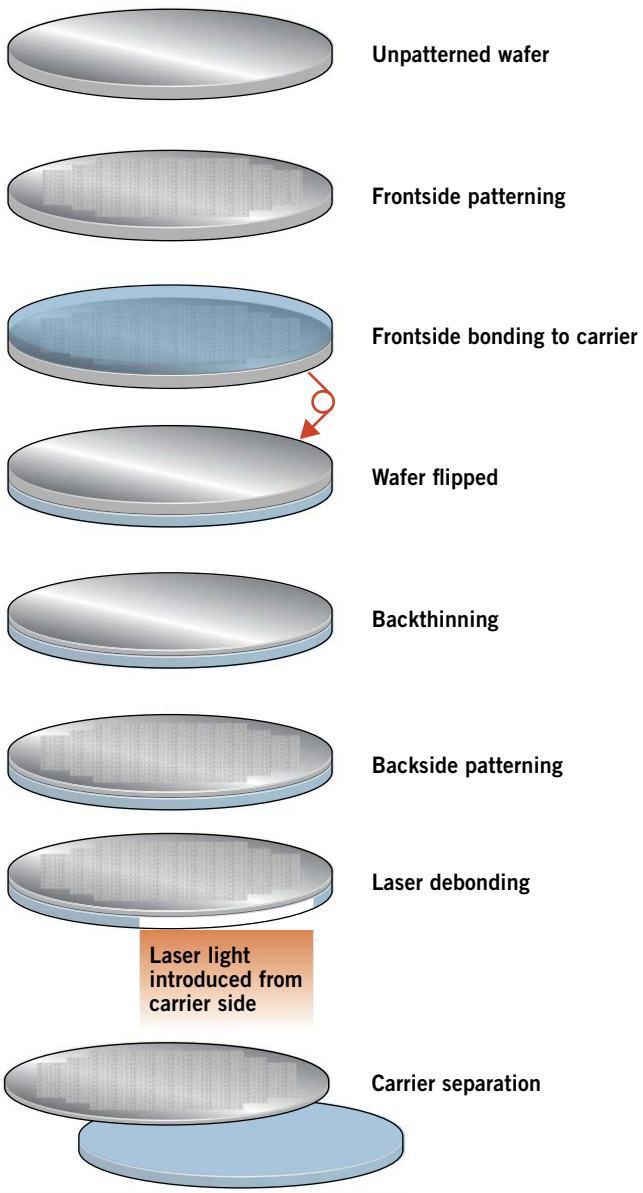


FIGURE 1. Schematic of the key process steps for thin wafer processing using a temporary carrier wafer.

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back-thinned, and back-side processing is performed. Finally, laser light is introduced from the carrier side (which is transparent at the laser wavelength), causing debonding of the wafer from the carrier.

The most important advantage of laser debonding over other techniques is that it enables the use of polyimide-based temporary adhesives that can withstand exposure to temperatures as high as 400°C. This enables the bonded assembly to successfully survive the temperature cycling experienced in steps such as dopant activation after ion implantation. In contrast, most thermally or chemically activated temporary adhesives have difficulties tolerating temperatures above 200°C.

Because of this, laser debonding is most useful for IGBT and silicon-based power devices (MOSFETs, etc.) because these often require ion implantation and activation to create back-side drain contacts. However, for CMOS device wafers, active elements are typically all on the front side, and are thus completed before bonding to the carrier wafer. Furthermore, the eutectic bumps used on CMOS wafers will reflow when exposed to high temperatures so exposure to them is avoided anyway.

Unlike thermal or chemical debonding, which utilize silicon carriers, laser-induced debonding requires the use of glass carriers. In CMOS fabs, where ionic species are particularly undesirable, glass carriers are problematic to implement. Thus, laser debonding is likely to coexist along with other methods, with each having its own market niche.

In practice, the temporary adhesive for laser debonding is most commonly spin coated on to the wafer, which is then mated with the carrier. Bonding then occurs under pressure and elevated temperature. After thinning and back-side processing, the laser-initiated detachment occurs essentially at the glass/adhesive interface. After laser debonding, the glass substrate is lifted off the thinned wafer, leaving some residual adhesive, which is then removed using solvents.

Laser process considerations

The laser debonding process being developed at EVG (**Fig. 2**) is based on excimer lasers operating at either 308nm or 248nm. It's important to differentiate this

FIGURE 2. This high volume production tool from EVG integrates wafer handling robotics together with modules for various processes, such as cleaning, debonding and film frame mounting.

cold process from earlier techniques based on infrared lasers, which penetrate far into the adhesive layer (and sometimes even beyond), and cause debonding through a thermal mechanism (e.g., heating). Oxide layers are put into the assembly to absorb this infrared light, but if these are imperfect and the laser light penetrates through, it can damage wafer structures. After infrared laser debonding, residual adhesive must be physically peeled off.

In contrast, the ultraviolet light emitted by excimer lasers is absorbed very near the glass/adhesive interface, penetrating in just a few hundred nanometers. Thus, it leaves the thin wafer entirely unaffected. Furthermore, the ultraviolet light from the excimer laser debonds through a primarily photochemical means by directly breaking chemical bonds in the adhesive polymer. This non-thermal process breaks down the temporary adhesive at the glass/adhesive interface. Depending upon the polymeric backbone of the temporary adhesive, the precise debonding mechanism may vary. Modern laser debondable adhesives are designed in such way to have an easy and reliable debond, where the carrier wafer can be just lifted off the thinned device wafer.

> It is quite possible to achieve debonding with a single laser shot with a relatively modest power laser.

There are two basic approaches for implementing excimer laser-based debonding, namely, line scanning and step-and-repeat (see **Fig. 3**). In line scanning, the naturally rectangular output distribution of the excimer laser is reshaped into a thin line, which is focused on to the carrier/adhesive interface. The length of this laser line is slightly greater than the wafer diameter, and the width is typically around 200 µm, depending on the laser output power. This line is then scanned over the surface of the wafer a single time in order to produce debonding.

In step-and-repeat, a homogeneous laser square or rectangular field (typically about 5 mm on each side) is projected at the carrier/adhesive interface, and an exposure is made that is sufficient to cause debonding. Then, the wafer is indexed a distance corresponding to the spot height, and the process is repeated until the entire wafer surface is covered.

The mechanical simplicity of the line scan approach more readily lends it to higher throughput. However, it also typically requires a higher power laser because the light is spread over a larger area, thus lowering the energy density. Also, away from the wafer center, much of the laser energy is wasted (since the line goes off the edge of the wafer when the line is anywhere except the very center of the wafer).

Conversely, the step-and-repeat method requires less laser power, yet is still capable of reaching up to

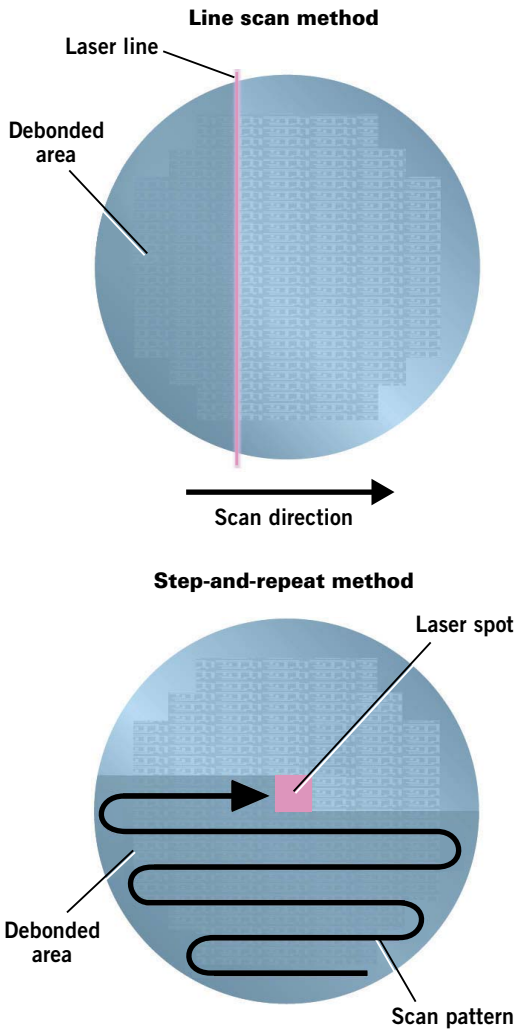

FIGURE 3. Two basic approaches for implementing excimer laser based debonding: line scanning and step-and-repeat.

40 wafers/hour throughput even at low laser pulse frequency of 20Hz. The necessary laser power for step-and-repeat also depends upon the number of laser shots utilized in each exposure. However, it is quite possible to achieve debonding with a single laser shot with a relatively modest power laser.

The minimum required laser power for debonding is also very dependent upon wavelength because of absorption in the glass carrier. Specifically, a typical glass carrier might absorb about 5% of the incident laser light at 308nm, while the absorption at 248nm could be 95%. Thus, nearly 20 times more laser power would be required at 248nm to achieve the same energy density at the glass/adhesive interface as with 308nm. There are also subtle differences in the specifics of the light/adhesive interaction between the two wavelengths. However, EVG has found that both wavelengths can be successfully employed.

Laser cost characteristics

Excimer lasers have long been used for microlithography, but it is important to realize that the types of sources optimum for laser debonding are completely different from those used for microlithography, possessing lower cost, smaller size, and different pulsing characteristics

Microlithography lasers output pulses with low energy, typically in the 20mJ per pulse range and operate at relatively high repetition rates, usually between 4 to 6kHz. These characteristics are desirable because they enable very precise total dosage control (by monitoring total delivered energy and varying the total number of pulses as needed).

Operating an excimer laser at such a high repetition rate translates directly into system complexity and cost. This is because the gas volume between the laser electrodes must be shifted between each pulse. Accomplishing this at a multi-kHz repetition rate therefore requires a relatively powerful and complex blower arrangement. Just as important, excimer laser tubes can only deliver a set number of pulses before they require complete

replacement. So, operating at a higher repetition rate runs through this operational lifetime more quickly, necessitating expense for both replacement parts and maintenance downtime.

In contrast, the lasers used for debonding operate in almost exactly the opposite regime. Specifically, they produce relatively high per pulse energy, typically at the 500mJ per pulse level, while operating at repetition rates of only 10 to 200Hz.

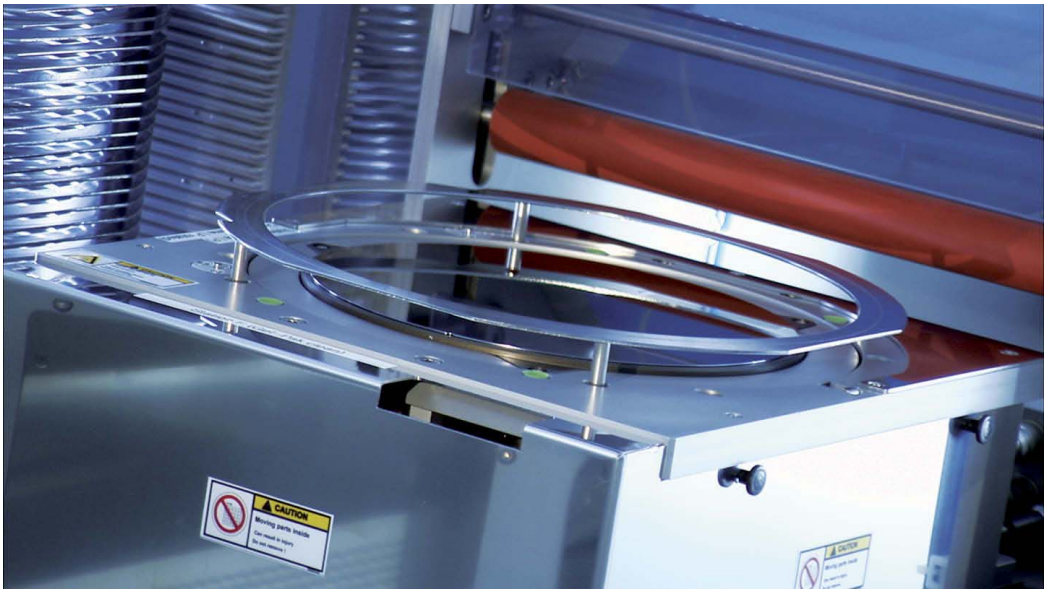

FIGURE 4. In this film frame mounter, the wafer is secured by tape to the frame prior to debonding. This enables the thin wafer to be kept flat and safely handled after debonding has been performed.

This reduced repetition rate, together with a larger internal spacing between electrodes, simplifies the construction and operation of the laser, reducing its capital cost by typically an order of magnitude. Cost of ownership is also reduced: even when combined with three-shift operation, the low pulsing rate results in total pulse counts that are so low that laser tube replacement only occurs at intervals of two to five years.

Microlithography lasers are also optically very complex since stepper systems require very narrow (i.e., extremely monochromatic) laser light. In addition, many microlithography lasers now operate at 193nm, which requires the use of much more expensive optical components than longer wavelengths. And, of course, the beam shaping and projection objective optics used for microlithography (at any wavelength) are quite costly.

Again, none of this is the case with the excimer lasers used for debonding. No line narrowing or wavelength stabilization systems are required, and the beam delivery optics used for both line scanning and step-and-repeat systems are orders of magnitude simpler and less expensive than microlithography optics. Furthermore, operation at 248nm, and especially 308nm, allows the use of much more economical optical materials (e.g. fused silica), which do not have to be replaced frequently.

These simpler debonding excimer lasers are also much physically smaller than microlithography lasers with simpler infrastructure requirements. For example, the Coherent COMPexPro excimer laser family provides 20W of output at 308nm (maximum pulse energy of 500mJ, maximum repetition rate 50Hz), measures only 1682 x 375 x 793mm, and operates from either 110 or 220V standard, single phase power.

In conclusion, laser debonding represents an economically viable method that can deliver the throughput required for fab process equipment. The characteristics of its polymeric adhesives make it particularly advantageous over other debonding techniques in the manufacture of a power device, or any other components that require exposure to high temperature during manufacture.

SPONSORED TECHNICAL PAPER

Automated Test Creation for Mixed Signal IP using IJTAG

MARTIN KEIM and **FRIEDRICH HAPKE**, *MENTOR GRAPHICS*, **TOM WAAYERS** and **RICHARD MORREN**, *NXP SEMICONDUCTORS*

The creation of test patterns for mixed signal IP has been, to a large extent, a manual effort. To improve the process used to test, access, and control embedded IP, the new IEEE P1687 standard 1 is being defined by a broad coalition of IP vendors, IP users, major ATE companies, and all three major EDA vendors. This new standard, also called IJTAG, is expected to be rapidly and widely adopted by the semiconductor industry.

The P1687 standard will enable the industry to develop test patterns for IPs on the IP level without having to know how the IP will be embedded within different designs. Mentor Graphics and NXP Semiconductors (NXP) worked together to implement P1687 on mixed-signal IPs in a 65 nm automotive design. The results demonstrate the significant advantages of P1687 over the current IEEE 1149.1 (JTAG) 2 test methodology, both in automating the test pattern development and in reducing test setup data volume by more than 50%.

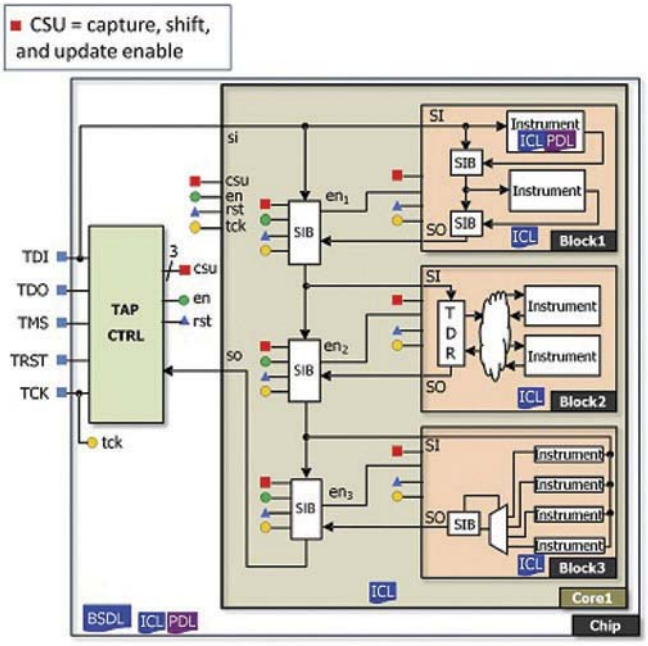

FIGURE 1: Example use of P1687 ICL and PDL.

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SPONSORED TECHNICAL PAPER

A Comparison of High-Purity Fluoropolymer Fitting Technologies

Executive Overview

When selecting a fluoropolymer fitting design to be used in ultra high-purity chemical applications, decision makers must consider different performance characteristics. A recent study was conducted that measured key fitting attributes, such as fitting pull-out force, cleanliness and assembly time. The study compared commercially available nonwetted insert, flare, and wetted insert style fittings. The methodologies employed and the test results are detailed in this paper.

Introduction

Fluoropolymer tube fittings used in ultra high-purity and corrosive chemical applications, such as the semiconductor industry, vary significantly by design type. The ideal fitting design type will result in a very clean connection that is easy to assemble and that provides robust and reliable leak-free service. Fitting performance characteristics should be carefully considered as part of the fitting selection and specification process as they will impact the ultimate performance of process tools and associated chemical distribution systems.

This paper presents the test results from a study that compared performance characteristics of several commercially available fluoropolymer fitting design types.

The following fitting design types were compared in the study.

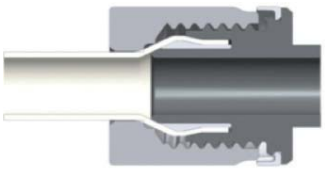

FIGURE 1. Nonwetted insert style fitting

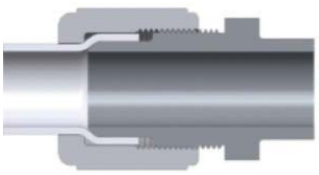

FIGURE 2. Flare style fitting A

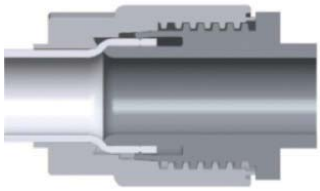

FIGURE 3. Flare style fitting B

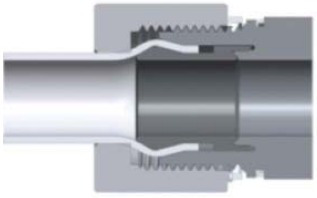

FIGURE 4. Wetted insert style fitting

Taiwan Semiconductor Manufacturing Company Limited

http://www.tsmc.com

Established in 1987, TSMC is the world's first dedicated semiconductor foundry. As the founder and a leader of the Dedicated IC Foundry segment, TSMC has built its reputation by offering advanced and "More-than-Moore" wafer production processes and unparalleled manufacturing efficiency.

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NF Platform—for MEMS Development and Fabrication

FARI ASSADERAGHI, **MIKE DANEMAN**, and **MARTIN LIM**, *InvenSense, Sunnyvale, CA USA*

In order for the MEMS industry to replicate the success of the CMOS fabless model, there is a need for a similar standardized process technology. This will ultimately lead to the proliferation of disruptive MEMS-based solutions for a plethora of applications including motion sensing, navigation for location-based services, wireless communications, health and environmental sensing and many others.

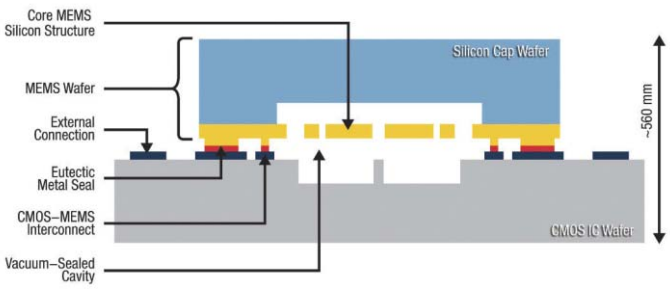

FIGURE 1. Cross section of die through NF Platform wafer-level CMOS-MEMS integration

The paper on MEMS fabrication describes the challenges for MEMS standardization, and introduces InvenSense's patented NF Platform as the most effective way to overcome them. The NF Platform is a versatile fabrication process that can support multiple products, addresses all cost contributions, and is already deployed at the top two CMOS foundries. Attributes of the NF Platform, as well as how to tape out silicon on InvenSense's open NF-Shuttle are also highlighted.

FIGURE 2. A proven fabrication process. Utilized for hundreds of millions of MotionTracking devices

InvenSense
Phone: 408-988-7339
Website: www.invensense.com/nfshuttle
Email: nfshuttle@invensense.com

InvenSense Inc. (NYSE: INVN) is the world's leading provider of MotionTracking™ solutions. The company's patented NF Platform and patent-pending MotionFusion™ technology address the emerging needs of many mass-market consumer applications via improved performance, accuracy, and intuitive motion- and gesture-based interfaces. InvenSense technology can be found in consumer electronic products including smartphones, tablets, gaming devices, optical image stabilization, and remote controls for Smart TVs.

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LEDS

The gleam of well-polished sapphire

REBECCA HOWLAND *and* **TOM PIERSON**, *KLA-Tencor, Milpitas, CA.*

If an LED manufacturer wants to improve yield or reliability, it's important to know the source of the problem.

Is it time for high-brightness LED manufacturing to get serious about process control? If so, what lessons can be learned from traditional, silicon-based integrated circuit manufacturing?

The answer to the first question can be approached in a straight-forward manner: by weighing the benefits of process control against the costs of the necessary equipment and labor. Contributing to the benefits of process control would be better yield and reliability, shorter manufacturing cycle time, and faster time to market for new products. If together these translate into better profitability once the costs of process control are taken into account, then increased focus on process control makes sense.

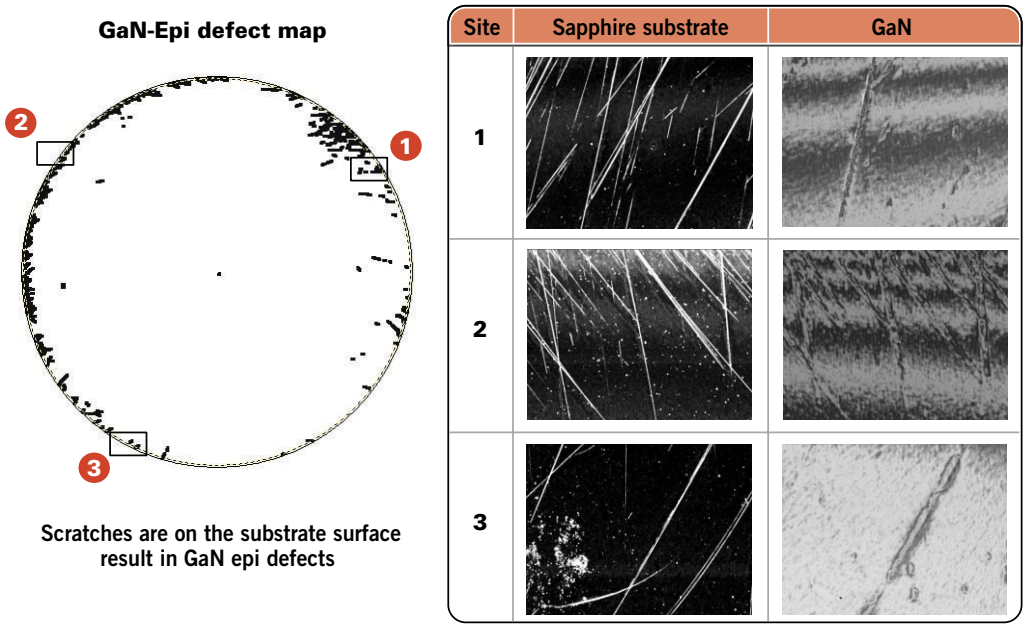

FIGURE 1. Scratches on the substrate surface result in GaN epi defects.

Let's consider defectivity in the LED substrate and epi layer as a starting point for discussion. Most advanced LED devices are built on sapphire (Al_2O_3) substrates. Onto the polished upper surface of the sapphire substrate an epitaxial ("epi") layer of gallium nitride (GaN) is grown using metal-organic chemical vapor deposition (MOCVD).

Epitaxy is a technique that involves growing a thin crystalline film of one material on top of another crystalline material, such that the crystal lattices match—at least approximately. If the epitaxial film has a different lattice constant from that of the underlying material, the mismatch will result in stress in the thin film. GaN and sapphire have a huge lattice mismatch (13.8%), and as a result,

REBECCA HOWLAND, Ph.D., *is a senior director in the corporate group, and* **TOM PIERSON** *is a senior product marketing manager in the Candela division at KLA-Tencor.*

the GaN "epi layer" is a highly stressed film. Epitaxial film stress can increase electron/hole mobility, which can lead to higher performance in the device. On the other hand, a film under stress tends to have a large number of defects.

Common defects found after deposition of the epi layer include micro-pits, micro-cracks, hexagonal bumps, crescents, circles, showerhead droplets and localized surface roughness. Pits often appear during the MOCVD process, correlated with the temperature gradients that result as the wafer bows from center to edge. Large pits can short the p-n junction, causing device failure. Sub-micron pits are even more insidious, allowing the device to pass electrical test initially but resulting in a reliability issue after device burn-in. Reliability issues, which tend to show up in the field, are more costly than yield issues, which are typically captured during in-house testing. Micro-cracks from film stress represent another type of defect that can lead to a costly field failure.

Typically, high-end LED manufacturers inspect the substrates post-epi, taking note of any defects greater than about 0.5mm in size. A virtual die grid is superimposed onto the wafer, and any virtual die containing significant defects will be blocked out. These die are not expected to yield if they contain pits, and are at high risk for reliability issues if they contain cracks. In many cases nearly all edge die are scrapped. Especially with high-end LEDs intended for automotive or solid-state lighting applications, defects cannot be tolerated: reliability for these devices must be very high.

Not all defects found at the post-epi inspection originate in the MOCVD process, however. Sometimes the fault lies with the sapphire substrate. If an LED manufacturer wants to improve yield or reliability, it's important to know the source of the problem.

The sapphire substrate itself may contain a host of defect types, including crystalline pits that originate in the sapphire boule and are exposed during slicing and polishing; scratches created during the surface polish; residues from polishing slurries or cleaning processes; and particles, which may or may not be removable by cleaning. When these defects are present on the substrate, they may be decorated or augmented during GaN epitaxy, resulting in defects in the epi layer that ultimately affect device yield or reliability (**Fig. 1**).

Patterned Sapphire Substrates (PSS), specialized substrates designed to increase light extraction and efficiency in high-brightness LED devices, feature a periodic array of bumps, patterned before epi using standard lithography and etch processes. While the PSS approach may reduce dislocation defects, missing bumps or bridges between bumps can translate into hexes and crescent defects after the GaN layer is deposited. These defects generally are yield-killers.

In order to increase yield and reliability, LED manufacturers need to carefully specify the maximum defectivity of the substrate by type and size—assuming the substrates can be manufactured to those specifications without making their selling price so high that it negates the benefit of increased yield. LED manufacturers may also benefit from routine incoming quality control (IQC) defect measurements to ensure substrates meet the specifications—by defect type and size.

Substrate defectivity should be particularly thoroughly scrutinized during substrate size transitions, such as the current transition from four-inch to six-inch LED substrates. Historically, even in the silicon world, larger substrates are plagued initially by increased crystalline defects, as substrate manufacturers work out the mechanical, thermal and other process challenges associated with the larger, heavier boule.

A further consideration for effective defect control during LED substrate and epi-layer manufacturing is defect classification. Merely knowing the number of defects is not as helpful for fixing the issue as knowing whether the defect is a pit or particle (scratches, cracks and residues are more easily identified by their spatial signature on the substrate). Leading-edge defect inspection systems such as KLA-Tencor's Candela products are designed to include multiple angles of incidence (normal, oblique) and multiple detection channels (specular, "topography," phase) to help automatically bin the defects into types.

ECONOMIC OUTLOOK

The Forecast for 2013: Back to business

2012 was a challenging year for a long list of reasons: weakness in PC demand, DRAM and overall memory price deterioration, semiconductor inventory rationalization, continued global macroeconomic uncertainty from lower global GDP growth, a slowdown in China, the Eurozone debt crisis and recession, Japan's recession, and the impact of the "fiscal cliff." In 2013, analysts see renewed vigor for chip sales.

Fab equipment spending shrinks back to flat

CHRISTIAN GREGOR DIESELDORFF, *director, SEMI Industry Research & Statistics, San Jose, CA USA*

Despite difficult times, growing demand for mobile devices (such as tablets and phones) inspires an improved outlook for chip sales in 2013. Various forecasts range from 4% to 16% revenue growth for 2013 (average of forecasts 7%). As observed in the past, chip sales and capex typically ride the same roller coaster; however, 2013 appears to be another year of uncertainty. While chip sales may rise in 2013, expectations for equipment range from timid 5% growth down to double-digit decreases — definitely not the same roller coaster.

The largest spenders on fab equipment are Samsung, TSMC and Intel. As of mid-December 2012, some of these companies still have not made any official announcement about 2013 capex plans.

The SEMI Consensus Forecast and the SEMI World Fab Forecast, with data collected from two different methodologies, point to the same conclusion. The year-end Consensus Forecast for wafer processing predicts 0% growth (flat) for 2013. Meanwhile, the World Fab Forecast report for Front End Fabs (published November 2012) also shows 0% growth (flat) for 2013 and total fab equipment spending hovering at US$ 32.4 billion (including Discretes and LEDs, used equipment and in-house equipment). The projected number of facilities equipping will drop, from 212 in 2012 to 182 in 2013. Fab equipment spending saw a drastic dip in 2H12 and, accounting for seasonal weakness and near-term uncertainty, will be even lower in 1Q13. Examining equipment spending by product type, System LSI is expected to lag in 2013. Spending for Flash declined rapidly in 2H12 (by over 40%) but is expected to pick up by 2H13. The foundry sector is also expected to increase in 2013, led by major player TSMC, as well as Samsung, Globalfoundries and UMC.

While fab construction spending slowed in 2012, at -15%, SEMI data projects an increase of 3.7% in 2013 (from $5.6 billion in 2012 to $5.8 billion in 2013). The World Fab Forecast tracks 34 fab construction projects for 2013 (down from 51 in 2012). An additional 10 new construction projects (with various probabilities) may start in 2013. The largest increase for construction spending in 2013 is expected to be for dedicated foundries and Flash-related facilities.

In 2012, many device manufacturers stopped adding new capacity due to declining average selling prices and high inventories. This is most pronounced in the Flash sector, as seen with Sandisk since the beginning of 2012, and both Samsung and Toshiba starting 3Q12.

Breaking down the industry by product type, capacity growth for System LSI is expected to decrease in 2013. Flash capacity additions dragged in 2H12. But more activity is expected for Flash by mid-2013, with nearly 6% growth. The data also point to a rapid increase of installed capacity for new technology nodes, not only for 28nm but also from 24nm to 18nm and first ramps for 17nm to 13nm in 2013.

If the global economy and GDP begin to improve, and chip sales actually do increase in the higher single-digit range, equipment spending is expected to ride the same roller coaster, going even higher for 2013.

The beginning of the next ic industry upturn

BILL MCCLEAN, *President, IC Insights*

The expectations for global economic growth consistently deteriorated throughout 2012, with worldwide GDP eventually growing by only 2.6% last year. It should be noted that 2.5% or less worldwide GDP growth is typically considered a global recession. IC Insights' forecast for 2013 worldwide GDP growth is 3.2%. Although this figure is higher than the 2.6% increase logged in 2012, it would still be 0.3 points below the 3.5% long-term average annual global GDP growth rate.

One of the primary reasons for weak 2012 worldwide GDP growth was the negative growth registered by the Eurozone and U.K. economies. Unfortunately, the Eurozone is not expected to display a strong rebound in 2013, with 0.0% growth forecast for the Eurozone economy this year.

China's GDP growth rate dropped to only 7.7% in 2012 with a modest rebound to 8.1% growth forecast for 2013. While many developed countries would welcome 7% or higher GDP growth rates, for China, this figure is significantly below the 10% and greater annual GDP increases logged from 2002-2009. In an attempt to address its economic "slowdown," the Chinese government was quick to inject stimulus into its economy starting in the second half of 2012 by aggressively lowering interest rates as well as enacting $156 billion in construction project programs. While this stimulus was too late to have a significant positive effect on its 2012 GDP growth, China's GDP is likely to get at least a modest boost from this activity in 2013.

While the correlation between worldwide GDP growth and IC industry growth has historically been good, IC Insights believes that the correlation in 2013 will be very good, as it was in 2012. Using a worldwide GDP forecast of 3.2%, the most likely range for worldwide IC market growth in 2013 is 3-7%.

The election-year cycle is one reason why IC Insights has identified 2013 as a possible slow growth year in the worldwide economy and IC industry. Over the past 10 post-U.S.-election years, worldwide GDP growth averaged 3.1% with worldwide IC industry growth averaging only 4%. Moreover, worldwide IC industry growth exceeded 8% in only three of these 10 post-U.S.-election years (1973, 1977, and 1993), and only once since the late 1970s.

IC Insights believes that the IC industry cycles are becoming increasingly tied to the health of the worldwide economy. While poor IC market growth has occurred during periods of strong worldwide economic growth, primarily due to IC industry overcapacity and the resulting IC price declines, it is rare to have strong IC market growth without at least a "good" worldwide economy to support it. Thus, over the next five years, annual global IC market growth rates are expected to closely mirror the performance of worldwide GDP growth.

Overall, the IC industry is set to emerge from a difficult 5-year period of minimal growth. From 2007-2012, the IC market grew at an average annual rate of 2.1%. In IC Insights' opinion, the "bottom" of the current cycle in the worldwide economy and IC industry was reached in 2012 and 2013 will mark the beginning of the next cyclical upturn—one in which the IC market CAGR will more than triple to 7.4% in the 2012-2017 time period.

Healthy revenue growth in 103, but capex outlook cloudy

ADRIENNE DOWNEY, *Director of Technology Research, Semico Research*

In February 2012, Semico forecast 2012 semiconductor capex to reach $59.8 billion. In December 2012, that forecast was virtually unchanged at $59.9 billion, down 5.6% from 2011. After two years of double-digit growth (98% in 2010 and 26.2% in 2011), the semiconductor industry

needed to back off and regroup. Most concerning is that the gap between the big spenders and the small has expanded. The top ten spenders for 2012 made up 81% of the total; this figure is up from the 76% of the total in 2011. Overall, the top ten combined spent $48.2 billion, which is only 0.3% up from 2011. Meanwhile, the rest of the companies went from spending $15.3 billion in 2011 to $11.7 billion in 2012, a decline of 24%. Some of the decline can be attributed to companies like SanDisk, which, along with its partner Toshiba, delayed fab expansion projects until 2013. Other companies like ST and TI made capacity improvements over the past few years, so spending in 2012 was mainly for maintenance.

In December 2012, most companies have still not announced capex plans for the following year. This year is no different. However, a handful of companies have given some indication of what they might spend next year. For example, TSMC is forecasting 2013 capex to be slightly up compared to 2012. Most of the other companies that have given a hint of 2013's capex have indicated flat to down spending compared to 2012. These companies include GLOBALFOUNDRIES, Avago, Fairchild, Micron, ON Semiconductor, SMIC, Spansion, and STMicroelectronics. GLOBALFOUNDRIES announced its "Vision 2015" initiative to expand 300mm capacity in Singapore, but no budget was announced for the project.

That being said, there are several construction projects that may give some indication of spending in 2013. Samsung is retrofitting its Austin fab to switch from NAND to logic production, with mass production beginning in the second half of next year. This is a $4 billion project spread out over 2012-2013. Intel's D1X and Fab 42 construction will wrap up in 2013; the company will also begin production at 14nm by the end of this year. Samsung, TSMC, and GLOBALFOUNDRIES are also working on the 14nm and 20/22nm nodes. UMC has Fab 12A Phases 5 and 6 under construction, with production schedule to begin in 2014. SanDisk and Toshiba will probably increase their spending to complete the ramp of Fab 5, which they said would be complete by the end of 2013.

Based on current indications, capital spending would seem to be flat in 2013. However, Semico predicts healthy revenue growth this year, which may encourage more spending, particularly in the second half of the year. This may bring total capex for 2013 into the positive range.

An economic outlook for the global IC market

MARK THIRSK, *Managing Partner, Linx Consulting LLC.*

Past contributors to this feature have often noted a correlation between the semiconductor market growth and global GDP. With careful correction this correlation can be used to forecast future IC market trends, although the process is not straightforward.

The consensus forecast for global GDP 2013 is now below trend at 2.6%, only a slight improvement over 2012, and less than the 3.2% seen in 2011. The US approach to solving fiscal Cliff is an excellent example of the difficulty governments are having in developing strategies to address unprecedented economic problems, although political solutions, however imperfect, helps to stabilize expectations, and solidify financial markets. In Europe, mild recession will continue through most of 2013, and Asia (excepting Japan) will likely show the best overall growth rates in the coming 12 months as measures to cool the Chinese economy are relaxed.

These extraordinary conditions in the global economy lead to wide variations in economic forecasts with an upside as high as 3.5% growth, and a pessimistic case as low as 1%. Against this backdrop, meaningful macroeconomic demand-side forecasts are difficult to develop.

Linx has worked with Hilltop Consulting to implement a proven macroeconomic forecasting tool that takes into account the global economic shocks and volatility to develop an Silicon area forecast for the global semiconductor industry. Predictions for 2013 show several notable trends:

1. Overall silicon area growth for 2013 should average approximately 6%.
2. The first quarter and the second half are likely to show slower growth than the second quarter. This trend is part of a seasonality which has been swamped by economic volatility over the last 3 to 4 years.
3. The modest growth forecast for 2013 is predominantly demand driven since inventory levels have not shown a significant spike in 2012.

The overall picture of Si area growth breaks down into the expected performance of device segments and technology nodes. Despite the shift to consumer electronics and mobile platforms we expect growth to be concentrated in CMOS products at ≤ 65nm with a continuing slowing of unit growth and analog and discrete devices. Strongest growth will remain with flash memories, and advanced foundry logic devices targeted at tablets and phones.

In contrast to advanced memory and logic processing, approximately 56% of the Si production continues at design dimensions in excess of 90 nm on wafer sizes of 200 mm or smaller. This market segment is extremely sensitive to economic volatility and has declined somewhat in the last four years. Manufacturers of these devices are often capital constrained and extremely cost sensitive, leading to little process innovation and limited capacity expansion.

On a technology basis, despite tight capital budgets, the introduction of devices at 28 and 22 nm half pitches continues apace, and significant process challenges are driving increased complexity and resultant challenges in patterning, cleaning, and deposition throughout the device manufacturing process. 2012 is forecast to have produced more silicon area at 32 nm than any other node, and the introduction of low 20 nm half pitches and flash has continued to grow startling rates. Significant challenges also exist in the in the advanced device markets due to geometric constraints and physical limits in scaling planar devices. At a time when lithography is unable to scale continuing device shrinks results in added complexity in critical patterning steps and demands the addition of multiple lithography steps to achieve a single pattern level.

Manufacturers of logic and memory alike are working to develop substitute technologies for planar transistors, MIM capacitors and floating gate structures. The broad introduction of metal gate finFETs, new types of storage cells, and three-dimensional memory stacks is still several years away, and this is driving interest in the adoption of three-dimensional packaging technologies such as through silicon vias to continue delivering increasing functionality in a package.

Despite the headwinds of increasing layer counts to compensate for the lack of high resolution lithography, and the need for new deposition technologies needed for novel processes and device architectures, we expect a small group of wafer makers to continue to chase these advanced technologies, while also pushing to implement 450 mm wafers. Few of these technologies will see implementation in 2013, but they will be the focus of headlines as new breakthroughs are made, while the semiconductor industry continues its trend of remarkable success.

Beyond CMOS, steady growth and accelerating change across non-mainstream chip markets

JEAN-CHRISTOPHE ELOY, *President & CEO, Yole Développement*

Sensors and optoelectronics will continue to grow faster than the mainstream semiconductor market. We currently expect 9%-13% growth in these sectors in 2013, accompanied by rapid changes in technology and market structures as well, as the specialty markets become increasingly mature.

MEMS and image sensors will continue to ride the smart phone and tablet wave, while declining LED bulb prices will start to push the technology towards wider adoption. Demand for power electronics will pick up after its 2012 plunge.

We expect the MEMS market to continue its steady double digit growth with an ~9-11% increase to around $12 billion in 2013, driven of course by increasing adoption of the sensors in the expanding smart phone and tablet business. We expect the penetration of accelerometers into mobile phones and tablets will approach 65% by the end of 2013, with magnetometers nearing 54% and gyroscopes flirting with 34%. Growth will begin to transition from discrete sensors to combinations of two sensors in one package with a single ASIC to reduce costs, and to increasingly sophisticated software solutions that translate the sensor data into usable functions. These trends are driving changes in the competitive landscape, with a crowd of new players targeting the key 3-axis gyroscope market, others introducing other new MEMS applications for the mobile market, chipset and software suppliers taking over the sensor management tasks, and a diversification of business models as the industry evolves.

Healthy increases in the smart phone applications—and in other consumer products increasingly enabled by these low cost, easy to integrate product—will be somewhat countered by slower growth in mature TV and printer applications.

The smart phone and tablet market is also driving healthy growth in CMOS image sensors. We expect ~11-13% growth to $7.5B in 2013. Backside illumination and 3D wafer-level packaging technologies will continue to rapidly gain market share, and new stacked sensor architectures will likely follow soon. These technological changes are bringing changing business models as well, as IDMs who are not vertically integrated up through the systems level will increasingly turn to outsourcing production to foundries.

In the high brightness LED market, the TV backlighting market has slowed and the solid state lighting market has yet to really take off, but we still expect respectable ~10% growth for packaged LED devices in 2013, as rapidly improving technology, and an excess supply of devices from the backlight side, will drive down LED bulb prices to start to drive wider adoption. We expect LED penetration of the lighting market across all segments (residential, industrial, outdoor and commercial) to reach about 8% of all lamps sold in 2013, to occupy about 2% of all lamp sockets. As in most of these non CMOS chip sectors, however, demand for more die doesn't necessarily translate into demand for more manufacturing equipment. We expect sales of front end equipment in 2013 to recover about 30% from its 2012 dropoff, but not back to peak levels of the boom years. Companies will start adding capacity again in the second half of the year for the ramp up in wafer area needed for the volume lighting market. But some of that capacity will come from stronger producers acquiring struggling suppliers and their underutilized equipment.

We expect recovering demand for discrete power devices to drive ~10% growth in power electronics to some $20 billion in 2013, after what we estimate was a ~20% drop in 2012 as China cut back on its big investments in railroad, solar power and wind power systems. Going forward, green tech demand from hybrid/electric vehicles, wind and PV systems should again help spur sales in 2014-2015, and then support stable 6%-7% long term growth after 2016.

Look for continued consolidation in 2013

RON LECKIE, *President, Infrastructure Advisors*

2012 brought a slowdown in consumer spending which has negatively impacted chip unit demand. In fact, chip units have been essentially flat for much of the last two years. However, the good news is that unlike in prior slow periods, average selling prices have maintained a steady level. As a result, the industry sits today with slightly elevated inventories and also with factory utilization levels that are generally about 15 percentage points below normal healthy levels. I look to enter 2013 with continued seasonal slowness, but anticipate that unit volumes and utilization levels will start picking up by the second quarter and throughout the year.

As a result, with utilization rates at the low end of the range, we will not be seeing any significant capacity additions until later in the year. Capital purchases will be primarily for new technology capabilities until unit volumes pick up and in turn drive capacity needs. The Test and Assembly equipment sectors should feel a recovery slightly ahead of their Wafer Fab counterparts since they tend to be more units-driven.

The semiconductor industry and its entire supply chain are certainly maturing and are becoming more dependent than ever on the overall economy. Individual companies either need to have new innovative products to gain market share and drive organic growth, or they need to acquire companies that will take them into new adjacent markets.

In recent years, we have seen consolidation by some of the larger companies in the industry. However, when walking around trade shows such as Semicon West, it is evident just how many small and medium sized companies still exist. For these companies to thrive in a mature market, they need critical mass and now is the time to be looking at strategic alternatives. Such smaller companies with complementary product lines and customers should be looking for merger opportunities. The semiconductor industry is truly global and for example, there are big synergies to be found when bringing together global sales and service operations. Customers prefer working with strong suppliers who will be around to support them for years to come.

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TECHNICAL FORECAST

2013 technology forecast: Unprecedented challenges ahead

We asked leading industry experts to give us their perspectives on what we can expect in 2013. The challenges ahead include 450mm, FinFETs and 3D NAND, TSVs and 3D integration, and sensor fusion.

RANDHIR THAKUR, *Vice President and General Manager, Silicon Systems Group, Applied Materials*

Multiple inflections will figure prominently in 2013. Among these, we see the foundry transition to 20nm process technology node as a significant milestone. 20nm is all about building advanced transistors that can deliver low leakage, low power and high performance in a smaller footprint. To achieve this combination of performance and energy efficiency, chip makers must adopt high k metal gate transistors which could deliver a 20 percent savings in power consumption while offering a 15% increase in speed. Further leakage and speed performance improvements at 20nm and below will be gained from FinFET transistors. Beyond advances to the transistor, we expect major inflections in lower resistance interconnects, advanced patterning, packaging, and 3D NAND flash technology.

We've never seen in this level of change in the industry or this pace of manufacturing process development. Innovations in new semiconductor materials, manufacturing processes and other technologies will be needed to support these inflections that each pose critical challenges. Unprecedented precision engineering will be needed to manufacture chips features measured in nanometers. At these dimensions every atom counts and controlling variability is vital to meet performance and productivity targets. Also pivotal in enabling future chips will be new classes of materials with superior properties that can be used in a broad range of process applications.

With demand for new forms of consumer electronics and new methods of computing driving the pace of innovations, we're going to see more changes in the next five years than we've seen in last 15. These innovations will require major research and development efforts and very early and close collaboration across the industry.

ARTHUR W. ZAFIROPOULO, *Chairman and CEO, Ultratech, Inc.*

After all the speculation, discussions and debates, the transition to 450mm wafers will happen. As an equipment manufacturer, it is not enough to simply survive, but it is imperative to thrive in the transition to 450mm. While driven by all the major semiconductor companies, the transition to 450-mm wafers will have a compounding effect on equipment manufacturers' R&D investments. By combining the technology challenges and the wafer diameter change, companies in the equipment industry will require a strong balance sheet to be successful.

Smart companies know that success lies in the ability to be bold and aggressive in R&D and remain

conservative on the balance sheet. Success is also determined by a company's efforts to prepare for the future by investing and developing the right technologies and supporting capabilities. By developing innovative technologies that address the critical issues around the transition and adoption, companies can play an enabling role for 450mm.

RICHARD GOTTSCHO, Ph.D., *EVP - Global Products, Lam Research Corporation*

The semiconductor industry is evolving and facing unprecedented technology and economic hurdles. Limits imposed by planar technology and a stalled lithography roadmap threaten to slow down the rate at which density, cost, and speed improvements can be made. As this industry has shown before, however, there is more than one way to skin a cat. FinFET devices offer superior speed at lower power consumption. 3D NAND enables bit scaling of flash memory without the need of lithography roadmap extension. Multiple patterning extends the lithography roadmap. Through-silicon via (TSV) technology brings increased density, lower power consumption, and faster computing to mobile applications. But, these inflection technologies have their own set of challenges.

FinFETs are challenging to etch because the 3D topography requires long over-etching to clear corners; etching selectivity becomes of paramount importance. Atomic-scale precision is required across not only the wafer, but also from wafer-to-wafer and from fab-to-fab. Etch costs increase for all these reasons. FinFET metal gates have high-aspect-ratio features that must be filled without voids with thin, conformal, low-resistivity diffusion barriers using atomic-layer deposition.

PAUL LINDNER, *Executive Technology Director, EV Group*

The Internet of Things is about more than just gathering information through ubiquitous sensors. Huge amounts of data need to be affordably stored and analyzed, in order to be useful, which requires keeping Moore's Law alive. Fortunately, new semiconductor 3D manufacturing technologies are poised to play a critical role in further commoditizing memory and processing power. In 2013 high volume production of true 3D technology will commence. The industry will also see intensified wafer level developments particularly around image sensors and memory, as new DRAM designs allow for monolithic integration at the wafer level. Wafer-to-wafer bonding processes, combined with built in self-test, error detection and correction are poised to overcome one of the few remaining hurdles to high-volume, low-cost 3D manufacturing.

RUDY KELLNER, VP & GM, Electronics Business Unit, FEI

Consumer demand for more power, speed and functionality in less space seems to be insatiable. Yet semiconductor manufacturers have reached the end of the era when this demand could be satisfied by simply shrinking the dimensions of fundamental planar device technologies. Now they must accommodate complex, three-dimensional (3D) device architectures and a plethora of new materials. At the package level they must develop and produce 3D designs that stack and interconnect multiple die without sacrificing yield or performance. The net result of all this innovation is a sharp increase in R&D capital intensity. In order to maintain profitability manufacturers must increase the productivity and return from their R&D investments. Moreover, time-to-market has become the new battle ground where the first to market enjoy a brief period of premium pricing and higher margins, before the battle begins again.

TONY MCKIE, *general manager,memsstar,Ltd.*

At the moment, the MEMS industry is experiencing tremendous growth, driven largely by numerous consumer electronics products whose MEMS components, both multiple and varied, are finding their way into people's everyday life. Whereas before a phone had a single microphone, today's high-end smart phones may have as many as three microphones for noise suppression using advanced beam forming audio techniques. This and other high-end consumer applications for devices such as accelerometers, gyroscopes, and MEMS oscillators are

the likely drivers in analysts' predictions for a 15 percent compound annual growth rate (CAGR) over the next five years.

HOWARD KO, *Senior Vice President and General Manager, Silicon Engineering Group, Synopsys, Inc.*

Whenever we communicate with our mobile phones, catch up on the latest news in our tablet computers, or snap those memorable holiday family photos with our digital cameras, we are relying on an indispensable semiconductor technology: the NAND flash memory. Over the past two decades, NAND flash memory has become one of the linchpins of the semiconductor market with revenues of approximately $21B in 2012 according to iSuppli. As in other semiconductor technologies, NAND flash evolution has been driven by density, performance and cost improvements. And as in planar CMOS logic, NAND flash technology has been progressively scaled to smaller feature sizes, becoming the process leader in driving the smallest line-widths in manufacturing as evidenced by the current 1x-nm (~19-nm) process node. Yet, despite plans to scale down to the 1y-nm (~15-nm) and possibly 1z-nm (~13-nm) nodes, the traditional planar floating gate NAND flash architecture is approaching the scaling limit, prompting the search for new device architectures. Not to be upstaged by the planar to 3-D (FinFET) transition in logic devices, NAND flash has embarked on its own 3-D scaling program, whereby the stacking of bit cells allows continuous cost-per-bit scaling while relaxing the lateral feature size scaling.

RAVI KANJOLIA, *Chief Technology Officer, SAFC Hitech*

We are in an age where chemistry is center stage in the race to advance Moore's Law and More Than Moore. The continued drive towards smaller feature sizes, increased performance, and lower power consumption requires highly complex architectures using new materials and advanced process technologies. This is primarily true for processes in which physical vapor deposition (PVD) is being displaced by atomic layer deposition (ALD) and chemical vapor deposition (CVD). For example, materials are being

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New Products

Back-end lithography system

The JetStep is a new 2X reduction stepper that has several advantages over the 1X approach, according to Rudolph, which acquired Azores last year. System advantages include the largest printable field-of-view, programmable aperture blades and large on-tool reticle library, large depth-of-focus along with autofocus to accommodate 3D structures in advanced packaging, very large working distance, and warped wafer handling (+/- 6mm). The system also feature programmable wafer edge protection, enabling a variable edge exclusion zone of 0.5-5 mm. The system also features a large (17mm) working distance between the lens and wafer, which helps avoid a common maintenance issue on 1X systems. In addition, with its flat panel lithography heritage, the JetStep System incorporates Azores' high precision grid motor stage. This provides a flexible platform that can be readily scaled to changing substrate sizes and types in the advanced packaging market. It can handle both standard and reconstituted 300mm and 330mm wafers, all panel sizes and is 450mm capable. **Rudolph Technologies**, Flanders, NJ. www.rudolphtech.com.

Stepper for LEDs, MEMS, power devices

Canon USA, Inc. recently launched the FPA-3030i5+ i-line stepper, designed for the manufacturing of LEDs, MEMS and power semiconductors. The FPA-3030 platform is an upgrade to earlier Canon "FPA-3000 platform" steppers. The FPA-3030i5+ features an overhauled software structure and electrical control system that allow application of optional advanced hardware (e.g., projection lens, wafer stage, and alignment system) that is not compatible with traditional FPA-3000 platform steppers. The FPA-3030i5+ is capable of providing imaging resolution below 0.35mm, while maintaining overlay accuracy of less than or equal to 40nm and throughput equal to or in excess of 104 wafers per hour. **Canon USA**, Lake Success, NY, www.usa.canon.com.

Updated LED wafer inspection tool

KLA-Tencor says its new fourth-generation LED wafer inspection system achieves greater flexibility, increased throughput, and improved efficiency for inspecting defects and performing 2D metrology in LED applications, as well as MEMS and semiconductor wafers (up to 200mm). The ICOS WI-2280, built on the company's WI-22xx platform, supports handling of whole wafers in carriers and diced wafers in hoop ring or film frame carriers, to accommodate multiple media with minimal equipment changeover. An enhanced rule-based binning defect classification and recipe qualification engine enable faster yield learning during production ramps, and improved process control and process tool monitoring strategies. Highly flexible advanced optical modules with dedicated image processing enable high defect capture rate and recipe robustness against varying process background. A frontend-to-backend-of-line connectivity analysis capability -- working in conjunction with the company's Candela LED unpatterned wafer inspection system and Klarity LED automated analysis and defect data management system -- delivers a single platform for defect source analysis. **KLA-Tencor**, Milpitas, CA, www.kla-tencor.com.

developed to form high purity functional layers for applications in logic, memory, and interconnect areas, all within given thermal budgets

JIM MELLO, *Vice President, Sales and Marketing , Entrepix, Inc.*

One of the biggest challenges for the industry is that 80 percent of the devices used for portable and mobile applications are currently manufactured on 200mm or smaller wafers. How this plays out going forward could change who the dominant players will be and therefore could drive consolidation. As the communications market advances, design wins play a large role in the uncertainty. The secondary equipment market provides ongoing opportunities throughout the entire market, especially during periods of economic difficulty, and is extremely well positioned to capitalize on the continued strength of the 200mm market.

ARDY JOHNSON, *Vice President of Marketing and Product Management, Rudolph Technologies, Inc.*

Advanced packaging is in the early stages of a dynamic growth phase. Demand for equipment and related tools in the 3DIC and wafer-level packaging area is forecasted to grow from approximately $370 million in 2010 to over $2.5 billion by 2016. Advanced packaging requirements are driving the evolution of back end manufacturing to become more similar to the front end where the need to tie the entire process together with effective process control has long been established.

Ideally, a photolithography solution for advanced packaging begins with a reduction stepper that is uniquely capable of meeting current and future requirements of advanced packaging processes: greater depth of focus to handle the thicker resists required by exaggerated wafer topography; flexible automation and specialized handling for warped wafers, reconstituted wafers, and large panels; on-the-fly focusing at every exposure to ensure maximum image quality; and an on-board reticle library and fast-change reticle wheel for increased productivity.

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New challenges for suppliers

Over the past 24 months, construction timelines for new wafer production facilities have contracted so much that construction firms are now required to move from bid package to on-site prep in as little as three weeks.

Naturally, this change is affecting industry suppliers. Construction firms are expecting their suppliers to back them in all aspects of preparing competitive bids under compressed timetables. And, further, they are expecting their suppliers to deliver on a promise for expedited product fulfillment, testing, training, documentation, and/or fabrication.

From the supplier's standpoint, this is the time to ask not just how do we deliver, but how can we do better? How can we leverage our strengths differently? How can we anticipate our customers' needs or help to preempt any issues that could arise, given the abbreviated timelines?

For example, a construction firm may be required to transform a mix of many subassemblies into an integrated system. In turn, it may be required to connect this integrated system to other systems, which are being assembled by different construction companies. Each system – and each component – will need to precisely match specifications to ensure proper alignment and installation in the end facility.

These are occasions when a supplier's resourcefulness can make the difference. The supplier can provide product information relating to compatibility issues and dimensions, as well as three-dimensional computer-aided design (CAD) drawings that can be plugged into standard design programs. It can also provide test reports and performance data. Throughout the construction cycle, the supplier's role and responsibility is to provide swift access to reliable information.

Further, how can the supplier extend this resourcefulness into the construction and execution phase? Can a knowledgeable expert be nearby and available if any further training is required or installation issues arise?

The relationship between supplier and construction firm is based first and foremost on the quality and reliability of the product. This baseline requirement ensures dimensional accuracy and consistency, with adherence to Copy Exact Change Control (CECC) guidelines.

> Any miscalculation in the design or bid can result in costly rework that jeopardizes the project.

But in this era of rapid mobilization, the relationship is also based on the rapid exchange of reliable information. And the stakes are high. Any miscalculation in the design or bid can result in costly rework that jeopardizes the project.

Here are four additional supplier benefits that have proven especially important to construction firms in the current environment:

A global supply chain. With tool fabrication and line production taking place around the world, a supplier should be able to provide products and support whenever and wherever they're needed.

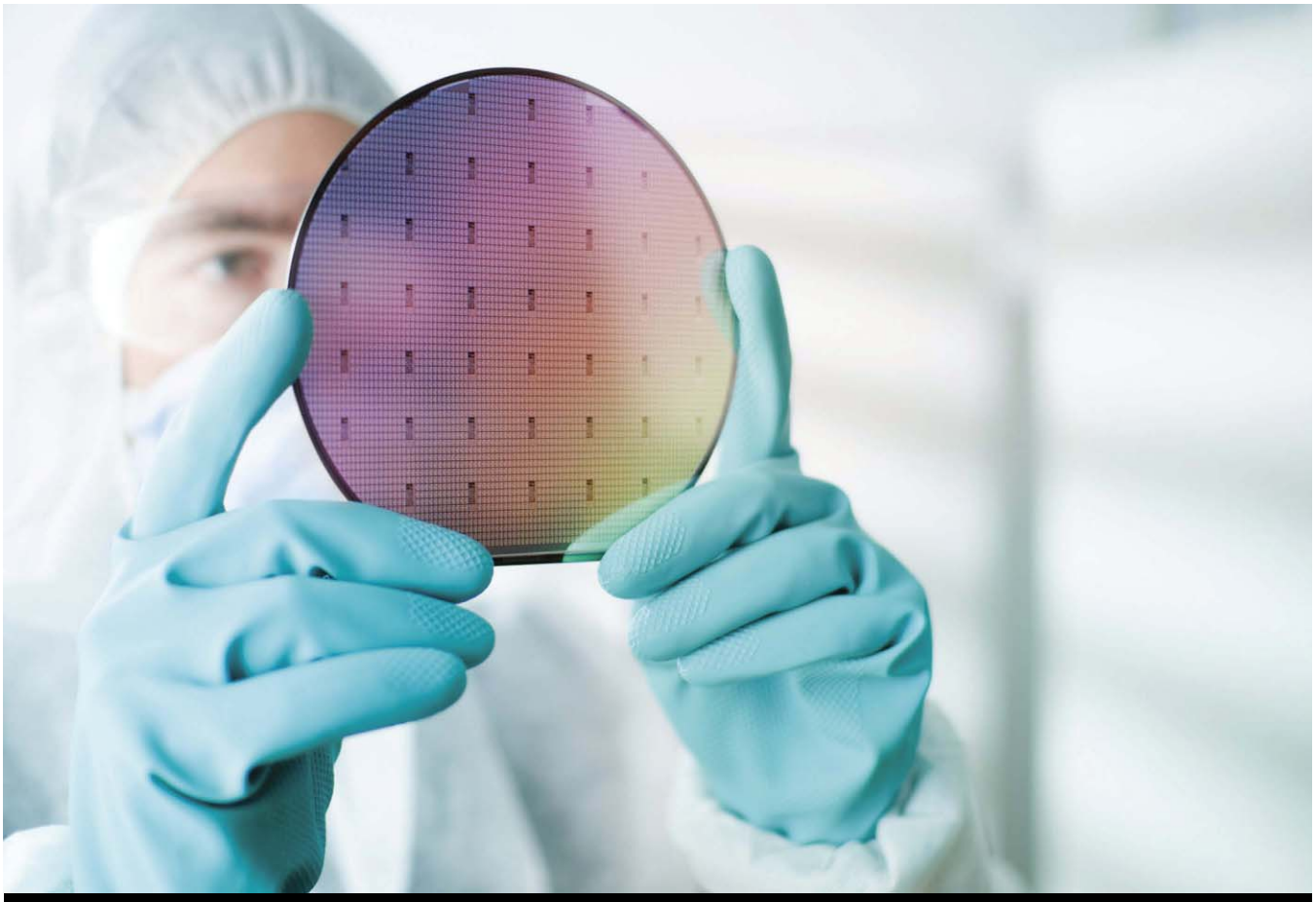
Training and safety. A comprehensive training program covers product selection, installation, proper equipment use, maintenance, and certification protocols with on-site quality assurance companies. Such a program ensures quality standards and contributes to a company's efforts to reduce recordable injuries and hold down its Experience Modification Rating (EMR).

Tight, consistent control. To facilitate easy set-up, installation, and welding, construction firms rely on suppliers who deliver products with tight, consistent dimensional and materials control.

Flexible product configurations. Construction firms may require discrete components or kits. Or, they may require engineered-to-order products, inventory management, or subassemblies, such as weldments or purge sticks, as well as plug-and-play component data for Turn Over Packages (TOPs).

These are all potential cost-saving options for the construction firm.

SEAN MARRIE *is commercial manager at Swagelok Company, Solon, Ohio USA*



Reduce chemical usage and minimize excursion events. Measurement made easy.

The new TALYS ASP310 analyzer fulfills the needs of equipment suppliers to semiconductor, solar and LED Fabs. This low cost, high performance wet bath monitor allows real-time end-of-bath alerts and enables effective bath dosing. The TALYS can quickly measure multiple chemistries at the same sample point. The performance of this analyzer permits equipment operators and engineers to reduce chemical usage and minimize excursion events with real time bath component predictions. Learn more at www.abb.com/analytical

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