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Insights for Electronics Manufacturing

2014 Outlook

P. 11

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17 industry visionaries provide the outlook for 2014 in this issue. Additional photos courtesy of imec and Intel.

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Slideshow: CES 2014 Highlights

This month in Las Vegas, the 2014 International Consumer Electronics Show focused on the Internet of Things, displaying many connected gadgets and services. This year's show featured more than 3,200 exhibitors, many of which were excited to show off new Internet-enable devices. Click through our slideshow of highlights for an overview of the show.

http://bit.ly/1d8j8D4

Intel vs. TSMC: An update

On January 14, 2014 we read on the Investors.com headlines page – Intel Seen Gaining Huge Pricing Advantage Over TSMC. Just three days later comes the responding headline: TSMC: We're "Far Superior" to Intel and Samsung as a Partner Fab. These kinds of headlines are not seen too often in the semiconductor business domain and it is not clear what the objectives are for such.

http://bit.ly/1ijUQd6

Insights from the Leading Edge

The 2013 IEEE IEDM was held in WDC the 2nd week of Dec. Contributing Editor Phil Garrou take a look at some of the key 3DIC presentations there.

http://bit.ly/1gMi4om

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MEMS: An enabler of the next internet revolution

The next internet revolution is shaping up and MEMS is poised to play an important role. Commonly referred to as the Internet of Things (IoT) or Machine to Machine (M2M) communications, this revolution consists primarily of machines talking to one another, with computer-connected humans observing, analyzing and acting upon the resulting 'big data' explosion it produces. While the first internet/web revolution changed the world profoundly, the disruptive nature of MEMS, M2M and the Internet of Things has the potential to change it even more as the big data machine will no longer be dependent on human data entry. The internet traffic will be automatically generated by millions of 'things' from which we can retool large parts of the world for better efficiency, security and environmental responsibility.

http://bit.ly/LjNYP1

Safety critical devices drive fast adoption of advanced DFT

Devices used in safety critical applications need be known to work and have the ability to be regularly verified. Therefore, a very high-quality test is important as well as method to perform a built-in self-test. Recently, there has been a strong growth in the automotive market and the number of processors within each car is steadily increasing. These devices are used for more and more functions such as breaking systems, engine control, heads-up display, navigation systems, image sensors, and more. As a result, we see many companies designing devices for the automotive market or trying to enter the automotive market.

http://bit.ly/1bOmtma

editorial

Is a "concorde moment" approaching?

Rick Wallace, president and CEO of KLA-Tencor, provided the keynote talk at the SEMI Industry Strategy Symposium (ISS) this year, held Jan 12-15 in Half Moon Bay, CA. He said he believes the semiconductor industry might be facing a "Concorde" moment, referring to the demise of supersonic passenger transport, the last flight of which was on 24 October 2003. "That failed not because of technology but because of economics," Wallace said. He sees a similar challenge coming down the road for continued scaling. "Moore's Law is much more likely to die in the boardroom than the laboratory," said.

> Supersonic passenger transport failed not because of technology but because of economics

Wallace also spoke about "The Road Less Traveled," indicating that the more traveled one is that of consolidation, which Wallace said leads to "losses in agility, flexibility and innovation." He said larger firms are not effective at driving innovation although they are effective at driving continuous improvement. "It's tough to see how a large scale merger makes a company better," he said. "Some firms will be too big to fail but my fear is that they will become too big to innovate."

The solution he said is young people. "We need to attract the young talent if we want real innovation. The longer you're around the more you see what can't be done," he said.

Wallace told a story about explaining to his 10 year old daughter what his company by using the iPad as an example. His daughter thought about it and said she understood: it was the "magic behind the gadget."

Part of attracting young people to the semiconductor industry is through education. After Rick's presentation, Denny McGuirk, president of SEMI, presented an award to Rick and to L.T. Guttadauro, president of the Fab Owners Association, in recognition of their work on SEMI's High Tech University (HTU). HTU is a career exploration program that encourages student interest in science, technology, engineering and match. Since 2001, the SEMI Foundation has delivered 143 programs to 4800 students and teachers worldwide.

Although some view the semiconductors as a commodity, hopefully efforts such as that of the HTU will explain the magic behind the gadget. "Who doesn't want to work on magic?" Wallace asked.

—Pete Singer, Editor-in-Chief

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EUROPE | **Merck** agreed to buy **AZ Electronic Materials SA** (AZEM) for $2.6B, making Merck one of the largest photoresist suppliers.

USA | **SEMI** honored teams from **Xilinx** and the **University of Florida** with the 2013 SEMI Award for North America at the 2014 SEMI Industry Strategy Symposium.

EUROPE | **ARM** and **UMC** announced an agreement to offer the ARM Artisan physical IP platform along with POP IP for UMC's 28nm high-performance low-power (HLP) process technology.

ASIA | **Samsung Electronics** announced that it has developed the industry's first eight gigabit (Gb), low power double data rate 4 (LPDDR4), mobile DRAM.

USA | The discovery of what is essentially a 3D version of graphene promises exciting new things to come, including much faster transistors and far more compact hard drives. A collaboration of researchers at the Lawrence Berkeley National Laboratory has discovered that sodium bismuthide can exist as a form of quantum matter called a three-dimensional topological Dirac semi-metal (3DTDS).

ASIA/EUROPE | The **TOWA Corporation** of Japan announced plans to expand their activities in Europe with an Innovation Center for Packaging Development and announced the launch of TOWA Europe B.V.

ASIA | **SAMCO** released its newest deep silicon etching system for MEMS and TSV production processing.

Micron revenue surges after Elpida deal officially closes

Micron Technology surged 130 percent in revenue during the third quarter as it finally closed its acquisition of bankrupt Elpida Memory of Japan, a vigorous ascent that also propelled the total market for dynamic random access memory (DRAM) to its best performance yet in 11 quarters, according to a new DRAM Dynamics brief from IHS Inc.

Micron ended the third quarter with sales of $2.63 billion, up a sizzling 131.3 percent from $1.14 billion in the earlier quarter, to give the Idaho-based maker 27.4 percent market share. Micron remains at No. 3 overall behind top-ranked Samsung, but Micron is now within striking distance of second-ranked SK Hynix.

Samsung still has a commanding lead with 36.8 percent market share of DRAM, but SK Hynix, with 27.8 percent share, is now just four-tenths of a percentage point ahead of Micron.

Micron's market share had been hovering in the 10 to 15 percent range for the last several years, but the addition of Elpida's revenue to its column has made a significant difference. The closing of the Elpida acquisition, more than a year in the making and a formidable rival of Micron in the past, will now more than double Micron's DRAM manufacturing capability. This means Micron will now claim 25 to 30 percent market share from this point forward.

Micron's market share in the third quarter received an additional bump because of the company's high exposure to the PC DRAM space, which has seen prices appreciate considerably since November 2012. Nearly 35 percent of Micron's revenue came from sales of PC DRAM, IHS estimates.

Overall the global DRAM market continued its blistering pace of expansion in the third quarter, with revenue up 10 percent sequentially to reach $9.59 billion. Not since the third quarter of 2010 has industry revenue climbed so high when the market's takings then hit $10.68 billion. Industry revenues had hovered at the $6 billion to $7 billion range for seven quarters beginning in the third quarter of 2010 and then breached the $8 billion mark in the second quarter, before making another substantial push this time to end up in rarefied territory.

Growth for the latest period was driven by an increase in shipments and average selling prices (ASP). Shipments are up 5 percent, while ASPs have jumped nearly 7 percent to reach $1.00 per gigabyte.

The DRAM industry is currently on a tear, helped by industry consolidation—including the Micron acquisition of Elpida—that has now left just three major producers, resulting in greater stability and higher prices because of controlled production, benefiting the remaining players.

Samsung expands shipments after SK Hynix suffers a fire

SK Hynix suffered a setback after a fire broke out at its Wuxi, China, plant, notably impacting the company's DRAM shipments in the third quarter. After growing nearly 40 percent in the second quarter, SK Hynix saw only a 4 percent uptick in revenue in the most recent period because of the fire. The impact of the disaster will be felt through the end of 2013, IHS predicts, but the company should be back to near normal by the end of the year.

Meanwhile, Samsung—already the undisputed leader of DRAM—took advantage of the SK Hynix calamity to grow its own shipments by nearly 15 percent on the quarter, along with a 7 percent hike in ASP. Such results could put Samsung on track to reap record earnings in the fourth quarter—Samsung's peak quarterly revenue was $4.35 billion in the third quarter of 2010.

For the fourth quarter, total DRAM shipments and prices are forecast to keep climbing. While signs suggest that prices have now reached their current peak with the spot market starting to soften, long-term prospects continue to look positive. And companies that outgrow the market average, such as Micron and Samsung, could well see revenues continue to go up.

TSMC, Samsung and Micron top list of IC industry capacity leaders

As of December 2013, Samsung had the most installed wafer capacity with nearly 1.9 million 200mm-equivalent wafers per month. That represented 12.6 percent of the world's total capacity and most of it used for the fabrication of DRAM and flash memory devices. Next in line was the largest pure-play foundry in the world TSMC with about 1.5 million wafers per month capacity, or 10.0% of total worldwide capacity.

Following TSMC were memory IC suppliers Micron, Toshiba/SanDisk, and SK Hynix.

In January 2013, Micron and Nanya amended their Inotera partnership such that Micron now takes 95 percent of Inotera's wafer output. Previously, Micron and Nanya evenly split Inotera's capacity. Then, in July 2013, Micron finally closed the deal on its acquisition of Elpida

Memory and the Rexchip business in Taiwan that Elpida operated in partnership with Powerchip. It took Micron a full year to complete the purchase after several delays with getting approvals from bondholders and governments. With the addition of the Elpida and Rexchip fabs as well as the extra Inotera capacity, Micron became the third-largest wafer capacity holder in the world in 2013 with nearly 1.4 million 200mm-equivalent wafers per month (9.3 percent of total worldwide capacity). At the end of 2012, Micron had the sixth-largest amount of wafer capacity.

The fourth-largest capacity holder at the end of 2013 was Toshiba with a little under 1.2 million in monthly wafer capacity (8.0 percent of total worldwide capacity), including a substantial amount of flash memory capacity for joint-investor/partner SanDisk. After Toshiba came another memory IC supplier SK Hynix with a little more than one million wafers/month (7.0 percent of total worldwide capacity). Rounding out the top six companies was Intel with 961K 200mm-equivalent wafers per month capacity, or 6.5 percent of total worldwide capacity. Just two years ago in 2011, Intel was the third-largest capacity leader, but in early 2012 the company reduced its ownership position in IM Flash as well as its wafer output share from its joint venture with Micron.

The three largest pure-play foundries—TSMC, GlobalFoundries, and UMC—are ranked in the top 10 listing of capacity leaders. In total, these three companies have held about 80 percent of the worldwide pure-play foundry market since 2010. Moreover, these three foundries had a combined capacity of about 2.5 million wafers per month as of December 2013, representing about 17 percent of the total fab capacity in the world.

The combined capacity of the top-5 leaders accounted for 47 percent of total worldwide capacity in Dec-2013. At the same time, just over two-thirds (67 percent) of the world's capacity was represented by the combined capacity of the top-10 leaders, while the top 15 accounted for 76 percent and the top 25, 85 percent, of worldwide installed IC capacity in Dec-2013. It should be noted that the shares of these groups have each increased significantly since 2009. The top-5 group gained 11 percentage points; the top-10 group, 13 points; the top-15 group, 12 points; and the top-25 group, seven points. Those are big gains over the course of just four years!

IC manufacturing is increasingly becoming a high stakes poker game with enormous up-front costs. Today, it costs $4.0-$5.0 billion for a high-volume state-of-the-art 300mm wafer fab and the cost to build tomorrow's 450mm wafer fab will probably be double that. Despite the cost-per-unit area advantage that larger wafers provide, there are fewer and fewer companies willing and able to continue investing that kind of money.

IC Insights believes that the capacity shares of the top 5, 10, 15, and 25 leaders will continue to increase over the next several years as the big get bigger, middle-tier manufacturers merge to consolidate resources and improve competitiveness, and a greater number of mid- to small-size companies move away from in-house IC fabrication and move toward using third-party foundries.

Rankings of IC manufacturers by installed capacity for each of the wafer sizes are shown in Figure 2. Looking at the ranking for 300mm wafer capacity, it is not surprising that the list includes only DRAM and flash memory suppliers like Samsung, Toshiba, Micron, SK Hynix, and Nanya; the industry's biggest IC manufacturer and dominant MPU supplier Intel; and the world's three largest pure-play foundries TSMC, GlobalFoundries, and UMC. These companies offer the types of ICs that benefit most from using the largest wafer size available to best amortize the manufacturing cost per die. The ranking for the smaller wafer sizes (i.e., ≤150mm) includes a more diversified group of companies.

A significant trend with regard to the industry's IC manufacturing base, and a worrisome one from the perspective of companies that supply equipment and materials to chip makers, is that as the industry moves IC fabrication onto larger wafers in bigger fabs, the group of IC manufacturers continues to shrink in number. There are just 36% the number of companies that own and operate 300mm wafer fabs than 200mm fabs and the distribution of worldwide 300mm wafer capacity among those manufacturers is very top-heavy. Essentially, there are only about 15 companies that comprise the entire future total available market (TAM) for leading-edge IC fabrication equipment and materials. When 450mm wafer fabrication technology comes into production, this manufacturer group is predicted to shrink even further to a maximum of just 10 companies. ◆

Economic recovery and pervasive computing to propel semiconductor manufacturing supply chain

Macroeconomic and microelectronic industry growth opportunities and innovation challenges underscored diverse perspectives from analysts, economists, technologists, semiconductor manufacturers and supply chain executives speaking at the SEMI Industry Strategy Symposium (ISS) that was held in January. The executive conference offers the year's first strategic outlook for the global microelectronics manufacturing industry and offered encouraging forecasts buttressed by the silicon requirements for the pervasive computing era.

Opening keynoter Rick Wallace, president and CEO of KLA-Tencor, invoked Robert Frost prose on the "The Road Not Taken" to illustrate competing industry views about growth. Wallace contrasted consolidation-driven industry mergers to what he characterized as more agile productivity-oriented innovation growth. He rejected dual-source strategies as the optimal path for the industry and its supply chain and called for industry to make a more convincing appeal to young talent. In a provocative differentiation from competitors, Wallace questioned whether "too big to fail is also too big to innovate."

Robert C. Fry, senior economist at Dupont, pointed to low but persistent global economic growth and highlighted positive data for global industrial production. He forecast global GDP growth of 3.1 percent in 2014 — up from 2.4 percent in 2013. Moreover, he commented on the increasing correlation between global GDP and semiconductor output, with high tech once

again growing faster than the economy. Fry stated that global leading indexes are trending up, but not strongly or universally. Semiconductor shipments are finally setting new highs again and semi shipments have been trending up for more than a year.

Bill McClean, president of IC Insights, also pointed to better GDP growth trends, from 2.1 percent (2008-2012) to a forecast of 3.4 percent growth for 2014. Noting the trend toward mobility, he said that 2014 will be the first year that communications IC spending surpassed computing IC spending. He forecast 7 percent semiconductor market growth in 2014 to $350.7 billion and called for capital equipment spending of $62.3 billion, 9 percent higher than 2013 ($57.2 billion).

Bob Johnson, research VP at Gartner, stated that in the short term, growth will return to equipment markets in 2014 with annual growth between 16 and 21 percent. He expects quarterly weakness in the first half of 2014 after a strong fourth quarter in 2013. Longer term, he sees foundries battling IDMs for supremacy in mobility markets, technology shifts on the horizon with the advent of 3D NAND and EUV, and 450mm implementation beginning by end of 2017. Also, Johnson said that by 2017, the dominant semiconductor revenue opportunity in the "Internet of Things" will shift from infrastructure to the "Things," and that the challenge will be in how to bring thousands of new products to market rapidly and cheaply.

Mark Thirsk, managing partner at Linx Consulting, discussed chemicals and materials needed for advanced semiconductor devices and forecast an improved outlook for 2014 with strong Q2 and Q3. A high upside potential remains in specialty materials for semiconductors, but significant R&D requirements remain a barrier. Materials demand grows faster than semiconductor unit growth due to process complexity — with Patterning, CVD and ALD, and CMP all driving materials demand growth. For the next 3-5 years, 3D packaging and TSV processing are key areas.

In the next SEMI Industry Strategy Symposium session, presenters spoke of both the challenges and opportunities inherent in Pervasive Computing. Nick Yu, senior VP at Qualcomm, discussed the unprecedented opportunity that the mobile era offers. Yu stated that what consumers want is a digital "6th sense," basically the "augmentation of human ability." The smartphone experience is also becoming the expectation in other device categories. Lama Nachman, principal engineer at Intel Labs, continued this thought with a presentation on "Context is Everything," stating that Intel wants to fundamentally transform the relationship between humans and computers with "context" — for communication, introspection, meetings, health, and more. She said that the platform implications of context include: "always-on" sensing and computing, low-power sensors and I/O, effective workload partitioning, and security and privacy.

Dale Ford, VP and chief analyst at IHS, stated that the semiconductor market growth continues its cyclicality, with September 2012 beginning a new cycle that will peak in the second half of 2014. Ford said that capital expenditures declined by 9 percent in 2012 and an additional 3.7 percent in 2013, with Intel and Samsung transitioning existing capacity for use on next-generation technology. Pablo Temprano, senior director at Samsung Semiconductor, also stressed that a transformation is in progress. Discussing memory growth and investment in the mobile era, he said that Mobile is driving the Cloud (2013 Capex at $10 billion for just top 4: Google, Microsoft, Amazon, Facebook). The total memory Capex Consensus forecast is $16 billion for 2014.

Finally, Rod Morgan, VP at Micron Technology, said that an increasingly connected lifestyle is driving memory requirements with mobile multi-functional devices, with embedded sensors and significantly greater memory consumption. Fast growing memory in a highly interconnected world demand is split across multiple sub-segments. The $16.4 billion mobile memory segment is a portion of the overall memory market (RAM $31.0 billion; Flash $26.6 billion). Citing the reliability, technology and security requirements of these embedded mobile device microelectronics, Morgan called for greater supply chain collaboration to enable the network infrastructure be successful. He said, "The pace at which we enable the infrastructure will determine the speed of innovation."

Will monolithic 3D IC technology become a real competitor to 3DIC with TSV?

Dr. Phil Garrou,
Contributing Editor

The language of 3DIC is certainly a bit confusing, especially when it comes to TSV-based 3DIC and what can be called monolithic 3DIC.

Back end (BE) 3DIC with TSV is a parallel process where each layer or stratum is fabricated with TSV separately and subsequently joined. Monolithic 3DIC is a front end (FE), sequential process where a second layer of silicon is deposited or grown onto the first finished chip and the transistor and interconnect processes are repeated.

The issue with the sequential process has always been the temperatures required to deposit or grow a second crystalline layer of silicon on top of the IC. It is difficult to overcome the 400°C process temperature limitation imposed by the use of aluminum and copper IC interconnect when creating the second layer of silicon and implanting and annealing the second layer of transistors.

For instance the early work of Akasaka-at the LSI R&D Labs of Mitsubishi Electric described the basic concept of monolithic 3DIC (Akasaka, Y., Nishimura, T., Concept and Basic Technologies for 3DIC", IEEE Proceed., IEDM, vol. 32, 1986, p. 488).

It was clear nearly 30 years ago that "to fabricate 3-D IC successfully, a wafer temperature during the crystallization should be kept low enough not to destroy the device or not to change the device performance fabricated in the beneath layer." They proposed that the key was to "to control the thermal profile in the polysilicon layer" and Akasaka proposed "…a laser or an electron beam recrystallization is thought to be a suitable method due to their effective low process temperature." Certainly laser annealing has come a long way since the first prognostications of Aksaka.

Packaging

Zvi Or-Bach of Monolithic 3DIC is now proposing the use of Smart-cut for the formation of the second strata (and not amorphous silicon crystallization) with shielding layers to protect the first strata interconnect, as shown in **FIGURE 1.**

Will these advances allow monolithic 3DIC to compete with TSV based 3DIC? Some say that sequential 3D technology can be much less complex and expensive to implement. Maybe we will be finding out soon.

CEA-Leti recently announced an agreement with Qualcomm to assess the feasibility and the value of sequential 3D technology [link]. The program between Leti and Qualcomm reportedly "..will allow the critical assessment of this technology in the context of practical applications, further evaluating the potential impact of this sequential 3D technology for future industrialization."

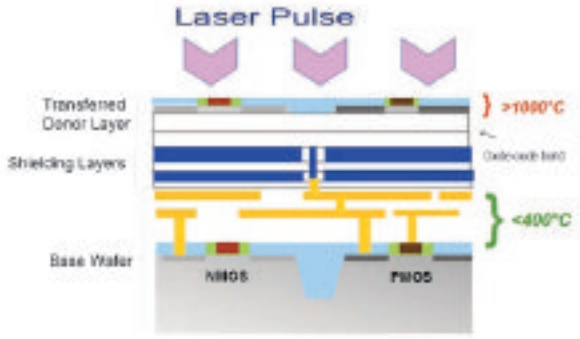


FIGURE 1. Monolithic 3DIC is proposing the use of Smart-cut for the formation of the second strata with shielding layers to protect the first strata

In early January Taiwan's National Applied Research Laboratories (NARL) said can use monolithic 3D-IC technology to make "super chips." They reported that it "enables 150 layers of chips to fit in space once used to stack a mere two chips using traditional technology while helping improve signal propagation speed and provide a higher order of connectivity."

At the recent IEEE IEDM meeting, Taiwan's National Nano Device Laboratories described fabricating a monolithic sub-50nm 3D chip, which integrates high-speed logic and nonvolatile and SRAM memory. To build the device layers, the researchers deposited amorphous silicon and crystallized it with laser pulses. They then thinned and planarized the silicon, enabling the fabrication of ultrathin, ultraflat devices. The monolithic 3D architecture demonstrated 3-ps logic circuits, 1-T 500ns nonvolatile memories and 6T SRAMs with low noise and small footprints.

Will 20nm high volume manufacturing be delayed?

Pete Singer,
Editor-in-Chief

Handel Jones, founder and CEO of International Business Strategies (IBS), spoke at SEMI's Industry Strategy Symposium in January, focusing on key trends, factors impacting the growth of the industry and the migration to smaller feature dimensions. He is bullish about 2014 and industry innovation, but cautious about how quickly the industry will move to new technology nodes due to higher costs, and long design cycles. Overall, he said he believed semiconductor market growth this year will be slightly better than 2013, due in part to the strength of the global GDP.

Perhaps most surprisingly, he had a fair amount of uncertainly about 20nm. "Will 20nm be a high tech technology node and when will that occur?" he said. "We're tracking design starts and design completions and we see a few 20nm designs but not a lot. Frankly, whether 20nm will be big or not will really depend on two customers: one is Qualcomm and the other is Apple." Handel said "there is a significant challenge in getting lower cost at 20nm" compared to 28nm due to a lack of increase in the gate density and the potential yield impact. "We think 20nm, if it does go into volume production, it will not be in 2014. Potentially 2015 and maybe 2016," he said.

Similarly, Handel believes there will be a postponement of 16/14nm. "We expect initial production in late 2016, beginning of 2017. That's for the SoC business. The FPGA markets will be different," he said. "There will also be delays in 10nm. Delays mean you can't really go on the 2 year cycle or even the 3 year. I know people will vehemently disagree with that, but if you look at what's really happening from a design start point of view and also the end customers, I think you'll agree with our conclusion," he said.

"If you look at the reality of the industry, 28nm high-k metal gate went into high volume production toward the end of 2013," said, adding that they define high volume as 10% of the output. "It took almost 4 years for 28nm high-k metal gate to go into high volume production. Now we're basically starting 20nm. Even if the fabs are ready what you have is the design cycle time. Preparing libraries and IP can take six months at least. Doing a complex design in 20nm can take you at least a year. Validating the design can take you another half a year. If it's a modem, and you need approval from the carriers, that's another half a year. Even if the fab is ready, you start these things and it's two years," he said. "We have an industry that is trying to adopt three technologies in three years. It's impossible," he said. "It's not realistic from an infrastructure point of view, even if it the fabs are there, for three technology nodes to ramp in three years."

Handel said that application processor (AP)/modem design can cost about $450-500 million in 16/14nm, with a timeframe of around 18 months. "You need 10X revenue so for that design, so if you're spending $450 million, you need $4.5 billion in revenue. A few companies can get that, but not many," he added.

"The economics of the industry are forcing changes. You've seen them already. The long ramp up time for 28nm HKMG, and 20nm with double patterning is clearly a major challenge from a technology point of view, and a bigger challenge from a cost point of view. FinFETs will be an even bigger challenge. Intel is having delays in their 14nm FinFETs, whether in high volume at 22nm, how will companies that have never done FinFETS before, how will design companies that have never designed in FinFETs before, how will they ramp faster?" he asked. That's a very good question.

2014 outlook: An era of unprecedented change

We asked leading industry experts and analysts to give us their perspectives on what we can expect in 2014. All expect it to be a banner year for the semiconductor industry, as the world's demand for electronics continues unabated. However, most believe we are seeing an era of unprecedented change, driven by a shift to mobile computing, the Internet of Things, higher wafer costs and difficult technical challenges. To address these challenges, new levels of innovation and collaboration will be needed.

Cyclical upturn continues in 2014: Positive yet cautious expectations persist

Bill McClean, President, IC Insights.

In 2013, the IC industry emerged from a difficult 5-year period of minimal growth and started on its next cyclical upturn, a welcome piece of news. From 2007-2012, the IC market grew at an average annual rate of just 2.1%. In IC Insights' opinion, the current cyclical upturn that started in 2013 will continue with several solid years of growth, peaking with 11% market growth in 2016. The IC market CAGR is forecast to nearly triple to 5.8% in the 2013-2018 timeperiod. During this time, unit shipments are forecast to increase at an average annual rate of 6.3% and the total IC average selling price (ASP) is forecast to decline at an average rate of 1.0%.

IC Insights believes that IC industry cycles are becoming increasingly tied to the health of the worldwide economy. It is rare to have strong IC market growth without at least a "good" worldwide economy to support it. Consequently, over the next five years, annual global IC market growth rates are expected to closely mirror the performance of worldwide GDP growth.

After increasing 2.8% in 2013, global GDP is forecast to rise to 3.4% in 2014 (**FIGURE 1**), which is on par with the 30-year average. The U.S., Japan, U.K., and the Eurozone (i.e., mature economic markets) are each forecast to experience improved, though still tempered, GDP growth in 2014.

In the U.S., the most significant factor holding back better GDP growth has been the high unemployment level. The unemployment level gradually improved and stood at 7.0% in December 2013. Some forecasts show it decreasing to 6.5% by the end of 2014. An improving employment picture, strong orders for new equipment, and upward-trending economic indicators add up to positive momentum for the U.S. economy heading into 2014.

China, which is the leading market for personal computers, digital TVs, smartphones, and automobiles, is forecast to lose more economic momentum in 2014. Its GDP is forecast to increase 7.5% in 2014, which continues an annual downward trend that started in 2010. China's GDP growth was 7.7% in 2013. China's new leadership is attempting to shift the country's growth from being highly dependent on infrastructure investment and exports to one that relies more on consumer consumption.

The historical correlation between worldwide GDP growth and semiconductor industry growth is good, but IC Insights believes that this correlation will be

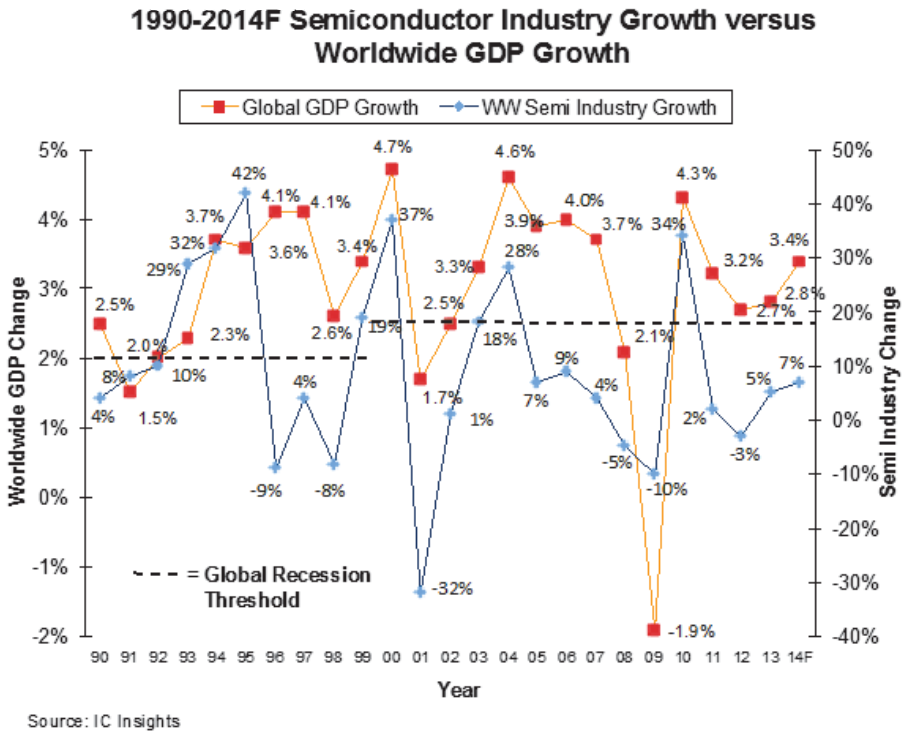


FIGURE 1. Global GDP is forecast to rise to 3.4% in 2014, which is on par with the 30-year average.

very good in 2014. Using a worldwide GDP forecast of 3.4%, the most likely range for worldwide semiconductor market growth in 2014 is 2-12%, with IC Insights' forecast calling for 7% growth in the 2014 semiconductor market.

Outlook for semiconductors and the value chain in 2014

Mike Corbett, Linx Consulting and Duncan Meldrum, Hilltop Economics

We approach 2014 with a combination of positive policy, financial, and economic forces that will push world growth up to a +3% range. With positive developments on the U.S. policy and jobs front, slow progress in Europe, and stabilization in Asia, the outlook for reasonable global growth in 2014 looks better than it has since the first year of recovery from the recession of 2008-09.

For the last few years, economic forecasts from most private and public forecasting groups were downgraded consistently as time passed as forecasters adjusted their longer term forecasts downward for the weaker capital accumulation that has occurred in this recovery. That process finally appears to be ending. The latest forecast revisions by Consensus Forecasts have been much more balanced, resulting in a barely perceptible upward revision to the world growth outlook.

Linx Consulting and Hilltop Economics have worked to tie global economic output to silicon demand, through a proprietary modeling service. Silicon demand, expressed in terms of millions square inches (MSI) is now projected to grow 6.5% in 2014. This is stronger outlook is based on demand improving, some snap-back from the Q4 slippage, and lower uncertainty around policy.

While this growth is a welcome relief from the relative stagnation for the last few year, and we have seen prices increase in traditionally price sensitive markets such as DRAM, this does not mean that the industry is on the path to sustained profitability, as it is entering an era of unprecedented change. There is fundamental industry change as the market re-aligns itself to transition from the PC era to the mobile era as well as architectural and technology changes. Key architectural changes being implemented include changes in both memory and logic devices, with the introduction of FinFETs and 3D NAND and MRAM, etc. Key technology changes the implementation of EUV lithography, novel materials as well as the introduction of 450mm wafers. All of which have inherent risk and need to be adequately funded and developed through to commercialization.

We already see the industry value chain re-aligning to face these major challenges. There are fewer IDMs investing in advanced node manufacturing; consortia are being reorganized and set up to help with the basic research; OEMs are consolidating to produce the scale required to bring new technologies and processes on-line; and, the chemicals and materials suppliers are starting to gain more knowledge on upstream suppliers for quality issues and some are exploring their strategic options for their electronic chemicals and materials business.

The semiconductor industry has a long history of success based on continued innovations in the business model, advanced technological solutions and forward thinking vision. Change is also a certainty in this

industry. In order to address the long list of challenges above, we believe that not only will new collaborative models be required, but they must be funded on a sustainable basis as well. Ensuring sufficient funding and profitable returns on R&D and capital investments will be a challenge for the entire industry.

Coming year promises increased capital spending and continued need for effective industry collaboration

Denny McGuirk president and CEO, SEMI

For most of the past 15 years, the industry has displayed a fairly predictable pattern of fab equipment spending, characterized generally by two years of decline followed by two years of positive growth. In 2012 and 2013, the fab equipment market contracted, while 2014 and 2015 are expected to be positive. According to the SEMI World Fab Forecast, the 2014 wafer fab equipment market is expected to grow over 28% to $32.2 billion. Taiwan will lead in spending (over US$9 billion), while Korea and the Americas will each spend at least $6 billion, and China and Japan will each spend about $4 billion. Spending for packaging and test equipment will also rebound in 2014 to $2.5 billion (4.2% growth over 2013) and $2.95 billion (5% growth) respectively. Spending on semiconductor materials will mirror semiconductors unit growth reaching an estimated $45 billion (2.5% growth)

In terms of construction, across the industry, there were 40 major projects on-going in 2013, and 28 are predicted for 2014. Construction spending growth for 2013 was about 40% (to $7.5 billion). By 2014, this will drop by 15% (to $6.4 billion). Several large construction projects are already underway or expected to start soon, but construction spending is expected to decline in both years. The two industry segments predicted to add the most capacity, based on demand, are foundries and NAND. Other segments, such as DRAM, analog, and logic, are not expected to add new capacity. MPUs may add some new capacity this year.

The coming year may add more clarity to uncertain technology roadmaps. The economics of technology nodes are increasingly dependent on the continued source power and throughput improvements on EUV lithography. These uncertainties, including the roll-out of 450mm wafer processing, have impacted plans and schedules for high-volume production. Penetration of 2.5D and 3D stacked ICs into high-volume applications are also dependent on continued process technology improvements. New materials and process innovations will continue to unfold in non-planar transistor architectures, and new test methodologies and flows will develop to meet the needs of leading-edge devices, including 3D stacked devices.

With increasing economic and technological uncertainty, the industry will continue to develop and evolve methods for more effective collaboration and expanded public-private partnerships. In addition to tighter supply chain engagement on next generation nodes, 450mm wafer processing and 3D-IC, both the European Union with its 10/100/20 program, and the U.S. Government, through the National Network Manufacturing initiative, will offer increased visibility and support for microelectronics manufacturing in the coming year.

The shift to materials-enabled 3D

Randhir Thakur Executive Vice President, General Manager, Silicon Systems Group, Applied Materials, Inc.

Innovations in mobile computing and communications will continue to be a driving factor for the semiconductor equipment industry. To enable high performance chips for new and exciting applications, our foundry/logic and memory customers that manufacture semiconductors are migrating from lithography-enabled 2D transistors and 2D NAND to materials-enabled 3D transistors and 3D NAND. These device architecture inflections require significant advances in precision materials engineering in conformal materials deposition, materials removal, and materials modification. Selective materials processes will play a more prominent role. Smaller features and atomic-level thin films also make interface engineering and process integration more critical than ever.

Some significant ongoing industry developments to highlight are the new materials and architectural changes in the transistor to reduce power consumption

and drive performance gains. The increased complexity of the 3D FinFET architecture in combination with continued scaling requires great precision in structure formation, especially when forming the gate. More advanced atomic-level process technologies in selective epitaxy, metal gate, implant, anneal, etch, and planarization are needed. Also critical to meeting the industry's precision engineering requirements are improved materials that offer more choices for increasing selectivity, control and performance. And, let's not forget the advances underway to develop new higher mobility channel materials.

Another exciting inflection in 2014 is our memory customers' transition from planar two-dimensional NAND to vertical three-dimensional NAND. 3D technology holds the promise of terabit-era capacity and lower costs by enabling denser device packing, the most fundamental requirement for memory. There are complex device performance and yield challenges, such as distortion-free high aspect ratio etching, staircase case patterning with precise step-width control, uniform and repeatable gate stack deposition. As memory makers introduce and scale this game-changing new technology from 32 to 48 to 64 and higher cell layer stacks, Applied Materials is focused on providing the precision materials engineering solutions to address their challenges.

The pace of technological innovation and change – especially in our increasingly global and connected world – is accelerating. Applied remains at the forefront of enabling these inflections with industry-leading technologies and expertise in precision materials engineering. We are collaborating earlier and deeper with our customers to solve device performance and yield challenges to extend Moore's law and enable new applications in our everyday life.

Innovation and collaboration key in 2014

Joe Cestari President, Total Facility Solutions

As far as the outlook goes for 2014-2015, investments coming from the semiconductor and microelectronics industries are going to be pretty robust. However, it will likely remain a consolidated group effort, with a majority of the investments coming from the few major players in the industry. The latest semiconductor industry forecast suggests a 21% increase in semiconductor equipment sales in 2014 to almost $44 billion.

The key drivers are flash fab investments in China and Japan, as well as processor and foundry fab investments in Ireland and the U.S. Strong demand for smartphones and tablet devices and pent-up need for capacity will lead the industry to one of the highest levels ever for equipment investment. Although equipment spending will see strong growth, new fab investments are expected to drop in 2014, as fabs under construction in 2013 will be installing tools in 2014.

We continue to see a need for increased collaboration moving forward. Whether you are a believer in Moore's Law or not, technology needs to continue to advance for the sake of cost and efficiency. However, this is not easily accomplished without some level of collaborative technology development. New efforts from the likes of the G450C and F450C should help drive the level of industry collaboration that will be necessary to advance technology in the years ahead.

The U.S. finds itself in a unique position; the market is still lingering with uncertainty as we deal with economic and political issues. However, US manufacturing costs are now on par with developing countries as land and labor continue to diminish as part of the overall capital and operating costs for a factory, so we should continue to see increased technology investments especially in the area of personal health and quality of life products.

In the coming years, we will need to find new ways to foster innovation. Gone are the days when start-ups were popping up left and right, but we need to continue to see this type of technological creativity and innovation to keep our industry alive. It's our job now to help nurture a new generation of engineers that have that start-up mentality, so we can continue to grow this industry at the pace our consumers demand.

Can we keep on benefiting from Moore's Law?

Rich Goldman Vice President, Corporate Marketing and Strategic Alliances, Synopsys

Keeping up with Moore's Law has always required significant investment and ingenuity, and this era brings additional challenges in device structures, materials and methodologies. As costs rise, a dwindling number of semiconductor companies can afford to build fabs at the leading edge. Those thriving include foundries, which spread capital expenses over revenue from many customers, and fabless companies, which leverage foundries' capital investment rather than risking their own. Thriving, leading-edge IDMs are now the exception. From a market perspective, companies focused on segments such as mobile, automotive, mil-aero and medical are prospering.

With this environment as a backdrop, we see five trends dominating the year ahead and expect companies leading in or well positioned to address these areas to do well.

FinFETs. Chipmakers will no doubt keep us well informed as they progress through FinFET tapeouts and deliver production FinFET processes, touting their power and speed advantages for customers. Those early to market will press their advantage by pursuing aggressive FinFET roadmaps.

IP & subsystems. As devices grow more complex, integrating third-party IP has become mainstream. The trend for reuse of integrated, tested IP is beginning to expand upwards to systems, so that designers no longer need to redesign well-understood systems, such as memory, audio and sensor systems.

Internet of Things/sensors. The Internet of Things is poised to ignite huge growth in 2014. Sensors will emerge as a key enabler, connecting our physical world to computation in products that allow us to remotely control our surrounding environment. Meanwhile, a wide variety of sensor types will enable the mobile phone to continue subsuming and disrupting markets from cameras, satellite navigation systems and fitness devices, to flashlights and other applications.

Systems companies bringing IC design in house. Large companies successful in system-level design and development, such as Google, Microsoft and others, are bringing IC specification and/or design in house in the belief that that they can do the best job of IC design for their specific needs.

Advanced designs at both emerging and established process nodes. While leading-edge semiconductor makers drive forward on emerging process nodes, others are finding success by focusing on established nodes (28nm and above) that deliver required performance at reduced risk. Thus, challenging designs will emerge at both ends of the spectrum.

2014 outlook: MEMS on the rise

Tony McKie, CEO, memsstar, Ltd.

Looking at the global MEMS market, industry experts are predicting double-digit device growth in the next three to five years. How that translates into capital equipment spending is yet to be determined. MEMS growth continues to be driven by consumer electronics, mobile and handheld applications. Significant additional growth will come from the Chinese mobile market, which could account for as much as 30% of overall MEMS spending for mobile and handheld applications.

There are ever-increasing opportunities for low-cost MEMS within the consumer market, which will drive innovation in the coming years. For example, not everyone needs a high-end microphone on their handheld or mobile device, so there remain opportunities to provide low-cost MEMS for these applications. Even a state-of-the-art smartphone has room for both low-cost and high-cost MEMS options, representing opportunity in a very cost-sensitive market.

Regarding new applications for MEMS, the market is limited only by people's imagination. For the sensor market, innovation will come down to how we integrate sensors onto new platforms. This results in MEMS being incorporated further into people's everyday activities; for example demand for sensors in the sports and personal health industries will grow significantly.

Challenges remain. In a cost-sensitive market, manufacturers will demand efficient processing with high yields compatible with a wide range of standard films and materials. This will allow MEMS devices

to be manufactured using standard equipment and processes, thereby minimizing cost.

While MEMS don't follow the demands of Moore's Law, increasing complexity and size will demand more advanced processing capability and performance focused on cost-effective volume manufacturing.

Challenges and innovations on front-end and 3D TSV

Frederic Raynal, CTO, Alchimer

Looking at 2014, we see challenges and innovations in both the front-end semiconductor and 3D TSV markets.

In the front end, we are seeing a focus on further scaling to smaller nodes. For logic, TSMC has just announced it is ready for 16nm node, and Intel is ramping to 14nm. Industry experts question whether shrinking to 10nm will be feasible from a technology perspective. For example, at 10nm, most of the layers in copper interconnection must be between 2 and 4nm thick, which poses challenges for the technologies used in volume manufacturing. Controlling the thickness of single as well as dual damascene layers requires new technologies, such as electrografting, which is much more controllable and able to meet emerging requirements. We strongly believe that new technologies will need to be introduced for logic at the 10nm node and memory at the 16nm node, with ramp occurring at the 10nm node for the industry to maintain the path of Moore's law.

We also expect to see 3D TSVs ramping to production in 2014. This is another area where innovation is needed that can meet demanding performance requirements while controlling costs, since cost is currently holding back widespread adoption of 3D-ICs. High-aspect-ratio (HAR) vias are a good candidate for new technology like electrografting, which is cost competitive compared with electrochemical deposition, chemical vapor deposition or physical vapor deposition, and delivers higher performance. For example, 40:1 aspect-ratio capabilities were recently demonstrated for electrografted barrier and seed layers, and 20:1 aspect ratio for fill processes.

It is widely expected that both the front-end and packaging areas of the semiconductor industry are poised for growth in 2014. Continued technology innovations will be a key driver in both areas in order to meet emerging performance requirements while successfully controlling cost and overcoming current roadblocks.

Productivity data is essential to success in 2014

Michael Plisinski, VP & GM Data Analysis and Review Business Unit, Rudolph Technologies, Inc.

We expect the demand for productivity data to be at an all-time high in 2014. Semiconductor manufacturers are under pressure to increase the yields of new, increasingly complex manufacturing processes. In the front-end, manufacturers are aggregating data across the fab to provide a more complete picture of the process interactions and improve tool productivity. In the back-end, manufacturers are implementing new "more than Moore" technologies, including three-dimensional ICs and advanced packaging processes that increase computing density by means other than reducing the size and increasing the number of transistors. These approaches require the integration of data not only across a fab, but from multiple fabs and factories around the world. Finally, consider the wide variety and disparate nature of the many sources of data that must be accommodated -- inspection and metrology systems, tool sensors, tool recipes, electrical tests, the fab environment and more -- and the magnitude of the challenge facing electronics manufacturers and suppliers of factory information systems becomes clear.

At Rudolph, we expect this challenge to come into clear focus in the coming year and we anticipate growing demand for robust yield management software systems that offer the capability to analyze large, complex data sets from across the factory and the supply chain. These systems must deliver more accurate information to customers faster than ever before. The scope of the information must expand to include not only yield improvement, but also improvements in equipment and engineering productivity, as well as reductions in manufacturing costs.

2.5/3D needs innovation in 2014

Leo Linehan, Global Business Director, Growth Technologies Business, Dow Electronic Materials

Recent customer data and analyst predictions for 2014 are projecting modest overall growth in the semiconductor industry, with higher growth expected in the advanced packaging sector. The demand for portability and the Internet of Things are driving packaging technologies that enable system-level integration of heterogeneous devices such as logic, memory, MEMS, RF and Si-based photonics.

One area to follow closely in 2014 is 2.5D/3D IC integration activity, because processes and materials play an important role in solving the remaining challenges holding up high- volume manufacturing (HVM) of these technologies. As such, much investment has and will continue to go into materials R&D for 2.5D and 3D ICs.

Looking at 3D ICs, the greatest challenge—and one that will be a focus in 2014—is developing material sets that will enable high-yield devices at competitive price points. Areas of interest include: temporary wafer bond/debonding to address thin-wafer handling; solutions for stress management, utilizing low-temperature polymer dielectric systems that help customers to manage their thermal budgets and to use thinner wafers while maintaining package reliability; development of copper (Cu) for Cu pillars as these structures become a mainstream technology with the incorporation of pillars of various pitches and designs for packaging applications; and solder materials, like tin-silver (SnAg) for tin-silver capping of Cu pillars.

Challenges caused by finer-feature sizes, thin-wafer handling and thermal issues can all be solved in large part with the right material sets. We anticipate 2014 will be a year of innovation to enable these technologies to ramp into HVM to meet the demands of the next generation of portable devices.

Turning collaboration into action

David Hacker, Strategic Marketing Manager, Edwards

As the semiconductor manufacturing industry enters another year of scaling down transistors and continues on the bumpier road of scaling up wafer sizes, there are grounds for optimism. The early indicators on projected capital expenditures across semiconductor device manufacturers seem positive for the leading companies, and perhaps more significantly, there are also indications that a broader base of other players is also ready to increase their investments.

While this ought to be universally accepted as good news, it does highlight one of our industry's historic conundrums. How and where do we strike the equilibrium between tactical demands for maximizing near term income and the strategic imperatives for investments in future innovation and development? Each organization has its own specific approach to resolving these challenges. While those methodologies are rightly confidential, the consequences should be made transparent, where practical, so that our industry can come into a productive alignment.

Uppermost in my thoughts about 2014 in this context is the potential impact of industry misalignments on the pace of development of 450mm and associated bridging node transitions. Since the first tentative steps on road to 450mm, opinion has been divided on whether and how we can avoid the mistakes we made in the stop and go implementation of the 300mm transition. We have heard much (some might say too much) about the need for collaboration. Now is the time, in these pre-competitive phases, to act to address that need and develop a cooperative model that balances collaboration and competition for the benefit of all.

Growth in base station markets may fuel acceleration of the adoption on GaN

Adrian Wilson, Head of Technologies Division, Element Six

Towards the end of last year analysts were predicting the global LTE base station market to grow at a rate of 49.5% CAGR from 2012-2016. In addition to the

rapid growth of LTE Base Stations, the carrier Wi-Fi market is following a similar pace. As many of you have no doubt read, the increase in carrier Wi-Fi is being driven by a combination of end-users with Wi-Fi enabled devices and the need to off load cellular traffic onto this alternative network.

It is anticipated that Wi-Fi will be integrated into small cell LTE base stations in the near future, where the interface to the carrier will be via the LTE network and the end-user interface will be via Wi-Fi.

At a regional level, China will reportedly install 3.5 million new macro cellular base stations in the next 6 years. As a reference, the US to date only has installed a total of 2 million cellular base stations of all sizes. Looking further afield, by 2018 it is projected that Asia-Pacific will represent almost 45 percent of the world's LTE installed base.

Even in countries where mobile phones have already saturated the market, the growing share of smartphones further increases the need for more wireless infrastructure; smartphones, for instance, use 24 times the data than that of traditional mobile phones.

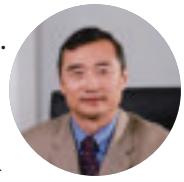
This combination of rapid growth in the population of base stations and the integration of Wi-Fi with small cell LTE base stations will demand radio-frequency (RF) power applifiers (PA's) with more power per module within the same or smaller footprint. This will enable base stations to continue to fit in small spaces andlower overall system cost, but will require much higher power densities. The convergence of this technology need in combination with the increasing availability of GaN RFdevices will see GaN being used in more and more designs requiring high-power RF PA's in 2014.

In recent years, Gallium Nitride (GaN)-based RFPAs have emerged as the leading solid-state candidate technology to replace silicon LDMOS and GaAs devices in many wireless applications, including cellular base stations. GaN is attractive for these applications in part because of its fundamental materials and related electrical properties. As a wide-bandgap material, it exhibits a high breakdown voltage thus enabling high power and high efficiency transistors. Power densities and power added efficiencies of 40W/mm and more than 65% respectively at 10GHz have been reported.

So with the need for more powerful RF PA's and GaN's ability to fulfill this need, 2014 will see GaN being used in more and more systems requiring RF PA's such as cellular base stations. However, as state-of-the-art GaN devices are driven to produce more power, heat overwhelms the transistors' gates and the material's maximum performance is never realized. So 2014 will also see increasing innovation in implementing thermal management solutions for GaN RF PA's. Engineers will increasingly explore and implement the use diamond heat spreaders, GaN-on-diamond wafer substrates, micro-channel cooling elements, and many other thermal-management solutions. GaN, when intimately bonded to Diamond, can operate at power densities in excess of 100W/cm2, satisfying the ITRS roadmap requirements.

Predicting 2014: The year of the SPICE model

Zhihong Liu, Executive Chairman, ProPlus Design Solutions, Inc.



2014 may be the year of the SPICE model. But then again, I could say this every year. The reason is simple –– the semiconductor industry continues to see the trend toward a closer working relationship between design and manufacturing, and SPICE models serve as the critical link.

At this point in time, however, the emphasis is more pronounced than usual as we see challenges managing process variations, plus we are transitioning from planar to 3D devices. Certainly, it becomes not only modeling engineers' concerns. It also draws increasing attention from designers, especially for leading-edge designs at advanced nodes.

SPICE models are getting more complex and hundreds of parameters are needed to accurately model characteristics of modern devices and processes, such as FinFET. Process variations, including random and systematic, and reliability aging effects that incorporate bias temperature instability (BTI), are limiting factors for a competitive design with acceptable production yields at advanced nodes.

SPICE models have direct impact on circuit simulations. As model complexity increases, using one set of parameters to model the entire process and the device characterization space becomes more difficult.

Certain rules, guidelines and assumptions, sometimes wrongly viewed as model "imperfections," have to be applied and are often embedded in the model document

or process design kit (PDK) to be considered in later design stages.

As a result, advanced designs rely on model quality. More important, designers need to have a better understanding of advanced node SPICE models and their limitations. They need to know how to properly use the models in their designs and what steps they can take to make a better design.

In 2014, FinFET will capture everyone's attention. Foundries will try to provide accurate yet calculation-efficient SPICE models for designers. Designers will look into models for this innovative device type, and look for good-quality SPICE models for their designs.

However, we already know FinFET modeling and FinFET SPICE simulation are challenging. Again, SPICE models are the keys to both. The answer may will be Verilog-A based BSIM-CMG model as they go mainstream with FinFETs, once again pushing SPICE model to the forefront.

Automated TEM and sample preparation accelerate ramp for new products

Matthew Knowles, Ph.D., Product Marketing Manager, FEI

At FEI we see at least two drivers assuming primary importance in our semiconductor manufacturing markets in the coming year. On the business side, time-to-market for new products is becoming increasingly important, as the first to market with new products enjoys a tremendous advantage in market share and value pricing. On the technical side, as device geometries continue to shrink, we may well be approaching a tipping point in the shift to transmission electron microscopy (TEM) as resolution requirements increasingly exceed the capability of the scanning electron microscope (SEM). Coupled with this shift is increasing demand from users for TEM systems that are easy to operate and provide a seamless start-to-finish workflow from wafer to results.

As the transition to TEM accelerates, process engineers are too often starved for the high-resolution information they need to accelerate the critical ramp from process development to high-volume production. The number of analyses is strictly rationed and turnaround times are too long. Increasing the number of TEMs is an obvious solution, but equally important is increasing the speed and productivity, and reducing the cost, of TEM analysis. Sophisticated automation will address these issues in the TEM itself, increasing speed and reducing requirements for specialized operator skills. However, the TEM itself is not the primary challenge. Preparation of the extremely thin samples required for TEM analysis has always been a bottleneck due to the artistry required by the operator. New automated sample preparation systems, located in or near the fab, will prepare site specific thin sections from full wafers at a fraction of the time and cost of manual techniques. Additionally, the resulting samples are much more uniform and repeatable in thickness and uniformity. When imaged downstream in the TEM, this results in more reliable images and process control information. Specifically-designed workflows for pathfinding and technology development, yield ramp and process verification, and high-volume production control will integrate seamlessly with the user requirements, eliminating the analytical bottleneck and providing engineers with an abundance of the information they need to insure their products are first and best.

Keys to success: Testing in the new mobile world

Michel Villemain, CEO, Presto Engineering, Inc.

The semiconductor industry is moving from a PC-centric, digital era to a communication and mobile world. This, combined with integration, is driving chips to interact more with the real world and to become increasingly analog. It has a profound impact on test and automated test equipment (ATE). Test equipment used to be rated by speed and timing accuracy, and priced by pins, but those are no longer defining features. The ability to support a wide range of analog and RF measurements is now the critical specification of a modern test solution.

Not so long ago the critical elements were the timing chip and the pin electronic IC. Both were advanced ASICs and defined the price of the equipment. Today, FPGAs support most speed and timing test requirements of current system on chip (SOC) devices, while bench instruments support most analog and RF demands. Bench systems are expensive and do not scale cost-effectively—

especially for parallel test. The challenge is therefore to package instrumentation into application-specific test hardware that offers a cost-effective, per-channel solution that can be scaled into multi-site test solutions. The successful test solutions of tomorrow will be those that can offer a portfolio of dedicated analog and RF options, and provide variations as quickly as the market itself evolves.

The second major back-end transformation, driven by communication and mobility, is packaging. More analog circuitry means not only new, multi-dimensional packages (including 2.5D and 3D), but also more bare die that are directly integrated into modules. As traditional test flows include wafer sort (primarily for fab yield control) and final test (quality insurance), bare die require a known-good die flow implemented by wafer-level test (WLT). New standards (802.11ad, 100/400G) and new RF bands will require probe technologies that can support up to 90GHz, combining reliable ohmic contact (signal integrity) with a gentle mechanical touch--especially on aluminum pads used by SiGe and CMOS processes.

Addressing these two challenges, for quickly deployed, dedicated analog/RF test solutions and reliable probing technologies, will allow cost-effective semiconductor solutions, then, in turn, deployment in volume of high-speed, high-bandwidth electronics solutions for communication and mobility.

Internet of Things driving change in the semiconductor industry

Dave Lazovsky, President and CEO, Intermolecular Inc.

With upwards of 30 billion devices projected to be connected to the Internet by 2020, the ensuing explosion of distributed compute, sensors and communication devices will usher in a new wave of semiconductor industry innovation and growth – the Internet of Things (IoT). Innovation in embedded memory will lay the foundation for a transition from NOR Flash technology (used in microcontrollers today) to more advanced embedded non-volatile memory (eNVM). Leading next-generation eNVM technologies include Resistive RAM (ReRAM) and Magnetic-based Spin Torque RAM (STT RAM). IoT products will benefit from advancements in these eNVM including higher performance, lower cost and lower power consumption.

Emerging eNVM technologies are the result of new memory device architectures, built from structures engineered at the atomic level with new materials. Every material and device structure change involves testing and analyzing tens of thousands of variables. This increasing device complexity has introduced significant economic challenges for semiconductor manufacturers. Research and development of advanced NVM technologies have contributed to exponentially increasing semiconductor R&D spending that reached approximately $60 billion in 2013. Intermolecular has pioneered an innovation platform and collaborative development model that increases R&D productivity by 10-100 times relative to conventional development methodologies. Intermolecular's customers are bringing new device technologies to market faster, and significantly reducing the risk associated with developing and commercializing advanced products based on novel materials and architectures.

Crisis? What crisis? New paradigm adjustments for capacity and equipment spending

CHRISTIAN GREGOR DIESELDORFF *and* **DAN TRACY**, *SEMI Industry Research & Statistics Group.*

Looking at the trends in the last 18 years, capacity growth rate in 2013 is at levels seen during an economic crisis, but what crisis exists?

The rock band Supertramp titled its fourth album "Crisis? What Crisis?" The title of the album, released in 1975, reflected the economic situation during that time. Back in 1973, OPEC proclaimed an oil embargo causing oil prices to soar; the stock market crashed and idled from January 1973 to December 1974, with the Dow Jones losing over 45 percent in 699 days; and a global recession put an end to the general post-World War II economic boom. This recession lasted from 1973 to March 1977, although the effects on the U.S. were felt into Ronald Reagan's first term. At that time, the semiconductor industry was in its infancy.

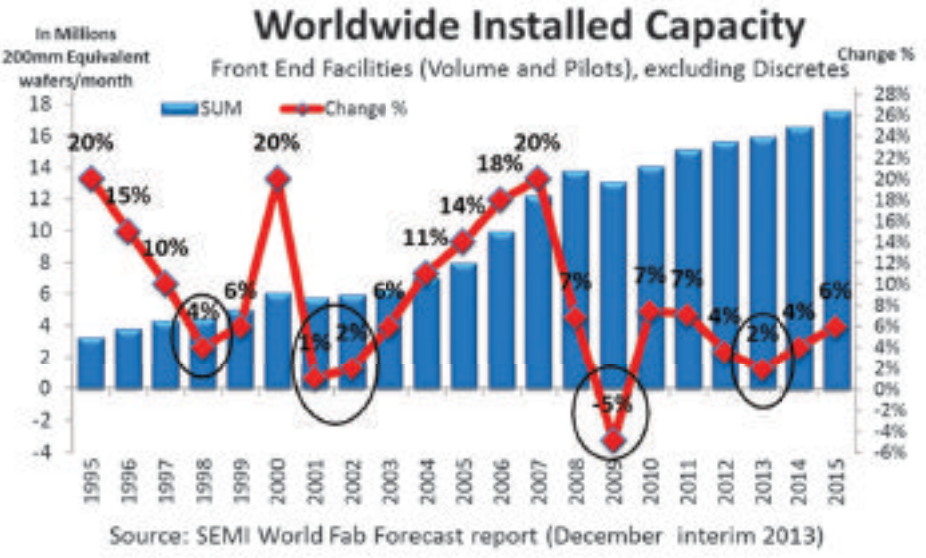


FIGURE 1. Installed capacity for front end facilities over time (without discretes).

Worldwide, the semiconductor industry growth rate back in 1973 was about 30 percent and slipped into 1975 with negative sales growth rates. Following a recovery in the late 1970s into the 1980s, the next negative growth for the semiconductor industry occurred in 1985 with a -17 percent decline in revenue. Another year of decline includes the -8 percent slide in 1998, surrounded by the Asian financial crisis in 1997 and the Russian financial crisis in 1998. The largest drop for the semiconductor industry, however, occurred in 2001 with the burst of the dot-com bubble, causing revenues to fall to -32 percent. More recently, the housing bubble crisis and the European sovereign debt crisis resulted in a revenue decline of -9 percent in 2009, certainly not as severe as in 2001 though the industry was on edge for a number of quarters as uncertainty reigned throughout the global economy

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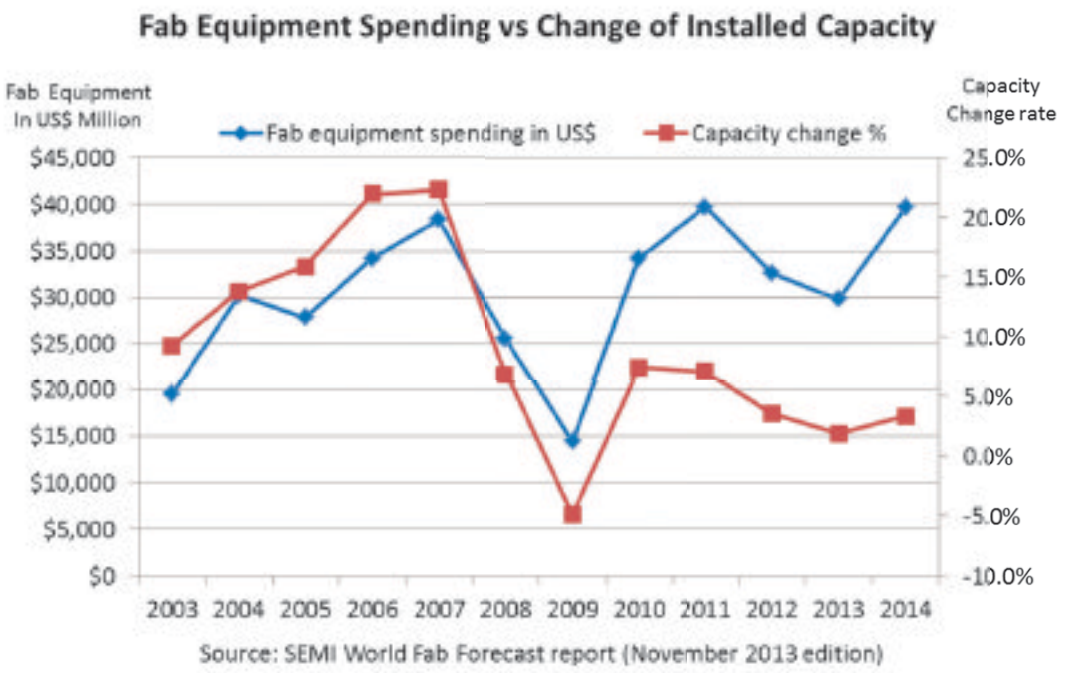

FIGURE 2. Fab equipment spending (new and used) for front end facilities versus change rate of installed capacity.

Comparing the 2001 crisis to the most recent crisis suggests a paradigm change for the semiconductor industry has transpired. Before 2009, capacity additions corresponded closely to fab equipment spending. These days, much more money is spent on upgrading existing facilities, while new capacity additions are much lower. In fact, the pace of new capacity additions has dropped to levels previously seen only during an economic crisis.

2013 installed capacity growth mimics economic crisis behavior

When SEMI's May fab database report was released, fab capacity was expected to increase 2.4 percent in 2013. By August, this was revised down. New data have caused a further revision down to 1.9 percent for 2013 (see **FIGURE 1**). The SEMI World Fab Forecast Report data also support lower expectations for capacity expansion in 2014 (5.4 percent predicted in May, down to 3.9 percent in August, and now to 3.3 percent in November). Most likely, device makers seek to avoid oversupply and a drop in selling prices for devices.

Looking at the trends in the last 18 years, capacity growth rate in 2013 is at levels seen during an economic crisis, but what crisis exists?

Semiconductor revenues for 2013 are expected to grow 4 to 6 percent, and 2014 expectations are also positive, mirroring other upward looking market indicators such as auto sales (at a six year high in September 2013), the Dow Jones (at a record high of 16,000 points in December 2013), and expansion of the U.S. GDP (up 4.1 percent in the 3rd quarter, as of mid-December 2013). So, why the low rate in capacity expansions?

The last time installed capacity growth rate was under 2 percent was during the 2009 economic crisis, and before that, in 2001. Even when impacted by the 1997 Asian Financial Crisis and the 1998 Russian Financial Crisis, capacity growth rates did not fall below 4 percent. So in examining history, capacity expansion in 2013 has behaved as if there were an economic crisis, despite no new crisis. In addition, SEMI (Figure 1) shows that addition of new capacity in 2014 will rank this year at the 4th lowest level over the past 18 years.

Another paradigm: more spending for existing facilities

Examining historic trends for equipment spending, most fab equipment spending before the 2009 crisis was going towards adding new capacity. After 2009, while fab equipment spending recovered, new capacity additions trended below pre-2009 growth rates (**FIGURE 2**).

In the five years between 2003 and 2007, the growth rate of new capacity increased from 6% in 2003 to 20% growth in 2007 (almost doubling the fab capacity in 5 years), according to the SEMI World Fab Forecast Report. This was driven mainly by DRAM and NAND companies in Korea, Taiwan and China. After the 2009 economic crisis, however, growth of new capacity dropped from 7 percent in 2010 to about 4 percent in 2014, thus with the expected capacity addition of only

17 percent in the five years from 2009 to 2014. Especially after 2009 we observed a number of company consolidations (Elpida, Powerchip, Rexchip), restructuring or change of direction (Promos, SMIC and a number of Japanese device makers), and even bankruptcy (Qimonda).

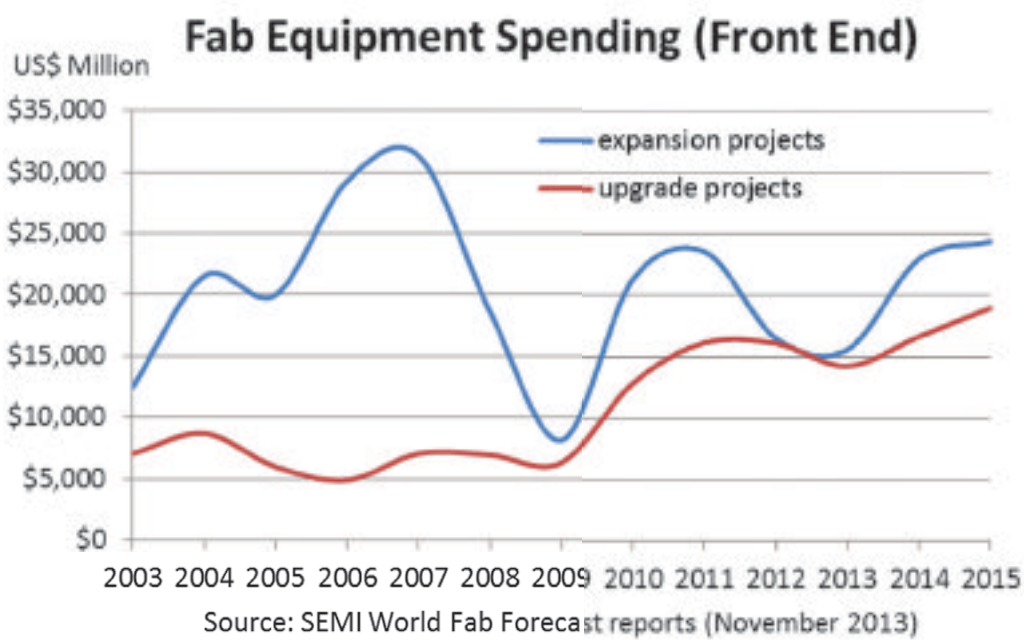

FIGURE 3. Fab equipment spending for new and used equipment (front end) for expansion projects and upgrade projects.

Increasing Spending for Upgrade Projects

Since the 2009 crisis, expenditures on upgrading existing equipment have grown sharply. Expansion projects, such as new fabs still account for the majority of fab equipment spending, but in lower proportions than in the past (**FIGURE 3**).

Costs for adding new equipment to a new facility are typically higher than upgrading some of the existing equipment. The number of companies building and equipping fabs continues to shrink through consolidation into larger companies as leading-edge technology upgrades become more expensive. Deployment of some leading-edge technology has begun to slow as NAND and DRAM industry bit growth moderates. For example, the cost per wafer to upgrade NAND to 3D generation may be twice as much as it was for 20nm class upgrades.

The new paradigm

According to SEMI, the two industry segments predicted to add the most capacity, based on demand, are foundries and NAND in 2013 and 2014. Dedicated foundries grew at a steady 10 percent in 2013, and will add another 8 to 10 percent in 2014. For the second largest segment, NAND, which lost about 4 percent of capacity in 2012, capacity rose 10 percent in 2013 and will add another 5 to 8 percent in 2014. Other segments, such as DRAM, analog, and logic, are not expected to add new capacity in 2013 and 2014. MPU may add some new capacity by 2014.

Top makers of mobile phones, Samsung and Apple, are major drivers for the industry. For example, after six years, Apple finally unlocked a crucial deal for iPhone ™ sales in China with 760 million potential customers, twice the U.S. market. This will inspire greater capacity additions such as for foundries and NAND.

Even in 2014, when the top two segments, foundry and NAND, are adding new capacity in upper single digits, the overall fab capacity growth rate globally is still among the five lowest in 18 year history meaning that other segments add little or no new capacity, or focus on upgrading process technology.

Crisis? What Crisis? The year 2013 was an unusual year. Compared to historical trends, globally new capacity growth appeared as in a year of economic crisis but there was none, and 2014 will be yet another year of minimal fab capacity expansion overall for the industry. Sectors that serve the leading edge for mobile devices will add the most capacity; other sectors reflect the lower growth observed across the broader semiconductor industry since the 2010 recovery.

The SEMI World Fab Forecast lists about 1,150 facilities. Sixty-seven of these (with various probabilities) have started or will start volume production in 2013 or later. The report lists major investments (construction projects and equipping) in 206 facilities and lines in 2013, and 180 facilities and lines in 2014. Visit www.semi.org/MarketInfo/FabDatabase.

A square peg in a round hole: The economics of panel-based lithography for advanced packaging

RICH ROGOFF, *Lithography Systems Group, Rudolph Technologies, Inc., Wilmington, MA*

Moving from round wafers to rectangular panels saves corner space, delivering a roughly 10% improvement in surface utilization.

We've been doing it for years–square die on round wafers. As the old adage suggests, we can make it work, but it is not always pretty. Now, as advanced packaging processes continue to develop–often adopting and adapting processes and equipment from front-end manufacturing–we need to be sure that we do not needlessly carry over baggage that impedes the optimization of these processes for their new applications. Front-end processes are designed to work on wafers, which are necessarily round and difficult to make larger. In the early days of advanced packaging, these wafer-level processes were extended to the back-end. Fan-in wafer-level chip-scale packaging (WLCSP) and wafer bumping are two prominent examples. However, as advanced packaging processes evolve further into the 2.5D and 3D space, opportunities present themselves to move away from round wafers and onto larger, square or rectangular substrates. Specifically, the manufacturing of fan-out packages on re-constituted substrates populated with KGD (known good die) and the use of high density interposer substrates for so-called 2.5D integration of advanced multi-die packages are experiencing above average growth. For these applications, the substrates can be rectangular and large. In fact, whole industries already exist, such as flat panel displays and solar panels, which

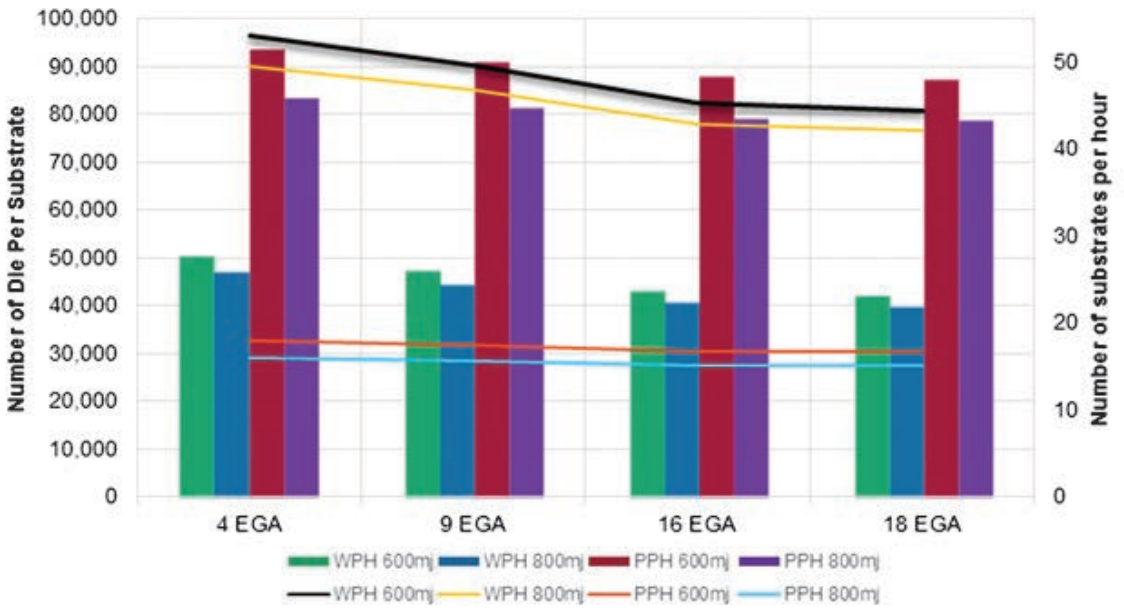

FIGURE 1. Results of throughput comparison.

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use similar manufacturing processes on large rectangular substrates.

In front-end photolithography processes, where square die first met round wafers, there is an inherent inefficiency near the wafer's edge, where squeezing as many die as possible onto the wafer inevitably results in part of the exposure field falling uselessly in the exclusion zone or off the wafer entirely. With an appropriately-sized rectangular substrate the rectangular pattern from the mask could fit perfectly, ultimately increasing the average number of die per exposure and thereby, the throughput of the exposure process. Likewise, using a larger substrate also increases throughput by reducing the nonproductive time spent exchanging substrates. Moreover, the same considerations that have historically driven increases in wafer size should also apply to non-round, non-wafer substrates, potentially providing substantial gains from using large panels throughout the manufacturing process. The flat panel display industry has increased its panel sizes over the years from 400 mm x 500 mm (Gen 2) to 2400mm x 2800mm (Gen 9) and beyond.

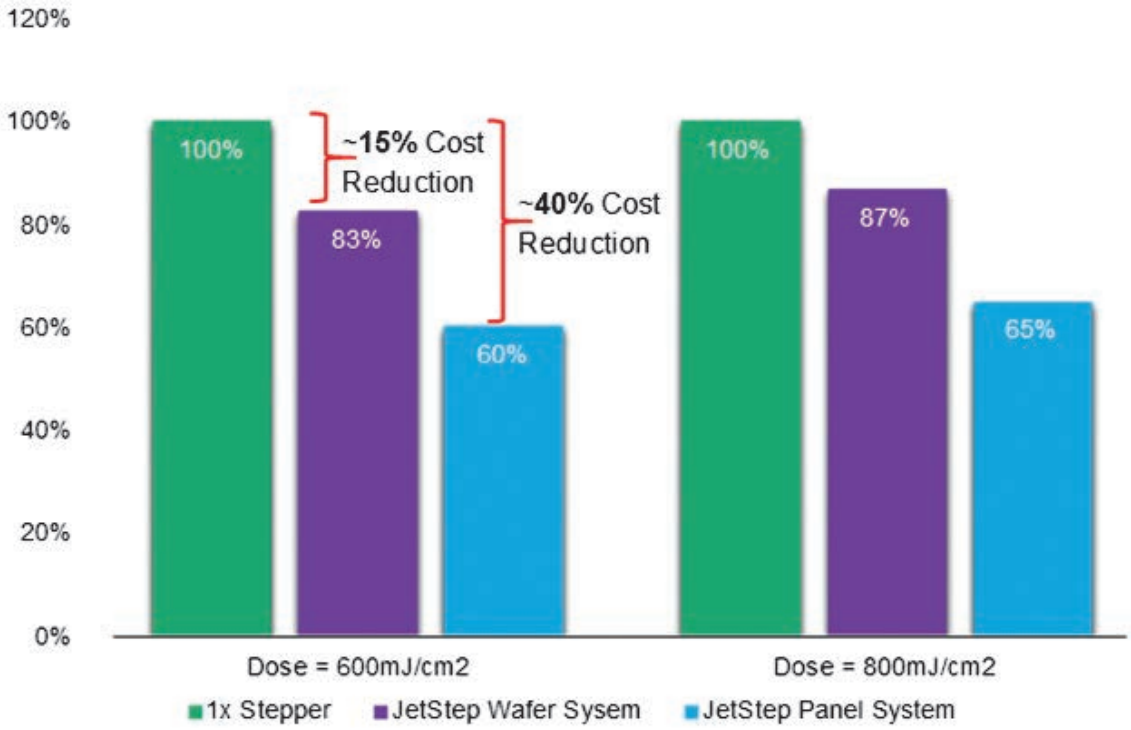

FIGURE 2. Relative cost per 100 die calculated for 8 mm X 8 mm die using 9 alignment points at 600 mj and 800 mj doses.

In an effort to understand the potential economic benefits, we constructed a model to compare the throughput of a 650 mm X 550 mm panel-based lithography process with a 300 mm wafer-based lithography process. The model considered 8 mm square die with 100 µm streets and a 5 mm wafer edge exclusion. We looked at two different mask (reticle) configurations containing 48 die (8 X 6) and 49 die (7 X 7) that could be exposed using the 84 mm diameter field of the 2x reduction JetStep™ Panel Lithography System (Rudolph Technologies). Both mask configurations resulted in 947 die per wafer. Since the square exposure field (7 X 7) required only 23 exposures, 6 less than the 29 exposures required by the rectangular field (8 X 6), all subsequent comparisons use the square field. The panel required 120 exposures resulting in 5214 die. It should be noted that either exposure field configuration was implemented on a standard 6-inch square, .25-inch thick reticle.

The most obvious advantage in the panel process accrues from the more than 5X greater number of substrate exchanges required by the wafer process, resulting primarily from the larger size of the panel substrate. Less obvious, but also important, are two different "square peg in a round hole" effects. The first is the decrease in the number of exposures required that results from the better fit of the rectangular field and the rectangular panel. The second is the increase in surface utilization that results from the better fit between the rectangular die and the rectangular substrate: 947 8 mm die cover 86% of the surface of a 300 mm wafer, whereas 5214 8mm die fill 94% of the surface of a 650 mm X 550 mm panel. A potential disadvantage of the panel process is the requirement for more alignment because of the increased substrate size.

For a more precise comparison, we calculated

	1X Stepper	JetStep Wafer	JetStep Panel
Exposure wavelength	ghi	ghi	ghi
Field size in mm²	68x26	66x52 or 59.4x59.4	66x52 or 59.4x59.4
Substrate size	Wafer 300mm	Wafer 300mm	Panel 650x550mm²
Dose use in mj	600 & 1000	600 & 1000	600 & 1000
Reticle size	6"	6"	6"
Lamp power	2 lamps at 1.2KW	3.5KW	3.5KW
Production parameters	90% uptime and 24/7	90% uptime and 24/7	90% uptime and 24/7
Number of exposures per substrates	44	23	120
Die sizes in mm²	3x3, 8x8, 16x16	3x3, 8x8, 16x16	3x3, 8x8, 16x16

TABLE 1-: Parameters used for FIGURE 2 comparison

throughput in die per hour, assuming each wafer exchange took 15 seconds (including WEP) and each panel exchange took 13 seconds. **FIGURE 1** compares the results for 8 mm X 8 mm die, including evaluation at two different doses (600 mj and 800 mj) and four different numbers of alignment points (4, 9, 16, and 18 points). In all cases, the panel process demonstrated approximately 2X (die per hour) throughput advantage over the wafer process. Predictably, increasing the dosage or the number of alignment points reduced the throughput for both wafer and panel processes. The decrease in throughput associated with increase in number of alignment points had an impact, for example, going from 9 to 16 points at the 600 mj dose reduced throughput by 8.8%.

Next, we estimated the cost-of-ownership for wafer and panel lithography processes, comparing three different wafer exposure systems (1X stepper, Rudolph 2X JetStep System for wafers, and Rudolph 2X JetStep System for panels). **Table 1** shows the parameters used for the comparison. **FIGURE 2** shows the relative cost per 100 die calculated for 8 mm X 8 mm die using 9 alignment points at 600 mj and 800 mj doses. At the 600 mj dose, cost per die decreased by approximately 18% for the JetStep wafer system and nearly 40% for the JetStep panel system, when compared to the 1X stepper. Similarly, at the 800 mj dose, cost per die decreased approximately 13% and 35%. We saw estimated cost savings of similar magnitude for smaller (3 mm X 3 mm) and larger (16 mm X 16 mm) die.

Summary

To summarize, moving from round wafers to rectangular panels ("panel-ization") saves corner space, delivering a roughly 10% improvement in surface utilization. The larger size of the substrate and the improved fit between the mask and substrate reduce the transfer overhead by a factor of 5. The potential reduction in throughput resulting from an increase in the number of alignment points is more than offset by the improvements in throughput. Compared to a 1X stepper on wafers, panel-based processes can reduce lithography cost per die by as much as 40%.

Clearly, there are many aspects of "panel-ization" that must be addressed before these processes gain broad acceptance. It is worth noting that panel lithography is not new. It is widely used in related industries, such as the manufacturing of flat panel displays and photovoltaic solar panels. The JetStep Panel System is built on technology that has over 40 lithography systems currently installed in these and similar applications. As this analysis demonstrates, the potential economic benefits of panel-based lithography are significant. The model discussed here evaluates relatively modest sized panels. Larger panels may offer even greater benefits. Clearly, the transition to panel-based processes for advanced packaging applications bears serious consideration. ◆

The impact on OPC and SRAF caused by EUV shadowing effect

FAN JIANG, *Mentor Graphics, Wilsonville, OR*

EUV's off-axis mask illumination introduces a special problem in EUV OPC – the shadowing effect.

While there is debate about when extreme ultraviolet lithography will be ready for production, there continues to be active research and development into making every part of an EUV system work, including optical proximity correction (OPC). That's right, there is no break from the pattern distortions seen in sub-wavelength lithography. In fact, EUV introduces significant new pattern-distorting effects. As EUV has developed over the last few years, the models for these new EUV-specific effects have also developed and improved. Now that pre-production EUV scanners are in foundries and being rigorously tested, tools to correct for EUV-specific optical effects are being fully integrated and tested. This article covers the impact on OPC caused by one of those new distortions, the EUV shadowing effect, and looks at a model-based solution for managing the shadowing effect. .

Scaling down to a wavelength of 13.5nm for EUV lithography requires dedicated optics, materials, and above all reflective reticles. An EUV optical system is built completely from reflective components (mirrors) because everything absorbs 13.5nm EUV wavelength. The reflective mask stack and off-axis mask illumination required with EUV induces new imaging effects, like mask shadowing, that need to be carefully captured through computational lithography. At the wafer level, the mask shadowing effect causes CD variation through the illumination scanner slit, with the amount of distortion depending on the orientation and position of the feature. Currently, the

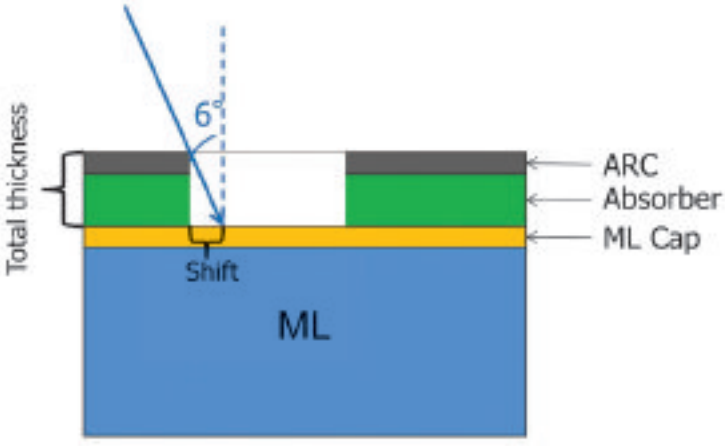

FIGURE 1. Image shift caused by the incident angle. The total thickness is a combination of the thickness of anti-reflect coating (ARC) and the thickness of absorber.

angle of incidence is 6° from normal with a changing azimuthal angle. This angle varies across the scanner's illumination slit and ranges from 67° to 123°.

This off-axis illumination causes a shadowing effect because the mask has a thickness, as illustrated in **FIGURE 1**. Theoretically, the shift of the image in this case can be written in terms of the total thickness and the incident angle: shift = total thickness x tan (6°).

In order to simulate this correctly, we need to use 3D mask simulation. What is more difficult is when we try to look at this issue through the scanner's illumination slit. We depict the position in the scanner slit as a combination of two parameters: radius, inter-

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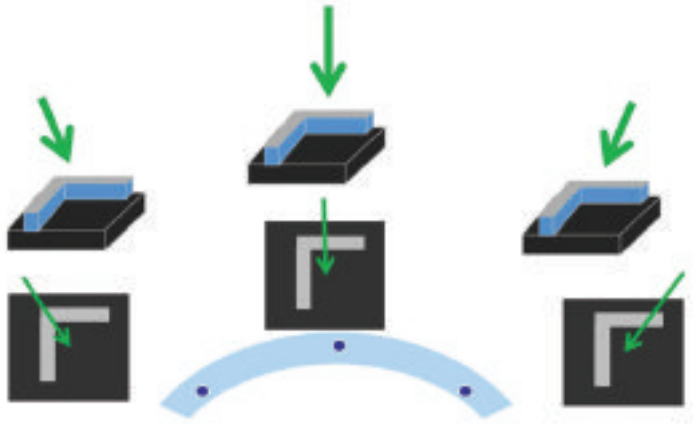

FIGURE 2. The impact from the incident varies through the scanner's illumination slit.

section of the optical axis with the mask plane, and the azimuthal angle Ø, varying from 66° to 114°, where Ø=90° corresponds to the slit center. At the slit center, vertical oriented lines are not subjected to the mask shadowing effect. Horizontal oriented lines, which are perpendicular to the plane of incidence, fully capture the mask shadowing effect. **FIGURE 2** shows that as the azimuthal angle changes through slit, the impact on the mask varies.

To evaluate topology-aware mask modeling for EUV imaging, we collected a large set of wafer CD data and compared the data to simulation data. **FIGURE 3A** shows the error between the wafer data and the simulation data without shadowing effect considered for different patterns. The simulation only uses 3D mask calculation at the center of the slit, so there is no simulation of the shadowing effect at the other slit locations. The result shows a parabola trend through slit, which is caused by the change of azimuthal angle.

We used 90° as the azimuthal angle in the 3D mask calculation. This is the correct azimuthal angle at the center of the slit. So the simulation data matches wafer CD data best at the center. When the azimuthal changes from 90°, the 3D mask calculation becomes less and less accurate. So the error gets bigger towards the edge. Error is calculated as measurement minus simulation, so the negative numbers shown in **FIGURE 3** mean that the simulation gave a larger number than did the wafer CD. The data in **FIGURE 3a** does not capture the through-slit shadowing effect, only the center effect. To have a correct simulation result, we have to add the through-slit shadowing effect into our model. We used a rule-based bias table to include it. The rule-based bias table could come from the following formulas, using the incident angle/azimuthal angle and the thickness of the mask:

$$H = h\tan\theta\cos\varphi\,;\; V = h\tan\theta\sin\varphi$$

where h is the total thickness of the mask, Ø is the incident angle and ϕ is the azimuthal angle. The relation between azimuthal angle and the location in the scanner slit direction is:

$$\cos\varphi = \frac{R}{\sqrt{R^2+y^2}};\sin\varphi = \frac{y}{\sqrt{R^2+y^2}}$$

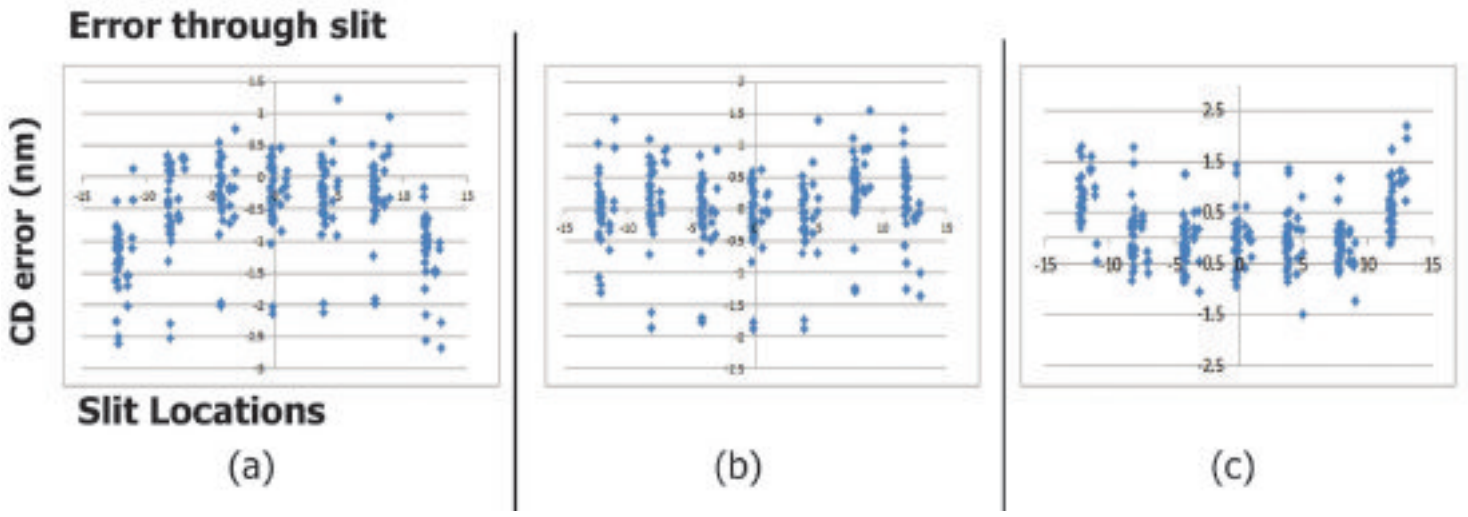

FIGURE 3. (a) CD error results of the simulation with shadowing effect considered at the slit center only, (b) using rule-based shadowing bias table, and (c) using a model-based method for through-slit shadowing effect.

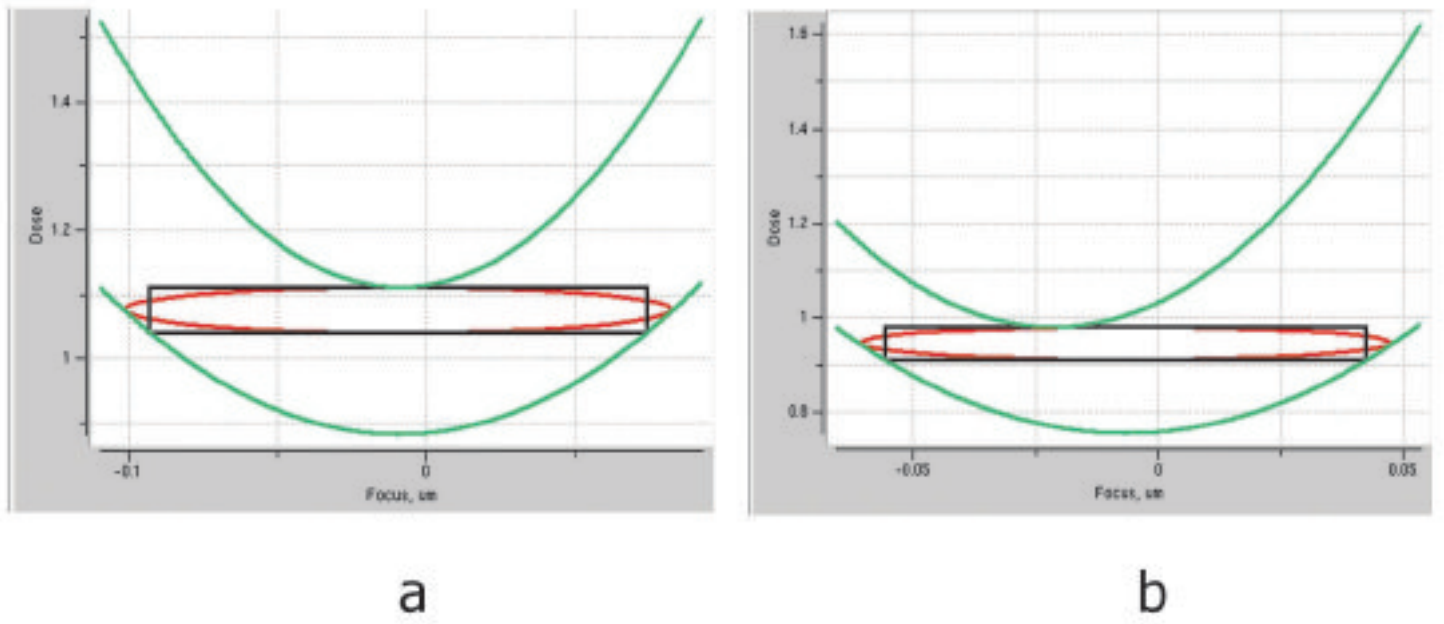

FIGURE 4. Process windows of asymmetric SRAF placement (a) and symmetric SRAF placement (b).

where R is the radius of the illumination slit, and y is the location. These equations link the location and bias together, and serve as a guideline for generating a bias table for the ideal theoretical shadowing effect. Sometimes the shadowing effect is not the only through-slit change we want to consider. For example, the aberration and the illumination may also change. When you have a set of experiment data at several slit locations, without any shadowing effect compensation, you could measure the difference between the wafer data and the target. This difference gives a bias table for through-slit change that includes shadowing bias change and also aberration and illumination change.

In the data shown in **FIGURE 3b**, the bias table comes directly from experiment data rather than theoretical formulas, which includes all the through-slit changes. When we applied this bias table in our simulation, we re-calculate the CD error.

We see in **FIGURE 3b** that at each slit location, the average errors between simulation and measured CD are significant decreased compared to the results in Figure a, However, the RMS error calculated from the data points in **FIGURE 3b** does not improve. This is because the shadowing effect seen varies between different patterns. The rule-based bias table considers the change through slit, but it considers the change for all different patterns the same. However, the change through slit is pattern dependent. To get a more accurate simulation result, we need to use model-based method to predict and correct for the shadowing effect.

As an example, there are 7 slit locations in **FIGURES 3a** and **3b**. If we use 3D mask modeling at all these locations, we should be able to calculate the shadowing effect correctly. The CD error result when using a model-based method instead of a rule-based bias table is shown in **FIGURE 3c**.

Comparing the RMS error calculated from the data in **FIGURE 3b** and **FIGURE 3c** at different slit locations, we see a significant benefit of using a model-based method for determining shadowing effect through slit.

These experiments showed us that in order to simulate shadowing effect with the most accuracy, model-based method may be necessary. Hence, when we talk about compensating for shadowing effect, we could use either a rule-based bias table for faster computation time or a model-based method for better accuracy.

The asymmetric illumination of EUV lithography also causes another problem—asymmetry of the SRAF pattern. The first question is when do we

	Slit location 1	Slit location 2	Slit location 3	Slit location 4	Slit location 5	Slit location 6	Slit location 7
Rule-based	2.72	2.73	2.64	2.72	2.56	2.68	3.05
Model-based	0.49	0.55	0.51	0.49	0.53	0.46	0.56

TABLE 1: RMS error of simulation with rule-based and model-based method for shadowing effect.

need to use SRAF in EUV? You might recall a similar situation in KrF and ArF. SRAF was first used with the 130 nm technology node with KrF, and recently, with a 0.39 k1 factor. In ArF, we started to use SRAF for the 90 nm node, with 0.35 k1 factor. For the 7 nm process node, the half pitch is 16 nm and the k1 factor is 0.41. This k1 number is close enough to what it was in KrF and ArF when we introduced SRAF that we can consider using SFRAF in EUV lithography. The next question for using SRAF in EUV is how to place scattering bars. We made a simple example with an isolated contact in a 7 nm node wafer. By applying symmetric SRAF, we get the process window in **FIGURE 4a**, and the depth of focus (DOF) is 98 nm. Also, we moved the SRAF around and looked for the best setting for DOF. The best DOF we found in this case is 167 nm, shown in **FIGURE 4b**, accomplished by using a set of asymmetric SRAF. By comparing the two process windows, we see that the process window of symmetric SRAF placement is not symmetric, which decreases the DOF. We conclude from this that to obtain the best process window, asymmetric SRAF placement may be needed due to EUV's non-telecentric imaging system.

EUV's specific off-axis mask illumination introduces a special problem in EUV OPC – the shadowing effect. This effect can be adequately compensated for by using a rule-based bias table, which gives faster runtime than the model-based simulations. But because not all the patterns at the same location require the same bias value, the model-based (3D mask simulation) compensation has a better prediction of the shadowing effect, and therefore gives a more accurate repair of shadowing errors. Finally, we found the best SFRAF placement is also asymmetric, as judged by DOF, because of the asymmetric nature of the incident angle. The shadow modeling results were verified on the pre-production ASML NXE:3100 EUV lithography tool. As EUV gets closer to production use, the OPC tools needed to correct for EUV-specific patterning effects are well developed, integrated, and tested. ◆

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Is it time for a roadmap for equipment and materials?

Hopefully everyone is familiar with the International Technology Roadmap for Semiconductors (ITRS). It was launched in 1992, when the Semiconductor Industry Association (SIA) coordinated the first efforts of producing what was originally The National Technology Roadmap for Semiconductors (NTRS). This roadmap of requirements and possible solutions was generated three times in 1992, 1994, and 1997. The NTRS provided a 15-year outlook on the major trends of the semiconductor industry. As such, it was a good reference document for semiconductor manufacturers, suppliers of equipment, materials, and software and provided clear targets for researchers in the outer years.

When the semiconductor industry became increasingly global, the realization that a Roadmap would provide guidance for the whole industry and would benefit from inputs from all regions of the world led to the creation of the International Technology Roadmap for Semiconductors (ITRS).

Much has been written about the ITRS, which is perhaps the best roadmapping effort of all time in any industry. In fact, I stumbled across a dissertation titled "Technological Innovation in the Semiconductor Industry: A Case Study of the International Technology Roadmap for Semiconductors (ITRS)" written by Robert R. Schaller in his pursuit of a degree in philosophy at George Mason University. Robert did a great job analyzing the importance of the roadmap and includes anecdotes such as a short-lived attempt at AMD to create an internal roadmap, and how the ITRS relates to the roadmap to peace in the Middle East.

While the latest updates and revisions of the ITRS usually come out around this time of year, the organizers tell me that it will be in the spring of 2014 for the latest edition (which will be a full revision vs an update, which alternate every year).

A key aspect of the ITRS is that they go out of the way to NOT try to pick "winners and losers" as I've heard it called. It is clearly stated that: "The ITRS is devised and intended for technology assessment only and is without regard to any commercial considerations pertaining to individual products or equipment".

That's all well and good I suppose, and there is plenty of information that a savvy supplier can pull from the Roadmap about what technology is needed and what the market demand might look like. But it's time to take it to the next step.

> It's time to think about creating a roadmap for equipment and materials companies, and their suppliers

It's time to think about creating a roadmap for equipment and materials companies, and their suppliers (i.e., suppliers of critical components and subsystems and raw materials). I recently had a conversation on exactly this topic with Gopal Rao, SEMATECH's senior director of business development. Prior to joining SEMATECH, Rao served as director of Manufacturing Research at Intel, where he led a strategic portfolio of advanced manufacturing projects in partnership with universities and national labs. A 24-year veteran of Intel, Rao progressed through a variety of assignments in senior engineering and management roles.

Gopal attended The ConFab 2013 as a representative of Intel, and said he found the private meeting with suppliers quite useful. What he proposes we do in 2014 was at least introduced the concept of a roadmap for equipment and materials suppliers, perhaps in a panel session, and suggest it be a common thread in the private meetings between sponsors (suppliers) and VIPs (delegates from IC manufacturing companies). We had more than 170 such meetings in 2013. At the end of the conference, we'll come up with a list of 4 or 5 "action items" for the industry to address.

In response to a blog I posted on this topic, Dalia Vernikovsky of Applied Seals North America (ASNA) said that such a roadmap was long overdue to "address and resolve critical areas of lack of controls and contamination sources that will be vital to assuring positive results in the type of technology that our present manufacturing is already seeing as problem areas."

The ConFab 2014, by the way, will be held June 22-25 at The Encore at The Wynn in Las Vegas. Don't miss it!

PETE SINGER
Editor-in-Chief

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