Solstice is a trademark of ClassOne Technology

# TELL ME: WHY SHOULD I PAY TWICE THE PRICE FOR A NEW PLATING TOOL?


Solstice S8 for cassette-to-cassette automated plating

## CLASSONE SOLSTICE – IT DOES EVERYTHING I NEED FOR HALF THE BIG GUYS' PRICE!

### Finally, advanced plating for the rest of us...

We all know the Big Guys focus on selling expensive, bleeding-edge tools to the largest users. What about the rest of us who still need to get the job done right within a reasonable budget? ClassOne has great solutions at half the price.

ClassOne's Solstice™ plating tools are designed specifically for users who run 200mm or smaller wafers – but still need advanced performance on substrates like silicon, glass, SiC, GaAs and sapphire. With options for single or multiple metals on the same tool, Solstice is the smart choice for technologies such as TSV, WLP, MEMS or RF.

### Quality plus performance – without the big price tag

Solstice quality begins inside, using top brand components throughout, like Gemu valves, Levitronix pumps and Genmark robots. Solstice is designed and built by industry veterans with literally hundreds of years of combined experience. So the focus is always on consistent superior performance. Such as uniformities of ≤3% on films from thick to thin!


Solstice LT for plating development

### Solstice is taking off!

It started last SEMICON West when our first Solstice was literally sold off the show floor! And ever since, there's been a non-stop stream of requests for demos, with orders now coming in as fast as we can manufacture.

So, call now to set up a demo and see this Solstice phenomenon for yourself. It truly is "advanced plating for the rest of us!" Call: (406) 755-2200. Or email: info@classone.com.

ClassOne TECHNOLOGY

*Advanced Plating For the Rest of Us*

**www.ClassOne.com • SEMICON China, Booth 5259**

SEMICONDUCTORS • PACKAGING • MEMS • LEDS • DISPLAYS JANUARY 2015

# Solid State TECHNOLOGY

Insights for Electronics Manufacturing



## 2015 Outlook: Entering the 3D Era

P. 15

Extension MEDIA

www.solid-state.com


Satisfying the semiconductor industry's simultaneous demands for performance enhancement and cost reduction requires endless innovation.

Nikon leverages proven immersion technology to deliver comprehensive solutions that extend ArF lithography and enable next-generation manufacturing.

Nikon. Innovation Never Stops.

See Nikon at:

LithoVision 2015 ‹and› SPIE. ADVANCED LITHOGRAPHY

www.lithovision.com

www.nikonprecision.com

Solid State TECHNOLOGY®

JANUARY 2015 VOL. 58 NO.1

On the cover: ASML's NXE:3100 scanner in imec's 300mm cleanroom. Copyright imec.

COVER

## FEATURES



## COLUMNS



## DEPARTMENTS

editorial

# Reframing the Roadmap: ITRS 2.0

The International Technology Roadmap for Semiconductor (ITRS) is being reframed to focus more on end applications, such as smartphones and micro-servers. Labeled ITRS 2.0, the new roadmap is a departure from a strong focus maintaining the path defined by Moore's Law. The original ITRS was published in 1992 at the National Technology Roadmap for Semiconductors; it became the ITRS in 1998.

In an IEEE paper published late last year titled "ITRS 2.0: Toward a Re-Framing of the Semiconductor Technology Roadmap," the roadmappers explain why it's time for a change. "As new requirements from applications such as data center, mobility, and context-aware computing emerge, the existing roadmapping methodology is unable to capture the entire evolution of the current semiconductor industry. Today, comprehending how key markets and applications drive the process, design and integration technology roadmap requires new system-level studies along with chip-level studies."

The ITRS roadmapping committee has already been reorganized to focus on ITRS 2.0. There are now six groups focused on what ITRS chairman Gargini calls the "building blocks."

- **System Integration**—studies and recommends system architectures to meet the needs of the industry. It prescribes ways of assembling heterogeneous building blocks into coherent systems.
- **Outside System Connectivity**—refers to physical and wireless technologies that connect different parts of systems.
- **Heterogeneous Integration**—refers to the integration of separately manufactured technologies that in the aggregate provide enhanced functionality.
- **Heterogeneous Components** —describes devices that do not necessarily scale according to "Moore's Law," and provide additional functionalities, such as power generation and management, or sensing and actuating.
- **Beyond CMOS**—describes devices, focused on new physical states, which provide functional scaling substantially beyond CMOS, such as spin-based devices, ferromagnetic logic, and atomic switch.
- **More Moore**—refers to the continued shrinking of horizontal and vertical physical feature sizes to reduce cost and improve performance.
- **Factory Integration** consists of tools and processes necessary to produce items at affordable cost in high volume.

A revised ITRS was not released at the end of 2014, as has historically been the case. Gargini said the groups have been preparing white papers which should be released early this year. We'll be publishing summaries in Solid State Technology, so stay tuned.

**—Pete Singer,** Editor-in-Chief


Solid State TECHNOLOGY

**Pete Singer,** Editor-in-Chief
Ph: 978.470.1806,
psinger@extensionmedia.com

**Shannon Davis,** Editor, Digital Media
Ph: 603.547.5309
sdavis@extensionmedia.com

**Ed Korczynski,** Senior Technical Editor,
edk@extensionmedia.com

**Jeff Dorsch,** Contributing Editor

**Phil Garrou,** Contributing Editor

**Dick James,** Contributing Editor

**Vivek Bakshi,** Contributing Editor

**Sara Ver-Bruggen,** Contributing Editor,
Semiconductor Manufacturing & Design

**CREATIVE/PRODUCTION/ONLINE**

**Spryte Heithecker,** Production Manager

**Yishian Yao,** Media Coordinator

**Nicky Jacobson,** Senior Graphic Designer

**Caldin Seides,** Graphic Designer

**Slava Dotsenko,** Senior Web Developer

**MARKETING/CIRCULATION**

**Jenna Johnson,**
jjohnson@extensionmedia.com

**CORPORATE OFFICERS**

Extension Media, LLC
**Vince Ridley,** President and Publisher
vridley@extensionmedia.com

**Clair Bright,** Vice President and Publisher
Embedded Electronics Media Group
cbright@extensionmedia.com

**Melissa Sterling,** Vice President,
Business Development
msterling@extensionmedia.com

**For subscription inquiries:**
Tel: 847.559.7500; Fax: 847.291.4816;
Customer Service e-mail: sst@omeda.com;
Subscribe: www.sst-subscribe.com

January 2015, Volume 58, Number 1 • ***Solid State Technology*** ©2015 (ISSN 0038-111X) **Subscriptions:** Domestic: one year: $258.00, two years: $413.00; one year Canada/Mexico: $360.00, two years: $573.00; one-year international airmail: $434.00, two years: $691.00; Single copy price: $15.00 in the US, and $20.00 elsewhere. Digital distribution: $130.00. You will continue to receive your subscription free of charge. This fee is only for air mail delivery. Address correspondence regarding subscriptions (including change of address) to: *Solid State Technology, 1786 18th Street, San Francisco, CA 94107-2343.* (8 am – 5 pm, PST).

Solid State Technology is published eight times a year by Extension Media LLC, 1786 Street, San Francisco, CA 94107.



Extension MEDIA

1786 18th Street
San Francisco, CA 94107

# TAKE A LOOK!

Key Executives from these top companies are confirmed for The ConFab

| | | |
|---|---|---|
| AMD | GLOBALFOUNDRIES | On Semiconductor |
| Amkor | Hitech Semiconductor | Qualcomm |
| Applied Materials | IBM | Samsung |
| Atmel | IDT | Skyworks |
| Broadcom | Intel | TSI Semiconductors |
| Cree | KLA-Tencor | UMC |
| Flip Chip | Microchip | Plus many others! |
| Freescale | NVIDIA | |

The ConFab®

MAY 19-22, 2015
ENCORE AT THE WYNN
LAS VEGAS
www.theconfab.com

## SPACE IS LIMITED

**Make Plans Now to Join the Semiconductor Manufacturing Industry's Premier Conference & Networking Event**
**Visit www.theconfab.com today to learn more!**

Presented by: Solid State TECHNOLOGY®

www.theconfab.com

Owned and Produced by: Extension MEDIA

# online@ www.solid-state.com

## Web Exclusives

### Slideshow: IEDM 2014

Browse highlights from the IEEE International Electron Device Meeting in San Francisco. The conference scope not only encompassed devices in silicon, compound and organic semiconductors, but also in emerging material systems.

**http://bit.ly/1yYeQHh**

### RTI ASIP Conference: 3D Memory, Heterogeneous Integration, High Density Laminates, Embedded films

Dr. Phil Garrou continues his end of year look at presentations at the RTI ASIP Conference.

**http://bit.ly/1EMSSu7**

### Exponentially rising costs will bring changes

Scott McGregor, President and CEO of Broadcom, sees some major changes for the semiconductor industry moving forward, brought about by rising design and manufacturing costs. Speaking at the SEMI Industry Strategy Symposium (ISS) in January, McGregor said the cost per transistor was rising after the 28nm, which he described as "one of the most significant challenges we as an industry have faced."

**http://bit.ly/1LcQykI**

### IEDM 2014: Thanks for the MEMS-ories

Getting less attention at IEDM 2014 were the papers on sensors, microelectromechanical systems (MEMS) devices and bio-MEMS. This technology generates fewer headlines, although it is present in smartphones, fitness trackers, and many other electronic products. (From SemiMD)

**http://bit.ly/1xqiHjc**

### Ferromagnetic room temperature switching

A research team led by folks at Cornel University (along with University of California, Berkeley; Tsinghua University; and Swiss Federal Institute of Technology in Zurich) have discovered how to make a single-phase multiferroic switch out of bismuth ferrite (BiFeO3). (From SemiMD)

**http://bit.ly/1udl5Ur**

## n&b news and blogs

### Wearable Devices and the Search for the Holy Grail at 2015 International CES

2015 has already been heralded as the year of the wearable device and MEMS Industry Group chose wearables and the MEMS/sensors supply chain as the theme for their conference.

**http://bit.ly/1KR5Hl3**

### IEDM 2014: Monday was FinFET Day

Chipworks' Dick James anticipated that the third session on Monday at IEDM 2014 was going to be hot, with three FinFET papers by TSMC, Intel, and IBM – and he was right.

**http://bit.ly/1v8YoRl**

### Insights from the Leading Edge: Georgia Tech Interposer Workshop

Dr. Phil Garrou continues his look at the GaTech Global Interposer Workshop in his most recent blog post.

**http://bit.ly/1xb61bf**

### DRAM capacity rises from slump; Sector faces new challenges

SEMI announced details from the SEMI World Fab Forecast Report illuminating the state of the semiconductor manufacturing industry. Among the insights across the various segments, the changes in the DRAM segment are an example of the significant shifts in capacity and technology that are driving fab capacity and investment.

**http://bit.ly/1xifhZY**

# SEMICON® China2015

without limits.

**March 17-19, 2015 SNIEC, Shanghai, China**

## Why you should attend SEMICON China 2015

- The largest semiconductor industry trade and technology event, covering the complete IC manufacturing supply chain
- More than 10 theme pavilions and more than 30 concurrent technology and business forums addressing the latest technical trends and market developments
- Packaging trends and topics addressed in the Advanced Packaging Forum and China Semiconductor Technology International Conference (CSTIC 2015)
- High-level networking events, including the SEMICON China Gala Dinner, IC Night, networking luncheon, and golf tournament

## Grand Opening Keynote

**Tzu-Yin Chiu**
Chief Executive Officer & Executive Director,SMIC

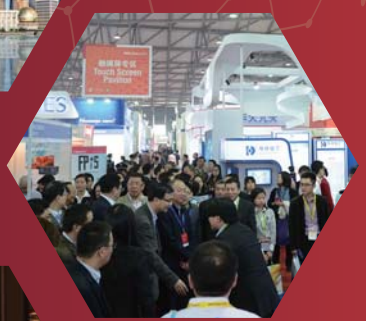
**Wang Xin Chao**
Chairman & CEO, JCET

**Tetsuro (Terry) Higashi**
Chairman of the Board, Tokyo Electron Limited

**Simon Yang**
President, CEO, XMC

**Michael Hurlston**
Executive Vice President, Worldwide Sales,Broadcom

**Jack Qi Shu**
VP, HLMC



**Earily bird for sweet gift**
*Scan and register on mobilephone*

*Visit and register on PC*
*http://223.4.179.170/semi2015/*

semi™

www.semiconchina.org

*Please send news articles to sdavis@extensionmedia.com*

# news

## worldnews

***USA*** | **Mentor Graphics** announced it has acquired Flexras Technologies.

***USA*** | **GLOBALFOUNDRIES** and **Linear Dimensions** announced a partnership to offer joint analog solutions for wearables and MEMS sensor markets.

***ASIA*** | **Samsung Electronics** has begun mass producing the industry's first 8 gigabit (Gb) GDDR5 DRAM, based on the company's leading-edge 20nm process technology.

***EUROPE*** | **imec** demonstrated broadband graphene optical modulator on silicon at IEDM 2014.

***USA*** | **Amkor Technology** licensed its copper pillar bump technology to **GLOBALFOUNDRIES**.

***EUROPE*** | **Holst Centre** and **imec** have realized a thin-film hybrid oxide-organic microprocessor.

***ASIA*** | **TSMC** held its 14th annual Supply Chain Management Forum and recognized nine outstanding suppliers.

***EUROPE*** | **Soitec** and **CEA-Leti** announced a new world record for solar efficiency at 46%.

***USA*** | **Murata Electronics North America** completed its acquisition of Peregrine Semiconductor Corporation.

***USA*** | Two companies were honored with the 2014 SEMI Award for North America at ISS 2015: **Brewer Science** and **Advanced Semiconductor Engineering Inc. (ASE)**.

## Global semiconductor market set for strongest growth in four years in 2014

Worldwide semiconductor market revenue is on track to achieve a 9.4 percent expansion this year, with broad-based growth across multiple chip segments driving the best industry performance since 2010.

Global revenue in 2014 is expected to total $353.2 billion, up from $322.8 billion in 2013, according to a preliminary estimate from IHS Technology (NYSE: IHS). The nearly double-digit-percentage increase follows respectable growth of 6.4 percent in 2013, a decline of more than 2.0 percent in 2012 and a marginal increase of 1.0 percent in 2011. The performance in 2014 represents the highest rate of annual growth since the 33 percent boom of 2010.

"This is the healthiest the semiconductor business has been in many years, not only in light of the overall growth, but also because of the broad-based nature of the market expansion," said Dale Ford, vice president and chief analyst at IHS Technology. "While the upswing in 2013 was almost entirely driven by growth in a few specific memory

*Continued on page 6*

## What's next for MEMS?

*By Paula Doe, SEMI*

The proliferation of sensors into high volume consumer markets, and into the emerging Internet of Things, is driving the MEMS market to maturity, with a developed ecosystem to ease use and grow applications. But it is also bringing plenty of demands for new technologies, and changes in how companies will compete.

While the IoT may be all about sensors, it is not necessarily a bonanza for most traditional MEMS sensor makers. "The surprising winner turns to be optical MEMS for optical cross connect for the data center, where big growth is coming," said Jérémie Bouchaud, IHS Director and Sr. Principal Analyst, MEMS & Sensors, at the recent MEMS Industry Group (MIG) "MEMS Executive Congress" held in Scottsdale, Arizona from November 5-7.

The market for wearables will also see fast growth for the next five years, largely for smart watches, driving demand for motion sensors, health sensors, sensor hubs and software –but even in 2019 the market for sensors in wearables will remain <5% the size of the phone/tablet market, IHS predicts. The greater IoT market may reach billions of other connected devices in the next decade, but sensor demand will be very fragmented and very commoditized. Smart homes may use 20 million sensors in 2018, but many other industrial applications will probably each use only 100,000 to 2-3 million sensors a year, Bouchaud noted.

*Continued on page 10*

# Semiconductor equipment sales forecast: $38B in 2014 to nearly $44B in 2015

SEMI projects that worldwide sales of new semiconductor manufacturing equipment will increase 19.3 percent to $38.0 billion in 2014, according to the SEMI Year-end Forecast, released today at the annual SEMICON Japan exposition. In 2015, strong positive growth is expected to continue, resulting in a global market increase of 15.2 percent before moderating in 2016.

The SEMI Year-end Forecast predicts that wafer processing equipment, the largest product segment by dollar value, is anticipated to increase 17.8 percent in 2014 to total $29.9 billion. The forecast predicts that the market for assembly and packaging equipment will increase by 30.6 percent to $3.0 billion in 2014. The market for semiconductor test equipment is forecast to increase by 26.5 percent, reaching $3.4 billion this year. The "Other Front End" category (fab facilities, mask/reticle, and wafer manufacturing equipment) is expected to increase 14.8 percent in 2014.

For 2014, Taiwan, North America, and South Korea remain the largest spending regions. In terms of percentage growth, SEMI forecasts that in 2015, Europe will reach equipment sales of $3.9 billion (47.9 percent increase over 2014), Taiwan will reach $12.3 billion (28.1 percent increase), and South Korea sales

*Continued on page 8*

*Continued from page 4*

segments, the rise in 2014 is built on a widespread increase in demand for a variety of different types of chips. Because of this, nearly all semiconductor suppliers can enjoy good cheer as they enter the 2014 holiday season."

More information on this topic can be found in the latest release of the Competitive Landscaping Tool from the Semiconductors & Components service at IHS.

## Widespread growth

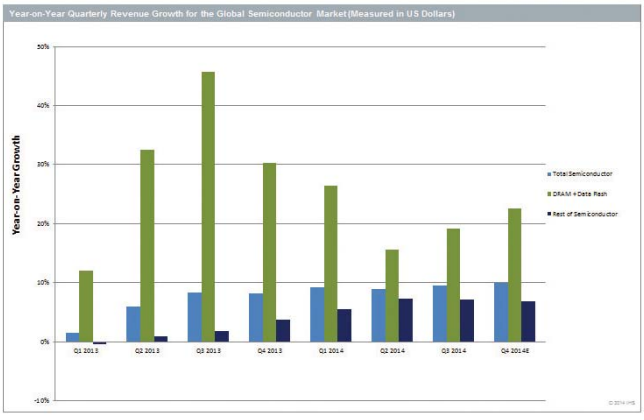
Of the 28 key sub-segments of the semiconductor market tracked by IHS, 22 are expected to expand in 2014. In contrast, only 12 sub-segments of the semiconductor industry grew in 2013.

Last year, the key drivers of the growth of the semiconductor market were dynamic random access memory (DRAM) and data flash memory. These two memory segments together grew by more than 30 percent while the rest of the market only expanded by 1.5 percent.

This year, the combined revenue for DRAM and data flash memory is projected to rise about 20 percent. However, growth in the rest of the market will swell by 6.7 percent to support the overall market increase of 9.4 percent.

In 2013, only eight semiconductor sub-segments grew by 5 percent or more and only three achieved double-digit growth. In 2014, over half of all the sub-segments—i.e., 15—will grow by more than 5 percent and eight markets will grow by double-digit percentages.

This pervasive growth is delivering general benefits to semiconductor suppliers, with 70 percent of chipmakers expected to enjoy revenue growth this year, up from 53 percent in 2013.




The figure presents the growth of the DRAM and data flash segments compared to the rest of the semiconductor market in 2013 and 2014.

## Semiconductor successes

The two market segments enjoying the strongest and most consistent growth in the last two years are DRAM and light-emitting diodes (LEDs). DRAM revenue will climb 33 percent for two years in a row in 2013 and 2014. This follows often strong declines in DRAM revenue in five of the last six years.

The LED market is expected to grow by more than 11 percent in 2014. This continues an unbroken period of growth for LED revenues stretching back at least 13 years.

Major turnarounds are occurring in the analog, discrete and microprocessor markets as they will swing from declines to strong growth in every sub-segment. Most segments will see their growth improve by more than 10 percent, compared to the declines experienced in 2013.

Furthermore, programmable logic device (PLD) and digital signal processor (DSP) application-specific integrated circuits (ASICs) will experience dramatic improvements in growth. PLD revenue in 2014 will grow by 10.2 percent compared to 2.1 percent in 2013, and DSP ASICs will rise by 3.8 percent compared to a 31.9 percent collapse in 2013.

## Moving on up

Among the top 20 semiconductor suppliers, MediaTek and Avago Technologies attained the largest revenue growth and rise in the rankings in 2014. Both companies benefited from significant acquisitions.

MediaTek is expected to jump up five places to the 10th rank and become the first semiconductor company headquartered in Taiwan to break into the Top 10. Avago Technologies is projected to jump up eight positions in the rankings to No. 15.

The strongest growth by a semiconductor company based purely on organic revenue increase is expected to be achieved by SK Hynix, with projected growth of nearly 23 percent.

No. 13-ranked Infineon has announced its plan to acquire International Rectifier. If that acquisition is finalized in 2014 the combined companies would jump to No. 10 in the overall

rankings and enjoy 16 percent combined growth.

Semiconductor revenue in 2014 will grow in five of the six major semiconductor application end markets, i.e. data processing, wired communications, wireless communications, automotive electronics and industrial electronics. The only market segment experiencing a decline will be consumer electronics. Revenue will expand by double-digit percentages in four of the six markets.

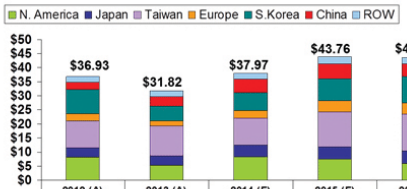
Japan continues to struggle, and is the only worldwide region that will see a decline in semiconductor revenues this year. The other three geographies—Asia-Pacific, the Americas and the Europe, Middle East and Africa (EMEA) region—will see healthy growth. The world will be led by led by Asia-Pacific which will post an expected revenue increase of 12.5 percent.

*Continued from page 7*

will hit $8.0 billion (25.0 percent increase).

The following results are given in terms of market size in billions of U.S. dollars:

SEMI® 2014 Year-End Equipment Forecast by Market Region




| | 2012 (A) | 2013 (A) | 2014 (F) | 2015 (F) | 2016 (F) |
|---|---|---|---|---|---|
| ROW | 2.10 | 2.08 | 2.17 | 2.44 | 2.35 |
| China | 2.50 | 3.38 | 4.66 | 5.14 | 4.62 |
| S.Korea | 8.67 | 5.22 | 6.41 | 8.01 | 9.11 |
| Europe | 2.55 | 1.92 | 2.65 | 3.92 | 4.25 |
| Taiwan | 9.53 | 10.57 | 9.63 | 12.34 | 12.83 |
| Japan | 3.42 | 3.38 | 4.14 | 4.41 | 4.71 |
| N. America | 8.15 | 5.27 | 8.31 | 7.50 | 5.81 |

***Source: SEMI; December 2014*** *Totals may not add due to rounding*

*Continued from page 6*

And most of this sensor market will be non-MEMS sensors, some mature and some emerging, including light sensors, fingerprint sensors, pulse sensors, gas sensors, and thermal sensors, all requiring different and varied manufacturing technologies. Much of the new sensor demand from automotive will be also be for non-MEMS radar and cameras, though they will also add MEMS for higher performance gyros, lidar and microbolometers, according to IHS. Expect major MEMS makers to diversify into more of these other types of sensors.

Yole Développement CEO Jean Christophe Eloy looked at how the value in the IoT would develop. While the emerging IoT market is initially primarily a hardware market, with hardware sales climbing healthily for the next five years or so, it will quickly become primarily a software and services market. In five to six years hardware sales will level off, and the majority of the value will shift to data processing and value added services. This information service market will continue to soar, to account for 75% of the $400 Billion IoT market by 2024.

## Re-thinking the business models?

The IoT will bring big changes to the electronics industry, from new technologies to new business models, and new leaders, suggested George Liu, TSMC Director of Corporate Development. He of course also argued that the high volume and low costs required for connected objects would drive sensor production to high volume foundries, and drive more integration with CMOS for smart distributed processing at CMOS makers.

Liu projected these changes would mean a new set of companies would come out on top. Few leading system makers managed to successfully transition from the PC era to the mobile handset era, or from the mobile handset era to the smart phone era, as both the key technologies and the winning business models changed, and chip makers faced disruption as well. "For one thing, the business model changed from making everything in house to making nothing," he noted. "The challenge is to focus on where one is most efficient."

"The odds of Apple or Google being the dominant players in the next paradigm is zero," concurred Chris Wasden, Executive Director, Sorenson Center for Discovery and Innovation at the University of Utah.

Lots of other things will have to change to enable the IoT as well. Liu projected that devices will need to operate at near threshold or even sub-threshold voltages, with "thinner" processing overhead, while the integration of more different functions will redefine the system-in-a-chip. Smaller and lower cost devices will require new materials and new architectures, new types of heterogenous integration and wafer-level packaging, and an ecosystem of standard open platforms to ease development. TSMC's own MEMS development kit has layout rules, but not yet behaviorial rules, always the more challenging issue for these mechanical structures. "That's the next big thing for us," he asserted. "These huge gaps mean huge opportunities."

## IDMs and systems companies still likely to dominate

Still, the wide variety, and sometimes tricky mechanics and low volumes, of many MEMS devices have been a challenge for the volume foundries. The fabless MEMS model has seen only limited success so far and is unlikely to see much in the next decade either, countered Jean Christophe Eloy, CEO of Yole Développement, who pointed out that some 75% of the MEMS business is dominated by the four big IDMs who can drive costs down with volumes and diversified product lines. To date, only two fabless companies—InvenSense and Knowles—are among the top 30 MEMS suppliers.

Most of the rest of the top 30 are system makers with their own fabs, making their own MEMS devices to enable higher value system products of their own, which is likely to continue to remain a successful approach, as the opportunities for adding value increasingly come from software, processers, and systems. "MEMS value has always been at the system level," noted Eloy.

GE's recent introduction of an improved MEMS RF switch to significantly reduce the size and cost of its MRI systems is one compelling example, with the potential of the little MEMS component to greatly extend the use of this high-contrast soft-tissue imaging technology. Though the company sold off its general advanced sensors unit last year to connector maker Amphenol Corp., it is still making its unique RF switch using a special alloy in house in small volumes as a key enabler of its high value MRI systems. These imagers work by aligning the spin of hydrogen nuclei with a strong magnet, tipping them off axis with a strong RF pulse from an antenna, then measuring how they snap back into alignment with lots of localized antennas with low power RF switches close to the body. "We're now launching a new receive chain using MEMS RF switches," reported Tim Nustad, GM and CTO, Global Magnetic Resonance, GE Healthcare.

"Later we can see a flexible, light weight MRI blanket."

### Opportunity for smaller, lower power, lower cost technologies

So far, MEMS makers have driven down the cost of devices by continually shrinking the size of the die. But that may be about to change, as the mechanical moving structures have about reached the limit of how much smaller they can get and still produce the needed quality signal. That's opening the door for a new generation of devices using different sensing structures and different manufacturing processes. For inertial sensors, options include bulk acoustic wave sensing from Qualtre, piezoresistive nanowires from Tronics and CEA/Leti, and even extrapolating gyroscope-like data with software from accelerometers and magnetometers. MCube's virtual gyro with this approach, now in production with some design wins, claims to save 80% of the power and 50% of the cost of a conventional MEMS gyro.

Piezoelectric sensing, often with PZT films, is also drawing attention, with products in development for timing devices and microphones. Sand9 claims lower noise and lower power for its piezoelectric MEMS timing, now starting volume manufacturing for Intel and others for shipments in 1Q15. It has also recently received a patent for piezo microphone, while startup Vesper (formerly known as Baker-Calling and then Sonify) also reports working with a major customer for its piezoelectric MEMS microphone.

### More open platforms ease development of new applications of established devices

The maturing ecosystem of open development platforms across the value chain is helping to ease commercialization of new applications. The two latest developments in this infrastructure are a standard interface to connect all kinds of different sensors to the controller, and an open library of basic sensor processing software. The MIPI Alliance

*Continued on page 12*

*Continued from page 11*

brought together major users and suppliers—ranging across STMicroelectronics and InvenSense, to AMD and Intel, to Broadcom and Qualcomm, to Cadence and Mentor Graphics—to agree on an interface specification to make it easier for system designers to connect and manage a wide range of sensors from multiple suppliers while minimizing power consumption of the microcontroller. Meanwhile, sensor makers and researchers are making a selection of baseline algorithms available for open use to ease development of new products. Offerings include Freescale's inertial sensor fusion and PNI Sensors' heart rate monitoring algorithms, along with other contributions from Analog Devices, Kionix, NIST, UC Berkeley and Carnegie Mellon to start. The material will be available through the MIG website.

Plenty of companies have also introduced their own individual platforms to ease customer development tasks as well, ranging from MEMS foundries' inertial sensor manufacturing platforms to processor makers' development boards and kits. Recently STMicroelectronics also adding its sensor fusion and other software blocks to its development platform.

KegData is one example of a company making use of these platforms to enable development of a solution for a niche problem – an automated system for telling pub owners how much beer is left in their kegs, using a Freescale pressure sensor and development tools. Currently the only way to know when a beer keg is empty is to go lift and weigh or shake it, a problem for efficiently managing expensive refrigerated inventory. Adding a pressure sensor in the coupler on top of the keg allows the height of the beer to be measured by the differential pressure between the liquid and the gas above it. The sensor then sends the information to a hub controller that communicates with the internet, letting the pub manager know to order more, or even automatically placing the order directly with the distributor. The startup's business model is to give the system to distributors for free, but sell them the service of automating inventory management for their customers, saving them the significant expense of sending drivers around to shake the kegs and take pre-orders.

More broadly, MEMS microphones are poised to continue to find a wide range of new applications. IHS' Bouchaud pointed out that cars will soon each be using 12-14 MEMS microphone units, to listen for changes in different conditions, while home security applications will use them to detect security breaches from unusual patterns of sounds, from people in the house to dogs barking. Startup MoboSens says it converts its chemical water quality data into audio signals to feed it into the phone's mic port for better quality.

## Opportunities still for new types of MEMS devices

Growth will also continue to come from new MEMS devices that find additional ways to replace conventional mechanical parts with silicon. Eloy noted that MEMS autofocus units may finally be the next breakout device, as they have started shipping in the last few weeks, and aim at shipping for products in 2015. MEMS microspeakers are also making progress and could come soon. But ramping new devices to the high volumes demanded by consumer markets is particularly challenging. "The only way to enter the market is with new technology, but high volume consumer markets make entry very hard for new devices," he said. "The market is saturated, wins depend on production costs, and not everyone can keep up…. The last significant new device was the MEMS microphone, and that was ten years ago."

But innovative new MEMS technologies also continue to be developed for initial applications in higher margin industrial and biomedical fields. One interesting platform is the MEMS spectrometer from VTT Technical Research Center of Finland. This robust tunable interferometer essentially consists of an adjustable air gap between two mirrors, made of alternating ALD or LPCVD bands of materials with different defraction indexes, explained Anna Rissanen, VTT research team leader for MOEMS and bioMEMS instruments. The structure can be tuned by different voltages to filter particular bands of light, while a single-point detector, instead of the usual array, enables very small and low cost spectrometers or hyper spectral cameras. VTT spinout Spectral Engines is commercializing near-IR and mid-IR sensors aimed at detecting moisture, hydrocarbons and gases in industrial applications. Other programs have developed sensors for environmental analysis by flyover by nano satellites and UAVs, sensors for monitoring fuel quality to optimize energy use and prevent engine damage, and sensors that can diagnose melanoma from a scan of the skin.

Keep up with these changing manufacturing technology demands at upcoming MEMS events at SEMICON China 2015, SEMICON Russia 2015, SEMICON West 2015, and at the new European MEMS Summit planned for Milan in September.

# Thermal Performance of 3DICs

**Dr. Phil Garrou,**
Contributing Editor

3DICs are assumed to suffer from stronger thermal issues when compared to equivalent implementations in traditional single-die integration technologies. Based on this assumption, heat dissipation is frequently pointed as one of the remaining challenges in the promising 3D integration technology.

There are four main aspects differentiating heat dissipation in 3D ICs: chip footprint, die thickness, inter-die interface and TSVs.

Heat dissipation in small hotspots is primarily diffused through the high thermal conductive silicon substrate and spreads in a semi-spherical direction, rapidly decreasing the heat density and lowering the peak temperature. In case of thinned silicon dies in a 3D stack, the inter-die interface layer acts as a thermal barrier due to its poor thermal properties, forcing the heat to spread laterally in the silicon substrate and thus resulting in a temperature distribution which approximates a cylindrical shape.

Thinned silicon dies present reduced lateral heat spreading capacity while poorly conductive adhesive materials used to bond dies together contribute to increase the vertical thermal resistance.

An increase in power density may come from higher power dissipation and/or from a reduction of the chip footprint. It means either more power needs to be removed from the same package or that the same power dissipation has to go through a reduced chip footprint. While chip footprint reduction is one of the advantages of 3D integration, it usually leads to higher temperatures for the same amount of energy dissipation when compared to single-die implementations.

At the 2014 IEEE 3DIC Conference recently in Cork, Ireland, Leti and ST Micro presented two papers on the thermal performance of 3DICs.

Leti shows that inserting TSVs as thermal vias is of limited value. They contend that it is more important to reduce the thermal resistance between the stacked silicon dies which is due to poor thermally conductive layers such as BEOL metallization and underfill.

Thinned dies can present a severe thermal impediment especially to chips with hot spots. Thinned dies present high lateral thermal resistances thus forcing the heat to go through the underfill layer to the next die, which acts as a heat spreader reducing the hotspot temperature. Consequently, the thinner the die the more important is the thermal coupling between dies in case of hotspot heat dissipation.

The use of "thermal TSVs" for thermal mitigation has been routinely reported in the literature. Several thermal-aware physical optimization techniques can be found in the literature which rely on simplistic thermal models where the TSV is treated as a vertical lumped thermal resistor with thermal conductivity calculated according to its diameter and length. Such thermal models ignore the lateral heat transfer and the impact of the thin $SiO_2$ layer, which surrounds each TSV and thermally isolates TSVs from silicon substrate. The poor thermal conductivity properties of the $SiO_2$ dominate the thermal impact of the TSVs in case of hotspot dissipation. Thus while having TSVs in the silicon substrate increases the equivalent vertical thermal conductivity at the same time it causes a lateral thermal blockage effect, especially for fine TSV pitches.

Increasing the TSV density increases the vertical thermal conductivity as well as the lateral thermal blockage effect. Splitting large TSVs into smaller ones increases the ratio of the $Si_O2$ layer thickness to the TSV diameter and hence increases also the lateral thermal blockage effect. Considering TSV technologies with very fine pitch, where this ratio is typically 1:10, also lead to TSV arrays with higher lateral thermal blockage effect.

**Packaging**

# Solid doping for bulk FinFETs

**Ed Korczynski,** Sr. Technical Editor

In another example of the old one-liner that "all that is old is new again," the old technique of solid-source doping is being used by Intel for a critical process step in so-called "14nm node" finFET manufacturing. In the 7th presentation in the 3rd session of this year's IEDM, a late news paper written by 52 co-authors from Intel titled "A 14nm Logic Technology Featuring 2nd-Generation FinFET Transistors, Air-Gapped Interconnects, Self-Aligned Double Patterning and a 0.0588m2 SRAM Cell Size" disclosed that solid source doping was used under the fins.

As reported by Dick James of Chipworks in his blog coverage of IEDM this year, the fins have a more vertical profile compared to the prior "22nm node" and are merely 8nm wide (Figure 1). Since Intel is still using bulk silicon wafers instead of silicon-on-insulator (SOI), to prevent leakage through the substrate these 8nm fins required a new process to make punch-through stopper junctions, and the new sub-fin doping technique uses solid glass sources. Idsat is claimed to improve by 15% for NMOS and 41% for PMOS over the prior node, and Idlin by 30% for NMOS and 38% for PMOS.

Solid glass sources of boron (B) and phosphorous (P) dopants have been used for decades in the industry. In a typical application, a lithographically defined silicon-nitride hard-mask protects areas from a blanket deposition in a tube furnace of an amorphous layer containing the desired dopant. Additional annealing before stripping off the dopant layer allows for an additional degree of freedom in activating dopants and forming junctions.

In recent years, On Semiconductor published how solid-source doping on the sidewalls of Vertical DMOS transistors enable a highly phosphorous doped path for the drain current to be brought back to the silicon surface. The company shows that phosphorous-oxy-chloride (POCl) and phospho-silicate glass (PSG) sources can both be used to form heavily doped junctions 1-2 microns deep.

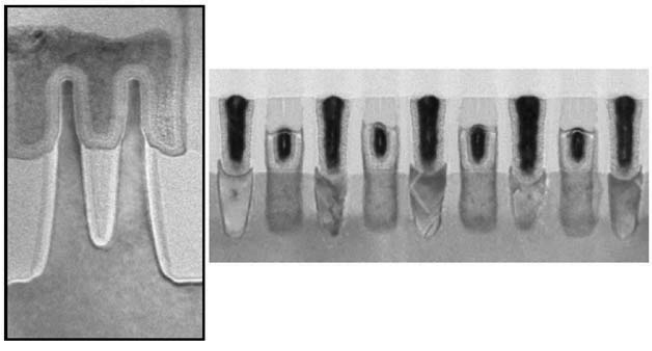


**FIGURE 1.** Intel Corp's "14nm node" finFETs show (in the left SEM) 8nm wide and 42nm high fins in cross-section, below which are located the punch-through stopper junctions. (Source: IEDM 2014, Late News 3.7).

The challenge for solid-source doping of 8nm wide silicon fins is how to scale processes that were developed for 1-2 microns to be able to form repeatable junctions 1-2 nm in scale. Self-aligned lithographic techniques could be used to mask the tops of fins, and various glass sources could be used. It is likely that ultra-fast annealing is needed to form stable ultra-shallow junctions.

Also seen at IEDM this year in the 7th presentation of the Advanced Process Modules section, Taiwanese researchers—National Nano Device Laboratories, National Chiao Tung University, and National Cheng Kung University—joined with Californian consultants—Current Scientific, Evans Analytical Group—to show "A Novel Junctionless FinFET Structure with Sub-5nm Shell Doping Profile by Molecular Monolayer Doping and Microwave Annealing." They claim an ideal subthreshold swing (~60 mV/dec) at a high doping level. Poly-Si n & p JLFinFETs (W/L=10/20 nm) with SDP experimentally exhibit superior gate control (Ion/Ioff >10E6) and improved device variation.

# 2015 outlook: Tech trends and drivers

*Leading industry experts provide their perspectives on what to expect in 2015. 3D devices and 3D integration, rising process complexity and "big data" are among the hot topics.*

## Entering the 3D era

**STEVE GHANAYEM**, *vice president, general manager, Transistor and Interconnect Group, Applied Materials*

This year, the semiconductor industry celebrates the 50th anniversary of Moore's Law. We are at the onset of the 3D era. We expect to see broad adoption of 3D FinFETs in logic and foundry. Investments in 3D NAND manufacturing are expanding as this technology takes hold. This historic 3D transformation impacting both logic and memory devices underscores the aggressive pace of technology innovation in the age of mobility. The benefits of going 3D — lower power consumption, increased processing performance, denser storage capacity and smaller form factors — are essential for the industry to enable new mobility, connectivity and Internet of Things applications.

The semiconductor equipment industry plays a major role in enabling this 3D transformation through new materials, capabilities and processes. Fabricating leading-edge 3D FinFET and NAND devices adds complexity in chip manufacturing that has soared with each node transition. The 3D structure poses unique challenges for deposition, etch, planarization, materials modification and selective processes to create a yielding device, requiring significant innovations in critical dimension control, structural integrity and interface preparation. As chips get smaller and more complex, variations accumulate while process tolerances shrink, eroding performance and yields. Chipmakers need cost-effective solutions to rapidly ramp device yield to maintain the cadence of Moore's Law. Given these challenges, 2015 will be the year when precision materials engineering technologies are put to the test to demonstrate high-volume manufacturing capabilities for 3D devices.

Achieving excellent device performance and yield for 3D devices demands equipment engineering expertise leveraging decades of knowledge to deliver the optimal system architecture with wide process window. Process technology innovation and new materials with atomic-scale precision are vital for transistor, interconnect and patterning applications. For instance, transistor fabrication requires precise control of fin width, limiting variation from etching to lithography. Contact formation requires precision metal film deposition and atomic-level interface control, critical to lowering contact resistance. In interconnect, new materials such as cobalt are needed to improve gap fill and reliability of narrow lines as density increases with each technology node. Looking forward, these precision materials engineering technologies will be the foundation for continued materials-enabled scaling for many years to come.

## Increasing process complexity and opportunities for innovation

**BRIAN TRAFAS**, *Chief Marketing Officer, KLA-Tencor Corporation*

The 2014 calendar year started with promise and optimism for the semiconductor industry, and it concluded with similar sentiments. While the concern of financial risk and industry consolidation interjects

itself at times to overshadow the industry, there is much to be positive about as we arrive in the new year. From increases in equipment spending and revenue in the materials market, to record level silicon wafer shipments projections, 2015 forecasts all point in the right direction. Industry players are also doing their part to address new challenges, creating strategies to overcome complexities associated with innovative techniques, such as multipatterning and 3D architectures.

The semiconductor industry continues to explore new technologies, including 3DIC, TSV, and FinFETs, which carry challenges that also happen to represent opportunities. First, for memory as well as foundry logic, the need for multipatterning to extend lithography is a key focus. We're seeing some of the value of a traditional lithography tool shifting into some of the non-litho processing steps. As such, customers need to monitor litho and non-litho sources of error and critical defects to be able to yield successfully at next generation nodes. To enable successful yields with decreasing patterning process windows, it is essential to address all sources of error to provide feed forward and feed backward correctly.

The transition from 2D to 3D in memory and logic is another focus area. 3D leads to tighter process margins because of the added steps and complexity. Addressing specific yield issues associated with 3D is a great opportunity for companies that can provide value in addressing the challenges customers are facing with these unique architectures.

The wearable, intelligent mobile and IoT markets are continuing to grow rapidly and bring new opportunities. We expect the IoT will drive higher levels of semiconductor content and contribute to future growth in the industry. The demand for these types of devices will add to the entire value chain including semiconductor devices but also software and services. The semiconductor content in these devices can provide growth opportunities for microcontrollers and embedded processors as well sensing semiconductor devices.

Critical to our industry's success is tight collaboration among peers and with customers. With such complexity to the market and IC technology, it is very important to work together to understand challenges and identify where there are opportunities to provide value to customers, ultimately helping them to make the right investments and meet their ramps.

## Controlling manufacturing variability key to success at 10 nm

**RICHARD GOTTSCHO**, *Ph.D., Executive Vice President, Global Products, Lam Research Corporation*

This year, the semiconductor industry should see the emergence of chip-making at the 10 nm technology node. When building devices with geometries this small, controlling manufacturing process variability is essential and most challenging since variation tolerance scales with device dimensions.

Controlling variability has always been important for improving yield and device performance. With every advance in technology and change in design rule, tighter process controls are needed to achieve these benefits. At the 22/20 nm technology node, for instance, variation tolerance for CDs (critical dimensions) can be as small as one nanometer, or about 14 atomic layers; for the 10 nm node, it can be less than 0.5 nm, or just 3 – 4 atomic layers. Innovations that drive continuous scaling to sub-20 nm nodes, such as 3D FinFET devices and double/quadruple patterning schemes, add to the challenge of reducing variability. For example, multiple patterning processes require more stringent control of each step because additional process steps are needed to create the initial mask: more steps mean more variability overall. Multiple patterning puts greater constraints not only on lithography, but also on deposition and etching.

Three types of process variation must be addressed: within each die or integrated circuit at an atomic level, from die to die (across the wafer), and from wafer to wafer (within a lot, lot to lot, chamber to chamber, and fab to fab). At the device level, controlling CD variation to within a few atoms will increasingly require the application of technologies such as atomic layer deposition (ALD) and atomic layer etching (ALE). Historically, some of these processes were deemed too slow for commercial production. Fortunately, we now have cost-effective solutions, and they are finding their way into volume manufacturing.

To complement these capabilities, advanced process control (APC) will be incorporated into systems to tune chemical and electrical gradients across the wafer, further reducing die-to-die variation. In addition, chamber matching has never been more important. Big data analytics and subsystem diagnostics are being developed and deployed to ensure that every system in a fab produces wafers with the same process results to atomic precision.

Looking ahead, we expect these new capabilities for advanced variability control to move into production environments sometime this year, enabling 10 nm-node device fabrication.

## 2015: The year 3D-IC integration finally comes of age

**PAUL LINDNER**, *Executive Technology Director, EV Group*

2015 will mark an important turning point in the course of 3D-IC technology adoption, as the semiconductor industry moves 3D-IC fully out of development and prototyping stages onto the production floor. In several applications, this transition is already taking place. To date, at least a dozen components in a typical smart phone employing 3D-IC manufacturing technologies. While the application processor and memory in these smart devices continue to be stacked at a package level (POP), many other device components—including image sensors, MEMS, RF front end and filter devices—are now realizing the promise of 3D-IC, namely reduced form factor, increased performance and most importantly reduced manufacturing cost.

The increasing adoption of wearable mobile consumer products will also accelerate the need for higher density integration and reduced form factor, particularly with respect to MEMS devices. More functionality will be integrated both within the same device as well as within one package via 3D stacking. Nine-axis international measurement units (IMUs, which comprise three accelerometers, three gyroscopes and three magnetic axes) will see reductions in size, cost, power consumption and ease of integration.

On the other side of the data stream at data centers, expect to see new developments around 3D-IC technology coming to market in 2015 as well. Compound semiconductors integrated with photonics and CMOS will trigger the replacement of copper wiring with optical fibers to drive down power consumption and electricity costs, thanks to 3D stacking technologies. The recent introduction of stacked DRAM with high-performance microprocessors, such as Intel's Knights Landing processor, already demonstrate how 3D-IC technology is finally delivering on its promises across many different applications.

Across these various applications that are integrating stacked 3D-IC architectures, wafer bonding will play a key role. This is true for 3D-ICs integrating through silicon vias (TSVs), where temporary bonding in the manufacturing flow or permanent bonding at the wafer-level is essential. It's the case for reducing power consumption in wearable products integrating MEMS devices, where encapsulating higher vacuum levels will enable low-power operation of gyroscopes. Finally, wafer-level hybrid fusion bonding—a technology that permanently connects wafers both mechanically and electrically in a single process step and supports the development of thinner devices by eliminating adhesive thickness and the need for bumps and pillars—is one of the promising new processes that we expect to see utilized in device manufacturing starting in 2015.

## 2015: Curvilinear Shapes Are Coming

**AKI FUJIMURA**, *CEO, D2S*

For the semiconductor industry, 2015 will be the start of one of the most interesting periods in the history of Moore's Law. For the first time in two decades, the fundamental machine architecture of the mask writer is going to change over the next few years—from Variable Shaped Beam (VSB) to multi-beam. Multi-beam mask writing is likely the final frontier—the technology that will take us to the end of the Moore's Law era. The write times associated with multi-beam writers are constant regardless of the complexity of the mask patterns, and this changes everything. It will open up a new world of opportunities for complex mask making that make trade-offs between design rules, mask/wafer yields and

mask write-times a thing of the past. The upstream effects of this may yet be underappreciated.

While high-volume production of multi-beam mask writing machines may not arrive in time for the 10nm node, the industry is expressing little doubt of its arrival by the 7nm node. Since transitions of this magnitude take several years to successfully permeate through the ecosystem, 2015 is the right time to start preparing for the impact of this change. Multi-beam mask writing enables the creation of very complex mask shapes (even ideal curvilinear shapes). When used in conjunction with optical proximity correction (OPC), inverse lithography technology (ILT) and pixelated masks, this enables more precise wafer writing with improved process margin. Improving process margin on both the mask and wafer will allow design rules to be tighter, which will re-activate the transistor-density benefit of Moore's Law.

The prospect of multi-beam mask writing makes it clear that OPC needs to yield better wafer quality by taking advantage of complex mask shapes. This clear direction for the future and the need for more process margin and overlay accuracy at the 10nm node aligns to require complex mask shapes at 10nm. Technologies such as model-based mask data preparation (MB-MDP) will take center stage in 2015 as a bridge to 10nm using VSB mask writing.

Whether for VSB mask writing or for multi-beam mask writing, the shapes we need to write on masks are increasingly complex, increasingly curvilinear, and smaller in minimum width and space. The overwhelming trend in mask data preparation is the shift from deterministic, rule-based, geometric, context-independent, shape-modulated, rectangular processing to statistical, simulation-based, context-dependent, dose- and shape-modulated, any-shape processing. We will all be witnesses to the start of this fundamental change as 2015 unfolds. It will be a very exciting time indeed.

## Data integration and advanced packaging driving growth in 2015

**MIKE PLISINSKI**, *Chief Operating Officer, Rudolph Technologies, Inc.*

We see two important trends that we expect to have major impact in 2015. The first is a continuing investment in developing and implementing 3D integration and advanced packaging processes, driven not only by the demand for more power and functionality in smaller volumes, but also by the dramatic escalation in the number and density I/O lines per die. This includes not only through silicon vias, but also copper pillar bumps, fan-out packaging, hyper-efficient panel-based packaging processes that use dedicated lithography system on rectangular substrates. As the back end adopts and adapts processes from the front end, the lines that have traditionally separated these areas are blurring. Advanced packaging processes require significantly more inspection and control than conventional packaging and this trend is still only in its early stages.

The other trend has a broader impact on the market as a whole. As consumer electronics becomes a more predominant driver of our industry, manufacturers are under increasing pressure to ramp new products faster and at higher volumes than ever before. Winning or losing an order from a mega cell phone manufacturer can make or break a year, and those orders are being won based on technology and quality, not only price as in the past. This is forcing manufacturers to look for more comprehensive solutions to their process challenges. Instead of buying a tool that meets certain criteria of their established infrastructure, then getting IT to connect it and interpret the data and write the charts and reports for the process engineers so they can use the tool, manufacturers are now pushing much of this onto their vendors, saying, "We want you to provide a working tool that's going to meet these specs right away and provide us the information we need to adjust and control our process going forward." They want information, not just data.

Rudolph has made, and will continue to make, major investments in the development of automated analytics for process data. Now more than ever, when our customer buys a system from us, whatever its application - lithography, metrology, inspection or something new, they also

want to correlate the data it generates with data from other tools across the process in order to provide more information about process adjustments. We expect these same customer demands to drive a new wave of collaboration among vendors, and we welcome the opportunity to work together to provide more comprehensive solutions for the benefit of our mutual customers.

### Process Data – From Famine to Feast

**JACK HAGER**, *Product Marketing Manager, FEI*

As shrinking device sizes have forced manufacturers to move from SEM to TEM for analysis and measurement of critical features, process and integration engineers have often found themselves having to make critical decisions using meagre rations of process data. Recent advances in automated TEM sample preparation, using FIBs to prepare high quality, ultra-thin site-specific samples, have opened the tap on the flow of data. Engineers can now make statistically-sound decisions in an environment of abundant data. The availability of fast, high-quality TEM data has whet their appetites for even more data, and the resulting demand is drawing sample preparation systems, and in some cases, TEMs, out of remote laboratories and onto the fab floor or in a "near-line" location. With the high degree of automation of both the sample preparation and TEM, the process engineers, who ultimately consume the data, can now own and operate the systems that generate this data, thus having control over the amount of data created.

The proliferation of exotic materials and new 3D architectures at the most advanced nodes has dramatically increased the need for fast, accurate process data. The days when performance improvements required no more than a relatively simple "shrink" of basically 2D designs using well-understood processes are long gone. Complex, new processes require additional monitoring to aide in process control and failure analysis trouble-shooting. Defects, both electrical and physical, are not only more numerous, but typically smaller and more varied. These defects are often buried below the exposed surface which limits traditional inline defect-monitoring equipment effectiveness. This has resulted in renewed challenges in diagnosing their root causes. TEM analysis now plays a more prevalent role providing defect insights that allow actionable process changes.

While process technologies have changed radically, market fundamentals have not. First to market still commands premium prices and builds market share. And time to market is determined largely by the speed with which new manufacturing processes can be developed and ramped to high yields at high volumes. It is in these critical phases of development and ramp that the speed and accuracy of automated sample preparation and TEM analysis is proving most valuable. The methodology has already been adopted by leading manufacturers across the industry - logic and memory, IDM and foundry. We expect the adoption to continue, and with it, the migration of sample preparation and advanced measurement and analytical systems into the fab.

### Diversification of processes, materials will drive integration and customization in sub-fab

**KATE WILSON**, *Global Applications Director, Edwards*

We expect the proliferation of new processes, materials and architectures at the most advanced nodes to drive significant changes in the sub fab where we live. In particular, we expect to see a continuing move toward the integration of vacuum pumping and abatement functions, with custom tuning to optimize performance for the increasingly diverse array of applications becoming a requirement. There is an increased requirement for additional features around the core units such as thermal management, heated N2 injection, and precursor treatment pre- and post-pump that also need to be managed.

Integration offers clear advantages, not only in cost savings but also in safety, speed of installation, smaller footprint, consistent implementation of correct components, optimized set-ups and controlled ownership of the process effluents until they are abated reliably to safe levels. The benefits are not always immediately apparent. Just as effective integration is much more than simply adding a pump to an abatement system, the initial cost of an integrated system is more than the cost

of the individual components. The cost benefits in a properly integrated system accrue primarily from increased efficiencies and reliability over the life of the system, and the magnitude of the benefit depends on the complexity of the process. In harsh applications, including deposition processes such as CVD, Epi and ALD, integrated systems provide significant improvements in uptime, service intervals and product lifetimes as well as significant safety benefits.

The trend toward increasing process customization impacts the move toward integration through its requirement that the integrator have detailed knowledge of the process and its by-products. Each manufacturer may use a slightly different recipe and a small change in materials or concentrations can have a large effect on pumping and abatement performance. This variability must be addressed not only in the design of the integrated system but also in tuning its operation during initial commissioning and throughout its lifetime to achieve optimal performance. Successful realization of the benefits of integration will rely heavily on continuing support based on broad application knowledge and experience.

## Process Data – From Famine to Feast

**DR. ZHIHONG LIU**, *Executive Chairman, ProPlus Design Solutions, Inc.*

It wasn't all that long ago when nano-scale was the term the semiconductor industry used to describe small transistor sizes to indicate technological advancement. Today, with Moore's Law slowing down at sub-28nm, the term more often heard is giga-scale due to a leap forward in complexity challenges caused in large measure by the massive amounts of big data now part of all chip design.

Nano-scale technological advancement has enabled giga-sized applications for more varieties of technology platforms, including the most popular mobile, IoT and wearable devices. EDA tools must respond to such a trend. On one side, accurately modeling nano-scale devices, including complex physical effects due to small geometry sizes and complicated device structures, has increased in importance and difficulties. Designers now demand more from foundries and have higher standards for PDK and model accuracies. They need to have a deep understanding of the process platform in order to make their chip or IP competitive.

On the other side, giga-scale designs require accurate tools to handle increasing design size. The small supply voltage associated with technology advancement and low-power applications, and the impact of various process variation effects, have reduced available design margins. Furthermore, the big circuit size has made the design sensitive to small leakage current and small noise margin. Accuracy will soon become the bottleneck for giga-scale designs.

However, traditional design tools for big designs, such as FastSPICE for simulation and verification, mostly trade-off accuracy for capacity and performance. One particular example will be the need for accurate memory design, e.g., large instance memory characterization, or full-chip timing and power verification. Because embedded memory may occupy more than 50% of chip die area, it will have a significant impact on chip performance and power. For advanced designs, power or timing characterization and verification require much higher accuracy than what FastSPICE can offer –– 5% or less errors compared to golden SPICE.

To meet the giga-scale challenges outlined above, the next-generation circuit simulator must offer the high accuracy of a traditional SPICE simulator, and have similar capacity and performance advantages of a FastSPICE simulator. New entrants into the giga-scale SPICE simulation market readily handle the latest process technologies, such as 16/14nm FinFET, which adds further challenges to capacity and accuracy.

One giga-scale SPICE simulator can cover small and large block simulations, characterization, or full-chip verifications, with a pure SPICE engine that guarantees accuracy, and eliminates inconsistencies in the traditional design flow. It can be used as the golden reference for FastSPICE applications, or directly replace FastSPICE for memory designs.

The giga-scale era in chip design is here and giga-scale SPICE simulators are commercially available to meet the need.

# Underdog DRAM

**CHRISTIAN G. DIESELDORFF**, *SEMI, San Jose, CA*

*DRAM shifts out of a slump, but sector faces obstacles.*

The DRAM sector experienced a major decline during and following the 2008-2009 financial crisis and eventually contracted — both the number of suppliers and installed fab production capacity. According to the SEMI World Fab Forecast Report, the outlook is now more positive as DRAM bit demand is on the rise and average selling prices improved in both 2013 and 2014. Installed capacity is expected to emerge from negative to positive territory by the end of 2016, but factors for growth are complicated by complex technology issues.

For five years before the economic downturn, yearly growth rates for installed fab capacity trended in high double digits. Looking back to 2007, eleven major companies produced DRAM chips in about 40 facilities globally, with installed capacity growing by 40 to 50 percent year-over-year from 2003 to 2007.

Since that time, the number of companies shrank from 11 players to six, with only 20 facilities in production and three major players (Samsung, Micron and SK Hynix) as the industry consolidated and contracted (**FIGURE 1**). Qimonda, Promos and Powerchip left the scene, while Elpida and Rexchip were acquired by Micron. In addition, some front end fabs were converted from DRAM to Logic, Flash or other purposes.

The smaller number of key suppliers has stabilized the DRAM investment cycle and increasingly the manufacturers focus investments on market demand, not on production share gain. Meanwhile, DRAM bit demand is growing for applications such as mobile and infrastructure/servers. One leading memory company has predicted CAGR of 27 percent for bit growth from 2013 to 2017.

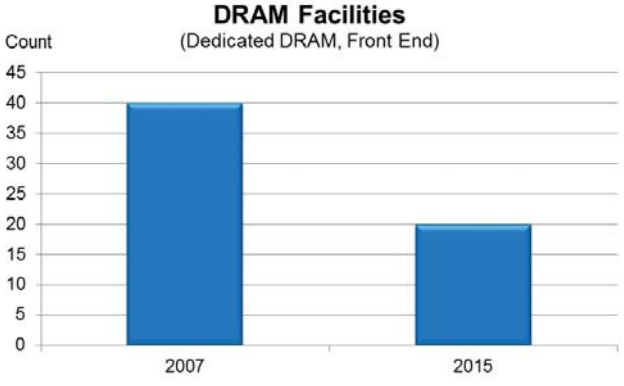



**FIGURE 1.** Major DRAM companies (including Inotera) operating chip facilities (Source: SEMI, 2015).

## Obstacle: New paradigm is a loss of capacity

SEMI's tracking of fab data reveal that when a company transitions a fab to the next leading edge technology there is a capacity loss. Increased complexity and more process steps mean that these fabs produce fewer wafers per square foot of cleanroom. This trend affects all industry segments, beginning at the 30/28nm node and smaller, and has been observed since 2012. Depending on the age of the fab and product type, this loss can be significant, as much as 10-20 percent (**FIGURE 2**).

SEMI's World Fab Forecast report tracks nine fabs following this pattern: significant loss of capacity when transitioning to the next leading edge technology node. From 2014 to 2016, existing DRAM fabs are expected to lose a total of about 25,000 wafers per month, every year when transitioning to next leading edge technology node.

To compensate for this and to meet expected

**CHRISTIAN GREGOR DIESELDORFF** *is Director of Semiconductor Industry Analysis & Statistics, SEMI, San Jose, CA.*

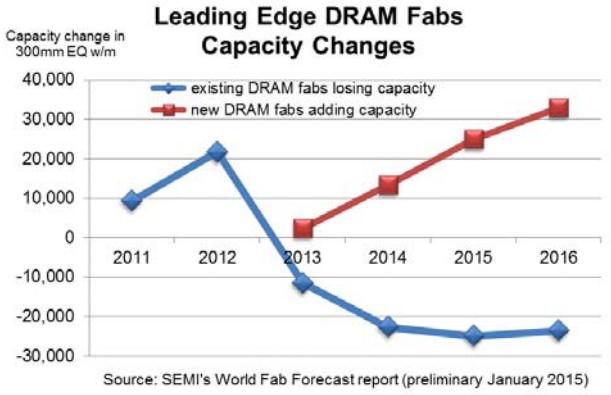



**FIGURE 2.** Blue line shows that existing DRAM fabs lose capacity over time when transitioning to next technology node, while the red line shows new DRAM facilities adding capacity. (Source: SEMI, 2015).

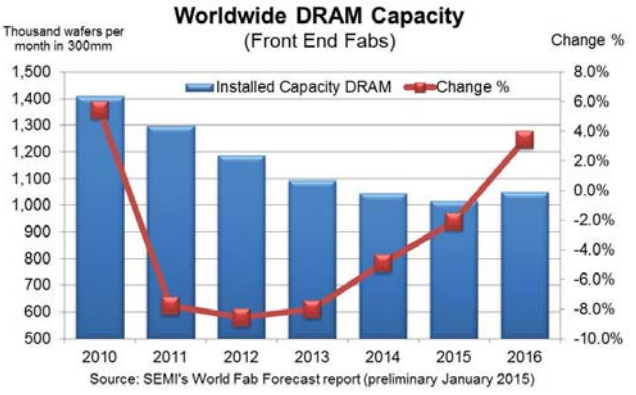



**FIGURE 3.** Worldwide DRAM capacity for Front End facilities in 300mm equivalent wafers per month and change rate in percent (Source: SEMI, 2015).

bit demand, the industry is beginning to add new capacity with new fabs and lines. By 2015, three or four new fabs or lines will be in operation. Of course, these will require time to ramp up; meaning that net capacity change likely will not shift from negative to positive territory until 2016, when about 3 percent growth is forecast. **FIGURE 3** illustrates how this could potentially affect worldwide DRAM capacity.

The worldwide loss of DRAM capacity from 2010 to 2014 is about 25 percent. The loss of capacity due to technology upgrade kicks in about 2013 timeframe. Before that the loss is due to consolidations, closure and change of product types.

## Obstacle: What's next, after 15nm?

Shrinking the DRAM nodes has become increasingly difficult. As most companies produce in volume 30nm-25nm, some companies began already to offer 21/20nm node. The next stage beyond that is only just being explored. Will the industry see another shrink down to 1Ynm? Or is this too challenging, and for most, not economically feasible? Other technologies may move forward to eventually replace conventional DRAM, such as non-volatile memories like MRAM (Magnetic RAM), FeRAM (Ferro-electric RAM) and ReRAM (Resistive RAM), and PRAM or PCRAM (Phase-Change RAM). As these technologies surface, DRAM capacity may be challenged again.

In summary, DRAM, the underdog, comes from behind and appears to promise positive growth by 2016. With the introduction of new technologies, it remains to be seen how DRAM capacity will be impacted and how much new wafer capacity will be needed. The SEMI World Fab Forecast Report lists over 40 facilities making DRAM products. Many facilities have major spending for equipment and construction planned for 2015.

# Processing of graphene on 300mm Si wafers in a state-of-the-art CMOS fabrication facility

**V. KAUSHIK, N. AGBODO, H. CHUNG, M. HATZISTERGOS, B. JI, P. KHARE, T. LAURSEN, D. LOVELL, A. MESFIN, T. MURRAY, S. NOVAK, H. STAMPER, D. STEINKE, S. VIVEKANAND, T. VO, M. PASSARO AND M. LIEHR**, *College of Nanoscale Science and Engineering, SUNY Polytechnic Institute, Albany NY.*

*The building blocks are described that can be used to fabricate other novel device architectures that can take advantage of the unique properties of graphene or other interesting single-layer (i.e., 2D) materials.*

Graphene is a 2-dimensional sheet of sp2-hybridized carbon atoms with unique physical, mechanical and electrical properties. Commonly found in its multi-layer form, graphite, its isolation as a single-layer has received major attention in the literature for CMOS applications in low-power, high-mobility, analog and radio-frequency devices [1-5]. Single layers of graphene can be obtained by exfoliation from graphite, thermal decomposition on SiC surfaces [6], or chemical vapor deposition (CVD) on metallic surfaces such as copper or nickel. For the evaluation of its compatibility with silicon-based CMOS, it is necessary to study graphene layers on silicon wafers. In this article, we demonstrate the introduction of single-layer graphene -- grown by CVD and transferred to 300mm Si wafers -- into a state-of-the-art CMOS fab, and the further processing of these wafers using advanced CMOS techniques in order to obtain working graphene-channel FETs. The fabrication steps developed in this work, chosen to minimize impacts to graphene quality during fab-based processing, can serve as building blocks for future research in conventional and novel device architectures.

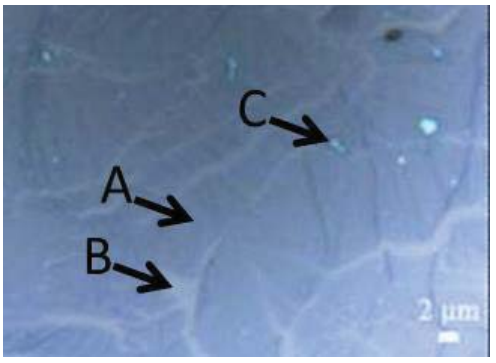
## Graphene growth, etch and transfer

Graphene was grown by low-pressure CVD in a typical tube furnace on commercially available Cu foil at ~950C by CH4 cracking. Prior to graphene transfer, a thermal-release tape was placed on the Cu foil to serve as a support for further processing. The Cu foil was then etched using a mixture of hydrochloric acid, hydrogen peroxide and de-ionized (DI) water. Multiple sequences of this etch were used to minimize re-deposition of the etched copper onto the tape with graphene, followed by a final DI water rinse, leaving only the graphene and tape remaining. The tape and graphene adhesion was then placed on a 300mm Si wafer or a Si wafer capped with SiO2 (SiO2/Si) and heated to remove the tape, resulting in a wafer with graphene on its surface. (Although the use of PMMA [poly methyl acrylate] has been reported [7] as a suitable support film for graphene transfer, we did not use it since the PMMA is typically dissolved in acetone, a solvent that is incompatible with 300mm fab integration due to health

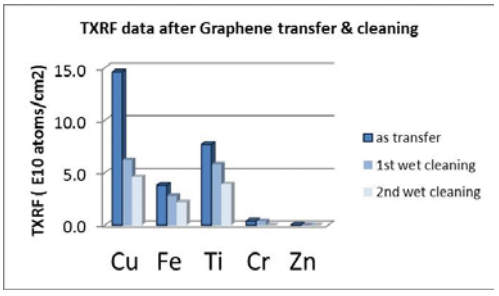
*The authors are with the College of Nanoscale Science and Engineering, SUNY Polytechnic Institute, 257 Fuller Rd, Albany NY 12203.*

and safety considerations.)

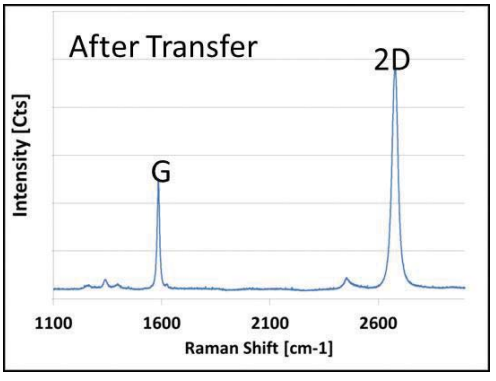
Due to the use of Cu foil and laboratory instruments, the graphene growth, etch and transfer processes have the potential to leave residual metal contamination on the wafer. Since the introduction of these wafers into the fab for further processing requires demonstration of low levels of metal contaminants, the handling of the graphene-on-Cu foil and the Cu-etching was performed by avoiding the use of metallic instruments. The detection of metallic ions on the transferred graphene was performed by TXRF (Total-reflection X-Ray Fluorescence), which is a highly surface sensitive technique. Using this feedback, we were able to determine that the use of ceramic scissors for cutting the foil, ceramic tweezers for handling the tape and foil, and a well-ventilated clean laminar-flow hood area were effective in reducing metallic contaminants.



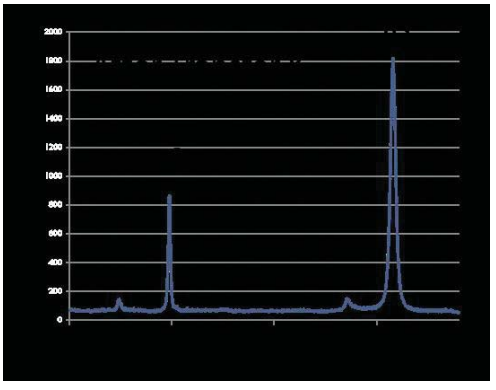

A




B




C



D

**FIGURE 1.** Shown is an optical micrograph of the graphene after transfer on to a SiO2/Si wafer and cleans indicating areas with graphene (A), areas with no graphene ((B) and suspected tape residue (C).Figure 1b shows metal contamination levels determined from TXRF spectra for as-transfer and after wet cleans. Figure 1c and d show Raman spectra obtained from graphene on SiO2 wafer before and after wet-cleans respectively showing no degradation in single-layer graphene quality.

**FIGURE 1A** shows an optical micrograph of graphene transferred on a SiO2/Si wafer and post-transfer cleans. While graphene covers most of the wafer surface, some gaps were observed due to imperfections in the transfer process. The use of thermal tape can potentially cause tape residue to remain on the graphene as well (shown in Figure 1a), which is partly mitigated by post-transfer cleans.

**FIGURE 1B** shows TXRF data of the concentration of metallic contaminants after graphene transfer and after post-transfer cleans using HCl chemistry. TXRF spectra of the SiO2/Si wafer after transfer showed high levels of metallic Cu, Fe and Ti. Post-transfer cleans of the wafer reduced the metallic contamination levels to ~5E10 at/cm2.

Raman spectroscopy is the technique most often used to measure the quality of monolayer graphene [2,8]. High quality graphene shows distinct peaks at 1580cm-1 (G peak) and 2690cm-1 (2D peak). In undamaged graphene the 2D peak is a factor of two higher than the G peak, with this ratio decreasing as the layer accumulates damage. In addition, damaging the graphene causes the appearance of a peak at 1350cm-1 (D peak). These features have been used to monitor the quality of the graphene layers at various stages in our process. **FIGURE 1C** shows a Raman spectrum of the graphene immediately following the transfer. The intensities of the 2D- and G-peaks are consistent with those for single-layer graphene. The low intensity of the D-peak in **FIGURE 1D** confirms that wet clean sequences used did not significantly degrade the electrical and physical properties of the graphene.

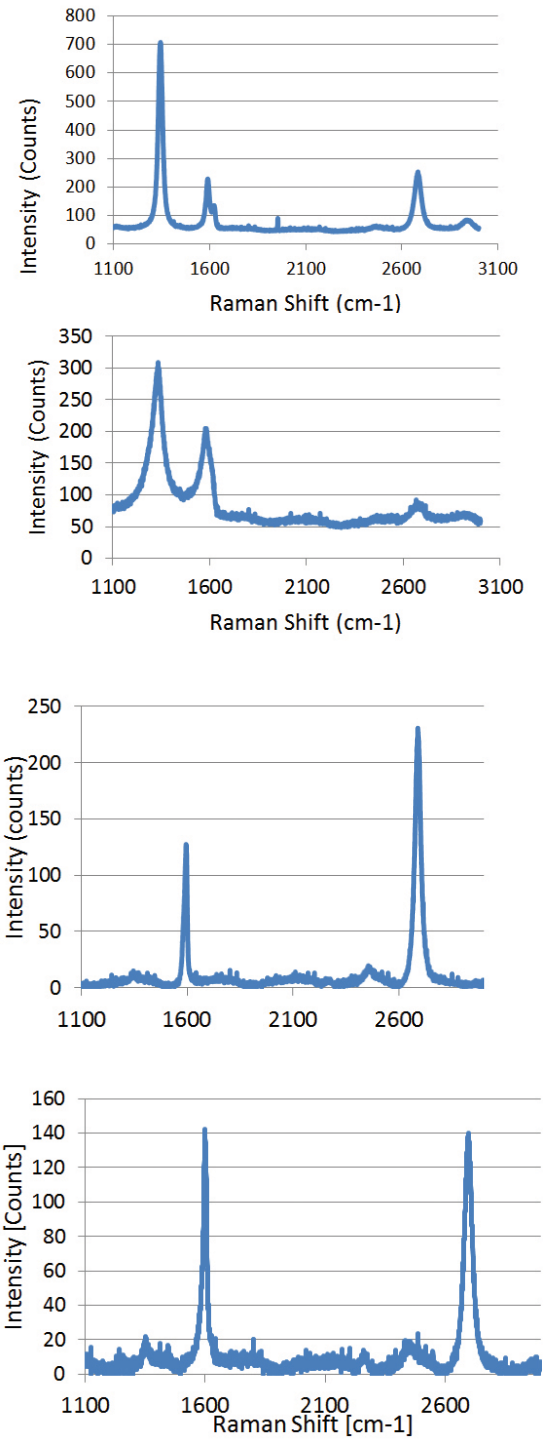



**FIGURE 2.** Shown are Raman spectra of the graphene layer with D-peak indicative of damage after after a) plasma oxidation and b) PVD metal deposition and oxidation. Figures 2c-d show Raman spectra after c) spin-on dielectric deposition and d) after subsequent bake anneal indicating a reduction 2D/G peak ratio but no D-peak.

## Device fabrication: Gate and dielectric formation

A simple MOSFET-like integration scheme using graphene as the channel material was chosen to demonstrate the processing of graphene in our 300mm line. For best device performance, a high quality gate dielectric is required, and several dielectric layers deposited over graphene were evaluated using Raman spectroscopy to observe their effects on graphene quality. Processes that involved high temperatures -- e.g., CVD or plasmas -- introduced defects into the graphene, as is evident from a D-peaks shown in **FIGURES 2A** and **2B**, thus ruling out typical gate dielectric layers available in CMOS fabs. Atomic layer deposition (ALD) processes have been reported to show poor nucleation on the graphene surface due to a lack of available bonds [9]. Evaporation processes, reported to be effective after depositing a thin metal on top of the graphene which is then oxidized, are not well suited to modern high volume manufacturing fabs. To circumvent these problems, we 'inverted' the conventional MOSFET structure using buried gates [10]. In this scheme, tungsten gate electrodes were fabricated in thermal oxide by a damascene process. After these electrodes were in place, a gate-quality 4nm HfO2 dielectric was deposited using an ALD process. Graphene was then transferred onto this HfO2 surface. This approach eliminates the need for a gate-quality dielectric deposition over the graphene. **FIGURE 3A** shows the process sequence for the device while **FIGURE 3B** shows a schematic of the device structure.

In order to process the wafers after graphene transfer, we capped the graphene with a spin-on dielectric film to protect its quality. We were thus able to avoid the above mentioned issues of high temperature, plasma processing, and nucleation. The spin-on dielectric film was ~35nm thick and allowed the graphene layer to withstand higher temperature and plasma processes, including film depositions, anneals, and reactive ion etching (RIE). With no discernible D-peak, the Raman spectra in **FIGURES 2C AND 2D** show that the capping layer preserved graphene quality.

Subsequently, a photolithography step followed by an RIE process was used to pattern the active area and

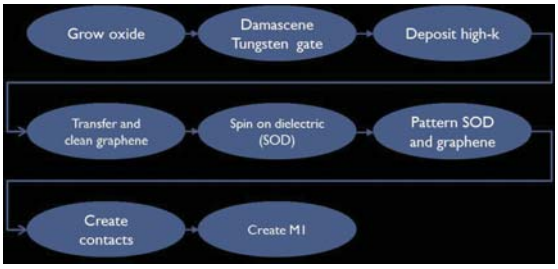



**FIGURE 3A**. Schematic of process steps used in the fabrication of graphene-channel devices.

to remove the capping dielectric, graphene, and gate oxide from the field area (**FIGURE 4A**). With the active graphene area patterned, the process then moved to the contact module.

## Device fabrication: Contact formation

The formation of metal contacts to graphene is one of the more challenging aspects of fabricating a graphene device in a modern fab. Most of the available literature reports the use of e-beam evaporation and lift-off techniques to form metal contacts to graphene [11,12]. However, these techniques and the typical metals used (Au, Au-Pd, Cr) are more suited to a lab environment than a high-volume Si fab. We used a conventional damascene contact process and a plated Cu-based metallurgy, which introduced challenges associated with the contact open etch and cleans, and during metal depositions.

In this study, the contact stack consisted of conventional nitride and oxide that was planarized using chemical-mechanical polishing (CMP). Immersion lithography was used to define contacts with dimensions ranging from 100nm to 350nm. After the dry etch process, the wafers were cleaned using a wet chemistry compatible with the exposed graphene. A modified metal barrier/liner/seed process was then used to initiate the metallization process in the contacts, followed by CMP of the metal overburden. Contact to the graphene was made along the circumference of the contact plug, which has been reported to be more effective than top contact schemes [13]. The contact module was followed by a standard metallization module using a damascene copper process to fabricate the pads for automated in-line testing of the graphene FETs. Future work will include further optimization of etches and variations of liner metallurgy and contact

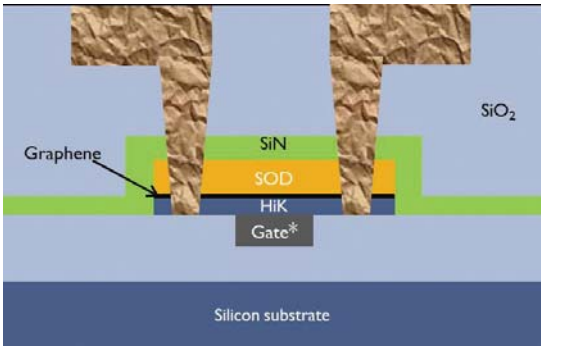



**FIGURE 3B**. Schematic of device structure to exercise process steps.

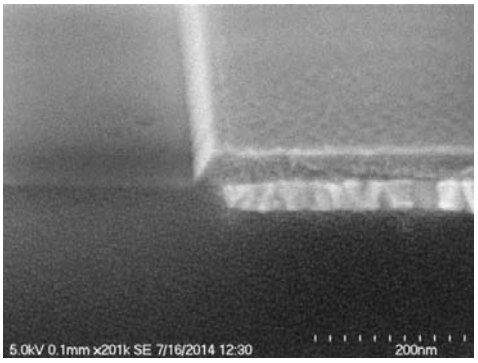
architecture (top vs. edge) to study the effects on contact resistance and device performance.

## Electrical test results

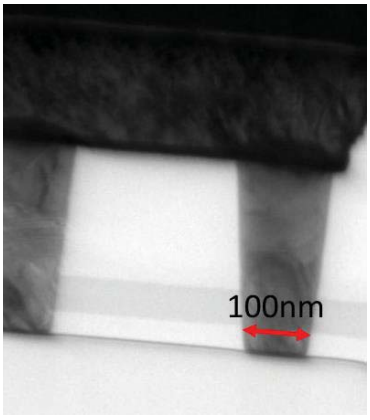
The devices were tested using DC current-voltage sweeps on various graphene-channel MOSFETs (GFETs) using a standard parametric tester. Two-point transport measurements demonstrated the MOSFETs' gate-voltage-induced resistance modulations. A typical transport curve is shown in **FIGURE 4D**. Transistor behavior was observed in GFET devices with various graphene channel widths ranging from 1µm to 10µm. GFET channel widths ranging from 50nm to 10µm were controlled by the patterned back gates. Low operating voltages (with Vg swept from -1V to 1V) were achieved due to our utilization of a thin high-k dielectric. The Dirac point in **FIGURE 4D** is shown to be nominally at 0V with the gate resolution at 50mV, which is the step-size of the sweep. Since we only used 2-point testing, the measured total resistance includes the channel resistance, series resistance of graphene area not covered by the gate, and the graphene-metal contact resistance. While this limits our ability to characterize the intrinsic GFET transport property, it does point to the challenges for the fabrications of product-like devices; i.e., significant reductions of contact and series resistances are definitely required.

## Conclusion

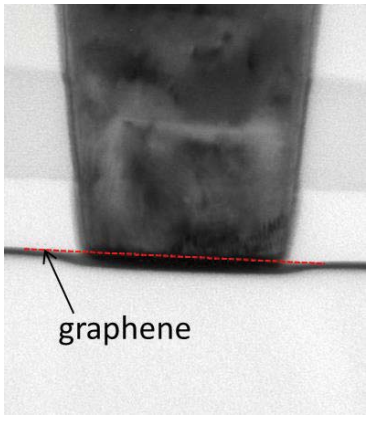
We have demonstrated that working MOSFETs with graphene channels can be fabricated in a conventional 300mm CMOS fabrication line using state-of-the-art process tools. The building blocks shown here can be used to fabricate other novel device architectures



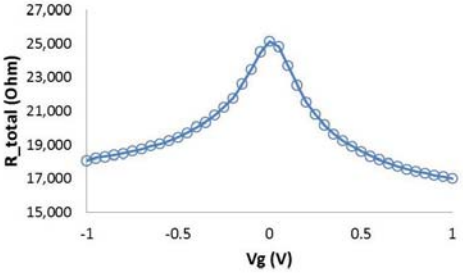

A




B




C




D

**FIGURE 4.** 4a shows XSEM of metal gate and active region after pattern and etch. Figure 4b shows lower magnification view of copper contacts through insulator and metal at top. Figure 4c shows higher magnification view of 100nm contact. Dotted line shows expected location of graphene. Figure 4d shows a transport curve of graphene FETs using a 2-point transport measurement on an in-line parametric tester. The gate voltage is controlled by the patterned back gate. The total resistance includes the channel resistance, series resistance of graphene area that is not covered by the gate, and the graphene-metal contact resistance.

that can take advantage of the unique properties of graphene or other interesting single-layer (i.e., 2D) materials. Further optimization of graphene transfer and contact schemes intended to reduce overall resistance are ongoing and will be reported in subsequent publications.

## Acknowledgement

The authors acknowledge the support of Profs. Alain Diebold and Ji-Ung Lee.

## References

1. "Electric field effect in atomically thin carbon films," by K. S. Novoselov, A. K. Geim, S. V. Morozov, et al., in Science, vol. 306, pp. 666–669, 2004.
2. "Honeycomb Carbon: A review of graphene" by M.J. Allen, V.C. Tung & R.B. Kaner in Chemical Review, 110, 132-145, 2010.
3. "Graphene Electronics: Materials, Devices, and Circuits" by Y. Wu, D.B. Farmer, F. Xia, and P. Avouris in Proceedings of the IEEE, Vol. 101, No. 7, 2013.
4. "Unusual transport properties in carbon-based nanoscale materials: nanotubes and graphene" by M. Purewal, Y. Zhang and P. Kim in Phys. Stat. Sol. (b) 243, No. 13, 3418–3422 (2006)
5. "On the importance of band gap formation in graphene for analog device application" by S. Das and J. Appenzeller, in IEEE Trans. Nanotechnol., vol. 10, no. 5, pp. 1093–1098, Sep. 2011.
6. "Epitaxial Graphene: Designing a new electronics material" by W. De Heer, C. Berger, X. Wu et al., in ECS Transactions 19 (5) 95-105 2009 [7]. "Toward Clean and Crackless Transfer of Graphene" by X. Liang, B. Sperling,I. Calizo, et al., in ACS Nano. VOL. 5 ' NO. 11 ' 9144–9153 ' 2011
7. "Toward Clean and Crackless Transfer of Graphene" by X. Liang, B. Sperling,I. Calizo, et al., in ACS Nano. VOL. 5 ' NO. 11 ' 9144–9153 ' 2011
8. "Raman Spectrum of Graphene and Graphene Layers", A. C. Ferrari, J. C. Meyer, V. Scardaci, et al. in Phys. Rev. Lett. 97, 187401 (2006).
9. "Scaling of Al2O3 dielectric for graphene field-effect transistors", B. Fallahazad, K. Lee, G. Lian, S. Kim, C. Corbet, D. Ferrer, L. Colombo and E. Tutuc in Applied Physics Letters, 100, 093112 (2012)
10. "Angle-dependent carrier transmission in graphene p-n junctions", by S. Sutar, E. Comfort and J-U. Lee in ACS Nano. Lett. Vol. 12, pg 4460 (2012).
11. "Contacting graphene" by J.A. Robinson, M. LaBella, M. Zhu et al., in Applied Physics Letters, 98, 053103, 2011.
12. "Understanding the Electrical Impact of Edge Contacts in Few-Layer Graphene" by T. Chu & Z. Chen in ACS Nano. Vol. 8 ' No. 4 3584–3589 2014.
13. "One-Dimensional Electrical Contact to a Two-Dimensional Material" by L. Wang, I. Meric, P.Y. Huang et al, in Science 1 November 2013: Vol. 342 no. 6158 pp. 614-617

# Improving the Reliability of Dry Vacuum Pumps in High-k ALD Processes

**MIKE BOGER**, *Edwards Vacuum, Tokyo, Japan*

*Design features that contributed most to the improved performance include increased rotational speed, integrated rotor sleeves, and increased purge injection temperature.*

The use of high-k dielectric films deposited through atomic layer deposition, primarily in batch furnaces, has intensified, particularly in the manufacture of memory devices and high-k metal gates (HKMG) in logic devices. ALD uses a sequential purge and injection of the precursor gases to generate slow, but accurate growth of the films one atomic layer at a time. One of the precusors is typically a metal-organic compound from a liquid source, commonly zirconium or hafnium-containing materials, followed by ozone to create the high-k film.

Wafers are usually processed in a furnace with batch sizes of 200 or more wafers. Reliability of the vacuum system is imperative to prevent contamination and consequent scrapping of the wafers. Unexpected failures can cause significant loss of work in process and process downtime. For example, if the vacuum pump seizes suddenly due to internal contamination by process by-products, the pressure in the pipe between the vacuum and furnace rises, and there is a risk that powder deposited in the pipe will flow back into the furnace. This powder can not only contaminate wafers in the furnace, but also force a time-consuming clean-up that may remove the furnace from operation for a day or more.

## The challenge

The mean-time-between-service (MTBS) for a vacuum pump used in semiconductor manufacturing varies greatly depending on the particular process it supports and the design of the pump. For the ALD processes considered here most failures caused process by-products can be grouped into four categories.

- Corrosion - Attack on the metal components of the pump results in the opening of clearances leading to loss of base vacuum. Depending on the location of corrosion, the oxidation of the metal may actually generate powder that can cause seizure of rotating elements.
- Plating - The deposition of metal compounds on the surface of internal components fouls internal mechanism clearances, causing the pump to seize.
- Powder ingestion - Powder that enters the pump can jam rotating elements, leading to seizure.
- Condensation - Compounds in the pumped gas stream transition from a gaseous to a solid phase within the pump, depositing on internal surfaces and eventually leading to loss of clearance and seizure.

**MIKE BOGER** *is the Global Market Sector Manager – Semiconductor, Edwards Ltd*

Monitoring of pump operating conditions, such as input power, current, and running temperature, can provide an indication of the health of the pump. Events that lead to failure are generally gradual in nature. Advance notice periods can be measured in days. However, failures of vacuum pumps on high-k ALD processes often happen suddenly with little to no indication of distress prior to seizure.

A typical example of a vacuum pump used on a high-k ALD process is shown in **FIGURE 1**. This pump was used in a full production environment and consisted of a 1,800 $m^3h^{-1}$ mechanical booster mounted above a 160 $m^3h^{-1}$ dry pump. In this case, the pump exhibited a strong spike in running power, approximately 20 times normal, and was immediately removed for inspection. Significant deposition is evident in the booster (Fig. 1 left) and also in the last stage of the dry pump (Fig. 1 right). Evidence of the loss of clearance that caused the spike in input power is observed as a shiny area on the rotor lobe. In operation this pump was exposed to TEMAH (hafnium-containing liquid precursor), TMA (aluminum-containing liquid precursor), and ozone for producing $HfO_2$ and TMA $Al_2O_3$. It was exchanged after 1,200 hours of use.

**FIGURE 2** provides another example of a pump that was removed due to detection of a spike in input current. In this case, the booster, second stage, and final stage of the pump are shown. Although the process was nominally the same (deposition of $HfO_2$ and $Al_2O_3$), the deposition pattern is different. In this case, the booster and early stages of the dry pump show signs of a thin coating of a material that exhibits a green iridescent sheen. The final stage of the pump has a brown powder accumulation, but of a lighter color than that shown in Fig. 1.

In both of the examples shown in Figs. 1 and 2, the service interval of the pump was short and below the user's expectations. In these cases, which are representative of all the pumps used on this process, the user was forced to exchange pumps frequently to minimize the risk of wafer loss. Other customers had similar experiences. **TABLE 1** lists the films deposited and the preventative maintenance service intervals implemented by four customers. Analysis of serviced pumps suggested that processes depositing zirconium oxide were more challenging for the pump.

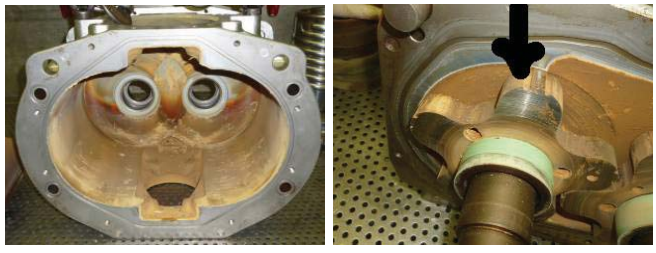


**FIGURE 1.** A picture of a disassembled pump after 1,200 hours of use on a high-k ALD process showing the deposition in the booster (left) and loss of clearance in the last stage of the dry pump (right).

**FIGURE 2.** Pictures of a disassembled pump that was removed for inspection after only 457 hours due to a large current spike detected during operation. In order, the pictures show the booster, second stage of the dry pump, and the final stage of the dry pump.

**TABLE 1.** **Customer experience during early introduction of the process**

| Customer | Deposited Film | Service Interval |
|---|---|---|
| A | $HfO_2$, $ZrO_2$, $Al_2O_3$ | 30-45 days |
| B | $HfO_2$, $Al_2O_3$ | 41 days |
| C | $HfO_2$, $Al_2O_3$ | 33-46 days |
| D | $HfO_2$, $Al_2O_3$ | approx. 60 days |

## Analysis

To better understand the reliability improvement challenge, a sample of the deposited material from a failed pump was analyzed. The results of the analysis, shown in **FIGURE 3**, revealed deposits rich in carbon and metal oxides, consistent with metal-organic precursors. The rate of oxide deposition appeared to be higher than that which would occur through pure ALD mechanisms, suggesting some chemical vapor deposition (CVD) or decomposition of the gases being pumped.

A survey of literature [1], [2], [3], [4] revealed that the typical reactants used in high-k ALD can react at high pressure and at low temperature without the need for external energetic activation. This suggests that even if there were no CVD or decomposition of gases within

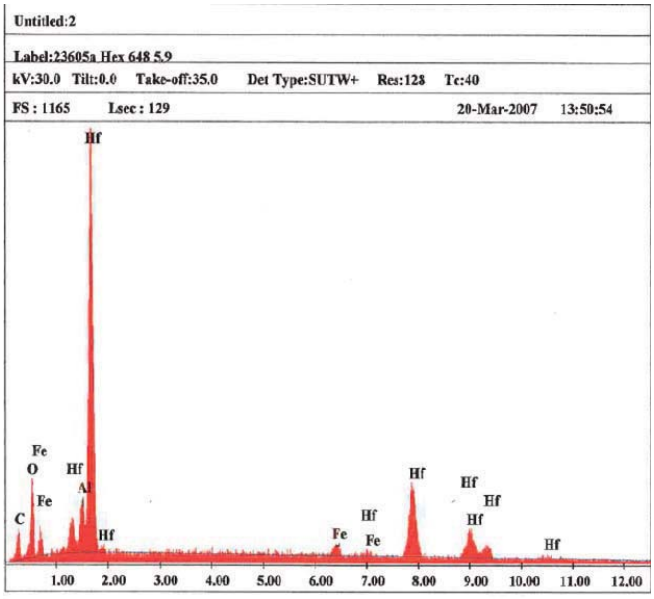



**FIGURE 3.** Analysis of the deposition within a failed pump showing hafnium, oxygen, and carbon components. FIGURE 4. Vapor pressure of TEMAH (0.2 mg/min with 14 slm of nitrogen) and simulated vapor pressure of TEMAH in the dry pump, inlet to outlet.

the pump, ALD-like films can still be deposited on the internal surfaces of the pump.

A simulation of the vapor pressure of TEMAH (one of the precursors used) within the pump was conducted, assuming a mass flow rate of 0.2 mg $min^{-1}$ for TEMAH. The simulation results were compared to the measured vapor pressure of TEMAH to determine if there was any risk of TEMAH condensing within the vacuum pump. The results, shown in **FIGURE 4**, suggest that there are sufficient safety margins in the actual conditions. The TEMAH will stay in vapor form while it travels through the pump, even if the actual flow varied by an order of magnitude from that assumed. Moreover, the pump temperature could be reduced substantially without risk of condensing TEMAH within the pump.

A number of pumps were inspected, a large majority of which were pumps exchanged prior to seizure. Unfortunately, although powder was evident in the final stages of all pumps, not all pumps had powders of the same color. Moreover, as seen in the middle photograph of Fig. 2, some pumps and boosters were relatively clean exhibiting just a green sheen of deposition. None of the observations, other than powder in the final stage of the dry pump, were

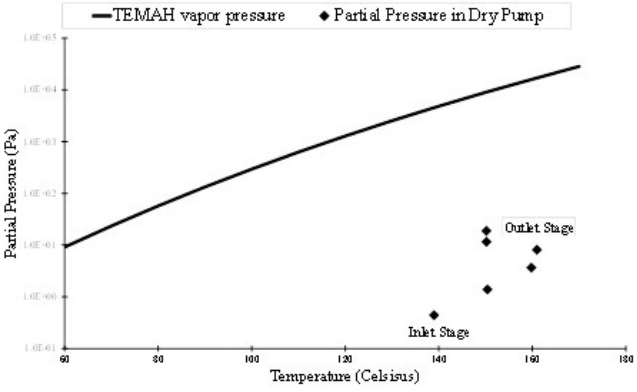



**FIGURE 4.** Vapor pressure of TEMAH (0.2 mg/min with 14 slm of nitrogen) and simulated vapor pressure of TEMAH in the dry pump, inlet to outlet.

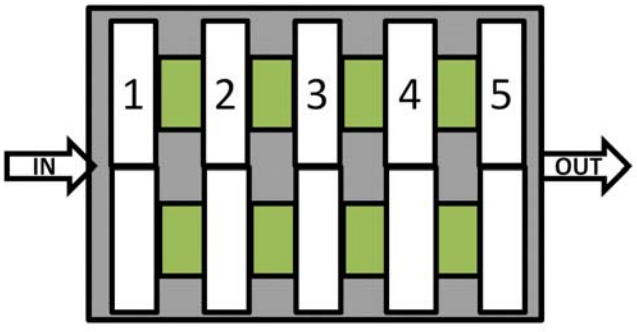



**FIGURE 5.** Schematic of the dry pump mechanism showing inlet (1st stage) to outlet (5th stage). Rotor sleeves are shown in green.

consistently repeatable, suggesting that factors upstream of the pump were also contributing to short service intervals. Powder loading varied between pumps and within the pumps, although the heaviest deposition was always located in the final stages of the dry pump. It is normal for the most deposition to occur near the exhaust of the pump because of the generally increased temperature of the exhaust gas and the increase in vapor pressure of the materials being pumped.

A diagram of the dry pump stages from inlet to outlet is shown in **FIGURE 5,** where the sleeves are also shown. Consistently, the final stage shaft sleeve, which is located between the 4th and 5th stage of the pump, was the weakest link in the design. Deposition would collect on the sleeve's surface. Resulting friction between the sleeve and the stator would cause the components to heat, expand, and finally seize the pump.

**FIGURE 6** shows the sleeves from between three

stages of a pump exchanged for service. Another example is shown in the right side picture of Fig. 1. The sleeves are steel with a PTFE coating, giving them a green color. Evidence of the deposition is clear in the shaft sleeves on the right side of the picture.

Extending pump service intervals

Inconsistencies in powder deposition that suggested variations in upstream conditions were ultimately traced to condensation in the gas lines to the process chamber. The amount of condensed liquid and the length of the flow step in the ALD cycle affected the amount of deposition. When the user took care to avoid condensation, a much more consistent pattern of deposition was observed within the pump.

For any particular dry pump, the two most convenient elements that can be adjusted are the nitrogen purge and the temperature of the pump. Adding purge, or changing the location of the purge, can affect the partial pressure of the gases being pumped. Purge can also affect the temperature of the gas being pumped. In this case the purge flow was already 76 slm and further increase could have affected the downstream gas abatement device.

Experiments to extend the MTBS focused on the pump running temperature. Temperature changes within the pump can dramatically affect the propensity of the pumped gases to condense on the internal surfaces of the pump as well as the rate of reactions of any gases being pumped. However,

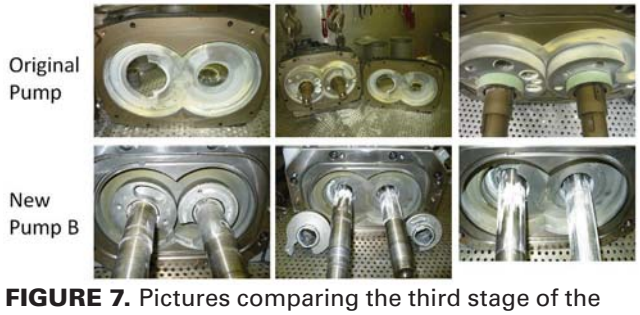



**FIGURE 7.** Pictures comparing the third stage of the original pump and New Pump B showing the different deposition patterns.

**TABLE 2.** New pump test results

| Pump | Purge Range | Tested Temperature Range | Service Interval |
|---|---|---|---|
| Original | 76 slm | 140–170°C | 30 day |
| New Pump A | 56 slm | 110–130°C | 120–190 day |
| New Pump B | 44 slm | 110°C | 120–190 day |

**FIGURE 6.** Picture of sleeves in an exchanged pump showing deposition on the outer surfaces.

varying the pump temperature from 140°C to nearly 180°C made any appreciable change to the service interval.

Finally, two pumps with designs that differed significantly from the original pump were evaluated. Additionally, new pump A provided significantly greater capacity at higher inlet pressures than new pump B, at the expense of greater power consumption. The results are shown in **TABLE 2**.

New Pump A was initially installed with a temperature set point of 130°C. It was removed after six months for inspection prior to failure. New Pump B was tested with a temperature set point of 110°C. It was removed after six months prior to failure. A comparison of the internal condition of the Original Pump and New Pump B is shown in **FIGURE 7**.

Four differences in the new pump design are believed to have contributed to improved reliability:

- 180% increase in rotational speed (180%), resulting in less residence time of the pumped gases.
- Reduced operating temperature. Although many semi¬conductor processes benefit from a hot pump, this ALD process does not.
- No rotor sleeve. The rotor sleeve in the new pumps was integrated with the rotor element itself. This not only removed the necessity for a coating, but appeared to strengthen the mechanism.
- Heated purge. The purge in

the new pumps is warmed to within 95% of the stator temperature to prevent cooling effects and reduce the chance of spontaneous condensation of gases.

Subsequent experience with a large number of pumps and customers has confirmed the advantages provided by the new pump design. New pump B is the recommended pump for this application with fixed service intervals varying between 4 and 6 months depending on the specific characteristics of the process supported.

## Conclusions

Deposition of high-k materials using ALD is a widely used technique for today's transistor and memory structures. At early introduction of the process in high volume manufacturing, pump reliability became a key concern. Careful analysis and cooperation with customers resulted in extending the service interval of the pumps from one to up to six months, an achievement that significantly reduced operating expenses and production losses due to wafer contamination and equipment downtime caused by unexpected pump failures. Analysis of the pump condition and test results showed that, more than temperature or purge, a different pump design provided the greatest improvement in service intervals. Design features that contributed most to the improved performance include increased rotational speed, integrated rotor sleeves, and increased purge injection temperature.

## References

1. J. M. et al., "Impact of Hf-precursor choice on scaling and performance of high-k gate dielectrics hf-based high-k materials," ECS Trans., p. 59, 2007.
2. X. L. et al., "Ald of hafnium oxide thin films from tetrakis (ethylmethylamino) hafnium and ozone," J. of ECS, vol. 152, 2005.
3. H. Furuya, "Formation of metal oxide film," Sep 2008, patent application: US20080226820 A1.
4. Y. S. et al., "Atomic layer deposition of hafnium oxide and hafnium silicate thin films using liquid precursors and ozone," J. Vac. Sci. Tech. A, vol. 22, 2004.

# Fab Managers Don't Like Surprises

**DAVID W. PRICE**, **DOUGLAS G. SUTHERLAND**, *KLA-Tencor, Milpitas, CA*

*Always quantify your lots at risk when making changes to your process control strategy.*

Nobody likes surprises—especially the managers of $10 billion factories. In a dynamic field like advanced semiconductor IC fabrication, there will always be unknowns. However, it is critical to know what you know and know what you don't know. Every measurement has error. The quality of the decision you make is highly dependent on the uncertainty in the data used to make that decision.

Process control spending is discretionary. Fabs will invest to the point that they believe the return on investment is favorable. It may make financial sense to sample less, skip certain measurements, or use a less capable inspection/metrology tool. However, the fab must always face facts and quantify the level of risk associated with these decisions. The stakes—missing an excursion resulting in costly yield loss—are too high to live in denial.

The fourth fundamental truth of process control for the semiconductor IC industry is:

**Always quantify your lots at risk when making changes to your process control strategy**

Quantifying your lots at risk equates to understanding the uncertainty in your measurement. This is a basic concept that most factory engineers learned at some point during their education, however, it is also one of the most tedious of tasks. As a result, this portion of the analysis is skipped more often than we care to admit.

Within process control there are really only two types of risk: Alpha risk and Beta risk. Alpha risk is a false alarm; it is when your inspection tells you that the wafer measured is out of control when really there is nothing wrong with the larger process. Beta risk is the opposite of this; it is when your inspection tells you that the wafer you measured was in control but really there is a serious problem. **FIGURE 1** summarizes the difference.

| | | Observed | |
|---|---|---|---|
| | | In Control | Out of Control |
| Actual | In Control | ✓ | Alpha Risk |
| | Out of Control | Beta Risk | ✓ |

**FIGURE 1.** Definition of Alpha risk and Beta Risk.

Alpha and Beta risk arise as a result of the inability to consistently make an inspection that accurately represents the process at that point in time. The best way to reduce both types of risk is to make the process itself less variable. There are few, if any, activities in semiconductor manufacturing that are more value-added than driving variability out of the process. It is much easier to spot real changes in the process when the native lot-to-lot variation is low. However, this cannot always be easily achieved and the Alpha risk (the number of false alarms) can sometimes only be reduced by moving the control limits further from the target (raising the upper control limit and / or lowering the lower control limit). Increasing the spread between the control limits will reduce the Alpha risk but it comes at the expense of increasing the Beta risk—it makes the inspection process less sensitive to real excursions.

Just as changing the native variability in the process usually warrants reassessing where to place the control limits, any time the characteristics of the measurement itself are changed (changing the sensitivity of the recipe, changing the area of the wafer that is inspected, changing the size of the review sample, etc.) the position of the control limits also needs to be re-evaluated.

**DR. DAVID W. PRICE** *and* **DR. DOUGLAS SUTHERLAND** *are senior director and principal scientist, respectively, at KLA-Tencor Corp., Milpitas, CA.*

As an example, consider a defect inspection step where 100 percent of the wafer area is inspected. For a particular defect of interest (DOI) the inspection finds between 40 and 60 DOI on each wafer under normal conditions and the upper control limit (UCL) is placed at 61. If the inspection strategy is changed such that further inspections will only sample 50 percent of the wafer area, the range of normal values will change from between 40 and 60 to between 12 and 42 for 50 percent area (or 24 and 84 when normalized back to the full wafer count). The increase in range is a result of the Binomial Probability Theory that quantifies the effect that sometimes there will be a disproportionate number of DOI in the area that was inspected and sometimes there will be a disproportionate number of DOI in the area that was not inspected.

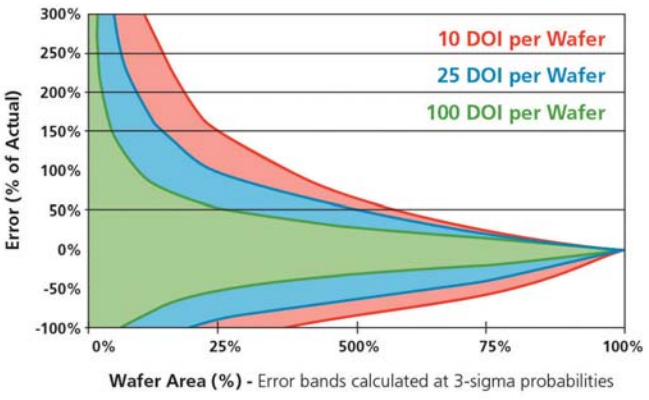



**FIGURE 2.** Percent Error versus Wafer Area for three different DOI counts. At 100 percent area there is no error introduced into the measurement. As the area decreases, the error increases. The error is largest for low DOI counts and is bounded by -100% on the low side and unbounded on the high side.

With the stroke of a pen, the decision to reduce the wafer area to 50 percent has tripled the variability in this particular part of the process from a range of 20 to a range of 60 DOI per wafer. In doing so, they have undone months of hard work by a team of engineers who worked diligently to drive the variability out of the process in the first place. The fab manager must now choose to keep the UCL at 61 and suffer many more false alarms or raise the UCL to 85 where they will have approximately the same number of false alarms but be much less sensitive to real excursions.

The impact of changing the inspected wafer area depends on several factors including the average DOI, the native variation and the size of the excursion that one is trying to detect. **FIGURE 2** shows how the percent error changes as a function of wafer area for three different DOI counts.

We have chosen the example of wafer area to illustrate the point because it is such a common practice but the same principles apply to all aspects of process control. The measurement is part of the process— **when you degrade the quality of the measurement you degrade the quality of the process.**

There are many ways in which process control risk manifests itself in the fab. One simple approach is to get in the habit of asking the questions: "how many lots are at risk if I do this?" and, "what are the error bars on this analysis?"

For example, how many lots are at risk if the fab:

- Skips an inspection step?
- Uses a less sensitive inspector or pixel size?
- Reduces the sampling rate?
- Use a less precise metrology tool?
- Measure fewer features per wafer?

Changing process control strategy to reduce costs may seem like a short term solution but it is seldom if ever sustainable for one very simple reason: fab managers don't like surprises!

## References

1. You Can't Fix What You Can't Find, Solid State Technology, July 2014
2. Sampling Matters, Semiconductor Manufacturing and Design, September 2014
3. The Most Expensive Defect, Solid State Technology, December 2014

*Author's Note: This is the fourth in a series of 10 installments that explore fundamental truths about process control—defect inspection and metrology—for the semiconductor industry. Each article introduces one of the 10 fundamental truths and highlights their implications. Within this article we will use the term inspection to imply either defect inspection or a parametric measurement such as film thickness or critical dimension (CD).*

# Techniques for Simplifying Pulsed Measurements: Part 1

**DAVID WYBAN**, *Keithley Instruments, a Tektronix Company, Solon, Ohio*

*Pulsed measurements are defined in Part 1, and common pulsed measurement challenges are discussed in Part 2.*

Performing a DC measurement starts with applying the test signal (typically a DC voltage), then waiting long enough for all the transients in the DUT and the test system to settle out. The measurements themselves are typically performed using a sigma-delta or integrating-type analog-to-digital converter (ADC). The conversion takes place over one or more power line cycles to eliminate noise in the measurements due to ambient power line noise in the test environment. Multiple measurements are often averaged to increase accuracy. It can take 100ms or longer to acquire a single reading using DC measurement techniques.

In contrast, pulsed measurements are fast. The test signal is applied only briefly before the signal is returned to some base level. To fit measurements into these short windows, sigma-delta ADCs are run at sub-power-line interval integration times; sometimes, the even faster successive approximation register (SAR) type ADCs are used. Because of these high speeds, readings from pulsed measurements are noisier than readings returned by DC measurements. However, in on-wafer semiconductor testing, pulse testing techniques are essential to prevent device damage or destruction. Wafers have no heat sinking to pull away heat generated by current flow; if DC currents were used, the heat would increase rapidly until the device was destroyed. Pulse testing allows applying test signals for very short periods, avoiding this heat buildup and damage.

## Why use pulsed measurements?

The most common reason for using pulsed measurements is to reduce joule heating (i.e., device self-heating). When a test signal is applied to a DUT, the device consumes power and turns it into heat, increasing the device's temperature. The longer that power is applied, the hotter the device becomes, which affects its electrical characteristics. If a DUT's temperature can't be kept constant, it can't be characterized accurately. However, with pulsed testing, power is only applied to the DUT briefly, minimizing self-heating. Duty cycles of 1 percent or less are recommended to reduce the average power dissipated by the device over time. Pulsed measurements are designed to minimize the power applied to the device so much that its internal temperature rise is nearly zero, so heating will have little or no effect on the measurements.

Because they minimize joule heating, pulsed measurements are widely used in nanotechnology research, such as when characterizing delicate materials and structures like CNT FETs, semiconductor nanowires, graphene-based devices, molecular-based electronics and MEMs structures. The heat produced with traditional DC measurement techniques could easily alter or destroy them.

To survive high levels of continuous DC power, devices like MOSFETs and IGBTs require packaging with a solid metal backing and even heat-sinking. However, during the early stages of device

**EGBERT WOELK, PH.D.**, *is director of marketing at Dow Electronic Materials, North Andover, MA.* **ROGER LOO, PH.D.**, *is a principal scientist at imec, Leuven, Belgium.*

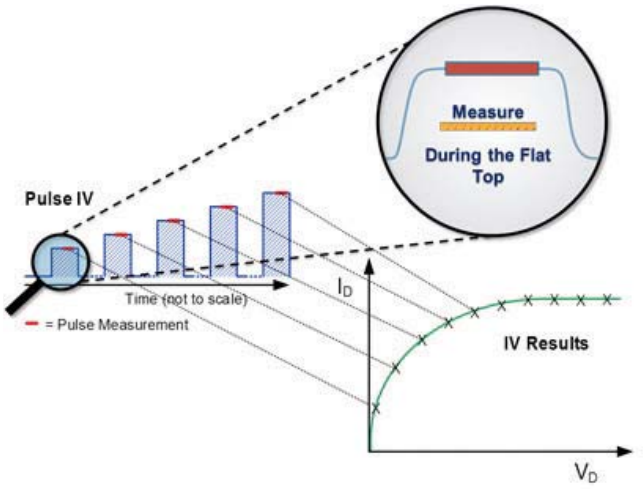



**FIGURE 1.** Pulse I-V technique.

development, packaging these experimental devices would be much too costly and time consuming, so early testing is performed at the wafer level. Because pulsed testing minimizes the power applied to a device, it allows for complete characterization of these devices on the probe station, reducing the cost of test.

The reduction in joule heating that pulsed testing allows also simplifies the process of characterizing devices at varying temperatures. Semiconductor devices are typically so small that it is impossible to measure their temperature directly with a probe. With pulsed measurements, however, the self-heating of the device can be made so insignificant that its internal temperature can be assumed to be equal to the surrounding ambient temperature. To characterize the device at a specific temperature, simply change the surrounding ambient temperature with a thermal chamber or temperature-controlled heat sink. Once the device has reached thermal equilibrium at the new ambient temperature, repeat the pulsed measurements to characterize the device at the new temperature.

Pulsed measurements are also useful for extending instruments' operating boundaries. A growing number of power semiconductor devices are capable of operating at 100A or higher, but building an instrument capable of sourcing this much DC current would be prohibitive. However, when delivering pulse mode power, these high power outputs are only for very short intervals, which can be done by storing the required energy from a smaller power supply within capacitors and delivering it all in one short burst. This allows instruments like the Model 2651A High Power SourceMeter® SMU instrument to combine sourcing up to 50A with precision current and voltage measurements.

## Pulsed I-V vs. transient measurements

Pulsed measurements come in two forms, *pulsed I-V* and *transient*. Pulsed I-V (**FIGURE 1**) is a technique for gathering DC-like current vs. voltage curves using pulses rather than DC signals. In the pulsed I V technique, the current and voltage is measured near the end of the flat top of the pulse, before the falling edge. In this technique, the shape of the pulse is extremely important because it determines the quality of the measurement. If the top of the pulse has not settled before this measurement is taken, the resulting reading will be noisy and or incorrect. Sigma-delta or integrating ADCs should be configured to perform their conversion over as much of this flat top as possible to maximize accuracy and reduce measurement noise.

Two techniques can improve the accuracy of pulsed I-V measurements. If the width of the pulse and measurement speed permit, multiple measurements made during the flat portion of the pulse can be averaged together to create a "spot mean" measurement. This technique is commonly employed with instruments that use high speed Summation Approximation Register (SAR) ADCs, which perform conversions quickly, often at rates of 1µs per sample or faster, thereby sacrificing resolution for speed. At these high speeds, many samples can be made during the flat portion of the pulse. Averaging as many samples as possible enhances the resolution of the measurements and reduces noise. Many instruments have averaging filters that can be used to produce a single reading. If even greater accuracy is required, the measurement can be repeated over several pulses and the readings averaged to get a single reading. To obtain valid results using this method, the individual pulsed measurements should be made in quick succession to avoid variations in the readings due to changes in temperature or humidity.

Transient pulsed measurements (**FIGURE 2**) are performed by sampling the signal at high speed to create a signal vs. time waveform. An oscilloscope is often used for these measurements but they can also be made with traditional DC instruments by running the ADCs at high speed. Some DC instruments even include high-speed SAR type ADCs for performing transient pulsed measurements. Transient measurements are useful for investigating device behaviors like self-heating and charge trapping.

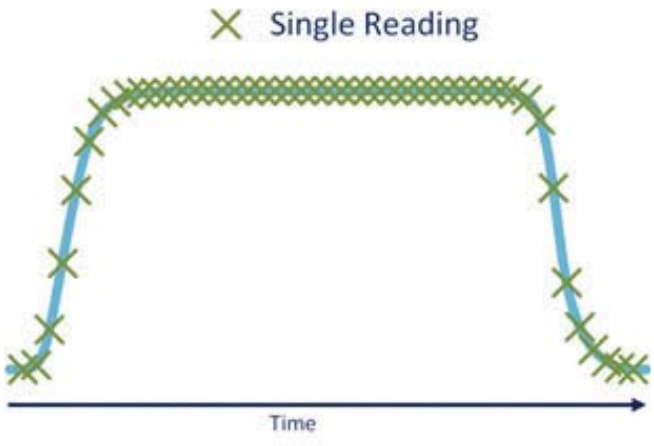



**FIGURE 2.** Transient pulse measurements.

## Instrumentation options

The simplest pulse measurement instrumentation option is a ***pulse generator to source the pulse combined with an oscilloscope to measure the pulse*** (**FIGURE 3**). Voltage measurements can be made by connecting a probe from the scope directly to the DUT; current measurements can be made by connecting a current probe around one of the DUT test leads. If a current probe is unavailable, a precision shunt resistor can be placed in series with the device and the voltage across the shunt measured with a standard probe, then converted to current using a math function in the scope. This simple setup offers a variety of advantages. Pulse generators provide full control over pulse width, pulse period, rise time and fall time. They are capable of pulse widths as narrow as 10 nanoseconds and rise and fall times as short as 2-3 nanoseconds. Oscilloscopes are ideal for transient pulse measurements because of their ability to sample the signal at very high speeds.

Although a simple pulse generator/oscilloscope combination is good for fast transient pulse measurements, it's not appropriate for all pulse measurement applications. A scope's measurement resolution is relatively low (8–12 bits). Because scopes are designed to capture waveforms, they're not well suited for making pulse I-V measurements. Although the built-in pulse measure functions can help with measuring the level of a pulse, this represents only a single point on the I-V curve. Generating a complete curve with this setup would be time consuming, requiring either manual data collection or a lot of programming. Pulse generators are typically limited to outputting 10-20V max with a current delivery capability of only a couple hundred milliamps, which would limit this setup to lower power devices and/or lower power tests. Test setup can also be complex. Getting the desired voltage at the device requires impedance matching with the pulse generator. If a shunt resistor is used to measure current, then the voltage drop across this resistor must be taken into account as well.

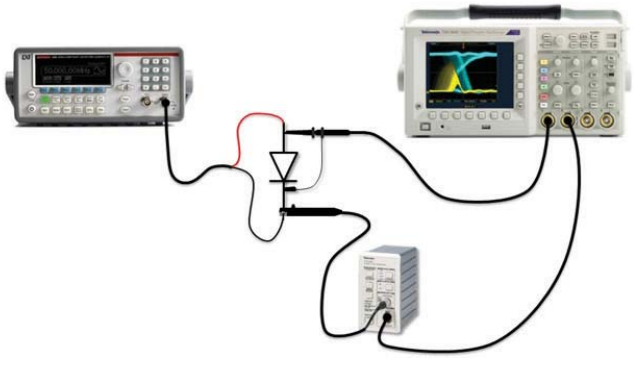


**FIGURE 3.** Pulse measurement using a pulse generator and an oscilloscope. Voltage is measured across the device with a voltage probe and current through the device is measured with a current probe.

***Curve tracers*** were all-in-one instruments designed specifically for I-V characterization of 2- and 3-terminal power semiconductor devices. They featured high current and high voltage supplies for stimulating the device and a configurable voltage/current source for stimulating the device's control terminal, a built-in test fixture for making connections, a scope like display for real-time feedback, and a knob for controlling the magnitude of the output. However, ***Source measure unit (SMU) instruments***

(**FIGURE 4**) have now largely taken up the functions they once performed.

SMU instruments combine the source capabilities of a precision power supply with the measurement capabilities of a high accuracy DMM. Although originally designed for making extremely accurate DC measurements, SMU instruments have been enhanced to include pulse measurement capabilities as well. These instruments can source much higher currents in pulse mode than in DC mode. For example, the Keithley Model 2602B SourceMeter® SMU instrument can output up to 3A DC and up to 10A pulsed. For applications that require even high currents, the Model 2651A SourceMeter® SMU instrument can output up 20A DC or 50A pulsed. If two Model 2651As are configured in parallel, pulse current outputs up to 100A are possible.

SMU instruments can source both voltage and current with high accuracy thanks to an active feedback loop that monitors the output and adjusts it as necessary to achieve the programmed output value. They can even sense voltage remotely, directly at the DUT, using a second set of test leads, ensuring the correct voltage at the device. These instruments measure with high precision as well, with dual 28-bit delta-sigma or integrating-type ADCs. Using these ADCs along with their flexible sourcing engines, SMUs can perform very accurate pulse I-V measurement sweeps to characterize devices. Some, including the Model 2651A, also include two SAR-type ADCs that can sample at 1 mega-sample per second with 18-bit resolution, making them excellent for transient pulse measurements as well.

**FIGURE 4.** Model 2620B System SourceMeter SMU instrument.

In addition, some SMU instruments offer excellent low current capability, with ranges as low as 100pA with 100aA resolution. Their wide dynamic range makes SMU instruments an excellent choice for both ON- and OFF-state device characterization. Also, because they combine sourcing and measurement in a single instrument, SMU instruments reduce the number of instruments involved, which not only simplifies triggering and programming but reduces the overall cost of test.

Although SMU instruments are often used for pulse measurements, they don't operate in the same way as a typical pulse generator. For example, an SMU instrument's rise and fall times cannot be controlled by the user; they depend on the instrument's gain and bandwidth of the feedback loop. Because these loops are designed to generate little or no overshoot when stepping the source, the minimum width of the pulses they produce are not as short as those possible from a pulse generator. However, an SMU instrument can produce pulse widths as short as 50–100µs, which minimizes device self-heating.

The terminology used to describe a pulse when using SMU instruments differs slightly from that used with pulse generators. Rather than referring to the output levels in the pulse as amplitude and base or the high level and the low level, with SMU instruments, the high level is referred to as the *pulse level* and the low level as the *bias level*. The term *bias level* originates from the SMU's roots in DC testing where one terminal of a device might be biased with a fixed level. Pulse width is still used with SMU instruments, but its definition is slightly different. Given that rise and fall times cannot be set directly and vary with the range in use and the load connected to the output, pulse width can't be accurately defined by Full Width at Half Maximum (FWHM). (refer to the sidebar for more information on FWHM). Instead, for most SMU instruments, pulse width is defined as the time from the start of the rising edge to the start of the falling edge, points chosen because they are under the user's control. In other words, the user can set the pulse width by setting the time between when the source is told to

go to the pulse level and then told to go back to the bias level.

***Pulse measure units*** (PMUs) combine the capabilities of a pulse generator and a high-resolution oscilloscope, which are sometimes implemented as card-based solutions designed to plug into a test mainframe. Keithley's Model 4225-PMU, designed for use with the Model 4200 Semiconductor Characterization System (**FIGURE 5**), is one example. It has two independent channels capable of sourcing up to 40V at up to 800mA. Like a standard pulse generator, users can define all parameters of the pulse shape. Pulse widths as narrow as 60ns and rise and fall times as short as 20ns make it well suited for characterizing devices with fast transients. A Segment Arb mode allows outputting multi-level pulse waveforms in separately defined segments, with separate voltage levels and durations for each. Each PMU channel is capable of measuring both current and voltage using two 14-bit 200MS/s ADCs per channel for a total of four ADCs per card. Additionally, all four ADCs are capable of sampling together synchronously at full speed. By combining a pulse generator with scope-like measurement capability in one instrument, a PMU can not only make high-resolution transient pulse measurements but also perform pulse I V measurement sweeps easily using a spot mean method for enhanced resolution. ◆


**FIGURE 5.** A pulse measure unit card combines the capabilities of a pulse generator and a high resolution oscilloscope.

Solid State TECHNOLOGY

EXECUTIVE OFFICES

**Extension Media** 1786 18th Street, San Francisco, CA 94107-2343.

ADVERTISING

**Sales Manager**
**Kerry Hoffman**
1786 18th St.
San Francisco,CA 94107-2343
Tel: 978.580.4205;
e-mail: khoffman@extensionmedia.com

**North America**
**Kerry Hoffman**
Tel: 978.580.4205
khoffman@extensionmedia.com

**Germany, Austria, E. Switzerland & E. Europe**
**Holger Gerisch**
Tel: +49.0.8801.9153791
holgerg@pennwell.com

**China, Hong Kong**
**Adonis Mak**
Tel:+852.90182962
adonism@actintl.com.hk

**Taiwan**
**Diana Wei**
Tel: +886.2.23965128 ext: 270
diana@arco.com.tw

**Rest of World**
**Kerry Hoffman**
Tel: 978.580.4205
khoffman@extensionmedia.com

**The ConFab and Webcasts**
**Sabrina Straub**
Tel: 603.770.6569
sstraub@extensionmedia.com

## ad index

# Security should not be hard to implement

Data is ubiquitous today. It is generated, exchanged and consumed at unprecedented rates.

According to Gartner, Internet of Things connected devices (excluding PCs, tablets and smart phones) will grow to 26 billion devices worldwide by 2020—a 30-fold increase from 2009. Sales of these devices will add $1.9 trillion in economic value globally.

Indeed, one of the major benefits of the Internet of Things movement is the connectivity and accessibility of data; however, this also raises concerns about securely managing that data.

## Managing data security in hardware

Data security involves essential steps of authentication and encryption. We need to authenticate data generation and data collection sources, and we need to preserve the privacy of the data.

The Internet of Things comprises a variety of components: hardware, embedded software and services associated with the "things." Data security is needed at each level.

Hardware security is generally implemented in the chips that make up the "things." The mathematical security of authentication and encryption algorithms is less of a concern because this is not new. The industry has addressed these concerns for several years.

Nonetheless, hackers can exploit implementation flaws in these chips. Side channel attacks (SCAs) are a major threat to data security within integrated circuits (ICs) that are used to hold sensitive data, such as identifying information and secret keys needed for authentication or encryption algorithms. Specific SCAs include differential power analysis (DPA) and differential electro magnetic analysis (DEMA).

There are many published and unpublished attacks on the security of chips deployed in the market, and SCA threats are rapidly evolving, increasing in potency and the ease of mounting the attacks.

These emerging threats render defensive techniques adopted by the IC manufacturers less potent over time, igniting a race between defensive and offensive (threat) techniques. For example, chips that deploy defensive techniques deemed sufficient in 2012 may be less effective in 2014 due to emerging threats. Once these devices are deployed, they become vulnerable to new threats.

Another challenge IC manufacturers face is the complexity of defensive techniques. Often times, defensive techniques that are algorithm or protocol specific are layered to address multiple targeted threats.

This "Band-Aid" approach is tedious and becomes unwieldy to manage. The industry must remember that leaving hardware vulnerable to SCA threats can significantly weaken data security. This vulnerability may manifest itself in the form of revenue loss (counterfeits of consumables), loss of privacy (compromised identification information), breach of authentication (rogue devices in the closed network) and more.

## How to increase the permanence of security

A simplified way to look at the SCA problem is as a signal to noise issue. In this case, signal means sensitive data leaked through power signature. Noise is the ambient or manufactured noise added to the system to obfuscate the signal from being extracted from power signature.

Many defensive measures today concentrate on increasing noise in the system to obfuscate the signal. The challenge with this approach is that emerging statistical techniques are becoming adept at separating the signal from the noise, thereby decreasing the potency of the deployed defensive techniques.

One way to effectively deal with this problem is to "weave security into the fabric of design." SCA threats can be addressed at the source rather than addressing the symptoms. What if we can make the power signature agnostic of the data processed? What if we can build security into the building blocks of design? That would make the security more permanent and simplify its implementation.

A simplified approach of weaving security into the fabric of design involves leveraging a secure standard cell library that is hardened against SCA. Such a library would use analog design techniques to tackle the problem of SCA at the source, diminishing the SCA signal to make it difficult to extract from the power signature.

Leveraging standard cells should be simple since they are the basic building blocks of digital design. As an industry, we cannot afford to bypass these critical steps to defend our data. ◆

**CHOWDARY YANAMADALA,** *Senior Vice President of Business Development, ChaoLogix, Gainesville, FL*