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P. 12

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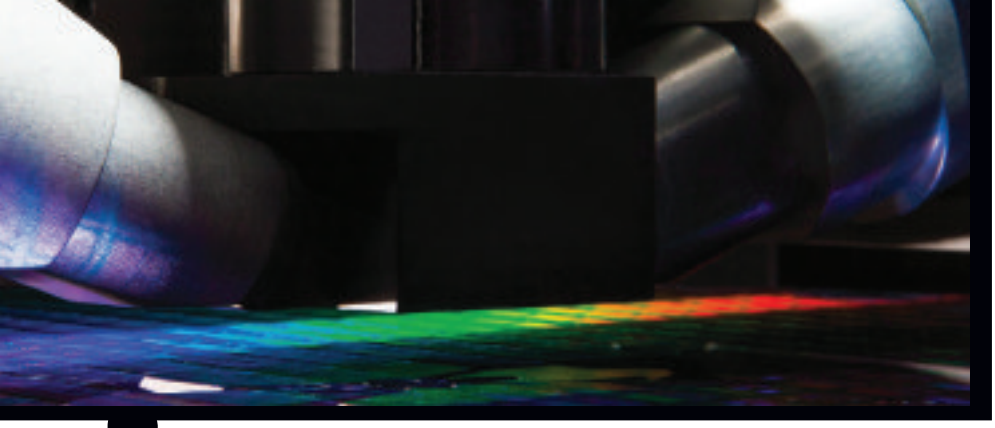

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JANUARY/FEBRUARY 2016 VOL. 59 NO. 1

KLA-Tencor Corp. offers two advanced metrology systems that support the development and production of 16nm and below IC devices: Archer™ 500LCM and SpectraFilm™ LD10.

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editorial

Does Consolidation Put Innovation at Risk?

Consolidation in the semiconductor industry continues apace, with more than $100 billion in mergers and acquisitions announced in 2015, and more to come in 2016 (versus $62.6 billion of 2010 to 2014 combined). "With our industry growth rates being so low, it's a lot cheaper to acquire market share than it is to invest and beat your competitor over the head," said analyst Bill McClean, speaking at SEMI's Industry Strategy Symposium (ISS) in January.

One potentially negative impact of consolidation is reduced innovation, said Ivo J. Raaijmakers, Chief Technology Officer and Director of R&D at ASM International, speaking at ISS on consolidation in the equipment supplier market. "The tail has been cut off. A lot of innovation happens in this tail," he said. "The question we have to ask ourselves is how can we ensure efficient innovation in such a consolidating landscape of equipment suppliers?"

The challenge is compounded by exponentially increasing chip complexity and R&D spending, along with rapid increases in material diversity.

Raaijmakers provided an equation that captures the mathematics of innovation:

$$dI/dt \; \alpha \; I \times \eta/\tau$$

where I is the number of innovations being worked on: loosely relates to R&D budget

η is the average success rate: what fraction of projects are successful, and

τ is the time constant: how long does it take from innovation to production

He noted that Industry consolidation lowers the number of innovation projects, the success rate decreases with complexity, and development time increases with complexity. "We are in deep trouble, unless we manage η and τ," Raaijmakers said.

There's not much hope in reducing the time constant. New developments have historically taken 7-10 years on average from conception to high volume production. "Can we decrease this by collaboration along the value chain? I think it will be difficult and if you can do it, it will not be a huge gain," Raaijmakers said.

On the other hand, there's much to be gained by increasing the efficiency factor, and collaboration can be effective here. "Collaboration along the innovation chain can significantly lower the risk of adoption, increase the success rate, and may increase the speed," Raaijmakers said. "Are we all working on the right things to push through into manufacturing? How quickly can you narrow down choices?"

Raaijmakers said a company needs to be ambidextrous. "You have to be good at taking things into volume production and supporting it there. And you have to be good in R&D. Maintaining those two traits is not so easy," he concluded.

—Pete Singer, Editor-in-Chief

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Web Exclusives

A year in review: A look back at the top stories from 2015

Historic consolidation, new collaborations around new scaling limitations, and big ideas on the development of the Internet of Things are just a few of the topics our readers couldn't get enough of in 2015.

http://bit.ly/1SjjX1u

Packaging conference addresses challenges, opportunities in new technologies

On the second day of the 12th annual 3D ASIP conference, the heavy hitters came out to talk. Attendees heard presentations from executives of Amkor Technology, the Defense Advanced Research Projects Agency (DARPA), Northrop Grumman, Taiwan Semiconductor Manufacturing, Teledyne Scientific & Imaging, and Xilinx, among other companies. (From SemiMD.com)

http://bit.ly/1KecV6l

What to expect in 2016 in the chipworld

This might seem to be a bit like fortune-telling, but it's actually a compilation of the notes we've made from this year's press announcements, coupled with the trends we've observed and keeping an open ear at the industry events that we've attended.

http://bit.ly/1ZloWOo

Koyanagi and Ramm win 3DIC Pioneering Award

At the 12th annual 3D ASIP [Architectures for Semiconductor Interconnect and Packaging] Conference, sponsored by RTI Int, in Redwood City CA, Professor Mitsumasa Koyanagi of Tohoku University and Dr. Peter Ramm of Fraunhofer EMFT were the conference's first recipients of the "3DIC Pioneer Award."

http://bit.ly/1Zlr7RQ

Dow, DuPont to merge in combination of chemical giants

In a deal with significant implications for high-tech chemicals and materials, The Dow Chemical Company and E. I. du Pont de Nemours and Company (DuPont) have agreed to merge, forming the second largest chemical company in the world, behind BASF SE. (From SemiMD.com)

http://bit.ly/1RNPoiT

n&b news and blogs

A wild ride in 2015 – and two steps forward in 2016

2015 will be remembered for a wild ride that fundamentally changed the industry. In 2015 a wave of M&A activity swept across the industry supply chain — unlike any single year before — with scores of transactions and notable multi-billion dollar companies being absorbed. In 2016, we all will be working within a newly reconfigured supply chain.

http://bit.ly/1Oj2eTV

The first degree – Ominous threshold reached

The Met Office, the UK's official office of meteorology, recently announced that, based on data acquired over the first 9 months of the year, 2015 is likely to be the first year in which the average global temperature exceeds by more than 1°Celcius (C), the average temperature for preindustrial years before we began to burn significant amounts of fossil fuels.

http://bit.ly/1njPNOV

Intel/Micron detail their 3D-NAND at IEDM

On the Monday afternoon at IEDM the key paper was the Intel/Micron talk on their 3D-NAND flash part (paper 3.3), which is currently sampling to customers. Samsung put their V-NAND flash on the market last year, but that uses charge-trap technology, whereas the Intel/Micron device has adapted conventional floating gate technology to the vertical direction.

http://bit.ly/1TWt59W

Insights from the Leading Edge: A Comeback for WLP in IoT

IMAPS 2015, also known as the 48th International Symposium on Microelectronics, was held in Orlando, Fl. There were 30 sessions, more than 150 presentations and more than 135 exhibit booths. Certainly, in terms of microelectronic packaging, this is the largest annual exhibition in the USA. Dr. Phil Garrou blogs on a number of the presentations that stood out during this symposium.

http://bit.ly/1RmsosP

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news

worldnews

USA – **GlobalFoundries** announced the availability of FX-14, an application-specific integrated circuit offering built on the company's next-generation 14nm FinFET process technology.

USA - **Micron Technology, Inc.** announced that President Mark Adams will resign for personal health reasons. He will remain with the company until February 1, 2016, to support the transition.

ASIA - **TSMC** submitted an application to the Investment Commission of Taiwan's Ministry of Economic Affairs for an investment project to build a wholly-owned 12-inch wafer manufacturing facility and a design service center in Nanjing, China.

USA – **Fairchild Semiconductor** received an unsolicited proposal from **China Resources Microelectronics,** which is expected to result in a "superior proposal," as defined in the agreement and plan of merger with **ON Semiconductor**.

EUROPE - **imec** demonstrated the integration of high mobility InGaAs as a channel material for 3D vertical NAND memory devices formed in the plug (holes) with the diameter down to 45nm.

USA - Two **GLOBALFOUNDRIES** engineers, one in New York and one in Vermont, have been designated as IEEE Fellows by the Institute of Electrical and Electronics Engineers.

ASIA - **Mattson Technology** agreed to be acquired by **Beijing E-Town Dragon Semiconductor Industry Investment Center**, a limited partnership in China, for about $300 million in cash.

EUROPE - **Leti** announced the development of local-strain techniques in FD-SOI fabrication to improve next-generation performance.

ASIA – **TowerJazz** announced the signing of a definitive agreement with **Semiconductor Laboratory**, an Asian governmental agency. Under the agreement, TowerJazz will leverage its manufacturing expertise and assets while providing during the coming three years the required process engineering and equipment maintenance support for successful operation of the facility.

USA - **Ferrotec** received multiple orders of e-beam evaporator systems from **WIN Semiconductors**.

Worldwide semiconductor revenue declined 1.9% in 2015, Gartner reports

Worldwide semiconductor revenue totaled $333.7 billion in 2015, a 1.9 percent decrease from 2014 revenue of $340.3 billion, according to preliminary results by Gartner, Inc. The top 25 semiconductor vendors' combined revenue increased 0.2 percent, which was more than the overall industry's growth. The top 25 vendors accounted for 73.2 percent of total market revenue, up from 71.7 percent in 2014.

"Weakened demand for key electronic equipment, the continuing impact of the strong dollar in some regions and elevated inventory are to blame for the decline in the market in 2015," said Sergis Mushell, research director at Gartner. "In contrast to 2014, which saw revenue growth in all key device categories, 2015 saw mixed performance with optoelectronics, nonoptical sensors, analog

Continued on page 8

Samsung, TSMC remain tops in available wafer fab capacity

IC Insights has released its Global Wafer Capacity 2016-2020 report that provides in-depth detail and analysis of IC industry capacity by wafer size, by process geometry, by region, and by product type. The new report provides a ranking of the industry's 25 largest IC manufacturers in terms of installed capacity as of December 2015. The top 10 capacity leaders are shown in Figure 1. Among the world's top 10 capacity leaders in 2015 were four companies headquartered in North America, two companies based in South Korea and in Taiwan, and one company each from Europe and Japan. The list includes the world's four largest memory suppliers, three largest foundries, the largest microprocessor supplier, and Texas Instruments and ST—the two biggest suppliers of analog ICs.

Collectively, the top 10 leaders had installed capacity of 11,737K wafers/month at the end of the year, which equates to 72% of global capacity and up slightly from 10,885K wafers/month or 71% in 2014.

- As of December 2015, Samsung had the most installed wafer capacity with 2.5 million 200mm-equivalent wafers per month, which represented 15.5% of the world's total capacity with most of it used for the fabrication of DRAM and flash memory devices.
- Second in line was the largest pure-play foundry in the world TSMC with about 1.9 million wafers per month capacity, or 11.6% of total worldwide capacity.
- Micron substantially increased its available capacity in recent years primarily through acquiring existing capacity from others. With the addition of the Elpida and Rexchip fabs as well as the extra Inotera capacity, Micron first became the third-largest wafer capacity holder in the world in 2013. Micron had the sixth-largest amount of wafer capacity in 2012, and in the beginning of that year the company acquired Intel's stake in two IM Flash Technologies fabs, giving Micron access to all the capacity from those fabs.
- The fourth-largest capacity holder at the end of 2015 was Toshiba with about 1.3 million in monthly wafer capacity (8.2% of total worldwide capacity), including a substantial amount of flash memory

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Stanford researchers advance area selective ALD to develop more energy efficient electronics

Stanford University researchers sponsored by Semiconductor Research Corporation (SRC) have developed a new area selective atomic layer deposition (ALD) process that promises to accelerate the manufacturing of higher performing, more energy efficient semiconductors.

It is well known that next-generation electronic, optoelectronic and sensing devices that contain nanoscale dimensions face increasingly difficult materials and fabrication challenges as the downward scaling of these devices continues. Conventional semiconductor manufacturing processes are time-consuming and expensive, in part due to the need for lithographic patterning. The Stanford research leverages simple ALD and etching processes that eliminate this lithography step and improve selective deposition of dielectric materials by more than 10 times in film thickness compared to similar advanced processes.

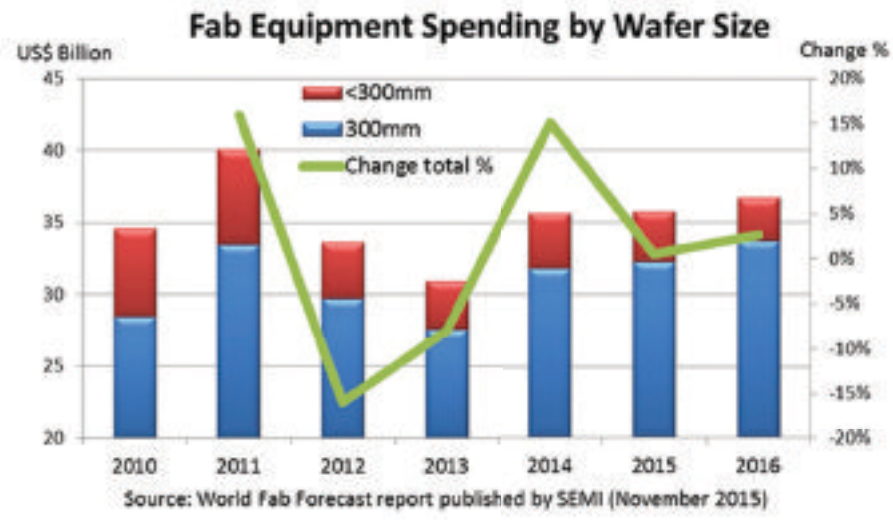
Due to difficulties of current top-down fabrication processes that contain multiple deposition, lithography and etching steps, along with problems with misalignment in lithography, using an alternative approach in which the desired materials are directly and selectively deposited would significantly facilitate the process, according to the Stanford team.

"Our technology is a promising candidate for overcoming the challenges of top-down processing and misalignment because it greatly improves the ability to perform selective deposition of materials. This research introduces a novel processing method to meet the increasingly difficult materials challenges associated with new devices," said Dr. Stacey Bent, Department of Chemical Engineering Chair and Jagdeep and Roshni Singh Professor in School of Engineering, Stanford University.

Continued on page 9

Fab equipment spending: Look for upward swing into 2016

Worldwide semiconductor fab equipment capital expenditure growth (new and used) for 2015 is expected to be 0.5 percent (total capex of US$35.8 billion), increasing another 2.6 percent (to a total of $36.7 billion) in 2016, according to the latest update of the quarterly SEMI World Fab Forecast report.



SEMI reports that in 2015, Korea outspent all other countries ($9.0 billion) on front-end semiconductor fab equipment, and is expected to drop to second place in 2016 as Taiwan takes over with the largest capex spending at $8.3 billion. In 2015, Americas ranked third in overall regional capex spending with about $5.6 billion and is forecast to increase only slightly to (5.1 percent) in 2016.

In 2015, 80 to 90 percent of fab equipment spending went to 300mm fabs, while only 10 percent was for 200mm or smaller. SEMI's recently published Global 200mm Fab Outlook provides more detail about past and future 200mm activities.

Examining fab equipment spending by product type, Memory accounts for the largest share in 2015 and 2016. While 2015's spending was dominated by DRAM, the SEMI World Fab Forecast reports that 2016 will be dominated by Flash, mainly 3D-related architectures. Capacity for 3D-NAND will continue to surge. SEMI's report tracks 10 major 3D producing facilities, with a capacity expansion of 47 percent in 2015 and 86 percent in 2016.

The Foundry segment is next in terms of the largest share of fab equipment spending in 2015 and 2016. In general, the foundry segment shows steadier, more predictable spending patterns than other device product segments. Coming in third place in fab equipment spending, MPU had lower spending in 2015. Logic spending was very strong in 2015, with 90 percent growth, driven by SONY's CMOS image sensors.

Throughout 2015, SEMI anticipates that there will be 1,167 facilities worldwide investing in semiconductor equipment in 2016, including 56 future facilities across industry segments from Analog, Power, Logic, MPU, Memory, and Foundry to MEMS and LEDs facilities. For further details, please reference to the latest edition of SEMI's World Fab Forecast report.

NXP and Freescale announce completion of merger

NXP Semiconductors N.V. and Freescale Semiconductor, Ltd. announced the completion of the merger pursuant to the terms of the previously announced merger agreement from March 2015. The merger has created a high performance mixed signal semiconductor industry leader, with combined revenue of over $10 billion. The merged entity will continue operations as NXP Semiconductors N.V. and has become the market leader in automotive semiconductor solutions and in general purpose microcontroller (MCU) products.

"Through this merger we have created an industry powerhouse focused on the high growth opportunities in the Smarter World, capitalizing on the emerging opportunities offered by the accelerating demand for connectivity, processing and security. Today's formation of the new NXP is a transformative step on our journey to become the industry leader in high performance mixed signal solutions," said Rick Clemmer, NXP Chief Executive Officer. "This merger enables us to deliver more complete solutions to our customers as we are emerging as the leader in the Secure Connections – and the supporting infrastructure – for the Smarter World domain. As a result, we reiterate today that we fully expect to continue to significantly out-grow the overall market, drive world-class profitability and generate even more cash, allowing us to continue creating significant value for NXP's shareholders."

As previously announced, the transaction is expected to be accretive to NXP non-GAAP earnings in 2016, and NXP anticipates achieving cost savings of $200 million in 2016 with a clear path to $500 million of annual cost synergies.

NXP also today announced the closing of the divestiture of its RF Power business to Jianguang Asset Management Co. Ltd ("JAC Capital"), after receiving official confirmation that JAC Capital has deposited the required funds at its bank in China to pay the purchase price. The cash proceeds for the sale will be received later this month following the required regulatory filings for cross-border transfers of funds from China. NXP has obtained bridge financing until the funds are received.

Clean apps focus of new JST Manufacturing lab

JST Manufacturing designers and builders of wet processing equipment (Boise ID) opened a new, state-of-the-art, on-site applications laboratory, where end users can develop their process with various chemistries and do tests on real equipment ranging from immersion and spray tools to dryers. The laboratory includes sophisticated metrology equipment including a scanning electron microscope and a Tencor particle counter.

End users can take advantage of the apps lab to "dial-in" on the optimization of their processes, and can minimize the amount of chemicals required and/or determine the tool features they need for their applications. This can save the customer money by eliminating features they do not need.

Typical examples of automated systems include process modules for solvents, acid, bases, deionized water rinse and drying. Mechanical, ultrasonic or megasonic agitation and other processes may also be incorporated, if desired. Another consideration is safety and there are many mandated requirements for items such as ventilation, fire suppression, chemical handling and explosion prevention.

"We like to give customers added flexibility by programming their equipment to do everything that the equipment is capable of doing," explains Louise Bertagnolli, JST president. "This enables them to dial in applications, such as chemical concentrations. They can also turn various features on or off, depending on your process requirements. Even though they may not need some of the features today, they may want to turn them on in the future, which can be both economical and powerful."

Worldwide semiconductor revenue, *Continued from page 4*

and ASIC all reporting revenue growth while the rest of the market saw declines. Strongest growth was from the ASIC segment with growth of 2.4 percent due to demand from Apple, followed by analog and nonoptical sensors with 1.9 percent and 1.6 percent growth, respectively. Memory, the most volatile segment of the semiconductor industry, saw revenue decline by 0.6 percent, with DRAM experiencing negative growth and NAND flash experiencing growth."

Intel recorded a 1.2 percent revenue decline, due to falls in PC shipments (see Table 1). However, it retained the No. 1 market share position for the 24th year in a row with 15.5 percent market share. Samsung's memory business helped drive growth of 11.8 percent in 2015, and the company maintained the No. 2 spot with 11.6 percent market share.

"The rise of the U.S. dollar against a number of different currencies significantly impacted the total semiconductor market in 2015," said Mr. Mushell. "End equipment demand was weakened in regions where the local currency depreciated against the dollar. For example in the eurozone, the sales prices of mobile phones or PCs increased in local currency, as many of the components are priced in U.S. dollars. This resulted in buyers either delaying purchases or buying cheaper substitute products, resulting in lower semiconductor sales. Additionally, Gartner's semiconductor revenue statistics are based on U.S. dollars; thus, sharp depreciation of the Japanese yen shrinks the revenue and the market share of the Japanese semiconductor vendors when measured in U.S. dollars."

The NAND market continued to deteriorate throughout the year. As a result, revenue grew only 4.1 percent in 2015, fueled by elevated supply bit growth that resulted in an aggressive pricing environment. The tumultuous NAND pricing environment rippled through most of the NAND solutions, particularly solid-state drives (SSDs), which continue to encroach on hard-disk drives (HDDs). The ensuing price war in SSDs further pressured the profitability of the NAND flash makers amid the biggest technology transition in flash history — 3D NAND. While 3D NAND commercialization was modest, it was limited to only one vendor — Samsung. Modest revenue gains have not stopped investment in NAND flash and 3D technology, with all vendors continuing to spend aggressively in the technology and most with new fabs.

After 32.0 percent revenue growth in 2014, the DRAM market hit a downturn in 2015. An oversupply in the commodity portion of the market caused by weak PC demand led to severe declines in average selling prices (ASPs), and revenue contracted by 2.4 percent compared with 2014. The oversupply and the extent of ASP declines could have been significantly worse if Micron Technologies' bit growth had performed in line with its South Korean rivals. Fortunately for the market, the company saw negative bit growth due to its transition to 20 nm, sparing the industry from an even more severe downturn.

Samsung, TSMC *Continued from page 4*

capacity for joint-investor/partner SanDisk.

- Rounding out the top 5 companies was another memory IC supplier SK Hynix with 1.3 million wafers/month (8.1% of total worldwide capacity).
- Intel's capacity declined slightly in 2015 because of the company's Fab 68 in China being taken off-line while it is converted from the production of logic chipsets to next-generation flash memory (3D NAND and XPoint).

Wafer Capacity Leaders at Dec-2015
(Monthly Installed Capacity in 200mm-equivalents)

2015 Rank	2014 Rank	Company	Headquarters Region	Dec-2014 Capacity (K w/m)	Dec-2015 Capacity (K w/m)	Yr/Yr Change	Share of Worldwide Total	Inclusion or Exclusion of Capacity Shares from Joint Venture Fabs
1	1	Samsung	S. Korea	2,345	2,534	8%	15.5%	
2	2	TSMC	Taiwan	1,657	1,891	14%	11.6%	+SSMC, +Vanguard
3	3	Micron	N. America	1,539	1,601	4%	9.8%	+IM Flash, +Inotera
4	4	Toshiba/SanDisk	Japan	1,276	1,344	5%	8.2%	
5	5	SK Hynix	S. Korea	1,170	1,316	13%	8.1%	
6	7	GlobalFoundries	N. America	646	762	18%	4.7%	+SMP
7	6	Intel	N. America	719	714	-1%	4.4%	+IM Flash
8	8	UMC	Taiwan	526	564	7%	3.4%	
9	9	Texas Instruments	N. America	520	553	6%	3.4%	
10	10	STMicroelectronics	Europe	487	458	-6%	2.8%	
		WW TOTAL		15,412	16,350	6%	72%	

Source: Companies, IC Insights

Given the skyrocketing cost of new wafer fabs and manufacturing equipment and as more IC companies transition to a fab-lite or fabless business model, IC Insights expects that an even greater percentage of fab capacity will be in the hands of fewer suppliers through the end of the decade. ◆

Stanford researchers, *Continued from page 6*

Current approaches utilize lithography for nanoscale patterning. Using lithography and etching for fabrication of 2D or 3D structures often results in misaligned features and causes a risk of shorting or high resistant areas. However, selective deposition using ALD can reduce these risks and reduce the process time and steps.

Bent explained that selective deposition allows layers of material to be added onto a substrate only where desired without the need for additional lithography steps. However, the high level of selectivity needed for a manufacture-worthy process has not yet been achieved in area selective deposition studies. In addition, most methods for area selective deposition require long processing times.

The Stanford research has been focused on selective deposition of dielectric materials on metal/dielectric patterns. These type of structures can be found in interconnects and back-end-of-line (BEOL) processing. With ALD being used in other stages of the device fabrication process as well, the results from the Stanford experiments can potentially be applied to a variety of nanoscale electronic, optoelectronic and sensing devices.

The research developments occurred during the second year of research on the topic, and the Stanford team is continuing to explore new methods for area selective ALD to improve both selectivity and manufacturability.

"The Stanford team's research has shown for the first time that, by following selective deposition of a dielectric material using pre-treatment by an inhibitory material, they can significantly reduce the process time (from 48 hours to less than 1 hour) and also improve the limits of selective deposition of dielectrics by more than 10 times," said Kwok Ng, Senior Science Director of Nanomanufacturing Materials and Processes at SRC. ◆

IWLPC Insights

PHIL GARROU,
Contributing Editor

The 12th annual International Wafer Level Packaging Conference (IWLPC) was held in San Jose in October. The technical focus consisted of 1) fan-out WLCSP, 2) 2.5 and 3D IC packaging, and 3) MEMS. This conference is becoming a major player in the exhibition end of the packaging business this year having 65 booths set up in San Jose. Here's a review of the news in these areas.

DECA

Cost, yield and reliability issues have effectively limited the widespread adoption of FOWLP. Placing singulated chips on the carrier to form the molded panel requires high placement accuracy. Any misplacements can lead to pattern overlay difficulties in the buildup process on the reconstituted panel. The requirement for high placement accuracy restricts throughput at the pick-and-place operation, leading to high process costs. During the molding operation and mold cure, die drift or movement can occur. This die drift can further complicate pattern overlay matching in the buildup process on the panel and can result in yield loss when the drift is excessive.

In the DECA process die with preformed Cu studs are placed face-up on a carrier, using a high speed pick and place tool. The front and sides of the die are then covered with mold compound using compression molding. The molded panel is debonded from the carrier, and the front surface is ground to reveal the Cu studs. A high speed optical scanner is used to determine the actual position of every die on the panel. This information is fed into a proprietary Adaptive Patterning design tool, which adjusts the fan-out unit design for each package on the panel to match actual die locations. Finally, the design files for each panel are imported to a lithography machine which uses the design data to dynamically apply a custom, Adaptive Pattern to each panel during the fan-out build-up process. Adaptive Patterning works by dynamically adjusting one or more build-up layers to accurately connect to the Cu studs protruding through the mold compound for each individual die in the molded panel.

SPTS – Plasma dicing

Plasma dicing is attracting significant interest within the semiconductor industry as a viable alternative to conventional singulation methods using saw blades or lasers. Plasma dicing promises benefits such as increasing wafer throughput, die per wafer and die yields (due to low damage processing). For small die, in particular, where the time required for a high number of mechanical slices in "series" can be substantial, a "parallel" process such as plasma dicing which etches all dicing lanes simultaneously, can significantly increase wafer throughput.

Maximum benefits are gained when plasma dicing is "designed in" from the beginning. With dicing lanes defined by photolithography, these lanes can be narrower than the width of a dicing blade, saving valuable silicon real-estate which can be used to increase the number of die per wafer. Also, the designer can make sure that dicing lanes are free from metals and other layers which can hinder plasma etching. This is often quoted as the prime challenge which prevents implementing plasma dicing in an existing production scheme.

IMEC/KLA-Tencor

IMEC/KLA-Tencor shared their results on investigations to determine the best way to insure µbump presence and co-planarity. µbump dimensions are being scaled down to 20 µm pitch (10 µm in width and 8 µm high). For die-to-die and die-to-wafer stacking, the need for highly accurate and repeatable measurement of µbumps at both die-level and wafer-level is a must for this technology to become a viable industrial option. Bump co-planarity is defined as the difference between the heights of the tallest and the shortest µbump within a die.

A failure to properly characterize the co-planarity of each die and detect defects of interest such as damaged, missing or mis-located bumps can lead to the wrongful classification of the die as suitable for assembly. This may have a number of yield-affecting consequences during stacking, such as open and short circuits, die cracking and thermal sinks. As the number of die in a typical die stack increases, a single falsely classified die will affect the entire product.

One of the challenges in constituting a meaningful subset for measurement is to define a population of µbumps which is large enough to be statistically significant and to select µbumps from areas in the die which will represent height range and coplanarity of the full die.

Packaging

Measuring 5nm particles in-line

ED KORCZYNSKI,
Sr. Technical Editor

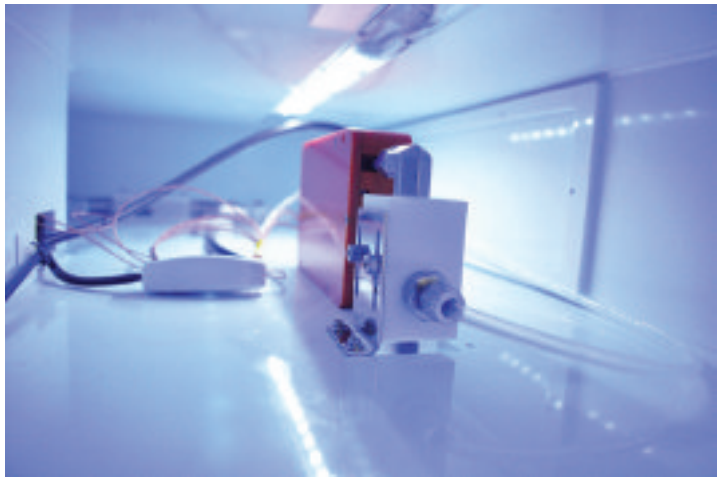
Industrial Technology Research Institute (ITRI) worked with TSMC in Taiwan on a clever in-line monitor technology that transforms liquids and automatically-diluted-slurries into aerosols for subsequent airborne measurements. They call this "SuperSizer" technology, and claim that tests have shown resolution over the astounding range of 5nm to 1 micron, and with ability to accurately represent size distributions over that range. Any dissolved gas bubbles in the liquid are lost in the aerosol process, which allows the tool to unambiguously count solid impurities. The Figure shows the compact components within the tool that produce the aerosol.

Semiconductor fabrication (fab) lines require in-line measurement and control of particles in critical liquids and slurries. With the exception of those carefully added to chemical-mechanical planarization (CMP) slurries, most particles in fabs are accidental yield-killers that must be kept to an absolute minimum to ensure proper yield in IC fabs, and ever decreasing IC device feature sizes result in ever smaller particles that can kill a chip. Standard in-line tools to monitor particles rely on laser scattering through the liquid, and such technology allows for resolution of particle sizes as small as 40nm. Since we cannot control what we cannot measure, the IC fab industry needs this new ability to measure particles as small as 5nm for next-generation manufacturing.

There are two actual measurement technologies used downstream of the SuperSizer aerosol module: a differential mobility analyzer (DMA), and a condensation particle counter (CPC). The aerosol first moves through the DMA column, where particle sizes are measured based on the force balance between air flow speed in the axial direction and an electric field in the radial direction. The subsequent CPC then provides particle concentration data.

Combining both data streams properly allows for automated output of information on particle sizes down to 5nm, size distributions, and impurity concentrations in liquids. Since the tool is intended for monitoring semiconductor high-volume manufacturing (HVM), the measurement data is automatically categorized, analyzed, and reported according to the needs of the fab's automated yield management system. Users can edit the measurement sequences or recipes to monitor different chemicals or slurries under different conditions and schedules.

When used to control a CMP process, the SuperSizer can be configured to measure not just impurities but also the essential slurry particles themselves. During dilution and homogeneous mixing of the slurry prior to aerosolization, mechanical agitation needs to be avoided so as to prevent particle agglomeration which causes scratch defects. This new tool uses pressured gas as the driving force for solution transporting and mixing, so that any measured agglomeration in the slurry can be assigned to a source somewhere else in the fab.



Aerosol sub-system inside "SuperSizer" in-line particle sizing tool co-developed by ITRI/TSMC. (Source: ITRI)

TSMC has been using this tool since 2014 to measure particles in solutions including slurries, chemicals, and ultra-pure water. ITRI, which owns the technology and related patents, can now take orders to manufacture the product, but the research organization plans to license the technology to a company in Taiwan for volume manufacturing. EETimes reports that the current list price for a tool capable of monitoring ultra-pure water is ~US$450k, while a fully-configured tool for CMP monitoring would cost over US$700k. ◆

Semiconductors

Yield and cost challenges at 16nm and beyond

ROBERT CAPPEL *and* **CATHY PERRY-SULLIVAN,** *KLA-Tencor Corp., Milpitas, CA*

A new 5D solution utilizes multiple types of metrology systems to identify and control fab-wide sources of pattern variation, with an intelligent analysis system to handle the data being generated.

In order to produce IC devices at sub-16nm design nodes, semiconductor manufacturers are integrating many novel technologies, including multiple patterning, spacer pitch splitting, 3D logic and memory structures, new materials and complex reticles. The challenges associated with these innovative technologies place huge cost strains on the semiconductor industry. In this environment, high yields and fast ramps play critical roles in helping semiconductor manufacturers maintain profitability.

Process control has helped IC manufacturers accelerate yield over the last 30 years, providing the inspection and metrology technologies necessary for early identification of critical process issues. As IC device design nodes shrunk over time, process control systems kept pace through the implementation of innovative technologies that enabled detection of defects and process variations that inhibited yield and reliability. For example, KLA-Tencor's optical wafer inspection systems have evolved over the past 30 years from using a tungsten-halogen light source, off-the-shelf microscope objectives and an off-the-shelf sensor to utilizing a laser-pumped broadband light source that is brighter than the sun, optics that are as complex as those used in steppers and custom sensors that are 1,000 times faster than a digital camera. Today's broadband plasma optical patterned wafer inspectors are now capable of detecting 10nm defects—only four times larger than the diameter of a DNA strand. Moreover, the detection of these defects across all die on a 300mm wafer is equivalent to finding hundreds of coins dispersed across an area the size of the state of California from many miles in space—in an hour.

The multiple technologies used to produce today's leading-edge devices create challenges for process control. Inspection and metrology systems need to be able to extract signal from smaller defects and process/pattern variations, often on complex 3D structures with high-aspect ratio features. With novel materials and increased process variability, this signal extraction needs to happen in an environment of increased background noise. In addition, with multiple patterning and more process steps, inspection and metrology tools need to provide increased productivity to enable sufficient production monitoring to detect excursions. For example, FinFETs produced using multiple patterning techniques require process control strategies that utilize advanced inspection and metrology systems that integrate design information and produce the sensitivity necessary to help address smaller critical defects, 3D structures and narrow process windows. In addition, the inspection and metrology solutions must also provide improved productivity to help cost-effectively monitor and control the increased number of process steps associated with fabricating the FinFETs using multiple patterning.

These challenges drive the innovation that produces the unique process control technologies and solutions that find design, patterning or process issues early. This capability is essential for IC manufacturers as it enables

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production of today's leading-edge and future technologies with maximum yield and device performance at reduced risk and cost.

The value of process control

The inspection and metrology systems at the core of process control are not used to fabricate IC devices, as they do not add or remove materials or create patterns. However, rather than being superfluous steps in IC manufacturing, process control is critical for making high-yielding, reliable devices. By finding defects and measuring critical parameters, inspection and metrology systems monitor the hundreds of steps required to manufacture a device. These process control measurements help fab engineers identify and troubleshoot process issues when there is an excursion. Process control is fundamentally tied to yield as it would be near impossible for fabs to pinpoint process issues that affect yield without inspection and metrology.

Achieving a fast yield ramp to get products to market quickly is essential for chipmakers—any delay in yield ramp affects revenue [1] and can affect future investment in R&D and the release of next-generation products. By taking steps such as implementing capable process control strategies, a fab can attain shorter development times, faster manufacturing ramps and improved production yield. In fact, the value chipmakers can attain from process control is realized in many forms, including: strong return on investment; lower manufacturing costs and risks; increased revenues; faster time to money; improved cycle times; greater profits; and, business continuity.

In order to provide deeper insight into the value of process control, the ten fundamental truths of process control (**FIGURE 1**) were compiled. Each of the fundamental truths has been introduced in a series of Process Watch articles [2-10], including details on the applications of these truths to semiconductor IC manufacturing. By understanding the fundamental nature of process control through these ten truths, fabs can implement strategies to identify critical defects, find excursions and reduce sources of variation.

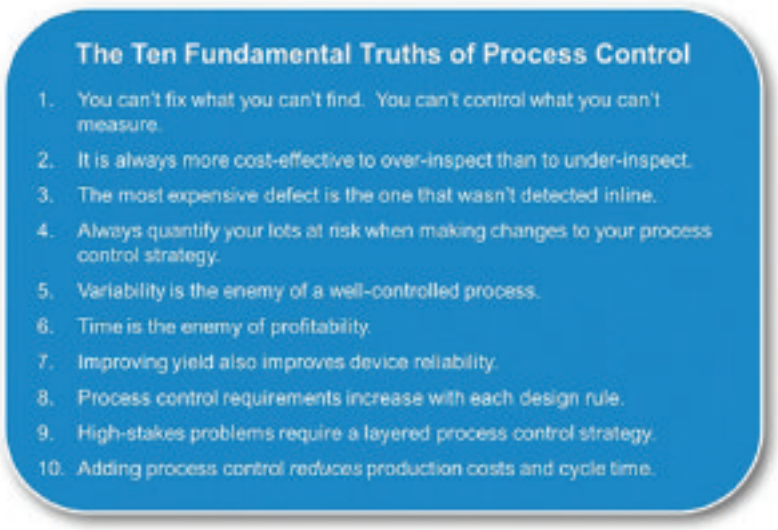


FIGURE 1. The ten fundamental truths of process control for the semiconductor IC industry.

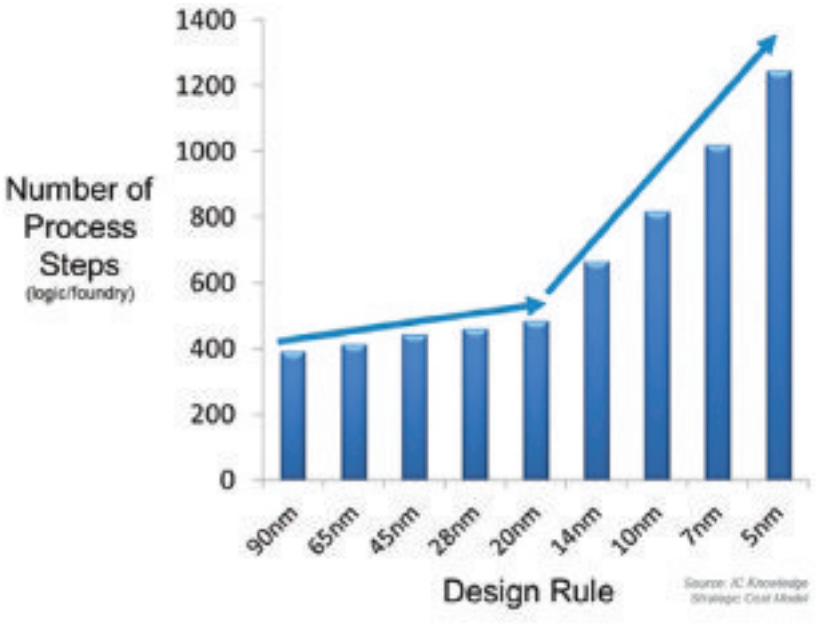


FIGURE 2. The number of process steps increases dramatically with decreasing design rule starting at the 16/14nm design node. Source: IC Knowledge Strategic Cost Model.

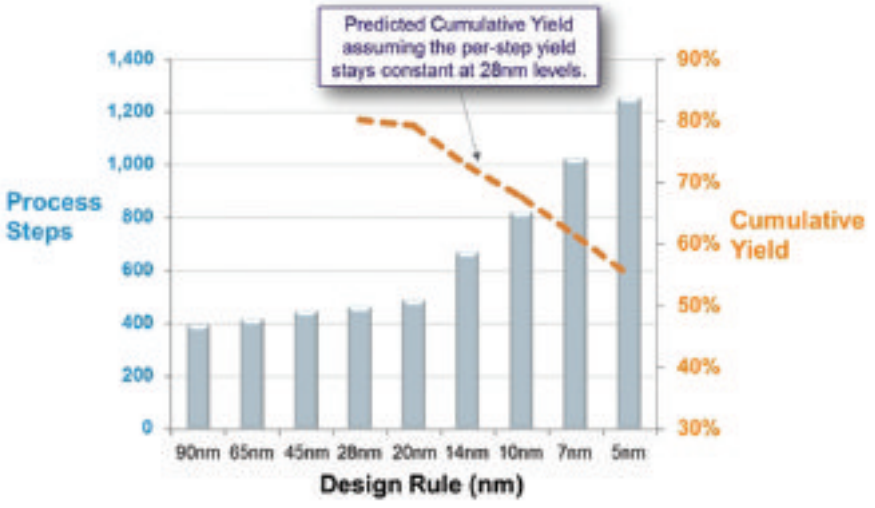


FIGURE 3. With increasing process steps, the predicted cumulative yield will drop for advanced design nodes if the per-step yield stays constant at 28nm levels.

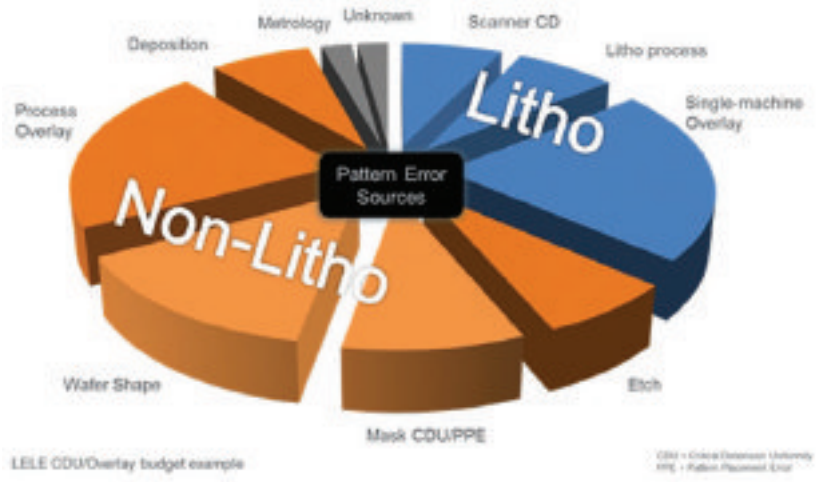
Given the increasing complexity of advanced devices and process integration, one of the most critical fundamental truths that fabs must account for going forward is: Process control requirements increase with each design rule [9]. As **FIGURE 2** shows, the number of process steps increases dramatically starting with the 16/14nm design node. As the number of process steps increases, all steps must be held to a higher standard for excursions, defect density and variability. If the per-step yield stays constant at the level achieved for the 28nm node, then the predicted cumulative yield will drop with each smaller design node (**FIGURE 3**). Because of this compounding nature of yield loss, fabs must obtain tighter controls and lower defect density at each individual process step. This drives the need for new process control strategies that not only detect yield-critical defects and subtle process variations, but also allow engineers to increase inspection and metrology sampling. Such process control capability enables direct monitoring of the increased number of process steps and quick detection of excursions that can have a tremendous impact on wafer manufacturing costs.

Strategy for future process control challenges

In moving to sub-16nm design nodes, semiconductor manufacturers are faced with many challenges to Moore's Law. On the technical side, there are the complexities associated with the integration of novel technologies (e.g., multiple patterning, 3D structures, new materials, complex reticles, increased number of process steps). On the economic side, the convergence of these multiple technologies creates increased pressure on fabs to maintain control of costs. Transistor costs are related to the scaling factor, manufacturing costs and yields. With rising fab, design, development and lithography costs, the best solution semiconductor manufacturers have to achieving the cost goals of Moore's Law is accelerating yield.

In trying to achieve faster yield ramps, IC manufacturers must confront the many issues surrounding the robustness of their design and process window. On the design side, engineers must be able to find and assess design weak points in order to drive improvements that ensure the device design and fabrication techniques are stable for production. At the sub-16nm design nodes, the required pattern overlay budgets are ≤4.5nm, critical dimension specifications are ~2nm and process windows are extremely narrow. In order to drive the changes necessary to achieve these tight patterning specifications (**FIGURE 4**), engineers need to understand fab-wide sources of patterning error and the impact of variations on process windows.

In this environment of tackling difficult technical challenges within cost targets, process control is essential.



Technology Node	28	20	14	10
Overlay budget	9nm	6nm	4.5nm	3.5nm
CD specs	4.5nm	3nm	2nm	1.3nm

FIGURE 4. For advanced multi-patterning technologies, the sources of patterning errors are fab-wide—occurring both inside and outside the lithography cell. In order to meet the incredibly tight specifications for overlay and critical dimensions, engineers must look at reducing the fab-wide sources of process variation.

Developing the necessary process control solutions is challenging—requiring both tremendous innovation and close collaboration among multiple sectors within the semiconductor industry. Not only is it necessary to develop novel technologies that provide advanced inspection and metrology system performance, it is also essential to pursue innovation towards comprehensive process control solutions—strategies that tie process control systems together, so they work in concert in the fab with intelligent analysis systems handling the complex, high-volume data being generated. These process control "system of systems" can help fabs achieve faster yield ramp through quick design verification and process window discovery, expansion and control.

Two examples of process control solutions are shown in **FIGURE 5**. With defect discovery the goal is to detect and identify yield-critical defects that highlight design issues during development and process drift during production. The discovery system leverages design information through NanoPoint™ technology on the 2920 Series broadband plasma optical defect inspection systems to find critical pattern defects that affect yield the most dramatically. The Surfscan® SP5 unpatterned wafer inspection system aids in preventing yield issues by detecting tiny substrate defects that can distort the subsequent films and pattern structures on advanced 3D devices, such as FinFETs and vertical NAND flash. Finally, the eDR-7110 e-beam review and classification system identifies the defects detected by the 2920 Series and Surfscan inspectors. By producing comprehensive information on critical nanoscale defects, the defect discovery solution helps fab engineers characterize, optimize and monitor their advanced processes to accelerate time-to-market.

The goal of the 5D™ patterning control solution [11, 12] is to help IC manufacturers obtain optimal patterning on advanced devices. With today's complex multiple patterning and spacer pitch splitting technologies, patterning errors are no longer tied to the lithography cell. Patterning errors can come from fab-wide sources, such as wafer distortion caused by CMP that directly relates to scanner focus errors. The 5D solution utilizes multiple types of metrology systems to identify and control fab-wide sources of pattern variation, with an intelligent analysis system to handle the data being generated. A critical component of this system solution is

FIGURE 5. The future of process control involves "system of systems" solutions which tie together multiple inspection and metrology systems with intelligent data analysis. Shown are two examples of process control solutions: KLA-Tencor's defect discovery solution on the left and KLA-Tencor's 5D patterning control solution on the right.

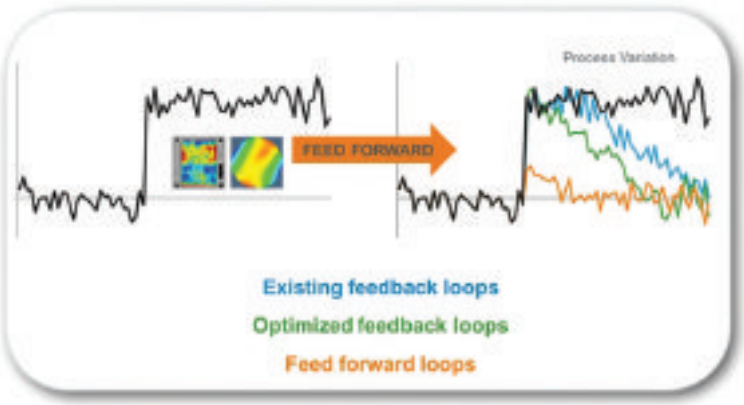


FIGURE 6. KLA-Tencor's 5D patterning control solution implements multiple data loops to help optimize patterning. Existing feedback loops (blue) have existed for several design nodes and detect and compensate for process variations. New, optimized feedback loops (green) provide earlier detection of process changes. Innovative feed forward loops (orange) utilize metrology systems to measure variations at the source, then feed that data forward to subsequent process steps.

the ability to feed back and feed forward metrology data (**FIGURE 6**). Feedback loops have been utilized for many design nodes. For example, Archer™ 500LCM overlay metrology systems identify patterning errors and feed back information to the lithography module and scanner to improve the patterning of future lots. But, there is also the opportunity to feed forward information that can further improve patterning. For example the WaferSight™ PWG patterned wafer geometry measurement system can measure wafer shape after processes such as etch and CMP and this data can be fed forward to the scanner to improve patterning [13 - 15]. Overall, this 5D solution—utilizing fab-wide, comprehensive measurements and an intelligent combination of feedback and feed forward control loops—can help fab engineers expand their process windows, reduce variation within those windows, and ultimately obtain better patterning results.

These comprehensive process control solutions are a critical part of IC industry success, enabling high yields and fast ramps by allowing engineers to more quickly and cost-effectively address a broad range of process issues. Going forward, it is essential to maintain an ecosystem of innovation and collaboration that ensures novel process control systems and solutions are developed that address IC process and cost challenges.

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Executive viewpoints: 2016 outlook

Each year, Solid State Technology turns to industry leaders to hear viewpoints on the technological and economic outlook for the upcoming year. Read through these expert opinions on what to expect in 2016.

Solving inflection challenges through materials engineering

Prabu Raja, vice president, general manager, Patterning and Packaging Group, Applied Materials

This year, the industry will see significant progress on several crucial technology inflections. Memory manufacturers are transitioning to 3D NAND to build higher performance, higher density memories at a lower cost per bit. We expect all major memory suppliers to ramp their 3D NAND devices into high-volume production in 2016.

The transition from planar to 3D NAND devices creates a new set of manufacturing requirements, prompting the shift to materials-enabled scaling and the need for new materials and process technologies. New deposition and etch products capable of precise, atomic-level layer-to-layer thickness and uniformity control are crucial to fabricating the multi-layer stacks of memory cells. And with numerous enabling patterning and conformal materials being used to build complex structures, materials selectivity is becoming an essential capability.

In the second half of 2016, we expect to see the ramp of 10nm 3D FinFET process technology in logic and foundry. The 10nm platform is necessary to sustain historic transistor performance gains, increase transistor packing density per Moore's Law and bring next-generation chip designs to market. However, this inflection is heavily dependent on multi-patterning techniques to overcome the current optical lithography resolution barrier given the delays in EUV litho tool readiness. Multi-patterning is equally critical in the DRAM transition from 20nm to 1Xnm to achieve continued growth in memory bit density. While multi-patterning supports continued scaling, it raises process complexity, driving rigorous new requirements for precision in deposition and etch processes.

As chipmakers race to deliver on the industry's inflections, they will drive investment in a variety of innovative products. Looking ahead, we expect 2016 to represent an important turning point where entirely new capabilities will move into 10nm/1Xnm node production environments. In particular, with more materials used to fabricate advanced device designs, we expect new technologies such as selective material deposition and removal, which can selectively remove or deposit material in a target area without touching or damaging other materials, to play a prominent role in creating the chips that make our connected world possible.

Expect application diversity in the new era of electronics

Aaron Thean, Vice President of Process Technologies and Director of the Logic Devices Research

After more than 50 years of scaling transistor density and performance, we are entering a new technology era of diverse applications and pervasive connectivity. Looking back, CMOS technology has focused on performance and density. The industry tended to converge towards standard CMOS technology platforms that served computers and laptops, and more recently smart mobile devices. But as we move into a new era, the Intuitive Internet of Things (I2oT), we anticipate a growth in application space. A highly-connected ecosystem of

data centers, smart mobile devices and sensor nodes will demand dramatic data bandwidth increase. At the same time, a trend towards specialized hardware with a variety of energy-efficient electronic systems that can satisfy a myriad of performance, form-factor and cost needs, may emerge. Instead of one baseline technology, there will be more heterogeneity at the system level.

The same trend is fostered by a change in the semiconductor landscape. For some years now, there is a consolidation of companies that invest in advanced CMOS technologies. Only the lead players adopt the most advanced technology nodes, with the big chunk of applications still reliant on older nodes. Interestingly, system companies start to offer products that implement technologies spamming the entire spectrum: from older process technologies to the most advanced technologies. This way, they are customizing and specializing for functionality, cost and form factor. This new trend of flexibly mixing and matching technologies to serve the system gives rise to new and mounting challenges. Challenges for performance, power, cost and density scaling to future process technologies.

Different challenges with flash, STT-MRAM and ReRAM

Arnaud Furnemont, department director memory at imec

Research in memory is really exciting these days: in parallel you have the scaling of classical memories (SRAM, DRAM, Flash) and the emergence of new memories capable of enabling new applications or even new system hierarchies. At imec, we mostly focus on three concepts which all come with different challenges.

First is Flash, and specifically 3D NAND. Here it's the integration challenge that is keeping us all busy. Before, the focus was on device scaling, but now it's all about stacking more layers. Last year, we explored new materials for the channel (e.g. III-V channel in 3D NAND) and for the trapping layer (YAlO instead of SiN), in parallel with device reliability characterization and modelling.

Another important memory type is STT-MRAM where a complex magnetic stack makes the scene. Focus here is on choosing the right material combination and developing the perfect stack (with perfect interfaces!). Over the last years, imec made a lot of progress to build a good stack. But even more challenging is the patterning of this multi-layers structure without affecting the magnetic properties of the device. Very recently we were able to demonstrate 45nm devices with good performance. Tool suppliers are improving the etch platforms and I expect STT-MRAM as embedded memory in the foundries by 2017 and as standalone memory by 2020. In the latter case, more scaling is necessary and this implies more etch issues which will have to be solved.

Thirdly, we explore resistive RAM. The challenge for this type of memory is picking the right combination out of the numerous kinds of stacks and materials. And to do this, you need a fundamental understanding of what happens inside each stack. Imec has developed in depth characterization and modelling on OxRAM and CBRAM memories, expected to be used in embedded applications. Globally, RRAM suffers from a trade-off between write energy and stability. VMCO is another RRAM variant developed at imec to break this trade-off. To be competitive in standalone applications, RRAM will also need to be combined with a selector, which requires again material selection and benchmarking. This is a role that imec is willing to take on for its partners.

Finally, there is also a high-level challenge that the memory researchers and developers are facing. It's the changing landscape in which emerging memories have more and more impact on the system architecture. Before, the system hierarchy was built with the memory technologies that were available. In the future it might be the other way around: the system architects will tell us what to develop. A closer collaboration between the device team and system architects is therefore indispensable. Imec's memory 'insite' activity will tackle this challenge.

New technologies will fuel pockets of growth in 2016

Mike Plisinski, Chief Executive Officer, Rudolph Technologies, Inc.

While the 2016 outlook for the semiconductor industry as a whole appears increasingly uncertain, there are areas where significant

growth remains likely. In particular, advanced packaging, driven by growing consumer demand in applications ranging from smartphones and tablets to the Internet of Things (IoT), shows great promise for continued innovation.

First, we see outsourced assembly and test (OSAT) manufacturers driving the development of new packaging technology. For example, we've seen major gains in the adoption of fan-out packaging and copper pillar technology, evidenced by ongoing capacity expansion, and the addition of new players—the most obvious perhaps being the large ongoing investment by a leading foundry in Asia where our inspection equipment has received a prominent role. We see more and more manufacturers choosing to add yield management and/or advanced process control (APC) software, to obtain a competitive advantage in not only cost, but also reliability. This is achieved by transforming ultra-large data sets into useful information used for predictive analytics (reducing costs) and analysis across the supply chain (improving reliability).

The growth in advanced packaging is also driving the adoption of sophisticated lithography techniques for these new technologies. Our JetStep advanced packaging stepper is now in high-volume manufacturing use at several top OSATs. The system allows our customers the flexibility to handle all of the current advanced processes within a single tool, which provides a compelling cost of ownership value. We also see emerging processes, such the adoption of rectangular panel substrates, in some packaging applications, certainly in fan-out, but also embedded and other packaging technologies. Rectangular panels promise significant gains in economy-of-scale and processing efficiency.

Lastly, expansion in radio frequency (RF) device capability continues to grow, with the increasing number of devices that communicate wirelessly and the increasing number of frequencies with which they communicate. Measuring the electrode and piezo layers of SAW/BAW filters will only grow as more and more filters are required in mobile devices. Beyond mobile, the expansion in RF is also driven by WiFi, Bluetooth and IoT requirements for connectivity, so we expect it to accelerate even as the smartphone growth curve flattens.

The IoT, and concerns about fab safety and environmental impact will be driving forces

Paul Rawlings, Vice President Marketing, Semiconductor and DSL Business, Edwards

In addition to the continuing efforts to maximize performance and efficiency of mainline 300mm process equipment and develop 400mm capability, we see a number of factors that are likely to play an important role driving markets during the coming year. Among them are an accelerating resurgence in demand for 200mm equipment, growing emphasis on safety in the fab and increasing concern about the impact of manufacturing on the environment.

It has been more than ten years since 300mm equipment shipments surpassed 200mm and became the dominant manufacturing process for advanced memory and microprocessors. Over most of the intervening years, device and equipment manufacturers focused almost solely on the race to improve the performance and efficiency of 300mm processes and invested heavily in what was at first regarded as an inevitable transition to 400mm. Both IDMs and foundries found themselves with idle 200mm capacity. More recently, a number of new applications have appeared that do not require the advanced capabilities available in 300mm processes, and can in fact, be produced more cost-effectively on 200mm lines. These include a variety MEMS based devices – motion sensors, audio and radio frequency; image sensors; communications, power, and analog devices. To date, these developments have been driven primarily by the explosive growth of smart phones and automotive systems. Now the internet of things (IoT) looms large on the horizon with the expectation that advanced, multifunctional electronics will soon be incorporated into an almost unlimited variety of new connected products. Many of these will not benefit from the advanced capabilities or economies of scale provided by 300mm processes and will be most efficiently produced on existing or new 200mm lines. We expect to see increasing demand for support and retooling in this market.

We are also seeing increasing emphasis on safety in the fab among our customers and we strive to be an integral part of their efforts. For instance, last year we received a prestigious safety award from LG electronics in Korea

that recognized our excellence in safety management, for both performance on site and for the safety ethos which exists throughout our company. We have made and continue to make great efforts to ensure that that ethos permeates our corporate culture – 100 percent safety, 100 percent of the time. From a business point of view, we believe that as our customers increase their own emphasis on safety it will become a significant differentiator in the competitive marketplace.

Hand in hand with safety goes an increasing awareness of the impact of manufacturing on the environment. Increasingly this is true in developing economies as well as the developed world. China, for example has reached a crisis level in some regions and has responded with increasingly strict environmental standards. Edwards has long been a leader in environmental awareness within the semiconductor manufacturing community. Our abatement products play an important role in limiting our industry's impact on the environment. We are one of few manufacturing companies in the world that can claim to have a negative net carbon footprint – the combined effect of our own operations and the operation of our vacuum and abatement products over their lifetimes is to remove carbon from the environment. As an industry we have made significant progress in reducing our contribution of greenhouse gases, including particularly damaging PFCs. One trend that we see playing an important role in semiconductor manufacturing in the coming year will be increasing emphasis on the preventing the formation and release of oxides of nitrogen, NOx. As production capacity grows, so too does the volume of nitrogen used to dilute process gases in the exhaust stream. Unless carefully managed, some of this nitrogen can be converted to NOx, which, although not greenhouse gases, are a health hazard.

Greater process control essential to enable future scaling

Richard Gottscho, Ph.D., Executive Vice President, Global Products, Lam Research Corp.

2016 looks to be an exciting year as several key inflection technologies – including multiple patterning, FinFET, and 3D NAND – continue to move into high-volume manufacturing worldwide. While these inflections enable the continuation of Moore's Law, the increasing number of steps and overall complexity add significantly to the challenge of reducing process-induced variation.

At the 10 nm node and below, edge placement error (EPE) is becoming a significant limitation to continued scaling. Historically, the degree of EPE was largely determined by misalignment in lithography overlay. Today, EPE can be dominated by other process components, and variations from both lithography and non-lithography steps are pushing EPE beyond the allowable design specifications. This is exacerbated by the adoption of multiple patterning techniques such as litho-etch-litho-etch. One way to reduce overlay errors is to decrease the mask count, for example, by advancing to next-generation EUV lithography. With or without EUV, improved on-product overlay can be achieved by reducing line edge roughness through etching- and deposition-induced smoothing.

Another contributor to EPE in multi-patterning comes from pitch walking. This is particularly challenging in self-aligned patterning schemes, where several deposition and etch process steps are used to define the line/space patterns. In this case, the critical dimension (CD) is defined not only by lithography, but also by core etch, spacer deposition, spacer etch, and wet clean process steps used to double or quadruple the density. To improve CD uniformity and minimize pitch walking, advanced process and process control solutions such as atomic layer deposition (ALD) and die-scale fine-tuning to correct for incoming pattern variation are being adopted in volume manufacturing.

Increased complexity is evident not only in multiple patterning, but also in device architectures that are migrating from 2D to 3D. In a FinFET, for example, the channel area is defined not only by fin width and length, but also by fin height. Precise control of CDs in all directions is vital to FinFET device performance. There will also be an increasing need for precision atomic layer etching (ALE) to minimize damage, reduce roughness, and increase selectivity.

In the case of 3D NAND, vertical stacking of memory cells poses its own process control challenges. Achieving uniform formation of the memory cells from top to bottom of the multi-layered film stack requires stringent control during film stack deposition, hardmask deposition, hardmask open etches, and the memory hole etch itself. Currently, 3D NAND devices with up to

48 layers are in volume manufacturing. With applications such as SSDs now adopting 3D NAND technology, enabling next-generation structures with up to ~100 layers is putting more pressure on equipment suppliers and device manufacturers to minimize variations and defects through advanced process control.

As the industry embraces the benefits offered by inflection technologies – lower power, higher density, and more functionality – chipmakers are facing mounting challenges imposed by increased complexity and cost. Next-generation non-volatile memories, alternative interconnect strategies, new channel materials, and new device architectures such as nanowires will further increase complexity and demand even greater control of unit processes as well as the interaction between those processes. Finding solutions to improve process control, reduce variation, and reduce cost is essential for the industry to continue scaling.

Test will be front and center for semiconductors in 2016-2017

Michel Villemain, CEO, Presto Engineering, Inc.

Over time test has become accepted as second nature for semiconductor manufacturers: it needs to be done, it has a known value, it is considered a separate step to bringing a product to market, and it is clearly business as usual. However, the semiconductor industry is once again evolving and several new themes will vastly change the view of test, how it is perceived, implemented, and the value it brings.

The first major change coming is the new 5G communications standard that promises to provide greater data transmission rates and speed. To reach this next plateau, the industry will need to adopt higher, millimeter-wave frequency designs to handle bandwidth, and thus it will be confronted with testing devices in the +30GHz range. This is nothing new since small volume demand already exists for applications like point-to-point cellular communications. However, the real challenge will come when the industry needs to run high volume as new infrastructure coming on line outpaces the know-how required to support it.

Second is the Internet-of-things (IoT) market. This new and clever monolithic term is really a great way to consolidate applications linked by common characteristics, notably the ability to "sense" the real world, to "analyze" the sensed data both locally and remotely, make intelligent decisions, and be connected to the Internet/Cloud for data crunching. Success in IoT will come from using known technologies and building blocks to solve a new class of use cases. Much of this sensing and gathering of data can involve intrusion control, management of critical processes, and/or personal data--all of which need to be protected.

Securing IoT products will require a combination of solutions including secure Internet access, secure software stacks, and product/hardware security via secure elements. In recent years, professional security hackers have shown that there are numerous ways to enter a system and take control of it. For example, test access ports, USB's and other backdoors are an open opportunity for malevolent hackers. So, as one of the best ways to secure an IoT system for more sensitive devices, the industry is likely to take a proven page from the payment system world by injecting unique secure codes into semiconductors.

The IoT will also call for more complete systems (SOC's, SIP's). The mixing of sensing, local computation, storage, and transmission – "all in one" – promises to challenge testing strategies as there is a lack of analog test standardization, now commonly found in digital devices.

With driver-assisted/self-driving automobiles, ADAS/AD (advanced driver assistance systems, automated driving), the automotive industry is turning to the aerospace world for inspiration. Redundancy is a critical element to insure both safety and quality, and engineers will be faced with multicore designs both for logic and storage involving totally new testing strategies for BIST and traditional external verification.

In summary, test needs to get ready for change -- and this is good because it signals the coming of many new and exciting products in 2016-17. ◆

Helium reduction at pre-metal sub-atmospheric CVD

JAE HEE KIM, *Thin Film Dielectric Fabrication Engineering, Texas Instruments, Dallas, TX*

A novel SACVD PMD invention sets the benchmark for helium reduction efforts by achieving four key objectives: cost reduction, quality, process robustness and productivity.

The United States is the world's largest helium supplier and half of its supply comes from a helium reserve regulated by the Bureau of Land Management just outside of Amarillo, Texas. As many predict, at the current rate of production the maximum expected life of this reserve is 2020. As a result of a shortage that began in 2013, the cost of bulk helium has been increasing significantly (**FIGURE 1**).

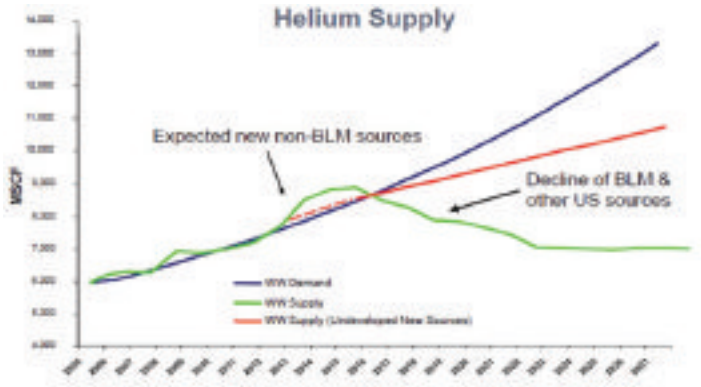

FIGURE 1. Helium supply and demand forecast [1].

Considering semiconductor manufacturing is one of largest helium consuming industries [2], it becomes crucial to invest continuous efforts to minimize helium usage during wafer fabrication processes and to identify new opportunities for helium reduction. In this article, we'll take a look at a new innovative process to do just that.

Sub-Atmospheric Chemical Vapor Deposition (SACVD) for pre-metal layer consumes a significant amount of helium to assist in process gas delivery during deposition and in-situ chamber clean which makes the best candidate for helium reduction effort benchmarking. Also, SACVD Pre-Metal Dielectric (PMD) consists of various processes including phosphosilicate glass (PSG) and borophosphosilicate glass (BPSG) which makes the fan-out process more applicable for a bigger impact on helium reduction. So how do we do it?

Objectives

There are four key objectives to a new SACVD PMD process development that my team has looked at: cost, quality, process robustness, and productivity. First, a new carrier gas was identified to maximize helium usage reduction. Second, solutions to both new hardware and process conditions were developed for quality improvement. A new blocker plate was qualified to improve within wafer thickness uniformity. Additionally, gas conditions were developed to improve the gap-fill capability for leakage reduction. Third, a new pressure condition was qualified for process robustness improvement. An old two-step baseline process was designed for better gap fill by depositing initial 4kA film at 700Torr for lower deposition rate and the rest of the film at BKM pressure, 200Torr for better cycle time. However, this baseline two-step process, which operates at near atmospheric pressure on a sub-atmospheric CVD tool platform, is marginal

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for pumping speed degradation which leads to inline defect. Susceptibility of defect formation was reduced by lowering process pressure from 700Torr to 600Torr during the initial PMD layer. Last, overall process conditions were evaluated to achieve a desirable deposition rate in order to ensure comparable manufacturing throughput. Furthermore, a new process condition was selected to avoid process chamber restriction for flexibility of manufacturing.

New process carrier gas identification

Initial process development was divided into two categories: BPSG and PSG. Development began with PSG since there is one less process parameter, Boron compared to BPSG process. Preliminary tests showed that a 100 percent N2 carrier drives an unstable film thickness range. Based on findings, a helium and nitrogen mix carrier gas was selected for further process evaluation. The main focus at this stage of evaluation were to identify process conditions including a helium and nitrogen mix carrier gas flow to achieve maximum helium savings, comparable cycle time, and thickness uniformity improvement.

Process condition development

Based on design of experiments (DOE) with four key process parameters (N2, He, O3, spacing), we learned that deposition rate is faster with increasing He and slower with increasing N2 and O3. Thickness uniformity degrades with total carrier gas flow. Based on DOE results, initial proposed condition was carrier 5500sccm (3:1 = N2:He), O3 3000sccm, spacing 200mils for better thickness uniformity and shorter cycle time while saving the maximum amount of helium.

Unfortunately, this condition degraded at baseline margin to form voids in 700Torr deposition film due to faster deposition rate. Focus was then shifted to identify a recipe condition that lowers the deposition rate during 700Torr deposition for a better gap fill capability which also can be used for both 200Torr PSG and two-step PSG to ensure manufacturing flexibility.

Based on deposition rate DOE with three parameters including Ozone, tetraethyl orthosilicate (TEOS) and spacing (**TABLE 1**), ozone flow has first-order effects on the deposition rate, and spacing has second-order effects. TEOS flow has third-order effects on deposition rates but also reduces dopant concentration of film. Temperature change was not considered since it affects other recipe conditions at a greater degree. Increasing pressure was also not considered since the process already operates at a high pressure of 700Torr.

TABLE I
NEW PMD PROCESS RESPONSE

Parameter ↑	Deprate	Thickness Range	B%	P%
TEOS Flow	↑	↔	↓	↓
Spacing	↓↓	↑	↑	↑
Temperature	↓	↑	↑	↑
Pressure	↓	↔	↓	↑
Ozone Flow	↓↓↓	↑	↑	↓
N2 carrier flow	↓	↑	↔	↔

TABLE 1: New PMD Process Response

Then it was decided to include Ozone and spacing, in addition to helium and nitrogen, into further process characterization. We ran comprehensive three factorial DOE to deposit 4kA PSG film at 700Torr at various settings of total carrier flow, spacing, and ozone. This was in order to achieve a lower deposition rate for better gap fill and good thickness uniformity. DOE conditions were determined based on JMP prediction profiler and calculators to evaluate a wide spectrum of different deposition rates at 700Torr and thickness range.

To evaluate the DOE result, two techniques were used. First, wafer samples were prepared by sputtering top

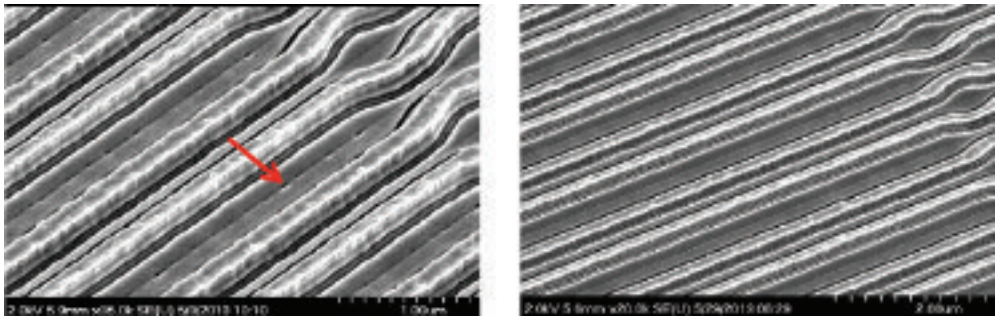

FIGURE 2. Top down SEM shows new PMD (right) has a less number of voids compared to old PMD process (left).

down until they reached the very initial layer of PMD to open up any voids that are present in PSG film. Effectiveness of gap-fill capability was rated by quantifying a number of voids on the scanning electron microscopy (SEM) images captured at same magnification on the consistent location of the wafer sample. This is a more effective technique than collecting transmission electron microscopy (TEM) on a defined location on samples since top down SEM can capture broader areas of wafer samples. Second, wafers were also submitted for dynamic secondary ion mass spectrometry (SIMS) to ensure if the dopant profile throughout PSG film is comparable to the baseline. This critical step is to verify that there is no sign of unstable dopant distribution that could lead to any adverse effects, such as increased etch selectivity or poor gettering (**FIGURE 2**).

Based on DSIMS collected, it was found that the dopant concentration profile becomes unstable if the total carrier gas flow is less than 5500sccm. Phosphorous (P) concentration profile shows fluctuation all throughout the film at a total carrier gas flow less than 5500sccm while phosphorous percent profile was steady at total carrier gas at 5500sccm or higher (**FIGURE 3**).

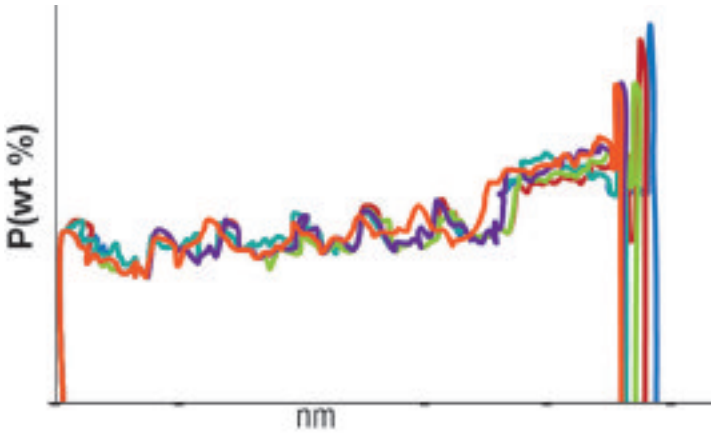

FIGURE 3. Dynamic SIMS suggests dopant concentration profile is wavy when total carrier gas flow falls under 5500sccm.

Among many conditions that satisfy a total carrier gas flow of less than 5500sccm, when ozone flow is 5000sccm and total carrier gas is 5500sccm with a 3:1 ratio of nitrogen to helium, the top down SEM result shows a greatly reduced number of voids in film. This means the deposition rate during 700Torr is slow enough to improve gap-fill capability. At the same time, Ozone flow at 5000sccm was fast enough during 200Torr to maintain a comparable cycle time. Therefore, this condition can be used for both single step PSG and two-step PSG which allows flexibility for manufacturing to run both processes without equipment restriction. Dynamic SIMS also verified that this condition provided a stable dopant profile. Thickness uniformity was also comparable to the baseline on this recipe condition. Therefore, spacing 200mils, ozone 5000sccm, and a total carrier flow 5500sccm was chosen as a finalized new PSG condition.

For the BPSG process, the same technique was used for evaluation. DSIMS was used to ensure both Boron and phosphorous concentration profiles are comparable. The same carrier gas conditions with nitrogen and helium at a ratio of 3:1 of 5500sccm and Ozone 5000sccm were selected for the final condition. TEOS was increased from 600mgm to 800mgm to make sure the deposition rate is comparable to maintain manufacturing cycle time at PMD (**TABLE 2**).

TABLE II
FINALIZED PMD SINGLE STEP PROCESS GAS CONDITION

	BPSG		PSG	
Parameters	Old	New	Old	New
O3 (sccm)	4000	4000	5000	5000
TEOS(mgm)	600	800	900	900
He (sccm)	6000	1375	7000	1375
N2 (sccm)	0	4125	0	4125

TABLE 2: Finalized PMD Single Step Process Gas Condition

Flash parametric legacy issue improvement

A high aspect ratio of device structure can cause voids in PMD that lead to poor isolation and yield loss. There are many contributing factors that modulate PMD voids, including a stacked gate vertical profile and a sidewall spacer profile. Among all contributing factors, however, a void-free PMD process was proven to be the most effective way to minimize leakage. The void-free PMD was achieved by qualifying a new two-step PSG process with a mix carrier gas.

The new two-step PSG process with a mix carrier greatly lowers the deposition rate during the initial PMD layer. This helps deposit film more uniformly at higher pressures to minimize voids, while depositing the rest of the PMD at a faster deposition rate at lower pressure helps to compensate cycle time loss from the initial deposition.

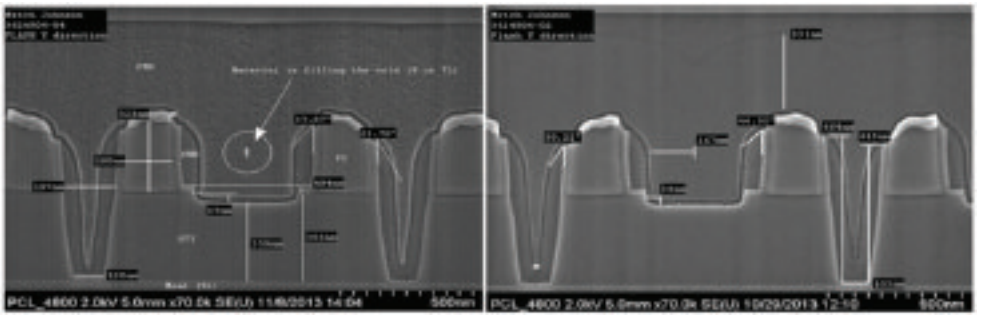

FIGURE 4. Void-free PMD (right) shows excellent gap fill while baseline PMD (left) shows a void filled with W [3].

The new two-step PSG alleviates leakage susceptibility on the wafer edge and reduces sensitivity to the PMD void-contributing factors by adding significant margins to leakage failure due to voids. Notably, the PMD gap-fill improvement added significant integration marginality between the sidewall spacer profile and the PMD which led to lower process and tool sensitivity at the sidewall spacer etch. This increases manufacturing capacity by releasing sidewall spacer etch process chambers with historical leakage failure susceptibility to production. Most importantly, parametric outlier probability was greatly improved by 20 percent and a zero standard parametric failure rate was achieved by qualifying void-free PMD (**FIGURE** 4).

Process robustness improvement

There were technical challenges with center cluster defects on the new two-step process. Center cluster defects affected isolation contact resistance. Based on TEM (**FIGURE 5**), defects formed around where a low deposition rate completed and a faster deposition rate resumed. Dynamic SIMS showed a phosphorous concentration peak at the defect which explained why this defect had a high contact etch selectivity.

After exposing the test wafer for 24 hours at atmosphere, haze was formed on its substrate. Time of flight secondary ion mass spectroscopy showed that haze was caused by a reaction between excessive phosphorous and atmospheric moisture. Additionally, a repeatability test showed that the tail of cluster defects extended towards gas exhaust. Based on these findings, this baseline two-step process which operates at near-atmospheric pressure on a sub-atmospheric CVD tool platform is marginal to maintain sufficient pumping speed during pressure transition from high process pressure to low process pressure (**FIGURE 6**). This significantly increased the chances of forming center cluster defects with a heavier carrier gas. This is because the pumping speed is lower at a higher pressure and mean residence time is longer at a higher pressure. Additionally, conductance is lower with N2 than with He due to heavier molecular weight.

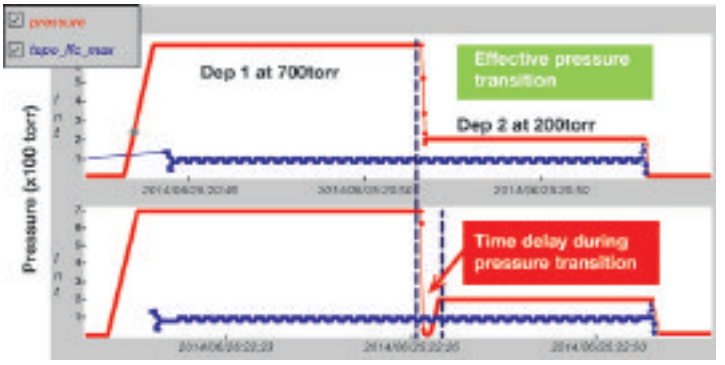

FIGURE 6. Real-time pressure trace top (good) and bottom (center cluster defect) time delays to reach 200Torr chamber pressure.

In order to address this issue, the new two-step process was reevaluated and a new process condition was developed. As summarized in **TABLE 3**, it was decided to maintain the same carrier gas flow to maintain bulk helium savings. Pressure condition for the first deposition step was modified from 700Torr to 600Torr. This new two-step process improved robustness by reducing risks of pumping speed degradation during the pressure transition from 600Torr to 200Torr. The new two-step process is also able to deliver a strong PMD void-fill improvement by maintaining a zero parametric failure rate for leakage.

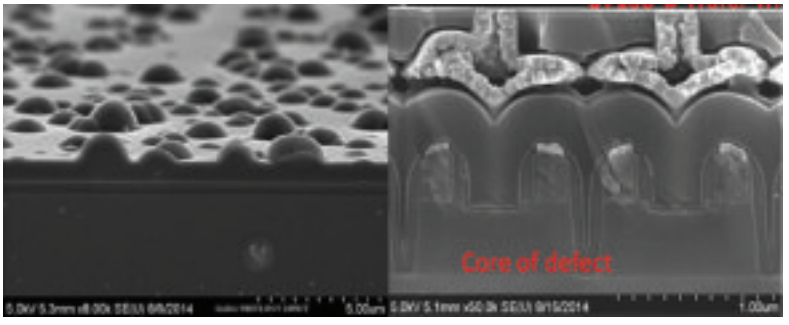

FIGURE 5. TEM on PMD surface (left). TEM on core of defect (right).

TABLE III
FINALIZED PMD 2STEP PROCESS RECIPE CONDITION

Parameters	Old 2step PSG	New PSG
O3 (sccm)	4000	5000
TEOS(mgm)	600	900
He (sccm)	6000	1375
N2 (sccm)	0	4125
1st Dep Pressure (torr)	700	600
2nd Dep Pressure (torr)	200	200

TABLE 3: Finalized PMD two-step Process Recipe Condition

Thickness uniformity improvement

The new SACVD PMD invention took part not only in process development but also in hardware improvement. The new process with a baseline helium blocker plate that helps uniform process gases dispersion showed higher within wafer thickness range which appeared on wafer substrate as in forms of lightly discolored spots. Based on Energy Disperse Spectroscopy (EDS) and Dynamic SIMS, defects were a part of the top 270A of PSG film. The location of spots were nicely matched to the hole pattern of the helium blocker plate. The nitrogen blocker plate was qualified as it consisted of the same material as the helium blocker plate but had a more dense hole pattern. It was not only able to eradicate the anomaly on the surface film but also to alleviate the baseline starburst pattern on the deposited film.

DSIMS confirmed that the dopant profiles on the nitrogen blocker plates are comparable to the ones on the helium blocker plate. The nitrogen blocker plate improved within wafer thickness uniformity by 35 percent on a new PSG film ranging from 12kA to 16kA compared to an old PMD baseline performance (**FIGURE 7**). Consequently, this improved the process capability index at post PMD Chemical Mechanical Polish (CMP) by improving process targeting based on improved thickness uniformity.

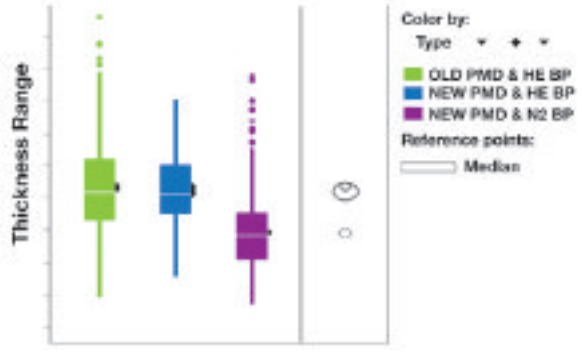

FIGURE 7. Post PMD CMP within wafer thickness range comparison.

Manufacturing and engineering productivity increased, as well, due to reduced tool down time. New blocker plate qualification also alleviated the sensitivity of film thickness uniformity to the heater age and possibly helped to extend heater life on the PSG chambers and reduce tool down time for range failure.

Conclusion

This novel SACVD PMD invention successfully set the benchmark for helium reduction efforts by achieving four key objectives: cost reduction, quality, process robustness, and productivity. It brings a substantial impact on bulk helium gas savings with worldwide limited supplies and increasing demand. The new PMD reduces bulk helium usage by 80.4 percent and 77.1 percent for PSG and BPSG respectively during deposition and completely eliminates helium usage during in-situ chamber clean.

This new process achieved outstanding gap-fill capability by lowering the deposition rate at initial PMD layer. The process successfully eliminated leakage failure at parametric by adding significant process integration marginality for void formation. It also improves process robustness by reducing risks of pumping speed degradation during the pressure transition from 600Torr to 200Torr. Process conditions are carefully developed for comparable manufacturing throughput and harmonized between single step PSG and two-step PSG in order to ensure manufacturing flexibility. Lastly, new hardware qualification also helps improve quality and productivity by lowering within wafer thickness range.

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[1] C. Kaneshige, 2013, an excerpt from GE Healthcare published in 2012

[2] Semiconductor Industry Association, August 1, 2012, Hearing on "Helium: Supply Shortages Impacting our Economy, National Defense and Manufacturing" (Hearing held on July 10, 2012). Testimony for the Record of the Semiconductor Industry Association.

[3] D. Rodriguez, 2014, unpublished

Improved ion implant exhaust management reduces energy, capital costs

STEVEN BALLANCE *Texas Instruments, Dallas, TX,* **KARL OLANDER** *and* **JOE SWEENEY,** *Entegris, Billerica, MA*

How Texas Instruments got greener, safer and saved money.

Over the last decade, considerable efforts have been put forth by manufacturers and suppliers to help reduce costs, consumption of natural resources, and where economically viable or by mandate, to become more green in fab operations. In the early 2000s, Texas Instruments (TI) outlined an opportunity to re-think its approach around one of the largest energy and cleanroom air consumption areas in the fab—ion implant operations.

In comparison to other manufacturing tools in the fab, ion implanters require the largest exhaust volume, typically using 2500 CFM in total ventilation, split between the gas box [400+ CFM] and the containment shell enclosure [2000+ CFM]. The energy cost to replace this volume of air equates to about $8,000 per tool and, with up to 30 implanters in a typical fab, the operating costs can reach up to $240K annually. In addition, the investment needed to replace this volume of clean, highly conditioned air is substantial and requires large infrastructure expenditures (**FIGURE 1**).

In the late 2000s, TI provided the industry with a glimpse of what was possible around air handling and energy reduction in its implant centers. The initial concept, implementation and projected results had been years in the making and were first published in August, 2009 by Solid State Technology, as provided by Steve Russo, then a senior member of TI's technical staff.

Typical Ion Implanter Exhaust Flows (CFM) and Energy Costs

Shell	1700–2000	General	$3.50/CFM/yr
Gas box	300–500	Acid	$4.50/CFM/yr

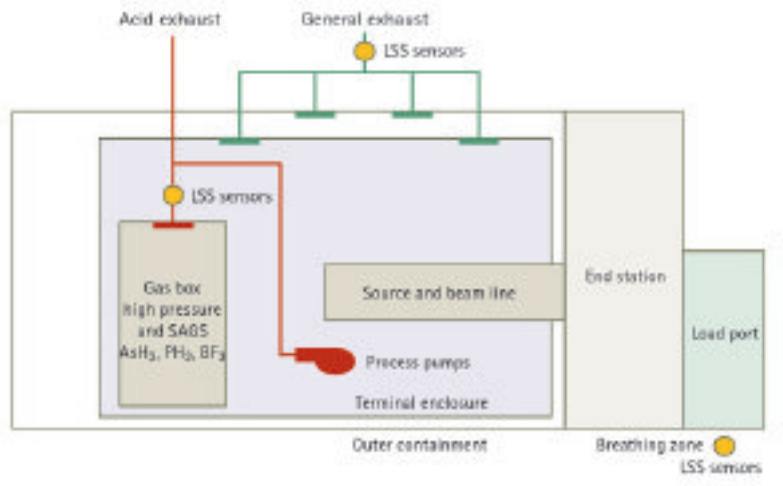

FIGURE 1. Typical ion implanter exhaust flows (cubic feet per minute) and energy costs.

STEVEN BALLANCE, P.E., *is a facilities engineer at Texas Instruments, Dallas, TX.* **KARL OLANDER** *and* **JOE SWEENEY** *are with the Electronic Materials division of Entegris, Danbury, CT.*

Exhaust and Make-up Air Capital Cost Comparison for a Ten-Implanter Expansion Project	Traditional Exhaust Configuration	Reduced Exhaust Configuration
Terminal enclosure exhaust (SCFM)	17000	Recirculated
Gas box exhaust (SCFM)	4500	1700
Total (SCFM)	21500	1700
	Installation Costs (US$)	
Galvanized steel duct	$13,000	$5,000
Coated stainless steel duct*	$100,000	$37,000
Exhaust fans	$100,000	$23,000
Fume scrubbers	$300,000	$60,000
Make-up air handlers	$220,000	$40,000
Total	$733,000	$165,000
Total Cost Avoidance	$570,000	
Net Cost Avoidance Per Implanter	$57,000	

*Assumes acid exhaust is required for small process effluent flow.

FIGURE 2. Reconfigured exhaust systems amounted to a $57,000 capital cost avoidance per process tool.

In the article, Russo explained the operating protocols for handling the highly toxic materials utilized in the ion implant process, which are traditionally stored within the tool itself. Now, after years of development and modification, a bigger picture, along with intriguing data, has emerged.

Recycling the shell exhaust

The 2009 article described how TI recycled the implanter shell exhaust within the fab, reducing the make-up air requirement by 80% [2000 CFM per tool]. Fab air is drawn through the implanter shell to dissipate heat from the process and provide dilution in the event of a process leak. This volume of air is treated as general exhaust, and traditionally expelled from the fab using blowers on the roof.

The successful implementation of the first phase, led to the recycle of the shell exhaust on more than 60 ion implant tools across three fabs without incident. Whereas the initial installation included ductwork to convey shell exhaust to the roof (if needed in an emergency), subsequent facilities were built on the premise of continuously returning the shell exhaust to the fab. In practice, the reconfigured exhaust systems amounted to a $57,000 capital cost avoidance per process tool. **FIGURE 2** illustrates these cost savings projections.

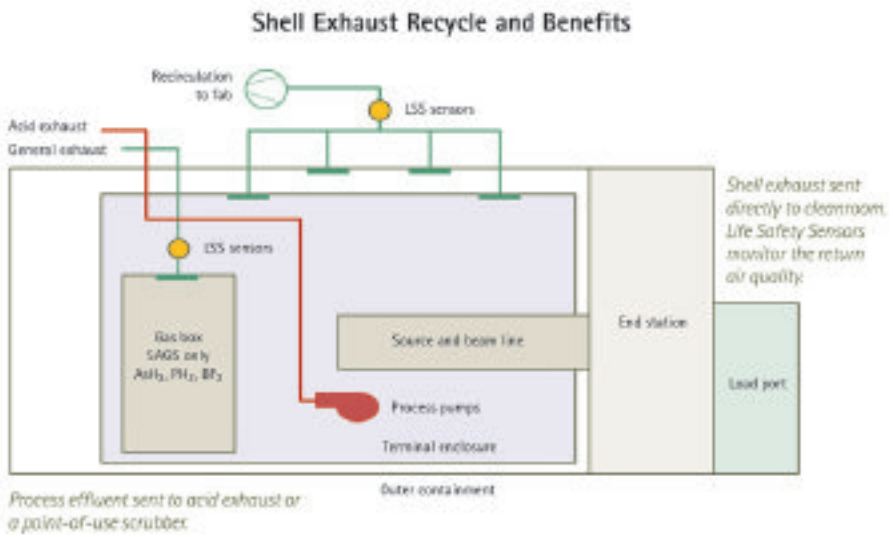

FIGURE 3. The new design configuration for shell exhaust recycle is shown.

Recycling the shell exhaust has resulted in avoiding $1.7 million in capital for exhaust and make-up air infrastructure, as well as, reducing annual energy cost by $470,000. The lower energy usage equates to reduced CO2 emissions of 6,500 metric tons. **FIGURE 3** illustrates the new design configuration for shell exhaust recycle.

The role of sub-atmospheric pressure gas sources

In redesigning the implant exhaust configuration, Russo and his team he relied on using only the safest gas packaging technology—sub-atmospheric gas sources, or SAGS.

These packages deliver gases below atmospheric pressure, greatly reducing the likelihood of a gas leak and providing the basis to redirect the shell exhaust back into the fab.

It is interesting to note that around the same time Russo published his first article on his new design, the National Fire Protection Agency (NFPA) adopted the SAGS classification for gas packages into the standard. The NFPA classified gas packages that store and deliver gas sub-atmospherically as SAGS Type I and packages that store gas under pressure but deliver gas sub-atmospherically as SAGS Type II. Both SAGS systems share a common feature—they require a process vacuum in order to deliver the toxic gas, virtually eliminating accidental gas releases (**FIGURE 4**).

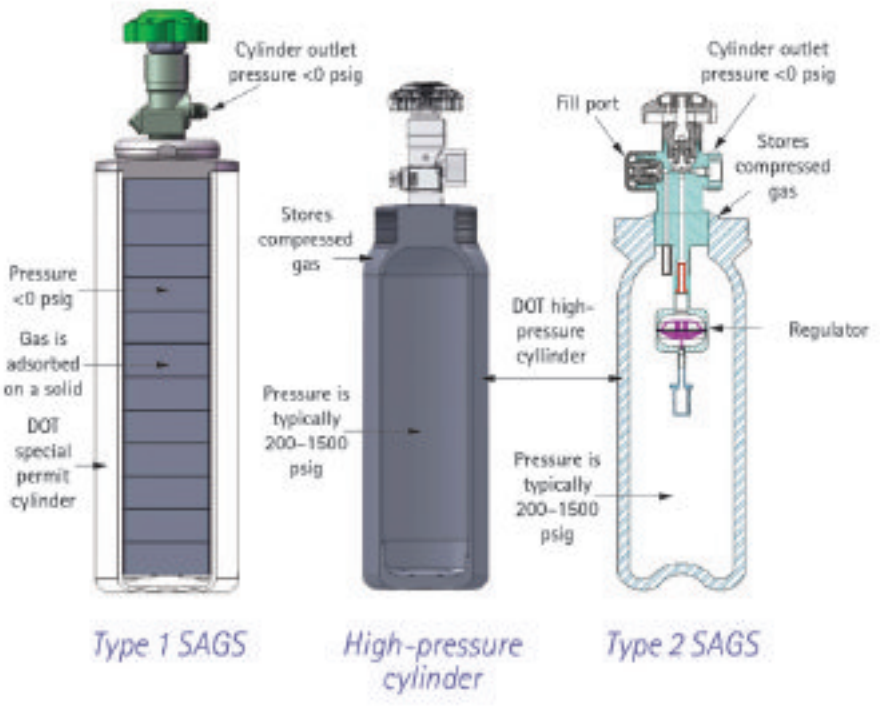

FIGURE 4. SAGS systems require a process vacuum in order to deliver the toxic gas, virtually eliminating accidental gas releases.

The initial planning for re-configuring the shell exhaust system in the new design was done to take full advantage of the safety profile of the SAGS packages. Using traditional high pressure delivery systems in the new design wouldn't have been prudent because of the higher gas leak potential and lower safety profile. Exclusively using SAGS technologies enabled the exhaust reduction program approach. Continuous efforts and success rely on doing everything possible to see that gas delivery is always sub-atmospheric and TI has taken precautions to ensure the gas delivery systems are consistently performing in this way.

Gas box exhaust reductions

The process of lowering implanter shell exhaust began over 12 years ago, and since then most TI tools have been fitted with this design. On its continued quest for reduced energy and costs, TI identified the gas box as being the next best opportunity.

The gas box exhaust, potentially containing hazardous materials, is sent through a scrubber before being released. Scrubbed (or acid) exhausts, therefore, consume more resources than shell exhaust and contribute more to the costs of fab operations.

Over the past few years, Texas Instruments and ATMI, now Entegris, providers of SAGS technologies, have teamed up to continue to look for efficiencies and safety measures in managing exhaust gas and energy usage in ion implant operations. After evaluating the energy reduction potential of the tool gas box exhaust, TI made modifications that led to reduced gas box exhaust rates of about 200 cfm, down from over 400 cfm. This resulted in an additional $800 savings per tool per year. Additional strategies to reduce gas box exhaust rates and improve overall safety are suggested below.

Building an integrated [smart] exhaust system

Today, ion implanters utilize dopant cylinders with manual valves that had their start when "lecture bottles" were first used 30 years ago—and space in the gas box was at a premium. Small cylinders and manual valves were standard. Even as solid source vaporizers were replaced, and the use of gases in larger cylinders became prevalent, the use of manual valves continued.

Interestingly, the Type 1 and Type 2 sub-atmospheric gas delivery cylinders used worldwide to supply implant dopant gases use manual valves. The presence of the manual valve presents a continuing risk because of

the possibility of human error during installation and purging sequences which could result in a gas release, albeit small. Yet, there is still room to reduce risk and continue to improve safety through the application of "smart" solutions.

Ultimately, the cornerstone to minimizing the occurrence and impact of a gas leak is all about maintaining the system under sub-atmospheric conditions at all times. Operating under sub-atmospheric pressure entails the continuous monitoring of gas pressure(s) in the delivery manifolds and the ability to respond quickly if pre-set pressure thresholds are exceeded.

The use of normally closed pneumatic valves provides the means to isolate the toxic gas within the dopant cylinder should the delivery manifold deviate from sub-atmospheric pressure protocols. The normally closed condition also removes from consideration cases where valves are either poorly closed or over-torqued. Cylinder cycle purging can then be done automatically, more efficiently and without the possibility of backfilling purge gas into the cylinder.

Varying the gas box flow rate

The ability to minimize the smallest of leaks would allow the gas box to be exhausted as a function of actual risk as opposed to continuously operating at a rate needed to mitigate projected worst-case scenarios. Controlling the gas box exhaust rate using a two position damper is one possible solution.

A two-position damper can control the gas box exhaust in either a low or high flow mode. The normal or reduced exhaust condition is allowed when all of the dopant delivery cylinders are showing a sub-atmospheric pressure condition or all of the cylinder valves are closed. Interlocks initiate the high flow rate any time the gas box door is opened, such as during cylinder changes or maintenance periods, or when triggered by events such as toxic gas detection, smoke detector alarm or detection of a super-atmospheric pressure condition in the dopant delivery manifold. It is estimated that the exhaust system would operate in the low flow mode >95% of the time.

With SAGS, a nominal rate of 40 cfm can be sufficient to satisfy regulations providing a 90% reduction in gas box exhaust requirements.

Taking the next step forward

TI justified recirculating the ion implanter shell exhaust within the fab based on a thorough risk analysis built around using SAGS technology. Over the last decade, they refined the practice and proliferated it across new fab installations, significantly reducing capital requirements for make-up air.

Developing an integrated exhaust system can ultimately reduce implant make-up air requirements by 98%—without compromising safety. Operating costs associated with the lower exhaust have been proportionately reduced, along with carbon dioxide emissions.

Further advances in exhaust/energy reduction are possible via a partnership between toolmakers, dopant suppliers and fab designers to incorporate an integrated exhaust system for ion implanters, and possibly other tools. It begins with insuring operating gas delivery is under sub-atmospheric pressure conditions all the time.

Future changes may include:

1. Adding pneumatic valve operators to the dopant cylinders
2. Variably exhausting the gas box proportional to actual risk conditions

Outstanding economic and environmental gains can continue to be made – and new standards created – if manufacturers, equipment makers and suppliers work together to envision the possibilities. As an industry, and as responsible corporate citizens, working together to pursue these types of opportunities can reduce energy consumption and exhaust while improving overall process safety.

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Collaboration is key to litho

The continuation of Moore's Law requires a combination of both physical and functional scaling, where our main challenge in lithography is to continue pushing the physical scaling limits in a controlled and cost-effective way. By serving as the collaboration hub of the industry in this area, imec is playing a key role in helping the industry to address the major technical challenges towards continued physical scaling. This is being done on multiple fronts.

First, work is ongoing on optical lithography where we try to squeeze everything we can out of immersion lithography by both enhancing resolution and controlling variability. Resolution enhancement for immersion is being achieved through both an increasing degree of multiple patterning and by leveraging the unique properties of novel materials such as in directed self-assembly (DSA). In DSA, sub-resolution patterns are created by the micro-phase separation of specially engineered polymer chains called block copolymers, which are directed in specific orientations by lithographically generated guide patterns. Minimizing the impact of variability is done by first developing techniques to measure, optimize and control the patterning process window, as then by the employment of clever patterning tricks to neutralize any remaining variability. Examples of such tricks, or the co-optimization of multiple unit process steps (litho, etch, deposition, etc.), are the variety of self-aligned integration schemes that are being developed.

But, of course, all eyes are on EUV lithography as it appears a necessity for the continuation of cost-effective physical scaling. Research institutes such as imec are helping industry to understand when and how to insert this technology. Certainly the performance of the tool - or more specifically the ramp in stable power of the light source - is a prerequisite for EUV insertion. ASML has realized some very promising results in this field this past year. However, there is a whole ecosystem involved with EUV lithography, such as materials, masks, understanding the imaging fundamentals, and development of computational techniques – and it is that ecosystem that imec is focused on.

GREG MCINTYRE, *director advanced patterning, imec*

EUV resolution is currently material-limited, thus imec has set up a strong program to work with materials suppliers to develop novel photoresist platforms, and now serves as the centerpiece for such work in the industry. There is also work ongoing on various aspects of the photomask. Our strong collaboration with the Japanese consortium EIDEC is aimed at understanding the capabilities of new mask inspection systems and to link this with printing performance. Additionally, imec launched a very successful pellicle program in 2015, where the pellicle is a very thin free-standing film designed to protect the mask surface from particles. We are now exploring various novel films and have set up a testing facility for characterization of samples developed around the world. Finally, various efforts are focused on understanding the complex interactions between the light source, mask, lens system, and photoresist and to employ computational techniques to optimize the resulting pattern.

With all these technical issues in mind, it becomes clear that collaboration is key to continue the path of lithography. Many parties are involved that all have to work together and contribute their piece of the puzzle. It's imec's role to bring all these parties together and understand how all the pieces fit together. This is done in our core CMOS program where all the main chip manufacturers, tool and material suppliers are gathered. But also the supplier hub that imec set up a few years ago, has evolved as a very important aspect of the collaboration platform. Tool and material suppliers can evaluate their products in an early phase of technology development and get valuable feedback on how to further optimize them. In the collaboration process, they bring in not only state-of-the-art tools and materials, but also valuable insights and experiences that help fuel imec's developments and thus strengthen the core CMOS program. In 2015, various supplier interactions ramped up and have definitely started to pay off. In summary, by serving as the collaboration hub of the industry, imec is playing a valuable role in pushing the limits of physical scaling.

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