

Solid State TECHNOLOGY

Insights for Electronics Manufacturing

Outlook for 2017

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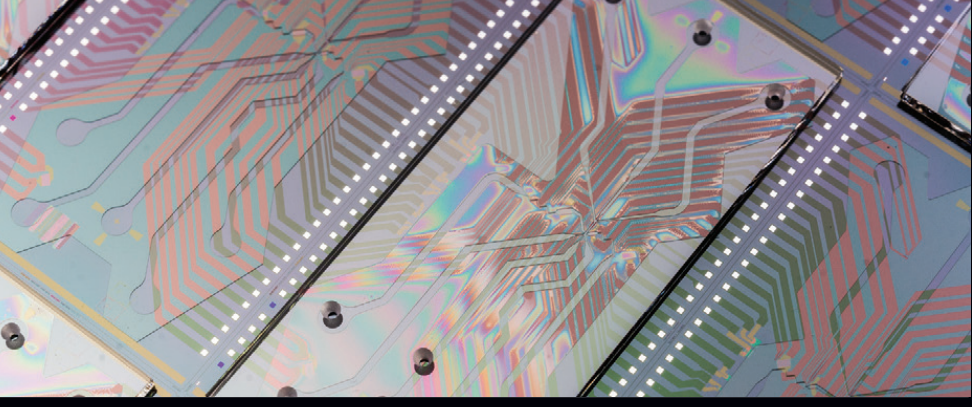
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Cell sorter chip on a silicon wafer. This chip can be used for a diagnosis tool that detects specific cells in fluids. Source: imec

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Five growth areas for semiconductors

The five hottest areas for semiconductor growth in the coming years are: the Internet of Things (IoT), automotive, 5G, virtual reality/augmented reality (VR/AR), and artificial intelligence (AI). That was the message from Gary Patton, GlobalFoundries' Chief Technology Officer and Senior VP of worldwide R&D, speaking at SEMI's 2017 Industry Strategy Symposium in early January.

The "things" in the IoT -- which will be driven by wearables, smart homes and factory automation, for example -- are just the tip of the iceberg, Patton said. It's really upgrades in the infrastructure that will be required to handle all the data produced by these things where the real opportunities lie. The data "has to go up into cloud computing where it's stored and it's processed and we do things with it," he said. The projections for the growth in wired cloud computing and servers is on the order of 30-40% per year over the next five years, he added.

Patton showed a chart that predicts semiconductor value for the IoT/cloud computing is expected to grow from \$16B in 2016 to \$62B in 2025. Automotive semiconductor value is expected to grow from \$32B to \$51B in the same time period, 5G to grow from \$0 to \$20B, AR/VR from \$4B to \$131B and AI from \$5B to \$50B.

Patton's thought when driving in a friend's Tesla was "this thing's a laptop on wheels," a sentiment echoed by other presenters at ISS. Patton said today's cars have roughly 50 sensors and around \$350 dollars of semiconductors. "As

we go forward and we get to autonomous cars, there's only going to be more electronics," he said.

Patton said that 5G, the emerging 5th generation telecommunications standard, is going to be huge. "The ability to get 10 gigabytes per second and one millisecond latency will be very key for these mission critical applications like autonomous cars," he said. "You can basically download videos in seconds rather than in an hour." Patton showed a chart that read "5G is as disruptive to wireless today as data was to voice."

Another one of the five hot growth areas for semiconductors is virtual reality. "This is moving from high end gaming to the mainstream with the advancement of technology," he said.

Artificial intelligence -- also known as deep learning -- is seen as another high growth area. "How do we actually do stuff with the data that's generated to make useful results?" Patton asked. "That will be a key growth area."

In terms of what semiconductor technology will be needed for these various applications, Patton said he divides the markets into three parts: clients (mobile, IoT and automotive), networking (5G) and data centers (compute/clouds). "There's not one technology that serves all. It's really going to require a range of technologies to really make all of these different segments and markets work," he said.

—Pete Singer, Editor-in-Chief

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Web Exclusives

A year in review: Top 10 stories of 2016

From the ground-breaking research breakthroughs to the shifting supplier landscape, these are the stories the Solid State Technology audience read the most during 2016.

<http://bit.ly/2k13nGp>

Do not go where the path may lead

What follows, in Part 1 of this two-part article, is a quick look back at the industry in 2016 and the road ahead in 2017 followed by what SEMI achieved in 2016 and where SEMI's road will lead in 2017 to keep pace our industry charging forward where there is no path.

<http://bit.ly/2kbSrbD>

Vital control in fab materials supply-chains

At the end of the inaugural 2016 Critical Materials Council conference, a panel discussion moderated by Ed Korczynski was recorded and transcribed. (From SemiMD.com)

<http://bit.ly/2jxRM36>

Fire, rain, and M&A

The expert panel, "The Future of M&A in the Semiconductor Industry," was a hot topic at SEMI's Industry Strategy Symposium (ISS) conference on January 11.

<http://bit.ly/2jenUdx>

IEDM 2016: Setting the stage for 7/5nm

At IEDM last month, there was much ado about the adjacent 7-nm late-news papers from TSMC and the GLOBAL-FOUNDRIES/IBM/Samsung group consortium from the Albany Nanotechnology Center, and with less ado, Samsung gave a 5-nm presentation later in the conference. Here we discuss all three talks, and try and make some comparisons.

<http://bit.ly/2k18GFQ>



Intel's 10nm enigma

Contributing Editor Dick James takes a look back at the talk given by Mark Bohr and Zane Ball (Building Winning Products with Intel Advanced Technologies and Custom Foundry Platforms) at the Intel Developer Forum (IDF) in August last year, and he's a bit puzzled.

<http://bit.ly/2kuDij1>

How new materials can solve contact resistance

Most connected computing devices today use 3D FinFET transistors enabled in part by technology innovations from Applied Materials. The challenging transition to FinFETs was essential to continue Moore's Law scaling. But as usual, when one problem is resolved others loom. One of the most serious of these is increased contact resistance. (From SemiMD.com)

<http://bit.ly/2k0Xmd1>

Insights from the Leading Edge: The expanding world of fan-out packaging

Contributing Editor Dr. Phil Garrou takes a look at the "Advances in Fan-out Packaging" course by Beth Keser of Qualcomm from the 13th annual 3D ASIP conference.

<http://bit.ly/2kaP7gB>

Market for power semiconductors in automotive to rev up by \$3B by 2022

The global market for power semiconductors used in cars and light passenger vehicles will grow by more in \$3 billion USD in the next six years, according to new analysis released by IHS Markit.

<http://bit.ly/2kCmF8r>

Pure-play foundry market surges 11% in 2016 to reach \$50B

The pure-play foundry market is forecast to play an increasingly stronger role in the worldwide IC market during the next five years, according to IC Insights' new 2017 McClean Report.

<http://bit.ly/2jxTMIQ>

worldnews

USA - MACOM successfully completed its acquisition of AppliedMicro.

ASIA - STATS ChipPAC was recognized for patent innovations for the seventh consecutive year by IEEE.

EUROPE - At the 2017 European 3D Summit in Grenoble, **EVG** and **imec** demonstrated for the first time 1.8µm pitch overlay accuracy for wafer bonding.

USA - Mentor Graphics CEO Walden C. Rhines was named IEEE Fellow.

ASIA - Toshiba announced the expansion of its lineup of industrial-grade e-MMC embedded NAND flash memory products.

USA - Researchers at the **University of Illinois at Urbana-Champaign** have advanced gallium nitride (GaN)-on-silicon transistor technology by optimizing the composition of the semiconductor layers that make up the device.

EUROPE - imec announced a collaboration with City of Antwerp and Flanders to establish Smart City Living Lab.

ASIA - Air Products announced plans to expand its nitrogen capacity in Pyeongtaek City, South Korea.

EUROPE - STMicroelectronics and **Valencell** announced a collaboration on biometric sensor platform for wearables and IoT.

USA - Materion Precision Optics acquired gettering capabilities for wafer level processing from Integrated Sensing Systems.

EUROPE - Seoul Semiconductor Europe GmbH announces new CEO, Andreas Weisl.

USA - Mentor Graphics announced that it has joined **GLOBALFOUNDRIES' FDXcelerator** Partner Program.

USA - Dow Corning expanded its LED packaging design options with the launch of new silicone coatings.

47% of semiconductor execs say industry in late expansion stage, says KPMG survey

Nearly half of semiconductor company business leaders believe their industry is in a late expansion phase and another 20 percent believe the industry is at an inflection point from expansion to contraction, according to the 2017 Global Semiconductor Industry Outlook from KPMG LLP, the U.S. audit, tax and advisory firm.

In addition, only about half of the semiconductor executives surveyed expect revenue to grow and research and development spending to increase over the next three years. This is less than last year when the vast majority of respondents predicted revenue growth and R&D spending increases in the three-year outlook.

"These are signs of a maturing industry, and lower growth rates may be the theme over the intermediate future," said Lincoln Clark, KPMG Global Semiconductor Industry Leader. "While there are some industry forecasts with a more optimistic one year outlook, there's also caution that the industry may be approaching the end of a growth cycle, and that caution is reflected

in the three year outlook by semiconductor executives in our survey. Pressure on the average sales price of semiconductors will continue to impact revenue and investment spending."

Semiconductor company business leaders said average sales price erosion is the top issue facing the industry over the next three years. Therefore, it follows that the number one strategic priority for semiconductor execs, according to the survey, is "diversifying into a new business area", with both "acquisition, merger or joint venture" and "talent development/management" second.

"The focus on diversification means that to successfully capitalize on future growth trends, companies must invest their R&D funds wisely and efficiently," said Clark. "Yet, this appears to be a challenge for some semiconductor companies."

Almost half (49 percent) of the semiconductor executives said their current R&D

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2015-2016 deals dominate semiconductor M&A ranking

More than two dozen acquisition agreements were announced by semiconductor companies worldwide in 2016 with a combined value of \$98.5 billion compared to the record-high \$103.3 billion in purchases struck in 2015, when over 30 deals were reached, according to a summary and analysis in IC Insights' new 2017 McClean Report. The dollar value of merger and acquisition agreements in 2015 and 2016 were both about eight times greater than the \$12.6 billion annual average of M&A announcements in the five previous years (2010-2014), says the new report, which becomes available in January 2017. Nearly half of the 15 largest semiconductor

acquisitions in history were announced in the 2015-2016 period, according to a ranking of M&A transactions over \$2 billion in the 2017 McClean Report (**Figure 1**). A total of 27 semiconductor acquisition agreements have had dollar values of \$2 billion or more since 1999.

IC Insights' ranking and acquisition data cover semiconductor suppliers, wafer foundries, and businesses licensing intellectual property (IP) for integrated circuit designs, but excludes transactions for fab equipment and material companies, chip

Continued on page 8

New report from IHS Markit names top four trends driving the IoT in 2017 and beyond

Fueled by lightning-fast demand for ubiquitous connectivity, the number of connected Internet of Things (IoT) devices globally will jump by 15 percent year-over-year to 20 billion in 2017, according to new analysis from IHS Markit (Nasdaq: INFO).

In a free new report entitled "IoT Trend Watch 2017," IHS Markit technology analysts have identified four key trends that will drive the IoT this year and beyond. Increasingly, the report says, businesses see the IoT as a tremendous opportunity to create unique value propositions by linking disparate systems of connected devices that range from multiscreen content sharing to smart city networks.

IHS Markit defines IoT as a conceptual framework, powered by the idea of embedding connectivity and intelligence into a wide range of devices. "These internet-connected devices can be used to enhance communication, automate complex industrial processes and provide a wealth of information that can be processed into useful actions – all aimed at making our lives easier," said Jenalea Howell, research director – IoT connectivity and smart cities for IHS Markit.

According to the report, the industrial sector – led by building automation, industrial automation and lighting – will account for nearly one half of new connected devices between 2015 and 2025.

IHS Markit has named these four trends as leading the IoT evolution in the coming years:

Trend #1 – Innovation and competitiveness are driving new business models and consolidation

- To date, the focus on IoT monetization has rightly revolved around the way in which suppliers earn revenue selling components, software or services to IoT application developers. Increasingly, however, the focus is shifting to the IoT developers themselves and how they will monetize new streams of data delivered by their IoT deployments.
- A wide range of monetization models are being tested, reflecting the fragmented nature of the IoT market across

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Global semiconductor sales up 7% year-to-year

The Semiconductor Industry Association (SIA) announced in January that worldwide sales of semiconductors reached \$31.0 billion for the month of November 2016, an increase of 7.4 percent compared to the November 2015 total of \$28.9 billion and 2.0 percent more than the October 2016 total of 30.4 billion. November marked the market's largest year-to-year growth since January 2015. All monthly sales numbers are compiled by the World Semiconductor Trade Statistics (WSTS) organization and represent a three-month moving average.

"Global semiconductor sales continued to pick up steam in November, increasing at the highest rate in almost two years and nearly pulling even with the year-to-date total from the same point in 2015," said John Neuffer, president and CEO, Semiconductor Industry Association. "The Chinese market continues to stand out, growing nearly 16 percent year-to-year to lead all regional markets. As 2016 draws to a close, the global semiconductor market appears likely to roughly match annual sales from 2015 and is well-positioned for a solid start to 2017."

Month-to-month sales increased modestly across all regions: the Americas (3.3 percent), China (2.7 percent), Europe (2.5 percent), Asia Pacific/All Other (0.7 percent), and Japan (0.4 percent). Year-to-year sales increased in China (15.8 percent), Japan (8.2 percent), Asia Pacific/All Other (4.8 percent), and the Americas (3.2 percent), but fell slightly in Europe (-1.6 percent). ◀▶

November 2016			
Billions			
Month-to-Month Sales			
Market	Last Month	Current Month	% Change
Americas	6.06	6.26	3.3%
Europe	2.82	2.89	2.5%
Japan	2.89	2.90	0.4%
China	9.78	10.04	2.7%
Asia Pacific/All Other	8.88	8.94	0.7%
Total	30.43	31.03	2.0%
Year-to-Year Sales			
Market	Last Year	Current Month	% Change
Americas	6.07	6.26	3.2%
Europe	2.93	2.89	-1.6%
Japan	2.68	2.90	8.2%
China	8.67	10.04	15.8%
Asia Pacific/All Other	8.53	8.94	4.8%
Total	28.88	31.03	7.4%
Three-Month-Moving Average Sales			
Market	Jun/Jul/Aug	Sept/Oct/Nov	% Change
Americas	5.43	6.26	15.2%
Europe	2.71	2.89	6.4%
Japan	2.73	2.90	6.1%
China	8.99	10.04	11.8%
Asia Pacific/All Other	8.35	8.94	7.1%
Total	28.22	31.03	10.0%

Worldwide semiconductor capital spending is forecast to grow 2.9% in 2017

Worldwide semiconductor capital spending is projected to increase 2.9 percent in 2017, to \$69.9 billion, according to Gartner, Inc. This is down from 5.1 percent growth in 2016 (see **Table 1**).

"The stronger growth in 2016 was fueled by increased spending in late 2016 which can be attributed to a NAND flash shortage which was more severe in late 2016 and will persist through most of 2017. This is due to a better-than-expected market for smartphones, which is driving an upgrade of NAND spending in our latest forecast," said David Christensen, senior research analyst at Gartner. "NAND spending increased by \$3.1 billion in 2016 and several related wafer fab equipment segments showed stronger growth than our previous forecast. The thermal, track and

implant segments in 2017 are expected to increase 2.5 percent, 5.6 percent and 8.4 percent, respectively.

Compared with early 2016, the semiconductor outlook has improved, particularly in memory, due to stronger pricing and a better-than-expected market for smartphones. An earlier-than-anticipated recovery in memory should lead to growth in 2017 and be slightly enhanced by changes in key applications.

Foundries continue to outgrow the overall semiconductor market with mobile processors from Apple, Qualcomm, MediaTek and HiSilicon as the demand driver on leading-node wafers. In particular, fast 4G migration and more-powerful processors have resulted in larger die sizes than previous-generation application processors, requiring more 28

	2016	2017	2018	2019	2020
Semiconductor Capital Spending (\$M)	67,994.0	69,936.6	73,613.5	78,355.6	75,799.3
Growth (%)	5.1	2.9	5.3	6.4	-3.3
Wafer-Level Manufacturing Equipment (\$M)	35,864.4	38,005.4	38,488.7	41,779.7	39,827.0
Growth (%)	7.9	6.0	1.3	8.6	-4.7
Wafer Fab Equipment (\$M)	34,033.2	35,978.6	36,241.1	39,272.8	37,250.4
Growth (%)	8.1	5.7	0.7	8.4	-5.1
Wafer-Level Packaging and Assembly Equipment (\$M)	1,831.2	2,026.8	2,247.6	2,506.9	2,567.7
Growth (%)	3.9	10.7	10.9	11.5	2.8

Source: Gartner (January 2017)

TABLE 1. Worldwide Semiconductor Capital Spending and Equipment Spending Forecast, 2015-2020 (Millions of Dollars)

nanometer (nm), 16/14 nm and 10 nm wafers from foundries. Nonleading technology will continue to be strong from the integrated display driver controllers and fingerprint ID chips and active-matrix organic light-emitting diode (AMOLED) display driver integrated circuits (ICs).

This research is produced by Gartner's Semiconductor Manufacturing program. This research program, which is part of the overall semiconductor research group, provides a comprehensive view of the entire semiconductor industry, from manufacturing to device and application market trends. Gartner clients can see more in "Forecast Analysis: Semiconductor Capital Spending and Manufacturing Equipment, Worldwide, 4Q16 Update." ◀



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47% of semiconductor execs, Continued from page 4

spending is not aligned efficiently with current core products and 40 percent said their R&D spending is not aligned efficiently with future growth opportunities.

Complementing M&A's selection as a top strategic priority is the fact that nearly 6 out of 10 respondents (57 percent) said that total M&A valuations will increase in 2017 compared to 2016. It is worth noting that the survey was conducted just ahead of some significant 4th quarter M&A announcements, which may have been in respondents' consideration for 2017. The survey found that revenue growth and intellectual property acquisition are still the top M&A drivers.

As semiconductor executives project lower revenue growth and seek to diversify, they are also concerned about new competitors and disruptors, which are seen as having the biggest potential impact on their company's growth over the next three years.

In looking at growth drivers in 2017, sensors/MEMS jumped to the top of the list of the highest growth opportunity. Wireless communications and Internet of Things solidified their positions as the top two most important application markets for revenue over the next year. Automotive was a close third.

Semiconductor executives also placed the U.S. back in the number one position, ahead of China, as the most important geographic area for both revenue growth and headcount growth. China was ranked first last year.

KPMG's study, conducted in September 2016, surveyed 153 semiconductor industry business leaders around the world, primarily senior level executives, including device, foundry and fabless manufacturers. Eighty-two percent of the companies represented in the survey have annual revenue of \$1 billion or more. ◀

2015-2016 deals dominate, Continued from page 4

Biggest Semiconductor Acquisition Agreements

Ranking	Acquisition-Buyer (Year Announced)	Price Tag (\$B)
1	NXP by Qualcomm (2016)	\$39.0
2	Broadcom by Avago (2015)	\$37.0
3	ARM by SoftBank (2016)	\$32.0
4	SanDisk by Western Digital (2015)	\$19.0
5	Freescale by U.S Investment Companies (2006)	\$17.6
6	Altera by Intel (2015)	\$16.7
7	Linear Technology by Analog Devices (2016)	\$14.8
8	Freescale by NXP (2015)	\$11.8
9	Burr Brown by TI (2000)	\$7.6
10	LSI by Avago (2013)	\$6.6
11	National Semiconductor by TI (2011)	\$6.5
12	ATI by AMD (2006)	\$5.4
13	Spansion by Cypress (2014)	\$5.0
14	Agere by LSI (2006)	\$4.0
15	Chartered by GlobalFoundries (2009)	\$3.9

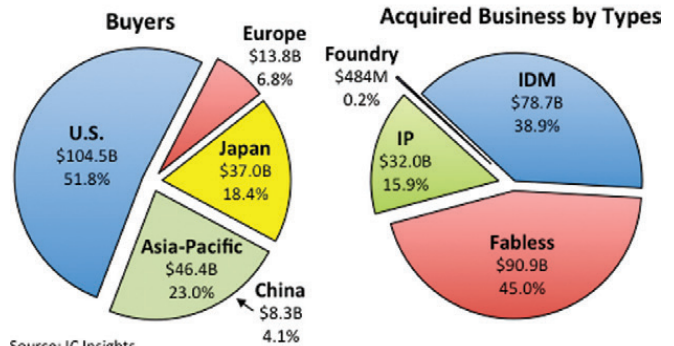
Source: Companies, IC Insights (2017 McClean Report)

FIGURE 1.

packaging and testing operations, and design automation firms. Overall, seven of the industry's \$2 billion-plus semiconductor acquisitions occurred in 2015 and five took place in 2016, with three each being announced in 2014, 2011, and 2006, two in 2012, and one each in 2013, 2009, 2000, and 1999.

Semiconductor M&A greatly accelerated in 2015 and continued to be high in 2016 as companies turned to acquisitions to offset slow growth in major end-use applications (such as smartphones, personal computers, and tablets). In the last two years, acquisitions have been driven by companies aiming to expand into huge new markets, especially the Internet of Things, wearable electronics, and highly intelligent embedded systems, such as automated driver-assist features in cars and autonomous vehicles in the future. China's goal of boosting its domestic semiconductor industry has added fuel to the M&A movement.

Breakdown of 2015-2016 M&A Wave



Source: IC Insights

FIGURE 2.

While Chinese moves to buy foreign semiconductor suppliers and assets grabbed a great deal of attention and scrutiny by governments wanting to protect national security and industries, U.S. businesses acquiring other companies, product lines, technologies, and assets accounted for 52% of the 2015-2016 M&A value, or about \$104.5 billion (Figure 2). Asia-Pacific companies were second among those making semiconductor acquisitions with 23% of the \$201.5 billion two-year total, or \$46.4 billion. Within the Asia-Pacific region, China represented 4% of the total, or \$8.3 billion.

Figure 2 also shows a breakdown the 2015-2016 acquisition agreements by semiconductor business types with the purchase of IDMs or parts of those companies being nearly 39% of the two-year total and takeovers of fabless chip suppliers, their product lines, and/or assets representing 45%. Acquisitions of semiconductor-design intellectual property suppliers and IP assets accounted for nearly 16% of the 2015-2016 M&A value while purchase agreements for wafer-foundry businesses and assets represented just 0.2% of the total. ◀

numerous vertical industries. Successful models will revolve around “servitization” and closer, ongoing relationships with end customers, the report says.

Trend #2 – Standardization and security are enabling scalability

- hype surrounding the promise of the IoT marketplace, scaling the IoT is highly dependent on two factors: first, the pace at which devices are connected and second, the ability to manage a large number of devices.
- Currently, diverse standards and technologies make it difficult to evaluate the many technology options available. Stakeholders also must take a holistic, end-to-end view of securing systems comprehensively and move beyond focusing only on device security.
- By 2020, the global market for industrial cybersecurity hardware, software and devices is expected to surpass \$1.8 billion as companies deal with new IoT devices on business networks as well as a new wave of mobile devices connected to corporate networks.

Trend #3 – Business models are keeping pace with IoT technology

- The methods used to monetize the IoT are almost as diverse as the IoT itself. Many pioneers of the IoT sold products to build it. That is still happening, of course, but now there is a shift to reaping the benefits of the data that’s been created.
- An overabundance of business models are being tested to determine which models work and for which applications. Advertising, services, retail and big data are just a few of the areas that have spawned many innovative experiments in monetization. In the coming years, the pace of innovation will slow as successful business models are identified.

Trend #4 – Wireless technology innovation is enabling new IoT applications

- Advances in wireless technologies will continue to extend the IoT at both the low and high ends. At the low end, low-power wide-area network (LPWAN) promises low cost, low power and long range, connecting millions of devices that previously could not be unified in a practical way. At the high end, 802.11ad makes it possible to wirelessly connect very high performance applications such as 4k video.
- Beyond 2020, 5G has the potential to address new, mission-critical use cases, particularly where mobility is essential. By 2020, IHS Markit expects around two billion device shipments by integrated circuit type will feature integrated cellular technology. ◀▶

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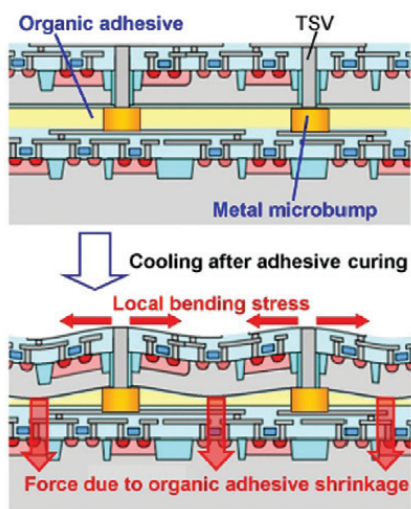
3D Processing at Tohoku U



PHIL GARROU,
Contributing Editor

At the recent IEEE 3DIC Conference, Koyanagi and co-workers at Tohoku Univ reported on their studies of Ti as a 3D TSV barrier layer.

Cu was substituted in the early 2000s for Al interconnect wiring which no longer meet the resistivity requirements in the aggressively scaled technology nodes. Cu, which has low electrical resistivity has proved itself as a potential interconnect material, only if necessary barrier layers are in place.



The most serious concern with Cu as interconnect material is the formation of midgap defects in active Si, since it diffuses fast into the Si. Owing to this, the minority carrier life time is reduced several orders even at 200 °C. Moreover, during this diffusion process

since Cu travels through SiO₂, the insulation nature of SiO₂ is degraded which can result in premature dielectric breakdown leading to device failure. The well-known method to prevent Cu diffusing into SiO₂ and then in Si is to sandwich an amorphous metal layer between the Cu and SiO₂. Required properties of a good barrier layer are low internal film stress, high thermal stability and low resistivity. Metals with high melting points are known to have larger activation energy for the diffusion to take place.

Although Ta is best suited as a barrier material based on melting point, Ta has more integrated film stress than Ti film, i.e. a 200nm-thick sputtered Ta film possesses internal stress of 1.4 GPa, whereas the stress in a similar thickness Ti film is 0.8 GPa. Internal stress is the main cause for the delamination of sputtered Ta

films. Thus Ti is a better barrier layer based on internal stress.

One way to improve the barrier performance of Ti, is to use a Ti/TiN structure as barrier layer, but TiN has a large resistivity ($\rho \sim 270 \mu \cdot \text{cm}$).

The Tohoku group has found a simple method to improve the barrier ability of Ti layer is to anneal the TSV structures in vacuum at temperatures up to 400°C. This results in a significant improvement in leakage current characteristics for SiO₂ dielectric. TiSix has been identified at the interface between Cu and SiO₂ during the sputter deposition.

Another presentation by Tohoku University examined the reduction of the keep-out-zone in 3DIC by local stress suppression with negative-CTE filler.

The thinning of the IC chips leads to low flexural rigidity of IC chips. In addition, the CTE of the underfill material is larger than that of metal microbumps. In other words, the underfill material shrinks more compared to metal microbumps. IC chips are bent by this shrinkage after the 3D integration process. This CTE mismatch induces local bending stress in thinned Si chips, and in turn effects the MOSFET electrical performance in thinned Si chips.

In general, SiO₂ or Al₂O₃ filler have been introduced into the underfill to reduce the CTE of underfill. High density filler is required to realize a CTE close to the value of the microbumps. However, it is difficult to use the conventional density underfill for 3D IC with fine pitch microbumps due to its high viscosity. What's required is a low viscosity low CTE underfill.

The Tohoku group suggests a negative CTE material as the filler to suppress the local bending stress. They used manganese nitride-based negative-CTE material as filler. The CTE of this material is -45 ppm/K at the temperature from 65 °C to 100 °C. ◀

Packaging



Photonics in Silicon R&D Toward Tb/s



ED KORCZYNSKI,
Sr. Technical Editor

The client:server computing paradigm colloquially referred to as the “cloud” results in a need for extremely efficient Cloud server hardware, and from first principles the world can save a lot of energy resources if servers run on photonics instead of electronics. Though the potential for cost-savings is well known, the challenge of developing cost-effective integrated photonics solutions remains. Today, discrete compound-semiconductor chips function as transmitters, multiplexers (MUX), and receivers of photons, while many global organizations pursue the vision of lower-cost integrated silicon (Si) photonics circuits.

Work on photonics chips—using light as logic elements in an integrated circuit—built in silicon (Si) has accelerated recently with announcements of new collaborative research and development (R&D) projects. Leti, an institute of CEA Tech, announced the launch of a European Commission Horizon 2020 “COSMICC” project to enable mass commercialization of Si-photonics-based transceivers to meet future data-transmission requirements in data centers and super computing systems.

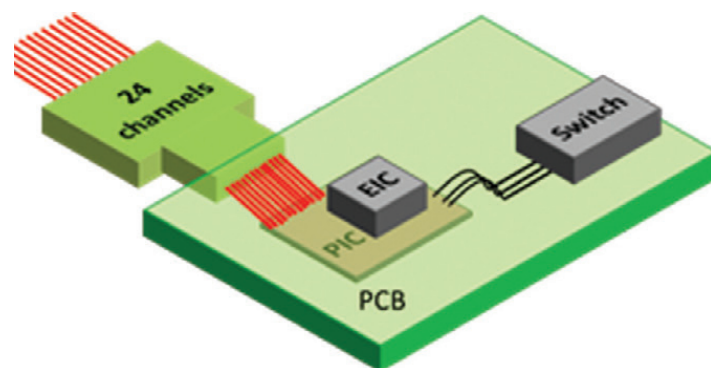


FIGURE 1. Schematic of COSMICC on-board optical transceiver at 2.4 Tb/s using 50 Gbps/wavelength, 4 CWDM wavelengths per fiber, 12 fibers for transmission and 12 fibers for reception. (Source: Leti)

The Leti-coordinated COSMICC project will combine CMOS electronics and Si-photonics with innovative fiber-attachment techniques to achieve 1 Tb/s data rates. These scalable solutions will provide performance improvement an order of magnitude better than current VCSELs transceivers, and the

COSMICC-developed technology will address future data-transmission needs with a target cost per bit that traditional wavelength-division multiplexing (WDM) transceivers cannot meet. The project’s 11 partners from five countries are focusing on developing mid-board optical transceivers with data rates up to 2.4 Tb/s with 200 Gb/s per fiber using 12 fibers. The devices will consume less than 2 pJ/bit, and cost approximately 0.2 Euros/Gb/s.

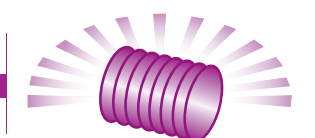
A first improvement will be the introduction of a silicon-nitride (SiN) layer that will allow

development of temperature-insensitive MUX/DEMUX devices for coarse WDM operation, and will serve as an intermediate wave-guiding layer for optical input/output. The partners will also evaluate capacitive modulators, slow-wave depletion modulators with 1D periodicity, and more advanced approaches. These include GeSi electro-absorption modulators with tunable Si composition and photonic crystal electro-refraction modulators to make micrometer-scale devices. In addition, a hybrid III-V on Si laser will be integrated in the SOI/SiN platform in the more advanced transmitter circuits.

Meanwhile in the United States, Coventor, Inc. is collaborating with the Massachusetts Institute of Technology (MIT) on photonics modeling. MIT is a key player in the AIM Photonics program, a federally funded, public-private partnership established to advance domestic capabilities in integrated photonic technology and strengthen high-tech U.S.-based manufacturing. Coventor will provide its SEMulator3D process modeling platform to model the effect of process variation in the development of photonic integrated components.

“Coventor’s technical expertise in predicting the manufacturability of advanced technologies is outstanding. Our joint collaboration with Coventor will help us develop new design methods for achieving high yield and high performance in integrated photonic applications,” said Professor Duane Boning of MIT. Boning is an expert at modeling non-linear effects in processing, many years after working on the semiconductor industry’s reference model for the control of chemical-mechanical planarization (CMP) processing. ◀

Semiconductors



Chips must learn how to feel pain and how to cure themselves

FRANCKY CATTHOOR and GUIDO GROESENEKEN, imec, Leuven, Belgium

Two specialists in the field explain how to make self-healing chips.

Transistor scaling has brought us a lot of benefits, but also a myriad of reliability issues. To extend the scaling path as far as possible, system architects and technologists have to work together. They have to find solutions – e.g. at system level – to realize self-healing chips, chips that can detect or ‘feel’ where errors occur and that know how to deal with them or in a way ‘cure’ them. Only then will it be feasible to design systems in technologies with transistors scaled down to 5nm dimensions. Two specialists in the field explain how to make such self-healing chips: ‘system architect’ Francky Catthoor and ‘technologist’ Guido Groeseneken.

Until a few years ago, manufacturers of ICs in less-deeply scaled CMOS technology could sell electronics with a guaranteed lifetime. The chips inside were built with devices that all had the same average characteristics and would all age in a predictable way. A so-called guard-band approach guaranteed proper functioning of the circuits and chips: extra margins were added to the average characteristics of the transistors to ensure good functioning, also in extreme scenarios. Due to scaling and related reliability issues, these margins or guard bands have risen from 10% to much higher ranges. As a result, from 14nm on, the guard-band approach will become gradually untenable for systems that require some type of guarantees. Does this mean the premature end of scaling?

Making reliable systems with unreliable devices

Groeseneken: “Maybe it means the end of the guard-band approach (**FIGURE 1**), but certainly not the end of scaling. In the past, the reliability of a system was for the larger part guaranteed by the technology engineers. But very soon this will no longer be possible, and we

are reaching a point where we, technology engineers, have to work together with system architecture experts to design reliable systems using ‘unreliable’ devices. In our research group, we measure and try to understand reliability issues in scaled devices. In the 40nm technology, it is still possible to cope with the reliability issues of the devices and make a good system. But at 7nm, the unreliability of the devices risks to affect the

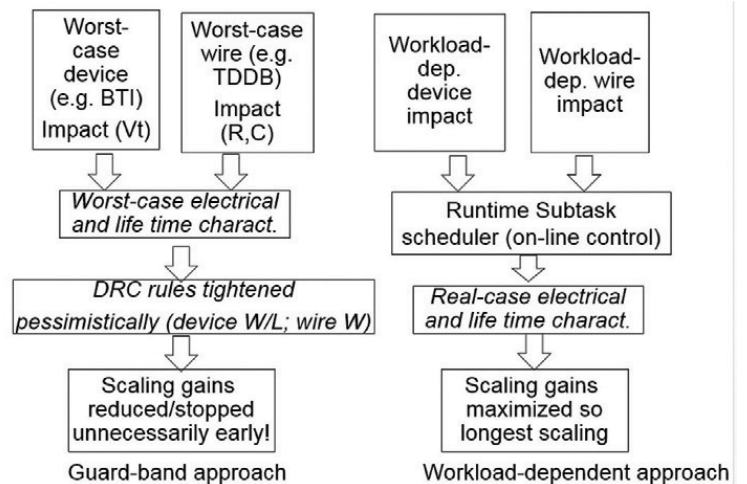


FIGURE 1. The guard-band approach based on corner points becomes untenable for systems based on technology nodes beyond 14 nm. This article proposes a workload-dependent model.

whole system. And conventional design techniques can’t stop this from happening. New design paradigms are therefore urgently needed.”

Device aging becomes a very complex matter in scaled technologies. Groeseneken: “First of all, even with a fixed workload, the devices no longer degrade in a uniform way. Each individual device shows its own

GUIDO GROESENEKEN is a scientific fellow at imec, covering research fields of advanced devices and reliability physics of sub-10nm CMOS technologies. He is also program director of the imec PhD program. FRANCKY CATTHOOR is an imec fellow and part-time full professor at the EE department of the KU Leuven.

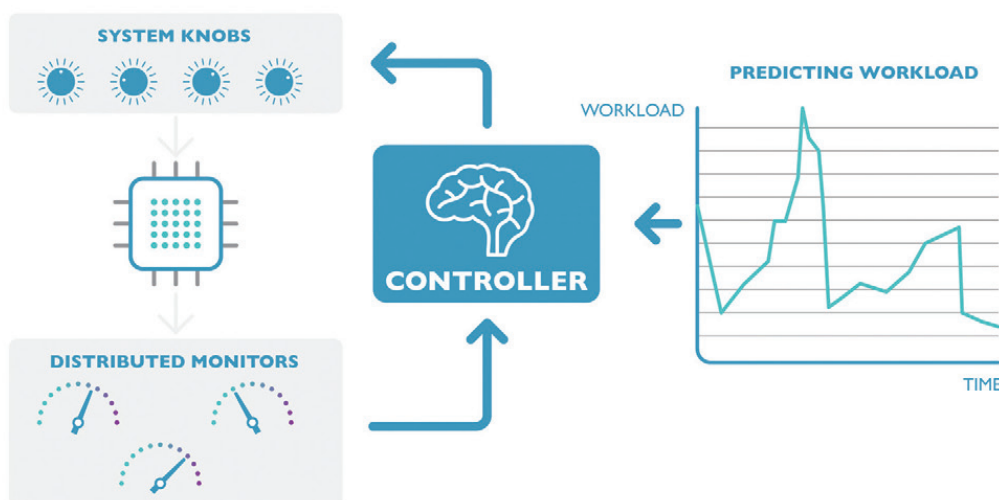


FIGURE 2. Future systems will include distributed monitors that detect local errors in the system, an intelligent controller that gathers this information and decides what to do, and knobs (actuators) that are regulated by the controller to fix the problem.

degradation level, so we have to start looking at the statistical distributions of degradation. And to make things worse, in a real system, the workload is not fixed. Just imagine a multimedia application in which the workload is dependent on the users' instructions to the system. This workload dependence makes it very complex to predict the degradation of scaled devices in a system."

Catthoor: "However, workload dependence doesn't have to be negative. Ultimately, it even holds the key to the solution we are working on to make reliable systems with deeply scaled devices. Future systems will have distributed monitors that detect local errors in the system, an intelligent controller that gathers this information and decides what to do, and so-called knobs (actuators) that are regulated by the controller and fix the problem (**FIGURE 2**)."

Groeseneken: "You could compare it with our body where the nervous system detects where the pain or infection is situated, sends the results to the brain which is the control organ that steers cells to fix the problem or make the body react to avoid the cause of the pain. We can indeed learn a lot from the way evolution has made the most sophisticated system ever: our body and the human brain."

Monitoring the chip's pain

The first requirement to make self-healing chips is to have a distributed monitor that can detect the chip's pain very locally. Groeseneken: "There are various

kinds of device variability that need to be monitored. First of all: the time-zero variability. This is the variation that exists in scaled devices, just after fabrication. Each transistor behaves slightly differently, even before they experience any kind of workload. This can be due to process variations during fabrication of the devices but is more and more dominated by so-called 'intrinsic' sources such as random dopant fluctuations or line edge roughness. This time-zero variability tends to become more

important with deeply scaled devices. Secondly, there is a time-dependent variability: each device or transistor ages in a different way during the system's operation. This can again be caused by differences in workload but also by intrinsic mechanisms such as random defect trapping in small devices. One has to make a distinction



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between functional reliability issues which affect the digital behavior of the device, and parametric reliability problems that affect the parameters of the device such as delay, power consumption, signal-to-noise ratio (SNR).”

The reliability of both the circuits and the whole system depends on the time-zero variability and the time-dependent variability of the devices. Catthoor: “And because these variations become more and more unpredictable, monitors are needed for both. A lot of research has been done on these monitors, especially in the academic world, and some are already in use today. For example, most chips today have functional monitors. In memories, where such error detection is rather easy to integrate and execute by doing a parity check. But even in arithmetic data paths, although less straightforward, functional monitors are developed and partly already in use today. Parametric monitors are less common for the moment. They are mainly used in highly-scaled high-performance applications.

An intelligent controller to heal the chip’s functional and parametric pain

The most important part of future self-healing chips is the controller. This chip’s brain will have to deal with both functional and parametric errors. Catthoor: “Both are linked to one another, but it’s important to fix the cause of the problem, not to focus on the consequences. If delay is the problem, then of course the functional behavior of the devices will be different too, but delay is the cause. On the other hand, if bit flipping is locally detected, than functional reliability mitigation has to be executed.”

Functional reliability mitigation is the healing of functional errors. Catthoor: “Functional reliability mitigation is used in scaled memories (e.g. 90nm). Just think of error-correcting code (ECC) memories in which bit flip problems are detected and corrected. Because in memories the focus is on density and scaling, the related problems and solutions typically first pop up here. With further scaling of memory cells, the ECC becomes more complex,

more distributed and eventually the cost will become too high. New techniques are needed.”

Together with top university EPFL (École polytechnique fédérale de Laussane) imec is working on workload-dependent functional mitigation techniques for memories and data paths. Catthoor: “There are three levels at which mitigation can be integrated. Circuit-level mitigation is very generic and can thus be used for every architecture style and application, but it implies an overhead in area and energy. The other extreme is mitigation at application level. This one is very specific but has to be redeveloped for every new application. Most companies don’t want to do this because of the high implied system design cost. In between, there is the mitigation at system-architecture level. This is not too specific and doesn’t create too much overhead. Imec, together with its academic partners, focuses on architecture-level mitigation and circuit-level mitigation (the latter only when fabrication cost can be kept low).

Also for parametric reliability issues, we are developing workload-dependent techniques. Again, our academic partners play a key role. Together with TU Delft we develop circuit-level mitigation techniques for SRAMs. And with NTU Athens we work on architecture-level mitigation techniques. Together we are developing a partly proactive system scenario-based controller. This controller prevents delay errors from propagating and causing damage at the system level. At the device level you can’t prevent these errors, but at the system level you can prevent them from doing harm. The collaboration with research teams like the one of Guido Groeseneken is very important because they provide us with the data and the models for the failure mechanisms that have to be used in the mitigation techniques.”

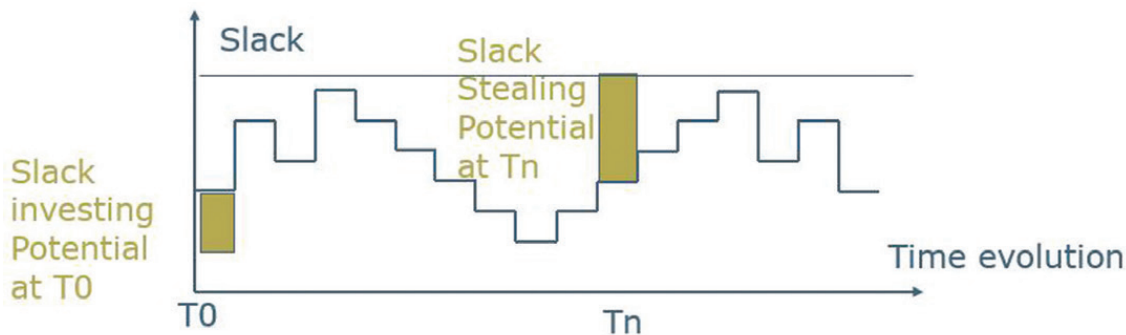


FIGURE 3. Self-healing chips could use the workload variation of the system for their benefit. Based on a deterministic predictor of the future, future slack is determined and used to compensate for the delay error and mitigate at peak load.

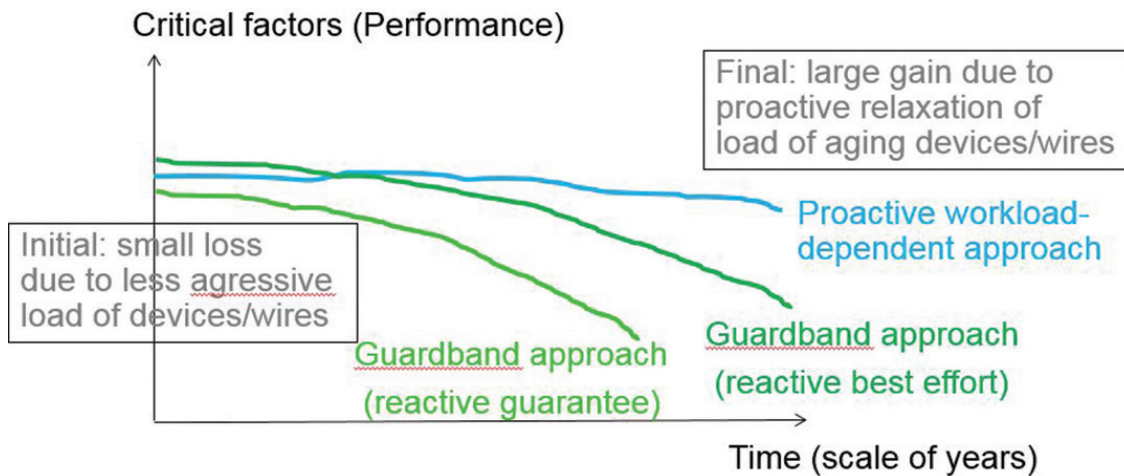


FIGURE 4. The proactive reliability mitigation approach based on the workload dependence implies a small initial loss in performance at time zero, but a large gain in system reliability over the years.

Groeseneken: “The big advantage for imec of doing this work is that we have all expertise needed under one roof, which puts us in a quite unique position to do this research”.

A fortuneteller for self-healing chips

The ultimate goal of imec and its academic partners is to develop a fully proactive parametric reliability mitigation technique with distributed monitors, a control system and actuators, fully preventing the consequence of delay faults and potentially also of functional faults (**FIGURES 3 and 4**). Catthoor: “The secret to the solution lies in the workload variation of the system. Based on a deterministic predictor of the future, you determine future slack and use this to compensate for the delay error at peak load. Based on this info on the future, you change the scheduling order and the assignment of operations.” Groeseneken: “Only with this self-healing approach (the fully proactive approach), we will be able to scale down to 5nm technologies. Actually, I believe that this approach is also present in our human body. Our brain and body are not designed (by evolution) to constantly cope with peak loads, but they keep in mind that in the future better times will come and use this slack to cope with current peak loads.”

Catthoor: “Workload-dependent modeling is essential to making reliable systems with scaled and unreliable devices. Imec brings together the knowledge on monitors, controllers and knobs that is being developed at the universities. We combine this with the knowledge from our technology people to work out simulations

and develop a fully proactive mitigation approach for future chips. The interactions we have with industrial partners allow us to develop an industry-relevant technique. I expect that by 2025, the industry will make true self-healing chips, and consumers will use truly reliable systems and applica-

tions. As in so many fields, the solution lies in collaboration. In bringing the expertise of technologists and system architects together, and in combining the essential contributions of academic groups and research centers that bring the early concepts in reach of the industry and society.”

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Innovations at 7nm to keep Moore's Law alive

DAVID LAMMERS, Contributing Editor

EUUV, cobalt contacts, are expected to be introduced at the 7nm node by several semiconductor manufacturers

Despite fears that Moore's Law improvements are imperiled, the innovations set to come in at the 7nm node this year and next may disprove the naysayers. EUV lithography is likely to gain a toehold at the 7nm node, competing with multi-patterning and, if all goes well, shortening manufacturing cycles. Cobalt may replace tungsten in an effort to reduce resistance-induced delays at the contacts, a major challenge with finFET transistors, experts said.

While the industry did see a slowdown in Moore's Law cost reductions when double patterning became necessary

several years ago, Scotten Jones, who runs a semiconductor consultancy focused on cost analysis, said Intel and the leading foundries are back on track in terms of node-to-node cost improvements.

Speaking at the recent SEMI Industry Strategy Symposium (ISS), Jones said his cost modeling backs up claims made by Intel, GlobalFoundries, and others that their leading-edge processes deliver on die costs (**FIGURE 1**). Cost improvements stalled at TSMC for the 16nm node due to multi-patterning, Jones said. "That pause at TSMC fooled a lot of people. The reality now may surprise those people who

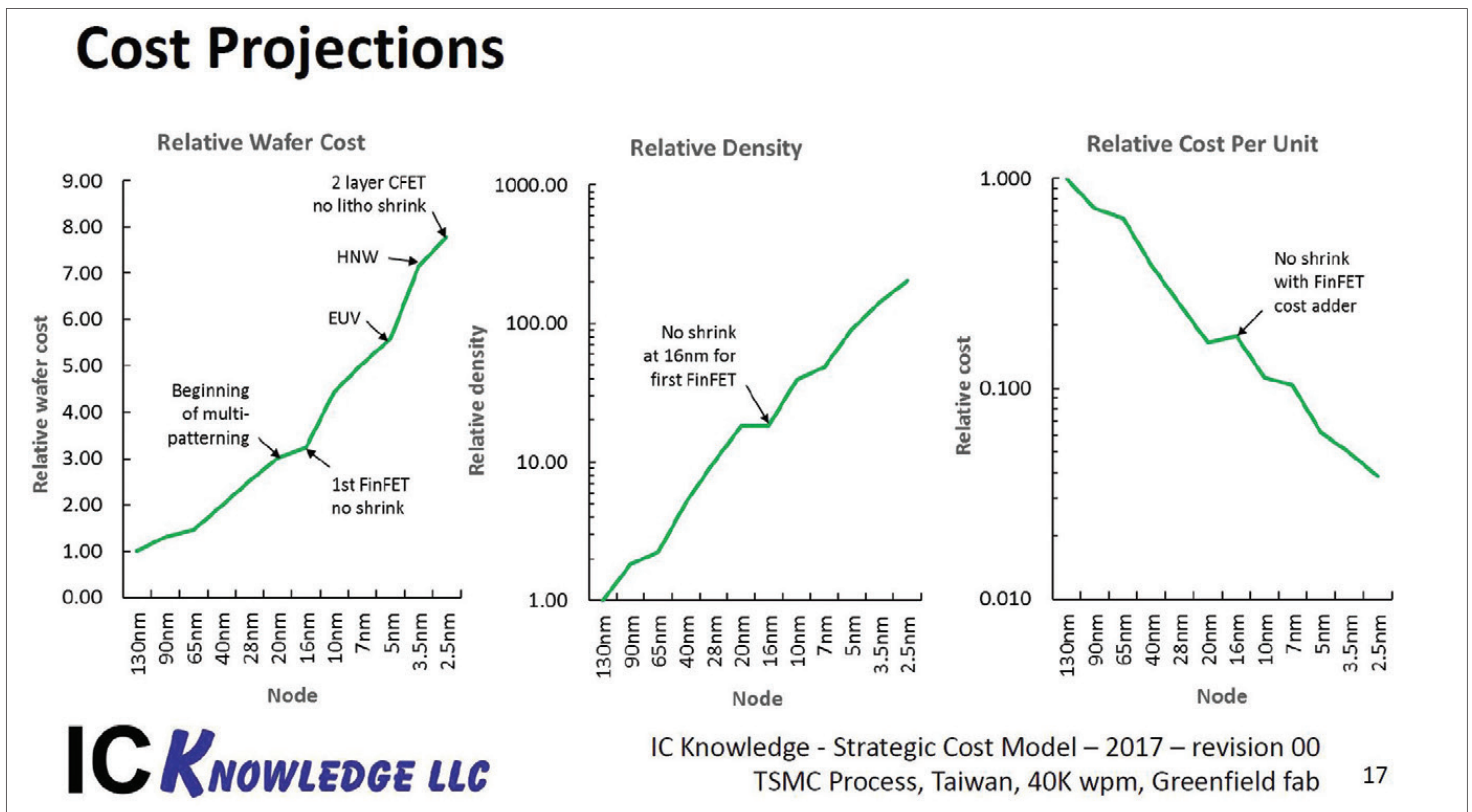


FIGURE 1. IC Knowledge cost models show the chip industry is succeeding in scaling density and costs. (Source: Scotten Jones presentation at 2017 SEMI ISS)

said Moore's Law was dead. I don't believe that, and many technologists don't believe that either," he said.

As Intel has adopted a roughly 2.5-year cadence for its more-aggressive node scaling, Jones said "the foundries are now neck and neck with Intel on density." Intel has reached best-ever yield levels with its finFET-based process nodes, and the foundries also report reaching similar yield levels for their FinFET processes. "It is hard, working up the learning curve, but these companies have shown we can get there," he said.

TSMC, spurred by its contract with Apple to supply the main iPhone processors, is expected to be first to ship its 7nm products late this year, though its design rules (contacted poly pitch and minimum metal pitch) are somewhat close to Intel's 10nm node.

While TSMC and GlobalFoundries are expected to start 7nm production using double and quadruple patterning, they may bring in EUV lithography later. TSMC has said publicly it plans to exercise EUV in parallel with 193i manufacturing for the 7nm node. Samsung has put its stake in the ground to use EUV rather than quadruple patterning in 2018 for critical layers of its 7nm process. Jones, president of IC Knowledge LLC, said Intel will have the most aggressive CPP and MPP pitches for its 7nm technology, and is likely to use EUV in 2019-2020 to push its metal pitches to the minimum possible with EUV scanners.

EUV progress at imec

In an interview at the 62nd International Electron Devices Meeting (IEDM) in San Francisco in early December, An Steegen, the senior vice president of process technology at Imec (Leuven, Belgium), said Imec researchers are using an ASML NXE 3300B scanner with 0.3 NA optics and an 80-Watt power supply to pattern about 50 wafers per hour.

"The stability on the tool, the up time, has improved quite a lot, to 55 percent. In the best weeks we go well above 70 percent. That is where we are at today. The next step is a 125-Watt power supply, which should start rolling out in the field, and then 250 Watts."

Steegen said progress is being made in metal-containing EUV resists, and in development of pellicles "which can withstand hydrogen in the chamber."

If those challenges can be met, EUV would enable single patterning for vias and several metal layers in the middle of the line (MOL), using cut masks to print the metal line ends. "For six or seven thin wires and vias, at the full (7nm

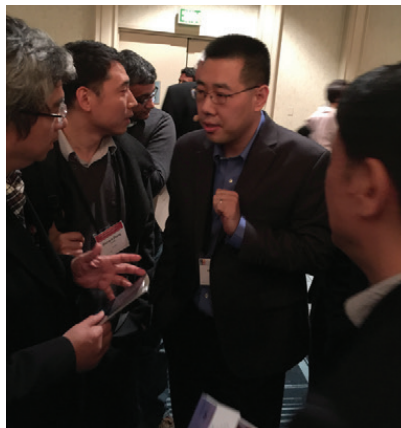


FIGURE 2. Huiming Bu was peppered with questions following a presentation of the IBM Alliance 7nm technology at IEDM.

node) 32nm pitch, you can do it with a single exposure by going to EUV. The capability is there," Steegen said.

TSMC's 7nm development manager, S.Y. Wu, speaking at IEDM, said quadruple patterning and etch (4P4E) will be required for critical layers until EUV reaches sufficient maturity. "EUV is under development (at TSMC), and we will use 7nm as the test vehicle."

Huiming Bu (**FIGURE 2**), who presented the IBM Alliance 7nm paper at IEDM, said "EUV delivers significant depth of field (DoF) improvement" compared with the

An advertisement for EtchDefender Technology. The background is a warm, orange-to-yellow gradient with a bokeh effect. At the top, it says "Exclusively from Conax..." in blue. Below that is a blue and silver cylindrical component. The EtchDefender logo, a stylized 'E' in a circle, is on the left, and the text "EtchDefender™ TECHNOLOGY" is on the right. A yellow box contains the text "Coated TCs for the ASM Epsilon™ that last up to 3X longer". At the bottom, it says "Conax introduces EtchDefender™ coating—the patent-pending solution for extending the life of quartz sheath thermocouples. EtchDefender™ increases yield and decreases cost of ownership. Find out more." The Conax Technologies logo is at the bottom right.

A dark blue banner with white text. On the left is the phone number "+1 800 223 2389". On the right is the website "conaxtechnologies.com/ss".

self-aligned quadruple (SAQP) required for the metal lines with immersion scanners.

A main advantage for EUV compared with multi-patterning is that designs would spend fewer days in the fabs. Speaking at ISS, Gary Patton, the chief technology officer at GlobalFoundries, said EUV could result in 30-day reductions in fab cycle times, compared with multiple patterning with 193nm immersion scanners, based on 1.5 days of cycle time per mask layer.

Moreover, EUV patterns would produce less variation in electrical performance and enable tighter process parameters, Patton said.

Since designers have become accustomed to using several colors to identify multi-patterning layers for the 14nm node, the use of double and quadruple patterning at the 7nm node would not present extraordinary design challenges. Moving from multi-patterning to EUV will be largely transparent to design teams as foundries move from multi-patterning to EUV for critical layers.

Interconnect resistance challenges

As interconnects scale and become more narrow, signals can slow down as electrons get caught up in the metal grain boundaries. Jones estimates that as much as 85 percent of parasitic capacitance is in the contacts.

For the main interconnects, nearly two decades ago, the industry began a switch from aluminum to copper. Tungsten has been used for the contacts, vias, and other metal lines near the transistor, partly out of concerns that copper atoms would “poison” the nearby transistors.

Tungsten worked well, partly because the bi-level liner – tantalum nitride at the interface with the inter-level dielectric (ILD) and tantalum at the metal lines – was successful at protecting against electromigration. The TaN-Ta liner is needed because the fluorine-based CVD processes can attack the silicon. For tungsten contacts, Ti serves to getter oxygen, and TiN – which has high resistance — serves as an oxygen and fluorine barrier.

However, as contacts and MOL lines shrunk, the thickness of the liner began to equal the tungsten metal thicknesses.

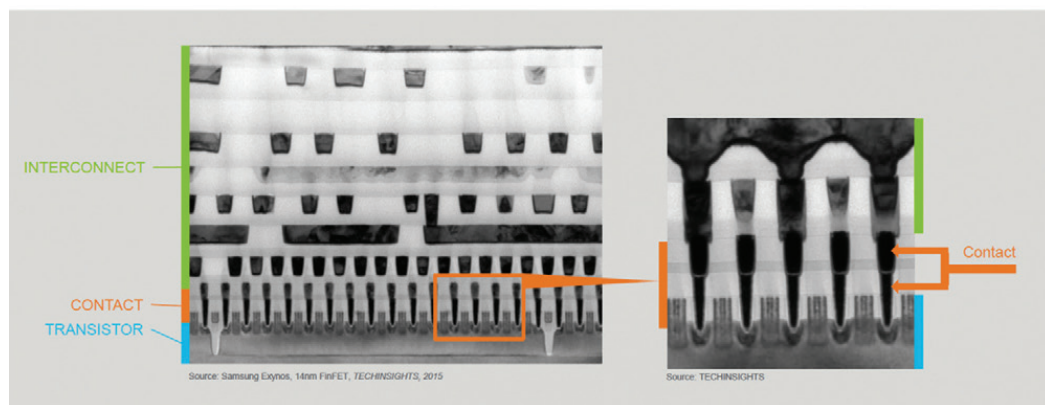


FIGURE 3. Contacts are a “pinch point” and the industry may switch to cobalt (Source: Applied Materials)

Dan Edelstein, an IBM fellow who led development of IBM’s industry-leading copper interconnect process, said a “pinch point” has developed for FinFETs at the point where contacts meet the middle-of-the-line (MOL) interconnects (**FIGURE 3**).

“With cobalt, there is no fluorine in the deposition process. There is a little bit of barrier, which can be either electroplated or deposited by CVD, and which can be polished by CMP. Cobalt is fairly inert; it is a known fab-friendly metal,” Edelstein said, due to its longstanding use as a silicide material.

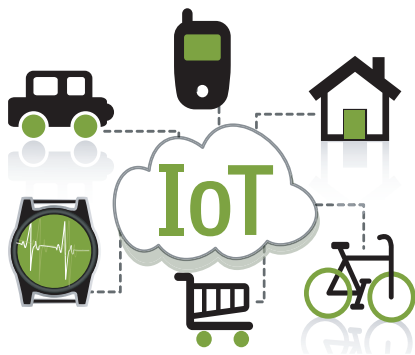
As the industry evaluated cobalt, Edelstein said researchers have found that cobalt “doesn’t present a risk to the device. People have been dropping it in, and while there are still some bugs that need to be worked out, it is not that hard to do. And it gives a big change in performance,” he said.

Annealing advantages to Cobalt

An Applied Materials senior director, Mike Chudzick, writing on the company’s blog, said the annealing step during contact formation also favors cobalt: “It’s not just the deposition step for the bulk fill involved – there is annealing as well. Co has a higher thermal budget making it possible to anneal, which provides a superior, less granular fill with no seams and thus lowers overall resistance and improves yield,” Chudzick explained.

Increasing the volume of material in the contact and getting more current through is critical at the 7nm node. “Pretty much every chipmaker is working aggressively to alleviate this issue. They understand if it’s not resolved then it won’t matter what else is done with the device to try and boost performance,” Chudzick said.

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Prof. Koike strikes again

Innovations underway at a Japanese university aim to provide a liner between the cobalt contact fill material and the adjacent materials. At a Sunday short course preceding the IEDM, Reza Arghavani of Lam Research said that by creating an alloy of cobalt and approximately 10 percent titanium, “magical things happen” at the interfaces for the contact, M0 and M1 layers.

The idea for adding titanium arose from Prof. Junichi Koike at Tohoku University, the materials scientist who earlier developed a manganese-copper solution for improved copper interconnects. For contacts and MOL, the Co-Ti liner prevents diffusion into the spacer oxide, Arghavani said. “There is no (resistance) penalty for the liner, and it is thermally stable, up to 400 to 500 degrees C. It is a very promising material, and we are working on it. W (tungsten) is being pushed as far as it can go, but cobalt is being actively pursued,” he said.

Stressor changes ahead

Presentations at the 2016 IEDM by the IBM Alliance (IBM, GlobalFoundries, and Samsung) described the use of a stress relaxed buffer (SRB) layer to induce stress, but that technique requires solutions for the defects introduced in the silicon layer above it. As a result of that learning process, SRB stress techniques may not come into the industry until the 5nm node, or a second-generation 7nm node.

Technology analyst Dick James, based in Ottawa, said over the past decade companies have pushed silicon-germanium stressors for the PFET transistors about as far as practical.

“The stress mechanisms have changed since Intel started using SiGe at the 90nm node. Now, companies are a bit mysterious, and nobody is saying what they are doing. They can’t do tensile nitride anymore at the NFET; there is precious little room to put linear stress into the channel,” he said.

The SRB technique, James said, is “viable, but it depends on controlling the defects.” He noted that Samsung researchers presented work on defects at the IEDM in December. “That was clearly a research paper, and adding an SRB in production volumes is different than doing it in an R&D lab.”

James noted that scaling by itself helps maintain stress levels, even as the space for the stressor atoms becomes smaller. “If companies shorten the gate length and keep the same stress as before, the stress per nanometer at least maintains itself.”

Huiming Bu, the IBM researcher, was optimistic, saying that the IBM Alliance work succeeded at adding both compressive and tensile strain. The SRB/SSRW approach used by the IBM Alliance was “able to preserve a majority – 75 percent – of the stress on the substrate.”

Jones, the IC Knowledge analyst, said another area of intense interest in research is high-mobility channels, including the use of SiGe channel materials in the PMOS FinFETS.

He also noted that for the NMOS finFETs, “introducing tensile stress in fins is very challenging, with lots of integration issues.” Jones said using an SRB layer is a promising path, but added: “My point here is: Will it be implemented at 7 nm? My guess is no.”

Putting it in a package

Steegeen said innovation is increasingly being done by the system vendors, as they figure out how to combine different ICs in new types of packages that improve overall performance.

System companies, faced with rising costs for leading-edge silicon, are figuring out “how to add functionality, by using packaging, SOC partitioning and then putting them together in the package to deliver the logic, cache, and IOs with the right tradeoffs,” she said. ◀

Executive viewpoints: 2017 outlook

Each year, Solid State Technology turns to industry leaders to hear viewpoints on the technological and economic outlook for the upcoming year. Read through these expert opinions on what to expect in 2017.

Driving the industry forward with materials engineering

Prabu Raja, vice president and general manager, Patterning and Packaging Group, Applied Materials, Inc.



Over the past few years, the industry has made remarkable progress in bringing 3D chip architectures to volume production. In 2017, we will continue to see exciting technology innovations for scaling 3D NAND devices to 64 layers, ramping the 10nm process node into volume manufacturing and increasing the adoption of highly integrated chip packages.

With the transition to the 3D and sub-10nm era, the semiconductor world is changing from lithography-based scaling to materials-enabled scaling. This shift requires multiple new materials and capabilities in selective processing.

The magnitude and pace of these changes are truly disruptive. For example, with 3D NAND materials innovations for hard mask deposition and hard mask etch are essential. The challenge is to build high aspect ratio vertical structures with uniform profiles from the top to the bottom as more layers are added. Selective removal processes can remove targeted materials in vertical and horizontal structures without damage or residue throughout the stack.

For logic/foundry, the introduction of the 10nm process node in volume manufacturing brings significant growth in the number of patterning steps. This trend will increase even more for 7nm and below designs. Patterning these advanced nodes requires innovative etch capabilities to deliver feature-scale uniformity with low line edge roughness. Selective processes and alternative manufacturing schemes will also be needed as the industry seeks

solutions for layer-to-layer vertical alignment. We expect this to result in a two-fold increase in the number of materials to be deposited and removed.

Finally, the industry will continue to adopt new and improved packaging schemes for enabling increased device performance, lower power consumption and to deliver desired form factors. In 2016, we saw the volume adoption of Fan-Out packaging in mobile devices and this trend is expected to grow further in 2017. The high performance computing segment will pursue 2.5D interposer and/or 3D TSV packaging schemes for higher memory bandwidth, lower latency and better power efficiency.

Applied Materials is focused on delivering game-changing selective process technologies and materials innovations to help solve the industry's toughest challenges.

Semiconductor IP... and the impact of multi-die IC design

Bob Smith, Executive Director, Electronic System Design (ESD) Alliance



In the early days of integrated circuits, it was quite a feat to produce chips that contained a few hundred transistors. Of course, that quickly gave way to chips with thousands of transistors and ... Moore! Today's largest SoCs contain an astounding 10-billion transistors.

Is the end in sight?

Some industry pundits declare that the end of Moore's Law is upon us. I disagree. The semiconductor industry is realizing that Moore's Law will continue on, but in different ways than previously considered. In fact, the rapid growth

of semiconductor IP and new packaging technologies are catalysts enabling this shift based on a new semiconductor world view that is moving from transistor-centric to system-centric.

The emerging wave of building systems based on multi-die ICs is changing the industry's thinking about Moore's Law. Rather than counting the number of transistors integrated into a single die, the move to multi-die considers the functionality achieved by integrating functional building blocks instead of discrete transistors. This is Moore's Law at work, but the atomic level is moving up a level to building blocks instead of discrete transistors.

The explosion in IoT is another key driver as it demands the integration of heterogeneous functions such as sensors/actuators, optical, analog, mixed-signal and memory components. The market size for these functions, \$187 billion, is actually greater than the market for logic functions. They are also a near perfect fit for multi-die ICs since the restriction of using a single process is gone because each function or die can be implemented in the optimal process. Benefits to adopting multi-die and the advanced packaging technologies are enormous, from higher performance and 3x power reduction to overall lower cost.

In total, multi-die IC design is system design and will extend Moore's Law because it integrates functional blocks to build a system. Semiconductor IP and advanced packaging technologies that eliminate the interconnect overhead will be the drivers for multi-die IC.

What's required is a meeting of the minds among tool providers, designers and manufacturers to drive multi-die IC design as the way to extend the life of Moore's Law. If the semiconductor industry agrees, design will become more system-centric as a result of these shifts and a new way of exploiting Moore's Law.

2017: The mobile and digital revolution is driven by innovative materials

Paul Boudre, CEO of Soitec



For decades, electronics have contributed tremendously to the advancement of human lives, with PCs and smart phones serving as prevalent examples. But now we are at the beginning of enormous digital transformations that will revolutionize all aspects of society. It starts with IoT, autonomous driving,

5G communications and cloud computing extending to virtual reality, augmented reality and artificial intelligence. These trends have been evident over the last few years, but 2016 brought many of them into reality. In 2017, we will see a strong acceleration in the technologies' maturity and widespread adoption.

Creating disruptive applications requires more than just increased computing speed. Very low power consumption, integration of analog and sensing functions, immunity to radiation and the ability to combine silicon and non-silicon materials must be achieved – and at costs enabling mass markets.

Semiconductor materials are vitally important in meeting these objectives. Now more than ever, engineered materials are enabling the device-level performance to address these challenges and opportunities. For example, radio-frequency silicon-on-insulator (RF-SOI) and fully depleted SOI (FD-SOI) have become industry standards for wireless and digital applications, respectively.

As a substrate engineering innovator and supplier, we are working with our customers —and with the customers of our customers—to understand and anticipate their needs. We must provide solutions that help them differentiate themselves by creating truly innovative, breakthrough products for both established and emerging markets.

Using RF-SOI substrates, front-end modules have brought 4G LTE capabilities to all mobile devices. This technology will remain instrumental in attaining 5G specifications in sub-6-GHz frequency bands while other types of SOI engineered substrates will be used for millimeter-wave applications. In 2017, we are expecting significant advancements in defining material solutions for 5G applications.

On the digital side, FD-SOI brings unique value propositions of PPA (Power - Performance - Area) with analog integration capabilities, all at very competitive

costs. Staying planar also allows designers to really integrate RF, analog and digital functions in one device. That's an untouchable advantage for FD-SOI in key mobility, industrial and automotive applications. With this technology being widely adopted across all mobile applications at multiple technology nodes by leading foundries, including Samsung and GlobalFoundries, 2017 will be the year of FD-SOI.

Credible IoT customers are emerging, and the first consumer product is a proof point of what's coming. The latest GPS from Sony is already available in a smart watch.

Built on 28nm FD-SOI, it cuts power consumption by a factor of 10. This new GPS will go into watches, as well as home and industrial applications.

Chip reliability is one of the top requirements in cars. This is where FD-SOI brings a major differentiation versus other semiconductor technologies. Leaders in automotive semiconductors such as NXP and Mobileye have been the first adopters of FD-SOI based chips. In 2017, we will see end products from these companies reaching the market as well as a big upsurge in design announcements on FD-SOI from many fabless companies with strong support from leading foundries.

In addition, the Smart Cut™ layer-transfer standard technology used in making SOI wafers also can bring compound materials into the silicon world. This approach will soon open doors for new applications including power electronics for electric cars, displays for virtual reality, photonics communication for data centers and many others.

In 2017, we will see even more collaborative efforts from market leaders to develop new material solutions for emerging applications destined to reach mass markets in a few years. With SOI and other engineered substrates enabling a new wave of products, our industry and the global electronics market will continue to thrive in the new age of materials.

IoT main industry driver

Chris Davis, SVP, Reno Sub-Systems



The general industry consensus is that 2016 is finishing strong and that this growth is expecting to extend into 2017. From our perspective, the internet of things (IoT) is driving this, but not from the sensor/device-level applications (although certainly, with billions of devices predicted, this too will be good for manufacturers). The true drivers are big data and all the things associated with storing, transmitting and processing the data. There is significant demand for faster processors and more memory—needed to move the data and analyze it, not to mention the need for more processors and ICs to meet emerging bandwidth requirements. We also anticipate fewer cycles and expect demand to be more consistent.

There are many trends that bear watching that play into this outlook. Sensors are the tip of the iceberg; they will be in everything, but it is the data they generate that demands more infrastructure. Several applications are all actively progressing that will further drive the industry: artificial intelligence, deep machine learning, autonomous cars, robots, augmented/virtual reality, drones, 3D camera/data.

So what does this mean in the semiconductor industry? There is a drive, in both memory and processors, for smaller geometries so that chips can do more in a smaller space with less power. Nodes will continue to shrink to put more capability into the same size chips. The industry is just at the beginning of the move to 10nm and below, and new technologies will be needed to enable continued shrink.

Advanced packaging, chip stacking and 3D are all on the radar, but there remain improvements to front-end manufacturing that will drive the industry forward; subsystems offer one example. As etch and deposition process steps become more critical, higher precision and control are required as well as reduced process times to improve cost of ownership. Advanced RF matching and gas flow capabilities need to offer faster, multilevel pulsing and move beyond conventional RF matches—which already can't keep up. We look forward to working with original equipment manufacturers and independent device manufacturers to understand and solve these issues to enable the rapid growth we anticipate from the IoT.

2017: A transformative year for through-silicon vias (TSVs)?

By Frédéric Raynal, *aveni*



What do we predict will be major technology drivers for 2017? While bleeding-edge foundries and integrated device manufacturers (IDMs) are publicly discussing the challenges to manufacture devices at the 10nm and 7nm nodes, we know there is much they are not talking about. Such as, how long will copper remain viable for metallization? When will radical material and the associated structural changes require implementation? Will 2017 be the transformative year when through-silicon vias (TSVs) reach mainstream adoption?

We believe logic devices as we know them today will continue to be manufactured, but with some caveats. FinFETs (fin field-effect transistors) still will be used in front end of line (FEOL). Likewise, copper metallization for back end of line (BEOL) is extendible to the 3nm node, provided dimensions do not physically limit the material choice. Conventional acidic copper electrochemical deposition (ECD) is reaching its limits at the 10nm and 7nm nodes, with high likelihood that only alkaline chemistries will meet requirements.

Cobalt (Co) electroplating is in active development to replace tungsten chemical vapor deposition (CVD-W) for middle of line (MOL) ≤ 7 nm. Device designers are driving this material change because Co can be electrodeposited with a bottom-up approach, whereas CVD-W's inherently conformal deposition becomes a liability at smaller geometries.

On a related note, some device manufacturers are moving to Co for BEOL at ≤ 10 nm, which imposes requisite cost increases, delays due to development and reduced chip performance. Concerns about copper electromigration are driving this change. Marginal seed layers have compromised the reliability of devices metallized with acidic copper chemistries for ECD. Alkaline chemistries can delay transition from copper to unconventional metallization schemes, while maintaining high device reliability, to at least the 3nm node. However, 2nm is widely considered to be the technology disruption point for new integration schemes, be they carbon nanotubes or others.

Finally, we won't predict that 2017 will be the breakthrough year for TSVs. They will remain as niche applications: most notably, high-bandwidth memory and CMOS image sensors.

Greater collaboration for 2017 and beyond

Colin Cameron, Global Pads Business Director, CMP Technologies, Dow Electronic Materials

The global semiconductor industry is on the upswing right now, and we expect to see this extend into 2017. With respect to end-use markets driving the most growth, smartphones continue to be a major contributor. After a few years of declining growth, the PC market is leveling off and still comprises a significant share. Among the other notable segments are tablets, servers, and automotive.

Advanced storage applications such as servers and solid state drives are fueling growth in advanced chips and are creating new uses for 3D NAND flash memory, which is being increasingly used to store higher quantities of data in as small a footprint as possible. Going vertical increases density and generally reduces cost. The manufacturing process brings additional challenges compared to 2D, especially when considering the increased planarization needed for the increase in layers and their respective thicknesses. This puts more demand on the chemical mechanical polishing (CMP) step, which is being used to a greater extent.

This year, we're seeing the emergence of production at the 10nm node, supporting trends in consumer devices such as advanced smartphone design and high-end graphic processors to support streaming video. Implementation for 10nm has shown the tremendous value in deeper collaboration between semiconductor manufacturers and materials suppliers. Manufacturers are increasingly in need of customized solutions, and suppliers are working more directly with their customers to ensure that advanced technologies can be manufactured reliably.

China's semiconductor market has been growing rapidly, and its local IC industry continues to develop, with manufacturers bringing new production on line and more new construction starting in 2017. This scaling is creating demand throughout the semiconductor supply chain.

As a consumables supplier, we've been developing new CMP solutions that offer both performance improvements for future technology nodes as well as cost of ownership benefits for mature nodes. When planning for 7nm and beyond, the smaller geometry will significantly tighten specifications for defect levels and planarization. Narrower process margins may require new materials tailored for each application, making collaboration more critical than ever in the new year.



The Battle for Mobility

Mike Plisinski, CEO, Rudolph Technologies, Inc.

The rapid adoption of technology in our everyday lives—smartphones, tablets, drones, smart homes, and autonomous cars, with more coming—is generating

data in unprecedented volumes, which is driving demand for high-speed processing and storage across the internet. At the same time, it is creating markets for a variety of mobile and connected devices (the Internet of Things) that must integrate multiple functions (sensors, communications, storage, and processing) in the smallest possible volume. As a result, our industry is enjoying a period of exciting expansion across multiple segments, not only in leading-edge processors and advanced memories, but also in advanced packaging and specialty semiconductor chipsets used in communication and sensing.

Advanced packaging, in particular, is going mainstream, as it allows product designers to integrate varied functions and pack more capability into ever smaller volumes—with higher performance at a lower cost. TSMC, for example, has introduced its own integrated fan-out (InFO) process in order to provide this capability. This dynamic will continue to transform fan-out packaging, which initially attracted customers needing small footprints and form factors, but as InFO has shown, has scaled to high value devices like processors, and ultimately, will expand to multi-chip systems-on-package (SoP). As it does, the increasing number of devices with high I/O requirements and the desire to bring chipsets closer together will drive continuing shrinks in re-distribution lines (RDL) and bumps.

And TSMC is not alone. As advanced packaging achieves critical mass, most major manufacturers are pursuing R&D and process development efforts to reduce feature sizes and improve package reliability. Device failures from packaging, especially for advanced logic devices, are very expensive, and package interconnect reliability carries the potential for substantial product liability, hence effective process control methods and product tracking are essential. Smaller geometries will require tighter process control requirements and increased sensitivity in metrology and inspection systems. Improving reliability will depend on identifying and addressing process-specific failure mechanisms, such as saw induced stress (cracks and chips) and residue on interconnects. Other unique requirements, such as uncertainty in die placement on reconstituted substrates, will require integration of both process and process control information to provide a cohesive solution for processes like fan-out lithography on panels.

Advanced packaging is rapidly becoming a differentiator for product manufacturers and a growth enabler for our industry. We expect these themes to be significant drivers for Rudolph and across the industry in 2017. ♦

Technologies to extend semiconductor scaling

AN STEEGEN, Executive Vice President Semiconductor Technology & Systems, imec

An Steegen reveals some of the secrets of semiconductor scaling – a pipeline full of materials, device architectures and advanced techniques that promise to further extend semiconductor scaling.

The explosive growth of data traffic fuels the demand for ever more processing power and storage capacity. Moore's Law continues to be necessary, but innovations are needed beyond this law to help managing the devices power, performance, area and cost.

The end of happy scaling?

Data traffic explosion, fueled by the Internet of Things, social media and server applications, has created a continuous need for advanced semiconductor technologies. Servers, mobile devices, and IoT devices drive the requirements for processing and storage. "At the same time, this trend is also creating more diversification," said An Steegen, Executive Vice President Semiconductor Technology & Systems at Imec (Leuven, Belgium). "IoT devices, for example, will need low-power signal acquisition and processing, and embedded non-volatile memory technologies. For mobile and server applications, on the contrary, further dimensional scaling, continuous transistor architecture innovations and memory hierarchy diversification are among the key priorities."

But will we be able to continue traditional semiconductor scaling, as initiated by Gordon Moore more than 50 years ago? "For a long time, we have lived in the happy scaling era, where every technology node reshrinks and redoubles the number of transistors per area, for the same cost," Steegen said. "But the last 10-12 years, we have not been following that happy scaling path. The number of transistors still doubles, but device scaling provides us with diminishing returns. We've seen these dark periods of 'dark silicon' before, but, fortunately, we've always managed to get out of these periods. Again, the technology box will provide

new features to help manage power, performance and area node by node as we move to the next generation."

The technology box for dimensional scaling

On the dimensional scaling side, extreme ultraviolet lithography (EUVL) is considered an important enabler for continuing Moore's Law. "Ideally, we would need it at the 10nm node, where we will start replacing single exposures with multiple exposures. More realistically, it will hopefully be ready to lower the costs for the 7nm technology," said Steegen. "At imec, we already showed that EUVL is capable of printing 7nm logic dimensions with one single exposure." Still, issues need to be resolved, related to, for example, the line-edge roughness. "At the same time, to enhance dimensional scaling, we increasingly make use of scaling boosters, such as self-aligned gate contact or buried power rail. These tricks allow a standard cell height to be reduced from 9 to 6 tracks, leading to a bit density increase and large die cost reduction - a nice example of design-technology co-optimization."

Improving power/performance in the front-end of line

FinFET technology has been the killer device for the 14 and 10nm technology nodes. But for the 7-5nm, Steegen foresees challenges: "At these nodes, FinFET technology can't meet the 20% performance scaling and 40% power gain anymore. To go beyond 7nm will require horizontal gate-all-around nanowires, which promise better electrostatic control. In such a configuration, the drive current per footprint can be maximized by vertically stacking multiple horizontal nanowires. In 2016, at IEDM, we

AN STEEGEN is imec's Executive Vice President Semiconductor Technology & Systems. In that role, she heads the research hub's efforts to define and enable next-generation ICT technology and to feed the industry roadmaps.

demonstrated for the first time the CMOS integration of vertically stacked gate-all-around Si nanowire MOSFETs. Vertical nanowires, although requiring a more disruptive process flow, could be a next step. Or junction-less gate-all-around nanowire FET devices, which, as shown at the 2016 VLSI conference, appear as an attractive option for advanced logic, low-power circuits and analog/RF applications.” Further down the road, from the 2.5nm node onwards, fin/nanowire devices are expected to run out of steam. “Sooner or later, we will need to find the next switch,” she said. “Promising approaches are tunnel-FETs, which can provide a 3x drive current improvement, and spin-wave majority gates.” Spin-wave majority gates with micro-sized dimensions have already been reported. But to be CMOS-competitive, they must be scaled and handle waves with nanometer-sized wavelengths. An Steegen: “In 2016, imec proposed a method to scale these spin-wave devices into nanometer dimensions, opening routes towards building spin-wave majority gates that promise to outperform CMOS-based logic technology in terms of power and area reduction.”

Extending or replacing Cu in the back-end-of-line

Looking ahead, it might as well be the interconnect that will threaten further device scaling. Therefore, the back-end-of-line (BEOL) and the struggle to keep scaling the BEOL needs attention as well. “We look at ways to extend the life of Cu, for example with liners of ruthenium (Ru) or cobalt (Co). On the longer term, we will probably need alternative metals, such as Co for local interconnects or vias,” says Steegen.

The future memory hierarchy

Besides a central processing unit, memory to store all the data and instructions is another key element of the classical Von Neumann computer architecture. The ever increasing performance of computation platforms and the consumer’s hunger for storing and exchanging ever more data drive the need to keep on scaling memory technologies. Besides this scaling trend, existing memories that make up today’s memory hierarchy are challenged with the need for new types of memory. Steegen said: “STT-MRAM, for example, is an emerging memory concept that has the potential to become the first embedded non-volatile memory technology on advanced logic nodes for advanced applications. It is also an attractive

technology for future high-density stand-alone applications. It promises non-volatility, high-speed, low-voltage switching and nearly unlimited read/write endurance. But its scalability towards higher densities has always been challenging. Recently, we have been able to demonstrate a high-performance perpendicular magnetic tunnel junction device as small as 8nm, combined with a manufacturable solution for a highly scalable STT-MRAM array.” The future memory landscape also requires a new type of memory able to fill the gap between DRAM and solid-state memories: the storage class memory. This memory type should allow massive amounts of data to be accessed in very short latency. Imec is working there on MRAM and resistive RAM (RRAM) approaches.

Beyond classical scaling – towards system-technology co-optimization

A challenge for traditional Von Neumann computing is to increase the data transfer bandwidth between the processing chip and the memory. And this is where 3D approaches enter the scene. Said Steegen: “With advanced CMOS scaling, new opportunities for 3D chip integration arise. For example, it becomes possible to realize different partitions of a system-on-chip (SoC) circuit and heterogeneously stacking these partitions with high interconnect densities. At the smallest partitions, chips are no longer stacked as individual die, but as full wafers bonded together.” An increased bandwidth is also enabled by optical I/O. In this context, imec continues its efforts to realize building blocks (e.g. optical modulators, Ge photodetectors) with 50Gb/s channel data rate for its Si photonics platform.

Moore’s Law will continue, but not only through the conventional routes of scaling. “We have moved from pure technology optimization (involving novel materials and device architectures) to design-technology co-optimization (e.g. the use of scaling boosters to reduce cell height). And we are already thinking ahead about a next phase, system-technology co-optimization. And to keep computing power improving, we are exploring ways beyond the classical Von Neumann model, such as neuro-morphic computing, a brain-inspired computer concept and quantum computing, which exploits the laws of quantum physics. There are plenty of creative ideas that will allow the industry to further extend semiconductor scaling,” Steegen concluded. ◀

Hitback analysis improves defect visibility

CHET LENOX, DAVID W. PRICE and **DOUGLAS G. SUTHERLAND**, KLA-Tencor, Milpitas, CA

When performed properly, the hitback capture rate metric (in percentage) will quantify the number of fails which “hitback” to inline defects.

In order to maximize the profitability of an IC manufacturer’s new process node or product introduction, an early and fast yield ramp is required. Key to achieving this rapid yield ramp is the ability to provide quality and actionable data to the engineers making decisions on process quality and needed improvements.

The data used to make these decisions comes in two basic forms:

- Inline inspection and metrology results
- End-of-line (EOL) parametric testing, product yield results and failure-analysis

Inline inspection and metrology serve as the primary source of data for process engineers, enabling quick identification of excursions and implementation of corrective actions. End-of-line results serve as a metric of any process flow’s ability to produce quality product, generating transistor parametrics, yield sub-binning and physical failure analysis (PFA) data that provide insight into process quality and root-cause mechanisms.

In general, a fab is better off financially by finding and fixing problems inline versus end-of-line [1] due to the long delay between wafer processing and collection of EOL data. However, EOL results are a critical component in understanding how specific inline defects correlate to product performance and yield, particularly during early process development cycles. Therefore, the ideal yield improvement

methodology relies on inline inspection and metrology for excursion monitoring and process change qualification, while EOL results are used only for the validation of yield improvement changes.

In order for this scenario to be achieved, inline data must be high quality with appropriate sampling, and a clear correlation must be established between inline results and EOL yield. One key tool that is often utilized to achieve this connection is hitback analysis. Hitback analysis is the mapping of EOL electrical failure and PFA locations to inline defect locations identified by inspection tools.

Hitback analysis comes in two basic forms. In the traditional method, EOL yield failures guide PFA, often in the form of a cross-section transmission electron microscope (TEM) confirmation of a physical defect. This physical location is then overlaid against inline defect locations for correlation to inline learning. This analysis often offers clear causality for yield failures, but is slow (dozens/week) and can be blind to defect modes that are difficult to locate or image in TEM.

The second method, which is growing in popularity, is to overlay the EOL electrical failure location directly to inline defect data (**FIGURE 1**). This is largely enabled by modern logic design methods and analysis tools that allow electrical failures to be localized into “chain” locations where the failure is likely to occur. Furthermore, new technologies allow inline inspection to be guided to potential chain location failures based purely on design layout.

DR. CHET LENOX, DR. DAVID W. PRICE and **DR. DOUGLAS SUTHERLAND** are Yield Consultant, Senior Director, and Principal Scientist, respectively, at KLA-Tencor Corp. Dr. Lenox, Dr. Price and Dr. Sutherland have worked directly with many semiconductor IC manufacturers to help them optimize their overall inspection strategy to achieve the lowest total cost. This series of articles attempts to summarize some of the universal lessons they have observed through these engagements.

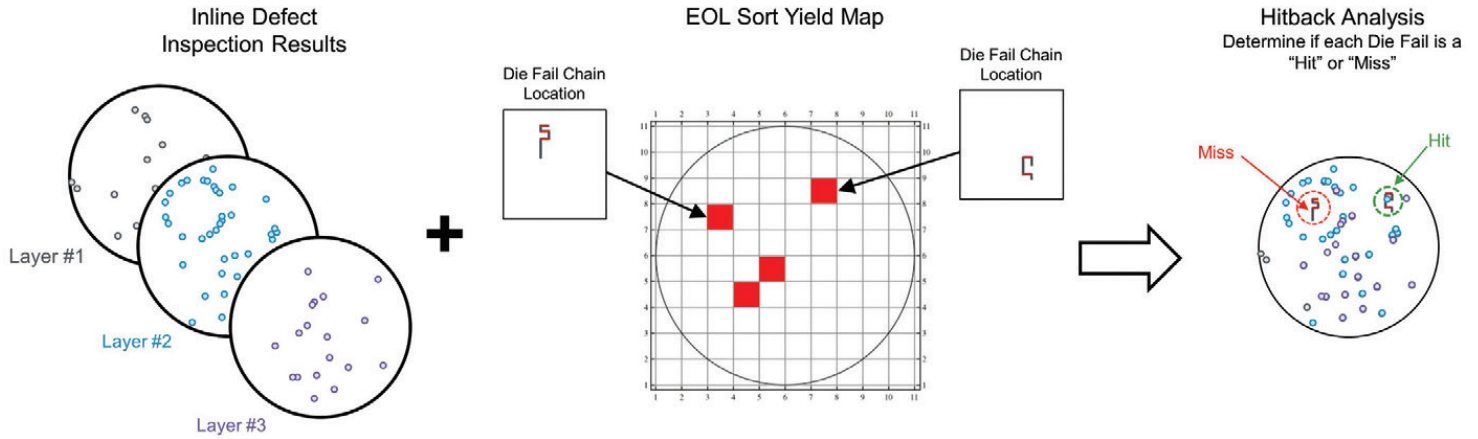


FIGURE 1. Hitback analysis technique where likely die fail chain locations from EOL are overlaid with inline inspection results.

For example, KLA-Tencor’s broadband plasma optical patterned wafer inspection systems incorporate patented technologies (NanoPoint™, pin•point™) that leverage design data to define very tiny inspection areas focused solely on critical patterns. [2-4] Using these design-based technologies to inspect patterns related to potential chain failures produces inspection results consisting of defects that are strongly correlated to end-of-line yield. This more direct technique allows for faster turn-around on analysis, enables higher sampling (hundreds of defects/wafer) and can provide successful causality on defect modes that are difficult to find physically at EOL.

To achieve successful direct hitback analysis from electrical fail chains to inline defect locations, a number of methodologies are helpful:

- Wafers that will be used for hitback analysis should be inspected at all key process steps. This avoids “holes” in potential causality to the EOL failure
- Geometry-based overlay algorithms should be used that combine the point-based inline defect location with area-based reporting of EOL chains

The overlay distance allowed to label a chain-to-defect distance a “hit” must be large enough to allow for inspection tool defect location accuracy (DLA) but small enough that the statistical probability of false-positives is low (**FIGURE 2**)

- All defects found by the inspector should be used for analysis, not just defects that are classified by subsequent review steps
- Electrical fail chain locations should utilize layer information as well as x/y mapping

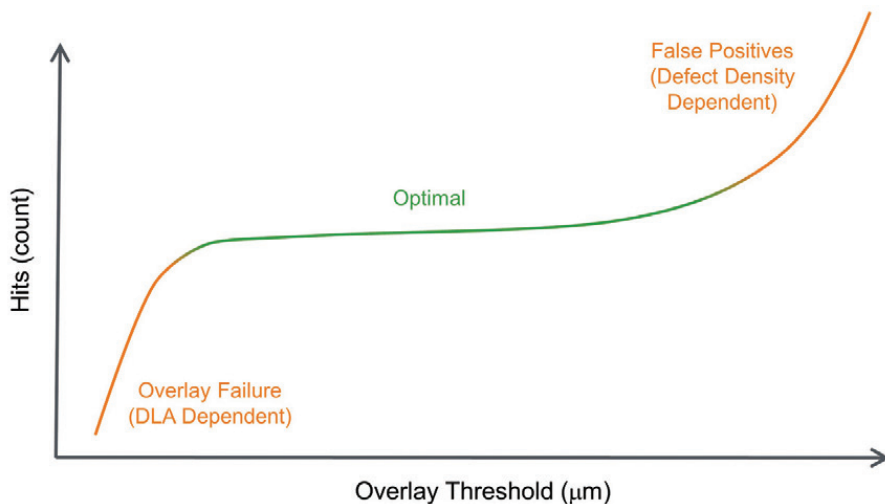


FIGURE 2. The threshold used to overlay EOL electrical chains to inline defects must be optimized to avoid failures or false positives.

When performed properly, the hitback capture rate metric (in percentage) will quantify the number of fails which “hitback” to inline defects. This metric can be used broadly as an indicator of inline inspection capability, with higher numbers indicating that inline inspection can be more confidently used in yield improvement efforts. Therefore, hitback analysis should be performed as early as possible in the development cycle and new product introduction timescale. This allows time for inline defect inspection capture rate improvement through these traditional methods:

- Inspection tool and recipe improvement, including the use of guided inspection based on product layout

- Lot-, wafer- and die-level sampling adjustments
- Process step inspection location optimization

When performed regularly, hitback analysis greatly assists in improving inline inspection confidence and improves yield learning speed. Hitback capture rates increasing to more than 70 percent are not uncommon for effective inline monitoring schemes. It is worth mentioning that the slower EOL PFA Pareto generation and hitback analysis is still required even when direct EOL-to-inline is performed in order to validate the chain fails and hitback capture rate.

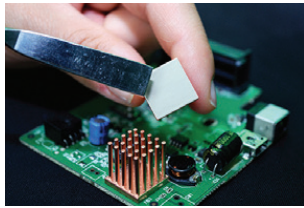
Yield ramp rate is often the primary factor in the profitability of a fab's new process and new product introduction. This ramp rate is strongly influenced by the effectiveness of inline wafer inspection, allowing faster information turns and quicker decision making by process engineers. Hitback analysis is a key method for gauging the effectiveness of inline inspection and for driving inspection improvements, particularly when correlating EOL electrical chain failures to inline defect results.

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Author's Note: The Process Watch series explores key concepts about process control—defect inspection and metrology—for the semiconductor industry. Following the previous installments, which examined the 10 fundamental truths of process control, this new series of articles highlights additional trends in process control, including successful implementation strategies and the benefits for IC manufacturing. For this article, we are pleased to include insights from our guest author and colleague at KLA-Tencor, Chet Lenox. ◀

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Mergers & Acquisitions in 2017

At SEMI's Industry Strategy Symposium this year (<http://www.semi.org/en/iss>), a mergers & acquisitions panel, moderated by Robert Maire of Semiconductor Advisors, took a look at how the industry might look in the future. The panel consisted of:

- Patrick Ho, senior research analyst, Semiconductor Capital Equipment at Stifel Nicolaus
- John Ippolito, VP Corporate Development at MKS Instruments
- Israel Niv, former CEO of DCG Systems
- Tom St. Dennis, chairman of the Board of FormFactor.

Will the huge deals of 2015 and 2016 continue?

Setting up the panel, Maire observed that 2015 and 2016 were huge in transaction size (over \$100 billion announced in 2015), but while the values of the deals have jumped, the number of deals has remained fairly consistent over the past several years. Also, China has more significantly moved into the M&A market in 2015, in the range \$4 to \$5 billion.

It appears that M&A will continue, but not at the same pace as 2015 and 2016 due to increasing political, regulatory, and industry pushback. In the equipment space, while big deals such as Advantest and Verigy were possible in 2011, the current climate has seen big deals falter including Applied Materials and Tokyo Electron; Lam Research and KLA-Tencor; and Aixtron and Fujian Grand Chip.

However, Maire observed that the motivations for M&A continue; for instance, Intel needs to offset a declining PC market and ramp IoT, VR, and Cloud activity and will likely consider M&A as part of its approach. Similarly, opportunities for equipment companies to increase scale and size exist for process control companies and in the back-end segment where further consolidation appears necessary.

China becomes a player

China's ambitions in M&A may have been complicated by recent events, but with a \$150 billion investment fund there are likely more opportunities ahead. China has stated the intent to move from producing just 10 percent of its IC



By SEMI Staff

consumption to 70 percent in ten years and catching up technologically by 2030. While some see concerns given China's investment and later pricing collapses in FPD, PV, and LED, others see China's efforts to increase its indigenous production of ICs as similar to what has happened as the industry spread from U.S. and Europe to Japan, Taiwan, and Korea.

The panel responded to questions from Maire, questions submitted from the audience, and live audience questions. Ho noted that big deals in semiconductor equipment appear, for the time being, to be difficult or over. However, there is still low-hanging fruit and smaller deals. There is a need to focus on scale and size because customers (IC manufacturers) are bigger and fewer. For example, Form Factor's combination with Cascade brought size and scale and enabled Form Factor to be more competitive.

The future for semiconductor equipment consolidation

Several questions revolved around where M&A would happen in the semiconductor equipment space. There was general consensus that M&A of any of the "big five" (not named, but likely ASML, Applied Materials, Lam Research, Tokyo Electron, and KLA-Tencor) were off the table in the short term due to both regulatory pressure and industry pushback given fears of overly strong supplier power. Niv thought there were opportunities for consolidation in the metrology and process control space. Ippolito thought there might be further consolidation opportunities in motion control. St. Dennis thought there were opportunities throughout the whole supply chain. He pointed out that the benefits of acquiring a good company were significant, including great talent (difficult and time consuming to develop organically), synergies in not just SG&A, but in technology and field organizations.

The role of private equity was raised. Ippolito noted that the private market and private equity have roles to play in consolidation opportunities, noting the success of Atlas Copco with Edwards Vacuum and Oerlikon Leybold as an example.

Several questions focused on China. Niv pointed out the industry needs to think about China similar to how they thought about Japan when Japan was emerging as an IC manufacturing power. Partnering with Japanese companies was an effective strategy for many and brought long-term success in that market. Ippolito thought that very large China deals might be off the table for a while, but smaller deals would likely go through. He noted that \$150 billion (the China investment fund) is a lot of money and that tends to find a way forward. ◀

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