

Solid State TECHNOLOGY[®]

Insights for Electronics Manufacturing

Impact of NVDs
on Yield P. 18

Bonding Wire
Advances P. 22

MEMS
Manufacturing P. 26

ALD for
Metal Gates P. 14

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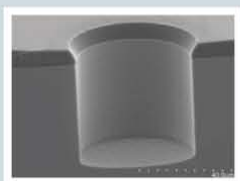
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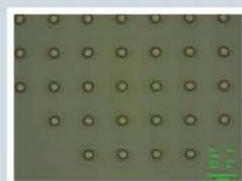
TSV CLEAN AND RESIST STRIP



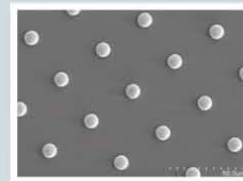
After DRIE



After SSEC Cleaning



Optical



SEM

Si ETCH TO REVEAL Cu VIAS

WET ETCH WAFER THINNING AND STRESS RELIEF



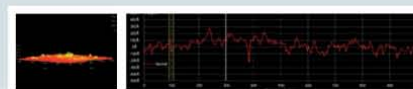
Wafer Thinning



≤ 2% Uniformity of Etch
with TTV Unchanged

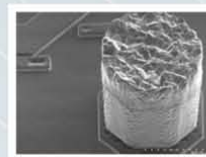


Before Etch (Surface Roughness)



After Etch (Surface Roughness)

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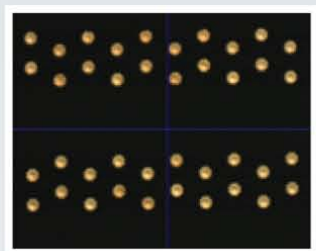


Before Etch

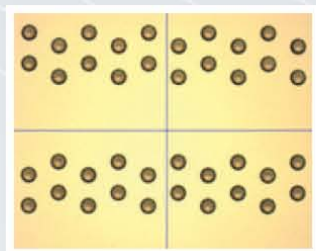


After Etch

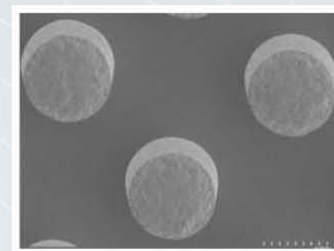
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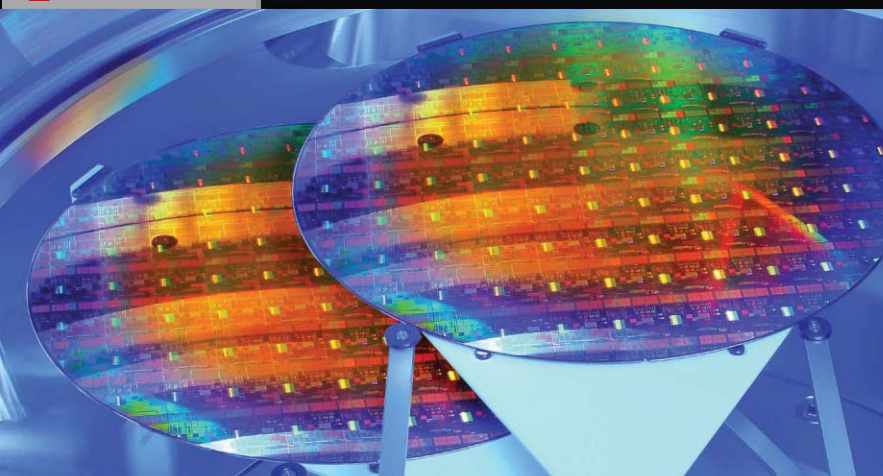


Pre-strip



Post Dry Film Strip





Solid State TECHNOLOGY®

JULY 2012 VOL. 55 | NO. 6

Metal ALD has become an enabling technology for gate stack integration. Source: ASM America.

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ALD | Atomic layer deposition for metal gate integration

High-k based transistors have introduced the semiconductor industry to increasingly complex metal gate integration schemes and novel, low temperature deposition techniques such as ALD. *Mohith Verghese, ASM America, Phoenix, AZ.*

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METROLOGY | Impact of charge during gate oxide patterning on yield

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This case study describes Microchip's experience with perfluoroelastomers o-ring seals. *Dalia Vernikovsky, Applied Seals North America Inc., Newark, CA, and Brad Ecker and Seth Urbach, Microchip Technology, Inc., Chandler, AZ.*

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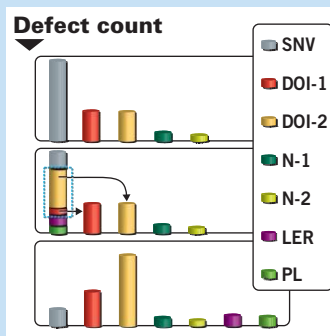
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Web Exclusives

Process Watch:

The dangerous disappearing defect

In this first installment of a series called "Process Watch," experts from KLA-Tencor explain why a defect might be classified as "Not Found" or "SEM Non-visual (SNV)," and how a SNV count can disguise or hide real problems. <http://bit.ly/L6rNZs>



You make MEMS. Should you make sensor fusion software?

Solid State Technology's Meredith Courtemanche looks at the options for sensor fusion software, made by MEMS manufacturers and third-party, device-agnostic providers. <http://bit.ly/LmZ2Ez>

@ The ConFab:

Chip industry future

"The Economic Outlook for the Semiconductor Industry," with Jackie Sturm of Intel, Dan Hutcheson of VLSIresearch, and Jim Feldhan of Semico discussed how to succeed in the new chip industry. <http://bit.ly/LjsFF2>



@ The ConFab:

Legacy fab issues

Older fabs face tool & skills obsolescence; scarce availability of parts, software, and support; etc. The Executive Roundtable shared concerns, roadblocks, and possible solutions, say Bill Ross of ISMI and Joanne Itow of Semico. <http://bit.ly/KGIK84>

@ The ConFab:

Video interviews

G450 Consortium's Tom Jefferson <http://bit.ly/MSw8iZ>

ACT International's Bill Tobey <http://bit.ly/LDz1kM>

Renesas' Ali Sebt <http://bit.ly/NBocUN>



Mobile displays @ ITF

What would our smart world be without displays? That was the question posed by imec's Paul Heremans, at ITF.

<http://bit.ly/K3DewF>

MEMS Symposium: Chasing \$1 trillion

Michael A. Fury reports on the MEMS Technology Symposium, with the theme "Sensors: A Foundation for Accelerated MEMS Market Growth to \$1T."

<http://bit.ly/K3DPP2>

LEDs outshine legacy lighting @ LightFair

"LED is now the dominant force in lighting," reports Ted Konnerth. What does that mean for traditional lighting, apps, distribution, and talent?

<http://bit.ly/NzCViX>

MEMS isn't NEW

Karen Lightman, MEMS Industry Group, lets us in on the real meaning of MEMS new product development.

<http://bit.ly/JVqEiv>

ECTC: 3D and TSVs

Electronic Components and Technology Conference (ECTC) focused on 3D integration and TSVs, says Pete Singer.

<http://bit.ly/L3pfb8>



editorial

Price, Power and Performance

At The ConFab 2012, which took place in June at The Encore at The Wynn in Las Vegas, Mike Noonan of GLOBALFOUNDRIES kicked off the Fabless-Foundry Supply Chain session, noting that the manufacturing cycle time is now sometimes longer than the product lifetime.

Noonan noted that the semiconductor industry has always had the cyclic reality of the semiconductor cycle to deal with. This challenge has been compounded by several factors in recent years that fabless and fab-lite companies must contend with. These are:

- Financial markets demanding higher returns and hence more operational efficiency
- Fewer options for leading edge manufacturing

In parts of the world, people's first experience with the internet will be on a smart phone

Product lifecycles that much shorter than design and even production times in some markets

- Disaggregated worldwide supply chain that can be disrupted by natural disasters

In the same session, Nick Yu of Qualcomm described the "internet of things" as the biggest platform in the history of mankind. "It's going to explode," he said. "The world is moving to a higher level of abstraction," he added, pointing to the amount of social networking in the world. "All of these applications are in their infancy," he said, noting that in many parts of the world, people's first experience with the internet will be on a smart phone. "PCs and laptops are probably a thing of the past," he said. "The smartphone is the remote control for your life." He also said your first 3D camera is going to be in your phone.

All presenters emphasized three requirements moving forward: power, performance and price. "Power and cost are now a higher priority than performance," he said. "Chip cost reduction may not happen at advanced technology nodes," Yu warned.

BJ Woo of TSMC highlighted the many challenges faced by foundries, and the responsibilities they face. "Just delivering an accurate SPICE model is very challenging," she said. Fortunately, new technologies can actually reduce variability. "When you move to high-k metal gate, the variability is reduced," she said. "When you move to FinFET, it's even further reduced."

—Pete Singer, Editor-in-Chief

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CHINA | LED maker **Cree Inc.** is opening new technology centers in Shenzhen and Shanghai, China <http://bit.ly/KETu73>

WORLD | **Universal Display Corporation's** white OLED lighting technology breaks performance records <http://bit.ly/LKW914>

USA | Inertial sensor maker **Qualtré Inc.** closed a \$10 million round of financing with 3 investors from Massachusetts, where Qualtré is based <http://bit.ly/L9uCKv>

EUROPE | **EpiGaN NV** opened its GaN epitaxial material production site, on the Research Campus Hasselt in Belgium <http://bit.ly/LmW17d>

KOREA | **Amkor Technology** will build a state-of-the-art factory and global research and development center in the Incheon Free Economic Zone, Seoul <http://bit.ly/L0uVp0>

CHINA | **ASE** opened its Phase 3 manufacturing facility in Weihai, boosting discrete packaging and test capacity <http://bit.ly/JLiFLp>

EUROPE | **ON Semiconductor** expanded its Roznov, Czech Republic, operations with a 4,000sq.m. research and design facility <http://bit.ly/LrgOoO>

WORLD | Chinese suppliers of large-size LCD panels are the fastest growing segment of the industry, although major South Korean brands continue to dominate <http://bit.ly/KD6RXd>

USA | **Freescale Semiconductor** named Gregg A. Lowe president and CEO, replacing Rich Bayer. Lowe joins Freescale from Texas Instruments <http://bit.ly/Nn384h>

Semiconductor fabs use significantly less energy today, but work remains

Semiconductor manufacturing facilities dramatically decreased their normalized fab energy consumption from 1997 to 2011, shows The International SEMATECH Manufacturing Initiative (ISMI) Worldwide Fab Energy Study. Sanjay Rajguru, director of ISMI called energy-efficiency and conservation "critical" for semiconductor manufacturers.

Compiling data from 300mm and 200mm semiconductor fabs in Asia, North America, and Europe, the study's benchmark data helps identify areas to reduce energy use and improve efficiency in semiconductor manufacturing operations.

Process equipment consumes more than 50% of energy in a fab, found ISMI's Environment, Safety and Health (ESH) Center researchers. Energy consumption here halved in the study time period. Non-process-equipment energy consumption has dropped to one-fourth of 1997 values. The next

highest energy users were central chiller plants and bulk gas production. Waste heat recovery and reuse practices were benchmarked for best-in-class performance.

To explore bulk-gas production energy efficiency, ISMI initiated a workshop in collaboration with experts at member companies. The participants benchmarked best-in-class metrics and reviewed best-in-class design practices for nitrogen plants, specifically focusing on air compressors, which consume up to 85% of the bulk gas energy budget.

Based on the energy survey results, ISMI will focus on efficiency at the nitrogen system, controlled dry air (CDA) system, process cooling water system, and process vacuum system. ISMI is also working to reduce water and chemical usage.

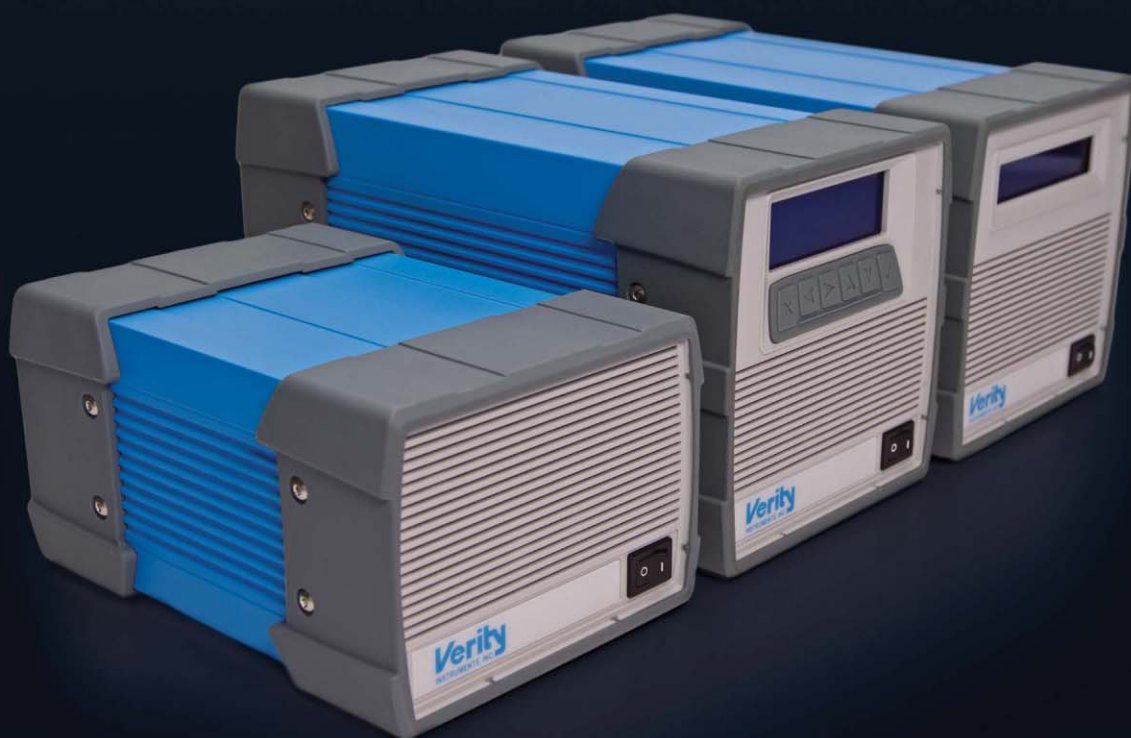
SEMATECH is an international consortium of leading semiconductor device, equipment, and materials manufacturers. —M.C

Guangzhou exemplifies China's LED industry

Guangzhou (China) Lightfair Conference is the biggest lighting fair in Asia, with companies throughout the LED lighting supply chain, including new Chinese MOCVD makers, International Solid State Lighting Alliance and China SSL Alliance. Citi alternative/renewable energy analyst Timothy Arcuri notes trends at the show in LED manufacturing and pricing ahead of China's subsidy program going into effect.

Continued on page 9

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newscont.

Biggest auto MEMS maker, biggest growth in 2011

Bosch GmbH Automotive Electronics of Germany retained its position as the world's top supplier of automotive MEMS in 2011, according to IHS.

Overall, 2011 revenue for automotive MEMS sensors amounted to \$2.24 billion, up 14% despite a disrupted supply chain in the aftermath of natural disasters last year in Japan and Thailand. Expansion in the next two years will be driven by government mandates in the US and Europe for electronic stability control (ESC) and tire-pressure monitoring systems (TPMS).

The automotive MEMS Top 10 enjoyed combined revenues in 2011 of more than \$2.0 billion, up 11%. The top 10 comprised 91% of the market.

Booking \$625 million in revenue last year, Bosch's 19% expansion outpaced the growth of the automotive MEMS industry as a whole. It was also \$339 million ahead of the #2 supplier, Denso Corp., which grew 9% to post revenue of \$286 million in 2011.

"Bosch's success last year can be credited to its internal captive market, which promoted stable revenue and visibility into future demand for the company," said Richard Dixon, principal analyst for MEMS & sensors at IHS. "Bosch is the No. 1 supplier overall in MEMS sensor shipments for ESC systems in vehicles; as well as supplying the highest combined total of related automotive MEMS sensors such as accelerometers,

gyroscopes and pressure sensors. Bosch's performance was also boosted by a rapidly growing airbag market in China, along with a surge in demand for frontal and

an overly strong yen against the US dollar hindered exports.

Moving up a spot to #3 in 2011 was Panasonic, with revenue of \$202 million, up 12%. Most of Panasonic's

TABLE. Top 10 automotive MEMS manufacturer by revenues (\$M).

Rank	Company	2011 revenue	2010 revenue	Y/Y growth
1	Bosch	\$625	\$524	19%
2	Denso	\$286	\$263	9%
3	Panasonic	\$202	\$181	12%
4	Freescale	\$191	\$190	1%
5	Sensata	\$190	\$153	24%
6	Analog Devices	\$161	\$136	18%
7	Infineon	\$139	\$117	19%
8	VTI	\$103	\$76	36%
Tie: 9 & 10	GE Sensing	\$64	\$57	12%
	Delphi	\$64	\$62	3%
Total Top 10		\$2,025	\$1,759	11%

SOURCE: IHS iSuppli Research, June 2012.

side airbags in the United States."

Denso is the major supplier in its domestic Japanese market, with a diverse customer base that includes almost half of Toyota's auto MEMS business. Denso reported heavy declines in sales in Q2 2011 after Japan's 3/11 earthquake-tsunami disaster, but recouped its losses during the next quarter. Denso is a top supplier of MEMS sensors of automotive heating/ventilation/air conditioning (HVAC) systems, as well as satellite airbag accelerometers and oil-pressure sensors. The company's growth during the last two years has been relatively subdued compared to the rest of the auto MEMS market, because

sales came from its automotive gyroscope business, reflecting a narrower focus compared to that of the leading two companies. However, Panasonic is the undisputed leader in in-dash navigation gyroscopes and ranks a very close second to Bosch in gyroscopes needed for ESC systems. The two devices are the highest-priced components in the automotive MEMS space. Panasonic is no longer the sole supplier of yaw rate sensors to European Tier-1 Continental, and in the future will see increased competition from VTI on combo-packaged inertial sensors for ESC systems.

Freescale Semiconductor dropped down one place to

#4 with automotive MEMS revenue of \$191 million, in a near tie with #5 Sensata. Freescale is the leading supplier of satellite airbag accelerometers, even though it temporarily lost share in that market with earthquake damage at its Sendai, Japan facility. Sensata concentrates MEMS production on pressure sensors, and is #1 in high-pressure applications like brake and common fuel rail sensing, using its silicon piezoresistive sensors that are glass-bonded to steel substrates. Sensata also had the second-highest yearly growth rate of 24%.

Among the remaining Top 10, growth ranged from 3% at Delphi to 36% for VTI, thanks to VTI's strong position in ESC accelerometers. Infineon and Analog Devices Inc. joined Bosch, Sensata and VTI in recording growth rates higher than the industry average, while GE Sensing had slightly below-average expansion of 12%.

Fuji Electric fell just outside the top 10, with overall revenue of \$30 million.

Learn more about this topic with the IHS iSuppli report entitled: "Fat Years Ahead for Automotive MEMS Sensors."—**M.C**

Continued from page 9

The NDRC's demand rebate program is more positive than Citi originally estimated, because the rather meager RMB2.2B (~\$350MM) would get more funds if this iteration of the subsidy catalog's funds are depleted, expected to take only ~12-24months. Producers are even more excited by provincial-level subsidies, Arcuri says. In Guangdong, the province in which the conference took place, these will boost revenue for local LED producers to RMB5B (~\$850-900MM) by 2015.

Major buyers like Kingsun are finally coming to shop at the local LED makers, sourcing up to 60% of their LEDs domestically by 2013. Companies that months before were making Christmas lights are now making bulbs; bulbmakers are vertically integrating rapidly into fixtures. Lumens/W at these companies have increased dramatically even from last fall.

Citi heard of many examples of Chinese LED makers selling well below cost to gain an edge, and this could intensify as the government subsidies roll out.

Citi estimates that ~60% of all reactors shipped to China are turned on, with ~60% utilization on these tools, implying overall utilization of ~35-40%. The "gray market" for MOCVD tools is gaining steam, but province-specific. Citi's observed talk of stronger vendors within a given province buying new, unused, or virtually unused tools from weaker vendors (in most cases recertified by the tool vendor). As long as the equipment does not leave the province, local government is happy, sometimes even "playing matchmaker" behind the scenes to force consolidation.—**M.C**

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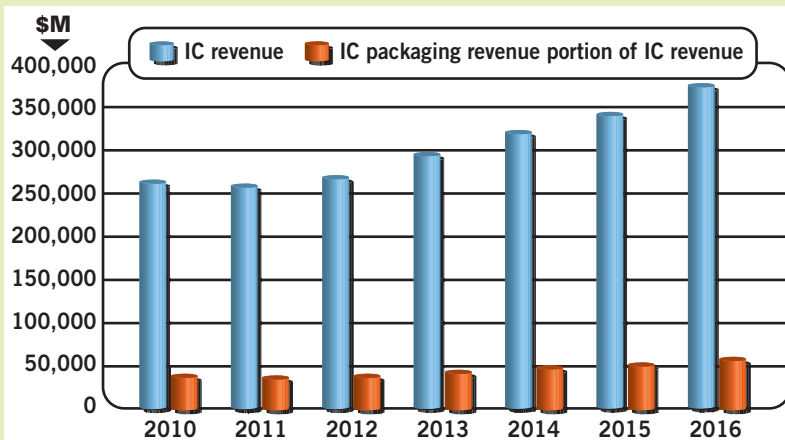
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newscont.

Packaging revenue outgrows package unit growth

Growth in smartphones and tablets and resurgent automotive demand are increasing IC demand. In turn, increased demand for product functionality is driving up IC packaging revenue faster — a 9.8% CAGR — than IC unit growth — 7.3% CAGR 2010-2016, says New Venture Research (NVR).

Handheld electronics will boost the growth of special purpose logic (SPL) communications chips by 16.7% CAGR revenue through 2016, versus 3.5% CAGR in



IC device and packaging revenue forecast (\$M), 2010-2016.
SOURCE: New Venture Research.

units. Packages for mobile components are dominated by FPGA and QFN designs, which are at opposite ends of the pricing structure. The third most popular packaging type, QFP, is decreasing in usage over time.

Wireless infrastructure products are also in high demand, which is helping boost consumption for standard cell and programmable logic device (PLD) chips. These devices will grow at a CAGR of 16.1% in terms of revenue through 2016, while the device units are projected at 15%. High-I/O BGAs are the package of choice over the forecast period — package revenue growth is projected to be slightly higher, at 16.3% CAGR through 2016.

Logic chips are in demand for a host of products, pushing 32-bit MCUs to an 11.1% CAGR unit demand, although only 4.7% device revenue CAGR, through 2016. QFPs and BGAs are the highest-demand package designs, although the QFP is waning. Thus, the package revenue is growing at a CAGR of 12.8% through 2016 for 32-bit MCUs.

This information is included in the newly released report "The Worldwide IC Packaging Market, 2012 Edition", from New Venture Research (NVR), a technology market research firm. — M.C

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From The ConFab:

State of advanced packaging technologies

As packaging has played a larger and larger role in chip performance, form factor, and capabilities, Solid State Technology's The ConFab has increased its focus on back-end processes. Cue "Advanced Packaging and Progress in 3D Integration," a session chaired by Abe Yee, Nvidia, and featuring David McCann, senior director of technical business operations, GLOBALFOUNDRIES; Sandeep Bharathi, VP of engineering, Xilinx; Ron Huemoeller, SVP of advanced interconnect platform development, Amkor, and William Chen, VP, Advanced Semiconductor Engineering Incorporated (ASE).

2.5D and 3D packaging are coming together to enable the end-goal of silicon devices — high density, low power, low cost, high yield, small form factor heterogeneous silicon blocks integrated on one package, feeding a seemingly insatiable demand for video, Internet, etc. Society is shifting to "ambient intelligence," Chen said. McCann pointed out the interconnection density increase enabled by advanced packaging, whether it be 2D like flip chip bumps (10k I/Os per IC) or 3D like TSV (50k I/Os). Stacking silicon interconnects enables lower latency and power consumption in higher density than traditional I/Os, said Bharathi, creating 100X the die-to-die connectivity bandwidth per watt versus high-speed serial or standard parallel I/O.

Bharathi explained Crossover SoCs — devices that combine multiple functions on a single device with heterogeneous die. With active die

stacked atop active die in a 3DIC, Crossover SoCs raise thermal and mechanical challenges. Bharathi looked at a case study of stacked silicon interconnects in FPGAs at Xilinx, FPGA building block "tiles" organized in columns then combined to create an FPGA. The device combines a 28nm active die and 65nm passive interposer, with low-risk micro-bumps and TSVs; the silicon interposer reduces stress with low-*k* materials.

Huemoeller zeroed in on TSVs, which can take monolithic die to die slices, or be used to segment monolithic analog/logic/cache functions onto separate die. Stacking die frees up process node choices. Wafer yield goes up, and costs go down, with no form factor sacrifice. Quoting Samsung, Huemoeller said that TSVs interconnecting stacked die offer 8X better bandwidth and 50% power savings compared to PoP.

Advanced packages call for new materials and assembly and test methods. McCann pointed out that transistors and packaging are not 2 isolated silos. Copper-filled TSV interconnects add stress to the silicon. Thinning on transistors also must be characterized for potential impacts. The wafer processing steps are complicated for advanced packaging, and KGD testing is still developing, Bharathi added.

Expect >80% CAGR for 2.5D interposers through 2015 (300mm equivalent). 2.5D interposers can be made from laminate, glass, or silicon, each with pros and cons. Laminates are limited to larger line/space pitch than package designs will require. Glass vias can be very expensive. Silicon interposer production is one option for idle legacy foundry lines, said Huemoeller.

Chen points out that, over time, various advanced packaging methods, such as WLP, die stacking, and interposer interconnects, are converging. Parallel trends are emerging that use silicon interposers and 3D packaging with heterogeneous integration. Heterogeneous integration puts MEMS devices, memory, logic processors, and RF devices all on one substrate, in a small form factor.

Read a discussion of the packaging supply chain with these ConFab speakers at <http://bit.ly/KnQBsQ>. ♦



Meredith Courtemanche,
digital media editor

Packaging



The demise of sapphire wafers?

“Are we witnessing the demise of sapphire wafers?” I was asked recently. “Not yet!” was my reply.

Today GaN epitaxial films grown on sapphire wafers provide the best solution for manufacturing LEDs. These chips are used as back lights in all mobile phones, all tablet computers, in most LCD-TVs, and will soon be used in many solid state lighting applications. Yields are improving, costs are dropping rapidly. Many new suppliers have entered the market. The use of LEDs for LCD-TV backlighting has provided a significant jump in unit volume – an important driver of scale and cost savings. Still people are looking for alternatives. Why?

LED makers want to move to larger wafers so they can lower unit costs. Most LED production is done on sapphire wafers 100mm in diameter and smaller. Semiconductor grade silicon wafers are readily available at 200mm and 300mm. If LED grade GaN epitaxial films can be grown on large silicon wafers, there could be a clear path to lower unit costs.

GaN epitaxial films grown on sapphire or silicon have many crystal defects. These defects cause yield loss and decrease the efficiency of converting electric current to light. The ideal material would be single crystal GaN. If large GaN boules can be grown, very efficient LEDs might be built with very few chips lost to crystal defects.

LEDs

But life is not so simple. LED material systems are very complex. We

are operating at the edge of knowledge. It's hard to move fast. Progress is measured in decades, not years. For example, the spacing of atoms in GaN is a poor match to the atom spacing in silicon. Novel buffer layers have been developed to mitigate these problems. Recent results show efficient LEDs can be built. But buffer layers add cost and production is still “2 years” away. In the meantime sapphire suppliers are supplying 150mm and 200mm wafers. It's no longer obvious that silicon wafers are a “must have” technology for LEDs.

Sumitomo and Soitec have joined forces to fabricate high quality GaN engineered substrates. Sumitomo will grow the large boules of GaN. Soitec will use their ion-implant technology to slice off thin GaN films, and then attach these to carrier substrates. The Soitec “slicing” method will conserve expensive GaN material. Still, cost, conversion efficiency and yield remain as serious unknowns.

This competition reminds me of the early days of IC technology. There was a two decade long debate about which technology was best for IC production. Silicon won, not because it was the ideal semiconductor material, but because it moved to high volume and low cost first and kept moving as more suppliers entered the market using silicon wafers. The parallel today in LED manufacturing is sapphire wafers. Sapphire may not be the ideal material, but it is rapidly moving ahead of the competition.

At SEMICON West this year, many of the teams working on these alternative material systems will be presenting their progress. There can always be a breakthrough result. Better check it out. ◀



Griff Resor,
Resor Associates,
Maynard, MA USA



Bridgelux Inc. has achieved
135 Lumens per Watt
GaN-on-silicon based LED
technology



ALD

Atomic layer deposition for metal gate integration

MOHITH VERGHESE, ASM America, Phoenix, AZ.

High-k based transistors have introduced the semiconductor industry to increasingly complex metal gate integration schemes and novel, low temperature deposition techniques such as ALD.

As high-k/metal gate (HKMG) technology becomes mainstream for high performance and low standby power logic devices, it is useful to review the rapid evolution of integration schemes that has made this new process architecture possible. The introduction of high-k as the gate dielectric of the transistor was one of the most significant of recent process integration changes in the semiconductor industry. Replacement of traditional silicon oxide (SiO_2) and silicon oxy-nitride (SiON) dielectric layers was difficult in itself, but it was quickly discovered that metal gate integration was the single most challenging aspect of proliferating HKMG technology in production. Whereas past technology nodes utilized highly doped polysilicon gate electrodes for NMOS and PMOS devices, the use of high-k gate dielectrics necessitated a shift to metal gate electrodes. High-k materials like hafnium oxide (HfO_2) were found to interact negatively with polysilicon, causing a variety of issues such as high threshold voltages (V_T) and increased equivalent oxide thickness (EOT)[1]. Metal gates, on the other hand, integrate well with the new metal oxide dielectrics, but can also come with a host of issues. Integration concerns such as film stability, compatibility with existing production flows, and contami-

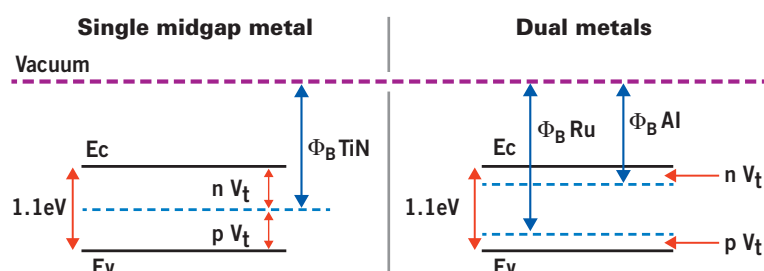


FIGURE 1. Work Function Requirements for CMOS Devices

nation in manufacturing fabs have to be taken into account. However, the single most important factor in choosing the appropriate metal gate is effective work function control. The effective work function of the metal gate dictates the ultimate threshold voltage of the device which in turn allows lower power operation and higher clock speeds.

Transistor work functions

NMOS and PMOS transistors have different effective work function requirements to align appropriately with the respective Fermi levels in the underlying silicon (**Fig. 1**). To enable low V_T operation, band edge effective work functions are highly desirable (<4.1 eV for NMOS, >4.9 eV for PMOS) [2]. Metals have inherent theoretical work functions associated with them and it is possible to identify metal films which exhibit the required nominal

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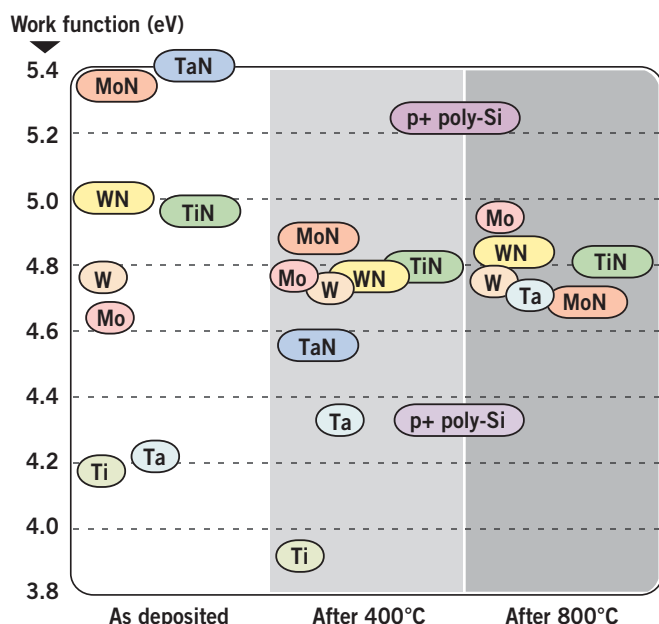


FIGURE 2. Effect of Thermal Budget on Metal Work Function

values. However, effective work function is highly dependent on the interaction at the metal-dielectric interface and hence it is sensitive to metal thickness, deposition techniques, film composition/contamination and thermal budget. In fact, the same metal can exhibit a wide range of effective work functions after complete device integration. One verity is the drift of the effective work function of most metals towards mid-gap (~ 4.5 eV) upon exposure to thermal anneals (**Fig. 2**) [3]. Furthermore, only a few metals exhibit the required thermal stability to survive the lengthy device manufacturing flow. The industry quickly converged on titanium nitride (TiN) as the most effective metal gate for HfO_2 based gate dielectrics. Novel low temperature deposition techniques like atomic layer deposition (ALD) are able to isolate a largely p-type version of TiN. However, thermal budget is still a concern and in traditional, gate first process flows, the TiN effective work function is driven to mid-gap after the high temperature, dopant activation anneals [4]. Some integrated device manufacturers (IDMs) have used innovative approaches to continue the use of gate first process flows along with a single mid-gap TiN based metal layer by the use of capping dielectric layers to modify the final effective work function of the device and maintain low V_T operation [5].

Replacement gate processes

In recent years, some IDMs have transitioned to replacement gate (RPG) process flows where the formation of the high-k/metal gate stacks are performed after completion of all high temperature process steps such as dopant activation anneals. This enables a work-around the work function drift problems present in gate first integration and exploits the metals gate's native work function in the transistor [6]. While the result is a more complex integration scheme, the RPG flow gives unparalleled control of metal effective work functions. However, RPG flows also introduce more three dimensional challenges for deposition techniques. Removal of the dummy poly gate after spacer formation results in an opening that must be filled conformally with high-k and metal gate films with precise thickness control (**Fig. 3**). Because of its inherent conformality, ALD is a must for some of the critical steps of the formation of the metal gate stack for optimal control within the die and across the

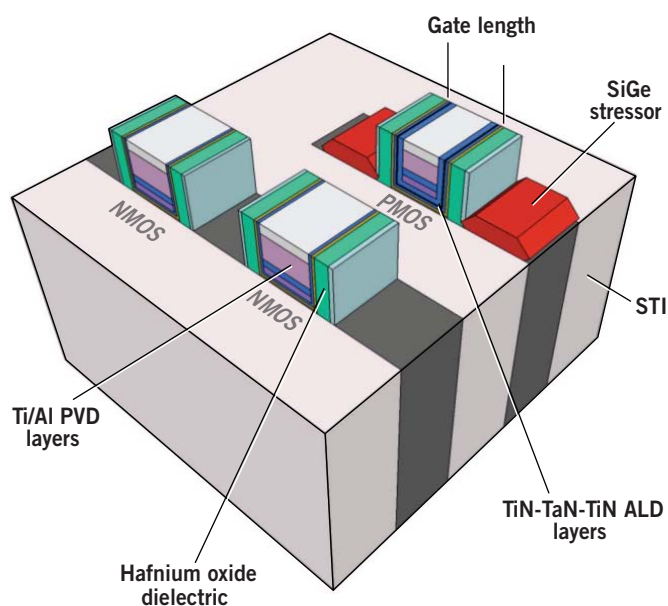


FIGURE 3. Planar Replacement Gate Device Structure

entire wafer. NMOS work function has been the most elusive as most pure metals with low work functions (e.g. Al, Ti, Ta) are both unstable on high-k (resulting in metal migration and high leakage currents)[7] and difficult to deposit conformally at a low temperature by thermal ALD [8]. Hence, early versions of RPG technology used combinations of ALD, physical vapor

deposition (PVD) and chemical vapor deposition (CVD) for metal gate formation.

As shown in **Fig. 3**, the novel RPG NMOS metal stack that has become standard in the industry uses a thin TiN layer and Ti/Al mixtures to set the correct effective work function [9]. Although the thin TiN layer alone is not enough to set the appropriate band edge work function, controlled diffusion of Al from the layer above allows for a work function shift towards the conduction band without degrading gate leakage significantly [10]. The PMOS transistor utilizes a thin TaN barrier along with a thicker TiN layer above it to prevent movement of Al close to the metal/high-k interface. This TiN-TaN-TiN stack is also responsible for setting a high, p-type effective work function for the PMOS transistor [11]. The final step is an Al contact fill for both NMOS and PMOS transistors. The difficulty in effectively controlling this complex RPG flow for planar devices is compounded as gate length scales. Tighter gate pitches result in higher aspect ratios and reduced real estate for the multiple metal layers required. Conformal fills of the required pure metals are also extremely challenging and variations in thickness of the thin TiN and TaN layers results in difficulty in controlling the V_T across multiple dies on the wafer and across different transistor channel lengths. Device reliability also becomes significantly challenging in highly scaled RPG devices.

Scaling the planar transistor to gate lengths below 22nm has required high doping of the channel and source/drain regions to control short channel effects. As a result, random doping fluctuation is now a leading V_T variability issue [12]. A fully depleted device allows for a lighter channel doping or the complete elimination of doping in order to obtain better V_T variability control. As a result, a transition to three dimensional, FinFET type devices is underway for the most advanced logic nodes. Furthermore, FinFETs can relax EOT/L_{gate} scaling requirements as drive current enhancements can be achieved through better electrostatic control [13]. FinFETs also relax effective

work function requirements for metal gates (typically by approximately 100-200 mV) due to the undoped nature of the fully depleted fins [14]. However, a work function span is still required and RPG process flows remain the best path to achieve appropriate NMOS and PMOS targets.

The three dimensional channel region poses a larger issue for NMOS devices. While ALD TiN alone can achieve PMOS metal gate targets, PVD layers are no longer an option for setting NMOS work function. A

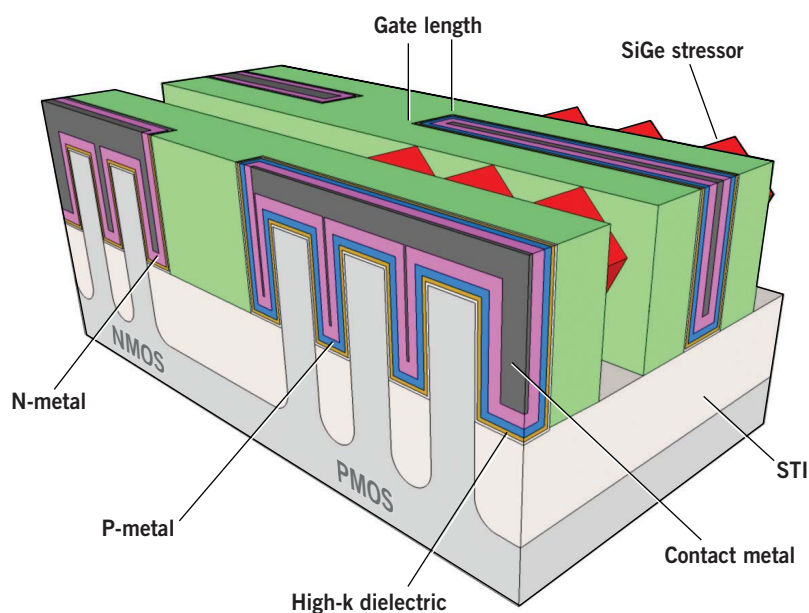


FIGURE 4. FinFET Replacement Gate Device Structure

non-conformal Ti/Al layer would result in variations in V_T both around the fin and between transistors. PVD films can neither conformally cover the fin nor is there enough space to pursue the complex multi-layer solution that was implemented for RPG planar devices (**Fig. 4**). As a result a low temperature, ALD, n-type work function material is a requisite for successful NMOS FinFET devices. This requirement has to be coupled with the previously discussed prerequisites of thermal stability and metal migration control. Ideally, the metal gate would be able to set the appropriate work function at the thinnest possible physical thickness to allow for denser packing of the fins and the transistors and for better scalability to future nodes. Furthermore, the work function metal should

be compatible with the contact metal material so that valuable real estate between transistors is not used up by electrically inadequate barrier layers.

Conclusion

High-k based transistors have introduced the semiconductor industry to increasingly complex metal gate integration schemes and novel, low temperature deposition techniques such as ALD. Although these techniques are already immensely leveraged for RPG planar devices, the additional requirements for three dimensional FinFET device structures will further propel ALD into new spaces. The industry will inevitably see less of a reliance on traditional CVD and PVD metal films and an intense focus on ALD equivalents or replacements. Metal ALD has clearly become an enabling technology for gate stack integration in front end of line (FEOL) with expansion possibilities into middle end of the line (MEOL) and back end of the line (BEOL) applications. ◀

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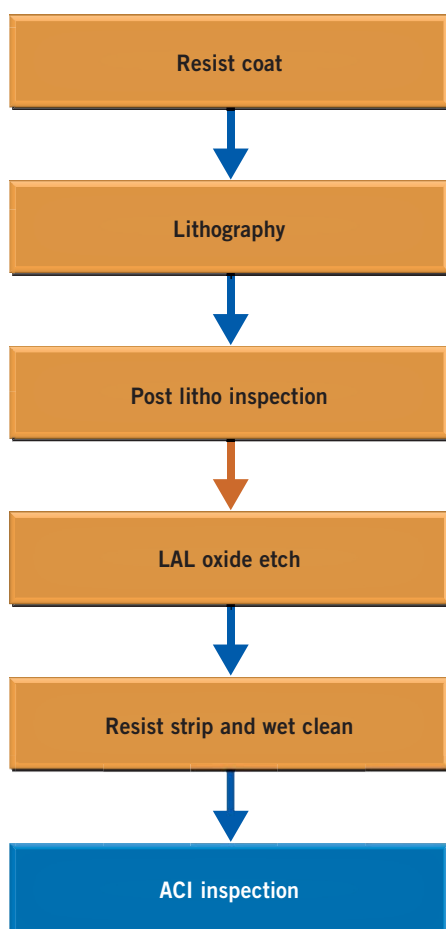
METROLOGY

Impact of charge during gate oxide patterning on yield

JUNGTAE PARK, Samsung Electronics Co.; **SUNGJIN CHO** and **JEFF HAWTHORNE**, Qcept Technologies Inc.

Detection of non-visual defects in the steps prior to optical inspection was used to trace the cause of a silicon pitting defect.

Achieving high yields in a leading-edge semiconductor manufacturing facility requires a dedicated effort to identify and eliminate the causes of defects that result in yield loss. Process measurement and inspection tools play a critical role in this effort by quantifying process variability and identifying the root cause of specific types of defects. A wide range of optical inspection tools have been developed to detect physical defects such as pits, particles and scratches. However, up to 30% of yield loss in today's fabs is not traceable to physical defects. Many of these yield issues are caused by Non Visual Defects (NVDs). NVDs are defects that are not detectable by optical inspection, and include sub-monolayer residues, contami-



nation, and process induced charging of dielectric films [1-3].

In this paper we discuss the detection and investigation of a silicon pitting defect. This physical defect was detected using standard optical inspection after an oxide wet etch operation, and resulted in yield loss at the end of line. Initial yield engineering efforts focused on varying the process conditions for the steps prior to inspection. This failed to eliminate the defect and was not successful in identifying the root cause of the pitting. Subsequent efforts focused on the detection of NVDs in the steps prior to inspection. This approach was successful in identifying the root cause, which enabled the optimization of the process and a

FIGURE 1. Process flow prior to detection of the silicon pitting defect at After Clean Inspection (ACI).

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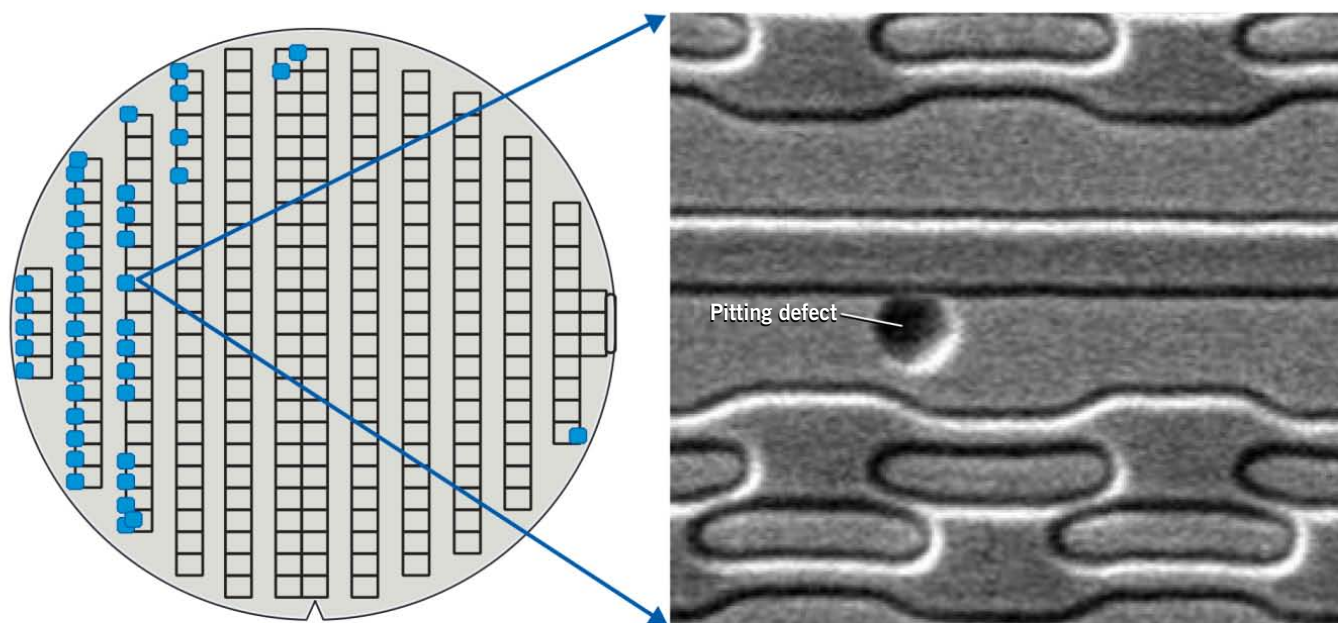


FIGURE 2. A defect map from a brightfield optical inspection tool used for ACI, and the SEM review image of one of the pit defects.

significant reduction in the overall defect rate, leading to higher end-of-line yield.

Figure 1 shows the process flow prior to the point at which the pitting defect was detected. A wafer with a thermal oxide film is coated with photoresist. The resist is then patterned using lithography. This creates openings in the photoresist where the oxide film will be removed by the wet etch process. An optical inspection is performed after lithography (Post Litho) and prior to the etch operation. A wet etch of the oxide film is then performed in a low ammonium fluoride liquid (LAL), after which the photoresist is removed and the wafer cleaned. Finally, an optical After Clean Inspection (ACI) of the etched wafer is performed.

Figure 2 shows a defect map from a brightfield optical inspection tool used at ACI. A large number of physical defects were detected, primarily near the left edge of the wafer. Scanning Electron Microscope (SEM) review was used to classify the defects as pits in the silicon surface. The image on the right of Fig. 2 is a SEM image of one of these pits.

The pitting defect was detected at ACI on 100% of the production wafers, and the defect maps showed strong correlation to end of line yield. The defect was not isolated to a single tool or set of tools, suggesting that the defect was induced by the process. The initial

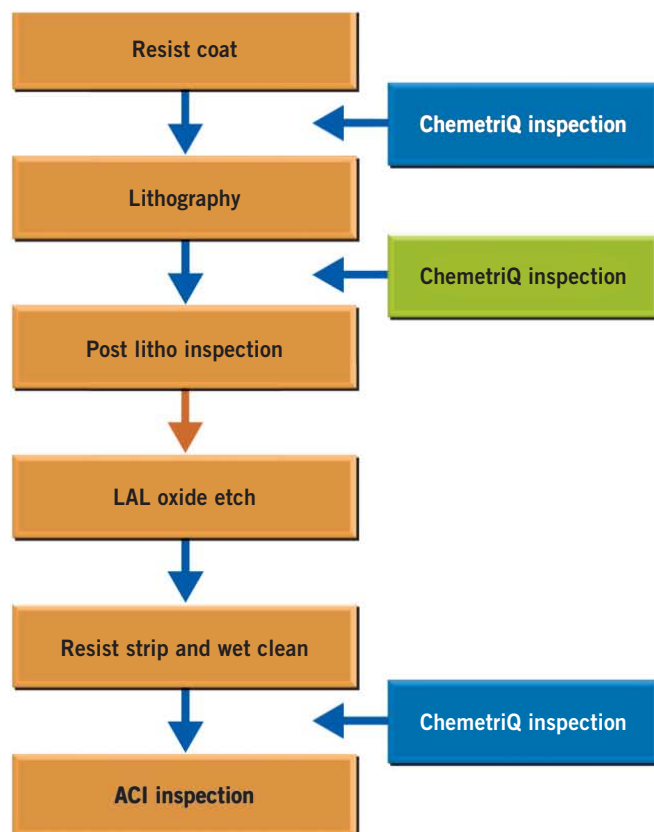


FIGURE 3. ChemetriQ inspection was inserted into three points in the process flow for detection of possible NVDs. NVD charge results identified the inspection point inserted prior to Post Litho Inspection as the source of the process induced charge (show in green).

METROLOGY

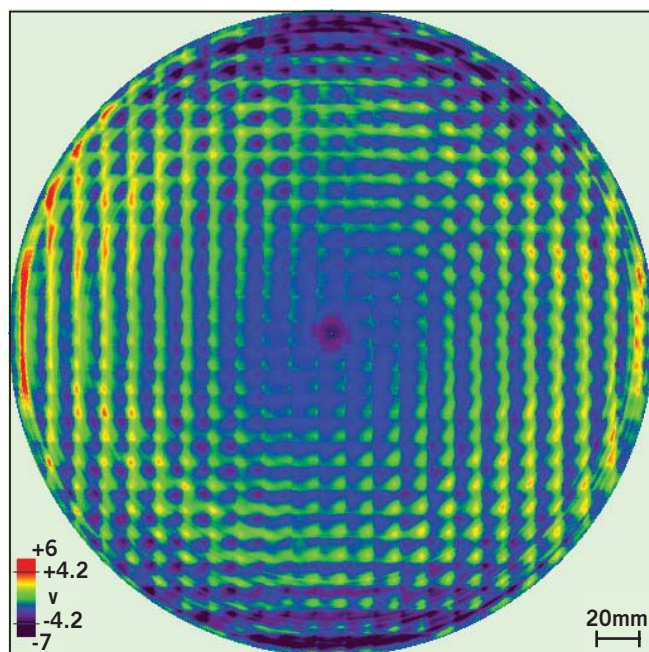


FIGURE 4. ChemetriQ charge map showing process-induced charge Post Litho.

assumption was that the defect occurred at the LAL oxide etch or the resist strip and wet clean operation. Experiments were run to vary the process conditions at these steps, but these variations had no effect on the number of defects. It was then decided to look at NVDs as a possible cause of the defect.

The ChemetriQ® inspection system from Qcept Technologies was used to inspect wafers at different points in the oxide etch process. This system uses a scanning surface potential difference imaging technique to generate fast, full wafer images of variations in the surface potential of a wafer [1]. Surface potential variations can be caused by several different types of non-uniformities such as sub-monolayer concentrations of contamination, including organics and

metallic, and by charge trapped on or in dielectric films.

The first study inserted ChemetriQ inspections at the same points in the process as Post Litho Inspection and ACI (**Fig. 3**). No residues or charge were detected at ACI, but at Post Litho charge patterns were detected on the product wafers. Specifically, high positive charge, resulting in peak surface potential values ranging from +4 to +9 Volts, was detected primarily on the left side of the wafer in the region of the pitting defect as shown in **Fig. 4**.

At this point, it was clear that the wafers were charged at Post Litho. An additional ChemetriQ inspection step was inserted after resist coat to better determine the source of the charge, as shown in Fig. 3. **Figure 5** shows ChemetriQ charge maps before and after lithography. Charge induced potentials after resist coat are near 0 Volts. However, after lithography the surface potential increases to greater than 4 Volts. This clearly shows that the source of the charge was the lithography step (expose and develop).

ChemetriQ inspection was implemented at Post Litho to monitor charge levels on production wafers. Peak charge levels were calculated on a per-die basis, thresholded, and exported to yield management software via KLARF files. The peak charge levels were well correlated with pitting defects detected at bright-field inspection (**Fig. 6**).

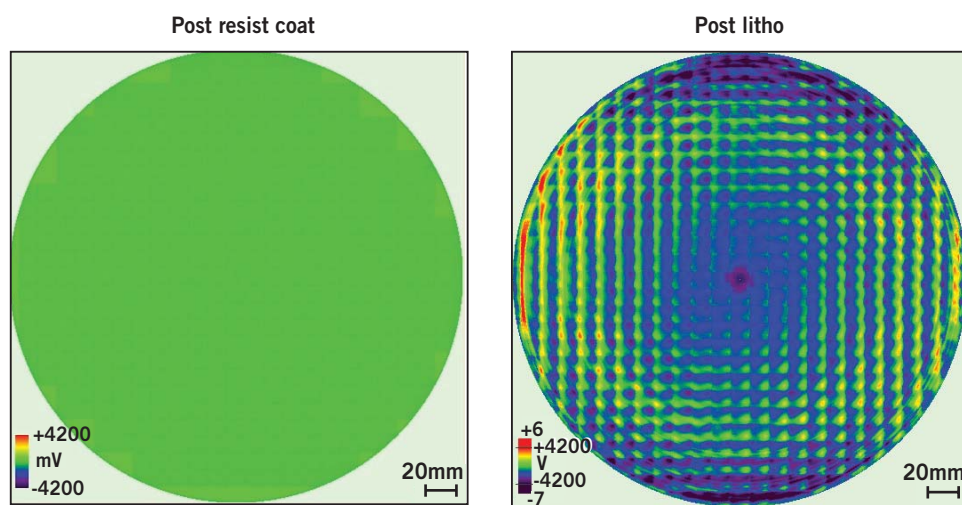


FIGURE 5. ChemetriQ charge maps of product wafers after resist coat and after lithography. Charge induced potentials after resist coat are near 0 Volts. Charge levels are much higher after the lithography process, where charge induced potential is greater than 4 Volts.

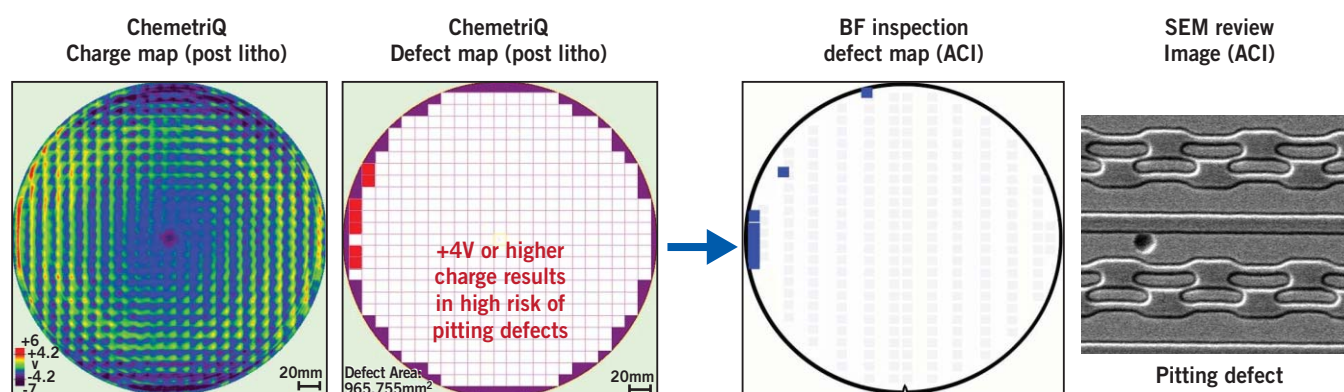


FIGURE 6. High positive charge levels were thresholded and correlated with pitting detected by brightfield optical inspection.

Additional experiments were run in an attempt to modify the lithography process to reduce charging and, potentially, the number of pitting defects. It was found that by altering the lithography rinse process, peak surface potential values could be reduced to +3 to +5 Volts. In addition to reducing the overall charge levels, the optimized lithography process also reduced the number of wafers that had pitting defects from 100% to less than 20%, and fewer die were affected per wafer.

The success in reducing pitting defects by reducing surface charge provides strong evidence that charge on the photoresist prior to oxide etch was a direct cause of the pitting. This raises the question of how positive charge on an oxide film can lead to silicon pitting during etch. It is well known that hydrofluoric acid can electrochemically etch silicon if the wafer is anodized [4,5]. However, in this case no potential was applied to the wafer. Positive charge on the photoresist would have the effect of attracting electrons and repelling holes at the surface of the silicon, depleting p-type silicon of holes and eventually attracting enough electrons to invert the surface. This charge-induced biasing of the surface could be an important factor in accelerated etch of the silicon near the charged film, but additional work is required to understand the precise mechanism leading to pits.

In some cases, NVDs affect yield without creating a corresponding physical defect. For example, sub-monolayer metallic contamination can affect material properties resulting in yield loss. In other cases, NVDs can lead directly to physical defects through known mechanisms such as electrostatic

discharge [3]. The pitting defect described here provides an interesting example where an NVD at one step in the process unexpectedly causes a physical defect at a later step in the process, which is then detected by an optical inspection tool. In this case the NVD, which is process induced charge, is a precursor to a physical defect, which is silicon pitting. This suggests that other physical defects might have precursor NVDs, such as charge or contamination, and that the detection of NVDs could provide useful insight into the cause of physical defects that are detected at later inspection steps. ◀

Acknowledgement

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PACKAGING

Bonding Wire: Is Scalability the Wave of the Future?

DOMINIK STEPHAN, RED Micro Wire Pte., Ltd., Singapore

*A new technology enables bonding wire to be cast instead of drawn.
The micro wire can be used like traditional copper bonding wire
but offers several advantages that make it more cost-effective.*

Miniaturization and scalability continue to be major trends in the semiconductor industry, and they necessitate that the entire manufacturing infrastructure adapt and evolve in order to grow. In order to facilitate such growth, and greater miniaturization, it is important that the entire industry works together to attain new development targets, including those of wire bonding.

Miniaturization of bonding is critically correlated with the number of bond pads that must be placed per unit area. In the case of ball bonding, each bond pad must fully accommodate the ball bond within the bond pad, without encroaching onto adjacent bond pads. The ball/pad reduction factor applied in the industry is typically between 70-80%.

Next in line of correlation is the FAB (free air ball) during the process of bonded ball formation. Typically, the FAB is about 10-20% smaller than the bonded ball, due to the squashing of the latter during bonding. At the moment, the limiting factor for this FAB diameter is the wire diameter, assuming a typical BSR (the ratio between the FAB diameter over the wire diameter) is about 1.6-2.0. If we assume the smallest wires currently in mass production are about 0.6mil (15 μ m), this means that the FAB is about 24-30 μ m, bonded ball about 29-33 μ m, bond pad about 33-36 μ m,

and bond pad pitch, at best, is 35-38 μ m.

Table 1 shows the correlation between process stage/bond pad pitch (BPP) and required bonding wire diameter to facilitate FAB formation.

The International Technology Roadmap for Semiconductors (ITRS) suggests the bond pitch should be down to 20 μ m in 2013. This will require a large leap in wire manufacturing know-how. Back-calculating indicates the need for wire of 8-10 μ m in diameter. All major

TABLE 1. Required bonding wire diameter (μ m)

year of mass production			2005	2007	2009	2013
process / BPP (bond pad pitch)	50	40	35	30	25	20
Bonded ball diameter	40	32	29.5	22.5	18.75	15
FAB diameter	32.4	31.0	27.0	18.7	15.6	12.5
Wire diameter (at FSR=1.6)	20	19	17	12	10	8
Wire diameter (at FSR=2.0)	16	16	14	9	8	6

wire bonding plants today are running 0.7mil copper wire (18 μ m) and have plans to qualify 0.6mil (15 μ m) within the next year or two. One of the critical factors for not seeking more aggressive targets is the lack of availability of a bonding wire of lower diameter and an infrastructure that supports such a process, including bonding machines and capillaries.

Current standard materials and tools make it possible to scale down to a certain level, but attempting to go beyond that leads to the figurative brick wall.

DOMINIK STEPHAN is the Director for Application and Product Marketing for RED Micro Wire (RMW) in Singapore.

Capillary manufacturers are producing caps for 0.6mil wire in mass production having a hole diameter of about $21\mu\text{m}$. There have been attempts to go as low as $15\mu\text{m}$, accommodating

0.5mil wires, mainly for Au wire bonding. For copper wire bonding designs, the sizes to date have been typically slightly larger.

Wire bonding infrastructure is so extensive that no other chip-interconnection technology can displace wire bonding in the foreseeable future, although other technologies, particularly flip chip, will experience increasing utilization. Increasing miniaturization of electronic circuits has put relentless pressure on wire bonding technology to (1) increase yields (<5 ppm defects); (2) decrease pitch (< $30\mu\text{m}$ for ball bonds) and (3) provide the lowest possible and ever decreasing cost.

Creating smaller wires – the challenges

Wire makers, wire drawing equipment manufacturers and tool makers are all approaching a boundary with existing technologies, although there are efforts to make smaller wires. When wire diameter is successfully reduced, more issues correlated with wire uniformity and production control of the low tension required during the drawing process appear. These may result in lower yield and higher cost. Another limiting point is the drawing die, which can experience high erosion and cause lower yields at very small diameters. Furthermore, once the wire is drawn to the final stage, it has dramatically “work-hardened” and must be recrystallized by an annealing process. This is typically done at about 30-60% of a metal’s melting point at which, in return, it loses significant strength. This introduces further breaks, lower yield and higher cost. In order not to break the wire or stretch it (which would weaken its mechanical performance), annealing tension must be controlled at <0.5g. This is much less than the tension control capability of the typical dancer arms and pulleys supplying the tension. Here new technologies would be needed to facilitate wire drawing and annealing processes for cost effectiveness.

Even if the wire can be successfully drawn, the properties of the wire itself can be a challenge. As diameter decreases, strength decreases as a square function (0.5 mil is 25% the strength of 1 mil).

Assuming an average copper wire, having a tensile strength of about

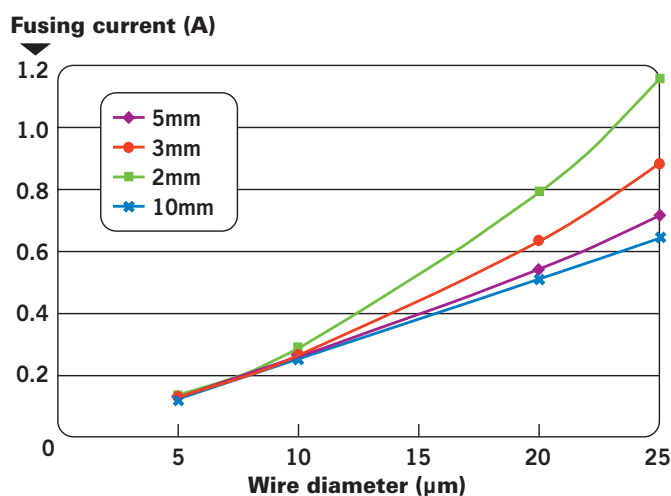


FIGURE 1. Fusing current (based on calculation) for wires of different wire diameter and testing length.

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TABLE 2. Comparison of breakloads

wire diameter	normal copper wire	soft copper wire	RMW glass composite
25 μ m	9.8	14.7	19.6
20 μ m	6.3	9.4	12.6
15 μ m	3.5	5.3	7.1
10 μ m	NA	NA	3.1
5 μ m	NA	NA	0.8

200MPa, the force needed to break the wire is only about 10g, making a 0.5mil wire only about 2.5g. Such a low material strength is very difficult to manually handle, and poses issues to testing strength during the application. The stiffness is a fourth power (0.5 mil is 1/16 the stiffness of 1 mil – stiffness = deflection under a load.) This poses many issues to the handling and the application of the wire. In general, elastic modulus is not the same as stiffness. Elastic modulus is a property of the constituent material; stiffness is a property of a structure.

Another inherent issue with lower wire diameters is the electrical performance. Naturally, the current carrying capacity is lower with lower diameter. This needs to be taken into consideration by packaging designers.

Recently there has been a new wire introduced that encases traditional copper wire in glass coating. Following, we'll take a look at how that wire scales versus traditional copper wire.

If wire properties are not sufficient, the wire will not hold its shape and will sag under its own weight. Here again a stiffer solution might help. Thinking outside the box, the ability to ignore the issue of adjacent wire shorting would ease this pain. However, increased strength is usually correlated to increased hardness, which is detrimental to the bond. The first bond poses a larger risk of cratering or bond pad deformation. The second bond poses the risk of lower strength values based on lower deformation and, respectively, a lower bond area. However, in glass coated wire, some of the strength comes from the glass layer, providing a geometric support. The hardness test shows that the copper core is even softer than a typically highly annealed copper wire, as seen in Table 3.

Table 2 is a comparison of breakload values (grams) for soft, normal and glass coated wire assuming 200,

300 and 400Mpa respectively (RMW wire is referred to as composite, because the glass is a structural member of the wire).

Table 3 wire hardness values of selected technologically available materials (*refers to the copper core).

In normal bonding wire, we need high elongation in copper to ensure sufficient ductility to make a strong second bond. However, in the case of glass coated wire, the EL/BL of the wire includes the glass, but the glass is not part of the first or second bond. So the wire EL will not be high, however the copper core is still very ductile.

From the tensile test chart in **Fig. 2**, one can see that the glass plays an initial part of providing strength and limiting ductility. After further elongation, the glass will eventually crack and give way to the extension of the copper.

Using smaller diameter wires

Let's look at the next step: How wires are used in the wire bonder. Users are having difficulty threading the wires and only highly experienced users are able to thread a 0.6mil wire though the wire path and into the capillary, without breaking it.

Further reduction in wire diameter will decrease visibility and, more dramatically, decrease the stiffness of the wire, which makes threading more challenging. A wire that is in its geometry stiffer than usual wire would make this process easier.

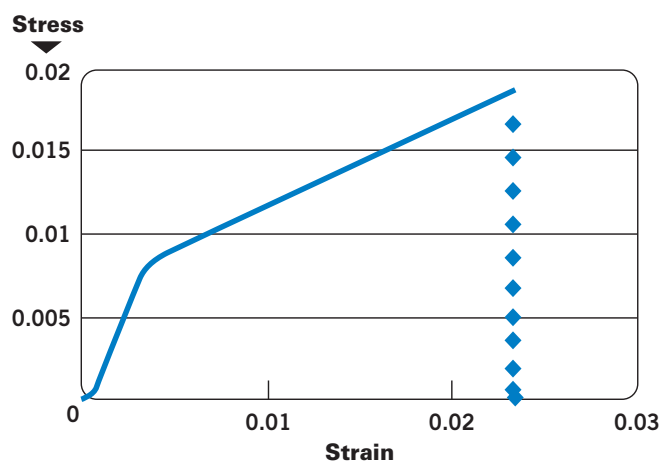


FIGURE 2. Tensile test chart of a RED Micro Wire glass-coated wire.

The next issue is related to the loop formation. A2 wire is supposed to keep its loop shape, which was imparted from the bonder trajectory during the loop formation (which is, most of the time, highly advanced with various forward and backwards motions).

The next step in the process is typically the molding process, where the wires are heavily exposed to mechanical stress/sweep. Mold compound viscosity and melt front velocities require scrutiny.

Another consideration on the infrastructure is the use of a wire bonding capillary as a tool for the bonding machine. Typically made from ceramic, they are currently only available in mass production, down to a diameter of about 15 μ m. They are getting increasingly difficult to make, but since there was no wire to drive the dimension, not enough effort has been applied to open these boundaries.

Glass-insulated wire – a solution to the problem

It is clear that there is a need for smaller wire diameter to support advances in miniaturization. There are, however, intrinsic challenges of physics that might limit the ability to manufacture and use such wire. Most of the issues are related the mechanical strength, and concerns about wire stability and shorting.

It seems natural to think about an insulated wire eliminating worry about shorting. Glass coated wire provides such an insulation and slightly inaccurate looping can be accommodated.

The issue of strength (or stiffness in this case) can also be addressed with the glass-coated wire. Glass that has an inherently higher strength compared to copper acts not only as a surface layer, but as an active element providing mechanical support to the wire. This leads to much higher strength and stiffness values compared to a bare copper wire (or any kind of coated wires, be it conductive or insulating).

Looking at the wire manufacturing process from a simplistic view, one could ask: How logical is it to cast the wire at a very large diameter, just to draw it down to a small diameter?

A solution whereby wire can be manufactured directly out from the melt covered by a glass coating is currently being tested and optimized for bonding wire applications.

Glass can greatly increase wire strength and stiffness, yet still provide a smaller, effective wire diameter on smaller bonds. Based on the manufacturing method, a full coverage of glass can be ensured, which in return ensures insulation. In addition, floor and shelf life are no longer limiting factors since there is no exposure of copper. ♦

Acknowledgement

The author would like to thank Dr. Jeffrey Seuntjens and Mr. Steven Creswick for their technical feedback, discussion and review, as well as the industry partners SPT, ASM, ITE and TPT for their experimental support.

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MEMS

Volume consumer markets are changing MEMS manufacturing

ERIC MOUNIER and JÉRÔME BARON, Yole Développement, Lyon, France

Changes in the way MEMS are manufactured are primarily being driven by high volume consumer MEMS markets.

High volume consumer MEMS markets are driving manufacturing changes across the MEMS industry, pushing companies to drive down die size, closely connect multiple die in combinations, and move towards an efficient infrastructure for system-level integration of high value solutions for final OEM customers. That means new demands—and new opportunities—for tighter process controls, more integrated wafer-level packaging technologies, more standard process and package platforms, and more software for easy-to-use integrated sensor solutions.

While the MEMS market still contains a highly diverse range of products, with plenty of specialty niches and high performance applications, it's also increasingly a volume consumer business. Consumer applications accounted for more than 50% of total MEMS industry revenue in 2011 (**Fig. 1**). And the four main devices for consumer mobile applications—accelerometers, gyroscopes, magnetometers and microphones—accounted for more than 50% of all MEMS units shipped last year (including automotive). Volumes will continue to expand, as smart phone shipments are likely to keep growing strongly, from 300 million units in 2011 to more than 800 million by 2016, and MEMS content per phone is also growing rapidly. More of

those MEMS devices will be combined into multisensor modules, both to reduce costs and to improve performance, as more accurate location and navigation information becomes a key distinguisher for smart phones. We expect these combo units will steadily replace discrete sensors and account for most of the growth in the inertial sensor market going forward, to become a \$1.7 billion opportunity by 2017.

Packaging innovations and production volumes drive die shrinks

Key to driving down costs to enable the growth of the consumer MEMS market is the rapid scaling down of die and package size. Over the last three to four

Sales forecasts (M\$)

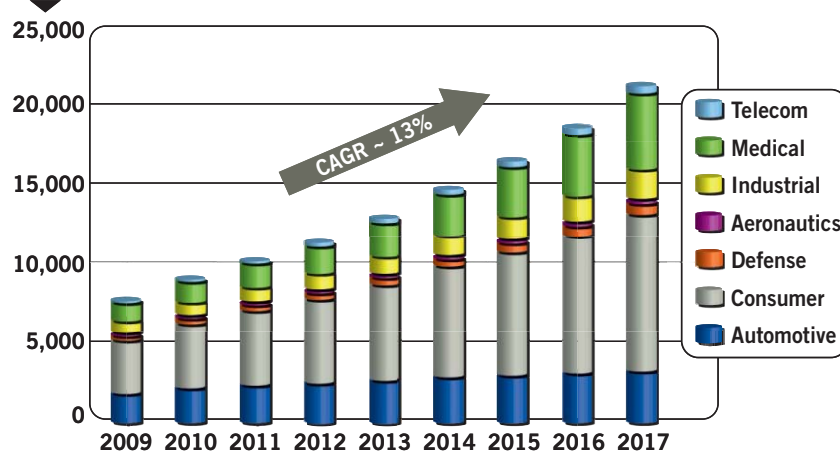


FIGURE 1. The MEMS market is increasingly dominated by consumer applications, which inescapably means high volumes, short product cycles times, and pressure for low costs. Source: Yole Développement.

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years, MEMS 3-axis accelerometer die have shrunk from 12mm^2 down to 2mm^2 . The next generation is headed to 1mm^2 die size. That has helped push production cost of the packaged and tested consumer accelerometers sharply down from nearly \$.40 in 2008 to \$.25 by 2011.

Gyroscopes are similarly shrinking fast. Typical 2-axis gyroscope die were 6mm^2 - 8mm^2 in 2007. Now InvenSense's 3-axis gyro is $\sim 4\text{mm}^2$. Manufacturing cost has come down accordingly, with the current 3-axis packaged gyros costing the same \$.75-\$.85 to produce as did old 2-axis versions three years ago.

Production volumes are one key contributor to driving down die size and costs. Though wafer volumes with the tiny MEMS die of course remain small compared to CMOS, MEMS wafer volumes are getting big enough to drive tighter manufacturing controls that allow driving down the feature size. Robert Bosch credits its consumer pressure sensor production for accelerating its tight control of its manufacturing process, as getting to multimillion unit volumes in months instead of years allows it to push the limits of size and thickness much faster, which it has then transferred to its automotive products. STMicroelectronics famously credits the high volumes of its single process platform used for all its accelerometers and gyroscopes for driving the tight process control to reduce structure size and maintain consistent performance across units.

Now new packaging approaches are starting to play an increasing role in shrinking the devices. The increasing use of metal-to-metal sealing to replace glass frit bonding frames will significantly reduce the die space required. SystemPlus' reverse engineering of STMicroelectronics latest 3-axis accelerometer, for example, shows it is using gold eutectic sealing instead of glass frit to shrink packaged die size from 4.7mm^2 in the last generation down to 2.1mm^2 . Wafer-level packaging and through-silicon or through-glass vias

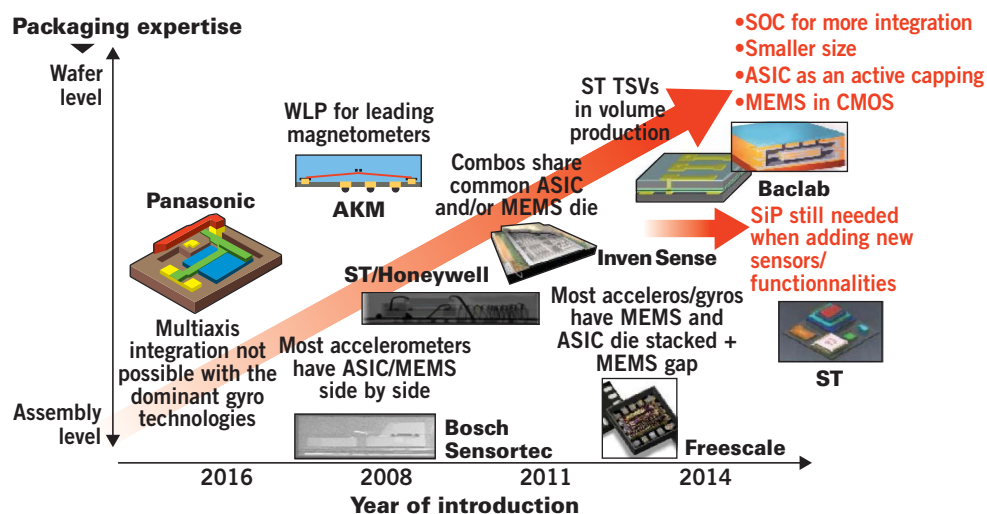


FIGURE 2. Demand for smaller, lower cost die, and faster handling of more complex multisensor data will drive MEMS packaging towards more value at the wafer level, with more TSVs and monolithic integration. Source: Yole Developpement.

are poised to reduce the contact pad area to shrink the die size even more. ST has recently launched an accelerometer with TSV, for example. By eliminating the area once used for I/O pads, the TSV process allows the MEMS die area to be reduced by $\sim 25\%$ compared to the usual accelerometer. It adds major manufacturing changes that increase the final wafer cost by more than \$100, but the reduction in die size still makes the final die cost competitive.

Combo sensors create new demands

The coming industry transition to combination sensors, putting two or more MEMS sensors in a single module, sharing one ASIC and one package, will also make more complex demands on backend processes (**Fig. 2**). Packaging, assembly and test currently account for some 35%-45% of the typical manufacturing cost of a MEMS accelerometer, more than either the MEMS die or the ASIC, and the added complexity of the combo modules will likely move even more of the value to these manufacturing steps. Effectively managing increasing volumes of sensor data from the combos, such as to reduce sensor drift for more accurate position sensing, will require shorter, faster connections between the components than the current standard wire bonding, likely driving the modules towards interposer and TSV solutions. That means the modules will need to be assembled with high yields from known good die to be economic, and then all six or nine or ten sensor axes tested and cross-calibrated.

MEMS

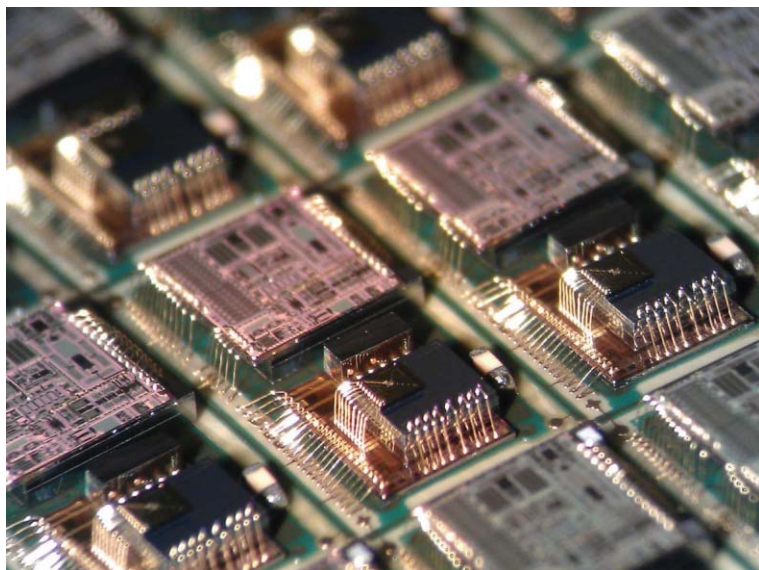


FIGURE 3. Inertial sensors combo stacked in SiP module on organic laminate substrate. Courtesy of STMicroelectronics.

Manufacturers will also need to figure out how to assure users of second sources for the complex multi-component systems. **Fig. 3** shows one example.

Cost and volumes drive MEMS

While most successful MEMS IDMS and foundries have long worked to re-use the same front-end process module for different devices as much as possible to speed time to market and time to yield, volume

consumer markets are driving the sector towards standard package platforms as well, as these consumer markets do not have the luxury of time or cost to support development of fully custom packages. Naturally the wide range of different MEMS devices will maintain their different needs, but several different types of standard platforms, driven by big players in big markets, will likely develop, such as WLP and TSV interconnects, or SiP modules with micro leadframes, or chip arrays using molded or cavity packaging (**Fig. 4**). For example, micro-phone packaging from major suppliers has all now settled around the same general platform MEMS and ASIC wirebonded in a SiP module on BGA/LGA laminate PCB substrate with an air access hole, under a metal lid.

Substrate suppliers and packaging subcontractors from the IC world are looking at developing libraries of building blocks or common platforms to ease development of MEMS packages for common product families. Unimicron in Taiwan, for example, is looking at giving a second life to its BGA or LGA substrate technology by developing a hole-making process to make the substrates suitable for multiple various MEMS applications. Tong Hsing Electronic

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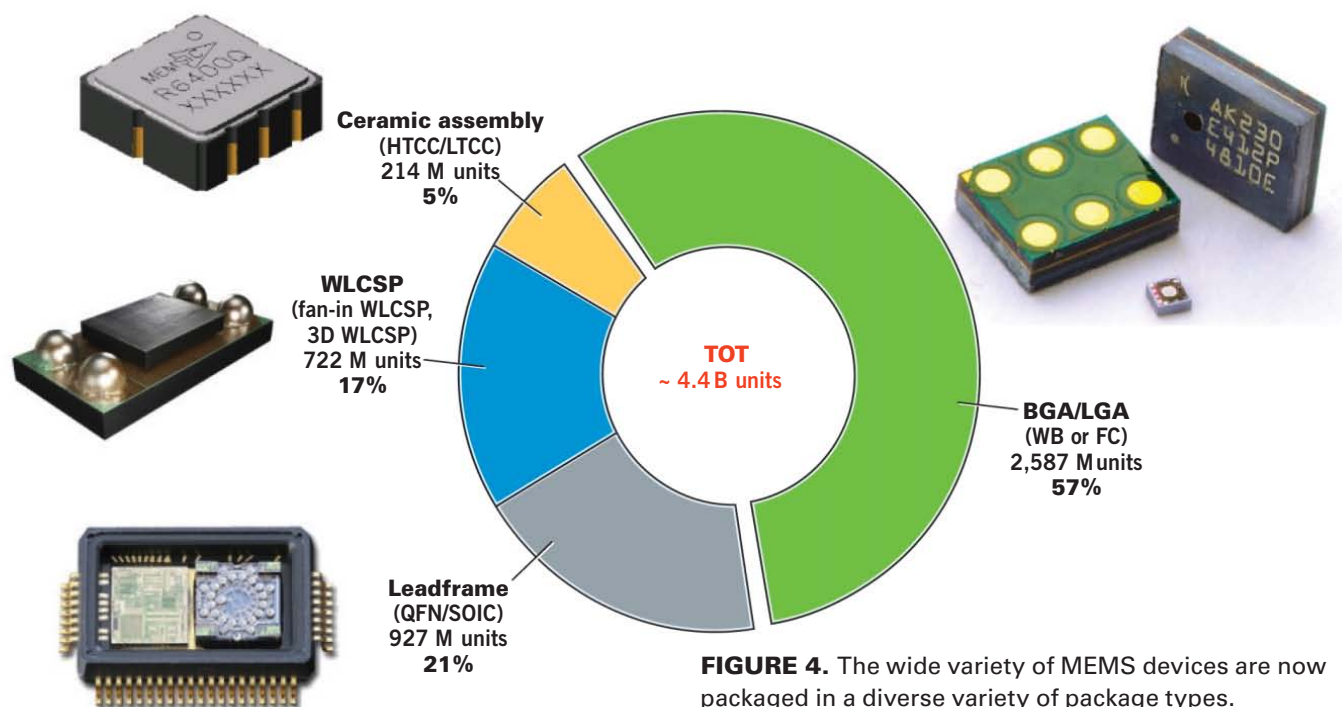


FIGURE 4. The wide variety of MEMS devices are now packaged in a diverse variety of package types.

METROLOGY

2D cross-sectional doping profiling study of advanced CMOS devices

SHU QIN, ZHOUGUANG WANG, Y. JEFF HU and ALLEN McTEER, Micron Technology Inc., Boise, ID.

Electron holography (EH), a powerful method for two-dimensional (2D) doping profiling, was used to study 2D cross-sectional doping profiles of advanced CMOS devices.

Electron holography (EH) was used to investigate two-dimensional cross-sectional activated dopant (carrier) profiles of the CMOS device SD regions, which are formed by two doping techniques, conventional beam-line ion implant and plasma doping (PLAD). Comparisons and correlations among 2D EH doping profiles, 2D doping profile simulations [1], and 1D SIMS/ARXPS impurity (B or As) profiles [2] are extensively investigated and evaluated. Correlation between 2D doping profiles and device parameters is also extensively investigated. The device structure is a standard self-aligned poly gate structure with a mask channel W/L ratio of

(nitride and oxide) was deposited by PECVD. PMOS device wafers were implanted by a conventional B beam-line ion implantation and a B₂H₆ PLAD process to form p⁺-type source and drain regions. The process conditions of the conventional B beam-line ion implantation are as follows: ion species is B⁺; energy is 2keV; dose is 5×10¹⁵/cm²; implant angle is 0°. The PLAD system is a pulsed, RF-excited continuous plasma-doping system, described in detail elsewhere [3]. The PLAD process conditions are as follows: the doping gas is B₂H₆, the nominal implant voltage and total dose are -6kV and 2×10¹⁶/cm², respectively. NMOS device wafers were implanted by a conventional

TABLE 1. Correlations among 2D electron holography data, 2D profile simulation data, and 1D SIMS data of PMOS devices

Implant Type	Species	Energy	Dose (/cm ²)	2D Electron Holography x _j (nm)			2D Simulation x _j (nm)			1D SIMS x _j *(nm)
				Vertical	Lateral	x _j (L)/x _j (V)	Vertical	Lateral	x _j (L)/x _j (V)	Vertical
Beamline	¹¹ B	2keV	5×10 ¹⁵	100.6	40.9	0.41	100.0	50.0	0.50	100
PLAD	B ₂ H ₆	-6kV	2×10 ¹⁶	110.7	46.1	0.42	NA	NA	NA	114

*1D SIMS x_j was defined at 2×10¹⁸/cm³ background concentration

6400nm/80nm and a gate oxide thickness of 40Å. Poly gates are 70nm in-situ phosphorus-doped poly-Si film for the NMOS device and counter-doped by B implant for the PMOS device. The raised source and drain regions were formed by an epitaxy process. SD spacer

As beam-line ion implantation and an AsH₃ PLAD process to form n⁺-type source and drain regions. The process conditions of the conventional As beam-line ion implantation are as follows: ion species is As⁺; energy is 10keV; dose is 8×10¹⁵/cm²; implant

SHU QIN, ZHOUGUANG WANG, Y. JEFF HU and ALLEN McTEER, Micron Technology Inc., Boise, ID.

METROLOGY

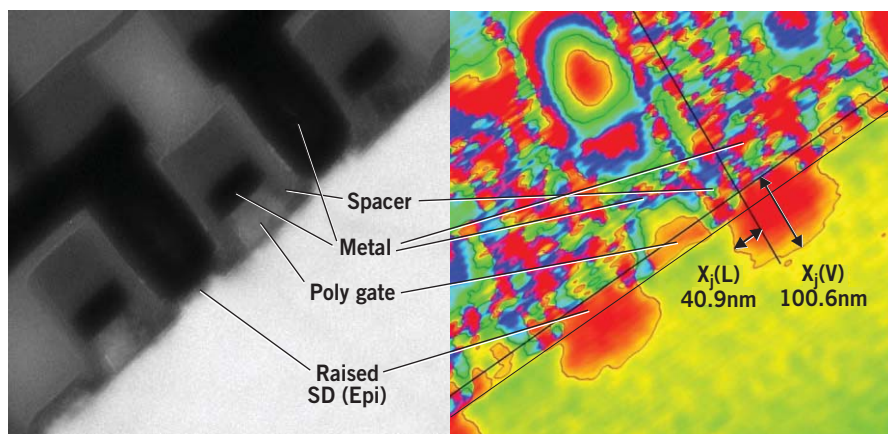


FIGURE 1. TEM and electron holography images of a PMOS device implanted by B beam-line implant with an energy/B dose of $2\text{keV}/5 \times 10^{15}/\text{cm}^2$.

angle is 0° . The PLAD process conditions are as follows: the doping gas is AsH_3 , the nominal implant voltage and total dose are -10kV and $1 \times 10^{16}/\text{cm}^2$, respectively. After SD implants, the implanted wafers were processed using standard strip/clean/rapid thermal-annealing process (RTP) to remove the photoresist film and activate the impurities. Contacts were formed by a standard Ti silicide/W-based metallization. After device manufacturing was completed, electrical characterization was performed. The device wafers processed with both implant techniques were sent for two-dimensional (2D) cross-sectional doping profile measurements by the EH technique. Single-crystalline Si blanket-monitoring wafers were processed with the device wafers through the implant/PLAD under

the same process conditions. Secondary ion mass spectrometry/angle-resolved x-ray electron spectroscopy (SIMS/ARXPS) method was used to measure the monitor wafers to find one-dimensional (vertical) as-implanted and annealed-retained impurity (B or As) profiles and doses in Si [2]. One-dimensional (vertical) impurity profiles in Si will be used to compare and correlate with 2D cross-sectional dopant profile results.

The cross-sectional TEM samples for electron holographic observations were prepared by focus ion beam (FIB) operating at 30keV . To obtain an uniform sample thickness, a sample piece was lifted out and milled from the back side (substrate side). All the samples were left thick enough ($\sim 300\text{nm}$) to reduce the effect of surface dead layers and produce higher p-n junction signals. Electron holography experiments were performed on a JEOL 2010F TEM equipped with a field emission gun and an electron biprism at 200kV acceleration voltage. Digital objective and reference holograms were collected using a 1024×1024 Gatan multi-scan charge coupled devices (CCD). To get a proper field of view for the currently studied devices, a Gatan Image Filter (GIF) was used to obtain extra magnification and better signal-to-noise ratio. The hologram pairs were

reconstructed using the Holoworks plug-in for Gatan DigitalMicrograph software.

In current work, the spatial resolution of the reconstructed electron holography images is estimated to be $\sim 5\text{-}10\text{nm}$, so the uncertainty of measurement from these images is $\sim 5\text{-}10\text{nm}$. The spatial resolution of electron holography is determined by the spacing of interference fringes in the recorded hologram, so it can be improved to be $\sim 1\text{nm}$ by decreasing fringe spacing. In addition, it is hard to precisely determine the positions of spacer

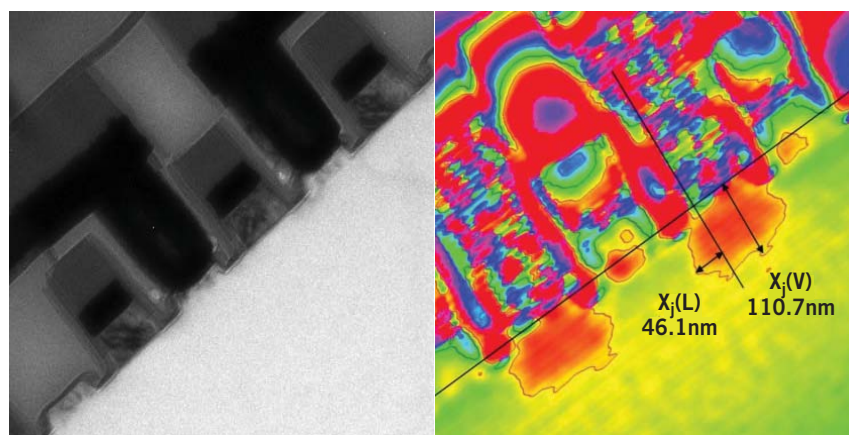


FIGURE 2. TEM and electron holography images of a PMOS device implanted by B_2H_6 PLAD with a voltage/total dose of $-6\text{kV}/2 \times 10^{16}/\text{cm}^2$.

TABLE 2. Correlations among 2D electron holography data, 2D profile simulation data, and 1D SIMS data of NMOS devices

Implant Type	Species	Energy	Dose (/cm ²)	2D Electron Holography x_j (nm)			2D Simulation x_j (nm)			1D SIMS x_j^* (nm)
				Vertical	Lateral	$x_j(L)/x_j(V)$	Vertical	Lateral	$x_j(L)/x_j(V)$	Vertical
Beamline	⁷⁵ As	10keV	8×10^{15}	80.0	42.0	0.525	95.0	48.0	0.505	59.4
PLAD	AsH ₃	10kV	1×10^{16}	82.0	48.0	0.585	NA	NA	NA	57.5

*1D SIMS $x_j(V)$ was defined at $2 \times 10^{18}/\text{cm}^3$ background concentration

walls in the reconstructed holography images, which may induce some errors for the lateral $x_j(L)$ measurements.

PMOS devices

Fig. 1 shows transmission electron microscopy (TEM) and EH images of a PMOS device implanted by B beam-line implant with energy and dose of 2keV and $5 \times 10^{15}/\text{cm}^2$. The EH method yields quantitative junction depth data based on electron wave phase/potential profiles. Because the green color indicates negative potential which represents electrons and the red color indicates positive potential which represents holes in the active region of the Si substrate, the contour line of 0 potential defines p+n junctions. As shown in **Fig.1**, the lateral junction depth $x_j(L) = 40.9\text{nm}$, vertical $x_j(V) = 100.6\text{nm}$, and $x_j(L)/x_j(V)$ ratio = 0.41. These junction depths are defined based on a combination of the TEM and EH images and process parameters.

Fig. 2 shows TEM and electron holography images of a PMOS device implanted by B₂H₆ PLAD with voltage and total dose of -6kV and $2 \times 10^{16}/\text{cm}^2$. The lateral junction depth $x_j(L) = 46.1\text{nm}$, vertical $x_j(V) = 110.7\text{nm}$, and $x_j(L)/x_j(V)$ ratio = 0.42. B₂H₆ PLAD shows slightly deeper of both lateral and vertical x_j and with a slightly larger $x_j(L)/x_j(V)$ ratio than the B beam-line implant.

Fig. 3 shows the final two-dimensional activated B profile of a PMOS device by process simulation [10] of B beam-line ion implant with energy/dose of 2keV/ $5 \times 10^{15}/\text{cm}^2$. The values of junction depth x_j are defined as the active carrier compensation, that is, hole concentration equal to electron concentration. The simulated lateral junction depth $x_j(L) = 50.0\text{nm}$, vertical $x_j(V) = 100.0\text{nm}$, and $x_j(L)/x_j(V)$ ratio = 0.50. 2D simulation results show very good consistence on $x_j(V)$, and slightly deeper $x_j(L)$ than 2D EH results because it is more difficult for 2D EH measurement to

define the lateral dimensions from such complicated lateral structures. There is no simulation for the PLAD process due to a lack of a PLAD dopant profile model.

Fig. 4 shows one-dimensional (vertical) SIMS profiles of B in the monitor Si wafers for B beam-line ion implant and B₂H₆ PLAD on annealed wafers. SIMS/ARXPS method was used to obtain an accurate B profile and dose in the silicon substrate [2]. SIMS measurement used O primary beam with energy of 1keV and normal incidence. As shown in **Fig. 4**, the B profile and dose components have been separated by the native oxide thickness, which is defined and decoupled by ARXPS measurement. The junction

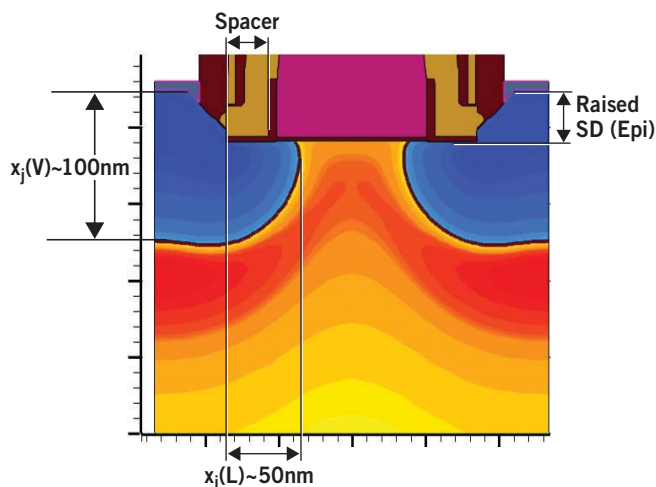


FIGURE 3. PMOS device final 2D activated B profile simulation of B beam-line implant with an energy/dose of 2keV/ $5 \times 10^{15}/\text{cm}^2$.

depth $x_j(V)$ are defined at $2 \times 10^{18}/\text{cm}^3$ background concentration. B₂H₆ PLAD with voltage/total dose of -6kV/ $2 \times 10^{16}/\text{cm}^2$ condition shows slightly deeper $x_j(V)$ than B beam-line implant with energy/B dose of 2keV/ $5 \times 10^{15}/\text{cm}^2$ condition, which is very consistent with 2D EH data. The slight discrepancy between 1D SIMS and EH data is a result of the different process steps between the blanket wafers for SIMS

METROLOGY

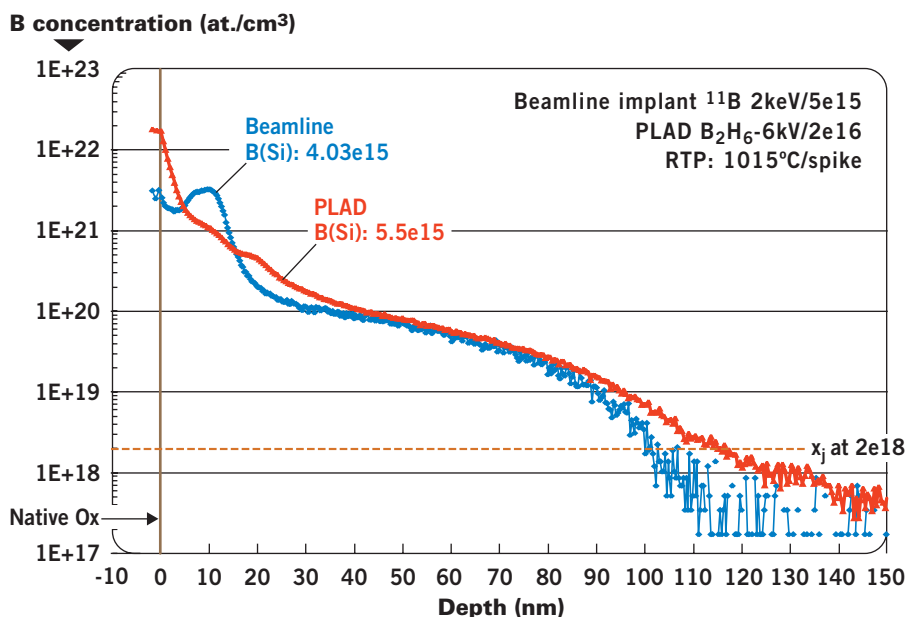


FIGURE 4. One-dimensional (vertical) SIMS profiles of B in the monitor Si wafers for B beam-line ion implant and B_2H_6 PLAD on annealed wafers.

measurement and the real device wafers for 2D EH measurement.

Table 1 shows comparison of B beam-line ion implant and B_2H_6 PLAD by different metrologies on vertical $x_j(V)$, lateral $x_j(L)$, and $x_j(L)/x_j(V)$ ratios. The error bars of EH measurement data, caused by a combination of the image definitions and EH measurement error bar, are within 10%. The error bars of SIMS measurement data are within 5%.

Reasonable correlations among 2D EH doping profiles, 2D doping profile simulations, and 1D SIMS/

ARXPS B profiles have been demonstrated. The discrepancy demonstrates the limits of the process simulations within the constraints of more complicated two-dimensional device structure and corresponding process steps. The results highlight that 2D process simulation cannot be implemented for PLAD process because of a lack of a PLAD doping model.

NMOS devices

Fig. 5 shows TEM and electron holography images of a NMOS device implanted by As beam-line implant with energy and dose of 10keV and $8 \times 10^{15}/cm^2$. Again,

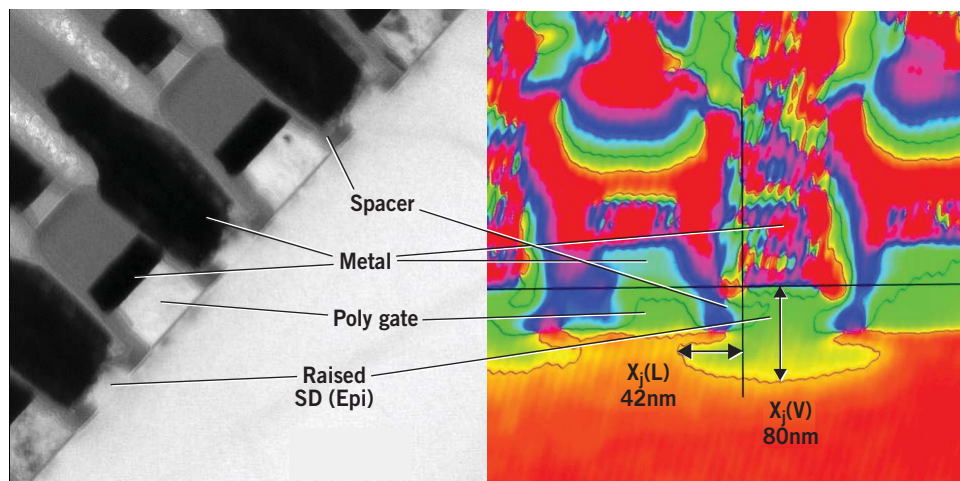


FIGURE 5. TEM and electron holography images of a NMOS device implanted by As beam-line implant with an energy/dose of 10keV/ $8 \times 10^{15}/cm^2$.

green color indicates negative potential which represents electrons and red color indicates positive potential which represents holes, the contour line of 0 potential defines n+p junctions. The lateral junction depth $x_j(L) = 42nm$, vertical $x_j(V) = 80nm$, and $x_j(L)/x_j(V)$ ratio = 0.525. **Fig. 6** shows TEM and electron holography images of a NMOS device implanted by AsH_3 PLAD with voltage and total dose of -10kV and $1 \times 10^{16}/cm^2$. The lateral junction depth $x_j(L) = 48nm$, vertical $x_j(V) = 82nm$, and $x_j(L)/x_j(V)$ ratio = 0.585. AsH_3 PLAD shows slightly deeper lateral and vertical x_j profiles, with a slightly larger $x_j(L)/x_j(V)$ ratio than the As beam-line implant. It is noticed that in **Figs. 5** and **6** there are p-type-like islands appeared near the corners of SD regions. They are EH measurement artifacts caused by the interface states of the SD spacers. It appears as an acceptor-like feature because PMOS device EH data in **Figs. 1** and **2** show much less impact.

Fig. 7 shows final two-dimensional activated

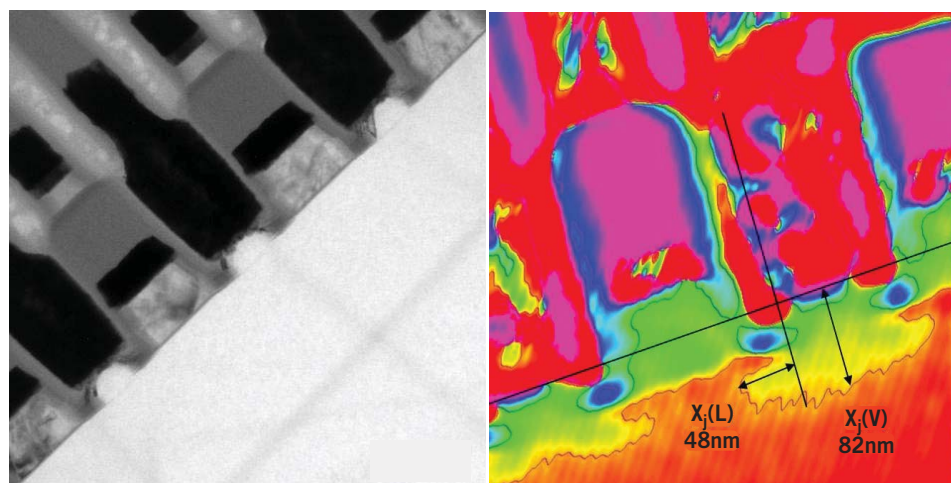


FIGURE 6. TEM and electron holography images of a NMOS device implanted by AsH₃ PLAD with a voltage/total dose of $-10\text{keV}/1 \times 10^{16}/\text{cm}^2$.

As profile of a NMOS device by process simulation [1] of As beam-line ion implant with energy/dose of $10\text{keV}/8 \times 10^{15}/\text{cm}^2$. The simulated lateral junction depth $x_j(L) = 48\text{nm}$, vertical $x_j(V) = 95\text{nm}$, and $x_j(L)/x_j(V)$ ratio = 0.505. There is no simulation for PLAD process due to a lack of a PLAD dopant profile model. 2D simulation results show deeper of both lateral and vertical x_j than 2D EH results.

Fig. 8 shows one-dimensional (vertical) SIMS profiles of arsenic in the monitor Si wafers for As beam-line ion implant and AsH₃ PLAD on annealed wafers. SIMS/ARXPS method was used to obtain an accurate As profile and dose in the silicon substrate. SIMS measurement used Cs primary beam with energy of 1keV and normal incidence. AsH₃ PLAD with voltage/dose of $-10\text{keV}/1 \times 10^{16}/\text{cm}^2$ and As beam-line ion implant with energy/dose of $10\text{keV}/8 \times 10^{15}/\text{cm}^2$ show very similar $x_j(V)$ on annealed wafers, and show fairly consistent (slightly shallower) x_j from 2D EH data. The slight discrepancy between 1D SIMS and EH data is a result of the different process steps between the blanket wafers for SIMS measurement and the real device wafers for 2D EH measurement.

Table 2 shows comparison of As beam-line ion implant and AsH₃ PLAD by different metrologies on vertical $x_j(V)$, lateral $x_j(L)$, and $x_j(L)/x_j(V)$ ratios.

Reasonable correlations among 2D EH doping profiles, 2D doping profile simulation, and 1D SIMS/ARXPS As profiles have been demonstrated. The discrepancy between 2D simulations and 2D doping

measurements is caused by two factors. One is because the simulation did not include an overetch process to form the SD contact window. The other factor is that the simulation modeling assumed a higher activation for As impurity [1]. However, the activation fraction of As under the current DT conditions is very low on the order of 34% [4]. The discrepancy also demonstrates the limits of the process simulations within the constraints of

more complicated two-dimensional device structures and corresponding process steps. The results highlight that 2D process simulation cannot be implemented for the PLAD process because of the lack of a doping model.

Although two-dimensional doping profiles by different metrologies show evidence of discrepancy or error, there is a clear trend to demonstrate that PLAD results in slightly deeper lateral junction depths $x_j(L)$ and slightly larger $x_j(L)/x_j(V)$ ratios than the beam-line counterpart under the current doping and annealing conditions. A slightly larger $x_j(L)/x_j(V)$ ratio of PLAD can be explained by its greater impact on the lateral profiles. The unique properties of PLAD, including

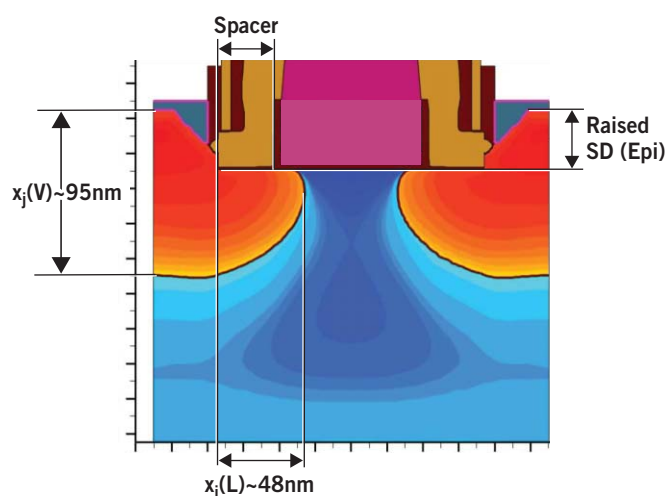


FIGURE 7. NMOS device final 2D activated As profile simulation of As beam-line implant with an energy/dose of $10\text{keV}/8 \times 10^{15}/\text{cm}^2$.

METROLOGY

higher surface impurity concentration and stable and repeatable parallelism of the ion trajectory compared to the incident angle variations of the conventional beam-line ion implants result in the greater impact on the lateral profiles of PLAD. A slightly deeper lateral junction depth $x_j(L)$ will result in a shorter effective channel length (L_{eff}) and cause a “hotter” short channel device, which will be indicated by a smaller device breakdown voltage (BV_{DS}), smaller V_T , and larger drive current (I_{DS}) and off current (I_{OFF}). However, short L_{eff} effects, by definition, will have less impact on long channel devices.

To confirm the 2D doping profile measurement data, both PMOS and NMOS device electrical performance were extensively investigated and evaluated. **Table 3** lists and compares electrical parameters for PMOS devices fabricated by B beam-line ion implant and B_2H_6 PLAD. **Table 4** lists and compares electrical parameters for NMOS devices fabricated by As beam-line ion implant and AsH_3 PLAD.

The diode breakdown voltages (BV_{DIO}) of the devices, which are dominated by the vertical junction depths $x_j(V)$, show similar for the devices processed by beam-line implants and PLADs, although PMOS device processed by PLAD shows slightly larger BV_{DIO} than that processed by beam-line implant. The BV_{DIO} data show a very good correlation with $x_j(V)$ data of 2D EH and 1D SIMS measurements. However, the devices processed by PLADs show “hotter” than those processed by beam-line ion implants, including lower BV_{DS} , lower V_T , higher transconductance (KL), higher I_{DS} , and higher I_{OFF} . The “hotter” device performance is attributed to a shorter effective channel length L_{eff} of

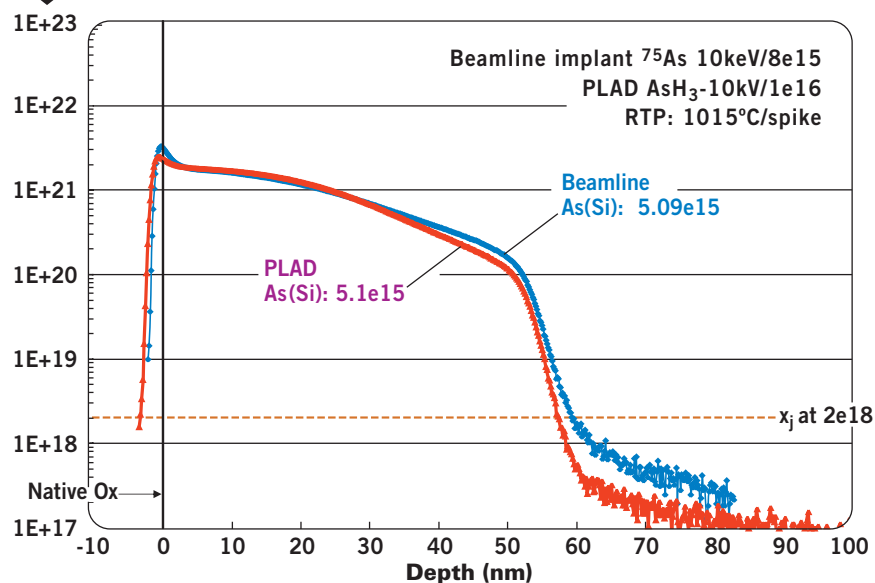
As concentration (at./cm³)

FIGURE 8. One-dimensional (vertical) SIMS profiles of arsenic in the monitoring Si wafers for As beam-line ion implant and AsH_3 PLAD on annealed wafers.

the PLADs than beam-line implants under the current process conditions. As shown in the tables, I_{OFF} is more sensitive to L_{eff} because I_{OFF} increases with decreasing L_{eff} in an exponential function. A slightly larger $x_j(L)/x_j(V)$ ratio of PLAD than Beam-line ion implant, and in turn, “hotter” device behavior confirm that PLAD shows more lateral impact on doping profile than beam-line ion implant. The electrical parameters of the long channel devices show little differences between beam-line implant and PLAD processed devices.

Conclusion

Electron holography, a powerful method for two-dimensional (2D) doping profiling, was used to study 2D cross-sectional doping profiles of advanced CMOS devices. The low energy high dose ion implantations were used to form source and drain (SD) regions of the advanced CMOS devices including conventional beam-line implant and plasma doping (PLAD). Good correlations among 2D EH dopant profiles, 2D dopant profile simulations, and 1D SIMS/ARXPS impurity (B or As) profiles have been demonstrated. Very good correlation between 2D electron holography doping profiles and device parameters has been demon-

TABLE 3. PMOS device electrical parameters (normalized)

Implant Type	Species	Energy	Dose (/cm ²)	Device Electrical Parameters (Mean)					
				BV_{DIO}	BV_{DS}	V_T	KL	I_{DS}	I_{OFF}
Beamline	¹¹ B	2keV	5×10^{15}	1	1	1	1	1	1
PLAD	B_2H_6	-6kV	2×10^{16}	1.10	0.84	0.86	1.29	1.60	45.5

TABLE 4. NMOS device electrical parameters (normalized)

Implant Type	Species	Energy	Dose (/cm ²)	Device Electrical Parameters (Mean)					
				BV _{DIO}	BV _{DS}	V _T	KL	I _{DS}	I _{OFF}
Beamline	⁷⁵ As	10keV	8×10 ¹⁵	1	1	1	1	1	1
PLAD	AsH ₃	-10kV	1×10 ¹⁶	1.01	0.51	0.83	1.03	1.05	7.4

strated. It has been found that both p- and n-type PLADs show slightly deeper lateral junction depths $x_j(L)$ and with slightly larger $x_j(L)/x_j(V)$ ratio than beam-line counterparts when keeping similar vertical junction depths $x_j(V)$ as beam-line counterparts. The findings increase the capability to predict the potential impact of process parameters and architecture changes that may be required to meet the performance needs of advanced CMOS devices. ◀

Acknowledgement

Additional contributors of this work are: Wendy Morinville, Kent Zhuang, Xue-Feng Lin, Kari Noehring, Chantelle Krasinski, and Shifeng Lu for SIMS/ARXPS measurements; Jaydip Guha for 2D process simula-

tions; and Rob Burke for the coordinating and technical assistance. Thanks to Drs. John Smythe and Kamal Karda for the technical review and corrections. All of them are with Micron, Boise, ID, USA.

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MEMS

Continued from page 28

Industries (THEIL) is similarly looking to develop a portfolio of re-usable blocks to speed development of MEMS packages for common product families.

Testing and calibration of the sensors –and increasingly cross calibration of sensors with other kinds of sensors perhaps from other suppliers—are also becoming more standardized to reduce costs at higher volumes. Test already accounts for some 18% of manufacturing costs, and testing and cross-calibrating more different stimuli in combination is becoming more complicated and requiring more costly equipment, with more sites in parallel for higher throughput. Companies like STMicroelectronics, which traditionally developed their own calibration equipment in house, are increasingly turning to buying commercial equipment from vendors like SPEA. Higher volumes and cost pressures will continue to push the industry towards the use of more standard high throughput commercial equipment, as well as drive efforts towards better design for test, more wafer level testing, and more testing service providers.

Higher volumes, more common platforms

This maturing of the MEMS business to a higher volume, less custom business may open opportunities for players from the IC world, who have so far played little part in this specialty, artisanal business. With MEMS volumes getting to levels where statistical process control starts to make sense, GLOBALFOUNDRIES claims that using CMOS-style monitoring, feedback and control at every step enabled it to go from equipment install to qualified products for volume production in what is, for the MEMS industry, a lightening pace of under two years. Fabless InvenSense has ramped its volume gyroscope business at TSMC and GLOBALFOUNDRIES. In a year when the overall MEMS foundry business is significantly lagging the 17% expansion of the industry overall, with only ~5% growth, players from the CMOS side did relatively well. TSMC saw 15% growth, and Xfab 33%. ▶

VACUUM

Efficiency in sealing: A BKM case study

DALIA VERNIKOVSKY, Applied Seals North America Inc., Newark, CA, and **BRAD ECKER**
and **SETH URBACH**, Microchip Technology, Inc., Chandler, AZ.

This case study describes Microchip's experience with perfluoroelastomers o-ring seals.

There are many reasons to review the productivity of equipment, whether processes are being upgraded or efficiencies need to be reviewed for optimal performance. In this case study, a best-known method (BKM) approach was taken to optimize the tool platform and the preventive maintenance (PM) cycles for that platform. The study was the result of a collaboration between a Microchip team of equipment engineers, technicians and process engineers, and an engineering/sales team from Applied Seals North America (ANSA).

We focused on three aspects of equipment optimization:

- The failure modes of existing seals (o-rings) were evaluated. In this case, six used seals were examined and a failure analysis (FA) conducted for each.
- The equipment was audited for proper sizing of the seals, as well as chemical compatibility. One of the six seals required special sizing and geometry to assure the optimal life of the sealing element. **Figure 1** depicts several different failure mechanisms observed. It's important to note that most of the FFKM family of seals has a high concentration of the

polymer base versus fillers. As a result, size and shape rarely influence higher costs (the terminology, FFKM, indicates the TFE backbone polymers that distinguish this material).

- We ensured that the seals were properly installed. Half of the failures of FFKM materials are typically a direct result of overstretching or twisting the material in the groove because most technicians are unaware of the sensitivity of these materials to basic



FIGURE 1. Seal failures can be caused by compression (left), powdery contamination from etching (middle), or damage due to poor installation (right).

handling issues. For example, white or translucent FFKM materials cannot be stretched on average of more than 3% and must be formed to shape in order to avoid stress points which allow early etching or chemical attack.

Tests took place with the incumbent seals on one

DALIA VERNIKOVSKY, is the CEO of Applied Seals North America Inc. **BRAD ECKER** is a senior process engineer at Microchip and **SETH URBACH** is an equipment engineer at Microchip Technology Inc.

chamber and the new seals on another chamber to accurately depict the same conditions when the test began.

Figure 2 depicts the data obtained, indicating a new seal design and new material of construction (a new compound) doubled the life of the products.

The need for standards

Why was this test so important? Newer generation sealing components – FFKMs, otherwise known as “perfluoroelastomers” -- are recognized for their chemical resistance and general ability to reduce contamination. However, if the components are not carefully evaluated and set in the equipment properly, new failures will arise. These failures take a great deal of time and money to be identified and resolved, which impacts productivity. This was the case at Microchip, where the seals exhibited a limited life expectancy.

Unfortunately, standards for this new generation of seals have yet to be adequately defined for the semiconductor industry. As a result, there is a significant gap in understanding how these parts must be installed and handled. This lack of understanding can result in significant hours of downtime. However, with the proper training and education for this new generation of product, these failures can be avoided and manufacturers can use “the right seal for the right application,” ensuring minimal downtime and reliable production runs. ASNA is heading the effort to generate these much needed standards through SEMI/Sematech, chairing a committee (F51-0200) to create such a document. The goal is to establish some level of performance criteria to guide our industry. More attention and participation by end-users and OEMs will assure that these standards are effective in areas of process, types of performance attributes and some criteria to capture those performance parameters (more information to be found at www.appliedsealsna.com)

The lack of understanding can also create a disasso-

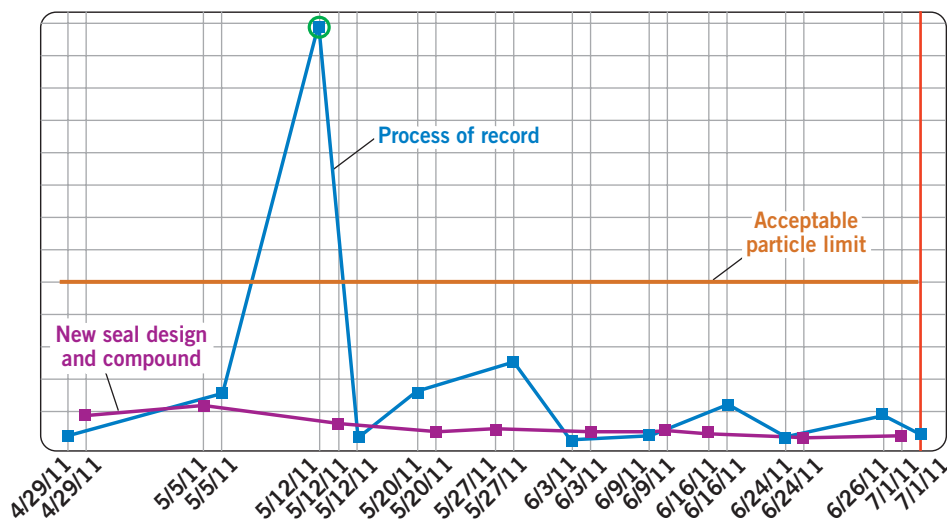


FIGURE 2. SPC chart of weekly tool qualification. On 5/12, the chamber was brought back into control with process response (no maintenance intervention).

ciation between the o-rings that are thought to be the answer to resolve advanced processes and their ability to do their job, that is, to seal (advanced processes include all the new hafnium precursors, harsher fluorine cleans and smaller and smaller killer defect parameters predominantly in etch, CVD and 22nm and below nodes). The conventional wisdom is that the “cleaner” the o-rings, the more they will be etched away and, as a result, the less they will mechanically fit. This issue can be avoided if the o-ring is designed properly and handled appropriately from the outset. Without addressing this important issue, failure of seals will continue to impact productivity and their misapplication will continue to cost the industry. Failures could continue to be factors in hardware of all types of advanced technologies and issues of chemical breakdown or mechanical failure will continue to be encountered. If these issues are not addressed, the effects of their misapplications and mishandling could impact the advances of these technologies for years. This is especially true because the cleaning gases (now generally NF_3) continue to evolve, and potentially have an even great impact on the life of the seals.

Many families of sealing elements are considered the same, when they are, in fact, very different one from the other and are not interchangeable. A basic knowledge of what they are made of, how they are made, the various

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New Products

SEMICON West Products

SEMICON West is taking place July 10-12 at the Moscone Center in San Francisco, CA.

High-current ion implant

The Applied Varian VIISta Trident single-wafer, high-current ion implant system embeds dopant atoms on 20nm wafers at high yields. The VIISta Trident precisely

tailors dopant concentration and depth profile to optimizing dopant activation and suppress defects in the extension, source/drain junction and contact regions at 20nm. The tool has a proprietary dual-magnet ribbon beam architecture for enhanced performance at low energy.

The system's Energy

Purity Module virtually eliminates high-energy species that can "smear" the transistor channel. Integrated cryogenic technology enables production implants as low as -100°C. **Applied Materials Inc.**, South Hall, **Booths 407, 552, 847, 1135, 2051, 2219.**

Ion beam system

MicroSystems' new IonSys 800 precision ion beam tool provides structuring and finishing processes down to a sub-nanometer scale. It features proprietary ion beam sources and is fully compatible with reactive ion beam processing based on fluorine and chlorine gas chemistry. The IonSys 800 system suits industrial ion beam etching and



deposition processes with high quality and productivity requirements. Its automatic handling robot features a cassette load-look and can be configured in cluster layouts. **MicroSystems**, South Hall, **Booth 1924.**

Automated temporary bonding/debonding system

The EVG850 TB/DB XT Frame from EV Group is an automated temporary bonding and debonding system for thin wafer handling, configured to address high-volume 3D IC and TSV manufacturing. The system temporarily bonds a device wafer to a rigid carrier wafer for safe and efficient processing of the device wafer. After subsequent processing (back thinning, lithography, metallization, etching, through via processing, etc.), the device wafer is debonded from the carrier substrate using various techniques dependent of the intermediate material.

The system can be configured for LowTemp debonding methods like ZoneBOND technology with the required EZR (Edge Zone Release) and EZD (Edge Zone Debond) modules. A thermal-activated, mechanical slide-off is utilized for thermo-plast materials, while UV-exposure and lift-off debond is utilized for UV-activated tapes. It accommodates up to 9 process modules and boasts a continuous-mode operation with an ultra-fast handling system, up to 4 FOUP load ports, a material buffer in the form of a local FOUP storage system holding up to 10 additional FOUPs, and in-line metrology module option. **EV Group**, South Hall, **Booth 719.**



MOCVD trap

Nor-Cal Products provides MOCVD device manufacturers increased up time with their new three-stage trap.

Features include a removable water coil assembly and particle filter with 50% greater capacity. The trap reportedly offers lower initial cost, lower cost of ownership, high capacity for extended PM, and ease of cleaning for GaN MOCVD reactors; AsP MOCVD reactors; and Aixtron G3, G4 and G5 systems. **Nor-Cal Products**, South Hall, **Booth 2441**.

Aluminum transfer valves

HVA's new high-performance aluminum slit valve range offer a slim profile and low vibration/particle levels, with reportedly light weight and high strength. Each valve component meets the throughput requirements of coating systems with up to 3 million cycles before maintenance. The valves are available in a range of sizes up to 2000mm as well as standard MESC 200/300/450mm sizes. **HVA**, South Hall, **Booth 2625**.



450mm WaferSense auto vibration system

CyberOptics Semiconductor Inc. added a 450mm form factor to its WaferSense Auto Vibration System family. Users put the wireless, wafer-like product through semiconductor fabrication processes to measure vibrations of wafer transfers in x, y and z dimensions. It can be used to observe and optimize wafer, cassette, SMIF and FOUF

motions without exposing process areas to the environment. The data helps establish yield-based vibration standards for equipment, identify vibration sources, and set acceptable acceleration parameters for equipment. Companion vibration monitoring software



allows engineers to set low, high, and band pass filters of equipment vibration frequencies to troubleshoot for vibration-related contamination. The software also allows engineers to collect and display acceleration data wirelessly to see the effects of adjustments in real-time. **CyberOptics Semiconductor**, South Hall, **Booth 2406**.

Electrochemical deposition tool for packaging

TEL NEXX's new plating tool, Stratus Thunder, is used for electrochemical deposition of TSV, middle and interposer, lead-free, copper pillar, and RDL advanced packaging materials. Stratus Thunder features a low-cost vertical plating architecture and additional features improve its productivity by up to 50%. **TEL**, South Hall, **Booth 1531**.



Packaging materials for LEDs, power semiconductors

ALPHA Argomax Silver sinter pastes and films suit power semiconductor die attach applications. Argomax was engineered to perform in fast-sintering, high-volume manufacturing to form lead-free metallic silver bonds. Alpha's Die Transfer Film process is a combination of ALPHA Argomax 8020 film and Datacon equipment capabilities. Alpha's Lumet line of lead-free solder paste covers a broad range of LED applications. Atrox conductive adhesive suits die attach applications. The company also makes solder spheres and fluxes for CSP and WLP. Alpha will introduce ultra-high precision stencils developed for semiconductor manufacturing applications. **Alpha**, a business unit of Cookson Electronics, South Hall, **Booth 2341**.

Watch the *Solid State Technology* website for many more product previews of SEMICON West.

VACUUM

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parts that include cross-linking agents, curative variations, and fillers must also be considered. Triazine cures (developed for high-temperatures reaching 300°C) are good for diffusion processes but not optimal in etch and CVD as they can become sticky when various chemicals are introduced. Peroxide-cured materials are superior for chemical resistance and cover over 80% of the process requirements in this industry. This is an important factor in the successful application of materials matched to successful production requirements. Along with that, basic fillers such as BaSO₄, TiO₂ and silicas are used but once again, understanding that there are many variations and forms of these materials will help discern how well they perform under these requirements (i.e., process dependency, cleaning gases, throughput, particles, etc.).

In summary, there are many key issues and challenges our industry faces with these components. As exemplified by a project dedicated to reducing particles on EUV mask blanks – a joint effort between SEMATECH and ASNA -- it was ascertained that many of the particles that led to defects were actually traced to the seals used in the deposition tool for the blanks. This program is dedicated to bringing EUV technology into practical use for the 22 nm node and beyond, yet must still deal with what some common hardware issues that remain unresolved.

Conclusion

Moving forward, work should focus efforts required to achieve the levels and types of particles, fillers, materials and designs that will facilitate the advancement of our science and assure that the industry's future aspirations will be met. Seals are only one element, but as more and more is discovered about contamination sources, we must address them so that they do not limit the ability to reach the levels of advancement we can achieve. The conclusion: working with material experts and components will indeed be a path that will enable the successful implementation of advanced technological leaps. ♦

Acknowledgement

Research and input provided by Brad Ecker, Project Leader and Seth Urbach, Equipment Engineer for the Microchip and the full team that was pulled together to make this project possible.

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Government's support for long-term research

The Federal government continues to send encouraging messages that the 2013 budget will include support for basic long-term university technology research in physical science and engineering.

As an industry, we cannot emphasize enough the critical role that university research plays in the future of technology and the nation's economy in general. The world-class U.S. university system built through decades of steady government support serves as a foundation for public-private partnerships, such as the Semiconductor Research Corporation (SRC), a non-profit industry consortium that partners with government agencies to support additional university research. This combined investment has produced new ideas and relevantly educated graduates, who have fueled our next-generation technologies and served as our technology leaders.

University research is America's ace in the hole. It is the means by which we educate the best and brightest, and it isn't a spigot that can be turned off and on without hamstringing the educational system and the nation's future economy. The university research engine has made the U.S. the cradle of discovery and

innovation that created industries including aerospace, biotechnology, information technology and all that is enabled by the Internet.

These high-tech industries, which share the semiconductor as their empowering workhorse, have generated tremendous economic growth and millions of highly skilled and highly paid jobs. Moreover, the semiconductor industry has enhanced the standard of living worldwide through the products it enables that shape our lives. These computer chips were born in the U.S. thanks to farsighted investment in basic research by the Federal government.

Today's technology-based economy critically depends on a robust university research enterprise—producing fundamental scientific advances and, just as importantly, well-educated scientists and engineers who can compete in a global economic playing field. What's not easy is finding the resources—the brightest minds and the funds—to fuel that research, especially in challenging economic periods. Funding further research for future innovation

Funding further research for future innovation is a delicate balancing act, to say the least

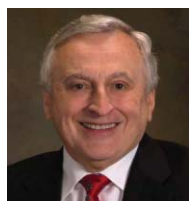
is a delicate balancing act, to say the least. For the past 30 years, SRC-funded research has involved students, faculty and industry experts working together. In these challenging

economic times, this model of collaboration can and should be extended.

Collaboration among industry, academia and government accelerates knowledge advancements, lowers risk and enables growth and innovation to continue for the benefit of industry and society as a whole. Industry taps into the expertise and pipeline of talent in academia, and university researchers gain understanding of industry needs.

However, collaboration requires these three sectors to work in unison; take any one out of the equation, and the likelihood for success significantly diminishes. In order for consortia such as SRC to survive and thrive in such economically tough times, government involvement is more important than ever. Moreover, basic research has a dramatically increased chance for success and return-on-investment when managed as part of a collaborative public-private program.

We salute the President and Congress for supporting basic research in general, and the National Science Foundation and National Institute of Standards and Technology (NIST) in particular. Programs such as the National Nanotechnology Initiative's Signature Initiative for Nanoelectronics for 2020 and Beyond and the Advanced Manufacturing Technologies Consortium proposed at NIST will continue to seed innovation and provide the people and ideas to keep the U.S. semiconductor industry competitive. Our nation can't afford *not* to plant the seeds of future knowledge, technology and talent. ♦



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