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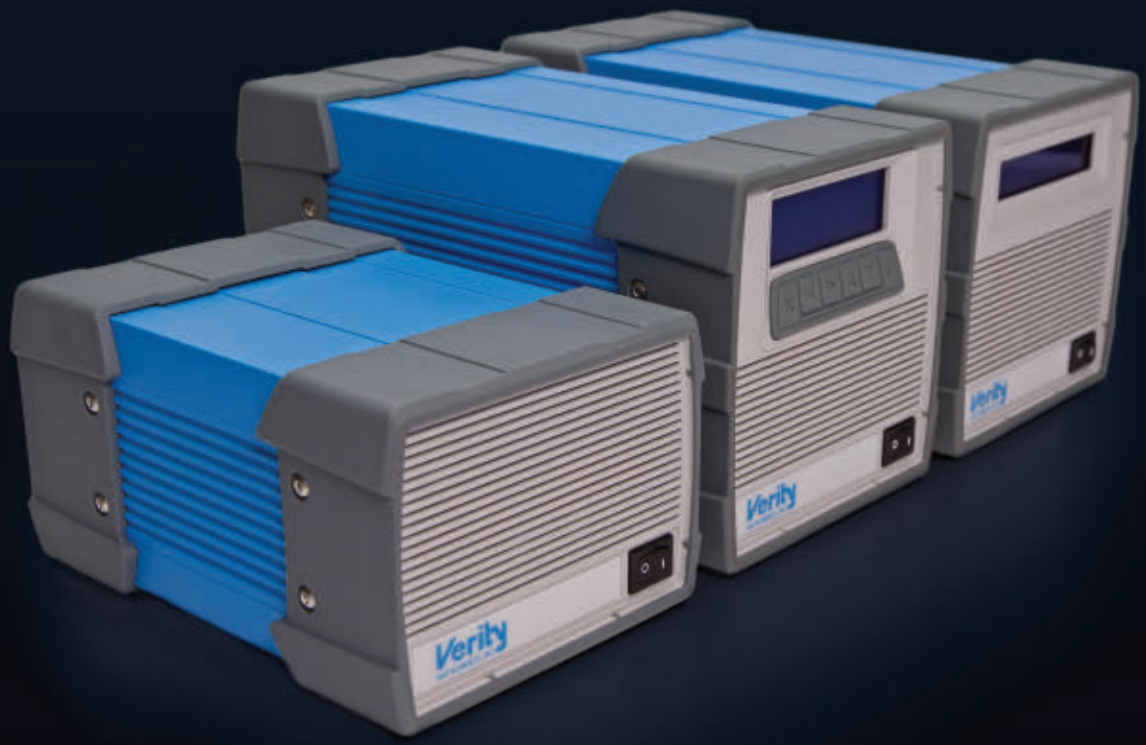

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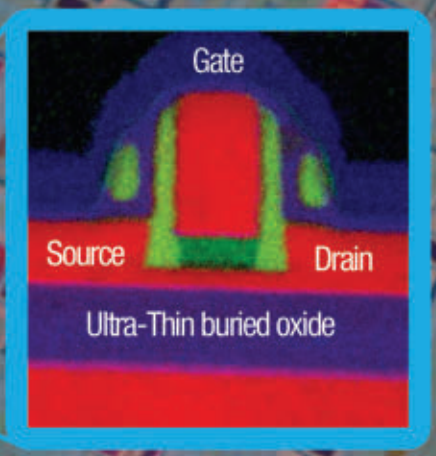

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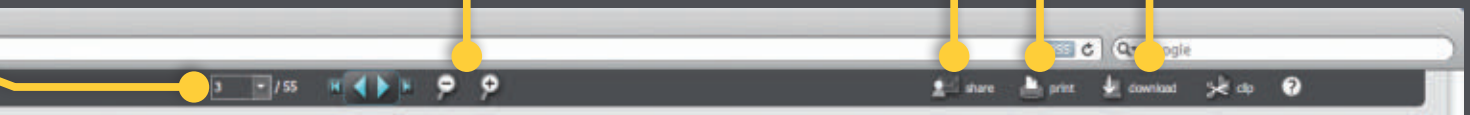

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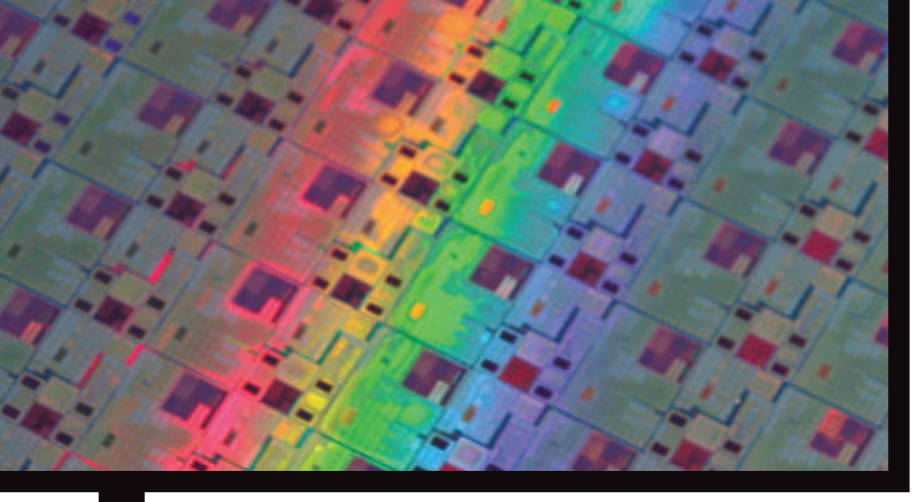

Solid State TECHNOLOGY®

JULY 2013 VOL. 56 | NO. 5

Fully depleted (FD) transistors are recognized as an effective solution for reducing the VT variability caused by random dopant fluctuation (RDF). As a planar technology, FD-SOI applies existing and design and process experience to small-channel transistors. Source: ST Microelectronics.

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450mm – It's bigger than you think

Much has been said of the 450mm transition. But the description of this inflection is something of a misnomer. Though everyone desires a smooth, coordinated and orderly conversion, it may be a little less placid than the term "transition" implies. Rather, I suggest calling it the 450mm "transformation." Because, even for the segments that continue manufacturing semiconductor devices on 300mm and 200mm silicon wafers, the industry will change dramatically with the introduction of 450mm wafer processing.

http://bit.ly/19M928x

Necessary attributes of a MEMS engineer for new product development

In the development of new MEMS products, the team is the most important factor. With this in mind, let's review the necessary attributes that make these engineers and entrepreneurs so successful in MEMS new product development.

http://bit.ly/14sfjEg

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Economy threatens semi growth, not technology–so say fab engineers at ASMC

Chipworks' Dick James reviews ASMC 2013. "I always come away impressed by the quality of the engineering involved; not being a fab person myself any more, it's easy to get disconnected from the density of effort required to equip a fab, keep it running and bring new products/processes into production," he says. **http://bit.ly/14OT8VB**

Tune in to the Solid State Watch

Want to stay up-to-date, but only have a few minutes? Check out our weekly newscasts for a recap of leading industry headlines.

http://bit.ly/17LtRQs

Insights from the Leading Edge: The future of packaging

Everyone understands the "Moore's Law Coming to an End" arguments. Dr. Phil Garrou believes that exactly when it will happen is less relevant than the fact that it is happening or has already happened for many mid-tier IC fabricators. Some top-tier fabs / foundries will find a way to move forward past 22nm to 14nm and beyond, but the important point is that the vast majority won't. This is not because the technology won't be available to them, but rather because it will be too expensive.

http://bit.ly/12fsU3B

A new inflection point for Solid State Technology

At press time, inflection points have been top of mind, as we get ready for The ConFab. I've been reviewing all the presentations and looking forward to a fantastic event. A recurring theme is that the semiconductor industry is at an inflection point as process complexity and cost increase, consolidation across the supply chain continues, and as the need for greater synergy between design and manufacturing becomes ever more apparent.

At Solid State Technology and The ConFab, we are also at an inflection point. I'm delighted to announce that we are now part of Extension Media LLC. San Francisco-based Extension Media operates more than 50 business-to-business magazines, engineers' guides, email newsletters, web sites and conferences, including Chip Design, ChipDesignMag.com, EECatalog.com, Embedded Intel® Solutions, Embedded Intel® Solutions China, EmbeddedIntel.com, AutodeskCatalog.com and the Multicore Developers Conference. Extension Media also co-produces SLDCommunity.com, LP-HP.com and SemiMD.com in partnership with the Sperling Media Group.

> The requirements of mobile devices have become the main driver in the industry.

Andy Grove, Intel's co-founder, described a strategic inflection point as "an event that changes the way we think and act." That's certainly true for me, as I look at the expanded reach of our combined forces and the potential for greater synergy between Solid State Technology, Chip Design and Extension Media's other brands.

As far as the rest of the semiconductor industry goes, it's clear that wafer costs are rising at a faster rate, partly due to increased process complexity and the delay in EUV. The cost/transistor is increasing by Moore's Law is slowing. 450mm may help, but the cost model has to be proven.

On the other hand, the requirements of mobile devices on PPAC (power, performance, area and cost/complexity) have become the main driver in the industry. It's quite possible that some consumer-driven disruptive technology is around the corner. Chips embedded in flexible displays? Internet of Things. Bioelectronics in clothing? Those are already happening.

What's the next inflection point? The ConFab 2014 will take place on June 22-24 in Las Vegas at The Encore at the Wynn. Mark it on your calendars, and I'll see you there.

—Pete Singer, Editor-in-Chief

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worldnews

EUROPE | **Silicon Labs** announced its agreement to acquire Energy Micro AS.

USA | **GLOBALFOUNDRIES** unveiled certified design flows to support 2.5D IC product development at the 50th Design Automation Conference in Austin, Texas.

EUROPE | **Fraunhofer Institute for Solar Energy Systems ISE** will partner with EV Group to develop equipment and process technology to enable electrically conductive and optically transparent direct wafer bonds at room temperature.

ASIA | Researchers from **Ulsan National Institute of Science and Technology** in South Korea and University of Illinois, U.S.A, developed the large-scale heteroepitaxial growth III-V nanowires on a silicon wafer.

EUROPE | **Alchimer** announced plans to collaborate with imec to evaluate copper filling solutions on advanced nano-interconnect technologies.

ASIA | **United Microelectronics Corporation** joined IBM's chip alliance for 10nm process development.

USA | **Intel** purchased the Global Navigation Satellite System business unit of ST-Ericsson.

ASIA | At **VLSI 2013 Symposium** in Kyoto, Japan, imec highlighted new insights into 3D finFETs and high mobility channels scaling for the 7nm and 5nm technology node.

Abu Dhabi doubles down on semiconductor research

The Advanced Technology Investment Company (ATIC) and the Semiconductor Research Corporation (SRC) last month launched the ATIC-SRC Center of Excellence for Energy Efficient Electronic Systems (ACE4S), to be hosted jointly in Abu Dhabi by Khalifa University of Science, Technology and Research, and Masdar Institute of Science and Technology. ATIC will dedicate over AED 17.5 million to the project over the next three years, which will be matched collectively by Masdar Institute and Khalifa University for a total budget of more than AED 35 million. This funding will drive innovation in next-generation electronic systems ranging in applications from smart phones and medical devices to the Internet of Things.

"This center is a significant research milestone for Abu Dhabi, the UAE and the region," said Sami Issa, Executive Director at ATIC. "ACE4S is a critical building block of our ecosystem strategy to help enable the development of homegrown talent in key areas of science and technology. Such talent development is essential as Abu Dhabi transitions into an innovation-based society as per the 2030 vision."

"Over the past 30 years, SRC has successfully helped establish numerous university research centers and distributed more than $2 billion dollars in research funds in the United States; ACE4S role as our first international center reflects significantly on the quality of research we pursue," said SRC President Larry Sumney. "The ACE4S Center has been established with valuable industry guidance from companies such as GLOBALFOUNDRIES, AMD, Applied Materials, Freescale, IBM, Intel, Mentor Graphics, Texas Instruments and Tokyo Electron (TEL) and will build on SRC-sponsored university research supporting 15 individual researchers in the UAE. Top semiconductor industry experts will oversee and serve as liaisons for each research task, and SRC will productively guide the overall research while also promoting strong student engagement—enabling us to identify areas of greatest need and foster the move of innovations from lab to market."

The center will be overseen by a steering committee of high-level ATIC, SRC, Khalifa University and Masdar Institute representatives and will be directed jointly by Professors Mohammed Ismail of Khalifa University, and Ibrahim Elfadel of Masdar Institute. The directors will oversee research across five targeted areas and work closely with a Technology Advisory

Board (TAB) of representatives from industry-leading companies.

GLOBALFOUNDRIES will serve a special role on the TAB, assigning Mohamed Lakehal as an Abu Dhabi-based industrial liaison to oversee design tape-outs to fabrication in GLOBALFOUNDRIES' facilities worldwide. The liaison will also support design enablement, deploying design-for-manufacture tools and raising the level of local semiconductor expertise.

"As a research-oriented institution, we are proud to be part of the ACE4S leadership and offer our expertise and research capabilities," said Dr. Fred Moavenzadeh, President, Masdar Institute. "Our faculty will aim to develop microelectronic technologies with healthcare applications individually and in collaboration with their peers within the initial period of the center's operation. These innovative products will include biosensor applications, wearable devices and self-powered wireless body area networks (WBAN). We believe these applications will have a wide impact because of their energy efficiency and novel designs."

"This partnership will transform the way we conduct research in nano-scale energy efficient systems-on-chips as it will help us educate and train a highly skilled workforce with relevant skills. This is a key element in driving innovation and entrepreneurship in the UAE's semiconductor sector in line with the Abu Dhabi 2030 vision," said Dr. Tod A. Larsen, president of Khalifa University. "The involvement of the SRC and its member companies in center development will help create a world-leading institution with a sustainable university/

Continued on page 6

GLOBALFOUNDRIES unveils plans to accelerate adoption of 20nm-LPM and 14nm-XM finFET processes

At the 50th Design Automation Conference (DAC) in Austin, Texas, GLOBALFOUNDRIES unveiled a comprehensive set of certified design flows to support its most advanced manufacturing processes. The flows, jointly developed with EDA providers, offer support for implementing designs in the company's 20nm low power process and its 14nm-XM finFET process. Working closely with Cadence Design Systems, Mentor Graphics and Synopsys, GLOBALFOUNDRIES has developed the flows to address the most pressing design challenges, including support for analog/mixed signal (AMS) design, and advanced digital designs, both with demonstration of the impact of double patterning on the flow.

The GLOBALFOUNDRIES design flows work with its process design kits (PDKs) to provide real examples that demonstrate the entire flow. The user can download the design database, the PDK, detailed documentation and multi-vendor scripts to learn how to set up and use the GLOBALFOUNDRIES design flow.

"As the developer of the industry's first modular 14nm finFET technology and one of the leaders at 20nm, we understand that enabling designs at these advanced process nodes requires innovative methodologies to address unprecedented challenges," said Andy Brotman, vice president of design infrastructure at GLOBALFOUNDRIES.

Production ready AMS flow from specification to verification

To address the unique requirements of analog/mixed signal (AMS) design at advanced processes, GLOBALFOUNDRIES enhanced its design flows to provide production quality scripts and packaged methodologies. The new reference flow establishes a working flow from specification to physical verification that has been taped out to be verified on working silicon.

The AMS reference flow provides comprehensive double pattern design guidelines. It gives overview of decomposition flow for both block level and chip level. The flow also addresses decomposition for different design styles. Recommendations for color balancing, hierarchical decomposition, ECO changes are discussed. The flows also present decomposition impact on DRC run time and resulted database size.

Notably, the reference flow includes support for efficiency and productivity improvements in the Cadence Virtuoso environment specifically for designing in a double patterned process. The flow includes support for Virtuoso Advanced Node

Continued on page 10

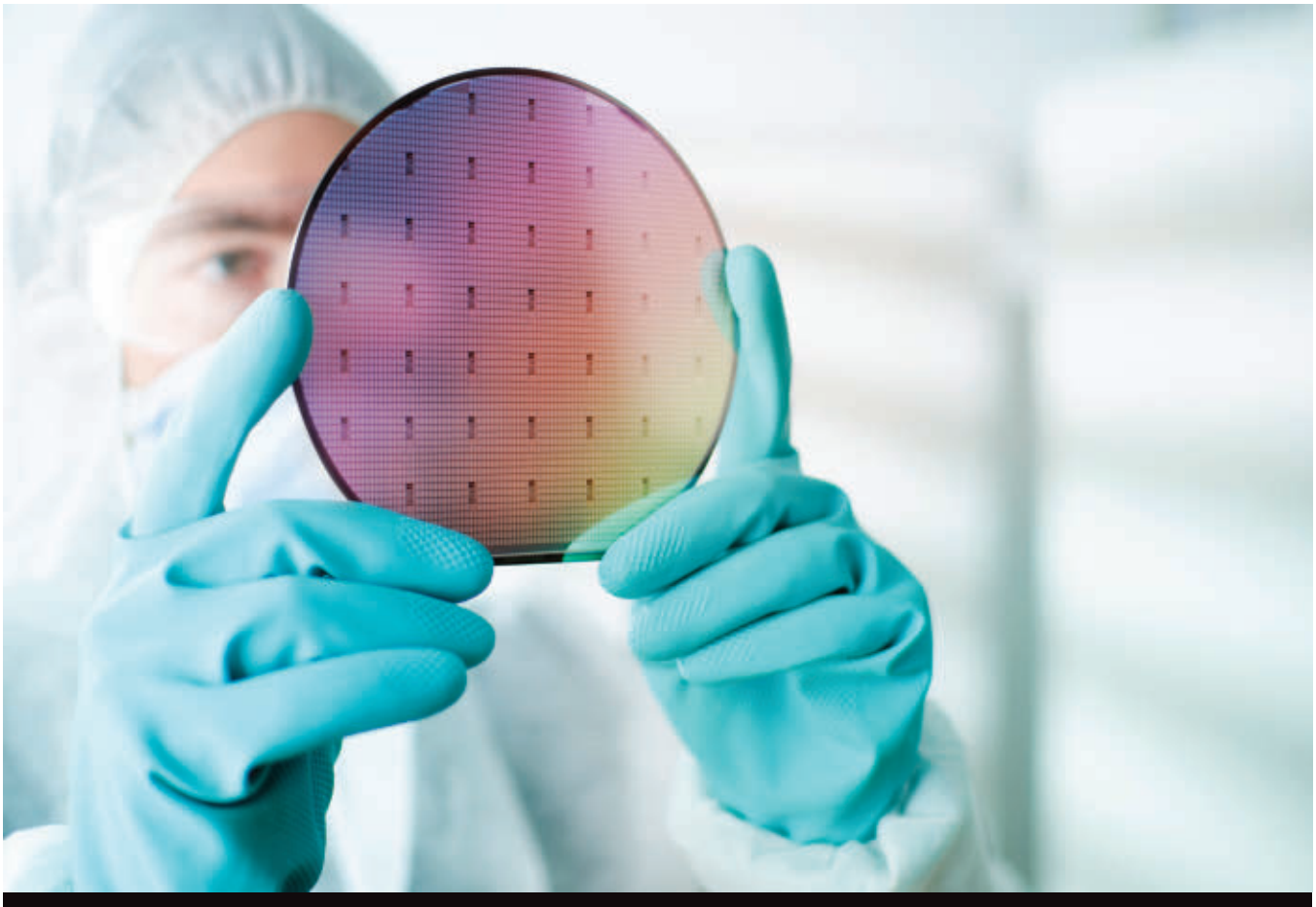
Semiconductor research *Continued from page 5*

industry collaborative research environment conducive to high-tech job creation and direct local and foreign investment."

The center will focus on energy efficient devices with research in energy harvesting, power management, sensor technologies and wireless communications networks. The research will be conducted primarily at Khalifa University and Masdar Institute but with important involvement from UAE University, American University of Sharjah and New York University, Abu Dhabi. Within the first three years, ACE4S will seek to produce integrated prototypes with healthcare applications as well as knowledge and research relevant to safety and security, aerospace, water quality and the environment.

Supporting the transition of innovations to market, the center will develop an aggressive Intellectual Property Management Plan (IPMP). The IPMP will include early identification of interconnected families of innovation arising from technical themes, placing special emphasis on the integrated systems selected for demonstration at the end of year three.

ACE4S is a continuation of ATIC's broader focus on cultivating a technology research ecosystem within Abu Dhabi. Additional programs supported in this vein include: the Twin-Labs research center, a collaboration between Masdar Institute and Technical University of Dresden with support from the State of Saxony, ATIC and GLOBALFOUNDRIES; the ATIC professorship chairs at UAEU and Khalifa University; the Masters in Microsystems degree in collaboration with Masdar Institute; and ongoing MEES research grants in collaboration with the SRC.



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Bosch and STM tie for No. 1 MEMS supplier of 2012

For the first time ever, no clear winner has emerged to claim top honors in the MEMS business for 2012, with Bosch of Germany and French-Italian STMicroelectronics ending up evenly splitting the title of No. 1 supplier for the year, according to a MEMS Competitive Analysis Report from information and analytics provider IHS.

With both companies just shy of the $800 million mark, Bosch and STMicroelectronics each had MEMS revenue of approximately $793 million in 2012. The two companies do not use the same exchange rates every quarter when converting their revenue from euros to the U.S. dollar, and as a difference of less than 1 percent separates the revenue levels of both, IHS found it was not possible this time to declare a clear winner as to who was No. 1 for 2012.

"With billions of dollars up for grabs, competition in the MEMS market is intense," said Jérémie Bouchaud, director and senior principal analyst for MEMS & sensors at IHS. "Nowhere is the rivalry more furious than the battle for the market's top spot. In fact, the content for number one is so closely contested that Bosch and STMicroelectronics battled each other to a draw in 2012."

Top 20 IDM and Fabless MEMS Suppliers Worldwide in Revenue (in Millions of US Dollars)

Rank	Company	2012	2011
1	Bosch	793	735
2	STMicroelectronics	793	644
3	Texas Instruments	751	776
4	Hewlett-Packard	676	748
5	Canon	377	369
6	Denso	298	292
7	Panasonic	296	308
8	Knowles Electronics	292	272
9	Analog Devices Inc	285	257
10	Freescale Semiconductor	255	245
11	Epson	223	246
12	Sensata Technologies	200	190
13	InvenSense	186	144
14	Avago Technologies	167	193
15	VTI	163	135
16	Infineon Technologies	156	139
17	General Electric	141	132
18	JDSU	114	103
19	FormFactor	109	115
20	TriQuint Semiconductor	109	91
	Others	1,957	1,828
	Total	8,342	7,961

MEMS in the money

Overall, the top 20 MEMS manufacturers last year accounted for a whopping 77 percent of the industry total of some $8.3 billion, as shown in Table 1. The figure excludes foundry revenue in order to avoid double-counting of fabless and foundry takings within the same ranking. For instance, excluded is MEMS foundry revenue from STMicroelectronics for its fabrication of Hewlett-Packard inkjet print heads, or similar foundry revenue from Texas Instruments for Lexmark inkjet print heads.

Foremost among all the players were the four companies at the top, each with revenue ranging from $675 million to $800 million, and collectively well ahead of the rest of the pack.

Bosch vs. STMicroelectronics

Bosch, the No. 3 entity in 2011, enjoyed a MEMS revenue boost of 8 percent last year including a nearly 5 percent uptick in its primary automotive MEMS business, which accounted for 82 percent of overall Bosch MEMS takings. Bosch is unchallenged as the top automotive MEMS supplier with 27 percent share of the market. The company also has a growing consumer and mobile MEMS trade—up 17 percent for the year—thanks to the soaring sales of pressure sensors in

handsets, compensating for slightly down revenues in accelerometers and microphones. But while the company did well in 2012, its result was impacted by an unfavorable exchange currency rate, especially in its U.S. automotive business.

STMicroelectronics, the No. 4 player in 2011, counted on a robust consumer and mobile business as its main source of MEMS revenue. While rival Bosch dominates automotive, STM leads in consumer and mobile MEMS with 32 percent of the market. STM also made inroads into automotive with $15 million in 2012, up from $10 million the year earlier. Gyroscopes were ahead of accelerometers in contributing to STM's cache, and similar to Bosch, pressure sensors for handsets boomed because of shipments into smartphones like the Samsung Galaxy S III.

Texas Instruments tumbles from the top

Falling out of the No. 1 spot was Texas Instruments, down to No. 3, with revenue down 3 percent to $751 million. While front projectors for business and education still formed the majority of its digital light processing (DLP) chip revenue, the segment was flat last year. In particular, DLP revenue in home theater and rear-projection TVs was down, especially with the exit of Mitsubishi as the last remaining rear-projection TV brand in North America. DLP revenue for pico-projectors also has not taken off as expected, with the chipset still too expensive and its adoption slow in the consumer and mobile markets.

At the No. 4 spot was Hewlett-Packard with revenue of $677

Continued on page 11

Globalfoundries *Continued from page 6*

12.1 and provides efficient access to the tool's productivity benefits for physical design with real-time, color-aware layout. Circuit designers can assign "same net" constraints in the schematic, and the layout designers can meet these requirements as they create the physical view.

The AMS flow provides detailed information on parasitic extraction and layout dependent effects, both of which introduce new challenges at 20nm and 14nm. For parasitic extraction, the flows are described in detail and customizable scripts and examples demonstrate OA and DSPF back annotation. In addition the flows illustrate methodologies to predict layout-dependent effects during schematic design and methods to include full models in post layout extraction. PEX flows for Synopsys StarRC extraction, Cadence QRC and Mentor CalibrexRC are supported.

Sign-off ready RTL2GDSII flows that address double patterning

GLOBALFOUNDRIES is also making available new flows that support a complete RTL-to-GDSII design methodology for targeting its 20nm and 14nm manufacturing processes. The company worked with EDA vendors to certify the flows in their respective environments and provide a platform for optimized, technology-aware methodologies that take full advantage of the performance, power and area benefits of the processes.

The result is a set of fully executable flows containing all the scripts and template files required to develop an efficient methodology. The flows serve as a reference to validate the correctness of the accompanying PDK as well as the vendor tool setup. In addition the flows offer access to other critical and useful information, such as methodology tutorial papers; guidelines and methodologies for decomposition of double patterned layouts; PEX/STA methodology recommendations and scripts; and design guidelines and margin recommendations.

A critical aspect of manufacturing at this level is the use of double patterning, an increasingly necessary technique in the lithographic process at advanced nodes. Double patterning extends the ability to use current optical lithography systems and the GLOBALFOUNDRIES flows provide comprehensive double pattern design guidelines. They address design for double patterning and the added flow steps for different design styles and scenarios.

Synopsys and GLOBALFOUNDRIES worked together to minimize the impact of changes associated with the 3D nature of finFET devices as compared to planar transistors. The two companies focused on making finFET adoption transparent to the design team. The collaboration on Synopsys' RTL to GDSII flow includes 3-D parasitic extraction with the Synopsys StarRC tool, SPICE modeling with the Synopsys HSPICE product, routing rules development with the Synopsys IC Compiler tool and static timing analysis with the Synopsys PrimeTime tool.

Cadence contributed a complete RTL-GDSII flow, including physical synthesis, and planning and routing developed with the Encounter Digital Implementation (EDI) System foundation flow. The seamless implementation flow, using Cadence Encounter RTL Compiler and EDI System, supports double patterning and advanced 20 and 14nm routing rules.

Mentor's Olympus-SoC place and route system is supported in the flow, providing support for new DRC, double patterning, and DFM rules. The Olympus-SoC router has its own native coloring engine along with verification and conflict resolution engines that detect and automatically fix double patterning violations. Expanded features include DP-aware pattern matching, coloring aware pin access, pre-coloring of critical nets, and DP aware placement. The Calibre InRoute product allows Olympus-SoC customers to natively invoke Calibre signoff engines during design for efficient and faster manufacturing closure.

Double patterning also impacts LVS and other DRC issues, and the flows provide methodology details to address these areas, including hierarchical decomposition to reduce data base explosion. Parasitic extraction methodologies and scripts are provided as well, offering ways to address double patterning-induced variations via DPT corners or with maskshift PEX features. ◆

MEMS Supplier *Continued from page 9*

million. HP also suffered a drop in ranking, down from No. 2 in 2011, as revenue associated with its inkjet printer heads contracted 10 percent last year. This follows a 15 percent decline in the shipment of inkjet printers. Moreover, HP's revenue from the replacement of disposable print heads has been shrinking continually as the company long ago started to move to printers with permanent print heads.

Rounding out the Top 5 but at a relatively far remove from the four other companies above it was Canon of Japan, with revenue of $377 million.

InvenSense on the rise

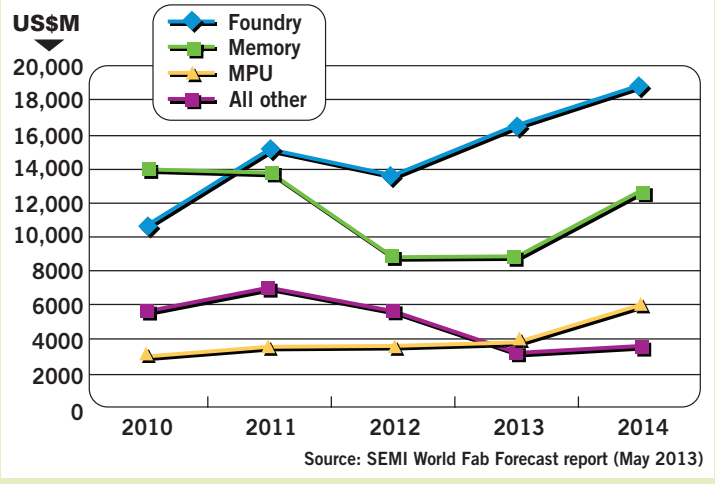
In all, revenue for companies from the succeeding sixth spot all the way to No. 15 each had takings between $100 million to just under $300 million.

Worth noting outside of the Top 5 was California-based InvenSense at No. 13, with revenue up 30 percent to $186 million. InvenSense is the most successful MEMS startup ever, its market breakthrough coming in 2009 thanks to its design in the Nintendo Wii Motion Plus gaming accessory. While InvenSense initially had been heavily dependent on gaming, the company wisely diversified its business and now looks to handsets and tablets as even more important sources of revenue.

InvenSense has also pioneered serial production of 6-axis inertial measurement unit comprising accelerometers and gyroscopes in a 4 x 4-millimeter package. Combo sensors last year accounted for half of the company's revenue, and InvenSense is now producing a very small 9-axis inertial measurement unit also containing a 3-axis magnetometer that measures only 3 x 3 millimeters.

Fab equipment spending: 23% growth in 2014

Fab equipment spending will grow two percent year-over-year (US$ 32.5 billion) for 2013 and about 23 to 27 percent in 2014 ($41 billion), according to the May edition of the SEMI World Fab Forecast. Fab construction spending, which can be a strong indicator for future equipment spending, is expected to grow 6.5 percent ($6.6 billion) in 2013, followed by a decline of 18 percent ($5.4 billion) in 2014. The new World Fab Forecast report covers fab information on over 1,140 facilities, including such details as capacities, technology nodes, product types,and spending for construction and equipment for any cleanroom wafer facility by quarter.



Source: SEMI World Fab Forecast report (May 2013)

Fab equipment spending for the second half of 2013 is expected to be much stronger with a 32 percent growth rate or $18.5 billion compared to the first half of 2013. The equipment spending increase in the second half is attributed to growing semiconductor demand and improving average selling price for chips. 2014 is expected to have about 23 to 27 percent growth year-over-year (YoY) to reach about $41 billion, which would be an all-time record.

Looking at product types, the largest amounts of spending on fab equipment in 2013 will come from the foundry sector, which increases by about 21 percent. This is driven mainly by capex increases by TSMC. The memory sector is expected to have an increase of only one percent — after a 35 percent decline in the previous year. The MPU sector is expected to grow by about five percent. A double-digit increase in the Analog sector in 2013 will still translate into low absolute dollar amounts, compared to the other sectors.

Construction spending is a good indicator for more equipment spending. Fab construction spending in 2013 is expected to be almost 15 percent growth YoY ($6.6 billion) with 38 known construction projects. Top spenders for fab construction in 2013 are TSMC and Samsung, who plan to spend between $1.5 and $2 billion each, followed by Intel, GLOBALFOUNDRIES and UMC. The SEMI World Fab Forecast report reveals more detail.

2014 shows a decline of about 18 percent ($5.4 billion) in construction spending with only 21 construction projects expected to be on-going. These construction projects include large fabs; some are 450mm-ready.

Since the last fab database publication at the end February 2013 SEMI's worldwide dedicated analysis team has made 389 updates to 324 facilities (including Opto/LED fabs) in the database. The latest edition of the World Fab Forecast lists 1,144 facilities (including 310 Opto/LED facilities), with 61 facilities with various probabilities starting production this year and in the near future. Seventeen new facilities were added and 8 facilities were closed.

The SEMI World Fab Forecast uses a bottom-up approach methodology, providing high-level summaries and graphs; and in-depth analyses of capital expenditures, capacities, technology and products by fab. Additionally, the database provides forecasts for the next 18 months by quarter.

Inside ASET's Dream Chip

Dr. Phil Garrou, contributing editor

The International Symposium on Electronic Packaging was held in Osaka the week of April 10th with keynote speakers, Dr. Subramanian S. Iyer of IBM, Dr. Takeshi Uenoyama of Panasonic, and Dr. Urmi Ray of Qualcomm.

There were 180 papers and over 20 posters. In addition, the Japan ASET consortium, Taiwan and Korea held special sessions.

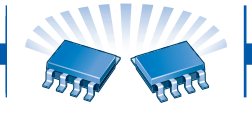
The ASET "Dream Chip" program recently ended in Japan. In the ASET special session, Sueoka and co-workers described their proposal for "High Precision Bonding for Fine Pitch Interconnection." Bonding fine pitch interconnect requires consideration of the factors which degrade the alignment accuracy such as thermal expansion of the machinery, and surface topologies of the chip an substrate.

They were able to bond 10μm pitch bumps. Using a flip chip bonder equipped with infrared alignment optics they found that they could observe alignment marks and adjust the chip position during the bonding process, even when the solder was molten. Most importantly they could eliminate the mis-alignment caused by joining non flat chips and due to thermal expansion of the tool head.

This dynamic alignment bonding scheme consists of 4 steps:

- pre-align for the approach of the chip to the substrate
- small gap align with IR light
- correct alignment for offsets caused by impact of the chip touching the substrate
- final align during the bonding while the solder is molten.

Packaging



Renesas and IBM Japan described "3D Package Assembly Development with the use of Dicing Tape Having NCF Layer". Dicing and stacking are important technologies in 3DIC assembly. Bumps on the wafer backside make it difficult for general dicing tape to achieve both high quality dicing and pickup. For tight pitch, small bump bonding it is also difficult to inject underfill into the narrow gap between the dies.

General dicing tape cannot bury the bumps and thus fully fix the die. This causes chipping and cracking of the die during dicing. If you increase the tapes thickness to fully bury the bumps, die pickup becomes difficult.

ASET studied a new ICF tape from Nitto Denko. The tape has a NCF layer (non-conductive film) on the dicing tape. Since this NCF layer ends up staying in the gap as underfill, they call this Inner chip film or ICF (just what we need more acronyms!) Hot lamination of the tape to the wafer will bury the backside bump. Wafer and NCF layer are diced together. The die pick up becomes easy since the required separation is between the ICF and the dicing tape adhesive.

Hozawa and ASET co-workers at ASET described their "3D Integration Technology using Hybrid Wafer Bonding and its Electrical Characteristics". In this study ASET examined 3D integration with vias last. Vias last was examined because it needs no modification of the front end process.

The process flow consists of: TSV formation; bump/contact ad formation; substrate thinning and stacking. They also examined W2W bonding and thinning after bonding as process flows.

Hybrid bonding was chosen where Cu-Cu and polymer – polymer bonding (they used PBO) occur at the same interface. Hybrid bonding provides both strong metal bonding and reliable polymer underfilling simultaneously.

In the full process sequence a silicon interposer wafer and the first device wafer are bonded F2F with hybrid bonding. After backside thinning the first device wafer, TSV formation and backside bumping the second device wafer is bonded to the stack B2F. Lastly the silicon interposer is thinned, TSV formed and bumps attached.

MEMS: After the prototype

David DiPaola,
contributing editor

After a functional A-sample prototype is built, it doesn't take long for a project to gain traction that has market pull.

This is usually the point that a project becomes highly visible within a company and it enters the Technology Development Process (TDP). The TDP is made up of multiple phases including concept, prototype, pilot and production with gates at the end of each phase. Design and process reviews are required at each gate but may also occur within a phase. These reviews are an open forum for communication of project progress and gaps towards technological, business and schedule milestones. Furthermore, the product is constantly evaluated against the market need and potential changes in market that may have occurred. The audience for the reviews at a gate include peers and management, who provide feedback on the project to date and collectively decide whether additional work is needed to complete the current phase or the completed work is sufficient to allow the project to proceed to the next phase with additional funding. In certain instances, a project that has not met all of the deliverables may be allowed to proceed to the next phase, but under strict conditions, that must be fulfilled within a given timeline. The goal of the TDP is to focus the team on high quality execution, effectively screen projects allowing only the best to proceed and hence accelerate successful innovation and profitability.

The MEMS Industry Group (MIG) Technology Development Process Template is an excellent tool for companies to use to implement the TDP within their organization (Marty et al. 2013). The goal of the TDP was to create a simplified frame work that could be easily customized to fit a company's needs. The TDP structure shown below is a slightly modified version of the TDP developed by MIG. In this version there are four major phases including concept, prototype, pilot and production with three major gates.

The concept phase is where ideas are generated and the initial A-samples are developed. It is also where the business case is first generated and the market need is defined. It is highly desirable to have market pull at this point. The prototype phase is where the design is developed in detail and B-samples are fabricated to support various levels of validation. The outcome of the prototype phase is to have design that can be manufactured in volume production. Towards the end of the prototype phase, production tooling is often released. The pilot phase is where production tooling is built and qualified. In addition, the product is made on production tooling (C-samples) and revalidated. It is important to note that there should be no change in the product design between the last revision in prototype and the first samples off the production tooling. The production phase is low to high volume production ramp. Often customers will require revalidation of products in production once a year for the life of the product.

At each gate, there is a design and process review for the project. In order for the team to be focused and efficient, there needs to be a clear set of deliverables defined for completion of each phase. These deliverables range from business and market definition to project technical details to production launch. This checklist provides an in-depth set of deliverables for the design reviews at each gate that can be tailored to the specific needs of an organization.

The Technology Development Process is an essential element of successful MEMS new product launches. The Design Review Checklist can also provide a frame work for discussion between management and engineers. With improved communication and efficient execution of technology development, the TDP is a great tool for accelerating innovation and profitable MEMS products.

MEMS

FD-SOI targets mobile applications

GIORGIO CESANA, *STMicroelectronics, Crolles, France and* **CARLOS MAZURE**, *Soitec, Bernin, France*

The FD-SOI technology platform is perfectly suited for mobile IC applications where power consumption has to be very low to maximize battery lifetime.

The IC industry has been innovative with the introduction of new materials and process modules like stressors, high-k and metal gates (HKMG). It has been very conservative in keeping the bulk planar transistor structure. As a result, the planar transistor has become a highly doped device with decreasing dimensions. Moreover, at these smaller dimensions, transistor characteristics suffer from statistical fluctuations like random dopant fluctuations (RDF) in the channel, which impair device matching in sub-100nm circuits. This has become an important problem beyond node 28/32nm limiting VDD reduction, thus limiting the reduction of both dynamic and standby power consumption.

There is strong consensus in the IC community that fully depleted (FD) transistors, also known as Ultra Thin Body (UTB) devices, are an effective solution for reducing the V_T variability caused by random dopant fluctuation (RDF). FD devices can be vertical, (FinFETs, 3D MOSFET) [1], or planar (FD-SOI) [2, 3]. Their key characteristic is that the silicon channel is undoped (**FIGURE 1**).

FD-SOI is an evolutionary innovation because it has the advantage of being a planar transistor structure that extends the applicability of bulk design flows with existing design and EDA tools. It is a non-disruptive MOSFET architecture change for SOC design and processing. FD-SOI requires ultra-thin Si (<20nm) over an ultra-thin buried oxide (BOX<25nm) for improved electrostatics [3]. FD technology brings numerous benefits for power reduction, area scaling and performance improvement while enabling a lower V_{DD} [3]. The IC SOC community has accepted that

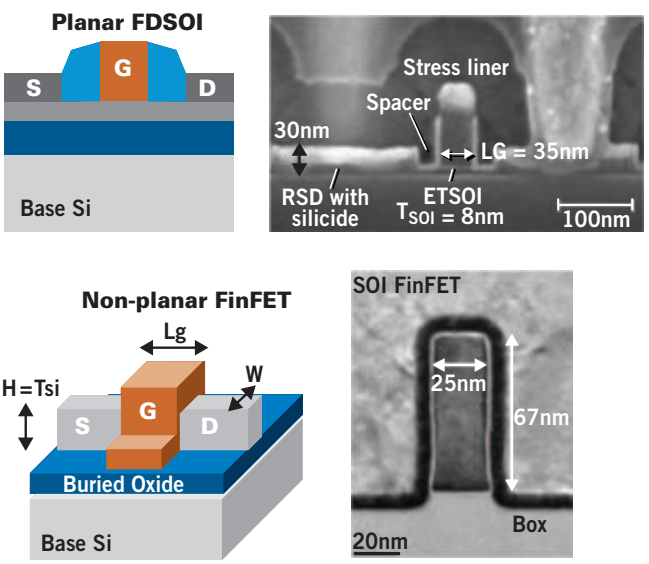


FIGURE 1. Examples of fully depleted devices: a) planar FD-SOI or ultra thin body UTB (TEM courtesy of IBM); b) 3D device FinFET (TEM courtesy of IMEC).

technology nodes beyond 20nm will have to use fully depleted (FD) MOSFETs.

Pushing performance, Intel introduced the 3D transistors, FinFET, first in 2011 for CPU applications [1]. The foundry world, in contrast, was able to scale conventional bulk CMOS technology from to 28nm to 20nm. The gain in density came with a higher price per unit area and little performance gain, however. Indeed, beyond the 28nm node, CMOS technology has become more complex with double patterning (node 20nm) and with 3D FinFET devices (node 14/16nm). The performance gain from node to node is well below the 30% boost we have

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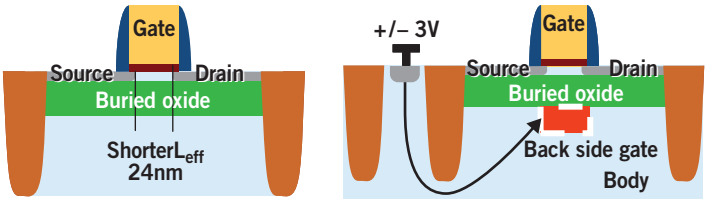

FIGURE 2. Schematic representation of the 28nm FD-SOI transistor. a) Cross-section of the FD-SOI MOSFET with the thin-layer channel on buried oxide; b) well contact used to apply back bias through the back gate underneath the buried oxide.

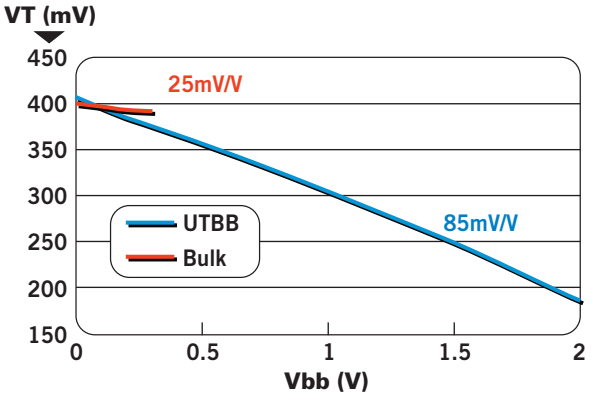

FIGURE 3A. VT variation as a function of applied back bias [4].

seen historically with scaling from a nodes n to the following n+1.

In this landscape, 28nm FD-SOI [4, 5] offers a very attractive value proposition: best low power at HKMG performance. In fact, 28nm FD-SOI gives the performance boost of scaling without changing the node. This is very interesting option for low-power ICs where area is not the driving factor and which could profit from a performance boost at constant or lower power consumption. Thus for many IC products moving to FD-SOI without changing the node can be very attractive from a power, performance and cost point of view. Only density-driven ICs need to rush to the next node. The offering of 28nm FD-SOI by foundries [6] will, without doubt, be interesting for numerous fabless companies having products in 28nm that could take advantage of a higher performance second generation 28nm technology without sacrificing low-power operation. Furthermore, low-power HKMG 28nm FD-SOI will also be very attractive 40nm IC products moving to 28nm.

FD-SOI technology

For bulk MOSFETs, the channel VT is tuned through channel and Halo doping, which is where RDF originates. In contrast, the FD-SOI channel is undoped,

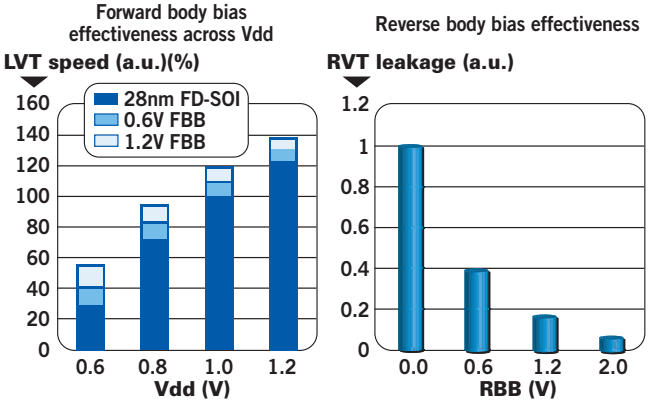

FIGURE 3B. Forward and Reverse Body Bias effectiveness for speed improvement and power saving.

significantly decreasing or eliminating RDF. The FD transistor VT is tuned through the gate work function and the back-bias voltage. Because of better electrostatics, FD-SOI transistors exhibit lower parasitics, which improves the transistor driving behavior. This is particularly advantageous at low VDD supplies. The better electrostatics also improve the short-channel effect as compared to the bulk 28nm version. This in turn enables a CMOS technology with shorter gate lengths (Lg=24nm), relaxing the integration constraints on the source and drain contact module.

FD-SOI in the ultra-thin body and buried oxide (UTBB) configuration [2, 3] offers the additional benefit of modulating the FD transistor characteristics by applying a back bias (**FIGURE 3a**). The FD-SOI transistor is, in principle, controlled by two gates: the actual transistor gate and the back plane, which acts as a second independent gate. Forward (FBB) and reverse back bias (RBB) circuit techniques have been used by many designers in earlier technology nodes but the range of biases were limited, on the one hand, by the source/drain to well diode forward-biasing, and, on the other hand, by the diminishing back biasing modulation of the bulk-transistor threshold voltages (VT) due to increasing channel doping levels. UTBB enables an extended back-biasing range of several VDD (-3V<VBB<+3V) and is a very powerful design tool for power management as well as for performance boosting, as illustrated in **FIGURE 3b**. Moreover, FD-SOI technology allows for dynamically adjusted threshold voltages.

Body bias requires a limited area overhead (2-3%), and can be restricted only to the IPs (i.e. CPU/GPU cores) that would benefit most from it to reduce the implementation effort and area overhead.

The 28nm FD-SOI process flow is a modified bulk 28nm HKMG LP process. It uses the same back end of the line andsame gate module. It is a simple incremental porting from bulk 28nm. Manufacturing even uses the

same tool set. Several process steps, specifically channel implants, halo implants and masking levels, are removed compared to the traditional 28nm bulk technology because of the undoped FD-SOI channel. There is less than a 20% change to the typical CMOS bulk flow [4, 6].

The extremely thin body and buried oxide layers makes it possible to etch them and to co-integrate SOI and bulk devices on the same SoC (**FIGURE 5a**). The ESD and I/O structures are kept in bulk for simplicity (**FIGURE 4b**). This is the hybrid integration with diodes and bipolars in bulk [2, 3, 4].

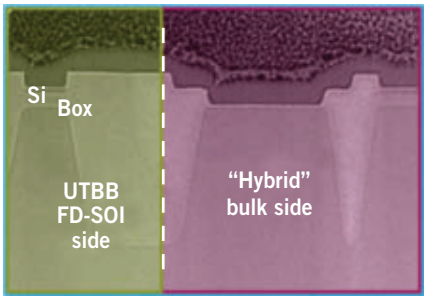

FIGURE 4A. SOI/bulk co-integration.

Device type	UTBB FD-SOI	Bulk
Logic	2Vt/PBO-16nm	
SRAM	✓	
Capacitance, Varactor	✓	
Drift MOS (OTP)		✓
Digital I/O	✓	
Analog MOS	✓	
RF MOS	✓	
Resistors	✓(Poly)	✓(Active)
Diodes (antenna)		✓
ESD devices	✓(FET)	✓ (FET, diode, SCR)
Vertical bipolar		✓

FIGURE 4B. Device partitioning of 28nm FD-SOI technology.

FD-SOI Substrates

FD-SOI technology builds on an SOI substrate with ultra-thin top Si (<12nm) and ultra-thin buried oxide (25nm) and with the utmost thin-layer uniformity of 6σ = ±0.5nm, all sites and all wafers [8].

Ultra-thin Silicon: The starting ultra-thin Si thickness has to be matched to the subsequent FD CMOS processing. Cleaning and sacrificial oxidations remove a few Si monolayers and this has to be considered when specifying the initial SOI thickness. The targeted Si channel thickness is typically between 5nm – 7nm [3, 7]. The SOI thickness (T_{Si}) has a direct effect on the MOSFET characteristics [5]. To take advantage of the improved electrostatic behavior of FD-SOI, the rule of thumb is L_G=1/3 T_{Si} (5) in the channel region.

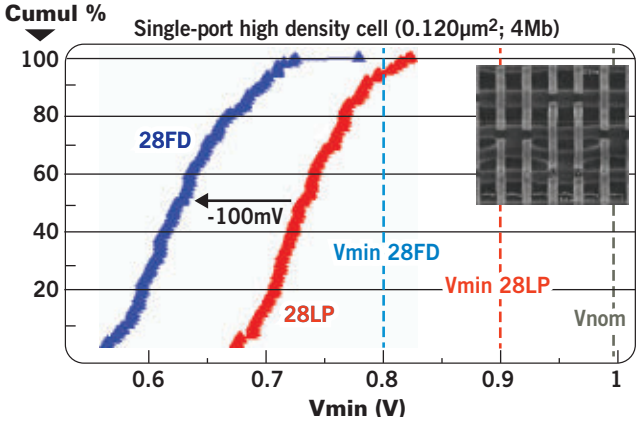

FIGURE 5. Comparison of 6T SRAMs for 28LP bulk vs. 28nm FD-SOI.

Thickness uniformity is the key parameter to control the V_T variation and short-channel effects (SCE) of the planar FD-SOI device. Typical uniformity requirements include on-wafer uniformity and wafer-to-wafer uniformity. Both of them combined are classified as layer total thickness variation (LTTV) and define the overall manufacturing process window for thickness uniformity. LTTV has to be achieved at the nanometer or sub-nanometer range for the SOI layer for all wafers and all sites in order to meet the FD specifications.

From circuit and device considerations, the maximum TSI fluctuation that can be tolerated is ±5Å within-wafer (WiW), total wafer range of the T_{Si} non uniformity, and wafer-to-wafer (WtW) T_{Si} reproducibility.

Ultra-thin BOX: The thin BOX (Buried Oxide) suppresses the lateral electrostatic coupling between source, drain and channel of the transistor through the thick BOX. Furthermore, the BOX thickness reduction improves the scalability of the FD-SOI device at almost constant channel silicon thickness down to L_G=10nm, which corresponds to the targeted gate length for the 10nm node. An ultra-thin BOX (UTBOX) enables the use of a back bias and a forward bias to adjust the transistor characteristics like current drive (Ion), off leakage (Ioff) and V_T within an extended VBB voltage range [9].

The BOX thickness T_{BOX} and silicon thickness T_{Si} are independent parameters for the SOI fabrication and can therefore be adjusted without degrading the properties of the top silicon layer. The oxide quality of ultra-thin BOX is very similar to the quality of equivalent gate oxides.

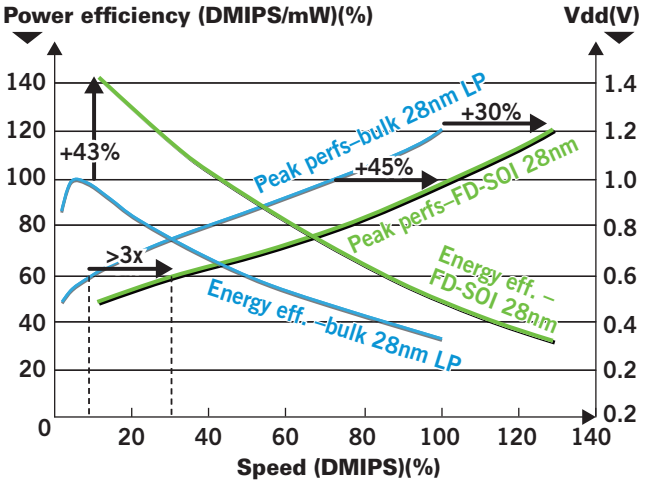

FIGURE 6. Best in class in core efficiency for 28nm FD-SOI vs. 28LP bulk.

FD-SOI Design

We use standard commercial EDA flow to design both bulk and FD-SOI. Design migration from Bulk to FD-SOI EDA flow is straightforward. The interconnects and routing are identical. FD-SOI devices behave very much like bulk transistors because there is no history effect and no floating-body effect, if T_{Si} is sufficiently thin (<10nm). Logic and memory design and architecture are also similar to bulk.

The differences between FD-SOI and bulk are related to process and devices, and include, SPICE models, integration of ESD and analog devices, and application of back-bias schemes.

FD-SOI standard and custom cells can be duplicated or ported from existing bulk cells. Re-characterization is required due to a different SPICE model: Input capacitance, timing, leakage and dynamic power data in library files will change. Timing analysis needs to be rerun to check that there are no setup/hold violations in case of direct porting. Porting bulk designs to FD-SOI is as simple as porting to an updated bulk design [10, 11, 13, 14].

The device models are validated on FD-SOI hardware and available with EDA tools. Compact device models [11, 12] are production ready.

Circuit Results

SRAM Robustness: The lowest AV_T values are achieved with FD-SOI [3, 9] due to the undoped channel and consequently the strong RDF reduction. Thus, lower V_{DD} operation is enabled for minimum SRAM cell size as compared to its bulk equivalent. The FD-SOI cell has a better read stability and write ability with respect to the bulk cell. The typical bulk countermeasures of increasing V_{DD}, or increasing the channel length and width to compensate for the V_T variability are no longer necessary. At the same cell size, FD-SOI makes it possible to gain 100mV to 200mV in Vmin compared to the bulk cell [4]. The operation regime at V_{DD}<0.8V is very attractive for mobile hand-held applications.

Circuit Performance: FD-SOI technology is particularly suited for high speed at low-voltage operation, reducing signifantly the power consumption (~V_{DD}^2). **FIGURE 6** illustrates two potential optimization paths: significantly more performance at the same power or a dramatic reduction of power consumption at the same performance.

FIGURE 7 shows the advantages of FD-SOI for different VDD voltages. At 0.6V, FD-SOI is already capable of delivering 550MHz, >3x the performance

of an equivalent 28LP technology implementation, without requiring any Forward Body Bias (FBB). Using Forward Body Bias, it is possible to reach 1GHz operation with a 0.6V source.

FD-SOI can also deliver the same performance as bulk while running at a lower operating voltage. As highlighted in Fig. 7, we have achieved the same performance in 28nm FD-SOI as 28LP while running with 200mV lower supply, and an even further saving of 200mV is possible when applying Forward Body Bias. This impressive reduction of 400mV on the supply voltage immediately translates into huge dynamic power savings.

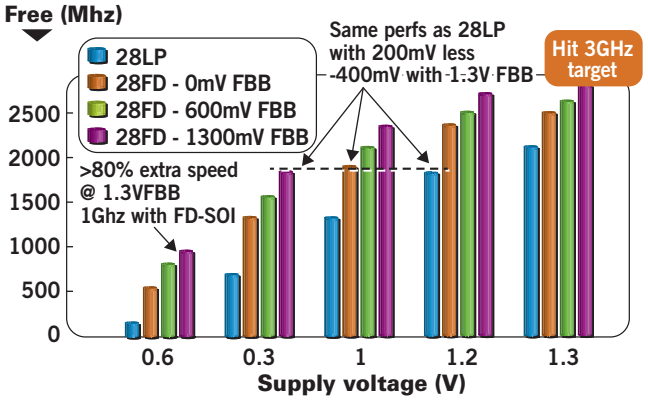

FIGURE 7. FD-SOI enables high speed at lower VDD. Example of ARM A9 core. Si data.

In overdrive conditions, by boosting performance with FBB, we have demonstrated 3GHz operation [13], overtaking what has been obtained to date with the A9 architecture.

Conclusion

The FD-SOI technology targets fast performance at low voltage V_{DD} and is an ideal technology to reduce the energy gap between battery energy supply and smart handheld system energy needs, so it runs cool. The industrial ecosystem is in place for the substrate supply, technology platform and design infrastructure. The FD-SOI technology platform is perfectly suited for mobile IC applications where the power consumption has to be very low to maximize battery lifetime. Furthermore, with its simplicity, FD-SOI is an evolutionary step from bulk towards fully depleted design because it maintains the planar device structure.

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Effects of measured spectral range on accuracy and repeatability of OCD analysis

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A broadband polarized reflectometry measurement, utilizing RCWA analysis, can be used to obtain detailed trench profile results.

There is a need for metrology to help control manufacturing processes for power semiconductors, where deviations from the desired structure geometry can affect device performance. Lithography and etch processes, specifically, create patterned structures, where the trench depth and width, or CD (critical dimension), must be tightly controlled. Traditionally, several techniques have been employed for this purpose, including cross-section Scanning Electron Microscopy (SEM), CD-SEM, profilometry, and Atomic Force Microscopy (AFM). Each method has its benefits and limitations, but none can provide detailed profile information with the combination of speed and measurement sensitivity of non-destructive optical metrology, based on broadband polarized reflectometry.

To demonstrate the capabilities of broadband polarized reflectometry, we performed measurements on power semiconductor samples using an optical metrology instrument, the n&k Olympian. One key aspect of this system is the relatively large wavelength range, extending from deep ultraviolet to near infrared wavelengths (190nm - 1000nm). This large range enables applications that would not be possible with the limited range of standard reflectometers (375nm - 750nm).

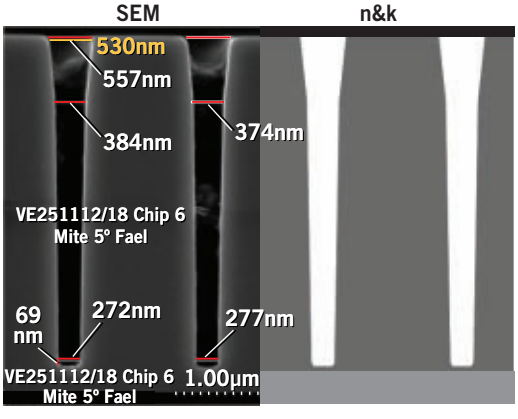

FIGURE 1: Cross-section SEM image of the tapered trench (left) and model of the trench structure within n&k analysis software (right). The model was created to be consistent with the trench profile seen in SEM images.

Measurement system

The n&k Olympian is a fully-automated metrology system for thin film and optical critical dimension (OCD or "scatterometry") measurements that uses broadband polarized reflectance. The data extends from the UV to NIR, with a separate optical system covering IR wavelengths up to 15,000nm. The measurement method is non-contact, non-destructive and high throughput, with typical measurement times (including the move, acquire, measure, and analyze steps) on the order of 5s per measurement point.

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For the UV-NIR wavelength range, there are two light sources. UV light comes from a deuterium arc lamp, while visible and near-IR radiation is provided by a tungsten filament lamp. The source light is focused on the sample and directed to a spectrophotometer by a series of mirrors, creating a measurement spot diameter of 50µm and incident angle of 4º from normal. The spectrophotometer contains a holographic diffraction grating and a photodiode array that separates the polychromatic beam into its individual wavelength components and records the reflectance at each wavelength, in one nanometer intervals. There is a rotating polarizer in the optical path enabling the collection of two sets of measurement data (S-polarized Reflectance and P-polarized Reflectance, or "Rs" and "Rp" respectively). When line/space grating structures are measured, the structures are oriented such that Rs data relates to the TE polarization and Rp data relates to the TM polarization.

To extract values for structure dimensions, a model of the measured area is created using n&k Analysis software. The software incorporates rigorously coupled wave analysis (RCWA) for periodic structures1 with Forouhi-Bloomer dispersion relations2, 3 for n and k. The model is used to calculate theoretical reflectance spectra. The structure dimension parameters, within the model, are varied using nonlinear regression analysis in order to obtain the best match between the experimental and calculated spectra. Inputs to an OCD structure model include the optical properties for all materials within the structure, which can be determined by measuring blanket film areas, and the structure pitch.

The measurement results are determined by converging on the maximum goodness of fit (GOF) value, which describes the similarity of the calculated reflectance of a modeled profile to the experimental reflectance. The variables within the model, including CD and depth, are reported as measurement results after the software determines that the GOF cannot be further improved by changing any of the values. A higher goodness of fit value generally means that the measurement results are consistent with the physical dimensions of the actual structure. If there is variation in neighboring features within the 50µm diameter measurement area, the results are considered to be the average dimensions.

To provide measurement results with this tool and technique, the area of interest must meet certain requirements. Typically, the measurement area is either the device structures, or within designed test areas meant to approximate the features found within the actual device. OCD test structures, including 2D line/space gratings or 3D hole arrays, must be repeated periodically, with a pitch less than 10µm.

Tapered trench measurement

To test the measurement capabilities of the n&k Olympian, Infineon Technologies created five silicon wafer test samples with line/space grating structures. Each sample was created using different process conditions, meant to represent possible unintended changes in the manufacturing process that could lead to differences in the dimensions of the grating structures, ultimately affecting the device performance. The samples were measured using both the n&k system and a cross section SEM, for comparison and determination of the approximate trench profile.

As shown in **FIGURE 1**, the tapered line/space grating structures have repeating spaces etched into silicon with a pitch of 1.7µm, nominal trench depth of 4µm, and space CD of 0.55µm. The pitch is based on the design layout and will not be affected by changes in the etch processing, so pitch is fixed within the analysis model. Trench depth and space CD are the parameters of interest that need to be measured. There were no materials besides silicon in the test

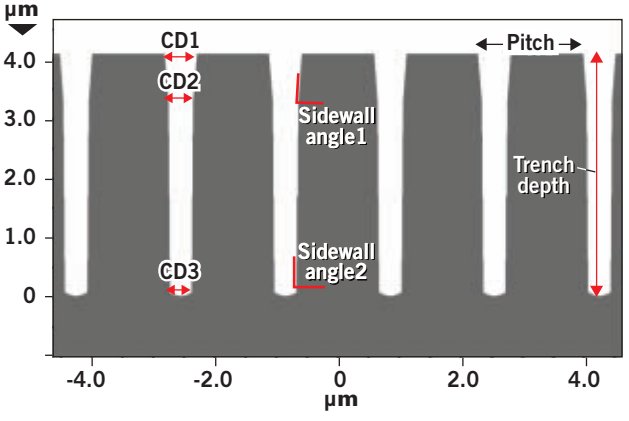

FIGURE 2: Cross-section view of the OCD model, drawn to scale. Pitch is fixed within the model, while CD1, CD2, CD3, and trench depth are measurement parameters. Sidewall angle values can be calculated from the results for CD and depth.

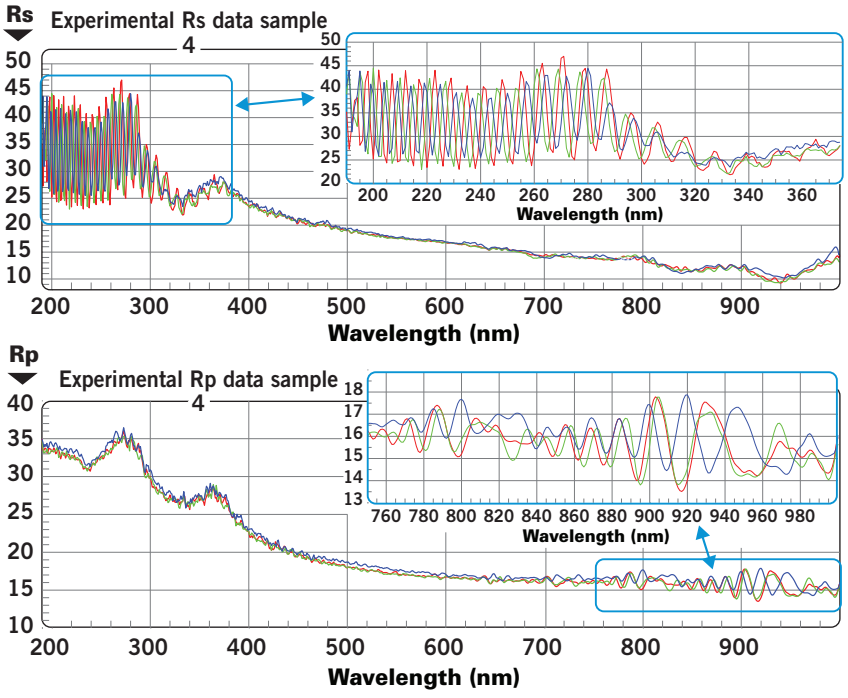

FIGURE 3: Experimental Rs and Rp Data for Sample 4, at 3 locations across the wafer. The data shows the areas of the spectra that are critical in distinguishing changes in trench depth and CD. The three locations appear to have differences in terms of experimental data, which relate to trench depth and CD, particularly from 190-350nm in Rs data and 800-1000nm in Rp data. A standard reflectometer with wavelength range of 375-750nm does not include data in the critical regions where there is good sensitivity to the trench depth and CD values, so measurement results using this limited wavelength range will be unreliable for Sample 4.

structures, but oxides, nitrides, and poly-silicon are often a part of OCD structures, and the analysis software allows for the inclusion of multiple layers on the trench mesa (above silicon lines), at the bottom of the trench, or on the trench sidewall.

A review of the cross-section SEM image for the grating structure (Fig. 1) shows the trench profile for one of the samples with two distinct sections. From the top of the trench until a depth of ~800nm there was a fairly constant sidewall angle, while from the depth of ~800nm to the bottom the trench sidewall angle changes to be closer to normal. Subsequent SEM images show that this inflection point is consistently near a depth of 800nm from the top of the trench. These observations of the trench profile were used to develop the analysis model for the n&k Olympian. Neither an AFM nor a CD-SEM would be able to measure CD at the inflection point as well as at the top and bottom of the trench.

Based on the trench profile from cross-section SEM images, the analysis model was created to include space CD variables at three

points (**FIGURE 2**): CD1 at the top, CD2 at 800nm from the top, and CD3 at 70nm from the trench bottom (to allow for some rounding at the trench bottom). There is good match between the SEM image and the schematic from the analysis software.

Each wafer was measured at 29 points using the n&k Olympian, while cross-section SEM images were taken at the center point for each sample. For the optical measurements, we considered two cases: 1) using the full wavelength range of the broadband polarized reflectometer (190nm - 1000nm), and 2) using a limited range typical of standard reflectometers (375nm - 750nm). This comparison was done to demonstrate the advantages of using a larger wavelength range, for this application. Other than the wavelength range, the modeling was identical for both cases.

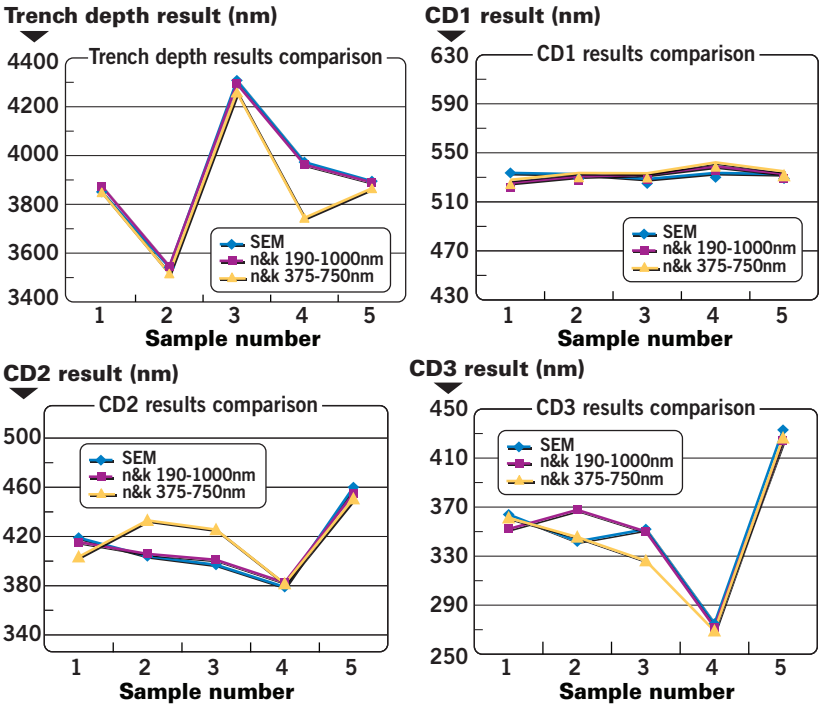

FIGURE 4: Comparison of n&k results, both limited range (350nm - 750nm) and broadband (190nm - 1000nm), to cross section SEM results for Trench Depth (upper left), CD1 (upper right), CD2 (lower left) and CD3 (lower right). For CD1 and CD3, the results match SEM results equally well for the full and limited wavelength range. For Trench Depth and CD2, the results from analysis of the full wavelength range have good agreement with the SEM results, while results from the limited wavelength range do not match as well. Sample 4 results were expected to be inaccurate for the limited wavelength range, and the trench depth for Sample 4 does not match the SEM result.

Experimental Data

Without any data analysis, observations of the experimental data, Rs and Rp, can provide insight into the measurement sensitivity to the structure depth and CD values. Looking at the experimental data, we clearly see oscillations in the Rs data from 190nm - 450nm, and in the Rp data from 800-1000nm. For Sample 4, the oscillations in the Rs data have a limited wavelength range and only extend from 190nm – 350nm, as shown in **FIGURE 3**.

To further test measurement sensitivity, we can create an analysis model using the nominal structural dimensions. We calculate the theoretical polarized reflectance for the nominal structure and compare this to the experimental data. By changing the parameter values for depth and CD within the model and recalculating the theoretical reflectance, we can observe the effects of changing depth or CD on the reflectance spectra. Overall, the simulations confirm that reflectance measurements of the 190nm - 450nm and 800nm - 1000nm ranges are important to measurement of the trench profile.

The calculations also confirm that decreasing the CD values limits the wavelength range in the Rs and Rp data where there is sensitivity to the depth and CD values. This is consistent with the experimental data that is measured for Sample 4, which has smaller CD values and exhibits sensitivity to the trench depth and CD values only from 190nm – 350nm in the Rs data and 800nm – 1000nm in the Rp data. This suggests that a standard reflectometer, with wavelength range of 375nm – 750nm, will have limited measurement capabilities for this type of trench structure, particularly when the CD values are smaller.

SEM Comparison

In order to verify the results from the optical measurement system, we compared results from SEM cross-sections for CD and depth to the values obtained

by the n&k Olympian. Using the full wavelength range, 190nm–1000nm, there is a good match between cross-section SEM results for depth and CD and the measured results from the broadband polarized reflectometer (**FIGURE 4**). Using a limited wavelength range, 375nm–750nm, with an analysis model that is otherwise identical, the results do not compare as well with the SEM data, particularly the trench depth of Sample 4.

The reason that Sample 4 measurements are inaccurate for trench depth, using the limited wavelength range, is related to the CD values. For Sample 4, the CD3 value measured by cross-section SEM is ~275nm, significantly lower than any of the other samples. For deep trenches in silicon, as the CD gets smaller the OCD interference fringes are reduced at longer wavelengths. Experimental data in the UV region is required for measurement of this structure, as shown by the broadband data.

In order to further test the measurement limitations, we performed simulations using the full wavelength range to see the effects of smaller CD values on the Rs spectra. As CD2 and CD3 get smaller, the amplitude of interference fringes decreases and the wavelength region is narrowed. With CD2 equal to 400nm and CD3 equal to 350nm, interference fringes are present from 190nm - 420nm. However, with CD2 equal to 300nm and CD3 equal to 200nm, interference fringes are only present from 190nm - 280nm. Therefore, as the CD values become smaller the system must include UV wavelengths in order to measure the trench depth and CD.

Wafer Uniformity

One advantage of an optical measurement system is the ease with which wafer uniformity maps can be created. While the cross-section SEM can show a detailed trench profile, it is both destructive and time consuming. With the broadband polarized reflectometer, however, wafer uniformity maps can be created in a few minutes, depending on the number of locations measured.

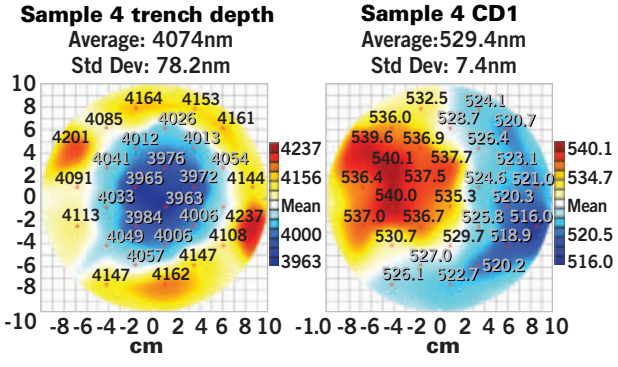

FIGURE 5: 29 Point Wafer Uniformity Results for Sample 4, 200mm wafer, as measured by broadband OCD. Dense mapping measurements are used to test the non-uniformity for depth and CD. Cross section SEM is typically done at a single point or a few points per wafer, so uniformity information is limited. The trench depth mapping shows a typical uniformity pattern after an etch process, with a center to edge effect, while CD1 is larger on the left side of the wafer, smaller on the right.

FIGURE 5 shows the wafer uniformity results for Sample 4 using the full wavelength range analysis (190nm

Continued on page 38

Innovative automation approaches for 450mm factories

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New approaches can help improve cycle time and achieve higher purity inter-process wafer environmental control.

Automation adds significant value by addressing key issues of cycle time, process variability and contamination. This is true for 300mm manufacturing and will be even more critical to enable the transition to 450mm manufacturing. It is important to look at some of the issues facing the industry right now to understand the impact and benefits that fab automation will enable for the future. Current cycle times are unacceptable at 300mm, hindering the full utilization of assets and dulling market responsiveness. As manufacturers transition to sub-20nm process nodes, the queue time between certain process steps becomes more sensitive to variability and more difficult to support with current AMHS architectures. For example, between etch and post-etch clean the timing must be carefully controlled because exposure to moisture and oxygen immediately begins to destroy critical dimensions of features on the wafer surface.

As the industry progresses to smaller process nodes lithography requirements are driving the need for multiple patterning. This doubles or quadruples the number of process steps per mask layer, further extending factory cycle time. In addition, processing larger substrates will likely require longer process times. An increase is most likely in tools like lithography, implant and some metrology steps where process times are based on the area of the wafer. As a result, the first wafer processed in a 450mm batch will wait longer while the remaining 24 wafers in the lot complete processing. After all 25 wafers are returned to the original front opening unified pod (FOUP) the entire lot must wait for AMHS transport to the next process step. The total queue time is too long, with unacceptable variation lot-to-lot and between the first and last wafer processed.

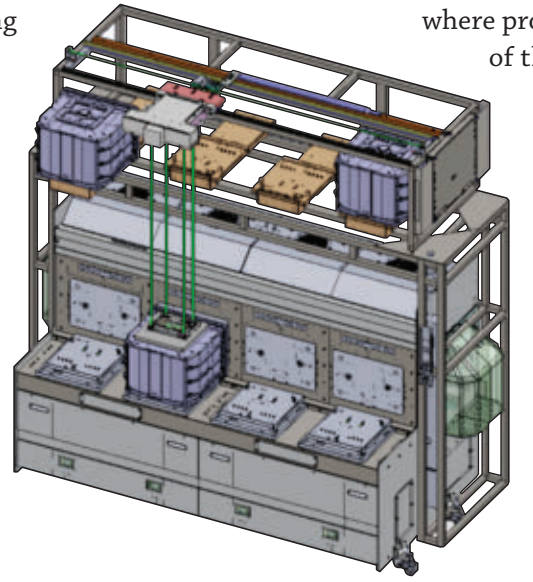

FIGURE 1. 450mm sorter/EFEM with integrated tool buffer and nitrogen purge.

Shorter cycle time and tighter inter-step timing control are possible through innovative automation approaches. An architecture that enables wafers to be protected from oxygen and moisture between process steps will reduce the dependency on critical process timing and can positively impact yield. In the early 1990's

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standard mechanical interface (SMIF) systems enabled a tighter level of environmental control by reducing the controlled volume of clean air or nitrogen and isolating clean 'zones' with mini-environments. At 450mm, similar techniques of reduced volume can enable creation of a safe and economical wafer environment to protect wafers from particulate contamination as well as moisture, oxygen, and any other contaminate that is potentially harmful to a given process. As was the case with SMIF, an end-to-end solution will be needed such that the wafers are never exposed to an environment that exceeds the maximum allowable exposure limit of contaminants. The solution will again need to be modular to enable flexibility in fab layout, configuration and equipment choices.

Using smaller lot sizes offers tremendous advantages. In a 25 wafer batch, 24 wafers are waiting while one wafer is in the process chamber. Reducing the lot size shaves valuable minutes from this variability, and significantly reduces the overall cycle time. Many papers have shown that equipment utilization goes up and cycle time goes down as lot sizes are reduced. Unfortunately, conventional AMHS systems are not able to support small lot delivery time without bottlenecks, effectively blocking the benefits. A local tool buffer, such as shown in **FIGURE 1**, can help relieve AMHS bottlenecks delivering FOUPs thereby enabling smaller lot sizes. Localized tool buffers can increase equipment utilization by removing transport from the critical path. Integrated nitrogen purging capability widens the process window so that the next step can be executed within the allowable critical time period.

Delivery time variability caused by AMHS can directly impact process uniformity and yield. An approach which links equipment cells directly can reduce variability and remove the burden of high-priority delivery from the AMHS. The cell approach can use a combination of interconnected tool buffers, interconnected vacuum platforms and interconnected EFEMs to accomplish the required lot arrival time and consistency. Ideal interconnection solutions create a virtual cluster with balanced wafer throughputs while maintaining layout flexibility. A modular approach is needed to maintain full application flexibility.

An exciting building block for the cell approach is interconnected EFEMs that can pass wafers directly from one process chamber to the neighboring EFEM, and then into the successive process chamber. This direct wafer exchange does not require FOUP input/output and AMHS operations, thereby reducing critical transfer times and eliminating variability. In this scenario lots are distributed across multiple tools and must later be merged back to maintain FOUP integrity. As always, software must manage and control these wafer movements without misstep.

Interconnected vacuum platforms will connect individual cluster tools together in a manner similar to a common vacuum handler. Wafers

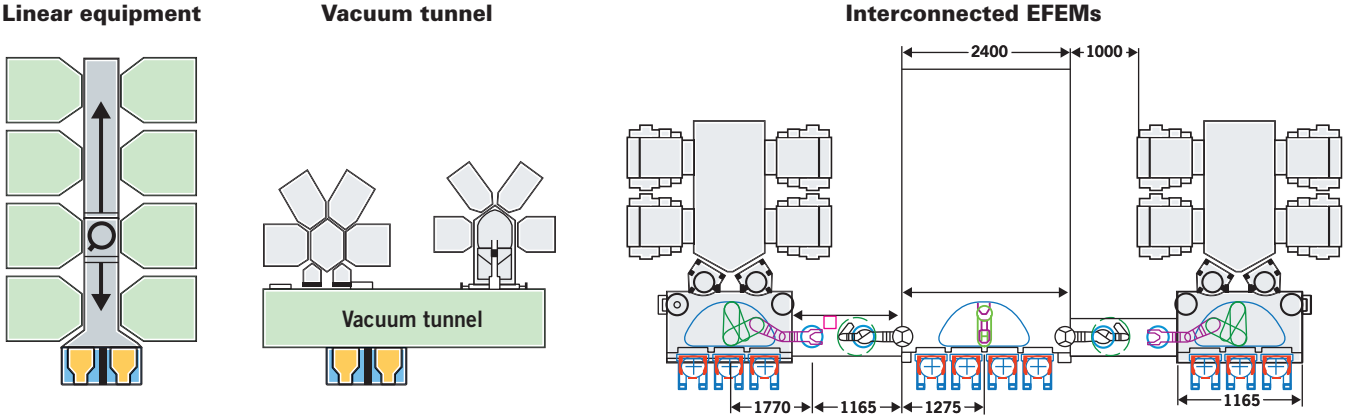

FIGURE 2. Interconnected vacuum platform.

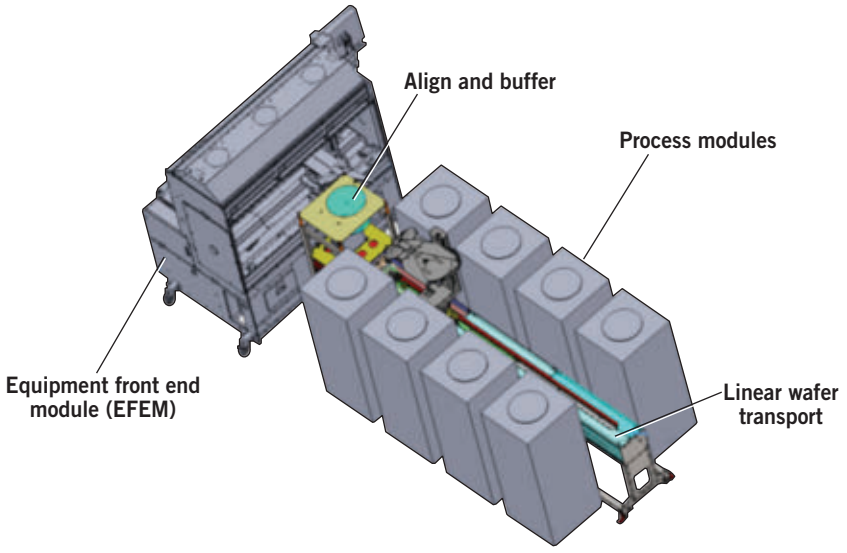

FIGURE 3. Linear tool architecture.

never have to leave the safety and purity of a vacuum environment between steps. A combination of these interconnectivity elements provides a flexible cell approach, an example of which is shown in **FIGURE 2.**

Linear tool architectures offer significant benefits, particularly if multiple equipment types can be integrated. In the atmospheric example shown in **FIGURE 3**, a traditional EFEM removes the wafers from the FOUP and transfers them inside the equipment. A linear robot transfers the wafers between process chambers arrayed in a linear configuration behind the EFEM. After some process steps are completed, the wafers are returned to the FOUP. If the cell is modeled as one tool with a complex recipe, no software modifications are required at the manufacturing execution system (MES) level.

Valuable time is lost in 300mm fabs searching for notches in wafers to assure correct rotational alignment relative to crystallographic orientation and to find the laser-scribed wafer ID. Notches are mechanical modifications to the wafer that can impact the ability of the wafer to withstand shock without breakage. One alternative method could involve laser scribing of an alignment mark at the center of the wafer, either top or bottom side. This would allow handling systems to immediately locate the fiducial mark and take action before handling the wafer, thereby saving time and improving wafer yield.

Beyond the front end, assembly and test will also benefit from more automation in the 450mm wafer generation as the back end adds increasing value. Already, requirements for cleanliness, repeatability and error free handling are driving the need for increased automation. It makes sense to leverage the successes of 300mm front end automation to improve the operations of back end fabs. While the technologies will need to be adapted to the unique needs of back end customers, the lessons learned in 300mm automation are significant and should not be lost.

Automation at 450mm is different from previous generations because advanced processes are very sensitive to the environment around the wafers. This pushes automation equipment into the realm of process control. Space constraints in 450mm factories are requiring equipment manufacturers to be creative in developing solutions that provide more output with less space. Automation providers must therefore also be key collaborators in optimizing equipment footprint. The weight and size of 450mm wafer carriers means that automated movement is essential. The overhead involved in moving and storing 450mm FOUPs will be large enough that running small lots in 450mm FOUPs will challenge fab economics. Flexible cell level automation such as presented in this paper may be needed to address these challenges.

In conclusion, innovative automation approaches will be required to fully realize the promise of increased efficiency and reduced costs in the 450mm generation. Because the semiconductor production process is complex and requires a high level of flexibility, no single approach will serve all fabs or all equipment within the fab. A flexible building block approach must be explored to enable each fab to optimize its facility for its unique production requirements.

Paradigm changes in 3D-IC manufacturing

THORSTEN MATTHIAS *and* **PAUL LINDNER**, *EV Group, St. Florian, Austria*

The process flows applied today for real product manufacturing are quite different from the process flows initially proposed for a universal 3D IC.

Successful 3D-IC prototypes have been demonstrated for many different devices. However, while for some applications 3D-IC architectures have been smoothly integrated into products despite their technical complexity and the omnipresent cost pressure, for other products there seems to be a long list of issues (cost, yield, thermal issues, lack of standards, lack of design tools, etc.) that prevents adoption of 3D-IC integration in the near future.

Common wisdom is that a technical innovation is first introduced for high-performance, high-margin applications, for which the performance gain can bear the additional cost. As the technology becomes more mature, costs are reduced and an increasing number of applications adopt the new technology. A good example of this in the semiconductor industry is flip chip bumping. However, if we look at 3D ICs the situation is not so clear. While it is true that some "cost does not matter" applications in the science, military or medical field use 3D stacking, many high-end devices (most notably CPUs) do not yet use 3D stacking. However, some of the lowest-cost devices in our industry such as light emitting diodes (LEDs), micro-electro-

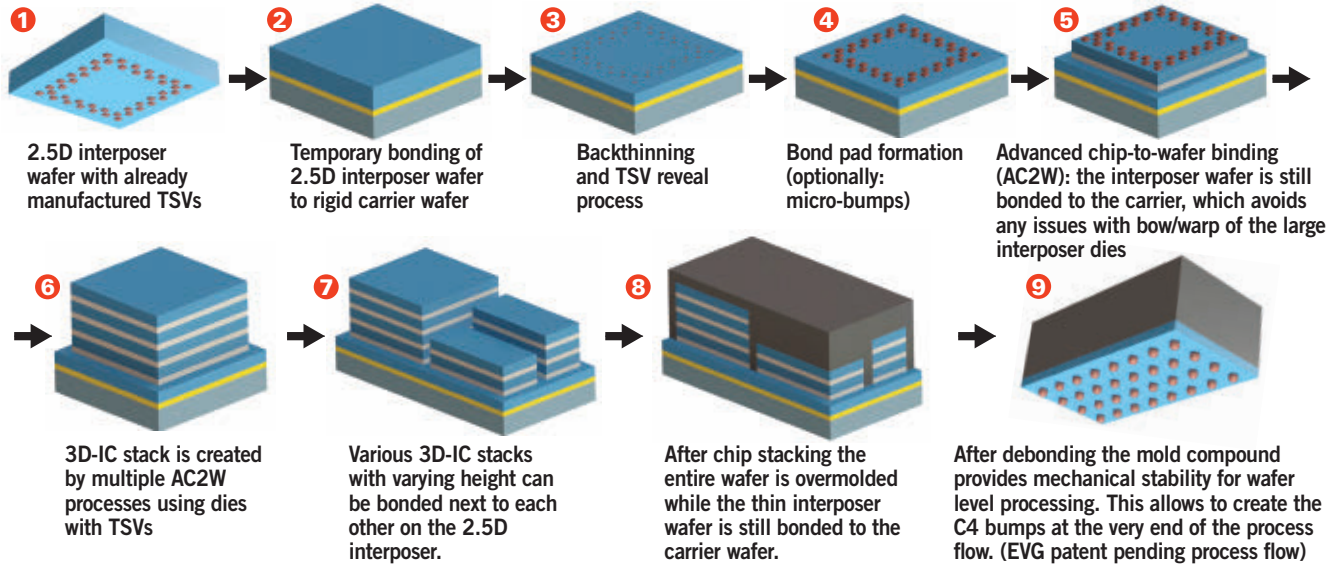

FIGURE 1. Exemplary process flow for 2.5D interposer with 3D-stacked chips (EVG patent pending) [2]

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mechanical systems (MEMS) and image sensors have successfully implemented 3D-IC technology.

Is the adoption of 3D-IC technology in high-volume, low-cost devices evidence of its technical maturity? In his famous book "The Innovator's Dilemma" Harvard Professor Clayton Christensen introduced the idea that any innovation and its potential for industrial adoption should be assessed in the context of their respective value networks [1]. The value network of a product (e.g. a CPU) is defined by the sales critical parameters (e.g. computing power, clock speed, on-chip cache memory and price) and by the expectations of the current customers about future requirements. Any innovation that improves the sales critical parameters within the current value network is defined as "sustainable innovation". Innovations that do not improve the sales critical parameters within the current value network are defined as "disruptive innovations". In his studies Prof. Christensen concluded that innovations cannot be introduced in value networks where they are considered "disruptive" no matter how technically mature, cheap or well established for other applications they are. However, in a different value network where the innovation is sustainable, the users can hone their skills and build expertise. If the expectations within one value network change, then innovations can be introduced very rapidly.

For example, for FPGAs the 2.5D interposer enables smaller die sizes, which allowed 28nm technology to be introduced at a reasonable wafer yield at an earlier point of time. The result of introducing interposers for FPGAs is that an FPGA with more and faster transistors can be manufactured earlier. Therefore, the 2.5D interposer for FPGAs is a sustainable innovation. For mainstream semiconductor devices like memory, Moore's Law is (or at least was until recently) a good proxy of the value network. If you put a TSV on a chip, you cannot put transistors onto the same area. TSVs reduce the number of transistors on the chip and increase the price per transistor.

Is 3D integration ready for volume production?

At first glance TSV and 3D IC are disruptive innovations. TSVs and die stacking have already been successfully implemented in high-volume manufacturing for CMOS image sensors, despite the fact that the combination of high technical complexity, immature technology, and low-cost/low-margin devices seems like a very unfavorable situation. From the pure technical point of view 3D-IC image sensors seem more challenging than other devices, such as stacked memory. The TSV density is higher, the TSV diameter is smaller, the pitch is smaller, the wafers are thinner and wafer-to-wafer stacking is necessary. However, the transition from front-side illuminated image sensors to backside illuminated image sensors as well as the current transition to 3D-stacked image sensors (where photodiodes and digital signal processing are manufactured on separate wafers) have resulted in technical improvements within the existing value network, including better resolution, smaller pixels, better signal-to-noise ratio, higher image processing speed and higher bandwidth.

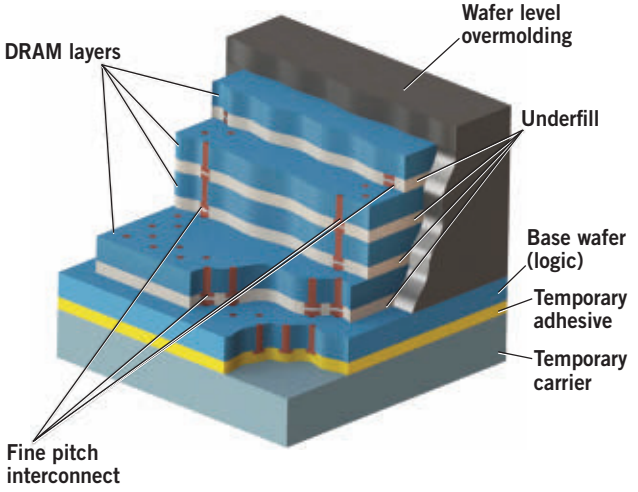

FIGURE 2. Overmolding prior to debonding is a key integration concept.

When engineers first looked at developing 3D IC technology, they did not design a 3D-IC device from the get go, but rather started with separate technical milestones. In most cases, the first milestone was to manufacture a daisy chain with 10, 1000 or 10000 TSVs. The focus was primarily on the unit processes for TSV manufacturing. The second milestone was to manufacture a thin die with TSVs and bumps on both sides, which might eventually be used in a real system. The paradigm for thin-wafer processing in early 3D/TSV development was that a tempo-

rarily bonded wafer had to withstand any kind of backside processes. Thus, flexibility and broad process windows were most important. In theory the idea to completely manufacture individual thin chips is very attractive as it enables known good die (KGD) manufacturing and fits into every possible integration scheme and business scenario. However, in practice this approach results in overly complex integration schemes, which are not optimal from a yield and cost perspective.

This paradigm changed when product groups began to adopt thin-wafer processing for specific products. Now the highest goal was to maximize profit on the product, and yield and cost of ownership were optimized for the entire process flow for chip and package—often abandoning previously considered universal one-size-fits-all solutions and resulting in completely new integration schemes. For example, whereas previous R&D efforts went into very thick films with the idea to embed C4 (flip chip) bumps, today's 3D-IC devices primarily apply bump-last process flows, which use very thin adhesive layers. This has the advantage of reduced cost, better film thickness control and higher yield as a result of avoiding bump damage caused by post-bump processing. Transitioning from very thick to thin films also reduces the duration of the baking steps for curing the films—enabling the design of temporary bonders with more than twice the throughput. **FIGURE 1** shows an exemplary process flow for 2.5D interposers with 3D-IC chips stacked by chip-to-wafer bonding [2]. Another key 3D-integration concept is overmolding prior to debonding, which allows double-side processing on ultra-thin wafers while avoiding thin-wafer handling altogether. As shown in **FIGURE 2**, after chip stacking the entire wafer is overmolded while the thin interposer wafer is still bonded to the carrier wafer. This overmolding compound creates a rigid film on top of the thin interposer wafer.

An analysis of the published process flows for 3D-IC manufacturing today shows that bump-last process flows and overmolding prior to debonding have already been implemented. Within TSMC's Chip-on-wafer-on-substrate (CoWoS) process flow [3], the chip stacking on the interposer occurs before the backside of the interposer is processed. It is a complete reversal from the previous paradigm that individual chips have to be tested prior to stacking. KGD manufacturing of the interposer is not possible with this process flow. However, from the pragmatic manufacturing point of view it allows manufacturing of thin wafers while avoiding handling of thin wafers. Implementing a bump-last approach also increases flexibility and eliminates the risk of bump damage during stacking. Texas Instruments' stacked wafer chip-scale package (WCSP) platform separates the interposer and chip manufacturing, which is more in line with the classical foundry/OSAT model [4]. However, like the CoWoS process flow, it allows the creation of ultra-thin interposers without the need to handle thin wafers at any point during manufacturing or assembly.

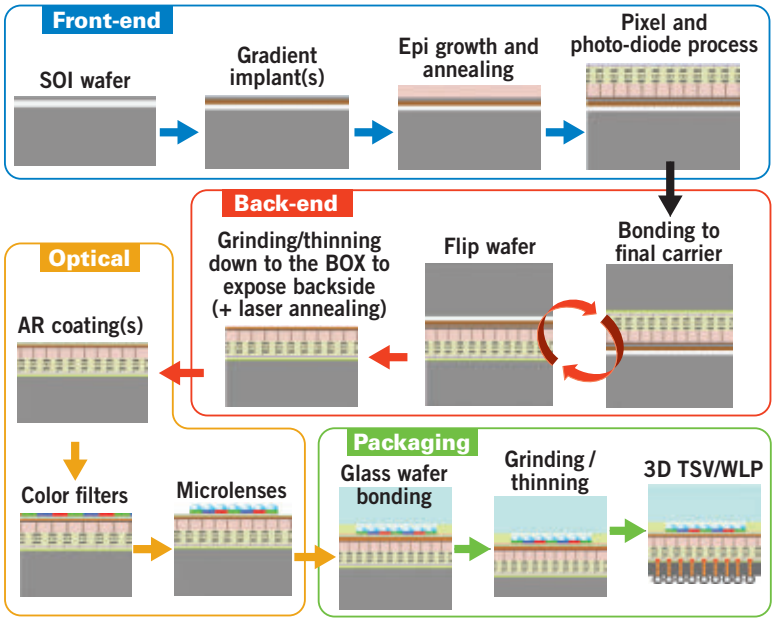

FIGURE 3. Process Flow for backside illuminated image sensors (Courtesy of Yole Développement)

FIGURE 3 shows a typical process flow for backside illuminated image sensors. An ultra-thin device wafer is created by permanent wafer bonding to a silicon

FIGURE 4. The EVG GeminiFB fusion wafer bonding system integrates wafer cleaning, LowTemp® plasma activation, SmartView® wafer-to-wafer alignment system and wafer bonding all in one system.

carrier wafer. After a series of process steps this wafer stack is bonded to a glass wafer, which then acts as a carrier wafer for further processing. This allows thinning of the initial silicon carrier wafer and creating TSVs. Essentially, the original carrier wafer now becomes an interposer wafer. An important aspect is that in this case the image sensor-interposer connection is bump-less, which allows interconnects with a fine pitch down to less than 2 micron while at the same time saving the cost to create bumps.

One paradigm of 3D-IC manufacturing was that the industrial adoption will first start with chip-to-chip stacking (C2C), later on move to chip-to-wafer-stacking (C2W) and finally move to wafer-to-wafer stacking (W2W). W2W integration has the fundamental limitations that the dies have to have the same size and that a good die might be stacked onto a defective die. However, with respect to manufacturing complexity it has a lot of advantages; first and foremost that it allows parallel processing of all dies on the wafer. In fact, it is remarkable that W2W stacking with TSVs has been successfully implemented for many devices already, especially low-cost devices. Due to the successful implementation of backside illuminated image sensor manufacturing on large substrates, a 300mm wafer bonding infrastructure has been established in the industry. Fusion wafer bonding (as shown in **FIGURE 4**) is the method of choice for bump-less chip-chip interconnects for both via-last integration for oxide-oxide bond interfaces and via-middle integration with hybrid oxide/metal bond interfaces. Fusion wafer bonding is also a key technology for monolithic 3D integration as it can be used to transfer thin layers of silicon on top of an already processed wafer.

One interesting aspect of W2W integration is that it enables ultra-shallow TSVs. It is possible to implement 1 µm x10 µm or 1 µm x 5 µm TSVs without the need to deal with 5 µm or 10 µm thin wafers. As the cost of TSV manufacturing is strongly correlated to TSV depth and TSV aspect ratio, W2W integration allows significant cost reduction. W2W integration also enables much better die-to-die alignment accuracies compared to C2C and C2W thereby enabling the usage of small TSV diameters and fine TSV pitch (**FIGURE 5**).

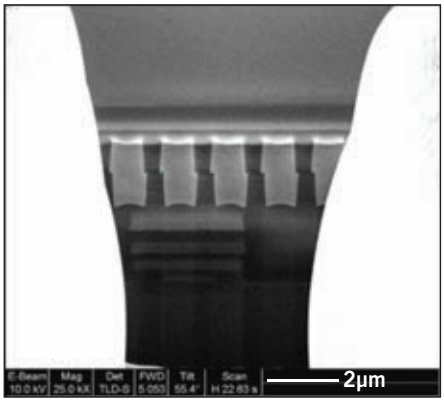

FIGURE 5. The EVG SmartView® aligner provides sub-micron wafer-to-wafer alignment accuracy enabling fine pitch interconnects. (Courtesy of SiliconFile Technologies, Inc.)

Stacked memory is a potential application for W2W stacking as the dies have the same size. It is questionable whether die testing prior to stacking can be implemented for memory. If testing prior to stacking were not to be implemented then W2W integration is a natural choice due to reduced TSV cost

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Semicon West: Precision is key to scaling below 14nm

DEBRA VOGLER, *SEMI, San Jose, CA*

TechXPOT speakers highlight the challenges ahead on the road to 14nm.

Semicon West 2013 will be held July 9-11 at the Moscone Center in San Francisco, and will feature over 500 exhibitors, 50 hours of conference programs and more than 30,000 industry attendees. In advance of the 2013 SEMICON West TechXPOTs on lithography and nonplanar transistors beyond 20nm, SEMI asked some of the speakers and industry experts to comment on the challenges they wanted to highlight. Many of the inputs focused on the need for precision in the processes used to form transistors, as well as how EDA can contribute to mitigating variability.

Likely enhancements on the logic roadmap below 20nm are a move to FinFET, improved FinFET implementation, high mobility channel, and gate all around (GAA) structures, noted Adam Brand, senior director, Transistor Technology Group at Applied Materials. He told SEMI that, "The increased complexity of the FinFET, high mobility channel, and GAA devices in combination with continued scaling requires more precision in structure formation and improved materials to address structure formation and parasitic effects."

The key steps for maintaining the structural integrity of the fin are precision etch, void-free STI fill, recess, and precisely tailored corner rounding through dummy gate oxidation. Dummy gate oxidation addresses the challenge of ensuring that electric fields can be avoided in the corner explained Brand, who will present at SEMICON West 2013. "The dummy gate serves two purposes," said Brand. "It's a structural element and it's there when you do the transistor formation so it can serve roles such as being the etch stop for the gate etch. It's also able to play a role in shaping the fin." The fin can be shaped by changing the oxidation rate depending on the amount of oxidation needed for the side vs. for the corner.

Precision again comes into play when forming the gate — precision CMP is required to control the dummy gate and replacement metal gate height. The dummy gate material must also be easily removed. "Advanced CVD materials offer more choices in materials for differentiating selective removal," said Brand. "Implant-based precision material modification (PMM) has been effective in changing selectivity to

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obtain better structure control." He noted that in the past, CMP had not played a role in directly affecting the geometry of the transistor, but now, it is playing a much more direct role in determining the size of the transistor features. For example, in the replacement metal gate step, CMP is used to polish the metals used for the replacement gate structure and it's also used for the self-aligned contact polish. "So now, you're polishing the gate at least three times in order to form it, and you need very precise gate height control because it affects the overall stack height and contact height."

Further complicating transistor scaling is that the 3-D structure adds complexity in strain-related mobility enhancement. "Source/drain stressor shaping is needed to optimize strain and control unwanted increase in the Miller capacitance," said Brand. "Lower k dielectrics are also needed to manage the Miller capacitance." He further explained that when strain is implemented in a FinFET, each source/drain area is a separate fin — as opposed to when strain is being implemented on planar devices. "When you grow the source/drain [in a FinFET], it grows both horizontally and vertically, so when you scale the pitch of the fins, there's the challenge that eventually those source/drain stressors come very close to each other and they might merge." The solution, therefore, has to allow the stressors to grow without having them merge between the transistors and still obtain the amount of strain that is wanted. The solution must also address the Miller capacitance.

The SOI value proposition changes below 20nm

Gary Patton, VP at IBM's Semiconductor Research and Development Center, told SEMI that in order for the full benefit of the FinFET to be realized below 20nm, a dielectric isolation scheme is necessary to counter the uniformity and variability challenges. "The arrival of the FinFET era has brought about a fundamental paradigm shift in the SOI value proposition such that the advantages of SOI-based innovation now extend well beyond just device performance as in the planar case," said Patton. Indeed, Soitec, and others, such as STMicroelectronics, are betting that SOI-based technology will be used as a bridge enabling the industry to get the performance benefits of a fully-depleted transistor while staying with a planar transistor all the way from 28nm down to 14nm, or perhaps even sub-14nm.

To those who question the added cost of going with an SOI-based platform, Patton said that the cost of dealing with the isolation challenge offsets the cost of using SOI substrates. "Offset costs are due to both additional process steps required for bulk, and increases to die area," said Patton. "An STI isolation module must be added for bulk FinFETs, as well as a series of masking steps and implants for isolation-leakage control and latch-up avoidance. Estimated additional processing costs of bulk isolation offsets the cost advantage of bulk substrates over SOI." He also pointed out that die area increases are driven by the need for well contacts, and I/O guard-rings (latch-up avoidance). "We also anticipate the overall die yield to be challenging for the bulk FinFET process due to variability and the need for matching performance of critical circuit paths in a chip."

Another consideration for proponents of SOI-based technology is the issue of process variability. "A buried oxide layer (BOX) in SOI fins is responsible for three areas of improvement in variability over bulk-isolated FinFETs," Patton told SEMI. "First, the top silicon layer is terminated by the buried oxide, is proven to be extremely uniform in thickness, and defines the height of the fin both physically and electrically, since any fin over etch does not contribute to the fin height." He further explained that the source and

drain are completely separated by the gated channel, unlike in a bulk FinFET, where there is a continuous path for leakage, requiring a highly doped punch-through stop.

"The non-abrupt nature of doping introduces a non-uniform doping profile, and hence, turn-on current, between the top and bottom of the fin, further eroding the FinFET advantage." Patton noted that a more practical consideration is the slope or taper of the fin itself. "From an electrical point of view, the ideal fin would be perfectly vertical and of uniform thickness from top to bottom. In a bulk fin process, a degree of taper must allow for the subsequent oxide fill and etch-back, and also to accommodate a reduced spacer over-etch budget (vs. an SOI fin). The fin taper introduces further non-uniformity to the FinFET, which reduces switching speed."

EDA tackles variability

Reducing/mitigating process variability is ever more critical to yield as the industry scales transistors below 20nm, and much can be done in the design arena to help. For example, EDA considerations can mitigate "noise" in the optical system [lithography] that is a source of variability.

Mike Rieger, group director, R&D, Silicon Engineering Group at Synopsys, uses communication theory to analyze certain aspects of a lithographic system. He told SEMI that when there are optical systems [lithography] without tuning, i.e., a "plain vanilla" system — all the spatial frequencies in the visible limit are present. Conversely, when the design is friendly to specific spatial frequencies and you then try to print that design with an optical system that is friendly to all spatial frequencies, there are other frequencies that leak through. This "leakage" causes a lowering of the contrast in the optical image. "With the lower contrast, the image is more susceptible to other sources of variation like defocused variation, or dose variation, and that translates into your printed features having more variation in their dimensions," said Rieger, another speaker at the upcoming SEMICON West.

Rieger added that, if you can prevent the unwanted frequencies from even being passed through the optical system, the net result is that the contrast is improved. Additionally, by tuning these frequencies, the diffraction orders in the stepper (the rays of light used to form the image) are manipulated. "You can eliminate the zero order ray. This zero order ray reduces contrast and it also limits the maximum frequency that you can image." The tuning process – also known as source mask optimization (SMO) – really isn't the end game, noted Rieger. "It's source design optimization that is the end game. You tune the configuration of your design to be consistent with the optimization of the source."

Regarding the parallel paths the industry is taking – extending optical lithography while developing EUVL — Rieger is realistic in his assessment of what EDA can bring to the table. "We're going to be using 193i for the foreseeable future — it will be years before 193i is replaced," said Rieger. But, "Optical lithography on a single exposure is maxed out in terms of the density it can print, so if you want to get more transistors per chip or more details per chip, you must do a couple of things." Those are: tuning the optics, which comes at a cost, and using multiple exposures. "To get an effective result, the whole process of the tuned optics and the multiple exposures must be comprehended in the physical layout software, and some of the things that need to be done go beyond what you can accomplish with the traditional rule-based constraint that you put on the layout."

For more information on SEMICON West 2013, visit http://www.semiconwest.org. To view all the TechXPOT info, visit http://www.semiconwest.org/SessionsEvents/TechXPOTs.

All-in-one microscope for advanced imaging, recording and measurement

KEYENCE Corporation has released a new multipurpose microscope. The VHX-700F allows users to leverage some of the advanced functions of the VHX Series, such as Depth Composition and 3D Display, while offering the same image quality and primary measurement capabilities at a lower price point. The VHX-700F incorporates observation, measurement, and image recording capabilities into a single device, while offering all of the imaging techniques found in traditional inspection equipment. The microscope boasts a 0.1x – 5,000x magnification range and provides bright field, dark field, and transmitted illumination. Additional attachments offer polarized, diffused, and DIC imaging methods. Users can also inspect inside of small openings with a complete lineup of borescopes and fiberscopes.

By combining the technology generally found in stereoscopic, metallurgical, measurement, and scanning electron microscopes, the VHX-700F is able to accentuate the strengths of these systems while avoiding many of their limitations. Not only can images be captured entirely in focus with the exceptionally large depth-of-field, but a variety of measurements can be completed directly on the image with just a click of the mouse. A multi-angle stand is paired with a rotating stage to allow 360 degree views without the need to fixture or manipulate the sample, and the camera easily detaches for handheld, non-destructive imaging of larger parts.

LEXT OLS4100 laser confocal microscope

Olympus tannounced the release of the LEXT OLS4100 laser confocal microscope system. Designed to deliver nanometer-level imaging, accurate 3D measurement, and outstanding surface roughness analysis, the OLS4100 features auto brightness and a new high-speed stitching mode.

The OLS4100's auto brightness setting is part of an automatic 3D image acquisition system that allows even first-time users to quickly acquire 3D images with the click of a button, greatly reducing image acquisition time. A new high-speed stitching mode allows the user to specify target areas from wider-area stitched images.

The OLS4100 employs a dual confocal system that, when combined with its high-sensitivity detector, enables the capture of clear images from samples consisting of materials with different reflectance characteristics. In addition to the laser image, the OLS4100 uses a white LED light and a high-color-fidelity CCD camera to generate clear, natural-looking color imagery comparable with that obtained with high-grade optical microscopes. This color image can be overlaid upon the 3D laser image for a 3D representation of your sample.

The OLS4100's new multilayer mode is capable of recognizing the peaks of reflected light intensities of multiple sample layers and setting each layer as a focal point, making it possible to observe and measure the upper and lower surfaces of a sample with a transparent coating. This multilayer mode also facilitates the observation and measurement of multiple layers of transparent materials.

3M QDEF brings 50% more color to LCD devices

3M announced it is in the final stages of scale-up for its new 3M Quantum Dot Enhancement Film (QDEF). The new film allows up to 50 percent more color than current levels in liquid crystal display (LCD) devices. 3M has teamed with Nanosys, Inc., to produce the 3M QDEF solution specifically to deliver more color, and to make devices such as smart phones, tablets and televisions, lighter, brighter and more energy efficient.

QDEF utilizes the light emitting properties of quantum dots to create an ideal backlight for LCDs, which is one of the most critical factors in the color and efficiency performance of LCDs. A quantum dot, which is 10,000 times narrower than a human hair, can be tuned to emit light at very precise wavelengths. This means display makers can create a highly-optimized backlight that only produces the exact wavelengths of red, green and blue light needed by an LCD for optimal color and energy performance. Trillions of these quantum dots protected by barrier film fit inside an LCD backlight unit. The new film replaces one already found inside LCD backlights, which means the manufacturing process requires no new equipment or process changes for the LCD manufacturer.

A single-wafer cleaning solution for 3D-IC/TSVs, advanced packaging, MEMS and compound semiconductor applications

EV Group and Dynaloy, LLC introduced CoatsClean—an single-wafer photoresist and residue removal technology designed to address thick films and difficult-to-remove material layers for the 3D-ICs/through-silicon vias (TSVs), advanced packaging, MEMS and compound semiconductor markets.

The CoatsClean process and chemical formulation are engineered to perform at higher temperatures, resulting in faster stripping rates and cycle times. This enables CoatsClean to operate as a single-wafer process for thick resist films and difficult-to-remove resists—resulting in improved performance, consistency, reproducibility and repeatability. The engineered formulation also enables selective stripping of the resist.

CoatsClean is also unique in its ability to dispense a small amount of material on the top of the wafer, and then activate the material with direct heat. This direct utilization of the material and heat dramatically reduces the strip material used. CoatsClean uses fresh solution for each processed wafer compared to competing techniques that use an immersion bath—resulting in greater process efficiency and eliminating cross contamination. The highly selective application of resist strip material eliminates damage to the wafer backside. The entire CoatsClean process is performed in a single bowl, which reduces tool footprint.

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– 1000nm) for both CD1 and trench depth, which cannot be accurately measured using the limited wavelength range (375nm – 750nm). The apparent wafer non-uniformity is common for samples after an etch process. For trench depth, there is a center to edge effect, with lower trench depth at the wafer center. For CD1, the largest CD value is on the left side of the wafer, with the smallest CD on the right side. The wafer non-uniformity is significant, which speaks to the importance of a multi-point measurement to verify that all points across the wafer are within specification. This would be extremely time consuming to achieve with cross section SEM measurements, but is much more practical with the n&k Olympian, where 25 points can be measured in about two minutes.

Conclusion

A broadband polarized reflectometry measurement, utilizing RCWA analysis, can be used to obtain detailed trench profile results. The system provides trench depth and CD results comparable to cross-section SEM, with a method that is both high-throughput and non-destructive. The capabilities have been demon-

strated with the measurement of five samples that have undergone different processing conditions. In comparison to the limited wavelength range of standard reflectometers (375nm - 750nm), use of a wider 190nm - 1000nm wavelength range provides more sensitivity to the trench profile, and the ability to accurately measure trench structures with smaller CD values and deeper trenches.

Acknowledgement

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and precise alignment capability. In this way, the image sensor has paved the way for W2W integration for memory.

Conclusion

3D integration can provide many benefits, but only where it can prove to be a sustainable innovation. TSV and 3D chip stacking have been successfully implemented for devices like FPGAs and image sensors, where 3D IC was a means to improve the sales critical parameters of the devices. Its implementation in high-volume manufacturing occurred despite high technical complexity and the omnipresent cost pressure, which is compounded for low-cost devices. Innovation theory suggests that once a new technology has been established for one product, it can be adopted very rapidly by other products.

The process flows applied today for real product manufacturing are quite different from the process flows initially proposed for a universal 3D IC. Chip manufacturing and packaging process flows have since been concurrently optimized. Today, C4 bumps are generally manufactured as late as possible in the overall manufacturing process. Thin-wafer processing is a key competence, but in many cases thin-wafer handling after debonding has been eliminated by either overmolding or wafer bonding to another device wafer prior to debonding. Image sensors apply the most radical concept of W2W stacking, which allows reduced manufacturing costs due to bump-less integration and ultra-shallow TSVs. 3D ICs based on W2W integration is a reality today.

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Learning the secrets of design for yeild

Random process variations and layout-dependent effects are a fact of life for designers working at the more advanced process nodes and become critical at 45nm. Besides random and systematic variation effects, reliability effects, such as bias-temperature-instability (BTI), also become prevalent, introducing another dimension of variations that impact parametric yield.

These variations are unavoidable and, in fact, increasing as we move to more advanced nodes, where circuit designers encounter yield problems and need to spend extra effort on variation analysis for yield and performance trade-off.

On one side, foundries have to double or even triple their efforts to make complicated model libraries to characterize different types of variations, despite having to cover variation sources across the full statistical space—an impracticality.

Conversely, efficiently running variation analysis with the best use of foundry models becomes critical for circuit designers, and is one of the more challenging aspects of system-on-chip (SoC) design that project teams face daily.

This means design-for-yield (DFY) considerations are more important than ever. And yet, we as an industry may not fully understand device modeling and its impact on DFY results. This is due in large measure to no clear definition of DFY. Some people are confused by DFY and design-for-manufacturing (DFM), and consider DFY a foundry's responsibility or do not know what the role of DFY is. The value of DFY highly relies on how "good" the foundry models are and how efficient the tool can leverage model information to run needed analysis, such as statistical circuit simulations.

Foundry models can never be perfect, but represent process information that a DFY analysis requires. Designers need to have an appropriate expectation on models, especially for advanced technologies, and also understand model limitations. With this understanding, extracting information from models and making good use of this information together with DFY tools is becoming more critical.

Of course, DFY is not a new phenomenon and tools being categorized for DFY have been available commercially for some time now. They haven't been widely adopted because they have not provided enough value to project teams due to the lack of information or confidence in the analysis results. Statistical simulation, such as Monte Carlo analysis, has been costly and time consuming, even for a 3s problem. Designers either skip Monte Carlo or often run a small number of samples that can limit the confidence level, making DFY analysis results unreliable and less valuable. Other types of analysis, including process-voltage-temperature (PVT) analysis, also run into similar problems if designers want to cover all corner cases that can easily increase up to hundreds of corners. A faster simulation engine, intelligent statistical analysis algorithms, and better use of foundry model information are the key components that EDA companies need to provide to make DFY tools more practical and reliable.

> We as an industry may not fully understand device modeling and its impact on DFY results

The final key would be on the application side. Circuit designers need to understand when and where they can apply DFY on top of their traditional design flow, and how to leverage DFY to achieve an optimal yield versus performance-power-area (PPA) trade-off. During the 50th Design Automation Conference (DAC) in June, a panel of foundry experts weighed in with their opinions: Dr. Min-Chie Jeng from Taiwan Semiconductor Manufacturing Co. (TSMC); Dr. Luigi Capodieci from GLOBALFOUNDRIES; and Dr. Bruce McGaughy from ProPlus Design Solutions, Inc. The panel, moderated by SST Editor-in-Chief Pete Singer, shared best practices and techniques to manage these sub-nanometer effects to improve manufacturability and yield.

Dr. ZHIHONG LIU,
Executive Chairman, ProPlus Design Solutions

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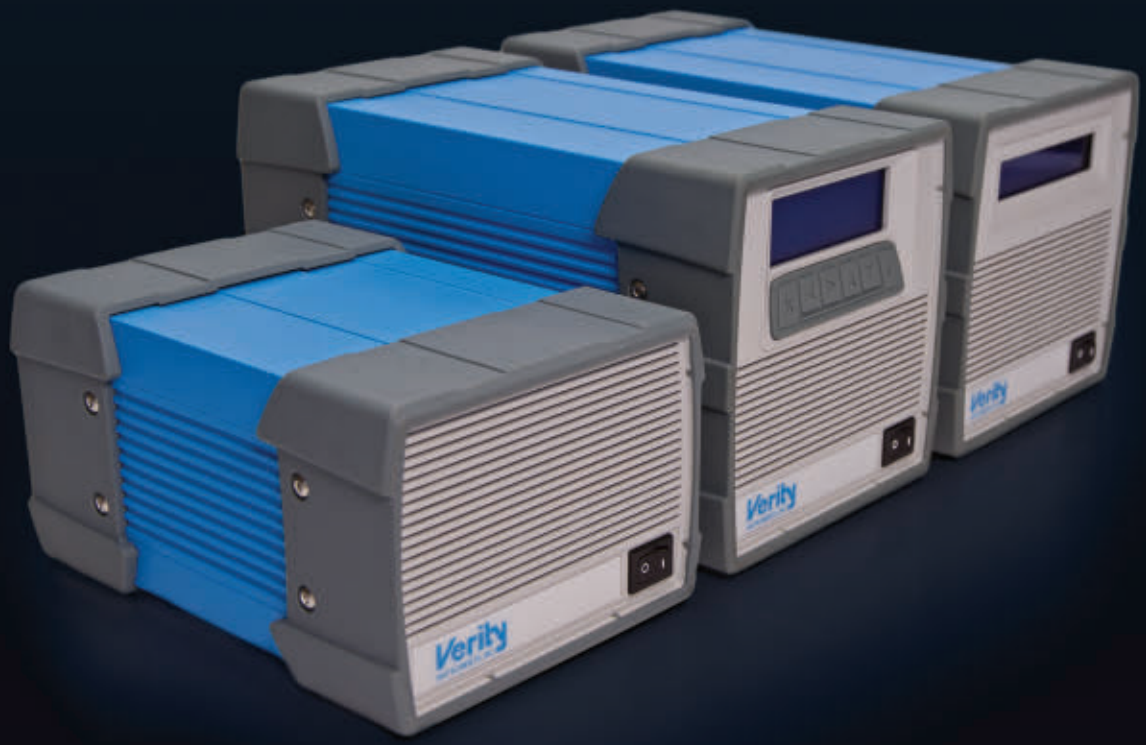

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