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EVG's integrated fusion bonding platform is designed for 3D/TSV high-volume manufacturing requirements.

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What consolidation means for you

The hottest rumor at the 2014 ECTC in Orlando was that STATSChipPAC (SCP) was "in play" (about to be acquired). One version of the rumor had at least 3 bids on the company including GlobalFoundries (IFTLE finds it hard to imaging GF could swallow both IBM and SCP at the same time), ASE and "a group of un-named mainland China companies." Inquiries to SCP contacts substantiated the rumors although they had no knowledge of the details. Sure enough the Wall Street Journal on indicated that SCP was "considering an offer for all its shares."

http://bit.ly/1vUy53u

Insights from the Leading Edge: Symposium on Polymers

The 16th biennial Symposium on Polymers was held this May in Wilmington DE. Keynote speakers included Steve Bezuk, Qualcomm, James Lee, Strategic Foresight Investments, John Hunt, ASE and Mark Poliks SUNY Binghamton.

http://bit.ly/1yiW0vE

Industry sustainability efforts mount with III-Vs and other advanced technologies

The introduction of new materials, such as III-Vs, into high-volume manufacturing of semiconductors, likely will occur sometime around the 7nm and/or 5nm nodes. III-V's introduction, along with the potential transition to 450mm wafers, and the increasing expansion of global regulatory requirements, will heighten environmental, health and safety (EHS) concerns that must be addressed as the industry goes forward. The Sustainable Manufacturing Forum to be held in conjunction with SEMICON West 2014, will feature experts in the manufacture of semiconductors, microelectronics, nanoelectronics, photovoltaics, and other high-tech products.

http://bit.ly/1lD9pVn

n&b news and blogs

The next big thing: IoT

The semiconductor industry has greatly benefited from the push to mobile technology, but what's next? It could well be the Internet of Things (IoT), which includes smart homes, smart cars, smart TVs, wearable electronics and beacons. According to an analysis by Business Insider, The Internet of Things alone will surpass the PC, tablet and phone market combined by 2017, with a global internet device installed base of around 7,500,000,000 devices.

http://bit.ly/SoYGqy

Qualcomm: Scaling down is not cost-economic anymore – so we are looking at true monolithic 3D

Over the course of three major industry conferences (VLSI 2013, IEDM 2013 and DAC 2014), executives of Qualcomm voiced a call for monolithic 3D "to extend the semiconductor roadmap way beyond the 2D scaling" as part of their keynote presentations. From SemiMD, part of the Solid State Technology network

http://bit.ly/1lD5SuC

Synopsys design flow support for Samsung-ST 28nm FD-SOI

The Synopsys' Galaxy Design Platform has been extended to support the Samsung-STMicroelectronics strategic agreement on 28nm FD-SOI. From SemiMD, part of the Solid State Technology network

http://bit.ly/1iak1QQ

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editorial

Three fundamental shifts

At The ConFab in June, Dr. Gary Patton, vice president, semiconductor research and development center at IBM, said there is a bright future in microelectronics (I heartily agree). He said that although there seems to be a fair amount of doom and gloom that scaling is ending and Moore's Law is over, he is very positive. "There are three huge fundamental shifts that are going to drive our industry forward, will drive revenue growth and will force us to keep innovating to enable new opportunities," he said.

> "It's estimated that today there are about 12.5 billion devices connected to the internet. That's expected to grow to 30 billion by 2020."

The first fundamental shift is the explosion of applications in the consumer and mobile space. Patton noted examples such as cars that can drive themselves and can detect people and bicyclists and avoid them, smart phones for as little as $25, wearable devices that not only tell you what you're doing but how you're doing, and 4K television. "That is an incredible TV system, but it's going to demand a lot of bandwidth; twice the bandwidth that's out there today. If you turn on your 4K system, your neighbors are going to start to notice it when they try to access the internet," he said.

Patton said that it's estimated that today there are about 12.5 billion devices connected to the internet. That's expected to grow to 30 billion by 2020. This represents the second fundamental shift commonly known as Big Data. "All these interconnected devices are shoving tremendous amount of data up into the cloud at the rate of 1.5 Exabytes (1018) bytes of data per month," Patton said. "And that's grown by about an order of magnitude in just the last 13 years. The estimate is that in the next 4 years, it's going to go up another order of magnitude. It's accelerating."

The third fundamental shift is with all this data going up into the cloud, the data is almost all unstructured data, such as video and audio. "It's related data but disconnected. How do we take that data and do something with it? That brings us to analytics and cognitive computing. We have really just started in this arena."

So there you have it. Three reasons to be very positive about the future of the semiconductor industry: an explosion of applications, the rise of big data and the need to analyze all that data.

—Pete Singer, Editor-in-Chief

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The ConFab

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ASIA | **Samsung Display** was awarded the Gold Display of the Year award at SID Display Week 2014 for it's curved super AMOLED display panel.

USA | **Dow Corning** launched the power electronic industry's first SiC wafer grading structure.

ASIA | Osamu Nakamura was named President of **SEMI Japan.**

EUROPE | **imec** presented at VLSI circuits symposium 2014 a low power pipelined SAR ADC in 28nm digital CMOS with record resolution, speed and power performance.

USA | **Entropic** announced plans to close and consolidate several global facilities, a move that would impact approximately 23 percent of its headcount.

CANADA | Researchers from the **University of Toronto** have designed and tested a new class of solar-sensitive nanoparticle, called colloidal quantum dots, that could lead to cheaper and more flexible solar cells.

USA | **ON Semiconductor** announced plans to acquire Aptina Imaging.

ASIA | **Samsung** announced that the IP and design enablement ecosystem for its foundry's 14nm FinFET process technology is firmly in place for customers to begin their early design work.

EUROPE | Researchers from the **Institut Català de Nanociència i Nanotecnologia** reported on a new cost-effective nanoimprint lithography methodology that improves ordering in periodic arrays from block copolymers.

On the road to recovery: Semiconductor growth expected for the next two years

According to the IMF and predictions by many other market research firms, 2014 and 2015 are expected to be growth years, comparable to or even better than the past few years. After years of decline, even the Europe area will show positive GDP growth in 2014 and 2015, signaling a strengthening recovery.

Historically, GDP, semiconductor revenues, and semiconductor capex are correlated. Last year was an exception with revenue up about 6 percent (year-over-year) but capex down -3 percent to -4 percent. Projected revenue is now predicted to be 8 percent for 2014 and 5 percent for 2015.

SEMI's data show that after two years of decline, semiconductor capex (excluding fabless and backend) is expected to grow for two years. While some companies are expected to keep capex steady in 2014, others have increased plans in 2014 with capex expected to increase 8 to 10 percent. With further growth between 6 and 8 percent expected in 2015, the industry may approach records at levels similar to 2007 and 2011.

Continued on page 6

200mm equipment market gaining new lease on life

In 2004/2005, shipments of 300mm wafer fab equipment (WFE) began to outpace that of 200mm platforms. As the "baton" in the node-scaling race appeared to pass from 200mm to 300mm, it was clear that device manufacturers were transitioning to higher-volume, more cost-effective 300mm toolsets for cost efficiencies of the production of advanced memory and microprocessor devices. Tool suppliers enabled the transition with the availability of the comprehensive 300mm toolset and began a new 300mm technology race, and leaving the major OEMs to focus on service and spares for the now legacy 200mm toolsets. With advanced device designs fully transitioned to 300mm, many IDMs and foundries were left with growing excess capacity on their 200mm production lines. Surprisingly, new life and attention has been refocused on the 200mm tool sets and available capacity as two phenomena are driving new requirement and economics. First, in 2006, a MEMS (Micro-Electro-Mechanical Systems)-based accelerometer became a game changer when introduced into Nintendo's next-generation Wii motion controller. This was the first significant and novel use of a MEMS device for motion tracking

Continued on page 10

UC Santa Barbara researchers introduce highest performing III-V metal-oxide semiconductor FET

Researchers from the University of California, Santa Barbara (UCSB) introduced the highest performing III-V metal-oxide semiconductor (MOS) field-effect transistors (FETs) at the 2014 Symposium on VLSI Technology.

The UCSB research promises to help deliver higher semiconductor performance at lower power consumption levels for next-generation, high-performance servers. The research is supported by the Semiconductor Research Corporation.

The UCSB team's III-V MOSFETs, for the first time in the industry, exhibit on-current, off-current and operating voltage comparable to or exceeding production silicon devices — while being constructed at small dimensions relevant to the VLSI (very-large-scale integration) industry.

For the past decade, III-V MOSFETs have been widely studied by a large number of research groups, but no research group had reported a III-V MOSFET with a performance equal to, let alone surpassing, that of a silicon MOSFET of similar size. In particular, UCSB's transistors possess 25 nanometer (nm) gate lengths, an on-current of 0.5mA and off-current of 100nA per micron of transistor width and require only 0.5 volt to operate.

"The goal in developing new transistors is to reach or beat performance goals while making the transistor smaller—it is no good getting high performance in a big transistor," said Mark Rodwell, professor of Electrical and Computer Engineering, UCSB. "In time, the UCSB III-V MOSFET should perform significantly better than silicon FinFETs of equal size."

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Fab equipment spending: 24% in 2014 with possible record in 2015

In the May 2014 World Fab Forecast publication, SEMI tracks more than 200 major projects involving equipment spending for new equipment or upgrades, as well as projects to build new facilities or refurbish existing facilities. Between last quarter's report in February and now, 265 updates have been made to the proprietary SEMI database. SEMI now predicts 24 percent growth (to about US$35.7 billion) for fab equipment spending (new, used, in-house) for Front End facilities in 2014 and 11 percent growth (to about US$39.5 billion) in 2015. In terms of equipment spending, 2015 is on track to surpass all-time record year 2011. See Figure 1.

2014, the three largest regions for fab equipment spending will be Taiwan with over US$10.3 billion, the Americas with over US$6.8 billion, and Korea with over US$6.3 billion. In 2015, these same regions will lead in spending: Taiwan will spend over US$11 billion, Korea over US$8 billion, and the Americas almost US$7 billion.

Although sixth in 2014 for projected fab equipment spending, the Europe/Mideast region will show the strongest rate of growth, about 79 percent compared to the prior year. The same region will continue to grow quickly in 2015, with an increase of about 20 percent.

Fab Equipment Spending Change Rates

	2012	2013	2014	2015
Americas	-15%	-34%	36%	2%
China	-40%	32%	69%	-6%
Europe & Mideast	-38%	-33%	79%	21%
Japan	-43%	8%	11%	15%
Korea	0%	-37%	23%	27%
SE Asia	-49%	53%	-43%	44%
Taiwan	4%	13%	11%	7%
SUM	-18%	-12%	24%	11%

(For Front End Facilities includes new, used, in-house).
Source: SEMI World Fab Forecast reports (May 2014)

Trade ratio for leading-edge upgrades affects capacity

Worldwide installed capacity is very low for both 2014 and 2015 and SEMI data do not suggest that this will change the next four years.

Depending upon node transition, product segment, and age of a fab, the trade ratio for space affects capacity in more significant ways. Because of increased complexity at the leading edge nodes, such as more process steps and multiple patterning, fabs experience a decline in capacity as the same fab space produces less. Worldwide, installed capacity grew by less than 2 percent in 2013 and is expected to grow just 2.5 percent in 2014 and 3 percent in 2015.

Future Fabs: Count of Facilities with Construction spending

	2012	2013	2014	2015
Americas	8	8	5	2
China	19	9	6	7
Europe & Mideast	12	12	3	3
Japan	7	3	5	1
Korea	5	4	3	1
SE Asia	2	4	2	3
Taiwan	9	9	8	5
SUM	62	49	32	22

(Counting Front End Facilities including Discrete/LED)
Source: SEMI World Fab Forecast reports (May 2014)

The SEMI data predict that Foundry capacity continues to grow at 8 to10 percent yearly (a steady pace from 2012) and Flash will be up 3 to 4 percent for 2014. Although DRAM equipment spending is expected to grow by 40 percent in 2014 as many fabs are upgrade to leading-edge processes, installed capacity for DRAM is expected to stay flat or even drop by -2 percent. SEMI's reports also cover capacity changes for other product segments: MPU, Logic, Analog/Mixed signal, Power, Discretes, MEMS, and LED and Opto.

According to the SEMI World Fab Forecast, by the end of 2014 there will be 26 volume fabs using technology nodes between 14nm to 16nm, including two with 3D-NAND. By the end of 2015, this is expected to increase to 33 volume fabs with 14nm to 16nm process nodes, including 11 with 3D NAND.

Fewer new fabs but will they be enough?

According to SEMI, 2013 was an all-time record year for construction projects for semiconductor Front End facilities (new and refurbish existing fabs) with over US$9 billion spent. Although less construction projects will occur during 2014 and 2015, there are still a few significant new fabs being constructed or in planning stages, in regions such as Europe/Mideast, Japan, U.S., and Taiwan. Thirty facilities (including Discretes and LEDs) will begin volume production in 2014 and 2015.

Excluding foundries, existing and known, currently planned IC volume fabs will reach full capacity by 2018 according to SEMI data. Considering the diminishing prospect for high-volume 450mm fabs in the immediate future, and that overall capacity is lost when upgrading facilities to leading-edge nodes, the industry must add more 300mm fabs to meet demand. The timeline to build and equip these new complex facilities, about 1.5 years, suggest that new 300mm fab plans will need to start by next year. ◆▶

Continued from page 7

To reach this breakthrough in performance, the UCSB team made three key improvements to the III-V MOSFET structure. First, the transistors use extremely thin semiconductor channels, some 2.5nm (17 atoms) thick, with the semiconductor being indium arsenide (InAs). Making such thin layers improves the on-current and reduces the off-current. These ultra-thin layers were developed by UCSB Ph.D student Cheng-Ying Huang under the guidance of Professor Arthur Gossard.

Next, the UCSB transistors use very-high-quality gate insulators, dielectrics between the gate electrode and the semiconductor. These layers are a stack of alumina (Al2O3, on InAs) and zirconia (ZrO2), and have a very high capacitance density. This means that when the transistor is turned on, a large density of electrons can be induced into the semiconductor channel. Development of these dielectric layers was led by UCSB Ph.D student Varista Chobpattana under the guidance of Professor Susanne Stemmer.

Third, the UCSB transistors use a vertical spacer layer design. This vertical spacer more smoothly distributes the field within the transistor, avoiding band-to-band tunneling. As with the very thin InAs channel design, the vertical spacer makes the leakage currents smaller, allowing the transistor's off-current to rival that of silicon MOSFETs. The overall design, construction and testing of the transistor was led by UCSB Ph.D student Sanghoon Lee under Rodwell's guidance.

"The UCSB team's result goes a long way toward helping the industry address more efficient computing capabilities, with higher performance but lower voltage and energy consumption," said Kwok Ng, Senior Director of Device Sciences at SRC. "This research is another critical step in helping ensure the continuation of Moore's Law — the scaling of electronic components."

Continued from page 4

in a high-volume consumer application. Next, in 2007, when Apple Inc. first introduced the iPhone to the world, it came to light that MEMS devices were enabling a number of its advanced motion-based features. Later, it would be noted that more than 75 percent of the semiconductor device content in the iPhone was sourced from 200mm wafer starts. The devices manufactured on 200mm wafers spanned a wide variety of applications that included not only MEMS applications (motion, audio, RF, etc.) but also CIS (CMOS Image Sensor), communications, power management and analog devices. Sold in the hundreds of millions per year, first the iPhone and then the multitude of other smart phones, tablet PCs, and related digital devices, that followed, drove the adoption of the emerging "More-than-Moore" class of devices (which were first pioneered on 150mm wafers at the time) onto 200mm wafers. These high-volume consumer applications gave rise to a resurgence in both new and used of 200mm equipment. This sudden requirement for new sourcing of "legacy" 200mm toolsets placed considerable strain on a supply chain that then focused almost exclusively on 300mm; tool vendors struggled in refurbishment, upgrade, and production of matching tools and processes that performed outside the requirements of traditional semiconductor applications (see Figure 1). Some of these additional requirements — including new and thicker films (>20µm), advanced DRIE (Deep-Reactive-Ion-Etch) capabilities capable of delivering aspect ratios approaching 100:1, and new process capabilities like HFv (Hydrofluoric Acid vapor) release etch and Wafer Bonding — resulted in OEMs needing to restart 200mm tool development. In some cases, OEMS needed to expand their product portfolios to support the growing needs of customers producing devices in the rapidly expanding "More-than-Moore" device segment. Fast forward to 2014 —what a difference approximately seven years has made to the industry segment and more specifically the number of opportunities in the 200mm WFE market for the new class of devices. The surge in mobile device applications and more recently wearable technologies, has meant that device manufacturers are increasingly under pressure to produce cheaper, smaller, more capable and more power efficient devices most economically and efficiently — and this remains optimally on legacy 200mm toolsets. Combining this with the materials and production challenges presented by ultra-high volume applications spelled out in the 'Trillion Sensor Vision' and the now looming IoT (Internet-of-Things) (see Figure 2), and it becomes clear that OEMs who continue to support and develop solutions for the 200mm WFE market have both significant challenges and potential rewards.

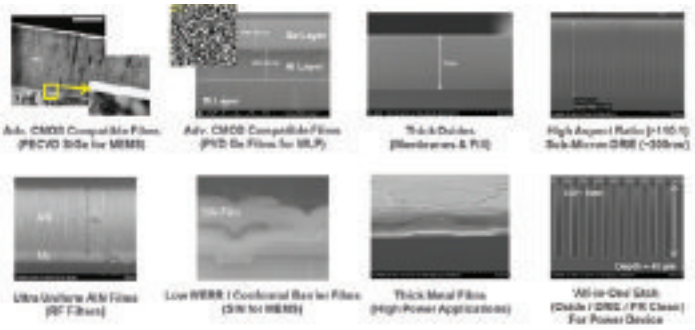


FIGURE 2.

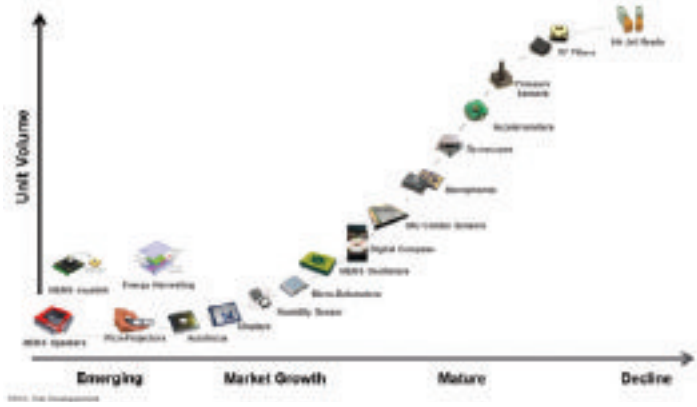


FIGURE 1.

Rising to the challenge presented by the demands of these rapidly growing market segments, Applied Materials is an OEM that has, over the past several years, continued to invest in the R&D of its 200mm portfolio products. Challenged to deliver new materials and processes (see Figure 3) in support the growing class of 200mm emerging technology applications that have come to include MEMS, CIS, Power Device, Analog, WLP (Wafer Level Packaging), TFB (Thin Film Battery), TSV (through-silicon via), etc., Applied Materials believes that working close to the customer and more collaboratively throughout the supply chain is paramount to success in a technically challenging and price sensitive market. The 200mm ecosystem supporting broadly expanding cost-senstive device classes represent a new fork in the roadmap that has been almost myopically focused on Moore's Law evolution.

IEEE Packaging Awards handed out at 2014 ECTC

The 2014 Electronic Component Technology Conference (ECTC) took place in Orlando, Florida. The ECTC is widely regarded as the premier microelectronic packaging conference in the world. This years meeting, headed up by General Chair Wolfgang Sauter (IBM) and Program Chair Alan Huffman (RTI Int) included: 1170 attendees, 369 oral presentations, and 101 exhibitors.

Presentation of IEEE Packaging Awards were made at the IEEE CPMT (Components, Packaging and Manufacturing Technology) Society luncheon at ECTC. Avi

The most prestigious of all awards, the IEEE CPMT "Field Award" went to Dr. Avram Bar-Cohen for "...contributions through leadership, education, and advocacy to thermal design, modeling and analysis of electronic components and for original research on heat transfer and liquid phase cooling." Dr. Bar-Cohen is currently Distinguished Professor of Mechanical Engineering at Maryland and DARPA program manager for their thermal programs known as "ICECool." It is the goal of the "field award" to give them to individuals whose names are synonymous with their field of interest and Avi Bar-Cohen is certainly synonymous with thermal issues in microelectronic packaging.

The Electronics Manufacturing Technology Award went to Dr. Raj Master (Microsoft), the Sustained Technical Contribution award to Prof Madhaven Swaminathan (GaTech), the Exceptional Technical Achievement Award to Prof Pradeep Lall (Auburn) and the David Feldman Outstanding Contribution Award to Prof. SW Ricky Lee (Hong Kong Univ).

2014 iTherm

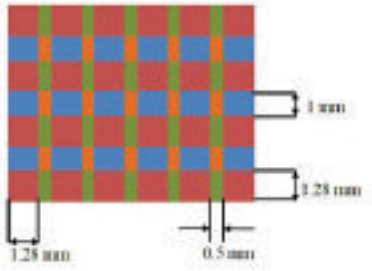
Dr. Phil Garrou,
Contributing Editor

IiTherm is the Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems. The 2014 iTherm was held concurrently with the ECTC in Orlando, FL. This year's General Chair was Mehdi Basheghi of Stanford and program chair was Madhusudan of Google. Attendance this year was up 50% to ~ 400.

Kumari and co-workers at HP addressed "Air Cooling Limits of 3D Stacked Logic Processor and Memory Dies." Their goal was to determine how many memory die can be integrated into a package with logic before exceeding the temp limitations of the memory die. Modeling was done for 10nm technology with 24 cores as shown in **FIGURE 1**. Core power is varied from 1.5 to 3 W (red cores). Stacked memory are 0.5W DRAM.

Oprins and Beyne discussed the "Thermal Modeling of the Impact of 3D Interposer Materials and Thickness on Thermal Performance and Die-to-die Thermal Coupling." For the test vehicle shown in **FIGURE 2**, they observe reducing the thermal conductivity from Si to glass results in an increase in the logic temperature and consequently a lower maximum logic power. The memory temperature at the other hand decreases for decreasing values of the conductivity since the in plane thermal coupling is reduced. This results in an increase of the allowable logic temperature. If the memory heating is included, an increase of the memory temperature can be observed for very low conductivity values.

Most applications for interposers combine high power components (logic) and temperature sensitive components (memory). Since the components are thermally coupled in the package, the logic power will be limited by either the temperature limit of the logic or memory, whichever is reached first. This means there is a trade-off between the logic self-heating and the thermal coupling which are impacted differently by the interposer material and thickness choice. It is shown that the Si interposer has a better thermal performance than the glass interposer in case only the logic temperature limit is taken into account and that the Si interposer package thermally outperforms the single chip package, the package-on-package configuration (PoP) and the 3D stacked configuration. In case the memory temperature limit and self-heating are taken into account as well, the glass interposer package has a better thermal performance for cases where the memory temperature limit memory is sufficiently lower than logic temperature limit. ◆



Tile	Power Map 1	Power Map 2	Power Map 3
Red	1.5	1.5	3
Orange	0.2	0.2	0.2
Green	0.5	0.2	1
Blue	0.2	0.2	0.2

FIGURE 1. Work at HP aimed to determine how many memory die can be integrated into a package with logic before exceeding temperature limitations.

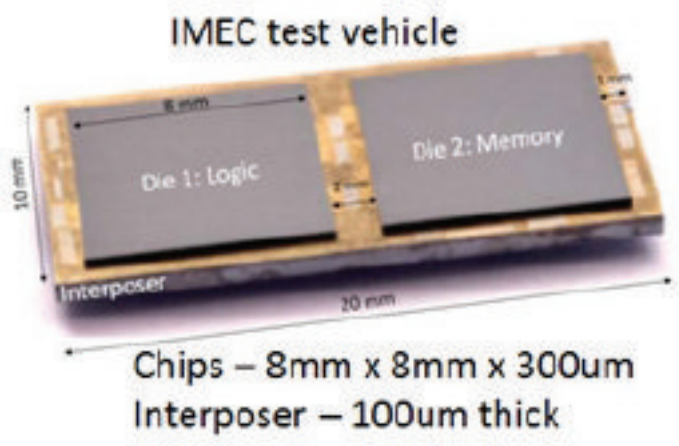


FIGURE 2. imec used this test vehicle to study thermal conductivity.

Packaging

Do we still need Moore's Law?

Shannon Davis,
Web Editor

Many questions were in the air at the 10th annual ConFab 2014, and perhaps one of the most interesting was raised during Dr. Roawen Chen of Qualcomm's opening keynote, "What's On Our Mind" when he asked, "Do we need Moore's Law? Should we pursue it unconditionally?"

The ConFab, held in Las Vegas, NV at The Encore at The Wynn in June brings together over a hundred different top executives and key decision makers in the semiconductor and equipment supplier industries. Throughout the week, The ConFab allows a space for discussion in conference sessions as well as private meetings, allowing for much-needed industry collaboration.

We've often postulated extending Moore's Law. We've even heard that it's already dead. Dr. Chen began his keynote with absolute certainty: "The ride with Moore's Law will eventually end," he said, "but not because of a technical reason, but because of a financial reason."

Dr. Roawen Chen, Senior Vice President of Global Operation at Qualcomm

"I don't think there will be enough volume for 7nm and below to make it a good ROI," he continued. He did, however, say that if EUV was ready tomorrow, it would change his outlook.

Dr. Chen remained quite positive that the semiconductor industry would flourish in spite of this and gave several reasons why this would be the case, chief among them was the growth of mobile applications and the resulting impact on the semiconductor industry. "Not everything demands Moore's Law," he said. "A lot of future, killer apps don't need leading edge. You don't need to migrate everything to leading edge."

Given the current and growing complexity of consumer devices, in particular mobile, the need for new innovation and packaging solutions is bigger than ever, Dr. Chen explained. "Innovation always wins," he said. "We've been using the same playbook for many, many years. We have to adapt to the new reality."

Ten years ago, he said, the enterprise was predictable and stable. PCs were the biggest semiconductor consumer – volume was higher, but seasonal. Smartphones, however, have become a lifestyle statement product, not just an IT device, and the demand has become more volatile.

Another change the semiconductor industry must adapt to is a new set of key industry drivers. The PC industry was driven by computing hardware, whereas the mobile ecosystem is driven by smartphone consumer data, not processing power, he explained. Surviving in a post-Moore's Law world requires deriving value from downstream in the semiconductor ecosystem. Deeper collaboration within the supply chain is more necessary than ever before, Dr. Chen explained.

"The bull whip effect is also more pronounced in the mobile era," said Dr. Chen, "and volatile customer demand amplifies the effect further up the supply chain." He also recommended a roadmap exchange on technology and manufacturing readiness.

Ultimately, while he has heard many in the industry sound apocalyptic-esque warnings, he and his Qualcomm colleagues remain optimistic. "'The end is near'? I don't believe so," he said. "There is still plenty of opportunity for new innovation." ◆

Semiconductors

Fusion bonding for next-generation 3D-ICs

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Recent developments in wafer bonding technology have demonstrated the ability to achieve improved bond alignment accuracy.

Scaling and Moore's law have been the economic drivers in the planar silicon arena for the last 30 years. During that period, major technology evolutions have been implemented in CMOS processing. The most recent of these evolutions have been extremely complex, including multiple-step lithographic patterning, new strain enhancing materials and metal oxide gate dielectrics. Despite these great feats of engineering and material science, the often predicted "red brick wall" is once again fast approaching and requires evasive action. In fact, several semiconductor suppliers have already shown that the "economic" brick wall has arrived at the 22nm node, where scaling can no longer decrease the cost per transistor [1]. Solutions are getting more difficult to track down in an industry driven by increasing performance at lower cost. 3D-IC integration provides a path to continue to meet the performance/cost demands of next-generation devices while avoiding the need for further lithographic scaling, which requires both increasingly complex and costly lithography equipment as well as more patterning steps. 3D-IC integration, on the other hand, allows the industry to increase chip performance while remaining at more relaxed gate lengths with less process complexity—without necessarily adding cost [1].

While the initial outlook on 3D-IC integration was initially misty, several paths to integration have since been identified, giving an unobscured view to the future in the third dimension [2]. The current state of 3D-IC integration is analogous to crossing the Alps. There are different options to get over the mountain range: by smart use of the valleys, more dangerous direct ascent and descent, or by the brute force of tunneling through. In the end, the most economic routes are combinations of all these factors. In 3D-ICs we see a similar process occurring now. Some 3D devices are established in the middle of the fabrication process, referred as mid-end-of-line (MEOL), while some are established using chip stacking at the back-end-of-line (BEOL). In the future, some 3D stacking will be pulled upstream into the front-end-of-line (FEOL). Which integration scheme will be adopted by a manufacturer depends mainly on the target device, market size and compatibility of processes. The most cost-effective approach to 3D-IC integration should be a combination of all three integration schemes. That said, for many applications 3D-IC integration in FEOL processing offers further potential to pave the way for cost reduction, performance increase and higher-power efficiency.

Front-end processing is still seen as a purely planar-based process, where the power/performance of the device comes from the silicon. However, many disruptive processes and materials, such as SiGe

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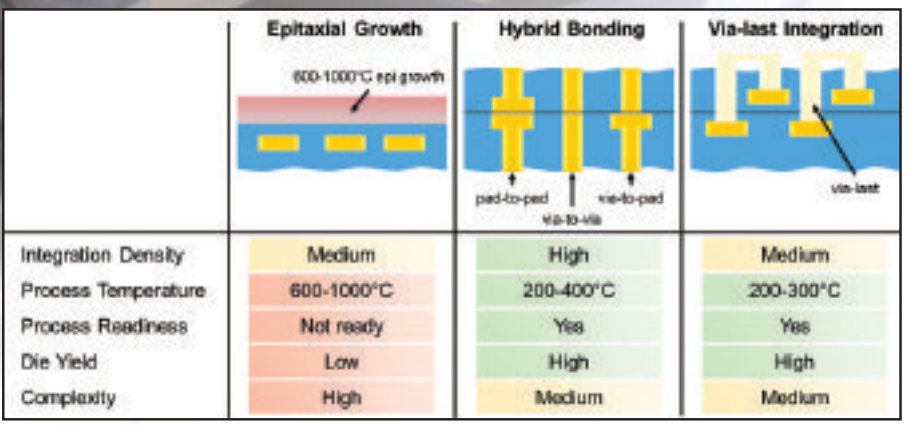

	Epitaxial Growth	Hybrid Bonding	Via-last Integration
Integration Density	Medium	High	Medium
Process Temperature	600-1000°C	200-400°C	200-300°C
Process Readiness	Not ready	Yes	Yes
Die Yield	Low	High	High
Complexity	High	Medium	Medium

FIGURE 1. Comparison of different 3D front-end-of-line integration schemes.

and other epitaxial layers, have already been implemented to enable device improvements. As a result, the boundary between planar and 3D stacking has already softened and paves the way for heterogeneous integration (e.g., memory on memory, memory on logic, etc.) to become prevalent going forward [3].

FIGURE 1 provides an overview of different 3D integration process schemes at FEOL. The first integration scheme being considered is layer-by-layer epitaxial growth, which has been a standard process for the semiconductor industry for the last 20 years. However, current epitaxy temperatures, which are in excess of 600-1000°C, make epi not a viable option for 3D integration today, since metal diffusion and broadening dopant distribution of the functional substrate wafer caused by these extreme temperatures would destroy the underlying IC layer. A second integration method is hybrid bonding, whereby a dual damascene copper and silicon oxide hybrid interface serves as both the full-area bonding mechanism and the electrical connection. A third route for 3D integration is the transfer of a thin processed semiconductor layer (ranging from tens to a few hundred nanometers in thickness) using a full-area dielectric bond. In contrast to hybrid bonding, the electrical connection is introduced by a via-last process between early interconnect metal levels on the bottom wafer and the second transferred transistor layer.

Both hybrid bonding and full-area dielectric bonding can be achieved through aligned wafer-to-wafer fusion bonding. However, high-interconnect density along with small routing dimensions set a high bar for bond alignment precision, which is necessary for fusion bonding. Fusion bonding is a two-step process consisting of 1) room-temperature pre-bonding and 2) a high-temperature annealing step. This essentially relates to the chemical bonds at interface. While pre-bonding is based on hydrogen bridges, thermal annealing facilitates the formation of covalent bonds.

An important benefit of fusion bonding is the widespread availability of bonding materials. Any exotic or novel material suffers a high barrier to adoption in the semiconductor industry, in part because it must comply with many different specifications and requires lengthy and extensive failure analysis to ensure no negative impacts are introduced across the entire chip process. With fusion bonding, however, all integration schemes rely on silicon oxide, silicon nitride or oxy-nitrides as dielectric bonding materials, and copper or other interconnect metals—all of which are standard in state-of-the-art IC production lines.

Early on, successful fusion bonding required that the bonding material be transformed into a viscous flow, which required extremely high temperatures (ranging from 800°C to 1100°C depending on doping as well as deposition method) [4]. However, major research has been and continues to be invested in interface physics and morphology prior to bonding and their effect on the bonding result. Recent efforts in low-temperature plasma activation bonding have enabled a reduction of the thermal annealing temperature to about 200°C and opened up the possibility for further material combinations [5,6]. In fact, fusion bonding is already being implemented in high-volume production for certain applications, including image sensors and engineered substrates, such as silicon-on-insulator (SOI) wafers. In the case of wafer-to-wafer fusion bonding, the process can readily being introduced into the CMOS process flow, which uses low-k dielectrics and standard metals.

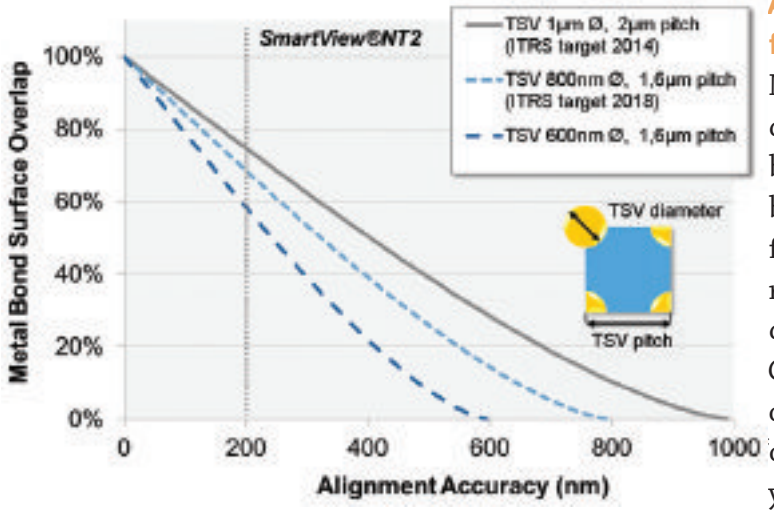

FIGURE 2. Calculated surface overlap of metal TSVs for hybrid bonding as a function of wafer-to-wafer alignment accuracy. Comparison of ITRS roadmap relevant TSV pitches and diameters reveal, alignment accuracy of better than 200nm (3σ) is needed to achieve 60% and more TSV overlap for hybrid bonding.

Alignment is key for fusion-bonded 3D-ICs

Minimizing the via dimension for via-last bonding, or the via and bonding pad dimensions for hybrid bonding, are key requirements for bringing down the cost of 3D devices. Considering that the role of a TSV is essentially only" for signal connection yet consumes valuable wafer real estate, further miniaturization has to be the logical consequence. Increasing integration density is a means of regaining valuable active device area. However, a direct consequence of smaller interconnect structures is the need for improved wafer-to-wafer alignment.

As indicated in the cross section of **FIGURE 1** for via-last processing after semiconductor layer stacking, lithographic etch masks for the vias need to be aligned to the buried metal layers. Bonding alignment is also key here, since the resist layer must match with contacts on both the bottom and top device layers. In order to minimize loss of silicon real-estate and maintain small wiring exclusion zones, the bond alignment must be within tight specifications and adapt to metal, via and contact nodes, as shown in **FIGURE 2**.

The semiconductor world would be easy if devices

operated at a constant voltage. However, a major concern with 3D-IC/through-silicon via (TSV) integration is the potential introduction of high-frequency response and parasitic effects. Again, bond alignment is of major importance here. Any via within the interconnection network will generate a certain electric field around it. Perfect alignment between individual interconnect layers results in a symmetric electric field, whereas misalignment can cause a local enhancement of the electric field. This in turn can result in an electric field imbalance. Further scaling of interconnects and pitch reduction between vias means that inhomogeneous electric fields gain importance. Memory stacking and high-bandwidth interfaces with massively parallelized signal buses are particularly sensitive to this issue [2].

bonding [7]. The newly introduced SmartView®NT2 bond aligner has demonstrated the ability to achieve face-to-face alignment within 200nm (3σ), as shown in **FIGURE 3**.

Several factors contribute to the global alignment of the wafers besides the in-plane measurement and placement of the wafers relative to each other. In fusion bonding, both wafers are aligned and a pre-bond is initiated. When bringing the device wafers together, wafer stress and/or bow can

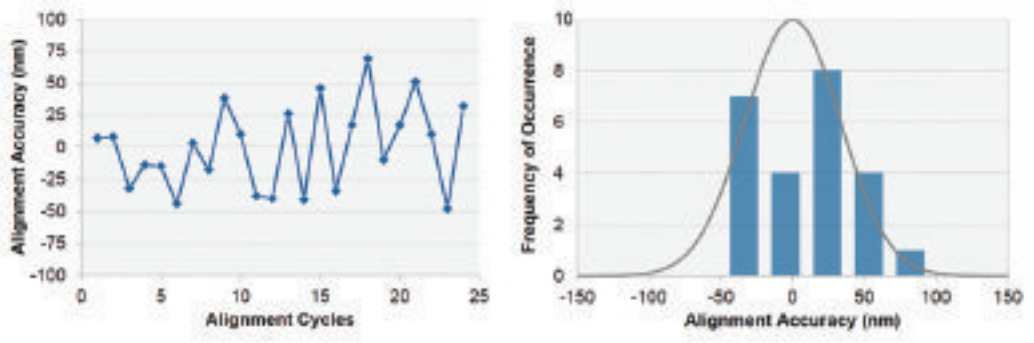

FIGURE 3. SmartView®NT2 alignment data for consecutive alignments (left), revealing an alignment accuracy of 200nm (3σ) from the histogram and corresponding normal distribution (right).

Optimizing alignment values

From the above discussion, it becomes clear that wafer-to-wafer alignment accuracy for fusion bonding has to be in line with interconnect scaling. The 2011 edition of the International Technology Roadmap for Semiconductors (ITRS) roadmap (at the time of writing this article, the Assembly and Packaging section of the 2013 ITRS Roadmap has not yet been published) specified that for high-density TSV applications, the diameter of vias will be in the range of 0.8-1.5 µm in 2015 [2], which requires an alignment accuracy of 500nm (3σ) in order to establish a good electrical connection. Previous studies have demonstrated that alternative wafer-to-wafer alignment approaches can achieve a post-bond alignment accuracy of better than 250nm for oxide-oxide fusion

influence the formation of a bond wave. The bond wave describes the front where hydrogen bridge bonds are formed to pre-bond the wafers. Controlling the continuous wave formation and controlling influencing parameters is key to achieving the tight alignment specifications noted above. In essence, optimizing a fusion bonding process means that one must optimize the force generated during the bonding.

For example, bowing and warping of processed wafers can be substantial after via etching and filling. TSVs in particular represent local strain centers on a wafer. Minimizing the via size and depth helps to reduce the strain, which heavily influences the shape and travel of the bond wave. At the same time, this bond wave also causes local strain while running through the bonding interface. Any wafer strain manifests in distortion of the wafer, which leads to an additional alignment shift. Process and tool optimization can minimize strain and significantly reduce local stress patterns. Typically, distortion values in production are well below 50nm. Indeed, further optimization of distortion values is a combination of many factors, including not only the bonding process and equipment, but also previous manufacturing steps and the pattern design. To a large extent, plasma activation also determines initial bonding energies, which impact the travel and formation dynamics of the bond wave and consequently wafer distortion.

Conclusion

In summary, aligned fusion wafer bonding is progressing rapidly to support front-end 3D-IC stacking. However, wafer bonding alignment accuracy must improve in order to meet the production requirements for both current and future design nodes. Controlling the local alignment of the wafers is only one aspect. Other important aspects include the initiation, manipulation and control of the bond wave. Recent developments in wafer bonding technology have demonstrated the ability to achieve bond alignment accuracy of 200nm (3σ) or less, which is needed to support the production of the next generation of 3D-ICs.

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Can lean innovation bring growth and profits back to semiconductors?

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New approaches to start-ups can unlock mega-trend opportunities.

The semiconductor industry returned growth and reached record revenues in 2013, breaking $300 billion for the first time after the industry had contracted in 2011 and 2012 (**FIGURE 1**).

FIGURE 1. Worldwide semiconductor revenue. Source: World Semiconductor Trade Statistics, February 2014.

However, even with that return to growth, underlying trends in the semiconductor industry are disturbing: The semiconductor cycle continues its gyrations, but overall growth is slowing. And despite 5% year-on-year revenue growth in 2013 (the highest since 2010), the expectation is that semiconductor growth will likely continue to be at a rate below its long-term trend of 8 to 10% for the next three to five years (**FIGURE 2**).

FIGURE 2. Semiconductor revenue growth. Sources: Semiconductor Industry Association and AlixPartners research.

An AlixPartners 2014 publication , Cashing In with Chips, showed that semiconductor industry growth had slowed to roughly half of its long-term growth average since the 2010 recovery—with no expectation that it will return to historical growth until at least 2017. Other studies have also shown that semiconductor growth has slowed not only relative to its previous performance but also versus growth in other industries. And a study conducted by New York University's Stern School of Business[1] found that the semiconductor industry's revenue growth lagged the average revenue growth of all industries and ranked 60th out of 94 industries surveyed. Surprisingly, the industry's net income growth of semiconductor companies lagged even further behind—ranking 84th out of 94 companies surveyed—and had actually been negative during the previous five years.

In another study released by AlixPartners that looked at a broader picture of the semiconductor

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value chain , including areas such as equipment suppliers and packaging and test companies, the research showed that outside of the top 5 companies, the remainder of the 186 companies surveyed had declining earnings before interest, taxes, depreciation, and amortization (**FIGURE 3**).

As revenue growth slows, costs increase at a rapid rate

As semiconductor technology advances, the cost of developing a system on chip (SoC) has risen dramatically for leading-edge process technologies. Semico Research has estimated that the total cost of an SoC development, design, intellectual property (IP) procurement, software, testing has tripled from 40/45 nanometers (nm) to 20 nm and could exceed $250 million for future 10-nm designs (**FIGURE 4**) [2]. This does not bode well for an economic progression of Moore's law, and it means that very few applications will have the volume and pricing power to afford such outlandish investment. If we assume that a 28-nm SoC can achieve a 20% market share and 50% gross margins, the end market would have to be worth over $1 billion to recoup R&D costs of $100 million. By 10 nm, end markets would have to result in more than $2.5 billion to recoup projected development costs. With few end markets capable of supporting that high a level of development costs, the number of companies willing to invest in SoCs on the leading edge will likely decline significantly each generation .

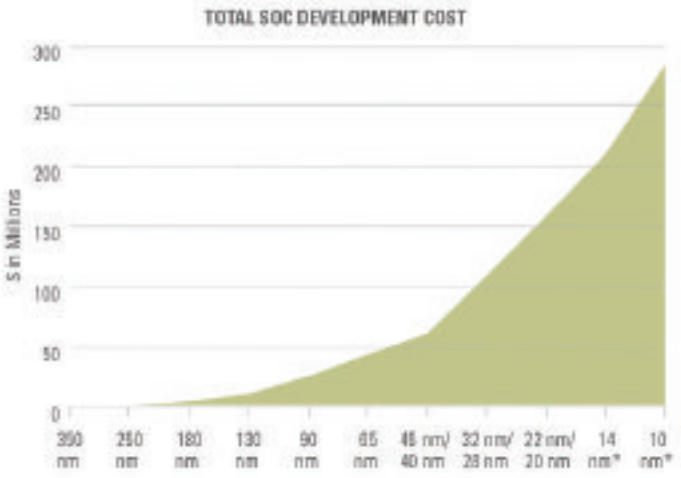

FIGURE 4. Development Costs are Skyrocketing. Source: Semico Research Corp.

	TOTAL	TOP 5	TOP 5 (% TOTAL)	OTHER 186
Revenue ($ billions)	407	112	28%	294
Revenue (year over year)	-3.4%	6.2%	—	-6.6%
EBITDA ($ millions)	90	46	51%	44
EBITDA (year over year)	-14.3%	1.2%	—	-26.3%
EBITDA (% of revenue)	22%	41%	—	15%

FIGURE 3. Spotlight on the top five (fiscal year 2012). Source: AlixPartners Research.

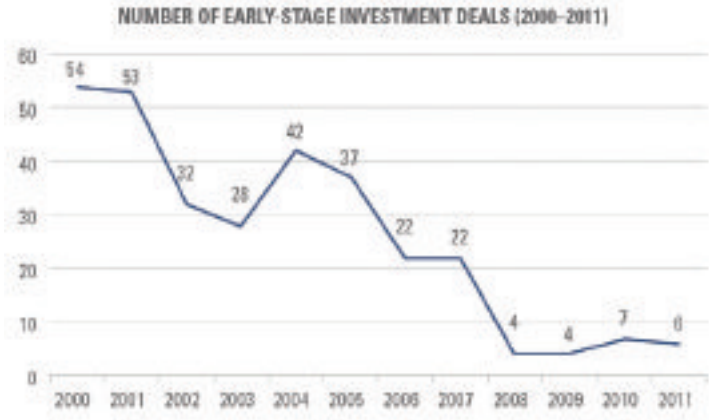

FIGURE 5. Number of seed/series a deals. Source: Global Semiconductor Alliance.

What happened to semiconductor start-ups?

The history of the semiconductor industry has been shaped by the semiconductor start-up. Going back to Fairchild, the start-up has been the driving force for growth and innovation.

Start-ups helped shape the industry, and they are now some of the largest and most successful companies in the industry.

But the environment that lasted from the 1960s until the early 2000s—and that made the success of those companies possible—has changed dramatically. The number of venture capital investments in new semiconductor start-ups in the United States has fallen dramatically, from 50 per year to the low single digits (**FIGURE 5**). And even though that drop is not as dramatic in

other countries—such as China and Israel—it is indicative of an overall lack of investment in semiconductors .

The main reason for the decline is the attractiveness of other businesses for the same investment. In the fourth quarter of 2013, nearly 400 software start-ups received almost $3 billion of funding, whereas only 25 semiconductor start-ups received just $178 million (representing all stages) (**FIGURE 6**). It seems that (1) the lower cost of starting a software company, (2) the relatively short time frame to realize revenue, and (3) attractive initial-public-offering and acquisition markets possibly make the software start-up segment more interesting than semiconductors .

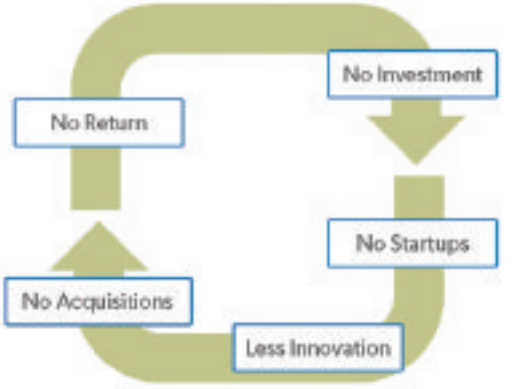

FIGURE 7. A vicious cycle limits innovation. .

This situation is unfortunate and has conspired to create a vicious and downward cycle (**FIGURE 7**) .

- Lack of investment limits start-ups.
- Lack of start-ups limits innovation.
- Less innovation and fewer start-ups reduce the number of potential acquisition targets for established companies.
- Reduced potential acquisition targets in turn limit returns for companies and returns for those who would have invested in start-ups.

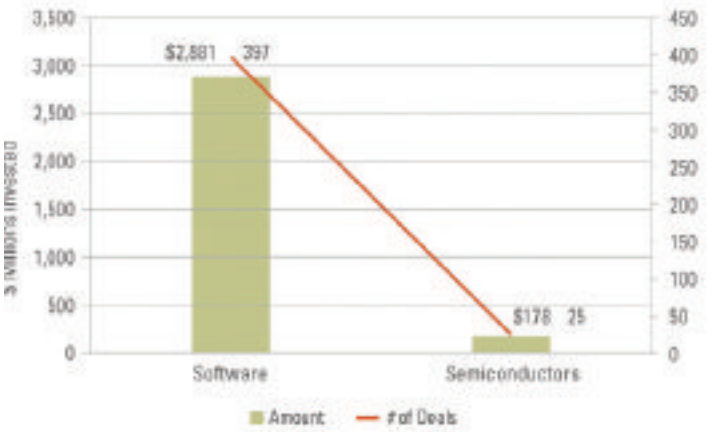

FIGURE 6. Funding of software and semiconductor start-ups. Source: PwC, US Investments by Industry/Q4 2013.

- Limited returns make future investments less likely and continue the cycle of less innovation and lower investment [3].

Therefore, it is reasonable to conclude that the demise of semiconductor start-ups is a contributing cause to the lackluster results of the overall semiconductor industry. And that demise and those lackluster results are further exacerbated by the rise of activist shareholders who demand a more rapid return on their investment, which possibly reduces the potential for innovation in an industry that has lengthy development cycles.

What about other industries?

It is tempting to think that the semiconductor industry is alone in this predicament, but other

industries face similar challenges and have figured out accretive paths forward. For example, biotechnology has some of the same issues:

- An industry that grows by bringing innovation to market
- Similarly lengthy development cycles
- Potentially capital intensive at the research and production stages

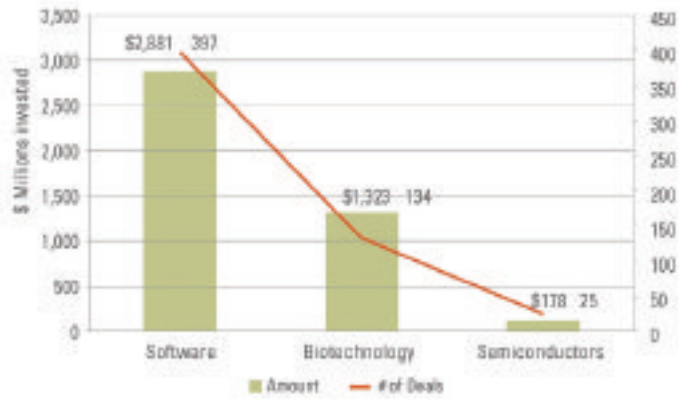

FIGURE 8. Funding of software and semiconductor start-ups. Source: PwC, US Investments by Industry/Q4 2013.

In addition, the biotech industry faces a challenge the semiconductor world does not—namely, the need for government regulatory approval before moving to production and then volume sales. Gaining that regulatory approval is a go-to-market hurdle that can add years and uncertainty to a product cycle.

However, in spite of its similarities to the semiconductor business and the added regulatory hurdles, the biotech industry enjoys a very healthy venture-funding and start-up environment. In fact, in the fourth quarter of 2013 in the United States, biotech was the second-largest business sector for venture funding in both dollars and total number of deals (**FIGURE 8**).

Why is this? What do biotech executives, entrepreneurs, and investors know that the semiconductor industry can take advantage of? There are several lessons to be learned.

- Big biotech companies have made investing, cultivating, and acquiring start-ups key parts of their innovation and product development processes.
- Biotech strategic and venture investors identify interesting problems to solve and then match the problems to skilled and passionate entrepreneurs to solve them.
- Those entrepreneurs are motivated to create and develop solutions much faster and usually more frugally than if they were working inside a large company.
- The entrepreneurs and investors are creating businesses to be acquired versus creating businesses that will rival major industry players.
- The acquiring companies apply their manufacturing economies of scale and well-established sales and marketing strategies to rapidly—and profitably—bring the newly acquired solutions to market.

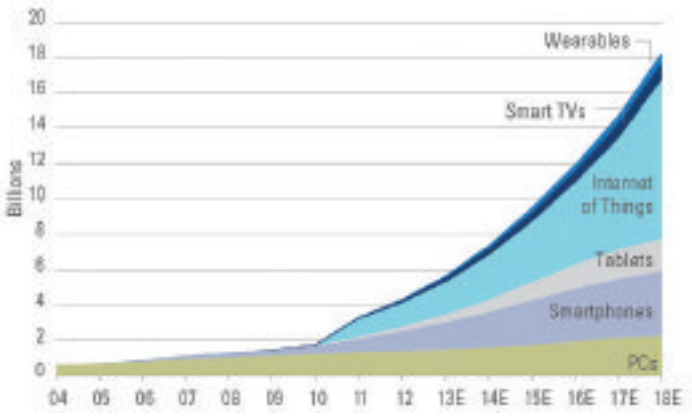

FIGURE 9. Global internet device installed base forecast. Sources: Gartner, IDC, Strategy Analytics, Machina Research, company filings, BII estimates.

This is the most exciting time to be in the semiconductor business

For several reasons, certain megatrends are driving the high-technology sector and the economy as a whole, and all of them are enabled by semiconductor innovation (**FIGURE 9**). Among the major trends:

- Mobile computing will likely continue to merge functions and drive computing power.
- Security concerns appear to be increasing at all levels: government, enterprise, and personal.
- Cloud computing will possibly cause an upheaval in information technology.
- Personalization through technology and logistics appears to be on the rise.
- Energy efficiency is likely needed for sustainability and lower cost of ownership.

- Next-generation wireless will likely be driven by insatiable coverage and bandwidth needs.
- The Internet of Things will likely lead to mobile processing at low power with ubiquitous radio frequency.

The Internet of Things megatrend alone will result in a tremendous amount of new semiconductor innovation that in turn will likely lead to volume markets. Cisco Systems CEO John Chambers has predicted a $19-trillion market by 2020 resulting from Internet of Things applications [4].

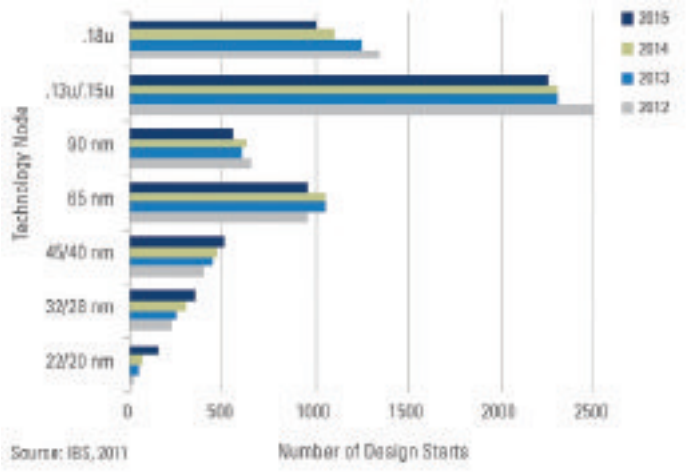

FIGURE 10. .13µm has the most design starts; 65 nm and 45 nm have yet to peak.

Does it really cost $100 million to start a semiconductor company?

The prevailing conventional wisdom is that it takes $100 million to start a new semiconductor company, and in some cases that covers only the cost of a silicon development. It is true that recently, several companies have spent eight- or nine-figure sums of money to develop their products, but those are very much exceptions. The reality is that most semiconductor development is not at the bleeding edge, nor is the development of billion-transistor SoCs.

The majority of design starts in 2013 were in .13 µm, and this year, 65, 55, 45, and 40 nm are all growing (**FIGURE 10**). These technologies are becoming very affordable as they mature. And costs will likely continue to decrease as more capacity becomes available once new companies enter the foundry business and as former DRAM vendors in Taiwan and new fab in China come online .

Another thing to consider is whether a new company would sell solutions that use existing technology or platforms (i.e., a chipless start-up) or whether a company would choose to originate IP that enables functionality for incorporation into another integrated circuit.

A chipless start-up would add value to an existing architecture or platform. It could be an algorithm or an application-specific solution on, say, a field-programmable gate array, a microcontroller unit or an application-specific standard product. It could also be service based on an existing hardware platform.

A company developing innovative new functionality for inclusion into another SoC paves a path to getting to revenue quickly. Such IP solution providers would supply functionality for integration not only into a larger SoC but also into the emerging market for 2.5-D and 3-D applications.

In both situations (the chipless start-up and the IP provider), significant cost may be avoided by the use of existing technology or the absence of the need to build infrastructure or capabilities already provided by partners. In addition, those paths have much faster times to revenue as well as inherently lower burn rates, which are conducive to higher returns for investors.

Even for start-ups that intend to develop leading-edge multicore SoCs, a $100-million investment is not inevitable. Take, for example, Adapteva, an innovative start-up in Lexington, Massachusetts. Founded by Andreas Olofsson, Adapteva has developed a 64-core parallel processing solution in 28 nm. The processor is the highest gigaflops/watt solution available today, beating solutions from much larger and more-established companies. However, Adapteva has raised only about $5 million to date, a good portion of which funding was crowd sourced on the Kickstarter Web site. This just shows that even a leading-edge multicore SoC can be developed cost-effectively—and effectively—through the use of multiproject wafers and other frugal methods.

Conclusions

Several conclusions can be drawn at this point.

- Even though the semiconductor industry is growing again, the underlying trends for profitability and growth are not encouraging.
- Cost of development is increasing rapidly on leading-edge SoCs.
- Historically, start-ups have been engines of innovation of growth and innovation for semiconductors.
- In recent years, venture funding for new semiconductor companies has almost completely dried up.
- That lack of investment in semiconductor start-ups has contributed to a downward and vicious cycle that will further erode the economics of semiconductor companies.
- The biotechnology industry has many parallels to the semiconductor. Interestingly, biotechnology has a relatively thriving venture funding and start-up environment, and we can apply that industry's successful approach to semiconductors.
- Despite the state of start-ups, it is now one of the most exciting times to be in semiconductors because most of the megatrends driving the economy are either enabled by or dependent on semiconductor innovation.
- It does not need to take $100 million to start the typical semiconductor company, because a great deal of innovation will use very affordable technologies, and come from chipless start-ups or IP providers that have much lower burn rates and ties to revenue.
- Even leading-edge multicore SoCs can be developed frugally (for single-digit millions of dollars) and profitably.

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Cryogenic etching reduces plasma-induced damage of ultralow-k dielectrics

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Reducing plasma-induced damage is key to advancing the scaling limits.

As semiconductor technology scales below the 20nm node, the capacitance between nearby metal lines increases and this results in loss of speed and cross-talk of the device. To control this unwanted increase in capacitance, insulating layers of porous low-k dielectrics are integrated through plasma etching. Porous organosilicate glasses (or OSGs) are the most popular dielectric materials, but their integration is very challenging. During plasma processing (such as patterning, surface cleaning and resist strip), the porous low-k material suffers from plasma-induced damage which degrades its k value and causes high leakage currents. The damage occurs through depletion of the methyl groups (Si-CH_3) which are very sensitive to the active species (radicals, ions and photons) present in the plasma.

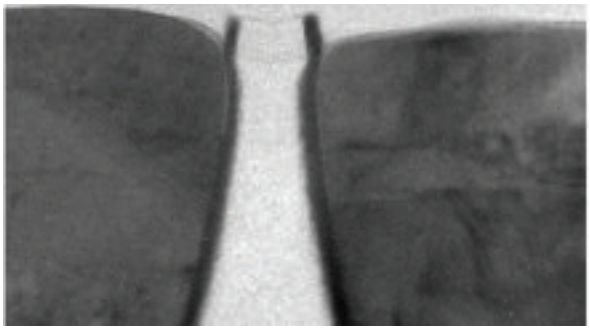

FIGURE 1. X-TEM picture of a cryo-etch damascene structure.

A new cryogenic etch method

To bypass these damages, imec researchers have developed a cryogenic low-k etching method. By applying cryogenic temperatures (below -70°C), etch-by products condense and seal the open pores against radical diffusion. Cryogenic etching allows IC manufacturers to reach scaling levels of 20nm and beyond, without compromising speed and device cross-talk. The new method is a good alternative to pore stuffing by sacrificial polymers, which today is intensively studied as a possible way of reducing plasma damage. Pore stuffing is certainly interesting, but has several challenges, namely its impact on the process flow and the possible deformation of the low-k film.

Setting up the experiments

Damage reduction by cryogenic etching was studied in more detail by applying the new method to different OSG films (different dielectric constants and pore structures), and by using different temperatures and etching chemistries. The researchers used a plasma-enhanced chemical vapor deposited (PECVD) OSG-2.0 material with a

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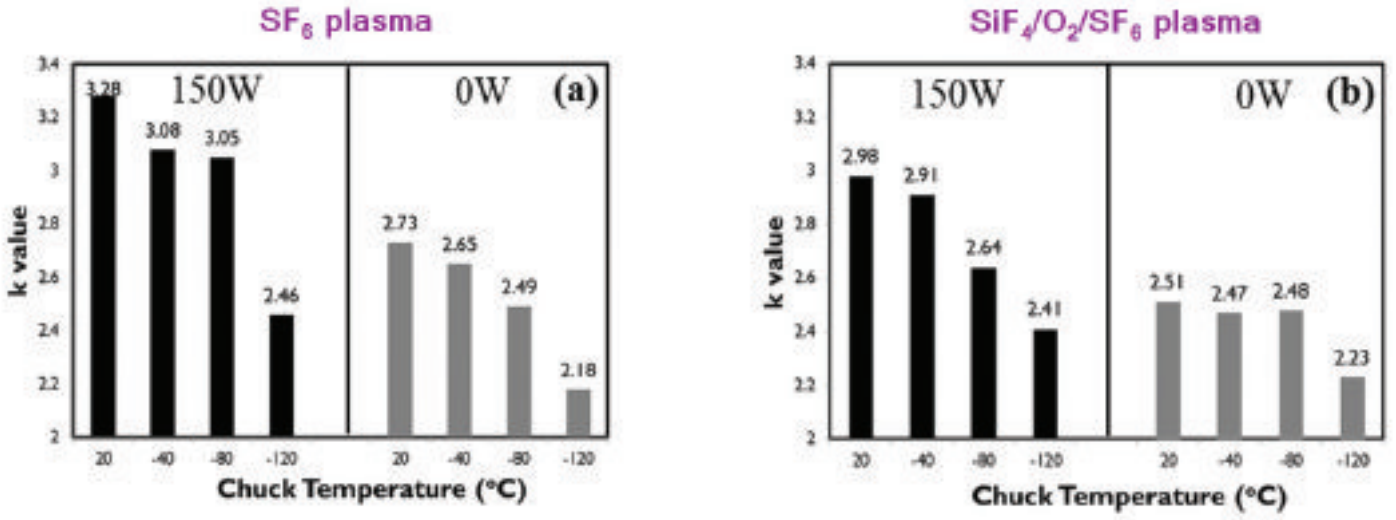

FIGURE 2. k value (at 100MHz) extracted from capacitance measurements for OSG-2.0 films etched by pure SF_6 plasma (a) and $SiF_4/O_2/SF_6$ plasma (b) at different substrate holder temperatures. Black bars represent the recipe with high bias power to simulate bottom etching, gray bars represent the recipe with 0W bias power to simulate sidewall condition. These results confirm the reduced dielectric degradation at cryogenic temperatures.

k value of 2.05 (referred to as ALKB), and a spin-on deposited OSG-2.3 material with a k value of about 2.3 (referred to as NCS). In the experiments, the temperature of the wafer could be varied between -150°C and 40°C by using a liquid nitrogen circulation system and a heating element. Different etching gasses were used, namely SF_6, SiF_4, O_2 and mixtures of these gasses. They used zero bias power to simulate the etching condition along the trench sidewall, and 150W bias power to gain information on the trench bottom.

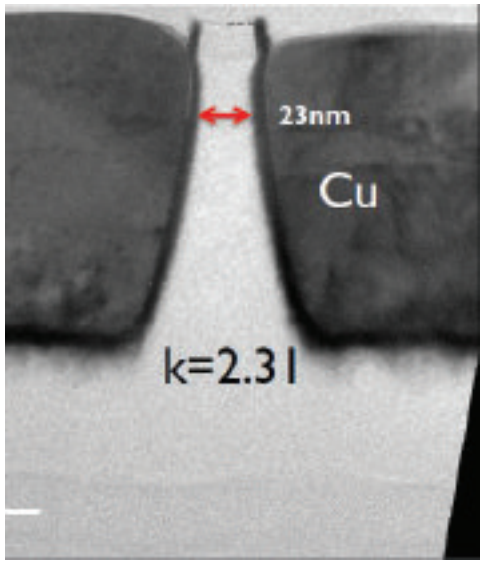

FIGURE 3. Cross-section transmission electron microscopy (X-TEM) image of a cryo-etch damascene structure. The integrated k value was measured to be 2.38, while the pristine k value was 2.31. The resulting Delta-k is 0.07, which is the lowest Delta-k that has ever been achieved for ultralow-k materials.

Outcome and protection mechanism

When a SF_6 plasma was used, almost no methyl groups depletion (visible as a smaller decrease of the Si-CH_3 peaks) was observed when the wafer temperature was below a certain critical level. This observation holds for both bias conditions, and is a first indication of a lower plasma-induced damage. Further investigations reveal that alcohol-like etch by-products are formed at cryogenic temperatures. These reaction products retard the oxidation of the methyl groups, condense on the low-k surface, diffuse into the pores and fill the interconnected pores. These deposited etch by-products protect the low-k films from plasma damage. The etch condensate remains at room temperature, and can be easily removed by high temperature annealing without additional damage to the low-k material. K-value extraction based on capacitance measurements confirms the reduced dielectric degradation at cryogenic temperatures. The plasma-induced damage can even be further reduced by adding SiF4 and O_2 into the gas discharge. When using this $SiF_4/O_2/SF_6$ gas mixture, an additional SiOxFy-like passivation layer is deposited which can efficiently protect the dielectric surface.

A threshold temperature, depending on pore size and porosity

The researchers also found that these phenomena occur below a critical wafer temperature and that this temperature depends on the porosity and pore size of the low-k material. While for the ALKB material (open porosity 46% and pore diameter 3.0nm), carbon depletion is suppressed at temperatures lower than -70°C, a temperature lower than -120°C is needed to suppress carbon depletion within the NCS material (open porosity 35% and pore diameter 2.0nm). This dependence is explained by the Kelvin equation predicting that the vapor condensation in pores happens at critical relative pressures which depend on the pore size.

Pattern transfer and future outlook

We are currently developing a modified approach, in which initial reactants are condensed instead of etch by-products. First results are very promising for industrial take up, since etch temperatures can be increased up to -50°C.

Also, the pattern transfer capabilities of cryogenic etching are being investigated. This includes a study of the mechanism of hard-mask preservation at cryogenic temperatures. The final goal is an accurate and complete pattern transfer, up to the bottom of the OSG film.

Acknowledgement

It is our great pleasure to thank our colleagues from GREMI Orleans (France) and Oxford Instruments (UK) for the joint experiments and for the possibility to use their cryogenic etch equipment.

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3D memory for future nanoelectronic systems

ED KORCZYNSKI, *Senior Technical Editor*

Bit-growth slows while specialized stacking accelerates innovation in future memory solutions for communications, energy, and health-care.

The future of 3D memory will be in application-specific packages and systems. That is how innovation continues when simple 2D scaling reaches atomic-limits, and deep work on applications is now part of what global research and development (R&D) consortium Imec does. Imec is now 30 years old, and the annual Imec Technology Forum held in the first week of June in Brussels, Belgium included fun birthday celebrations and very serious discussions of the detailed R&D needed to push nanoelectronics systems into health-care, energy, and communications markets.

3D memory will generally cost more than 2D memory, so generally a system must demand high speed or small size to mandate 3D. Communications devices and cloud servers need high speed memory. Mobile and portable personalized health monitors need low power memory. In most cases, the optimum solution does not necessarily need more bits, but perhaps faster bits or more reliable bits. This is why the Hybrid Memory Cube (HMC) provides >160Gb/sec data transfer with Through-Silicon Vias (TSV) through 3D stacked DRAM layers.

"We're not adding 70-80% more bits like we used to per generation, or even the 40% recently," explained Mark Durcan, chief executive officer of Micron Technology. "DRAM bits will only grow at the low to mid-20%." With those numbers come hopes of more stability and less volatility in the DRAM business. Likewise, despite the bit growth rates of the recent past, NAND is moving to 30-40% bit-increase per new 'generation.'

"Moore's Law is not over, it's just slowing," declared Durcan. "With NAND we're moving from planar to 3D, and the innovation is that there are different ways of doing 3D." **FIGURE 1** shows the six different options that Micron defines for 3D NAND. Micron plans for future success in the memory business to be not just about bit-growth, but about application-specific memory solutions.

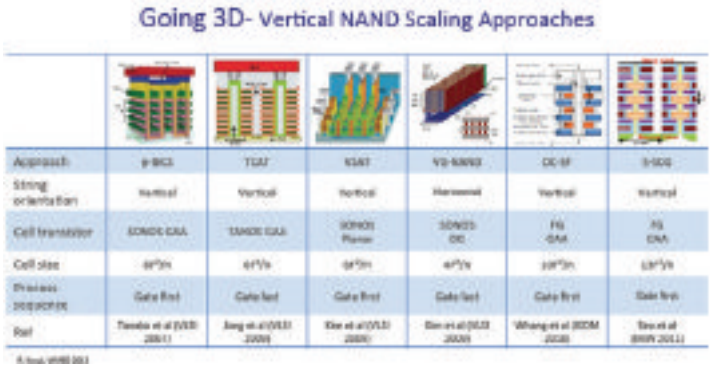

FIGURE 1. Different options for Vertical NAND (VNAND) Flash memory design, showing cell layouts and key specifications. (Source: Micron Technology)

E. S. Jung, executive vice president Samsung Electronics, presented an overview of how "Samsung's Breaking the Limits of Semiconductor Technology for the Future" at the Imec forum. Samsung Semiconductor announced it's first DRAM product in 1984, and has been improving it's capabilities in design and manufacturing ever since. Samsung also sees the future of memory chips as part of application-specific

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systems, and suggests that all of the innovation in end-products we envision for the future cannot occur without semiconductor memory.

Samsung's world leading 3D vertical-NAND (VNAND) chips are based on simultaneous innovation in three different aspects of materials and design:

1) Material changed from floating-gate,
2) Rotated structure from horizontal to vertical (and use Gate All Around), and
3) Stacked layers.

To accomplish these results, partners were needed from OEM and specialty-materials suppliers during the R&D of the special new hard-mask process needed to be able to form 2.5B vias with extremely high aspect-ratios.

Rick Gottscho, executive vice president of the global products group Lam Research Corp., in an exclusive interview with SST/SemiMD, explained that with proper control of hardmask deposition and etch processes the inherent line-edge-roughness (LER) of photoresist (PR) can be reduced. This sort of integrated process module can be developed independently by an OEM like Lam Research, but proving it in a device structure with other complex materials interactions requires collaboration with other leading researchers, and so Lam Research is now part of a new "Supplier Hub" relationship at Imec.

Luc Van den hove, president and chief executive officer of Imec, commented, "we have been working with equipment and materials suppliers form the beginning, but we're upgrading into this new 'Supplier Hub.' In the past most of the development occurred at the suppliers' facilities and then results moved to Imec. Last year we announced a new joint 'patterning center' with ASML, and they're transferring about one hundred people from Leuven. Today we announced a major collaboration with Lam Research. This is not a new relationship, since we've been working with Lam for over 20 years, but we're stepping it up to a new level."

Commitment, competence, and compromise are all vital to functional collaboration according to Aart J. de Geus, chairman and co-chief executive officer of Synopsys. Since he has long lead a major electronic design automation (EDA) company, de Geus has seen electronics industry trends over the 30 years that Imec has been running. Today's advanced systems designs require coordination among many different players within the electronics industry ecosystem (**FIGURE 2**), with EDA and manufacturing R&D holding the center of innovation.

"The complexity of what is being built is so high that the guarantee that what has been built will work is a challenge," cautioned de Geus. Complexity in systems is a multiplicative function of the number of components, not a simple summation. Consequently, design verification is the greatest challenge for complex System-on-Chips (SoC). Faster simulation has always been the way to speed up verification, and future hardware and software need co-optimization. "How do you debug this, because that is 70% of the design time today when working with SoCs containing re-used IP? This will be one of the limiters in terms of product schedules," advised de Geus.

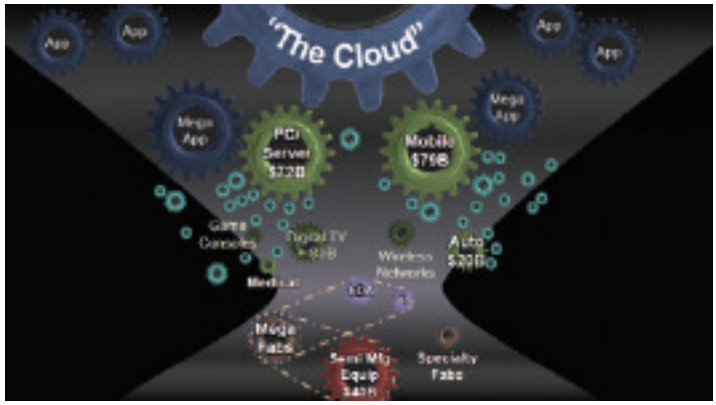

FIGURE 2. Semiconductor manufacturing and design drive technology innovation throughout the global electronics industry. (Source: Synopsys)

Whether HMC stacks of DRAM, VNAND, or newer memory technologies such as spintronics or Resistive RAM (RRAM), nanoscale electronic systems will use 3D memories to reduce volume and signal delays. "Today we're investigating all of the technologies needed to advance IC manufacturing below 10nm," said Van den hove. The future of 3D memories will be complex, but industry R&D collaboration is preparing the foundation to be able to build such complex structures.

DISCLAIMER: Ed Korczynski has or had a consulting relationship with Lam Research.

Superfast stress inspection for overlay control

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Tighter overlay requirements are motivating device manufacturers to explore new ways to characterize and manage overlay to improve yield.

Control of overlay in multi-layer devices structures has always been important in semiconductor fabrication. The understanding and control of stresses accumulated during device fabrication has becoming more critical at advanced technology nodes. Within-wafer stress variations cause local wafer distortions which in turn present challenges for managing overlay and depth of focus during lithography. As devices shrink, the overlay requirements become more and more stringent (**FIGURE 1**). The tighter overlay requirements are motivating device manufacturers to explore new ways to characterize and manage overlay to improve yield. The overlay budget includes contributions from the lithographic scanner, the reticle and the wafer. The wafer represents the largest source of overlay variability during high-volume manufacturing. Therefore, the development of an inspection strategy to control within-wafer and wafer-to-wafer variability may provide the key to meeting the challenges associated with future generations of devices.

Traditional wafer warpage or distortion measurements have typically used point-by-point measurements to generate low-density maps of the wafer geometry with a few hundred

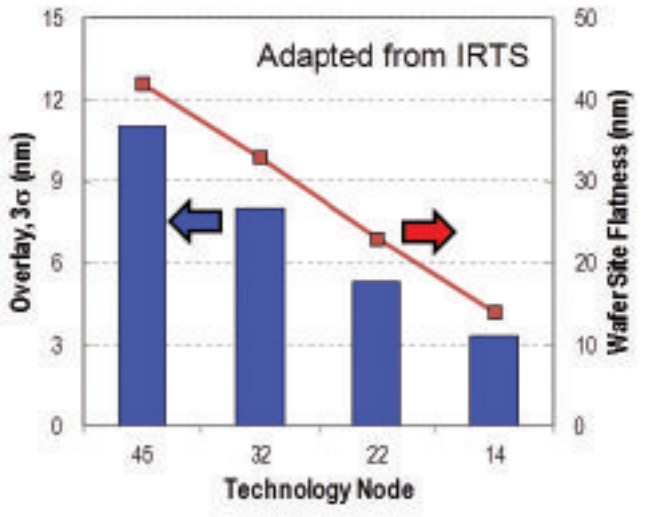

FIGURE 1. As devices shrink, the overlay requirements become more and more stringent.

data points across the wafer. Depending on the specific technique, a higher density map may be possible at the expense of throughput or limiting the measurement to a small portion of the wafer. The trade-off of point density and throughput has meant that the use of wafer distortion characterization for overlay control has been limited to off-line process development and not to improve yields.

The Superfast system based on the Coherent Gradient Sensing (CGS) interferometer uniquely

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provides high-density front-side pattern wafer maps (>3,000,000 data points) with fast data acquisition (seconds per wafer). The high throughput along with small foot print leads to a low cost of ownership relative to competing technologies.

This article discusses using deformation data from the front-side of a patterned wafer on the Superfast, we are able to understand the relationships between surface displacements, stress and overlay. It also reviews a case study evaluating the role of millisecond annealing parameters on overlay and stress.

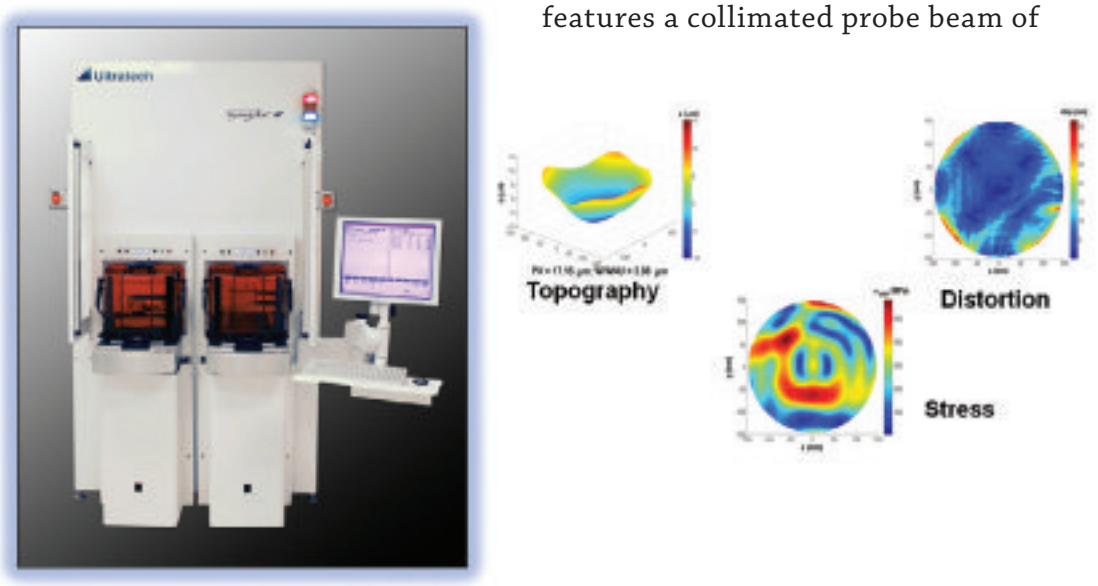

FIGURE 2. Typical results from the Superfast inspection system, designed for semiconductor manufacturing based on the CGS interferometer.

Superfast (CGS) technology description

The CGS interferometer is a type of lateral shearing interferometer. The interference is generated in a self-referencing manner using two parallel diffraction gratings. This self-referencing approach eliminates the need for an independent reference beam from, for example, a flat mirror and ensures excellent fringe contrast regardless of the reflectivity of the surface under investigation. This is a key differentiator to accurately measure patterned wafers.

The interferometer essentially compares the relative heights of two points on the surface that are separated by a fixed distance, called the shearing distance. Physically, the change in height over a fixed distance provides slope or tilt information and the fringes in a CGS interference pattern are contours of constant slope. The slope data derived from the interference patterns is integrated numerically to generate the surface shape or topography

Application to thin film stress measurement

The Superfast inspection system is designed for semiconductor manufacturing based on the CGS interferometer. The Superfast tool features a collimated probe beam of >300mm in diameter that is expanded from a relatively low power HeNe laser. The probe beam illuminates the entire wafer at once and the wafer is supported on three lift pins, which are then subtracted from the final analysis. The beam that reflects off of the wafer surface is distorted in accordance with the local height variations of the wafer. The distorted beam is steered through the two parallel diffraction gratings to generate an interference pattern that is imaged on to a CCD array. As a result, the wafer surface is mapped with high resolution (>3,000,000 data points) with measurement times of seconds.

Data integrity on patterned wafers is further enhanced through the implementation of phase shifting. Phase shifting is achieved by moving the gratings in the direction parallel to the shearing direction. Phase shifting provides several advantages and for the measurement of patterned wafers. The most notable being that fringe contrast in the interference fringes, that modulate with phase shifting can effectively be separated from pattern contrast, which is static with phase shifting. Phase shifting along with

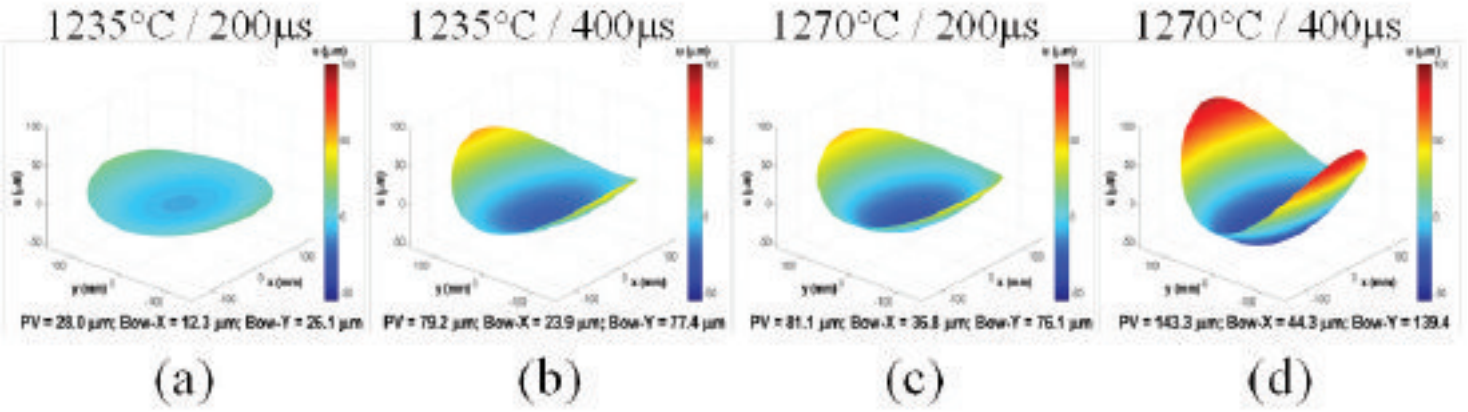

FIGURE 3. Displacement vector maps of the displacement residuals computed using a linear inter-field and intra-field correction.

the inherent self-referencing nature of the CGS technique results in relatively high measurement integrity on patterned wafers without the need for dedicated or distinct targets, pads or other specialized features in the layout. Typical results are shown in **FIGURE 2**.

Compared to other techniques, Superfast has several distinct advantages.

- Front-side Pattern Wafer Measurement- Core CGS 3G technology has been used to measure front-side of pattern wafers for over a decade
- High Data Density: Superfast generates high density maps of surface displacements that feature more than 3,000,000 points of data. In this manner, detailed within-die, die-to-die and wafer-to-wafer process variations that lead to overlay errors can be characterized.
- High Throughput/Low Cost: The Superfast data set consists of interferometric images of the full wafer. These images can be captured rapidly using CCD camera, providing system throughputs of 100-150 wafers per hour.
- Flexible Implementation: Superfast is capable of evaluating overlay at any step in the process flow and does not rely on dedicated overlay targets. In this manner, Superfast provides the ability to catch potential overlay problems due to process excursions upstream of lithography, thereby reducing material-at-risk and the need for subsequent scrap or rework.

Case study: millisecond anneal characterization

This section describes a case study to illustrate the application of Superfast technology to characterize a millisecond anneal process.

Four wafers of a full-flow 65nm device were annealed using Laser Spike Annealing (LSA). The device contained silicon germanium with 20% Ge. The four wafers were processed at peak annealing temperatures of 1235 or 1270°C and annealing times of 200 or 400 microseconds. Process-induced deformation information was collected by measure pre-anneal and post-anneal wafer topography using the Superfast system. After millisecond annealing, the wafers were processed through to contact patterning. Overlay data was collected post-lithography for all four wafers. The overlay was measured at 9 sites per shot for 28 shots. Surface displacement data was extracted at the same nominal locations on the wafer and displacement residuals were computed using linear inter-field and intra-field correction.

The displacement vector maps of the displacement residuals computed using a linear inter-field and intra-field correction are shown in **FIGURE 3**. Inspection of Fig. 3 reveals that the vector maps for the 1235°C temperature conditions (Figs. 3a & 3b) as well as the 1270°C / 200µs condition (Fig. 3c) all exhibit similar features such that the displacement vectors are generally in the same direction at a particular location in those three vector maps with the same relative vector magnitudes within-wafer. On the other hand, the

vector map for the 1270°C / 400µs anneal (Fig. 3d) shows a fundamentally different distortion characteristic, indicating perhaps a change in deformation mechanism associated with the higher thermal budgets. This data suggests that wafer distortion measurements may provide a relatively efficient way to study transitions in mechanisms that occur under different processing conditions.

The correlation between the surface displacement residuals and the overlay residuals is shown in **FIGURE 4**. The data in Fig. 4 is based on the |mean|+3 sigma values of both quantities as evaluated at the locations shown in the vector maps of Fig. 3. There are several features of the plot in Fig. 4 that are notable. First, the correlation between overlay residuals and displacement residuals is excellent with a correlation coefficient, r=0.985. Second, the extrapolation of the best-fit straight line to a displacement value of zero indicates a corresponding finite and positive overlay value of ~0.2. This result is not unexpected, since it is anticipated that other factors such as pattern placement error, lens errors and wafer distortion from other processes will contribute to the total overlay error. As such the overlay axis intercept provides an estimate of those other factors. Third, the slope of overlay versus displacement line is <1. A slope of less than 1 is consistent with the concept discussed in section 3, that the non-uniform stress component of the displacement field is related to the force acting along the interface or potential for mis-alignment. In this respect, it represents perhaps the maximum expected mis-alignment and the resulting overlay error will be some fraction of the 'potential' (i.e. slope <1). In addition, the slope value indicates that surface displacement is a more sensitive metric than overlay in that for the same process variability, surface displacement will change more rapidly than overlay.

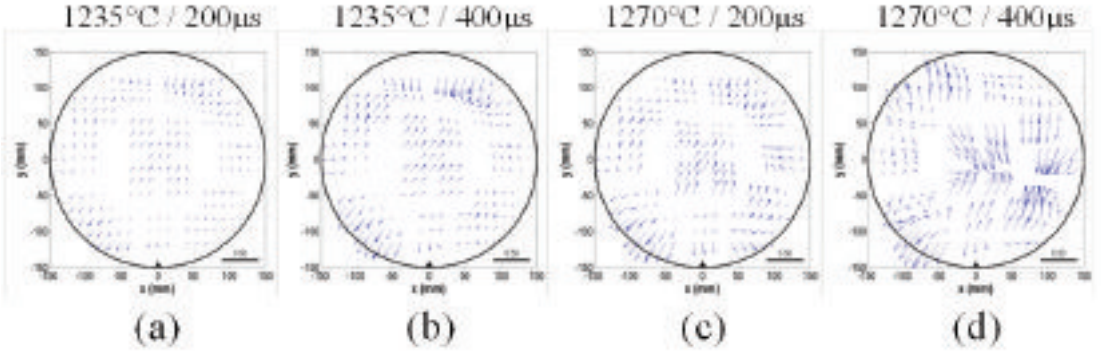

FIGURE 4. The correlation between the surface displacement residuals and the overlay residuals is shown.

Summary and conclusions

The tightening of overlay budgets at advanced technology nodes has led to a greater importance in understanding and when possible controlling wafer distortion. This paper has provided a description of a novel measurement and analysis approach to quickly and efficiently evaluate the effect of process-induced deformation on surface displacement and its relation to overlay errors. The millisecond annealing case study showed excellent correlation between the displacement residuals and overlay residuals with the correlation coefficient of 0.985. Utilizing the fundamental advantages of the CGS technology, the superfast is well suited for front-side patterned wafer topography measurement. The system allows for rapid measurement of wafer distortion and surface displacement with very high system throughputs. Data maps consisting of >3,000,000 data points can be acquired in seconds on patterned wafers without the need for special targets or dedicated structures. ◆

Novel integration of known technologies to reduce cost in 450 mm manufacturing

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A collaborative demonstration at G450C proactively trials and examines a solution to reduce cost for higher flows.

The impending change in silicon wafer diameter from 300mm to 450mm will increase the surface area of each wafer by 2.25 times. A worst-case scenario suggests that process gas flow rates required to maintain wafer throughput at acceptable levels would increase by the same scaling factor. Since the main reason to go to a 450mm wafer size is to lower manufacturing costs, we need to explore how to best minimize the downstream impact of higher gas flow rates on capital and operating expenditures of tool-support equipment, such as vacuum and gas abatement systems. In the case of flammable process gases, some thoughtful consideration and innovative options are required. The combination of higher flammable process gas flows and their associated safety dilution guidelines could greatly increase sub-fab space, equipment and facilities requirements, especially in the event that abatement systems are necessary to handle the total exhausted gas. Safely minimizing or eliminating additional dilution volumes is a viable opportunity to reducing the need for additional abatement units in a 450mm high volume manufacturing environment, the implication of which is increased capital and operational costs, not only for the base equipment, but also for site infrastructure which must be scaled to handle any additional abatement consumables and waste.

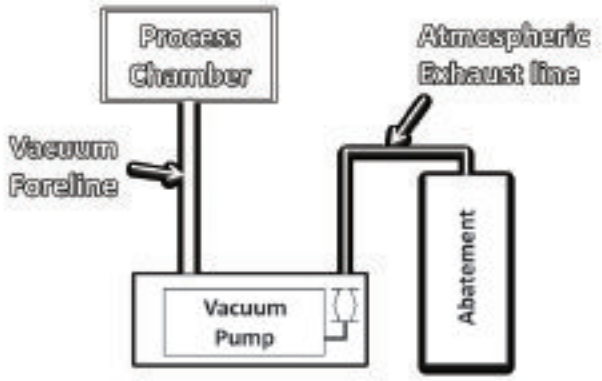

FIGURE 1. Process chamber and vacuum system diagram.

This article considers the likely impact and trade-offs of such flammable gas flow increases on process vacuum and abatement systems, which under a "business as usual" model would scale up purge and equipment sizes based on safety multipliers. Therefore, we propose an alternative approach: implementing an integrated vacuum and abatement system with a common supervisory control and monitored joints, which allows purge nitrogen flows and equipment sizes to be significantly reduced while still maintaining operational safety and compliance with SEMI standards

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and NFPA codes. Both the technical and cost implications are explored and data is provided from laboratory trials. The results suggest that there is an opportunity to enable 450mm capabilities by leveraging novel integration of known technologies to reduce gas flow increases and related capital and operating expenses.

Flammable gases

For higher gas flow rates in 300mm and 450mm, a particular challenge is safely handling and using flammable or pyrophoric process gases, such as hydrogen, silane, ammonia or phosphine. These gases are employed in a vacuum process chamber, pulled through a foreline using a pump which sits on the tool, in the sub-fab or both (**FIGURE 1**). These gases and their by-products are then exhausted at near atmospheric pressure to a point-of-use abatement device for treatment.

In a pure vacuum there is insufficient gas for combustion. A flammable gas can support combustion typically only above 50 mbar (0.725 psi or 5 KPa or 37.5 Torr). So the focus area is from the exit of vacuum pump to the abatement unit in the subfab, which is at about atmospheric pressure.

In order for a reaction to occur, there are three requirements in any system: 1) an ignition source, 2) sufficient fuel concentration and 3) an oxidizer present within the flammable concentration range of the fuel. Combustion will not occur if the ignition source is not energetic enough to initiate the reaction, or either fuel or oxidant is not present within the flammable concentration range.

In considering the first requirement for combustion, process gases pass through a vacuum pump, which is a metallic, motor-driven mechanical device, therefore, an ignition source cannot be ruled out nor can its energy be predicted. For the second condition, flammable process gases are dictate by process recipe requirements. Every "process fuel" gas has a lower flammable limit (LFL), which is the concentration in air below which it will not combust. **TABLE 1** shows some common process gases with their LFLs noted as a percentage of total gas composition.

TABLE 1. Flammable Gases and Lower Flammable Limits

Gas	LFL	Source
Hydrogen	4	Ref 1
Ammonia	15	
Diborane	0.8	
Carbon Monoxide	12.5	
Methane	5.3	
Propane	2.2	
Silane	1.37	
TEOS	0.9	
Phosphine	1.6 (estimated)	BOC Gases Material Safety Data Sheets
Dichlorosilane (DCS)	4.7	
Tetramethylsilane	1	
Acetylene	2.3	

Note: LFL is a % of total flow.
Source: Pumping Flammable Gases Applications Note P411-00-090. Edwards

Best safety practice as per NFPA68 and NFPA318, is to add an inert diluent such as nitrogen (N_2), to the process gas stream at or near the subfab vacuum pump. Flow rates are calculated to a fraction of LFL and based on maximum mass flow controller (MFC) settings and fab safety policy. For instance, a flow of 1 standard liter per minute (slm) of silane (SiH_4) at 1/2 LFL (1.37%) requires a flow of 145 slm of N_2. Many sub-fab vacuum systems include a N_2 purge from 0 to 200 slm. So an MFC larger than 1 slm of SiH_4 using this methodology, will drive a need for additional N_2 added after the pump to retain a non-flammable diluted gas mixture. (**TABLE 2**).

At an MFC of greater than 1 slm of SiH_4, the N_2 requirement increases rapidly. Extra N_2 not only increases the cost of the inert gas but requires that the downstream abatement and scrubbed exhaust system are able to handle the greater flow. This can double or triple the abatement capacity requirement, adding to the heat load in the sub-fab (when considering combustion type abatement), and increase facilities handling requirements. 150

TABLE 2. Silane Dilution requirements example

Silane (SiH_4) MFC	Nitrogen (N_2) Flow
slm	slm
0.5	72
1.0	144
1.5	216
2.0	290
2.5	362
3.0	435

Note: N2 calculated to ½ LFL of SiH4.

slm of N_2 costs (US average $0.05/$m^3$) about $5,000 annually and can occupy up to 25% of the abatement capacity, or more depending on the device. Using generic MFC flows for flammable process gases and surveying 300mm processes which could require 150 slm of N_2 dilution (additive to the typical dry pump purge) yields the list shown in Table 3 of processes which may have flammable gas flows (**TABLE 3**).

TABLE 3. Potential high flammable gas flow processes

Process	Flammable gases (slm)*						
	H_2	SiH_4	B_2H_6	PH_3	TEOS	Added N2	**New Chambers per annum
ALD W	50-60	1-2	0.5-1			> 150 slm	20 - 25
EPI	80-200			2-4		> 150 slm	700-800
MOCVD	100-200					> 150 slm	25-35
LPCVD Oxide					2	> 150 slm	200-250
LPCVD	362						
Poly		1-6		0.5-1		> 150 slm	Included above
SACVD					7-10	> 150 slm	180-220
PECVD Nitride		1-2			3-4	> 150 slm	900-1000
PECVD Oxide		1-2				> 150 slm	Included above

*Process gas flows are ranges based MFC equipment specifications for 300mm processes

**New Chambers per annum = Total chambers added 2014-2017 based on VLSI data and application assumptions averaged per year

Fab-wide, these critical processes require a lot of chambers and additional N_2 and this will only increase with 450mm flows. So, let us consider the case of the third condition needed to sustain a combustion reaction: oxidizers. Oxidizers can be present in the process gases, or oxygen can leak into the vacuum system from the environment. What if instead of diluting flammable gases, we prevented and monitored so that ambient oxidizers never enter the system?

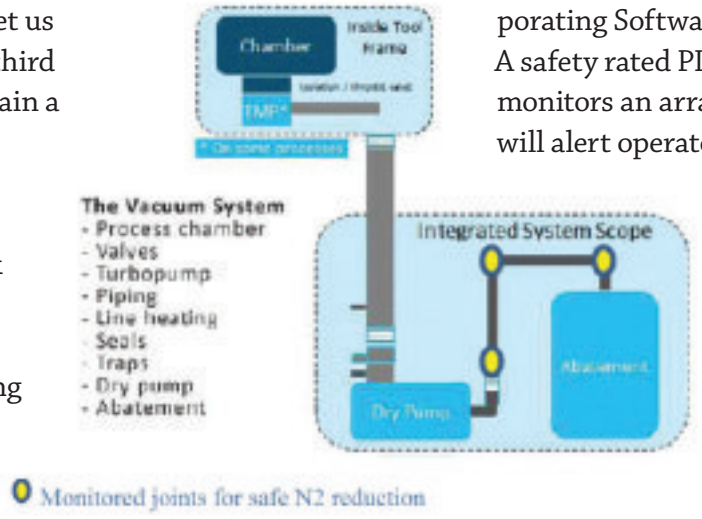

FIGURE 2. A simplified diagram of the Zenith Flex integrated vacuum system.

An alternative: The monitored connection

In the case of process recipes that prescribe flammable gases but no oxidizers and where dilution flows have become very high, an option is to prevent the introduction of an oxidizer, ambient air. To this effect, G450C and Edwards are looking to actively monitor the connections on the downstream side of the pump (**FIGURE 2**).

Critical to safe operation and monitoring is a fault tolerant, safety rated control designed to be compliant with NFPA 79, Section 9.4.3, "Control Systems Incorporating Software-and Firmware-Based Controls". A safety rated PLC (programmable logic controller) monitors an array of hardware based sensors, and will alert operators whenever a system fault is detected. Further, this control system will be integrated with the connected processing equipment and the factory safety system (often referred to as Toxic Gas Monitoring System or TGMS) to shut down gases when an out of specification condition exists.

Each connection has a secondary seal encircling it to create a space, which is then pressurized with N_2. A pressure change in that pressurized space indicates a breach either through the inner connection, where N_2 will be added to the process gas stream, or through the outer joint, with N_2 flowing to ambient (**FIGURE 3**). This arrangement of monitored connection provides the additional benefit of not allowing process gases to leak to ambient in the event of a connection failure. Monitoring looks for a change in pressure and is managed by the safety rated PLC (noted as system controller in **FIGURE 4**).

The system also incorporates the active monitoring of an existing flame arrester just up-stream of the

abatement to ensure that there is no flame propagation up the exhaust line. This monitor is interfaced to automatically shut off the process gases if a flame is detected at the monitored location.

The monitoring of the exhaust joints depends on the presence on nitrogen pressure. The uptime of the vacuum system would depend on nitrogen pressure to maintain purge flows and, for safety reasons, verification of the N_2 supply would be a fail-safe requirement. In the event of nitrogen pressure loss due to facilities failures or other reasons, this monitoring system is fail-safe, so that loss of nitrogen pressure will stop the process. It is not believed that this monitoring connection system is any more likely to fail than a high flow nitrogen purge system.

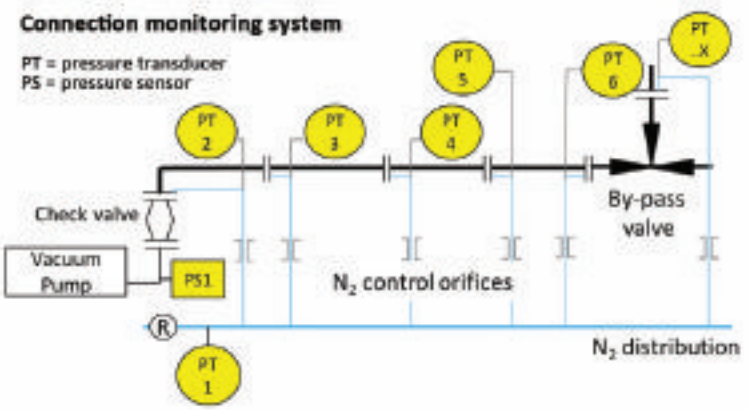

FIGURE 3. Monitored connection (PT = pressure transducer, PS = pressure sensor).

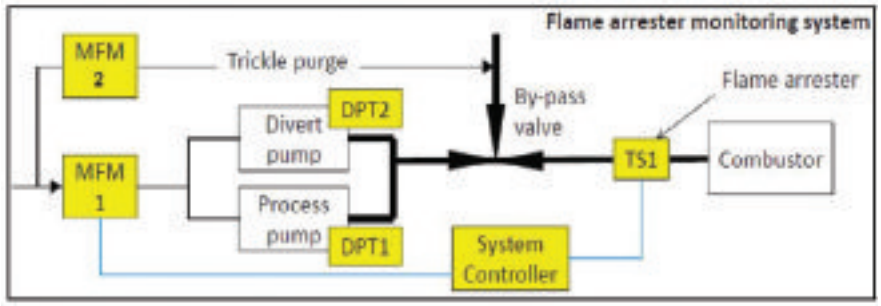

FIGURE 4. Flame arrestor (MFM = mass flow meter, DPT = dry pump temperature, TS = temperature sensor).

Testing

Prior to testing the system at G450C on the integrated vacuum and abatement system, a hardware test rig was set up in the laboratory to verify software, performance during leaks, fluctuations and signaling protocol.

The two main test objectives were:

1. to determine the pressure response when an o-ring fails and
2. to confirm independent, non-interfering monitoring of each coupling.

Test 1 was set up to measure the response to a hairline failure of an o-ring and compare that to a major failure by measuring the inter-seal pressure response in each case. The major failure responds with a noticeably different (larger) inter-seal pressure change than for a hairline failure. These test outputs established the set point levels for indicating an alarm or warning status (**FIGURE 5**).

Test 2 was used to confirm that individual couplings can be monitored independently from each other by observing that the measured pressure response from a failed o-ring in one coupling does not cause interference with the monitoring of another coupling. The same component parts that are to be installed at G450C were used in these verification tests monitored

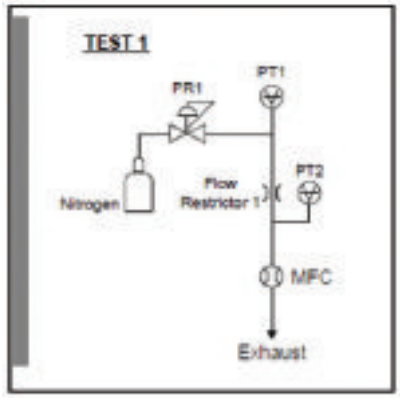

FIGURE 5. Monitored connection test set-up 1 (PR = pressure regulator, PT = pressure transducer, MFC = mass flow controller).

TABLE 4. Monitored Joint Test Results

Test	Objective	Upstream pressure PT1	Detection Pressure Set Point PT2	Result
		(psig)	(psig)	
1	Confirm protection during leak	15	7	Yes
	Confirm leak detection limit			73 sccm
2	Confirm system identifies which flange has leak			Yes
	confirm protection of non-leaking flanges unaffected by leak on one flange			Yes

by the safety PLC and IO (input/output) unit (**FIGURE 6**).

TABLE 4 summarizes the test results. In addition, a risk assessment and SEMI S2 third party review will be conducted to ensure thorough consideration of the equipment, implementation and safety. Once installed at G450C, the monitoring will be exercised and regular reviews will verify performance and other necessary procedures. Further evaluation will be given to ensure effective abatement performance with less dilute gases and potential options for additional utilities savings.

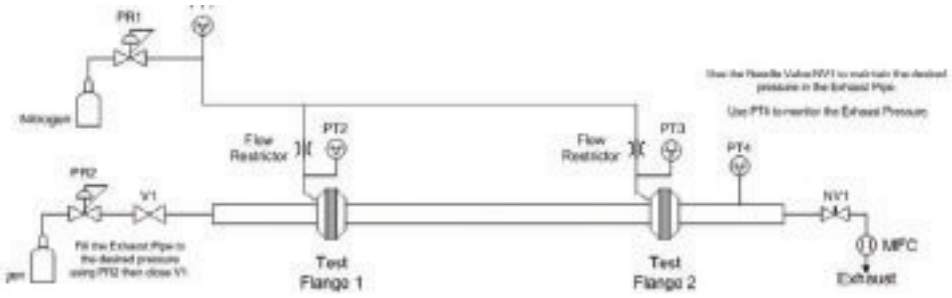

FIGURE 6. Monitored connection test set-up 2 (PR = pressure regulator, PT = pressure transducer, MFC = mass flow controller, V =valve, NV = needle valve).

Demonstrating at G450C

A CVD (chemical vapor deposition) tool with its silane MFC set to greater than 2 slm was chosen for the demonstration. With a single chamber, the current integrated pump, dilution and abatement system (Zenith Flex - **FIGURE 7**), can provide the required performance and capacity. However, if a second chamber is to be added, a second abatement device would be required just to accommodate the extra nitrogen required for dilution. In this case, the opportunity presents itself to set up the installation with the traditional dilution and have the monitored connection option for cost savings and demonstration purposes without risking wafer test runs. If there is an unforeseen issue with the monitored connections, the additional N_2 dilution and the required abatement is available.

Potential savings: Rough scenarios

In the case of a process tool using a 2 slm MFC for SiH_4 and requiring ½ LFL to meet facility safety requirements and assuming a 96 slm pump purge, an additional 194 slm of N_2 dilution is required. Using a conservative cost of $200,000 capital cost per unit for 600 slm of abatement capacity without accounting for additional footprint, maintenance, or operating costs, this represents $83,333 in apportioned abatement capital expenditure and installation just for the additional N_2 purge. Cost avoided in the first year is $88,000 and would likely be higher as abatement devices are supplied in discrete units and not in fractions. The additional cost of this monitoring system would be lower than the cost of the additional abatement capacity required with a N_2 purge system and would easily accommodate flammable process gas flow changes.

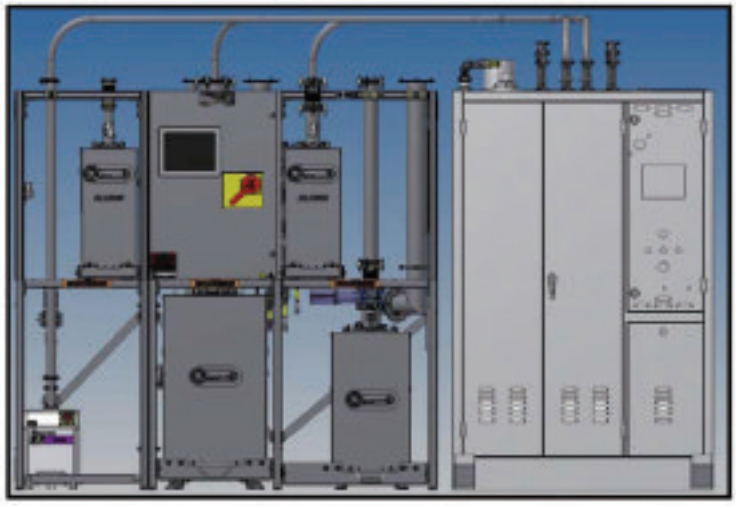

FIGURE 7. Zenith Flex: Integrated vacuum and abatement.

Additional considerations include the protocol for what to do in the event of a drop in the monitored connection pressure and to where the information is sent:

- safety management system
- tool process gas panel to initiate immediate shut down
- advisory warning system
- or a combination of the above

A process may contain multiple flammable gases and/or an oxidizer. In this case, a monitored connection strategy might be used in conjunction with a reduced dilution targeting the oxidant.

In the photovoltaic industry, for example, operating systems already exist where dilution

was not employed and exhaust pipeline pressure monitoring and bolted joints were used. Edwards has seen no adverse effects on a properly set up vacuum and abatement system at these facilities under standard operation.

Long exhaust lines can affect the gas velocity in the pipe and can cause by-products to solidify or precipitate out. In general, it is best to keep the exhaust line short and if necessary, heated to ensure that all process gases and by-products reach the abatement device for treatment. On some applications (**TABLE 3**) reduced dilution may lead to increased deposition in exhaust lines due to reduced gas velocity or increased chemical reaction rate. Where this is the case, exhaust dilution may be beneficial. However, the dilution factor is unlikely to be as high as is required to achieve 1/2 or 1/4 of the LFL.

As we build information from these case studies, lessons learned are codified in best known methods for process specific, integrated subsystem designs that provide the highest reliability at the lowest cost of ownership.

Conclusion

Based on increasing flow rates for flammable, pyrophoric and energetic gases, using the traditional N_2 dilution to keep gases below their LFL may no longer be economically feasible for some processes and could pose as a non-starter from a facilities perspective. The collaborative demonstration at G450C proactively trials and examines a solution to reduce cost for higher flows which could also be used in 300 mm process applications. An integrated vacuum and abatement system provides the communications platform and optimized piping to ensure the best design. Following a successful implementation on the CVD application, we will seek to expand this option for savings to other processes.

Acknowledgements

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Assume:

Process MFC for SiH_4 = 2 slm	N_2 price=$0.05/m3
Pump purge = 96 slm	
Abatement capacity = 600 slm	
LFL = 1.4%	1/2 LFL = 0.7%
No idle mode	100% up-time

Abatement cost (capital, install, connections) = $200,000

Additional N_2 dilution = 194 slm

Annual N_2 cost = $5,100

N_2 + pump purge = 250 slm abatement capacity

42% Extra abatement capacity required

Simplified additional abatement costs = $83,333

Simplified first year cost avoided with Monitored Connection $88,400

Not considered:
- Abatement operating, footprint, heat or extraction costs
- Price for N_2 dilution addition and monitoring
- Mixtures and other flammable gases
- Tuning of abatement for undiluted flammables destruction

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Scaling to 5nm with the usual suspects: Performance and cost

DEBRA VOGLER, *SEMI, San Jose, CA.*

There may be a non-EUV roadmap to 7nm, what will happen by 5nm is not so clear.

The semiconductor industry never lacks for challenges and/or controversy as it forges ahead from one technology node to the next. "Lithography is always a challenge," observes Dick James, senior technology analyst at Chipworks. While there may be a non-EUV roadmap to 7nm, what will happen by 5nm is not so clear, except "by the time the industry gets to 5nm, silicon will have run out of steam," said James. His recitation of the coming mountains to climb is extensive: integration of new materials, contact resistance of ever-smaller contacts, pitch quartering, contact etch and self-aligned vias, shrinking the gate stack, and modifying work function materials. And that's just the front-end!

"The big divide at the moment is FDSOI vs FinFET," James told SEMI. "If IBM survives, I could see them following the FDSOI route, but the rest of the industry seems to be going FinFET. By the time we get to 7nm and 5nm it will likely be moot, we'll have to do something else such as nanowires...in the end, it all boils down to performance vs. cost."

With respect to performance and scaling, Soitec's SVP of Digital Electronics Division and FDSOI guru Christophe Maleville, a clear proponent of SOI-based technology, told SEMI that a key challenge is delivering a worthwhile performance increase while allowing very low energy consumption. "In the PC era, performance was king," observed Maleville, who will speak at SEMICON West 2014. "Although power consumption was obviously a concern, it was okay to trade GHz for high leakage current. With the advent of the mobile, always-on device era, the weights of priorities have shifted." With mobile applications driving the industry, performance must also take into account low heat dissipation and battery life. "Delivering high drive current is one thing – and FinFET appears to be pretty good at that – but this has to be weighed against the other parameters that affect the actual in-application performance of the chip."

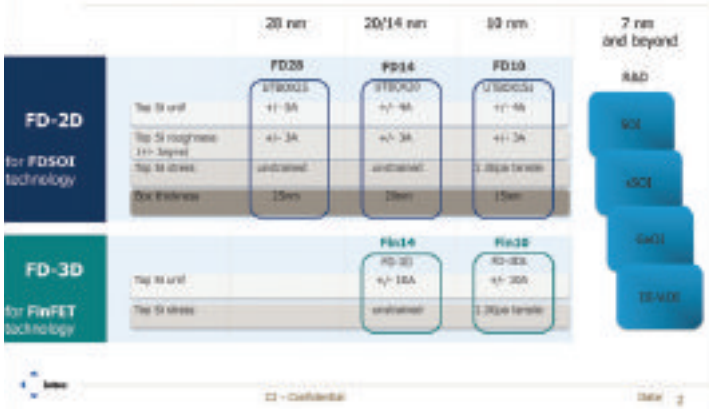

FIGURE 1. FDSOI product roadmap. (Source: Soitec)

Medium-term, i.e., down to the 10nm node, Maleville said that while there is a choice in transistor technology between FDSOI and FinFET, the latter has its challenges (**FIGURE 1**). At 14nm and below, particularly for bulk silicon, Maleville cites issues such as controlling substrate leakage

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and maintaining good variability. "In addition, because of its 3D architecture, parasitic capacitance of the FinFET device is relatively high and scaling means reducing the pitch into which FinFET transistors need to fit, which does not go in the direction of limiting (fringe) parasitic capacitance" said Maleville. "Beyond 14nm, these challenges will become even more pressing." Doing FinFET on SOI can help alleviate some of these challenges because it offers intrinsic isolation under the fin, thereby removing the need for a complex-to-optimize punch-through stopper junction. "It also eliminates some variability associated with the doping this junction requires." FinFET on SOI also aids in the manufacture of fins with well-defined height, "therefore, ensuring no excessive variability from fin geometry fluctuations."

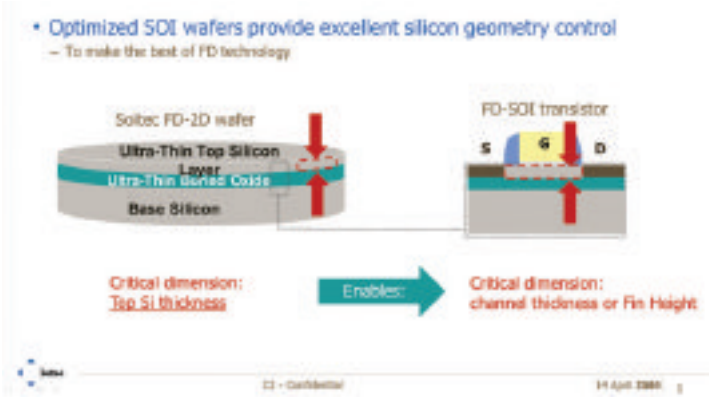

FIGURE 2. SOI value: part of device is integrated in the substrate. (Source: Soitec)

FDSOI technology is not without its own set of challenges. "The electrostatic control of an FDSOI transistor is, in principle, not as good as that of a multi-gate device," Maleville explained. "On the other hand, FDSOI is less subject to some of the pains associated with scaling FinFETs, such as keeping parasitic capacitance low enough, or keeping variability (including that originating from transistor geometry variations) under control." **FIGURE 2** illustrates the value that using SOI brings (for FD-2D technology) in terms of silicon geometry control and uniformity.

With respect to scaling FDSOI technology to 14nm, Maleville noted that excellent results were reported at IEDM 2013 and that both Leti and STMicroelectronics are showing roadmaps to scale FDSOI down to 10nm, with introduction of Ge in the channel, along with further source/drain optimization and the option to use strained SOI. With respect to starting SOI wafers, the key areas of work already underway according to Maleville are: 1) ensuring excellent thickness uniformity of the thin silicon layer, which needs to be improved from one node to the next; 2) reducing the thickness of the buried oxide from one node to the next, and 3) continuing to provide ultra-thin layers of top silicon with state-of-the-art defectivity required at each node.

Industry experts interviewed on the topic of scaling are in agreement about new device architectures (e.g., gate-all-around, nanowires, tunnel FET, etc.) along with new materials (e.g., Ge and III-V compound semiconductors). Regarding the introduction of new materials, Maleville notes that the following will have to be considered: 1) demonstrating at the device level that there is a CMOS solution based on the new materials that deliver better results than silicon in the power supply and geometrical dimension ranges envisaged for the 7nm-5nm nodes, and 2) finding a way to implement Ge or a III-V material of suitable quality for good transistor behavior. "The Smart Cut layer transfer technology employed to fabricate SOI wafers has a role to play here," said Maleville. "In particular, transferring germanium or III-V materials onto an oxidized silicon base (i.e., doing GeOI or III-V.OI) can be an interesting alternative to epitaxial growth of these materials on a bulk substrate."

Because of lattice mismatch, Maleville further explained that epitaxial growth of Ge or III-V on silicon is challenging and achieving decent material quality is difficult. Though the alternative approach of Smart Cut-based layer transfer comes with its own set of challenges (defectivity, etc.), "it has the advantage of allowing the slice of a high-quality layer from a donor that can have defects outside the transferred layer, and the ability for this donor to be recycled multiple times."

FIGURE 3. Carbon nanotubes (CNTs): only promising material. (Source: Stanford University)

Enter CNTs

While the industry winds its way through the myriad choices of lithography technologies, transistor architectures, and materials choices, experts note that once the industry gets to 5nm, something new will have to happen. One technology getting close scrutiny is carbon nanotube (CNT) logic transistors. H.S. Philip Wong, the Willard R. and Inez Kerr Bell Professor in the School of Engineering and Professor of Electrical Engineering at Stanford University, told SEMI that transistors made with carbon nanotubes as the channel material hold special promise. The promise is due to the ultra-thin body of the carbon nanotube being only about one nanometer, while at the same time retaining excellent carrier transport properties. "No other bulk semiconductor has this unique advantage that allows the carbon nanotube transistor to scale to the shortest possible gate length," said Wong (**FIGURE 3**).

The key issues in bringing CNT logic transistors to the forefront, noted Wong, include: 1) contact resistance (reducing the transfer length of the contact); 2) maintaining good carrier transport while meeting electrostatic requirements; 3) having a coordinated effort in industry (as exemplified by how the semiconductor industry solved the high-k/metal gate problem); and 4) taking a practical approach and recognizing that exotic, non-FET-based devices will not meet the time line of the industry for the 5nm node.

Recent developments of CNT transistor technology for digital logic include the synthesis of fully aligned carbon nanotubes on a wafer scale, device fabrication of high-performance carbon nanotube transistors, 3D integrated carbon nanotube circuits, low voltage (0.2 V) operation of carbon nanotube transistors, and compact models for circuit simulation. Performance benchmarking of carbon nanotube transistors with conventional CMOS at the device and the full-chip processor level have also been accomplished, along with the demonstration of circuits and complete systems.

Interested in learning more about the industry getting down to the 5nm node? Come hear from Soitec, imec, Intermolecular, GLOBALFOUNDRIES, SEMATECH, Stanford University, and G450C at the SEMICON West 2014 Semiconductor Technology Symposium (STS) session titled "Getting to 5nm Devices: Evolutionary Scaling to Disruptive Scaling and Beyond." For information about this program, the agenda or pricing, please visit www.semiconwest.org/sts. SEMICON West 2014 will be held July 8-10 at the Moscone Center in San Francisco.

Harnessing big data

NORD SAMUELSON, CHRISTOPHER POCEK *and* **CHRIS LANMAN**, *AlixPartners, San Francisco, CA*

Addressing the analytics challenges in supply chain management.

A changing workforce and lack of convergence between information technology (IT) and business may be preventing many companies from joining the big-data revolution. Defined as very large sets of data but more commonly used in reference to the rapid increase in amounts of data in recent years, big data will divide companies into two groups in the next decade: those able to benefit from big data's potential and those unable. Companies that create capabilities for capturing, processing, analyzing, and distributing data in order to make better decisions in real time will likely be able to outperform their competition and respond more quickly to their customers' needs. The data avalanche is coming from a number of sources, such as enterprise resource planning, orders, shipments, Weblogs, GPS data, radio-frequency identification, mobile devices, and social channels; and there is value to be created in all areas of a business by adopting a data-driven culture.

However, in discussions about big data's arrival, we sometimes forget to ask how effectively we're converting the data into value. Too often, huge investments in IT infrastructure coupled with sophisticated analytical and reporting software have delivered little value. Why? We often find it's because companies are understaffed, or they may lack the analytics talent who know how to build links between the data and the value drivers. There is also a gap between finding insights from data and then applying the insights to create value. That is where the levels of training and experience of a company's analysts enter the equation.

One area of particular concern is supply chain management (SCM). A company's SCM organization makes decisions about build plans, stocking locations, inventory levels, and so forth based on the conversion of raw data about demand, sales, and inventory on hand. And when there's a shortage of analytics talent, SCM is typically one of the first areas affected. Traditionally, analytical innovation happens in two ways: either through an internal-pipeline process of developing junior analysts into senior analysts or by periodically bringing in external experts to seed knowledge. But big data is challenging both approaches.

The internal pipeline is challenged by a workforce marked by shorter tenures. Shorter tenures result in more generalists in the workforce, often in place of the specialists needed for analytical innovation. For example, younger workers, such as millennials, are significantly less likely to settle into a long career at a company. According to a survey by Future Workplace, 91% of millennials (born in the 1980s and '90s) expect to stay in a job for less than three years (Meister 2012), meaning that those in analytical roles are usually in the job only long enough to execute established analytics—and not long enough to develop a holistic understanding of how data can be applied to drive business value. As a result, those on the business side and those on the IT side don't always learn to make the end-to-end connections between raw data and measurable value. The internal-pipeline approach is further challenged by companies themselves: frustrated by high turnover, companies are less likely to invest in developing their people—only to watch the people leave for higher-paying positions.

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The second approach—that of periodically bringing in external experts to rebuild a process or implement the latest software package—is also starting to show wear. The evolution cycle of new analytical techniques is rapidly slowing down as big data brings opportunities to better integrate internal and external data sources. Traditionally, companies have been able to implement software solutions or bring in experts to install the latest offering and then profit from that investment for five or seven years. The initial cost was justified by the continued value for years to come. But now, the volume, variety, and velocity of the new data being generated are changing the business landscape by calling for a more rapid cycle of analytical-tool introduction. And that landscape itself usually changes every two or three years. So, as a result, the days of big-bang projects appear to be coming to an end.

What can be done? Companies should look across the entire supply chain—or across any function, for that matter—and measure the amount of data being generated. Then they should weigh that measurement against the value actually realized. If data volumes are growing more rapidly than the corresponding increase in value, there may be an analytics talent challenge.

Three methods of creating value have proved effective in today's rapidly changing market.

1. Outsourcing portions of analytic requirements

Companies can approach analytics outsourcing in a variety of ways, ranging from a data prep model—in which a company hires a third party to process raw data to the point where an analyst can consume it—all the way to a fully outsourced model, in which a third party processes and analyzes the data, potentially adds other proprietary data, and sends back fully actionable information. The data prep model enables a company to focus a limited pool of analysts on the critical knowledge-capture portion of the process and thereby free up time spent on non-value-added processes. The fully outsourced model enables companies to stay up-to-date on the latest technologies and software without having to make up-front investments to purchase the latest software and technology.

2. Creating central analytics teams

Companies that rely heavily on converting data to knowledge can set up an analytic group focused solely on solving analytical issues across the company. Such companies have adopted analytics as a core differentiator and encourage analysts to develop the holistic view that facilitates insight. Central analytics groups seem to perform better than embedded groups—and especially when they report through the business side. Of course, maintaining a group dedicated to analytics is an investment that some companies may hesitate to make, but there is tremendous value in having such in-house expertise.

3. Partnering with academic or not-for-profit institutions

Academic and nonprofit organizations are often-overlooked resources. For instance, the brand-new Center for Supply Chain Management at the University of Pittsburgh intends to provide student and faculty interactions with industry representatives who will promote experience-based learning activities within the university's supply chain management courses. To improve the center's effectiveness, the university plans to create a Supply Chain Management Industry Council composed of member companies dedicated to SCM. The council members, along with tenured faculty specializing in teaching SCM, will foster interest and excellence in SCM and analysis. Other institutions offer training, certifications, and conferences that encourage and enable analysts to further develop and share ideas. The Institute for Operations Research and the Management Sciences recently introduced the Certified Analytics Professional certification to give companies an option for developing their people without having to make hefty investments in training organizations.

Big data is fundamentally transforming the way business operates. It is enabling management to track the previously untrackable, forecast the previously unpredictable, and understand interactions between suppliers and customers—all of it with unprecedented clarity. And winning organizations will invest in the necessary infrastructure and people to harness the transformative power of data.

SEMICON West 2014: Without limits

In addition to 700+ exhibitors, this year's show offers a variety of educational programs and networking opportunities, including the Semiconductor Technology Symposium, The Silicon Innovation Forum, The Sustainable Manufacturing Forum, and The Global Summit for Advanced Manufacturing.

2014 marks the 34th year for SEMICON West, the main tradeshow in the U.S. focused on semiconductor manufacturing. The show will be held July 8-10 in San Francisco at the Moscone Center, with exhibits opening at 10:00 am each day, closing at 5:00 pm on Tuesday and Wednesday and 4:00 pm on Thursday.

The main attraction of the show will be the 700+ exhibitors offering equipment, materials and services for the manufacturing of semiconductors and related products such as MEMS, LEDs, displays, bioelectronics, photovoltaics, silicon photonics, power electronics and printed/flexible electronics. Co-located with SEMICON West, for the 7th year, will be Intersolar North America. Registered attendees are able to visit both shows with their badge.

On the show floor, you'll see a range of equipment and materials related to: deposition (CVD, PVD, ALD); etch; ion implant; lithography; masks/reticles and mask-making equipment; chemical mechanical planarization (CMP), equipment and materials, silicon and non-silicon based wafers and substrates; process chemicals and gases; chemical handling systems; vacuum systems components, and parts; robotic systems and components; valves, actuators, gear systems, and other components; factory automation systems, software, and components; assembly and packaging equipment and materials; wire bonding; bump/flip chip/wafer-level packaging; automated semiconductor test equipment (ATE); test handlers; and probe cards and test materials. You'll find many of the products at this year's show highlighted at the end of this section.

Beyond the show floor, SEMI has a variety of events and symposium, ranging from hot topics presented twice a day in TechXPOTS in both the North and South Hall, as well full multi-day conferences. For example, a session on breakthrough research technologies will take place on Thursday, July 10, in TechXPOT South). It will explore the latest innovations and activities from the world's leading labs. It's designed to answer the questions: What's happening on the cutting-edge of semiconductor materials and process research? What issues and challenges are driving the world's research institutions, consortia, and universities?

Semiconductor Technology Symposium

Aligned with the latest inputs from the International Technology Roadmap for Semiconductors (ITRS), sessions at the STS will focus on the big trends shaping near-term semiconductor technology and market developments in areas including 450mm, advanced processes and materials, lithography, metrology, yield, design packaging, and test. For 2014, the Test Vision 2020 workshop will join the STS session agenda to address the key trends in ATE. It will be held July 8-10, Moscone North, Hall E, Rooms 130 and 131

STS is a paid technology and business conference addressing the key issues driving the future of semiconductor manufacturing and markets.

Silicon Innovation Forum

The Silicon Innovation Forum is a platform for early-stage companies to demonstrate their technologies, for investors to identify new business opportunities, and for both communities to explore the technology and business challenges shaping the future of microelectronics. The forum provides a stage for new and emerging innovators, industry leaders, strategic investors, and venture capitalists to discuss the needs and requirements of the industry's innovation engine. Participants will gain insights into technology, capital, partnership, and collaboration

TechXPOT Sessions

Sessions at the TechXPOTs are aimed at engineers and technologists looking for solutions to key technology challenges and looking to better understand cutting-edge and future technology developments. Developed in conjunction with SEMI technical committees, partner organizations, and technologists, the TechXPOT agenda will provide a deeper view of key technology developments in areas including test, advanced materials and processes, and productivity.

TechXPOT: South Hall

Tuesday, July 8, 2014

10:30am-12:45pm	Next Generation MEMS
1:30pm-3:30pm	Variability Control – A Key Challenge and Opportunity for Driving Towards Manufacturing Excellence

Wednesday, July 9, 2014

10:30am-12:30pm	Subcomponent Supply Chain Challenges for 10 nm and Beyond
1:30pm-3:30pm	Secondary Equipment for Mobile & Diversified Applications

Thursday, July 10, 2014

10:30am-12:30pm	3D Printing: Science Fiction or the Next Industrial Revolution?
1:30pm-3:30pm	Breakthrough Research Technologies: Universities, Industries, Consortiums

TechXPOT: North Hall

Tuesday, July 8, 2014

10:30am-12:30pm	Testing into the Future
1:30pm-3:30pm	Materials Session: Speeding on the Roadmap-The Future of 3D NAND Flash

Wednesday, July 9, 2014

10:30am-12:30pm	Bringing Silicon Photonics to Market
1:30pm-3:35pm	Driving Automotive Innovation-The Enabling Role of Semiconductor and IC Packaging

Thursday, July 10, 2014

10:30am-12:40pm	Disruptive Compound Semiconductor Technologies
1:30pm - 3:30pm	SEMICON West 2014 IoT Startup Showcase – An SK Telecom Americas Innopartners Program

strategies necessary for mutual success. Two panels consist of a "who's who" in the investor world, including: Robert Maire, President, Semiconductor Advisors, LLC; Eileen Tanghal, General Manager, Applied Ventures LLC; Kurt Peterson, Screening Committee, Band of Angels; Pete Moran, General Partner, DCM Ventures; Steve Hahn, Research Fellow, Dow Ventures; Sean Doyle, Director, Intel Capital; Dong-Su Kim, Senior Director, Samsung Ventures Investment Corp., and George Pavlov, General Partners, Tallwood Ventures.

Sustainable Manufacturing Forum

In conjunction with SEMICON West, the SEMI EHS Division is organizing a four-day event to share information about the latest technologies, products, and management approaches that promote sustainable manufacturing. Under the auspices of the SEMI Global Care program, the Sustainable Manufacturing Forum will showcase companies and speakers from around the world involved in the manufacture of semiconductors, micro-electronics, nano-electronics, photovoltaics (solar), solid state lights (LEDs), electronic displays (FPD), micro-electrical mechanical systems (MEMS), and other high tech products. Experts from these industries and their supply chains will address a wide variety of environment, health, safety (EHS), sustainability, and social responsibility topics that affect high tech manufacturing.

The Sustainable Manufacturing Forum will consist of 12 distinct Sessions, 20 hours of seminars, workshops and roundtable discussions. Professional networking opportunities are provided around these sessions. It will be held July 7th at the San Francisco Marriot Marquis, and July 8-10 at Moscone Center North Hall, Room 124.

Global Summit for Advanced Manufacturing

If you're looking to deepen your knowledge of practical solutions to manufacturing challenges, plan to attend GSAM 2014 and explore issues common in taking manufacturing to the next levels of miniaturization, integration, ruggedization, and automation. A wide variety of industry sectors -

electronics, food, heavy equipment, technology and textiles - confront similar challenges with new materials, tools and processes, while ensuring speed to market.

GSAM 2014 features high level speakers who have confronted these challenges and are willing to share their stories. Hear a wide range of experiences in successfully developing and manufacturing products for today's demanding markets.

Keynote talks


Mark Adams

Of special interest are the keynote addresses. Mr. Mark Adams, President, Micron Technology, Inc., will deliver a talk titled: "Innovation and Partnership: Driving the Future of the Semiconductor Industry." He says the future has never been brighter for the semiconductor industry, but there are unprecedented challenges as well. Like all semiconductor companies, memory manufacturers need to maintain strategic partnerships with our suppliers in order to deliver on the promise of a better tomorrow through technology innovation. In his talk, he'll Micron will review how favorable memory market conditions, advances in technology, growth driven by mobile, server and tablets and the consolidation of major semiconductor manufacturers can create a world of opportunities for innovation and success.


Sanjay Ravi

Mr. Sanjay Ravi, Worldwide Managing Director, Discrete Manufacturing Industry, Microsoft Corporation will also deliver a keynote talk, titled "The Art of the Possible: How Manufacturers are Leveraging Digital Technologies to Drive Business Transformation in a Connected World." He notes that today's semiconductor manufacturing enterprises must move faster and make decisions more rapidly in a highly complex and uncertain environment filled with more data but less insight. To transform their businesses to address these challenges, manufacturers are embracing digital technologies such as social, mobile, cloud, and big data analytics to drive innovation, streamline operations, and increase production agility and growth. During this session Microsoft will review with examples how manufacturers are employing digital technologies to transform their business and the benefits they gain.

SEMICON west power lunch

Another new feature of the show: the power lunch. Tired of the same old sandwich? Need a convenient place to meet without leaving the show? Have a hot meal at the new SEMICON West Power Lunch! For just $25, you get a choice of entrée, salad, dessert, and soft drinks and plenty of seating. Recharge while you power up! Location: North Hall.

SEMICON West 2014 Event Calendar

Monday, July 7, 2014

9:00am-5:00pm
SEMI PV Advanced Manufacturing Forum
InterContinental Hotel San Francisco

10:30am-12:30pm
Sustainable Manufacturing Forum: Session 1 - Sustainable Regulatory Compliance: USA & Europe
San Francisco Marriott Marquis

12:30pm-6:00pm
Imec Technology Forum US (by invitation only)
San Francisco Marriott Marquis

1:00pm-5:30pm
SEMI/Gartner Market Symposium
San Francisco Marriott Marquis

1:30pm-3:30pm
Sustainable Manufacturing Forum: Session 2- Sustainable Compliance: Asia
San Francisco Marriott Marquis

4:00pm-6:00pm
Sustainable Manufacturing Forum: Session 3 - Sustainable Materials Procurement
San Francisco Marriott Marquis

6:00pm-7:30pm
SEMI VIP Reception
San Francisco Marriott Marquis, Atrium

SEMICON West Calendar

Tuesday, July 8, 2014

9:00am-9:45am
Opening Keynote
Mr. Mark Adams, President, Micron
Keynote Stage, Moscone Center, North Hall, Room 135

9:00am-12:00pm
STS Session: Challenges, Innovations and Drivers in Metrology
Session Partner: SEMATECH
Moscone North, Hall E, Room 130

9:00am-12:00pm
STS Session: Mobility and More–The M&Ms of Cost Beneficial Advanced Packaging
Session Partner: CPMT
Moscone North, Hall E, Room 131

9:45am-10:00am
Opening Ceremonies
Keynote Stage, Moscone Center, North Hall, Room 135

10:00am-5:00pm
SEMICON West 2014 Exhibition Hours

10:30am-12:30pm
Sustainable Manufacturing Forum: Session 4 - Environmental Footprint Assessment
Moscone North Hall, Room 124

10:30am-12:45pm
Next Generations MEMS
TechXPOT South, South Hall

10:30am-12:30pm
Testing into the Future
Hosted by the Collaborative Alliance for Semiconductor Test (CAST)
TechXPOT North, North Hall

12:00pm-1:30pm
STS Sessions Networking Lunch
Moscone North, Hall E, Room 133

1:00pm-4:00pm
Silicon Innovation Forum Conference
Keynote Stage, Moscone Center, North Hall

1:30pm-3:00pm
Sustainable Manufacturing Forum: Session 5 - Green House Gass (GHG) Assessment
Moscone North Hall, Room 124

1:30pm-4:45pm
STS Session: Defectivity and Process Variability-Inspection, Defect Reduction Challenges and Process Controls at the Sub 20nm Nodes
Session Partner: SEMATECH
Moscone North, Hall E, Room 130

1:30pm-4:30pm
STS Session: Embracing what's NEXT – Devices & Systems for Big Data, Cloud and IoT
Moscone North, Hall E, Room 131

1:30pm-3:30pm
Variability Control–A Key Challenge and Opportunity for Driving Towards Manufacturing Excellence
Session Partner: SEMATECH
TechXPOT South, South Hall

1:30pm-3:30pm
Speeding on the Roadmap-The Future of 3D NAND Flash
Hosted by: SEMI Chemical and Gases Manufacturers Group (CGMG)
TechXPOT North, North Hall

3:30pm-5:00pm
Sustainable Manufacturing Forum: Session 6- Advanced Abatement Systems
Moscone North Hall, Room 124

4:00pm-6:00pm
Silicon Innovation Showcase and Reception
Moscone North Hall, Room 134

4-30pm-7:30pm
Connect with India - The Next Semiconductor Manufacturing Region
San Francisco Marriott Marquis

5:00pm-8:00pm
Leti Day (By Invitation Only)
W Hotel

SEMICON West Calendar

Wednesday, July 9, 2014

7:30am-10:00am
Sokudo Lithography Breakfast Forum 2014
San Francisco Marriott Marquis

7:30am-9:00am
SEMI Membership Breakfast and Announcement of the Board (Members Only)
San Francisco Marriott Marquis

8:00am-6:30pm
Global Summit for Advanced Manufacturing (Day 1 of 3)
San Francisco Marriott Marquis

9:00am-12:00pm
STS Session: Design for Test
Session Partner: Electronic Design Automation Consortium
Moscone North, Hall E, Room 130

9:00am-12:00pm
STS Session: Getting to 5nm Devices: Evolutionary Scaling to Disruptive Scaling and Beyond
Moscone North, Hall E, Room131

10:00am-10:45am
Keynote:
Mr. Sanjay Ravi
Worldwide Managing Director, Discrete Manufacturing Industry
Microsoft Corporation
Keynote Stage, Moscone Center, North Hall, Room 135

10:00am-5:00pm
SEMICON West 2014 Exhibition Hours

10:30am-12:00pm
Sustainable Manufacturing Forum: Session 7- Energy/Resource Conservation
Moscone North Hall, Room 124

10:30am-12:30pm
Subcomponent Supply Chain Challenges for 10 nm and Beyond
Hosted by: SEMI Semiconductor Components, Instruments, and Subsystems Special Interest Group
TechXPOT South, South Hall

10:30am-12:30pm
Bringing Silicon Photonics to Market
TechXPOT North, North Hall

12:00pm-12:30pm
Sustainable Manufacturing Forum: Session 8- Sustainable Technologies Award
Moscone North Hall, Room 124

12:00pm-1:30pm
STS Sessions Networking Lunch
Moscone North, Hall E, Room 133

1:30pm-4:30pm
STS Session: Readiness of Advanced Lithography Technologies for HVM
Moscone North, Hall E, Room 131

1:30pm-3:00pm
Sustainable Manufacturing Forum: Session 9- Next Generation Eco Fab, Part 1
Moscone North Hall, Room 124

1:30pm-4:30pm
Wafer Geometry Control for Advanced Semiconductor Manufacturing
San Francisco Marriott Marquis

1:30pm-3:30pm
Secondary Equipment for Mobile & Diversified Applications
Hosted by the Secondary Equipment and Applications Americas Chapter
TechXPOT South, South Hall

1:30pm-3:35pm
Driving Automotive Innovation-The Enabling Role of Semiconductor and IC Packaging
Session Partner: MEPTEC
TechXPOT North, North Hall

1:30pm-7:00pm
Test Vision 2020 Workshop and reception (Day 1 of 2)
Moscone North, Hall E, Room 130

3:30pm-5:00pm
Sustainable Manufacturing Forum: Session 10 - Next Generation Eco Fab, Part 2
Moscone North Hall, Room 124

4:00pm-5:30pm
Bulls and Bears
W Hotel

SEMICON West Calendar

Thursday, July 10, 2014

7:30am-10:00am
Entegris Yield Breakfast Forum 2014
San Francisco Marriott Marquis

8:00am-5:15pm
Global Summit for Advanced Manufacturing (Day 2 of 3)
San Francisco Marriott Marquis

8:00am-5:00pm
Test Vision 2020 (Day 2 of 2)
Moscone North, Hall E, Room 130

9:00am-12:00pm
STS Session: 450mm Technology Development Update
Moscone North, Hall E, Room 131

10:00am-4:00pm
SEMICON West 2014 Exhibition Hours

10:00am-4:45pm
FlexTech Alliance Workshop: Flexible Hybrid Electronics for Wearable Applications – Challenges and Solutions
San Francisco Marrriott Marqui

10:30am-12:30pm
Sustainable Manufacturing Forum: Session 11 - Sustainability of Advanced Materials
Moscone North Hall, Room 124

10:30am-12:30pm
3D Printing: Science Fiction or the Next Industrial Revolution?
Session Partner: SEMICO Research
TechXPOT South, South Hall

10:30am-12:30pm
Disruptive Compound Semiconductor Technologies
TechXPOT North, North Hall

12:00pm-1:30pm
STS Sessions Networking Lunch
Moscone North, Hall E, Room 133

1:30pm-3:30pm
Sustainable Manufacturing Forum: Session 12 - Fabless Considerations in Manufacturing
Moscone North Hall, Room 124

1:30pm-3:30pm
STS Session: Breakthrough High Volume Manufacturing: New Paradigms for the Road Ahead
Moscone North, Hall E, Room 131

1:30pm-3:30pm
SEMICON West 2014 IoT Startup Showcase – An SK Telecom Americas Innopartners Program
TechXPOT North

1:30pm-3:30pm
Breakthrough Research Technologies Universities, Industries, Consortiums
TechXPOT South

Friday, July 11, 2014

9:00am-4:00pm
Global Summit for Advanced Manufacturing (Day 3 of 3)
Manufacturer's Tour

New Products at SEMICON West 2014

Rapier XE system for 300mm wafer silicon etching from SPTS Technologies

SPTS Technologies' Rapier XE system for 300mm wafer silicon etching offers significant advantages over competing systems as well as improved etch rate over the 1st generation Rapier in applications where "blanket" etching or removing a large exposed area of silicon is required, such as via reveal processing.

In 3D-IC applications, via reveal processing occurs after the through silicon vias (TSVs) are formed, to prepare the vias for redistribution metallization. After completion of front-side wafer processing, the wafer is temporarily bonded, face down, onto a carrier wafer. The active silicon is then ground typically to within 5-10 µm of the TSV nodes. The silicon is then dry etched in a process that 'reveals' the vias to a step height typically in the range 2-5µm. To maximize yield, it is critical that all vias are revealed to a uniform height, which can be extremely challenging if the incoming wafer thickness varies across a wafer or from one wafer to the next. In the 1st generation Rapier and now the new Rapier XE system, issues of wafer-to-wafer silicon thickness variation is overcome with the use of the ReVia endpoint system.

New valve series offers improved flow performance and reduced energy consumption

GF Piping Systems' Type 514-519 High Flow Diaphragm Valve Series is uniquely designed valve that provides a true break-through for weir style valves. The valve features an optimized, turbulence-free flow geometry that offers significantly increased flow rate performance and lower energy consumption. These features expand the valve's suitability for applications where diaphragm valves were previously not considered due to flow restriction.

The valve's new flow geometry design provides Cv values that on average are more than double those of a diaphragm valve with a traditional design. The modified geometry provides linear flow and control characteristics that improve processing stability, resulting in reduced operating costs and more cost-effective media transport. A self-draining feature minimizes dead space and achieves improved hygiene and better resistance to crystallizing fluids.

The innovative valve design also eliminates the need for metal bolts required to hold traditional valves together. Instead, the bonnet is threaded directly onto the body, eliminating the need to re-torque the bolts due to thermal expansion. With its metal-free threaded bonnet connection, corrosive build-up is minimized in applications with highly aggressive media.

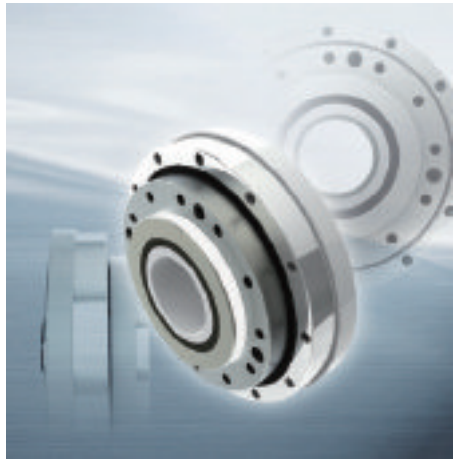
New Products

Assembléon's new 7 micron Hybrid solution

Assembléon will present its 7 micron Hybrid solution, the only system incorporating a single/pick single/place concept, now capable of 7 micron placement accuracy. The advantage of a Placement Head that carries only one component at a time is that, at full speed, its process can be fully optimized, monitored and controlled during the complete pick, dip and place cycle. The unique incorporated low-force closed-loop placement process takes care that even the thinnest devices can be placed accurate and its incorporated impact control takes care that no impact forces are applied during placement to guarantee the highest quality. It is therefore the only system that has very high production yields with an established placement defect rate lower than 1 defect per million placements (< 1 dpm). Besides the placement quality, it brings the traditional ingredients of the PCB assembly market, such as application flexibility, very high speed, accuracy, efficiency and cost control, along into the Advanced Packaging and Embedded Component Packaging markets.

The unique Hybrid, a cross-over platform between the PCBA market, WLP, SIP and ECP markets, combine high speed passive placements (up to 121,000 passives per hour) with high speed flip chip placement (up to 27,000 flip chips per hour) with flip chip accuracies at 7 microns at any placement location and angle on a substrate. The controllable placement Z-axis can adapt its placement height search algorithms for different heights, optimizing its placement force and process for 2.5D mounting, Package on Package or Embedded Passive and Active Devices applications.

Harmonic Drive introduces lighter gearheads



Harmonic Drive's new CSF/CSG-LW Precision Lightweight Gearheads is ideally suited for robotic applications, the new CSG-LW and CSF-LW gearheads are 30% lighter than previous designs without reducing the torque rating or significantly changing interface dimensions. The CSG high-torque gearhead delivers 30% more torque and 40% longer life with zero-backlash, 1 arc-min accuracy, and ±5 arc-sec repeatability. A high capacity cross roller bearing and output flange is used to support the driven load. A wide variety of sizes and reduction ratios are available with peak torques ranging from 450 in-lbs. to 60,500 in-lbs.

INFICON Transpector increases yield and maximizes uptime

The INFICON Transpector MPH Gas Analysis System is designed to "unlock your process" with industry leading performance for gas analysis applications to help maximize chip yields and minimize tool downtime. INFICON has leveraged its expertise in gas analysis process control equipment to create an RGA with industry-leading data collection speed (1 ms measurement time), minimum detectable partial pressure (<5E-15 Torr) and increased signal-to-noise ratio.

Transpector MPH is optimized for both common semiconductor RGA applications (like leak checking and contamination detection) and more demanding applications that are unavailable to other RGAs (Interwafer Monitoring, Photoresist). The unparalleled speed and sensitivity improve the quality and statistical validity of the RGA data, which increases the accuracy of Fault Detection Classification and other process control metrics.

New Products

White Knight to showcase electronic metering pumps

White Knight PEM050 electronic metering pumps dispense up to 50 ml of high-purity chemical with ±0.01% repeatability at high pressures (60-80 psi). The pumps feature swept PTFE fluid paths with fully-supported rolling diaphragms to maximize chemical compatibility and discharge capabilities. Positive control valves ensure accuracy by eliminating variability typical of check valves.

The pumps offer adjustable flow rates for use in single-wafer processing tools or premix vessels to ensure exact chemistry mixtures and allow for in-situ mixing directly at the head. They are ideal for chemical replenishing, blending, dosing, and spiking applications, as well as uses in cleaning of CVD equipment, photolithography, etch and clean processes, and blending chemical into process tanks prior to the introduction of substrates.

PEM050 pumps feature up to 5 ports with independently-controlled valves and programmable system logic. This enables a single PEM050 pump to deliver chemical to as many as 5 separate locations. They offer adjustable flow rates for use in single-wafer processing tools or in premix vessels to ensure exact chemistry mixtures, and they allow for in-situ mixing directly into the process stream.

With a discharge pressure rating of 60 psi and accuracy of ±0.01%, the pumps can eliminate the need for mixing vessels and other complex, expensive weight-based mixing systems, by injecting metered chemical directly into the process line.

LD Micro Precision introduces new LD Solder Paste/Epoxy Mixer

The LD Solder Paste Mixer (LD-SPM-101) will help to achieve a higher yield in the die attach process. Test results have shown a consistent improvement of approximate 30% adhesion strength and better dot size diameter variation improvement, approximately 30%.

The LD Solder PasteMixer (LD-SPM-101) is both a mixer and softener specifically designed for industrial epoxy, solder paste, medical, foodstuff (paste) paints, cosmetic cream etc applications. Contamination of the content is eliminated as the mixing process is done in an enclosed environment. Non-contact mixing!

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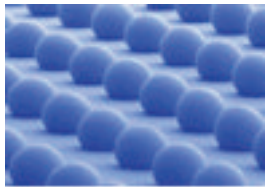

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Solid State TECHNOLOGY®

Coming Next Month:

CMOS Image Sensors

Authors from CMOSIS present different GS pixel architectures and technologies; compare performances. We will also give an outlook on further developments to be expected. The combination and implications of combining Backside Illumination (BSI) and GS operation are also discussed.

Thin Layer Etching

Nicolas Posseme from CEA/Leti presents an alternative etching process for thin layer etching with the proof of concept obtained on nitride spacer etching stopping on SiGe silicon for FDSOI applications. He explains the concept of this new etching approach showing that you can etch silicon nitride without foot formation and no SiGe recess whatever the over etch of your silicon film.

ad index

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A call to provide advanced equipment to growth companies

Historically, the major semiconductor capital equipment manufacturers have focused on supporting the bigger semiconductor companies at the expense of the smaller ones. The last decade's round of consolidations in the manufacturing and equipment sectors has only exacerbated this trend. This approach may make good business sense for the large equipment companies, but it's created a serious challenge for smaller IC manufacturers. Even worse, it now threatens to stifle the continuing innovation on which the high tech industry depends.

It's hard to fault the big equipment players for their business model. It's much more cost-effective and profitable to dedicate the bulk of your resources to those customers who want to buy multiple process tools featuring "bleeding edge" technology on highly automated, volume production platforms. In many cases, it's simply not as profitable to engage with smaller customers.

So what choice do the manufacturers have for populating their fabs if they're running 200mm or smaller wafers? One alternative is to buy refurbished tools, assuming they can find a tool that meets their needs, which is not always easy. Another is to buy a bigger tool with more performance capabilities than they need, which busts their equipment budget. There aren't many other options.

BYRON EXARCOS, *President,* **CLASSONE TECHNOLOGY**

Now, one could dismiss this issue by simply saying, that's the way this market works.

Continued growth in our industry has always depended on a certain path of continual innovation. "Smaller, faster, cheaper"— producing smaller, more powerful chips in ever greater volume on larger wafers was a highly successful means of turning computers and subsequent mobile computing and communication devices into household items. It's hard to fault a business/technology model that has been successful for so many years.

On the other hand, every emerging market eventually matures. We've all experienced the boom-and-bust cycles that roil our industry and what happens when the "last big thing" plateaus or dries up. Today, the capital equipment market is at a cusp. We need to examine whether the traditional smaller-design-rules/bigger-wafers/faster-throughput approach is helping or hindering the introduction of new technologies.

Today's emerging technologies include devices such as smart sensors, power and RF wireless devices. The fact is, many of these chips can be made quite well and quite profitably using larger design rules on 200mm or even smaller substrates. However, many of the companies developing these devices are not huge enterprises, and they're hampered by the unavailability of tools delivering the appropriate levels of process technology, automation and throughput — at a price they can afford. Ironically, our industry is in a phase where the equipment companies that once drove significant innovations, such as the introduction of copper deposition and low-k dielectrics, have become so large and narrowly focused that they're impeding the development of many other emerging technologies.

I have some understanding of the needs of smaller device manufacturers because one of our companies, ClassOne Equipment, has been selling refurbished equipment to them for over a decade. That is why we've now created a whole new company, ClassOne Technology, to provide new equipment at substantially lower prices specifically for 200mm and smaller substrates. We are introducing new electroplating systems, spin rinse dryers and spray solvent tools; and some of them are literally half the cost of high-end competitive units. We're particularly interested in serving all those small- to mid-sized companies who are making MEMS, power devices, RF, LEDs, photonics, sensors, microfluidics and other emerging-technology devices.

However, no single company can solve the entire problem. There is a glaring need for equipment manufacturers to bring the price/performance ratio of their tools back in line with the needs of more of the equipment users, not just those at the bleeding edge. If the tool manufacturers persist in trying to only sell the equivalent of sports cars to customers who just need pickup trucks, America's high tech industry may soon find itself trailing, rather than leading the innovation curve.

Satisfying the semiconductor industry's simultaneous demands for performance enhancement and cost reduction requires endless innovation.

Nikon leverages proven immersion technology to deliver ground-breaking solutions to extend 193 nm lithography and enable next-generation manufacturing.

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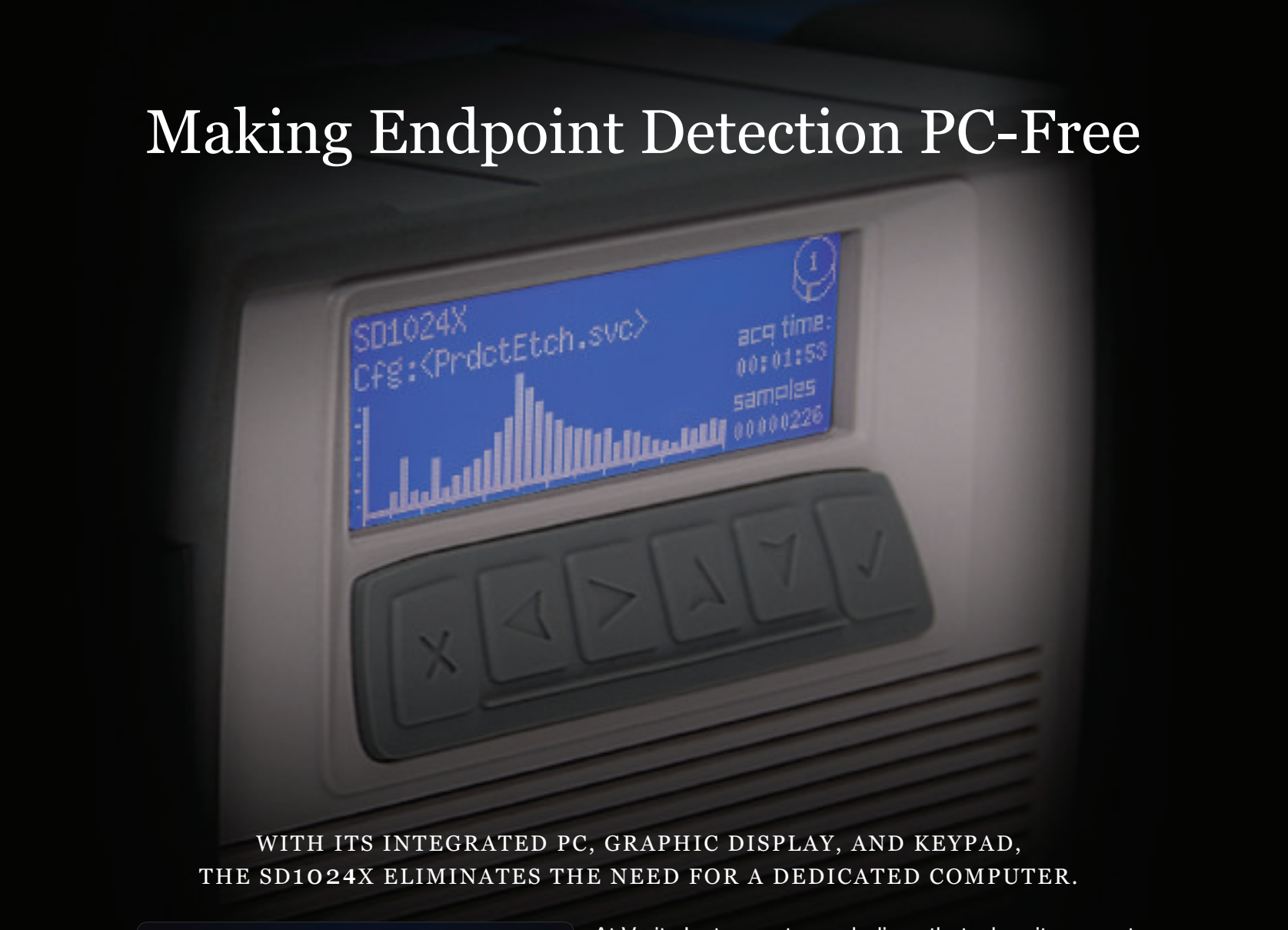

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