

Solid State TECHNOLOGY

Insights for Electronics Manufacturing

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Engineered SOI substrates are now a mainstream option for the semiconductor industry.

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Blood and tears at DAC

At this year's Design Automation Conference (DAC) in San Francisco, Brian Otis, a Director at Google, talked about how hundreds of millions of people are at risk of diabetes – and how a smart contact lens that continuously monitors blood glucose levels and transmits the data to a smartphone might just be the ideal solution.

There is a good correlation between your glucose levels in tears and that in blood (although it's a factor of magnitude lower), so a smart contact lens can measure glucose levels using a wireless chip

"What makes this all possible is the work that the semiconductor industry has done"

and miniaturized glucose sensor. The devices are embedded between two layers of soft contact lens material.

Google announced the smart lens project in January of 2014, at which time multiple clinical studies had been completed. A partnership was subsequently announced with Novartis's Alcon eye-care division in July of 2014.

Otis said that the universe of people who are either bona fide pre-diabetic or at risk is huge. "It's hundreds

of millions of people," he said. "Our hypothesis is that if we are able to create more comfortable CGMs (continuous glucose monitors), this will significantly impact the diabetes management problem we're facing. No one has solved this problem yet, but we really want to do this because it could improve people's lives," he said.

A smart contact lens could solve the problem because it's a wearable device that many millions of people already wear on a daily basis. "If there is an option of wearing the device that many people wear, that's comfortable and also corrects your vision and gives you this valuable information, you're likely to do that over than, let's say, pricking your finger," Otis said.

Otis described smart contact lenses as not just another gadget. "It's really part of an ecosystem that can form a new type of proactive healthcare. We're going to work really hard on that," he said.

What makes this all possible, of course, is the work that the semiconductor industry has done in miniaturization over the last several decades. Otis said more work is needed: "The chips, the passive components, the power supplies, the antennas: Everything needs to shrink," he said.

—Pete Singer, Editor-in-Chief

Solid State TECHNOLOGY

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Web Exclusives

3DIC Technology Drivers and Roadmaps

Ed Korczynski, Sr. Technical Editor describes how, after 15 years of targeted R&D, through-silicon via (TSV) formation technology has been established for various applications. There are now detailed roadmaps for different types of 3-dimensional (3D) ICs well established in industry.

<http://bit.ly/1lufRdm>

Conference features the latest in flexible display technology

At Display Week 2015, bigger is better. Smaller is better. And flexible may be best of all, for the era of wearable electronics. There are some huge screens on display, so to speak, throughout the conference's exhibition floor, such as BOE Technology Group's 110-inch 8K Ultra High Definition television or LG Display's curved 77-inch 4K UHD TV. There are also very small displays, such as E Ink's smallest electronic shelf labels. (From SemiMD, part of the Solid State Technology network)

<http://bit.ly/1G9HGup>

The ConFab: The semi industry is now mature

The conference portion of The ConFab 2015 started with an afternoon panel session, "Exploring the Edges of Semiconductor Technology and Business." Dick James kicked it off with a presentation on the state of the art in the business, as seen by Chipworks, followed by a panel discussion with James, Phil Garrou, and Gopal Rao.

<http://bit.ly/1JVjQUx>

Isolating electrical faults in advanced IC devices

Yield improvement and production engineers working on today's ICs encounter many challenges as defects affecting device operation go undetected by traditional in-line techniques. Electrical Failure Analysis (EFA) is a suite of techniques that helps the modern day fab increase yields by isolating faults to areas small enough for Physical Failure Analysis (PFA). In this webinar, we showcase a few of the proven EFA fault isolation techniques and describe how EFA helps to characterize the underlying defects.

<http://bit.ly/1JYnLQn>



Insights from the Leading Edge: Advanced Packaging at The ConFab

At the recent ConFab meeting in Las Vegas, aside from all the talk about consolidation, Bill Chen from ASE and Li Li from Cisco put together a great Advanced Packaging session.

<http://bit.ly/1Bglixz>

EUV lithography: What's next and when?

This year started with an announcement, during the SPIE AL Conference, of the achievement of 100 W+ power from high volume manufacturing (HVM) EUV sources in the fab. One hundred watts at intermediate focus has been a long-standing benchmark and is a definite success, and we also can be sure that source power and availability will increase this year. The focus will now change to addressing the remaining challenges of EUVL, with questions turning on what comes next and when, as the industry prepares to deploy EUVL into HVM.

<http://bit.ly/1BUUejP>

Many **THANKS** to the attendees, speakers and sponsors who made The ConFab 2015 a resounding success. We look forward to another great event in 2016!



Key Executives from these organizations were at The ConFab 2015:

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Applied Seals
ASE Group
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Astronics Test Systems
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USA – Fairchild Semiconductor launched its first product line of MEMS products.

USA – Avago Technologies announced plans to acquire **Broadcom** for \$37B.

ASIA – A research team at **KAIST** announced it has developed the first flexible phase-change random access memory

USA – DCG Systems, Inc. announced it has acquired **MultiProbe, Inc.**

EUROPE – imec announced at Intersolar Europe a new efficiency record for its large area n-type PERT crystalline silicon solar cell, now reaching 22.5 percent (calibrated at ISE CalLab).

ASIA – Sankalp Semiconductor announced FD-SOI services and IP partnership with **STMicroelectronics**.

EUROPE – CEA-Leti announced during the Design Automation Conference that seven partners have joined its new FD-SOI IC development program, Silicon Impulse.

USA – Pixelligent closed \$3.4 million in new funding.

EUROPE – Europe's leading nano-electronics institutes, **Tyndall National Institute** in Ireland, **CEA-Leti** in France and **imec** in Belgium, have entered a €4.7 million collaborative open-access project called **ASCENT** (Access to European Nanoelectronics Network).

ASIA – SK Hynix Inc. announced that it is shipping mass production volumes of 1st generation High Bandwidth Memory based on its advanced 20nm-class DRAM process technology.

NXP Semiconductors announces agreement to sell RF power business

NXP Semiconductors N.V. announced an agreement that will facilitate the sale of its RF Power business to Jianguang Asset Management Co. Ltd. Under the terms of the agreement JAC Capital will pay \$1.8 billion for the business.

The NXP RF Power business is one of the market leaders in high performance RF power amplifiers primarily focused on the cellular base station market, but with potential future growth applications in the areas of industrial lighting, next generation cooking and automotive electronic ignition systems.

"The creation of a new company focused on the RF power amplifier market is a ground breaking transaction for JAC Capital and a great deal for our customers. Although we would have expected a higher

valuation in a regular disposal, JAC Capital's ability to support continued growth and development of the business and its ability to sign and close a transaction rapidly was a key factor in enabling the best outcome for our customers and shareholders, as well as supporting the closure of the merger with Freescale Semiconductor," said Richard Clemmer, NXP Chief Executive Officer.

"We are happy to reach an agreement to acquire the RF Power business from NXP with its strong team and established technology. We will keep on increasing investment in R&D, manufacturing and customer service of the new company to strengthen its market position. JAC Capital and its shareholders will also help the new company to maintain fast and

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"Easy does it" — Fabs trim spending plans

By Christian G. Dieseldorff, Industry Research & Statistics Group, SEMI

Semiconductor capital expenditures (without fabless and backend) are expected to slow in rate, but continue to grow by 5.8 percent in 2015 (over US\$66 billion) and 2.5 percent in 2016 (over \$68 billion), according to the May update of the SEMI World Fab Forecast report. A significant part of this capex is fab equipment spending.

Fab equipment spending is forecast to depart from the typical historic trend over the past 15 years of two years of spending growth followed by one year of decline. Departing from the norm, equipment spending could grow every year for three years in a row: 2014, 2015, and 2016 (see Table 1).

At the end of May 2015, SEMI published its latest update to the World Fab Forecast report, reporting on more than 200 facilities with equipment spending in 2015, and more than 175 facilities projected to spend in 2016.

Continued on page 12

Avago Technologies acquisition of Broadcom creates new semiconductor powerhouse

Merger activity in the semiconductor industry moved to a new level with the announcement of the agreement for Avago Technologies to acquire Broadcom, according to IHS Inc., a global source of critical information and insight. The deal, which is valued at \$37 billion in cash and stock, will create a new company valued at \$77 billion.

"This is the latest and, by far the largest, merger in the semiconductor industry, as major players continue to move in an aggressive way to establish position and profitability in key segments of the industry," said Dale Ford, vice president and chief analyst for IHS Technology. "Investors have responded favorably to the announcement, with promised bottom-line benefits derived from realized cost savings."

The combined revenues of the two companies in 2014 exceeds \$14 billion, making the newly merged semiconductor company the sixth-largest globally, according to final annual semiconductor market shares. More significantly, the combination of the two companies creates the third-largest semiconductor supplier, trailing only Intel and Qualcomm, if memory integrated-circuit (IC) revenues are excluded. "The complementary product portfolios of the two companies move them into a powerful position, in both the communications IC market and the storage IC market," Ford said.

Quadrupling in size in two years

This latest move from Avago Technologies has formed a company with revenues four times greater than in 2013. The two biggest recent mergers by Avago Technologies were the acquisition of LSI in 2014 and this new acquisition of Broadcom. The mergers increase the company's strength in the communications and storage categories. Outside of these two areas, Broadcom has a much smaller presence in consumer electronics and industrial electronics and almost no revenue from other data processing and automotive electronics.

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MEMS suppliers ride automotive safety wave

Suppliers of MEMS-based devices rode a safety sensing wave in 2014 to reach record turnover in automotive applications, according to analysis from IHS, a global source of critical information and insight.

Mandated safety systems such as Electronic Stability Control (ESC) and Tire Pressure Monitoring Systems (TPMS) – which attained full implementation in new vehicles in major automotive markets last year – are currently driving revenues for MEMS sensors. Those players with strong positions in gyroscopes, accelerometers and pressure sensors needed in these systems grew as well, while companies in established areas like high-g accelerometers for frontal airbags and pressure sensors for side airbags also saw success.

Major suppliers of pressure sensors to engines similarly blossomed – for staple functions like manifold absolute air intake and altitude sensing – but also for fast-growing applications like vacuum brake boosting, gasoline direct injection and fuel system vapor pressure sensing.

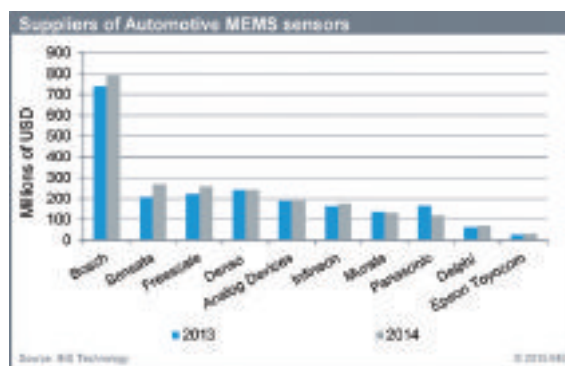
Bosch was the overall number one MEMS supplier with US\$790 million of devices sold last year, close to three times that of its nearest competitor, Sensata (US\$268 million). Bosch has a portfolio of MEMS devices covering pressure, flow, accelerometers and gyroscopes, and also has a leading position in more than 10 key applications. The company grew strongly in ESC and roll-over detection applications, and key engine measurements like manifold absolute pressure (MAP) and mass air flow on the air intake, vacuum brake booster pressure sensing and common rail diesel pressure measurement.

Compared to 2013, Sensata jumped to second place in 2014 ahead of Denso and Freescale, largely on strength in both safety and powertrain pressure sensors, but also through its acquisition of Schrader Electronics, which provides Sensata with a leading position among tire pressure-monitoring sensor suppliers.

While Sensata is dominant in TPMS and ESC pressure sensors, it also leads in harsh applications like exhaust

gas pressure measurement. Freescale, on the other hand, is second to Bosch in airbag sensors and has made great strides in its supply of pressure sensors for TPMS applications.

Despite good results in 2014, Denso dropped two places compared to its overall second place in 2013, largely as a result of the weakened Yen. Denso excelled in MAP and barometric pressure measurement in 2014, but also ESC pressure and accelerometers. Denso has leadership in MEMS-based air conditioning sensing and pressure sensors for continuous variable transmission systems, and is also a supplier of exhaust pressure sensors to a major European OEM.



Secure in its fifth place, Analog Devices was again well positioned with its high-g accelerometers and gyroscopes in safety sensing, e.g. for airbag and ESC vehicle dynamics systems, respectively.

The next three players in the top 10, in order, Infineon, Murata and Panasonic, likewise have key sensors to offer for safety. Infineon is among the leading suppliers

of pressure sensors to TPMS systems, while Murata and Panasonic serve ESC with gyroscope and accelerometers to major Tier Ones.

The top 10 represents 78 percent of the automotive MEMS market volume, which reached \$2.6 billion in 2014. By 2021, this market will grow to \$3.4 billion, a CAGR of 3.4 percent, given expected growth for four main sensors – pressure, flow, gyroscopes and accelerometers. In addition, night-vision microbolometers from FLIR and ULIS and humidity sensors from companies like Sensirion and E+E Elektronik for window defogging will also add to the diversity of the mix in 2021.

DLP chips from Texas Instruments for advanced infotainment displays will similarly bolster the market further in future. More details can be found in the IHS Technology H1 2015 report on Automotive MEMS. ◀

Continued from page 6

stable growth through our network of worldwide financial institutions, industrial leaders and JAC Capital's management team with many years of experience in the semiconductor and telecom industry," said Brighten Li, Chairman of JAC Capital Investment Evaluation Committee.

Under the agreement, the entire scope of the NXP RF Power business and approximately 2,000 NXP employees who are primarily engaged globally in the RF Power business, including its entire management team, are to be transferred to an independent company incorporated in the Netherlands, which

will be 100 percent acquired by JAC Capital upon closing of the transaction. Additionally, all relevant patents and intellectual property associated with the RF Power business will be transferred in the sale, as well as the NXP back-end manufacturing operation in the Philippines that is focused on advanced package, test and assembly of RF Power products.

The transaction, including the entry into and the terms of the definitive agreements and the approval of JAC Capital as the acquirer are subject to review and approval by the US Federal Trade Commission, the European Commission,

MOFCOM and other agencies in connection with their review of NXP's proposed acquisition of Freescale Semiconductor, Ltd.

NXP and JAC Capital expect the sale to close within the second half of 2015, pending required regulatory approval and employee representative consultations. NXP anticipates the sale of its RF Power business to be dilutive to earnings on a stand-alone basis in the fourth quarter 2015 and 2016. Proceeds from the sale of the RF Power business will be used to partly fund the previously announced acquisition of Freescale Semiconductor, Ltd. ◀

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The report shows a large increase in spending for DRAM, more than 45 percent in 2015. Also, spending for 3D NAND is expected to increase by more than 60 percent in 2015 and more than 70 percent in 2016. The foundry sector is forecast to show 10 percent higher fab equipment spending in 2015, but may experience a decline in 2016. Even with this slowdown, the foundry sector is expected to be the second largest in equipment spending, surpassed only by spending in the memory sector.

A weak first quarter of 2015 is dropping spending for the first half of 2015, but a stronger second half of 2015 is expected. Intel and TSMC reduced their capital expenditure plans for 2015, while other companies, especially memory, are expected to increase their spending.

The SEMI data details how this varies by company and fab. For example, the report predicts increased fab equipment spending in 2015 by TSMC and Samsung. Samsung is the "wild card" on the table, with new fabs in Hwaseong, Line 17 and S3. The World Fab Forecast report shows how Samsung is likely to ramp these fabs into 2016. In addition, Samsung is currently ramping a large fab in China for 3D NAND (VNAND) production. Overall, the data show that Samsung is will likely spend a bit more for memory in 2015 and much more in 2016. After two years of declining spending for System LSI, Samsung is forecast to show an increase in 2015, and especially for 2016.

Figure 1 depicts fab equipment spending by region for 2015.

In 2015, fab equipment spending by Taiwan and Korea together are expected to make up over 51 percent of world-wide spending, according to the SEMI report. In 2011, Taiwan and Korea accounted for just 41 percent, and the highest spending region was the Americas, with 22 percent (now just 16 percent). China's fab spending is still dominated by non-Chinese companies such as SK Hynix and Samsung, but the impact of Samsung's 3D NAND project in Xian is significant. China's share for fab spending grew from 9 percent in 2011 to a projected 11 percent in 2015; because of Samsung's fab in Xian, the share will grow to 13 percent in 2016.

Fab Equipment Spending 2015



FIGURE 1.

Fab Equipment Spending by Node

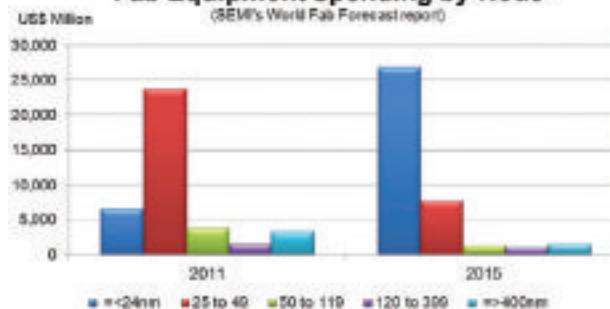


FIGURE 2.

Fab Equipment Spending

in US\$ Million	2011	2012	2013	2014	2015	2016
300mm	\$ 33,500	\$ 29,580	\$ 27,070	\$31,166	\$35,415	\$38,566
=<200mm	\$ 5,916	\$ 3,262	\$ 2,951	\$ 3,686	\$ 3,251	\$ 2,168
Total	\$ 39,416	\$ 32,842	\$ 30,021	\$ 34,852	\$ 38,666	\$ 40,734
Change %	16%	-17%	-9%	16%	11%	5%

Source: SEMI's World Fab Forecast report (May 2015)

TABLE 1.

Table 2 shows the share of the top two companies drive a region for fab equipment spending:

Over time, fab equipment spending has also shifted by technology node. See Figure 2, where nodes have been grouped by size:

In 2011, most fab equipment spending was for nodes between 25nm to 49nm (accounting for \$24 billion) while nodes with 24nm or smaller drove spending less than \$7 billion. By 2015, spending flipped, with nodes equal or

under 24nm accounting for \$27 billion while spending on nodes between 25nm to 49nm dropped to \$8 billion. The SEMI World Fab data also predict more spending on nodes between 38nm to 79nm, due to increases in the 3DNAND sector in 2015 and accelerating in 2016 (not shown in the chart).

When is the next contraction?

As noted above, over the past 15 years the industry has never achieved three consecutive years of positive growth rates for spending. 2016 may be the year which deviates from this historic cycle pattern. A developing hypothesis is that with more consolidation, fewer players compete for market positions, resulting in a more controlled spending environment with much lower volatility.

Learn more about the SEMI fab databases at:
www.semi.org/MarketInfo/FabDatabase. ◀

Region	Largest spending 2015	Share
Americas	1. Globalfoundries 2. Intel	36% 31%
China	1. Samsung 2. SMIC	30% 27%
Europe & Mideast	1. Intel 2. Globalfoundries	54% 15%
Japan	1. Flash Alliance 2. Sony	57% 21%
Korea	1. Samsung 2. sk hynix	66% 33%
SE Asia	1. Micron 2. Globalfoundries	71% 17%
Taiwan	1. TSMC 2. Inotera	65% 14%

Source: SEMI's World Fab Forecast report (May 2015)

TABLE 2.



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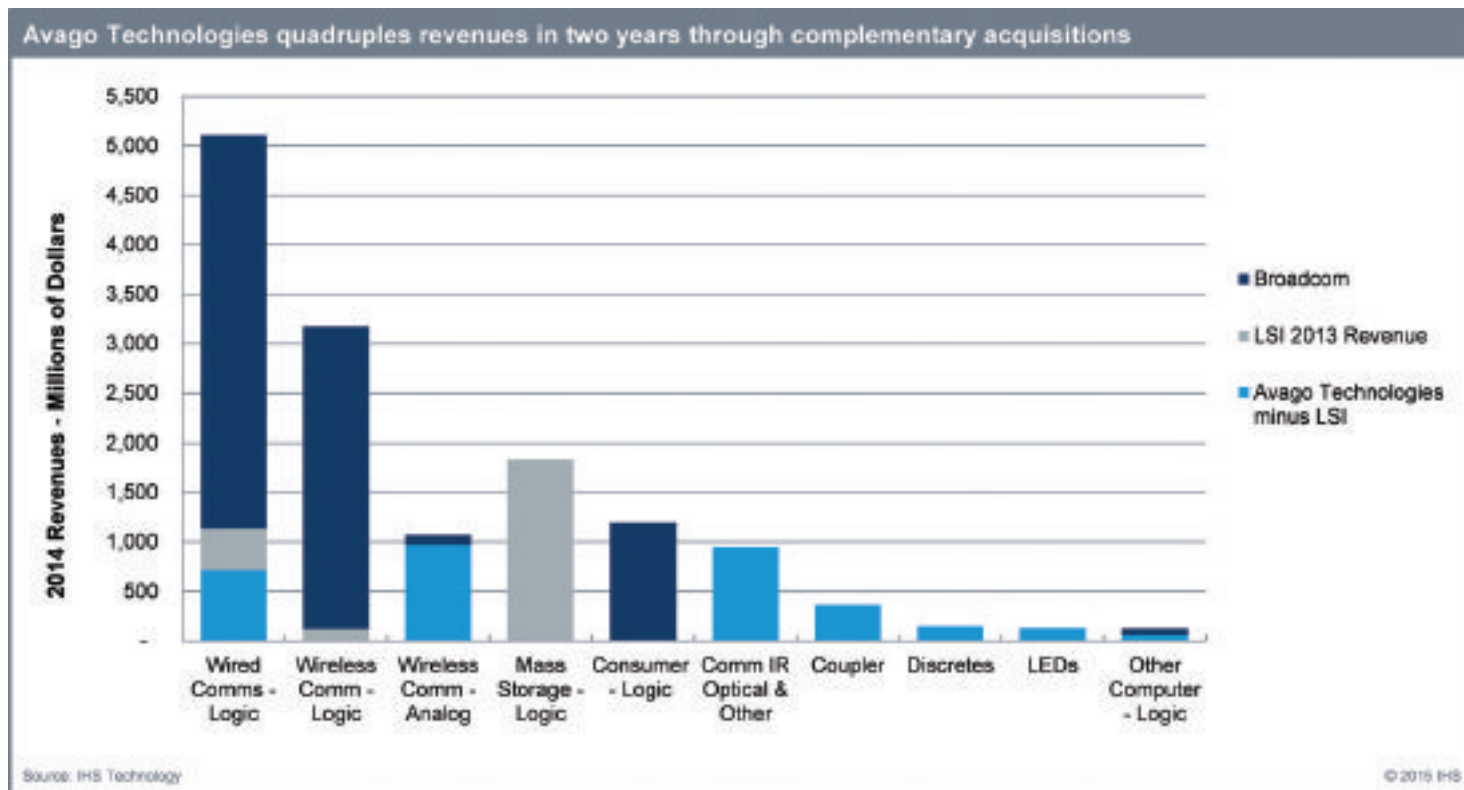
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Communications focus

The newly merged Avago-Broadcom will dominate the market, commanding 40 percent of the wired communications IC market, excluding memory. Revenues for this category in 2014 were more than five times larger than the next largest supplier, Intel.

The merged company will boost its share of the wireless communications IC market to nearly 8 percent, ranking fourth behind Qualcomm, Samsung Electronics and MediaTek. With an overall market share of 14 percent for all communications ICs, the company ranks second, trailing only Qualcomm and ahead of Samsung Electronics.

The strength of the merged Avago/Broadcom in the wired communications market positions it to benefit from the strong projected market growth. The five-

year compound annual growth rate (CAGR) for wired communications is 7 percent, leading all other market segments. On the other hand, semiconductors used in wireless communications products is projected to go through a period of weak growth at only 2 percent CAGR over the next five years. "The size of the combined company could give it a strong position to increase its market share over this time," Ford said.

Cost savings rolling to the bottom line

The companies predict \$750 million in annual cost synergies in 18 months. A quick look at the distribution of their revenues shows that 66 percent of Avago Technologies' revenue comes from products shipped to the Asia-Pacific (APAC) region, for use in electronics production. Broadcom derived 93 percent of its revenues from APAC shipments of its ICs. "The alignment of the supply chain between the two companies will facilitate the projected savings," Ford said. ♦

AMD announces HBM in 2015

For over two years now, I have been saying that memory stacks will soon be seen in high end graphics processor modules. Nvidia was the first to announce the use of stacked memory with GPUs. Nvidia's Volta GPU module was scheduled for 2015 release and was supposed to use the Micron Hybrid Memory Cube (HMC). Rumors are that after HMC's development fell behind the proposed roadmap timing, Nvidia moved the Volta introduction out to > 2016 after the Pascal module, which will be based on Hynix HBM 2, scheduled to be commercial in 2016.

Now the first commercial graphics products to feature HBM clearly will be AMD's R9 390X series Fiji GPU in 2015. The Rx 300 series will also reportedly be the first to feature TSMC's 20nm technology and the first to be equipped with HBM. There are 4 HBM stacks packed on the same interposer as Fiji. Each HBM stack has a capacity of 1GB of memory.

Recent rumors from Taiwan indicate that production is being slowed by issues concerning delivery of the silicon interposers from their primary supplier. Reports are that AMD is having to rely more heavily on the secondary supplier to try to keep production on track.

The first generation of HBM promises to deliver 4.5X the bandwidth of GDDR5 and 16X the bandwidth DDR3 as shown in Figure 1.

The second generation HBM is well underway and promises to double the bandwidth by doubling the speed from 1Gbps to 2Gbps. It will also quadruple the memory capacity for 4-Hi stacks from 1GB to 4GB.

Reportedly HBM2 is scheduled to be featured in AMD's upcoming "Greenland" GPU. It's rumored that the new graphics family will be manufactured at GlobalFoundries on their 14nm FinFET process node; that would be a major loss for TSMC. A summary of AMD graphics processor modules is shown in Figure 2.

There are also reports that AMD is working on multicore APUs that will use similar interposer / HBM memory technology. ♦



Dr. Phil Garrou,
Contributing Editor

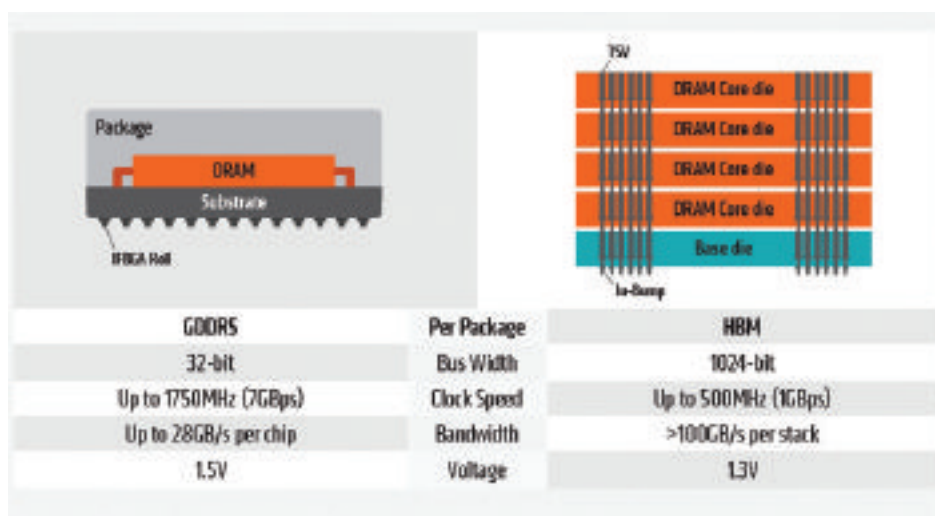


FIGURE 1. Comparison of HBM and other DRAMs. Source: SK Hynix.

WCCFTech	Year	Process	Flagship GPU	Product	Memory	Bandwidth
Southern Islands	2012	28nm	Tahiti	HD 7970	3GB GDDR5	264GB/s
Volcanic Islands	2013	28nm	Hawaii	R9 290X	4GB GDDR5	320GB/s
Pirate/Caribbean Islands	2015	28nm	Fiji	R9 390X	8GB HBM1	640GB/s
Arctic Islands	2016	14nm	Greenland	R9 490X	16GB HBM2	1TB/s

FIGURE 2. AMD graphics processor modules.

Packaging



Silicon technology extensions

In the spring meeting of the Materials Research Society held recently in San Francisco, Symposium A: Emerging Silicon Science and Technology included presentations on controlling the structure of crystalline spheres and thin-films. Such structures could be used in future complementary metal-oxide semiconductor (CMOS) devices and in photonic circuits built using silicon.

Alexander Gumennik, et al., from the Massachusetts Institute of Technology, presented on “Extraordinary Stress in Silicon Spheres via Anomalous In-Fiber Expansion” as a way to control the bandgap of silicon and thus enable the use of silicon for photodetection at higher wavelengths. A silica fiber with a crystalline silicon core is fed through a flame yielding spherical silicon droplets via capillary instabilities. Upon cooling the spheres solidify and expand against the stiff silica cladding generating high stress conditions. Band gap shifts of 0.05 eV to the red (in Si) are observed, corresponding to internal stress levels. These stress levels exceed the surface stress as measured through birefringence measurements by an order of magnitude, thus hinting at a pressure-focusing mechanism. The effects of the solidification kinetics on the stress levels reached inside the spheres were explored, and the experimental results were found to be in agreement with a pressure-focusing mechanism arising from radial solidification of the spheres from the outer shell to the center. The simplicity of this approach presents compelling opportunities for the achievement of unusual phases and chemical reactions that would occur under high-pressure high-temperature conditions, which therefore opens up a pathway towards the realization of new in-fiber optoelectronic devices.

Fabio Carta and others from Columbia University working with researchers from IBM showed results on “Excimer Laser Crystallization of Silicon Thin Films on Low-K Dielectrics for Monolithic 3D Integration.” This research

supports the “Monolithic 3D” (M3D) approach to 3D CMOS integration as popularized by CEA-LETI,

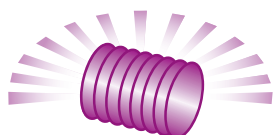
as opposed to the use of Through Silicon Vias (TSV). M3D requires processing temperature below 400°C if copper interconnects and low-k dielectric will be used in the bottom layer. Excimer laser crystallization (ELC) takes advantage of a short laser pulse to fully melt the amorphous silicon layer without allowing excessive time for the heat to spread throughout the structure, achieving large grain polycrystalline layer on top of temperature sensitive substrates. The team crystallized 100nm thick amorphous silicon layers on top of SiO₂ and SiCOH (low-k) dielectrics. SEM micrographs show that post-ELC polycrystalline silicon is characterized by micron-long grains with an average width of 543 nm for the SiO₂ sample and 570 nm for the low-k samples. A 1D simulation of the crystallization process on a back end of line structure shows that interconnect lines experience a maximum temperature lower than 70°C for the 0.5 μm dielectric, which makes ELC on low-k a viable pathway for achieving monolithic integration.

Seiji Morisaki, et al., from Hiroshima Univ, showed results for “Micro-Thermal-Plasma-Jet Crystallization of Amorphous Silicon Strips and High-Speed Operation of CMOS Circuit.” The researchers used micro-thermal-plasma-jet (μ-TPJ) for zone melting recrystallization (ZMR) of amorphous silicon (a-Si) films to form lateral grains larger than 60 μm. By applying ZMR on a-Si strip patterns with widths <3 μm, single liquid-solid interfaces move inside the strips and formation of random grain boundaries (GBs) are significantly suppressed. Applying such strip patterns to active channels of thin-film-transistors (TFTs) results in a demonstrated field effect mobility (μ_{FE}) higher than 300 cm²/V*s because they contain minimal grain-boundaries. These a-Si strip patterns were then used to characterize variability of n- and p-channel TFTs and CMOS ring oscillators. The strip patterns showed improved uniformities and defect densities, in general. A 9-stage ring oscillator fabricated with conventional TFTs had a maximum frequency (F_{max}) of operation of 58 MHz under supply voltage (V_{dd}) of 5V which corresponds to a 1-stage delay (τ) of 0.94 ns, while strip channel TFTs demonstrated 108 MHz F_{max} and τ decreased to 0.52 ns. ◀▶



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Substrate innovation for extending Moore and more than Moore

MARIAM SADAKA and CHRISTOPHE MALEVILLE, Soitec, Austin, TX and Grenoble, France

Engineered SOI substrates are now a mainstream option for the semiconductor industry.

The number of mobile subscribers worldwide reached 95.5% of the world's population in 2014 and is expected to reach 9.3B by 2019 (1). This fast growing trend is driving end markets towards satisfying stringent demands of mobile connected users. Whether it is a smartphone or a wearable device, the key requirements include low cost, extended battery life, more functionalities, smaller form factor, and fast time to market. In an effort to bring more performance, more functionality or less power consumption, innovation starting at the substrate level has demonstrated significant achievements. This includes implementing planar Fully Depleted Silicon-On-Insulator (FD-SOI) devices with full back bias capability to extend Moore's Law beyond 28nm and meet power/performance/cost requirements for low power SoCs. In addition, using High Resistivity SOI for integrating the RF Front End Module (FEM) providing significant die cost advantage with increased performance and functionality. In this paper, engineered substrates for next generation ultra-low power integrated digital and RF devices and other emerging applications will be discussed.

Device scaling and device functional diversification

Device scaling has been following Moore's law for the last five decades, doubling transistor density every two years, bringing higher performance, more functionality at lower cost. To maintain this trend, the industry implemented non-classical ways to continue on the scaling path. This started with innovation at the material level, then



FIGURE 1. Technology migration history [2].

innovation at the device structure level demonstrating improved electrostatic control enabled by fully depleted (FD) devices (**FIGURE 1**). FD devices include planar FD-SOI, vertical FinFET or multi-gate device structures. FD-SOI is a great example of device scaling in the substrate era, where the engineered substrate provides the fully depleted structure that solves the variability challenge and enables body bias capabilities to meet the power/performance and cost requirements for low power consumer SoCs.

The semiconductor industry also has another key focus called More-Than-Moore. This new trend provides added non-digital functional diversification without necessarily scaling according to Moore's Law. More-than-Moore technologies cover a wide range of domains, and there are numerous examples where advantages brought by substrate engineering enable better performance and more functionality. With the increasing demand for wireless data bandwidth and the emergence of LTE Advanced, new RF devices with higher levels of integration and more stringent specifications need to be developed. RF-SOI substrates are a great example of how engineered substrates play a major role in achieving

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the needed level of performance and integration. Two generations of High Resistivity SOI (HR-SOI) substrates compatible with standard CMOS processing were developed [3]. While Gen 1 HR-SOI is well suited for 2G and 3G requirements, Gen 2 HR-SOI enables much higher linearity and isolation meeting most stringent LTE Advanced requirements and thus is paving the way for higher levels of integration with better performance at an improved cost (**FIGURE 2**).

UTBB FD-SOI substrates

FD-SOI with ultra-thin Box, known as Ultra-Thin-Body and Box (UTBB) substrates, are an attractive candidate for extending Moore's Law at 28nm and beyond while keeping the cost benefit from shrinking. UTBB FD-SOI devices represent an extension of the planar device architecture demonstrating several advantages essential to low power SoCs.

FD-SOI devices have excellent immunity to Short Channel Effects (SCE) leading to improved sub-threshold swing and Drain-Induced Barrier Lowering (DIBL), and minimum Random Dopant Fluctuation (RDF), thanks to the undoped channel. This ensures lowest V_t variation [4,5], improves performance at lower V_{dd} as well as improves SRAM and analog mismatch and analog gain, allowing superior digital/analog co-integration [6].

UTBB FD-SOI devices combine the advantage of tuning the front gate and back gate work function [4] as well as enabling effective back bias capabilities for multi- V_t options (**FIGURE 3**). The back bias capability is a unique feature that enables V_t modulation for better trade-off of power and performance and can be effectively applied in a static or dynamic mode. Moreover, UTBB FD-SOI back bias capabilities show no degradation with scaling and offer a wider range of biasing versus bulk at no area penalty [5].

UTBB FD-SOI is a scalable technology supporting at least three nodes; 28nm, 14nm and 10nm (**FIGURE 4A**). The technology satisfies density/area, performance and power saving requirements without a disruptive change in device architecture and integration. Today, available foundry offerings demonstrate competitive performance at 28 & 22nm [1,7] and the technology is proven down to 10nm [8]. Scaling requires thinner SOI and BOX. In order to alleviate the constraints on SOI film thickness reduction, a scaling sequence

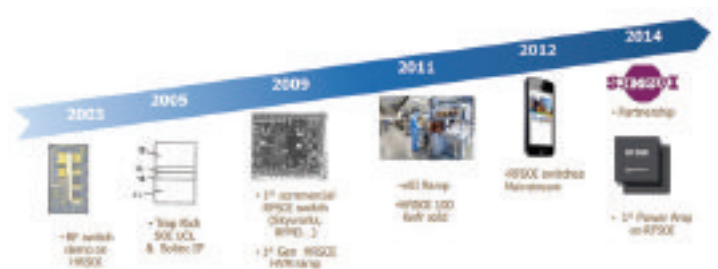


FIGURE 2. Soitec's RF-SOI leadership from ideas to high volume manufacturing.

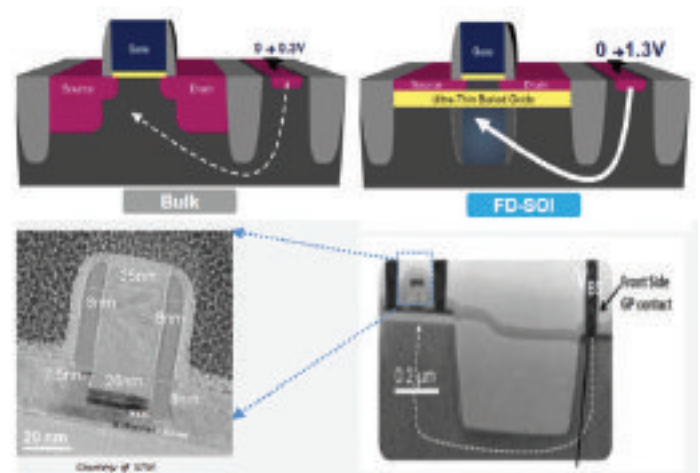


FIGURE 3. UTBB FD-SOI with Back Bias (Courtesy of ST Microelectronics).

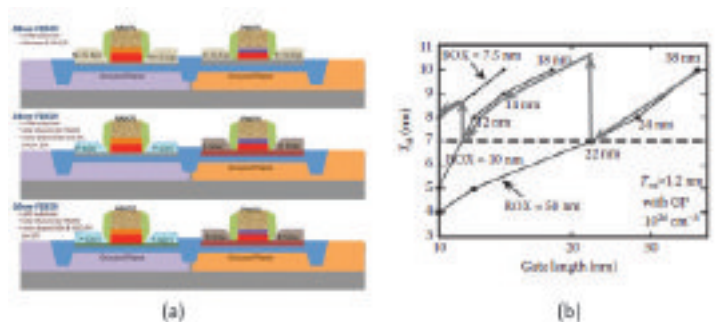


FIGURE 4. (a) UTBB FD-SOI Device integration supporting three nodes (11) (b) SOI/BOX thickness scaling ensuring a DIBL of 100 mV/V or below down to 7 nm node [9].

based on different BOX layer thickness was proposed, **FIGURE 4B** [9]. SOI substrates with 25nm BOX are already in production and 10 nm BOX has been demonstrated. Furthermore, the substrate roadmap beyond 14nm includes substrate strain engineering providing the advantage of enhancing the carrier mobility independent of device pitch. This includes strained silicon directly on insulator (SSOI) or strained SiGe-On-Insulator (SGOI) [10].

FD-SOI devices are planar devices that are fully

compatible with mainstream CMOS processing, designs and EDA tools, providing a faster time to market solution. In addition to fully leveraging conventional CMOS processes, FD-SOI process integration is simpler than bulk (**FIGURE 5**) [1, 12]. FD-SOI process saves several masks and process steps typically included for Vt tuning and for the integration of uniaxial stressors needed to boost performance in planar and FinFET bulk [13, 14]. Even with the drastically increasing lithography cost, such process simplifications more than compensate for the SOI substrate cost, resulting in a lower overall processed wafer cost [11].

While the vertical FinFET device features excellent gate control and high density/performance per area, it also requires a disruptive change in process and design resulting in higher cost and longer time to market. For applications that require the ultimate performance/digital integration and large die size, vertical FinFETs are a good solution. For other applications that cannot afford the FinFET solution, such as cost sensitive low-mid end mobile consumer applications, FD-SOI is a great

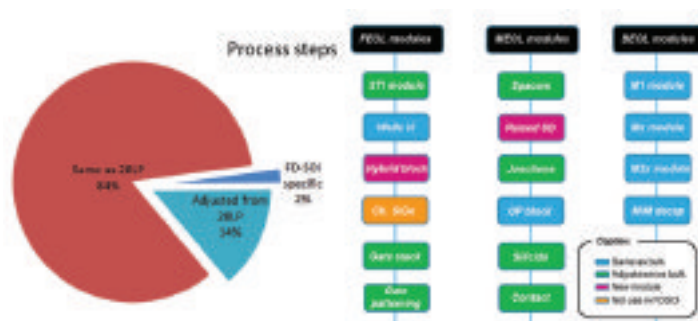


FIGURE 5. 28nm FD-SOI vs. 28LP process (courtesy of ST Microelectronics).

candidate for providing low power/high performance and more analog integration capabilities with the least process and design disruption for low cost and fast time to market. Furthermore, FD-SOI devices with back bias can operate at voltages as low as 0.35V [15,16] without area and costly design penalties making them excellent candidates for Ultra-Low Power (ULP) applications. FD-SOI devices consume less energy than bulk at the MEP (Minimum Energy Point) and maintain the smallest energy per cycle with higher operating frequency across the whole Vdd range [17, 18]. This makes UTBB FD-SOI

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technology a very attractive option for enabling ULP cost sensitive IoT applications.

Smart Cut™ enabling Å uniformity for Vt variability control

Optimization of the conventional Smart Cut process is essential for delivering ultra-thin SOI and BOX with well controlled wafer-to-wafer and within-wafer uniformity (**FIGURE 6**). The Smart Cut unique uniformity control relies on several key aspects of the process [19]: (a) A highly uniform thermal oxidation of a donor wafer to form the BOX (b) A conformal hydrogen implant through the oxide to define the separation plane in the Silicon (c) A high temperature anneal to eliminate the SOI roughness while keeping excellent on-wafer SOI uniformity (20).

Developing an efficient smoothing process to eliminate the Si roughness is critical for ensuring low transistor Vt variability. This requires Si thickness monitoring across the entire range of the spatial frequency. As existing ellipsometry and AFM characterizations are necessary but not sufficient, Soitec developed Differential Reflective Microscopy (DRM) to address the 100um scale SOI roughness. Consequently, bridging the gap between ellipsometry and AFM and providing a complete picture of surface roughness crucial for controlling Vt variations at the transistors level (**FIGURE 7**).

As the FD-SOI substrate plays a key role in defining the device structure, substrate local and global thickness

control is very important. This is especially true for UTBB FD-SOI devices, where the BOX thickness affects the efficiency of Vt tuning through back biasing, and the channel thickness uniformity and roughness influence the electrostatics of the device and Vt variation respectively. Today, Soitec guarantees volume production of SOI $12\text{nm} \pm 5\text{\AA}$ and BOX $25\text{nm} \pm 10\text{\AA}$ (6 sigma value, all sites, all wafers). When benchmarking variability; planar FD-SOI exhibits the best performance compared to Bulk technologies [4, 5]. Global variability is also reduced and maximum TS_i dispersion ($\sigma_{\text{TSi,max}}$) obtained on 300mm wafers

is already satisfying the objective for Vt variability for advanced technology nodes [4].

High resistivity SOI substrates

The rapid adoption of new wireless standards and the increasing demand for data bandwidth requires RF IC designers to develop devices

with higher levels of integration, meeting more and more stringent specification levels. The engineered substrates on which those devices are manufactured play a major role in achieving that level of performance. The improved high frequency performance of CMOS with process shrinks, and the availability of CMOS foundry technologies on 200 or 300mm substrates has made it possible



FIGURE 6. The Smart Cut process.

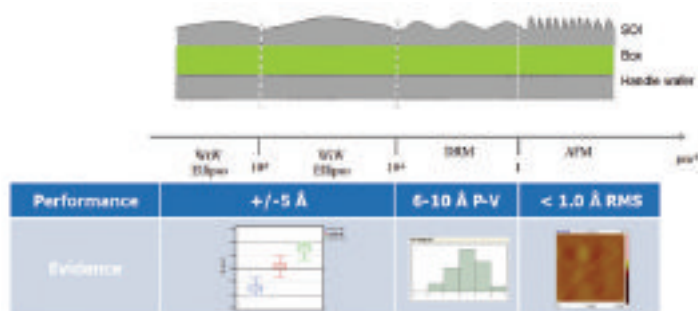


FIGURE 7. SOI layer thickness control.

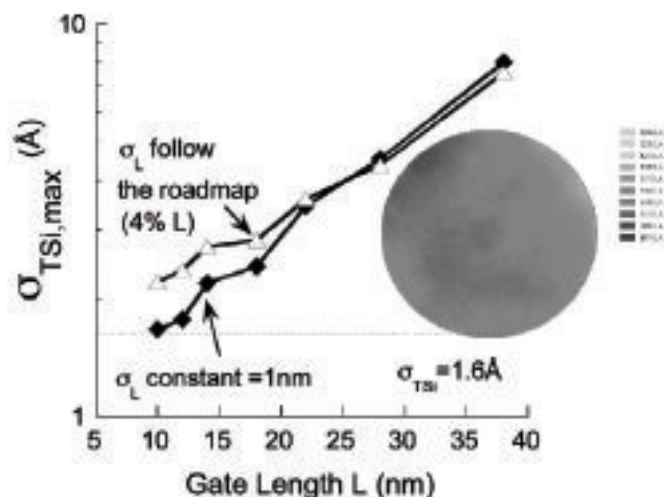


FIGURE 8. Silicon uniformity requirements to meet ITRS variability roadmap [4].

to have high volume fabrication of integrated Si based RF systems, including high quality passive devices [21,22] and RF switches and power amplifiers on SOI substrates [23]. Historically, switches and power amplifiers were built on gallium arsenide (GaAs) substrates. Since 2008, RF-SOI has progressively displaced GaAs and silicon-on-sapphire technologies by offering the best cost, area and performance for RF switches, and thus becoming the mainstream technology solution adopted by the majority of RF foundries [24].

Gen 2 HR-SOI engineered substrates

Typical SOI substrates do not have thick enough BOX to prevent the electrical field from diffusing into the substrate, inducing high-frequency signal losses, non-linearity and crosstalk which are detrimental to RF performance. To improve the insertion loss, harmonic distortion and isolation performance required for switches, the bulk base substrate of an SOI substrate was replaced by a high-resistivity base substrate known as Gen 1 HR-SOI. The adoption of Gen 1 HR-SOI wafers for RF applications has allowed monolithic integration of RF FEM, leading to smaller

size, better reliability, improved performance and lower system cost [25, 26]. While first generation substrates are well suited for 2G and 3G applications, they suffer from the a parasitic surface conduction (PSC) layer induced under the BOX due to fixed oxide charges which attract free carriers near the Si/SiO₂ interface. This drastically reduces the substrate effective resistivity by more than one order of magnitude, limiting the substrate capability in meeting the next step in performance for LTE advanced standards (**FIGURE 9**).

To address this intrinsic limitation, Soitec and Université Catholique de Louvain (UCL) developed a second generation (Gen 2) HR-SOI substrate with improved effective resistivity as high as 10KOhm.cm (**FIGURE 10**). This was achieved by adding a trap-rich layer underneath the buried oxide to freeze the PSC. These traps originate from the grain boundaries of a thin polysilicon layer added between the BOX and high resistivity substrate [27]. The high resistivity characteristics of Gen 2 HR-SOI substrates are conserved after CMOS processing, enabling very low RF insertion loss (< 0.15 dB/mm at 1 GHz), low harmonic

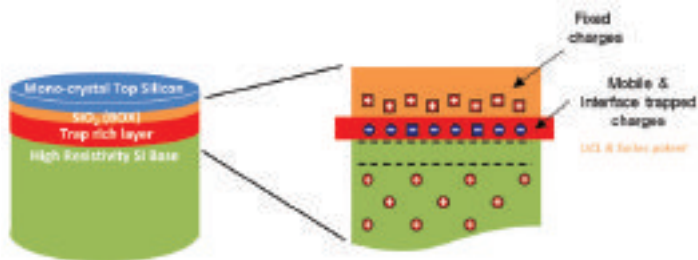


FIGURE 9. Gen 2 HR-SOI Substrate.

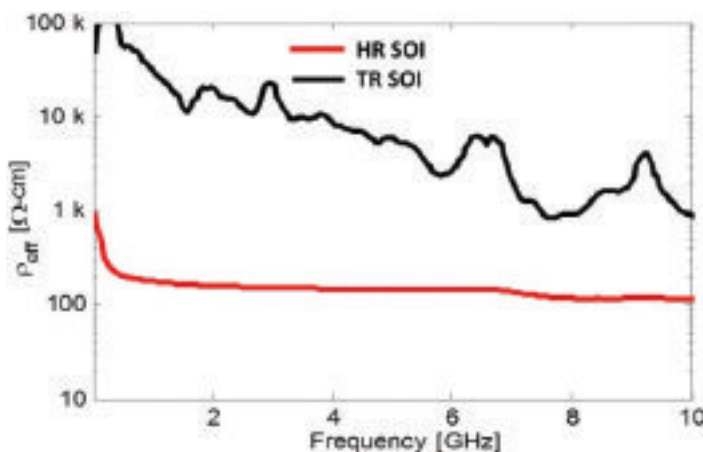


FIGURE 10. Measured effective resistivity of Gen 1 HR-SOI and trap-rich Gen 2 HR-SOI (TRSOI). Both use 10 kOhm.cm nominal resistivity handle Si substrate [25].



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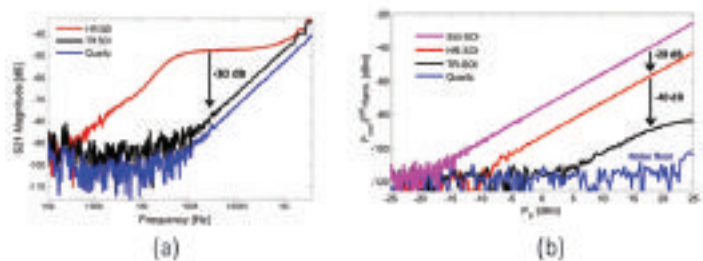


FIGURE 11. (a) Measured crosstalk comparing Gen 2 HR-SOI (TR SOI), Gen 1 HR-SOI and quartz [25]. (b) Measured harmonic distortion along a CPW line, on standard SOI (~ 10ohm.cm) and Gen 1 HR-SOI (~ 1 kOhm.cm) and Gen 2 HR-SOI (TR-SOI) (~ 10 kOhm.cm).

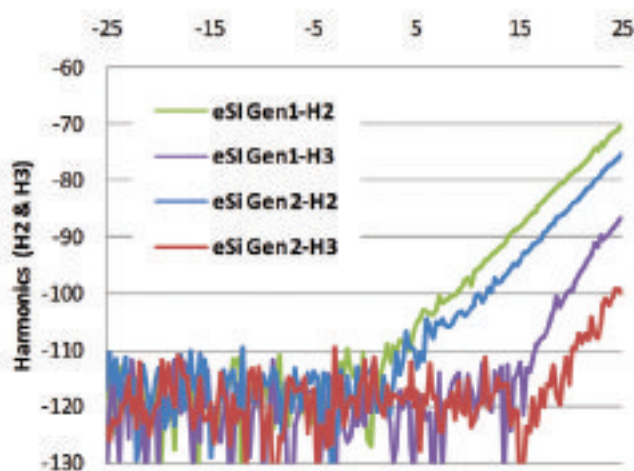


FIGURE 12. Harmonic two and three measured on CPW on commercially available versions of Gen 2 HR-SOI (eSi) substrates.



FIGURE 13. Gen 2 HR-SOI (eSi) substrates, advantages vs Gen 1 HR-SOI substrate.

distortion (-40dB) along coplanar waveguide (CPW) transmission lines, and purely capacitive crosstalk close to quartz substrates (**FIGURE 11**). It was further demonstrated that the presence of a trapping layer does not alter the DC or RF behavior of SOI MOS transistors [28]. With second generation HR-SOI products, RF IC performance is further advanced meeting more stringent losses, coupling and non-linearity specifications (**FIGURE 12**) [25].

TABLE 1. Performance / Cost elements for substrate driven advantages.

Segment	Performance contribution	Cost Benefits
Photonics	SOI and double SOI layers to guide light	Silicon integration and 300mm processing
FinFET	High mobility layers integration onto silicon, low TDD	Decoupling material epitaxy and device optimization.
Image sensor	Antireflective layers integrated in SOI stack to be front after BSI process	Simplification of BSI processing

Because the trap-rich layer in Gen 2 HR-SOI substrates is integrated at the substrate level, additional process steps and consequently more conservative design rules are no longer needed, leading to a more cost effective process and a possible smaller die area per function. Gen 2 HR-SOI substrates now enable RF designers to add diverse on-chip functions such as switches, power amplifiers and antenna tuners with excellent RF isolation, good insertion loss and better signal integrity at lower cost than traditional technologies (**FIGURE 13**). It also brings clear benefits for the integration of passive elements, such as high quality factor spiral inductors [29], tunable MEMS capacitors [30], as well as reducing the substrate noise between devices integrated on the same chip. Beyond performance, RF-SOI offers a unique advantage to further reduce board area by integrating all FEM devices on the same die [3].

In addition to innovation at the substrate level, Soitec developed the characterization needed to predict the RF Harmonic Quality Factor (HQF) at the substrate level and before device/circuit manufacturing. The characterization method is based on spreading resistance profiling (SRP), which can predict the 2nd harmonic distortion (HD2) performance of a coplanar waveguide (**FIGURE 14**). This essential metrology step is used today throughout the Soitec product line to ensure Gen 2 HR-SOI SOI substrates provide the expected RF performance at the device level.

New substrates for new collaborations

As demonstrated, UTBB FDSOI and Gen 2 HR-SOI substrates are well positioned to address ULP IoT and mobile connectivity applications that will respectively require drastic power reduction and higher frequency bands at very low cost. Combining advanced CMOS

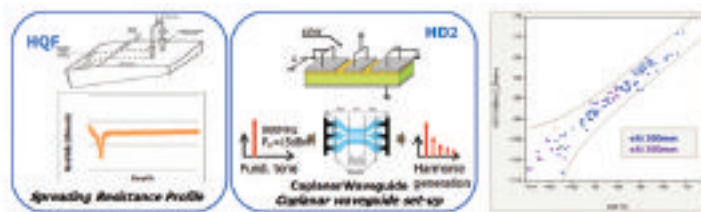


FIGURE 14. Harmonic Quality Factor (HQF) methodology.

process capabilities with the demonstrated benefit of engineered SOI substrates is paving the way for digital and RF integration for next generation cost sensitive integrated ULP mobile connected devices.

Furthermore, there are multiple examples where innovative substrate engineering can address roadmap challenges, enable further integration; provide differentiation in final product at a more efficient cost and footprint. Some examples of different application segments include: Photonics, Imaging sensors, advanced FinFET (**TABLE 1**).

Looking beyond a wafer and an application, entering the substrate era requires critical partnerships across the entire ecosystem. This includes having an augmented collaboration along the value and supply chain, covering collaborations with material, equipment and substrate suppliers as well as collaborations with foundries, IDMs and fabless companies. Soitec greatly supports this model and believes in establishing strong collaborations to seed future critical innovations.

Conclusion

Engineered SOI substrates are now a mainstream option for the semiconductor industry adopted by several foundries. UTBB FD-SOI substrates enable planar fully depleted devices with full back bias capability to extend Moore's Law at 28nm and beyond providing excellent power/performance/cost benefits. Gen 2 HR-SOI substrates enable FEM integration and higher linearity and isolation meeting stringent performance requirements for advanced standards at an improved cost. Combining advanced CMOS process capabilities with the demonstrated benefit of engineered SOI substrates is paving the way for digital and RF integration for next generation cost sensitive integrated ULP mobile connected devices. As such, engineered SOI substrates are well positioned to serve future integrated IoT applications.

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Fit-LINE, Inc.'s Three Key Factors to Create Leak-Free Fitting Assemblies for Fluid Processing Applications

Can operational efficiency, a critical factor in the fluid processing industry, be achieved by focusing on the synergy of fitting components and assembly technology? Creating quality fittings and innovative assembly tools for the most demanding applications is part of Fit-LINE, Inc.'s mission. With extensive high-purity fluoropolymer expertise and in-depth research, testing and evaluation, Fit-LINE has isolated three critical variables to ensure leak-free fitting assemblies.

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Variable #3 – Nut Tightening Methods

The final variable isolated by Fit-LINE in the pursuit of leak-free fitting assemblies is the method used to tighten assemblies to the required torque value. Hand tightening, a commonly-used practice, will not produce a consistent and accurate flared assembly seal. While the use of a torque wrench and nut adapter can provide more consistency, this combination is more complicated. Furthermore, overtightening the nut will affect the yield strength of the materials, which may result in leaks.

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Controlling Measurements of WLP in High Mix, High Volume Manufacturing

JIN YOU ZAO, STATS ChipPAC, Singapore, and **JOHN THORNELL**, Rudolph Technologies, Inc. Bloomington, MN, USA

The demand for 4-mask layer Cu-plated wafer-level chip scale packaging (WLCSP) is increasing rapidly, and the current capability for in-line Cu height measurements is not suitable for high volume manufacturing (HVM).

Thus, metrology constrains production capacity and limits volume ramp. Furthermore, the bottleneck created by a backlog of Cu step height measurements risks the timely detection of process drift and control. For a 4-mask layer Cu-plated WLCSP, accurate Cu step height measurement is required for both the Redistribution Layer (RDL) and Under Bump Metal (UBM) to ensure consistent delivery of good electrical performance and package reliability. This is especially important as WLCSP is moving towards finer feature size and pitch to meet increasing demand for smaller form factor.

In this article, the current measurement methodology is reviewed and an alternative measurement solution is derived. Full automation capability is delivered, yet the solution is reliable and versatile enough for high-mix production volumes. For quick-turn and high-mix volume manufacturing, accurate and fast in-line monitoring is crucial for timely process drift detection and control.

WLCSP in-line process measurement challenges

Contact-based profilometers are commonly used in wafer bumping for measurement of metal feature (RDL, UBM) thicknesses due to their ease of use and their low cost of ownership. However, the method of measurement is largely semi-automatic, and the identification of exact features and measurement locations is challenging.

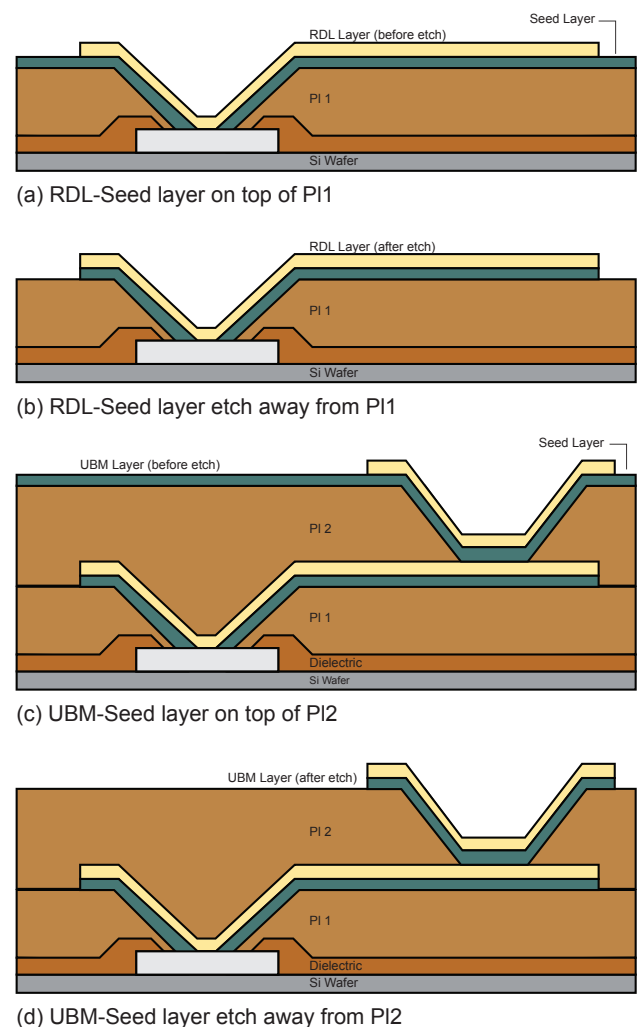


FIGURE 1. Wafer Bumping feature measurement configurations.

This becomes more acute in a high product-mix HVM environment, where measurement needs to be highly adaptive to different features on different products. As such, contact-based profilometers are limited to sampling

measurements, and cannot perform 100% die inspection for process characterization.

It is thus desirable to have an automated feature measurement system capable of measuring features at precise locations on different topology on wafers in both sampling and full inspection modes.

Specifically, feature measurement for wafer bumping comprises the following configurations (**FIGURE 1**):

- Cu RDL feature height measurement after Cu electroplating, where the sputtered metal seed layer to enable Cu plating remains on the first layer polyimide surface
- Final Cu RDL feature thickness measurement on first layer polyimide surface (PI-1) after the Cu seed layer is etched away. Accurate final Cu RDL thickness measurement would require a good gauging of the PI-1 thickness underneath, especially if the topology is not flat.
- Cu UBM feature height measurement after Cu electroplating
- Final Cu UBM feature thickness measurement on second layer polyimide surface (PI-2)

The development for automated feature measurement proceeded in two phases: (Phase-1) Cu step height highlight measurement on reflective metal surfaces, and (Phase-2) Cu thickness and polyimide thickness measurement on non-reflective surfaces.

Phase-1: Auto Cu height measurement

In this phase, the 3D inspection (3DI) system commonly used for solder bump height (typically greater than 20 μ m) measurement is explored for auto Cu feature height measurement. Typical 3DI system such as Rudolph's WaferScanner, is equipped with the 3D triangulation laser sensor (**FIGURE 2**). Laser triangulation, where a laser is directed at the wafer surface at an angle of 45° and focused to a spot size of 8 μ m, provides fast, precise measurements of bump height and coplanarity. Through a combination of laser-scanning and wafer movement, the beam scans the entire wafer

surface. A lens collects the reflected/scattered laser light and focuses it on a position sensitive detector.

To enable Cu feature height measurement (typically in the range of 2- 20 μ m), the Triangular laser sensor was redesigned with a spot size of 5 μ m, providing accuracy down to $\pm 0.2 \mu$ m. The laser scanning algorithm was also improved from an array to a stagger method to improve the repeatability of scanning signals. As Cu feature height measurement is influenced by the surrounding topology, the ability to select any datum for measurement is critical. This was achieved through the integration of camera-based 2D inspection to the improved triangular laser sensor system using the developed datum selection

program. An automated height measurement report can be conveniently generated for further analysis through the program (**FIGURE 3**).

To verify the consistency of measurement performance, both the improved 3D triangulation laser sensor system and contact profilometer were used to

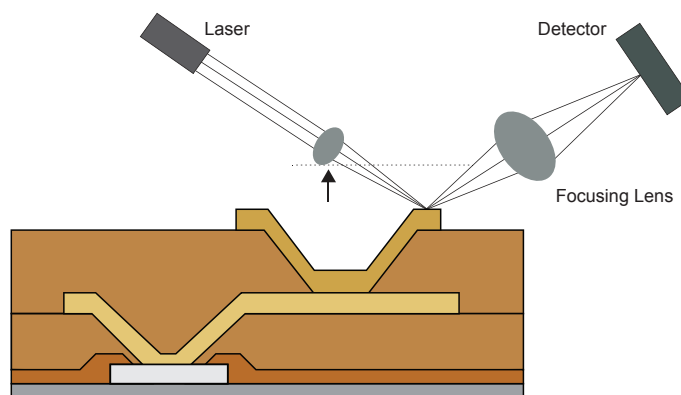


FIGURE 2. 3D triangular laser sensor working illustration.

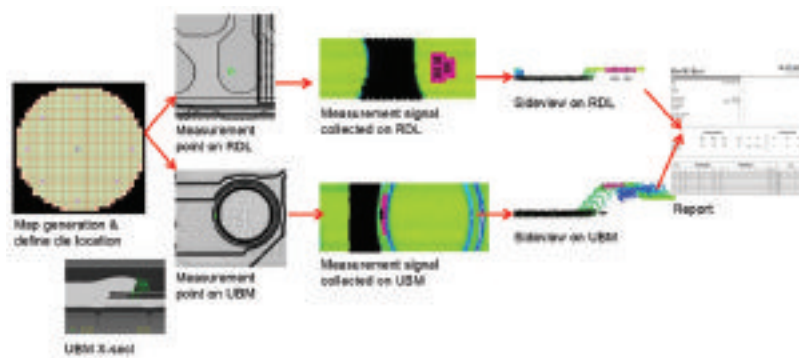


FIGURE 3. Selectable datum for Cu feature height measurement through camera-sensor integration.

measure feature Cu height on correlation device wafers. It confirmed that the automated 3D triangulation laser sensor system registers statistically similar Cu feature height mean compared to the manual contact profilometer, but required only one-fifth of the measurement time taken by the profilometer. Wafer bumping facilities which already have an existing pool of 3DI inspection tools can be modified to extend measurement application

to Cu feature height without the need for excessive new investment.

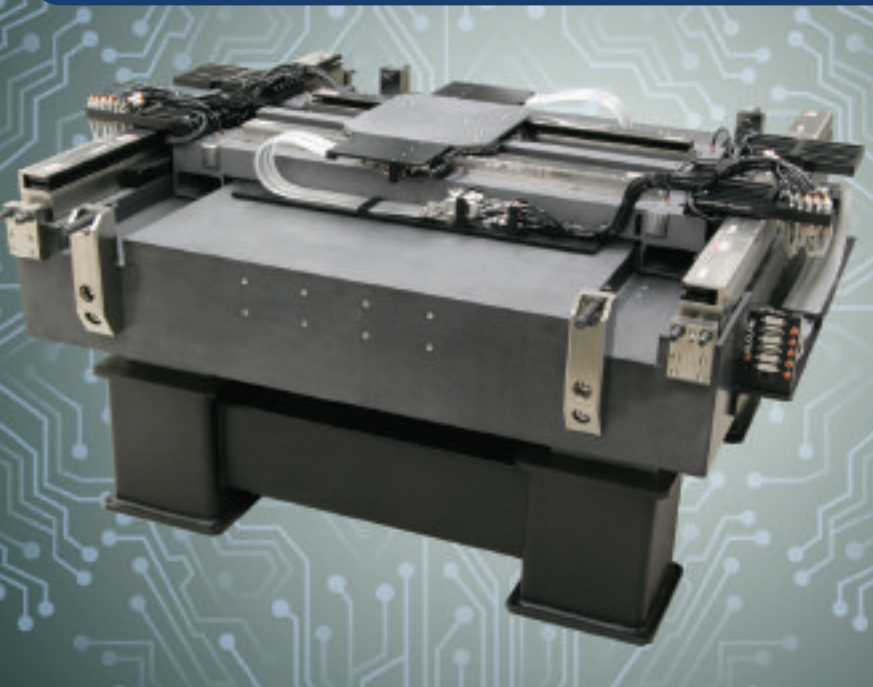
Phase-2: Auto Cu/ PI thickness measurement

While a strong signal can be derived using the 3D triangular laser signal for Cu feature height measurement after electroplating (Fig. 1, a and c), it is more difficult to establish a stable signal for Cu feature height measurement after the reflective metal seed layer is etched away, and a reference datum needs to be established on the remaining transparent polyimide surface (Fig. 1, b and c). Several conventional methods exist for non-contact measurement of step heights, such as various confocal sensors, triangulation sensors, and scanning white light interferometry. These sensors typically have difficulty differentiating between reflections from the top and bottom surfaces of a layer, that is, layer thickness. This limitation comes from the depth of focus of the objective, which in turn depends on its numerical aperture (NA). Thus, for all these techniques, sensor performance is highly dependent on objective lens.

To overcome this technical constraint, it was necessary to develop a metrology system that can measure concurrently the transparent layer thickness as well as the metal feature step height above the surface of the transparent layer. This can be achieved through the integration of reflectometry and visible light interferometry principles [3]. In this method, the direct reflection from the transparent layer provides direct thickness measurement of the transparent material, while the interferometry captures topography (distance from the sensor), allowing the system to measure the thickness of the opaque metals by scanning over the edge of the feature. This technique is called the visible thickness and shape sensor (VT-SS) system.

In the following sections we provide further description of how the VT-SS system can be adapted for feature height/thickness measurement on varying topology and opaque materials. For this work, we used the Rudolph Technologies NSX® System configured with the VT-SS sensor.

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VT-SS system MSA study

Measurement system analysis (MSA) seeks to qualify a measurement system for use by quantifying its accuracy, precision and stability. VLSI standard wafers with 8 μ m, 24 μ m, and 48 μ m step heights were used to assess gauge repeatability and reproducibility (GR&R) and accuracy of the VT-SS system, as well as system correlation on two different NSX Systems (tool matching) that were retrofitted with the VT-SS system.

A. Gauge repeatability and reproducibility

For the GR&R study, a total of ten parts on VLSI wafers (4 parts from 8 μ m, 3 parts from 24 μ m and 48 μ m respectively) were measured three times each, including wafer loading and unloading.

FIGURE 4 shows gauge R&R for VT-SS is 1.35% of tolerance and fully meeting AIAG standard of <10%.

B. Accuracy

Step height measurement accuracy was evaluated by means of bias and linearity analysis using the VLSI step height wafers. For this study, one location on each standard wafer was measured ten times and compared to the VLSI specification for the wafer.

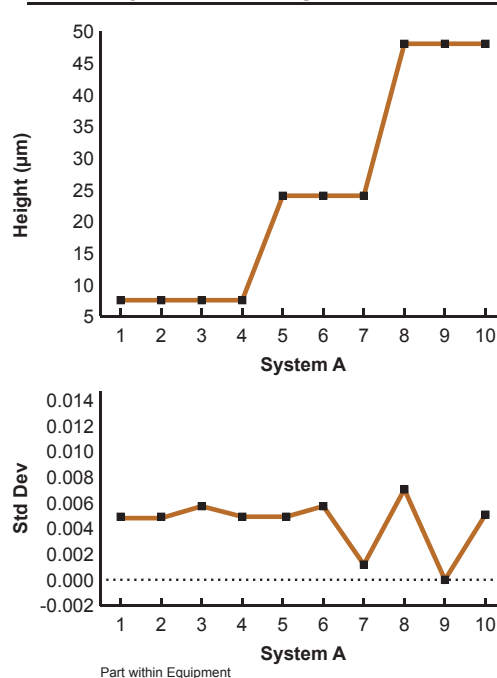
Based on the studies in **FIGURE 5**, measurement with VT-SS system shows an average bias of 0.95%, and linearity error of 0.0059%, meeting the AIAG standard of <5%.

C. Correlation of Multiple Systems

Having established VT-SS capability, the next evaluation is system correlation on multiple tools of the same configuration. The same VLSI wafers described above were measured on a second system with the same hardware and software configuration.

A summary of results are shown in **TABLE 1**, and a detailed example of the 24 μ m step height is shown in **FIGURE 6**. For each wafer, the two systems produce similar results, with an offset that ranges from approximately 10nm to 30nm. Considering that the measurement

Variability Chart for Height (μ m)



Gauge R&R

Measurement Source	Variation (5.15 StdDev)	% of Tolerance
Repeatability (EV)	0.027061	1.35
Reproducibility (AV)	0.000000	0.00
Equipment	0.000000	0.00
Equipment*Part	0.000000	0.00
Gauge R&R (RR)	0.027061	1.35
Part Variation (PV)	91.964971	4598.2
Total Variation (TV)	91.964975	4598.2

FIGURE 4. Measurement repeatability and reproducibility on ten different parts on VLSI wafers. The first four are from the 8 μ m step height wafer, #5-#7 are from the 24 μ m step height wafer, and #8-#10 are from the 48 μ m step height wafer.

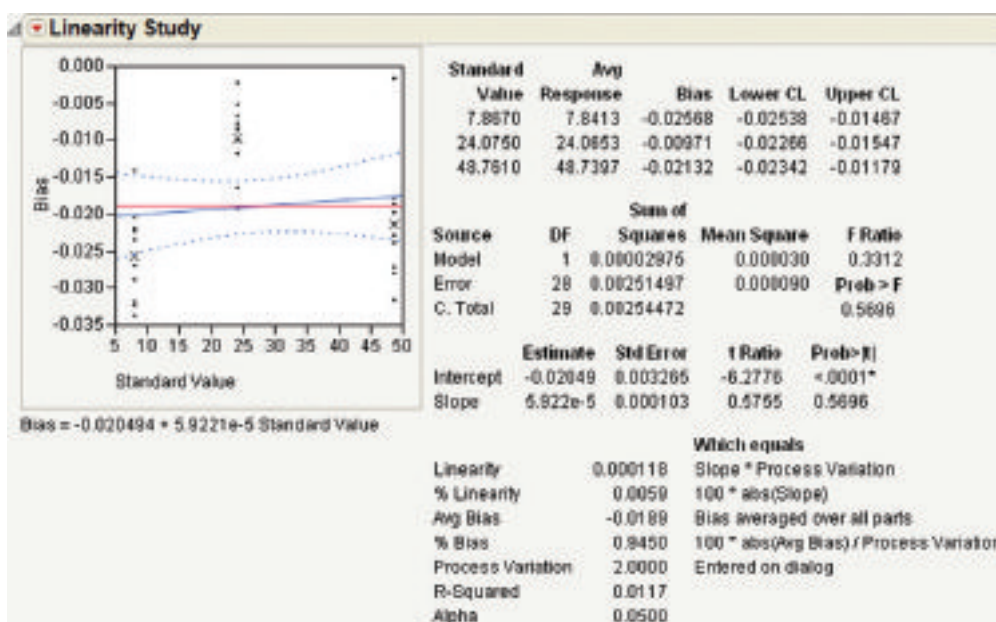


FIGURE 5. Accuracy study on VT-SS with VLSI standard.

uncertainty is on the order of 5nm (1- σ), the small system offset is within expectations.

VT-SS system application assessment

VT-SS system allows capturing of both the transparent polyimide thickness and opaque Cu feature height with a single scan from polyimide layer to Cu feature. From the part of the scan covering the polyimide, signals representing the direct measure of the polyimide thickness, the distance to the first surface of the polyimide, and the distance to a metal surface under the passivation stack are measured. The direct measure of the polyimide thickness is the measurement a standard spectroscopic reflectometer would produce. In that part of the scan where the sensor spot illuminates the Cu step height, the direct thickness peak and one of the distance peaks disappear. Only a distance peak to the surface of the Cu feature is present since the copper is opaque. The Cu step height above the first polyimide layer is then determined from the appropriate distance measures from each part of the scan. Thus, all the desired thickness and Cu thickness measurements are reported.

To aid interpretation of measured signal peaks, a visualization program was developed for automated generation of feature thickness. **FIGURE 7** shows an illustration of the program interface for visualization of measured thickness. Raw data can also be exported for further analysis.

A. VT-SS Cu RDL Layer thickness measurement

To assess VT-SS system's measurement performance on an

	Nominal	System A			System B		
		Average	Avg Error	Max Stdev	Average	Avg Error	Max Stdev
VLSI 8 μ m	7.867	7.826	-0.041	0.007	7.835	-0.032	0.006
VLSI 24 μ m	24.075	24.077	0.002	0.009	24.104	0.029	0.009
VLSI 48 μ m	48.761	48.746	-0.015	0.010	48.715	-0.046	0.006

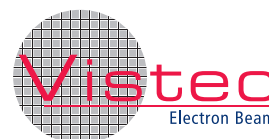
TABLE 1. Comparison of Measurements from Two Systems



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actual device feature, it was used to measure the Cu feature RDL thickness layer above the first polyimide (PI) layer (refer to Fig. 1, for a pictorial illustration) on a correlation device wafer. The measured RDL thickness was then cross verified with the actual measured Cu feature step height from a contact profilometer and WaferScanner

B. VT-SS Polyimide cum RDL layer Thickness

Further evaluation of the VT-SS system accuracy was achieved through comparison with cross sectional scanning electron microscopy (X-SEM) measurements. X-SEM allows evaluation of both RDL step height and PI thickness (Fig. 1, b). As discussed above the measurement sensor has the unique capability to simultaneously measure step height, i.e. a distance measurement, and film thickness. Both types of measurements must be independently evaluated for accuracy.

Conclusion

We have reported the development of VT-SS-based system on a fully automated platform for in-line process measurement of wafer bumping processes. This new metrology integrates both reflectometry and visible light interferometry principles. Based on MSA studies, VT-SS on a fully automated platform is a precise, accurate and fast metrology system. Engineering validations have shown VT-SS is highly capable in measuring critical dimensions such as RDL/UBM metal thickness, transparent polyimide/passivation thickness, and feature sizes in one single step. It relieves the current constraints imposed by existing measurement tools on in-line process control, especially in a high mix, high volume production environment. This allows WLCSP production to move to new milestones of quality, yield, cycle time and productivity.

Acknowledgment

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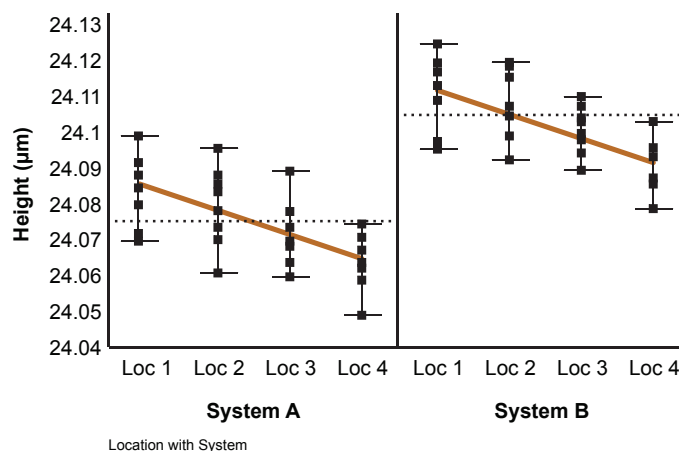


FIGURE 6. Comparison of 24µm step height measurements from two different systems at the same four wafer locations. The measurement offset between the two systems is on the same order of magnitude as the measurement repeatability.

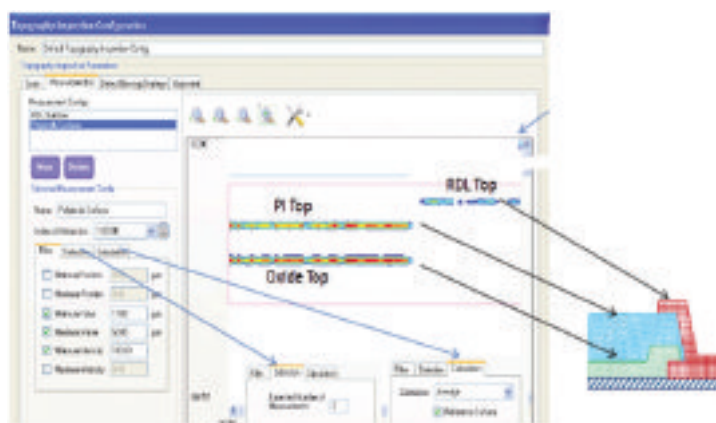


FIGURE 7. Program interface for measured thickness visualization.

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Is it time to switch to OASIS.MASK?

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A summary of OASIS standard advantages and weaknesses is presented, based on six years of experience with customer databases.

Six years ago, when OASIS was introduced, we highlighted why it was a positive replacement for GDSII [2]. Since then, users have started adopting OASIS in their flows, with benefits and disadvantages. One of OASIS strengths is its flexibility (unlimited coordinate precision, unlimited number of layers, etc.). But this flexibility has a price in terms of memory consumption and computing time.

A new standard, OASIS.MASK, is being introduced to address the requirements specific to photomask layout representation. This subset of OASIS (and as such fully OASIS compliant) introduces constraints that reflect the real-world limitations of mask manufacturing. As a result, OASIS.MASK interpretation and exploitation is more efficient and reliable.

OASIS: A review

GDSII was created for magnetic tapes and sequential storage. To take advantage of modern disks, OASIS offered to give direct access to parts of the file. It also strived to reduce file size by avoiding repetitions (using the same principles as compression algorithms). Another goal of OASIS was to remove some limitations such as numerical precision.

How has it been used?

- 1) Reference tables: In OASIS, most references to an object can be made either by its name or by a reference number. Reference tables map names to numbers at a single place, drastically reducing file size when only reference numbers are used.

- 2) Strict mode: OASIS strict mode allows fast random access in an OASIS file by taking advantage of reference tables. However, strict mode is optional, and readers can choose to ignore it, leading to situations where a file can appear valid to one reader, and invalid to another.
- 3) C-Blocks: OASIS CBLOCK records provide a way to embed compressed data within an OASIS file. Contrary to using an external tool on the whole file, they allow both compression and efficient access.

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- 4) Checksum: OASIS allows three different validation schemes: no validation, a CRC checksum or a byte sum. The CRC checksum (a 32 bits polynomial Cyclic Redundancy Check) is the only validation scheme that really detects errors, but at the cost of being byte-order dependent: The file must be written and read sequentially. Unfortunately, it seems that many tools turn off validation by default.

Advantages and weakness

- 1) Unlimited precision: OASIS defines a format for integers that support unlimited precision. In practice, many implementations choose to use the computer's native precision (usually 64 bits).
- 2) Choosing a description methodology: OASIS gives users a lot of choice, but never imposes or recommends any of the different options. In our experience, the following "rules" have proven to be the most reliable:
 - Use strict mode and make all references by number
 - Use CBlocks rather than compressing the whole file.
 - Use CRC checksum.
 - Never write numbers that cannot be represented as 64 bits integers.
 - Use type 6 or 7 for floating point numbers (IEEE 754 format).
 - When in doubt, use type 8 repetitions (for arrays), or type
 - 10 (for random repetitions): these are the most generic.
 - Use rotations which are multiples of 90 degrees. A rotation of 12.34 degree does not make much sense in a real mask!

OASIS.MASK: The missing link

OASIS has been a big step forward for the physical

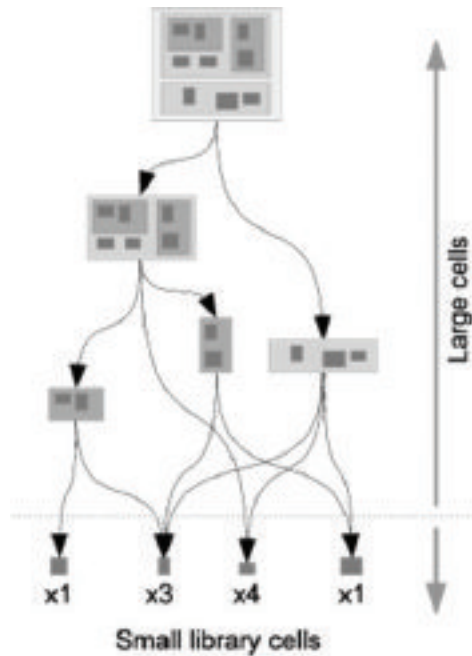


FIGURE 1. Functional hierarchical description of a chip.

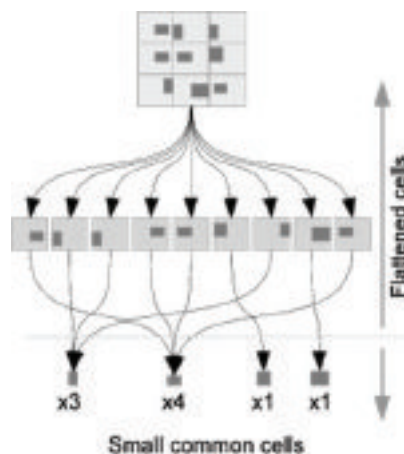


FIGURE 2. Topological hierarchical description of a chip.

design description. But photomask descriptions are still using older proprietary formats like MEBES, JEOL, VSB, MIC, HL, DXF or Gerber. There is a need for a new standard for mask layout description, and since it is not so far from design layout, the idea to reuse parts of OASIS emerged: SEMI P44, also known as OASIS. MASK was born [4].

OASIS.MASK is not really a new format. It is a formal subset of OASIS, adding some constraints and providing several extensions for mask data preparation tools. As a result, an OASIS.MASK file can be read by any standard OASIS parser.

While a design database is a hierarchical description based on the functions used in a chip, an OASIS.MASK file is a description of the layout based on the topology. It still keeps a hierarchy, but limits it to 3 levels. The first level is the top cell, the second level is made of so called localization areas and the third and last level is made of small cells named common cells. Localization areas are just rectangular areas at a given place of the full layout. OASIS.MASK may then be seen as a flattened view of the chip

just divided in windows.

This is more or less what is done in a MEBES file which is a fully flat description and is thus very big, sometimes exceeding a terabyte. In all large chips, there is an intensive usage of library cells. All basic gates or memory points are called millions of times but only need to be described once. This has been taken into account in OASIS.MASK in which only the upper level cells of the functional hierarchy need to be flattened. All "small" cells may remain unchanged and are called from the intermediate level of the hierarchy. These small cells are called common cells.

FIGURE 1 represents the functional hierarchy of a chip in OASIS format. **FIGURE 2** represents the same chip with the topological hierarchy in OASIS.MASK format. We can see that all small (common) repeated cells are described the same number of times in both representations, while large cells have been flattened.

- Names cannot be longer than 256 bytes
- Coordinate values for PLACEMENT records are limited to 32 bits signed integers
- Only repetitions 0-3 (regular 2D arrays) are allowed
- Magnification, mirroring or rotation are disabled
- There can only be one layer per file
- Layer numbers are limited to 256, and datatypes are ignored.
- Only rectangles and trapezoids are allowed
- The bounding box for all cells must be described
- A cell cannot be larger than 1 square millimeter (except Top Cell)
- The file offset of all cells must be provided

As stated in the OASIS.MASK specification, these constraints may evolve. For example we wouldn't be surprised to see 32 bit integers get promoted to 64 bits in the years to come.

OASIS.MASK extensions are implemented as plain OASIS properties, and remain compatible with the regular OASIS format. The major improvement of OASIS.MASK over OASIS is the introduction of localization areas, implemented with the P44_LOCALIZATION and P44_LOCALIZATION_AREA properties.

Being a subset of OASIS, OASIS.MASK introduces some restrictions on the original format. Most of them are to be expected (see 2.3.2), but some are more surprising:

- Cell names and properties can only include ASCII letters, numbers and underscore.
- File names cannot be more than 64 bytes long (256 including directory)
- Hierarchy is limited to 3 levels
- Strict mode is mandatory, all references are made by numbers (32 bits integers).

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- Validation checksum is mandatory (sadly, byte sum is allowed, although ineffective)

The P44_COMMON_CELL property is used to declare common cells. The P44_GEOMETRY_OFFSET_AVAILABLE and P44_GEOMETRY_OFFSET properties allow fast access to the geometry records of every cell. The P44_TOP_CELL_NUMBER property declares the reference number of the top cell. Since the P44_LOCALIZATION property also contains the top cell record offset in the file, finding the top cell in an OASIS.MASK is and very fast, contrary to a generic OASIS file. Most of the OASIS.MASK properties are mandatory. They drastically speed up file access and topological extraction of mask areas.

Applications

In most design flows, a final Design Rule Check (DRC) and Layout vs. Schematic Check (LVS) are run on databases before mask making. This mandatory step is considered as fully reliable. But, unfortunately, some configurations are subject to interpretation. A typical example is a path with a segment smaller than the width (**FIGURE 3**).

In such cases, a database certified as correct by a DRC could lead to an error on the silicon because the mask data preparation tool and the layout tool may have different interpretations. It is thus of utmost importance to perform the verification at the last possible step in the flow and on a format without any ambiguity, such as OASIS.MASK. And since any tool able to read OASIS files is able to read an OASIS.MASK database, a DRC could theoretically be executed directly on an OASIS.MASK file.

But at the current state of the OASIS.MASK specification, several problems remain. The first one is related to layers, because an OASIS.MASK file cannot contain more than one layer. To perform a full DRC, we must load multiple OASIS.MASK files at the same time, each of them containing a single layer.

Additionally, data type usage is not clear: they are widely used in OASIS files, but are ignored in OASIS.MASK. Datatypes might still be present in the file, but

cannot be relied upon since they will be ignored by some tools. All these limitations imply that we cannot use the same DRC deck to verify the design database and its converted version in OASIS.MASK format.

The second issue is related to the hierarchy. As previously mentioned, a design database has most of the time a functional hierarchy. This hierarchy should follow the schematic hierarchy and the LVS is performed hierarchically. Each cell in the schematic should match a cell in the layout, and the interconnections between them should match the connections drawn at a higher level of the hierarchy. Working on the hierarchy speeds up the process, and makes it easier to identify and localize errors.

In an OASIS.MASK file, the functional hierarchy is replaced by a topological hierarchy, which makes it completely different from the schematic. Only “small” cells may remain.

This means that a hierarchical LVS will be able to identify all gates and library cells but all the interconnections at a higher level will be processed flat, leading to a dramatic increase in processing time.

Post layout

With advanced process nodes, layout requires some post processing to meet manufacturing constraints. The two major operations to be performed are “dummification” and OPC (Optical Proximity Correction). Dummification consists of inserting small geometries in empty areas of some layers in order to guarantee a homogeneous density across the whole chip.

In order to have a better distribution of parasitics introduced by all the dummy geometries, they are often placed in a non-orthogonal way as explained in [3]. A full chip may contain millions of dummy geometries and it is important to have them grouped together in arrays instead of having millions of individual instantiations.

One of the interesting features of OASIS was the possibility to describe non-orthogonal arrays of cells or geometries. This is known as type 8 repetition. But OASIS.MASK does not allow repetition of other types than 0-3, i.e. a regular orthogonal arrays. This has a



FIGURE 3. How should the upper right corner of the path be filled?

very negative impact on the output file size.

All geometries in an OASIS.MASK are split in basic trapezoids. This means that the fracturing step is mostly done, even if some work might still remain, like Boolean operations, clipping or sizing (bias adjustment). All these operations create trapezoids which remain compatible with OASIS.MASK (see, for example, **FIGURE 4**).

As stated in [1], OASIS.MASK is well suited for efficient reading. But to enable fast random access based on the topology (e.g., display the top left corner of the mask), OASIS.MASK files must use localization areas efficiently. For example, in **FIGURE 5**, only the localization area matrix will permit fast access.

When building the matrix, there is a tradeoff between access time and file size: small localization areas will allow for faster access, but will also increase file size. Also note that localization areas are not declared in a regular array and do not have to share common dimensions. For some files, it can thus be more efficient to build an “adaptive” matrix.

The evolution

The OASIS.MASK format offers the advantage of removing any risk of misinterpretation of the description thanks to the exclusive usage of trapezoids. Limiting OASIS.MASK files to one layer and ignoring datatypes prevents the DRC from running on a single file and producing 100% reliable checks. So, we

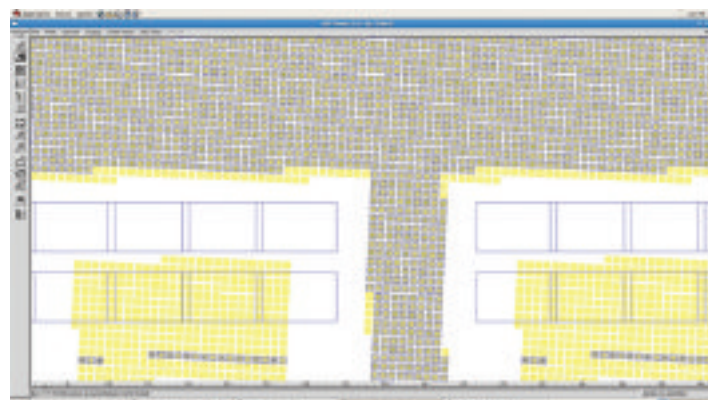


FIGURE 4. example of non-orthogonal dummies requiring type 8 repetitions.



FIGURE 5. Clipping a trapezoid with a rectangular area will always generate a convex polygon that can be fractured in never more than 3 trapezoids.

suggest to drop these constraints in future versions of OASIS.MASK. No change to the format is required as a different layer number may be specified for each trapezoid. Supporting several layers and datatypes should come at almost no implementation cost.

OASIS.MASK has restricted the types of repetitions to only standard orthogonal arrays. Neither type 8 repetitions for regular non orthogonal



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arrays, nor type 10 for random repetition can be used anymore. Usage of type 8 repetitions really improves dummy cells instantiation, as described in III-B2. Suppression of type 10 repetitions (non-regular repetitions) increases file size and writer complexity, because searching for regular arrays in non-regular matrices to create type 1 repetitions is costly (**FIGURE 6**).

Transformations

OASIS.MASK does not allow any geometrical transformation: Rotations, symmetries and magnifications are forbidden. It is true that applying arbitrary magnification factors and doing non orthogonal rotations may lead to rounding issues, and thus to differences in the final results produced by different tools. So, it make sense to disallow such cases, especially if we consider that they almost never appear in chips layout.

But simple rotations of multiple of 90 degrees are also forbidden and this has a real impact on the file size. In practice, we will always find the 4 possible orientations for each library cell in a complex design. This means that we will have to individually describe each common cell with its 4 orientations.

Remember that one of the benefits of OASIS.MASK over MEBES was to be able to keep all the small cells of a design “as is” in a common record. So we lose 75% of this benefit by disallowing orthogonal rotation. If we also take into account the possibility to apply a horizontal or vertical mirror on the cells, we again multiply by 4 the number of common cells to be described.

Conclusion

During the last few years, we have seen all the benefits of the OASIS format, as well as some of its weaknesses. OASIS is a complex format that provides many options, and it seems like everybody uses it in a different, sometimes suboptimal, way.

Using a single format for layout description during the whole design flow would have a lot of benefits, since each conversion done without 100%



FIGURE 6. Different localization-area usage.

reliable checks is a potential risk.

But this single format should not bring more constraints than benefits. Using standard OASIS at the beginning of the flow is really valuable as the designer can deal with a functional hierarchy, but as soon as the functional design by itself is completed, and the project enters a pure physical design phase, it may be a good solution to switch to OASIS.MASK. This is a smooth conversion since this format is still compatible with current tools.

OASIS.MASK still has some shortcomings, and we have pointed out some of the limitations which today prevent integrating this format in some steps of the flow. But as its specification mentions, “part of restrictions on OASIS.MASK may be relaxed, and OASIS.MASK specification may be extended”.

So we are confident that this format will be able to evolve and become a standard used across the whole design and layout flow. Our industry has much to gain from it in terms of robustness and usability.

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More change for the chip industry

PAULA DOE, SEMI, San Jose, CA

As if scaling to 7nm geometries and going vertical with FinFETs, TSVs and other emerging technologies wasn't challenge enough, the emerging market for connected smart devices will bring more changes to the semiconductor sector. And then there's 3D printing looming in the wings.

Sometime between 2009 and 2010, there was a point of inflection, where the number of connected devices began outnumbering the planet's human population. And these aren't just laptops, mobile phones, and tablets – they also include sensors and everyday objects that were previously unconnected, says Tony Shakib, Cisco Systems VP IoE Vertical Solutions, who will talk about the impact of these changes on the chip industry at SEMICON West this summer in San Francisco. Connected “things” may reach 25 to 50 billion by the year 2020, he projects (**FIGURE 1**). These connections of people, process, data and things will create opportunities for new revenue streams, new options for competitive advantage, and new operating models to drive both efficiency and value, potentially driving

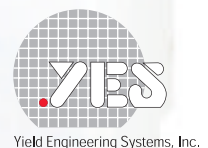
massive gains in efficiency, business growth, and quality of life, he suggests. “But as we connect the unconnected, this will require that we think differently about business strategy and IT, analytics, security, and more.”

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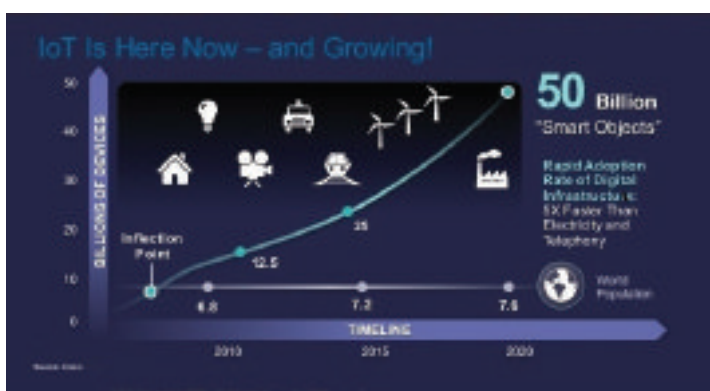


FIGURE 1. Connected “things” may reach 25 to 50 billion by the year 2020. Source: Cisco

PAULA DOE is a contributing editor for SEMI, San Jose, CA

Chip makers will need to provide easy-to-use IoT security for startups

One big change: some 50 percent of Internet of Things (IoT) solutions by 2017 will probably come from startups, according to Gartner's projections. "Whatever the exact percentage, the increased role of new and small players in the IoT edge devices will be a fundamental paradigm shift from the big companies that have conventionally dominated the electronics industry, says Gowri Chindalore, head of Technology and Business Strategy for Microcontrollers business group at Freescale, who will speak on the issue at SEMICON West's "Monetizing the IoT: Opportunities and Challenges" session. "And these startups' knowledge of security is often very low. So as IC makers we need to make it easy for them to do." He suggests the best solution is to offer on-chip security features, such as secure storage, cryptographic accelerators, and tamper resistance mechanisms, and supplement them with a software dashboard that makes it easy for the systems maker to set up and enable the desired features appropriate for the application. Though the encryption technology is very complex, by using library programs and selling in volume, the actual cost can probably be reduced to a few cents per chip.

Security for the internet will also improve markedly within several years as passwords are replaced by personal transmitters that automatically send secure codes to websites at log on. Similarly, local aggregator devices at the edge for all the IoT devices in the house or the factory will serve as the security gateway to screen users or devices by transmitted codes or biometric sensors. "We need proliferation of these security features into even all the benign IoT gadgets in the house to protect the network, but consumers will be willing to pay the small extra cost for security — especially after a few more highly publicized instances of hacking," he notes.

Designers combining more IP blocks face challenges in reliability and verification

The key challenge across the board from the design side for successful IoT devices will be

figuring out how to combine the right component capabilities of sensors and memory and processing and connectivity and size and power for a compelling application, and then making the right tradeoffs in the architecture to make it all work, explains Steve Carlson, VP marketing, Cadence Design Systems, another speaker at SEMICON West. "IP blocks will be especially useful for smaller companies to add functions without necessarily having the in house expertise," he notes. But combining the blocks will challenge many users by dramatically new issues of isolating noisy analog parts from the digital as they add RF and sensors that they haven't had to deal with before, and all at near-threshold and ultralow power. That will mean more issues with variation and reliability, and verification will increasingly need to include both hardware blocks and software together, so emulation will become more critical, he notes.

Fabs may need to deal with more diverse processes, but may improve productivity

"The IoT will drive demand for more IC manufacturing across a wide range of technologies, from the most advanced logic process to high voltage devices and MEMS, all with diverse requirements," says Peter Huang, VP Field Technical Support, TSMC North America, another speaker. He notes that MEMS and other emerging devices, ranging from micro-lenses for machine vision to batteries to power wireless sensors, will require some unique tools and processes, and will be less easily scalable than CMOS. Material handling and the need for isolated lines will create additional challenges. "Heterogeneous integration will require 2.5D packaging for both form factor and cost," he suggests. "And the real challenge will be high volume manufacturing and IP interface at the package level."

Though manufacturing equipment is already highly automated and interconnected, the availability of hundreds of low-cost, connected sensors may bring opportunities to increase tool automation and productivity, he adds (**FIGURE 2**).



FIGURE 2. Compact integration of multiple chip and sensor technologies for IoT devices will demand more sophisticated system- in-package technology. The new Apple Watch has 30 components in its core S1 SiP, all packed on to a 26mm x 28mm motherboard and overmolded with a conventional IC packaging resin compound. (Source: Chipworks)

Progress on technology for 3D printing of tooling and components

Then there's the disruptive potential for 3D printing some of the tooling and components all along the supply chain to speed time to market, allow more customization, reduce weight and simplify dealing with legacy parts — if the process can meet the required quality and cost. Phillip Trinidad, president of service provider Proto Café, who has worked with semiconductor sector players, argues that progress in optimizing designs now means additive manufacturing is increasingly becoming suitable not just for prototyping, but also for production of specialty

parts in performance plastics.

In addition, there's recent progress in 3D printing for challenging metal industrial parts, which will be addressed at SEMICON West "Factory of the Future: Disruptive Technologies from IoT to 3D Printing -- Impact on the Semiconductor Manufacturing Sector" session. Ryan Dehoff, lead for Metal Additive Manufacture at Oakridge National Laboratory, will provide an update on the current state of the art for printing in metal, while Wayne King, director of the Initiative for Accelerated Certification of Additive Manufactured Metals, will talk about the progress on speeding qualification of the additive metal parts by modeling and inline process monitoring and control.

Along with the regular coverage of next-generation scaling technology, SEMICON West 2015 will also address the impact of the Internet of Things and 3D printing on manufacturing technology across the semiconductor supply chain, as well as related developments in MEMS, emerging non-volatile memory technology, and automotive and biomedical applications. Please visit. www.semiconwest.org. ♦

ECAE improves sputtering target performance

STEPHANE FERRASSE, SUSAN STROTHERS and **CHRISTIE HAUSMAN**, Honeywell Electronic Materials, Sunnyvale, CA

Because it can achieve extreme deformation, Equal Channel Angular Extrusion (ECAE) can deliver submicron, high strength and uniform microstructures. The resulting improvements in strength allow for monolithic targets with a longer target life of 20-100%.

First observed in 1852, cathodic sputtering is a form of physical vapor deposition (PVD) that involves the bombardment of a target material by positive ions to physically remove atoms from the surface, forming a vapor for substrate coating. It wasn't until the 1960s and the growth of the electronics industry, however, that sputtering received significant attention.

Since then, sputtering has become entrenched in many integrated circuit (IC) production processes. While sputtering performance has benefited from advanced sputtering system designs and target material improvements, more is needed to meet future demands as device features shrink and thin film specifications become tighter.

The physical and chemical properties of sputtering targets play an integral role in thin film performance and device yield since they impact thin film composition, uniformity, consistency, defects (particulate), and step coverage. In addition, target utilization and lifetime is a factor in cost of ownership (CoO) as it correlates to chamber throughput and uptime.

This article explores how the microstructure of sputtering targets can be engineered to improve strength, life and thin film quality. It also compares conventional thermo-mechanical processing (TMP) to the breakthrough TMP of Equal Channel Angular

Extrusion (ECAE®) technology from Honeywell.

Key sputtering target properties

A great deal of research has been directed toward improving the microstructure of sputtering targets. Key target properties and challenges that impact thin film functionality and device yield include:

- **Chemical purity:** Elemental impurities in sputtering targets are undesirable as they transfer to the thin film and adversely impact performance. However, higher purity metals are weaker and less able to withstand the stresses induced in the sputtering chamber. This poses unique manufacturing and end-use challenges unlike most other uses of metallic products.
- **Metallurgical defects:** Thin film particulate contamination has been an ongoing and growing challenge with each successive technology node. Porosity, inclusions, inconsistent grain structures, and large second phases present in the target material can — through arcing — cause direct or indirect particulate contamination on the wafer.
- **Thermal stability:** High thermal stability in the target material is needed to withstand high-power sputtering applications.
- **Target grain size:** Fine grain size provides higher strength and contributes to superior

STEPHANE FERRASSE, SUSAN STROTHERS and **CHRISTIE HAUSMAN** are with Honeywell Electronic Materials, Spokane, WA.

film uniformity. Consistent grain structure throughout the target provides stable uniformity through target life.

- **Target strength:** Sufficient yield strength is required to prevent target warping, which can contribute to film non-uniformity and arcing.

Key solutions to those challenges include:

- **Alloying or doping** is an extremely common way to add strength, increase thermal stability and promote grain refinement in all metals. Unfortunately, in semiconductor applications it is usually not desirable for alloys or doping elements to become part of the thin film itself, so it is rarely an option. The exception is when the alloying element improves the thin film properties.
- **The use of high strength backing plates** bonded to high purity targets to add strength to the entire target assembly. This is a very common and acceptable practice, but it introduces several risks and manufacturing challenges, such as a failed bond, arcing at the bond line and deflection in the assembly. Coefficient of thermal expansion (CTE) mismatches between the target and the backing plate can also pose serious challenges to target manufacturing, especially for brittle materials. Furthermore, the use of high-temperature bonding methods can cause grain growth and destroy desirable target metallurgical properties. This necessitates trade-offs between grain size, bond type and bond strength.
- **Improvements in TMP** to improve the microstructure, as described in the next section.

TMP fabrication overview

The choice of fabrication method has an impact on sputtering performance because the more deformation applied to the metal, the smaller the grain size. Two types of TMP, shown schematically in

FIGURE 1, are described below.

- **Conventional TMP.** This uses a combination of forging, rolling and heat treatment steps to obtain finer microstructures. It delivers good results and has been the industry standard. It is, however, restricted in terms of the amount of strain and deformation it can impart on the material. The amount of deformation, often expressed as a percent reduction of billet height, is limited to about 90% (equivalent strain of 2.3) in practice for targets. Higher reductions of greater than 90% require excessive tonnage and initial billet height, and impose severe requirements on conventional TMP equipment (stroke, daylight and tonnage capability). The maximum attainable strain of approximately 2.3 is not optimal for refinement of grain size. This,



Figure 1: Schematic of ECAE (note: P is punch pressure and τ_t is the friction along channels) and Conventional TMP

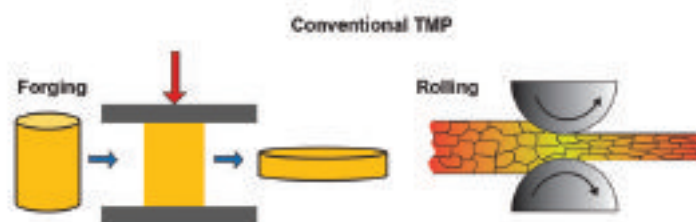


FIGURE 1. Schematic of ECAE (note: P is punch pressure and τ_t is the friction along channels) and conventional TMP.

combined with the need for a backing plate to add strength, may not meet the needs of high-performance IC applications.

- **ECAE.** This is a state-of-the-art extrusion process that is specifically designed to deliver the next level of microstructure performance. A billet is extruded through two intersecting channels of equal cross-sections – allowing attainable strains of 4.6-7, equivalent to greater than 99.9% reduction. As shown in **FIGURE 1**, the channels meet at a 90-degree angle and severe plastic deformation is realized uniformly by simple shear, in multiple passes, without changing the size or shape of the starting

material. ECAE also has the flexibility to manipulate the metal in multiple directions. Together, these features enable submicron and homogeneous microstructures.

Performance comparisons

Finer grain structures result in improved yield strength and ultimate tensile strength, as described below

Grain Sizes The attainable grain sizes for ECAE versus conventional TMP methods are shown in **TABLE 1**. As shown, the extreme deformation of ECAE results in finer microstructures, and thus improved strength. Grain sizes from 0.2-0.8 μm can be achieved for monolithic targets, a refinement in grain size by a factor of up to 100 times depending on the material.

Strength The ability of ECAE grain refinement to improve yield strength (YS) and ultimate tensile strength (UTS) is dramatic. YS, in particular, is critical for target applications because it governs the onset of permanent plastic deformation that leads to target warping. As shown in **FIGURE 2**, the yield strength of several ECAE submicron grained, high purity materials – including Al-0.5 wt% Cu, Cu, Cu-0.11 wt% Al, and Cu-1% Mn – is four to six times higher than a conventional TMP material.

Thermal Stability Thermal stability in terms of a material's resistance to grain growth during sputtering is critical for consistent thin-film uniformity. The grain structures in Table 1 for both ECAE and conventional TMP materials are stable under high power sputtering conditions.

Metallurgical Defects Any heat treatment can

Target Material	ECAE	Conventional TMP
Pure Aluminum (Al)	60-80	200-1000
Al Alloys	0.4-0.5	30-200
Copper Alloys (Cu)	0.2-0.4	30-150
Tantalum (Ta)	0.5-0.8	50-150
Titanium (Ti)	0.2-0.3	8-30

TABLE 1. Achievable Grain Sizes, μm

Figure 2: Strength of Submicron Grained ECAE versus Conventional TMP

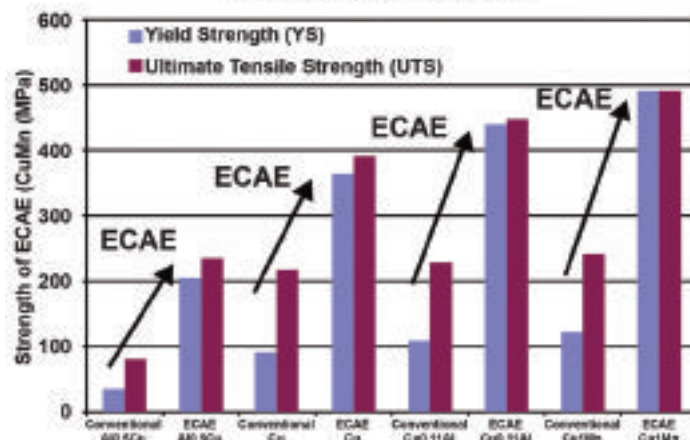
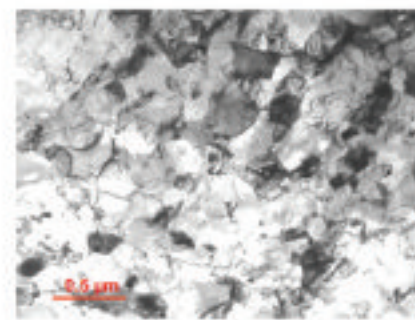


FIGURE 2. Strength of submicron grained ECAE versus conventional TMP.



Optical Micrograph
100X Magnification



Transmission Electron Micrograph
10,000X Magnification

FIGURE 3. Comparison of Second Phases in Conventional TMP (left) and ECAE Al-0.5% Cu (right).

be performed prior to ECAE because the level of grain refinement during ECAE does not depend on initial grain size. Therefore, traditional heat treatment such as solutionizing used in conventional TMP can be completely replaced or combined optimally with ECAE to remove or refine second phase precipitates. For example, as shown in **FIGURE 3** in the optical micrograph, a conventional TMP Al_{0.5}Cu exhibits 1-7 μm (AlCu) second phases. However, during the multi-pass ECAE process at room temperature, repetitive shearing, elongation, breakage and homogenization of second phases leads to their refinement to less than 100 nm as displayed in the TEM image of submicron ECAE Al_{0.5}Cu. This is a dramatic refinement of second phases by a factor of over 100 compared to conventional TMP targets. ECAE has a similar effect on refinement and reduction of other material defects such as voids, inclusions or dendrites.

ECAE cost-performance benefits

The properties of ECAE targets described above provide important cost-performance benefits over conventional TMP techniques, allowing users to lower their total CoO. A few key examples are described below.

Monolithic Design Improves Target Life and Productivity

With ECAE, previously bonded planar Al and Cu alloy targets can be designed as single-piece, monolithic targets. This translates into a longer target life versus their bonded counterparts produced via conventional TMP. As shown in **FIGURE 4**, sputtering is not limited by the bond line and therefore, the erosion groove can extend much deeper for optimum material utilization. In fact, monolithic ECAE submicron Al and Cu alloy targets (200 mm and 300 mm) show a 20-100% increase in target life.

This longer target life equates to cost savings by:

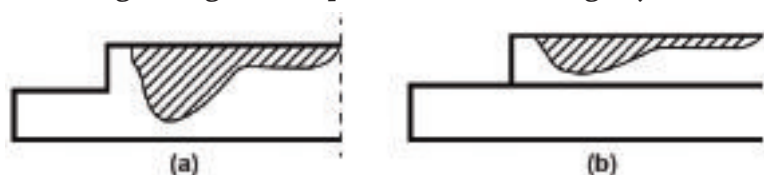


FIGURE 4. Erosion profile of a monolithic planar target design (a) and conventional bonded design (b).

- Reducing downtime associated with target changes for greater tool utilization.
- Reducing the cost per kWh of the sputtering target.
- Eliminating risks associated with backing plates such as de-bonding or deflection.

Improved Wafer Yield Due To Improved

Performance An even greater cost savings for users is the increase in wafer yield associated with better performing sputtering targets. Second-phase precipitates, inclusions and voids all contribute to arcing and subsequent wafer-killing defects. Minimizing these defects drastically reduces potential sources for arcing. Additionally, submicron microstructures are more resistive, which increases the threshold voltage for arcing and enhances plasma stability. Put simply, when arcing is reduced, wafer particles are reduced and wafer yield is increased. Increasing wafer yield has the single most dramatic impact on device cost.

Summary

Sputtering targets produced via TMP – both conventional and ECAE – are designed to meet thin film deposition needs. ECAE, however, has the added ability to meet more challenging IC geometries and performance. Because it can achieve extreme deformation, ECAE can deliver submicron, high strength and uniform microstructures.

The resulting improvements in strength allow for monolithic targets with a longer target life of 20-100%, depending on design. Added to this is the ability of ECAE to minimize arcing, and to reduce the size of precipitates and inclusions and other metallurgical defects, while meeting needs for chemical purity and thermal stability. Manufacturers can reduce their CoO through improvements in thin film uniformity, greater productivity, higher wafer yield, lower production costs and less downtime. ♦

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Simply obeying the laws of economics

There are laws and then there are laws. “Moore’s Law” to me is more of an observation. Gordon Moore simply noticed what was going on and commented on it. Powerful laws, to me, are usually laws of physics like Newton’s law of gravity or Einstein’s Law of relativity.

When we consider the laws of economics, many economists would contend that consolidation is a law, i.e., a natural process which has happened consistently to all industries since the industrial revolution. Through consolidation a mature industry usually has only a few (2-3) players (for instance Boeing and Airbus in the aircraft manufacturing business) whereas young industries like the internet may initially have hundreds.

So what does this have to do with microelectronics you might ask? Well, just ask the former employees of Altera and Broadcom. If this were the early 1990’s James Carville (Clinton’s spinmeister) would respond “It’s consolidation stupid” (although I am not a Carville fan). Consolidation is what happens as industries mature. We are in the midst of it, it’s natural and probably unstoppable.

Let’s first take a look at what’s happened in the hard disk drive segment of our industry.

Greater than 200 companies have been in the hard disk drive business since the 1960’s. They initially competed on data density and latency and smaller

form factors. Most of that industry has vanished through bankruptcy, mergers

and acquisitions. Surviving manufacturers are Seagate, Toshiba and Western Digital. Seagate acquired Samsung’s HDD business in 2011; Western Digital (WD) merged with Hitachi’s HDD business in 2011. This gave Seagate 40% of the HDD market and WD ~ 48%. The remaining ~ 12% was owned by Toshiba who acquired Fujitsu’s HDD business in 2009. Thus by 2012 what was several hundred players had been whittled down to 3 by, I contend, the laws of economics.

Now let’s look at DRAM. In 1980 there were 40+ DRAM fabricators but by 2015 we are down to Samsung, Hynix and Micron. See the trend?

The best description that I have seen of what’s happening is the 2002 Harvard Business Review article “The Consolidation Curve” by G. K. Deans, et. al. Their main point is that all industries have similar life cycles and knowing where your company stands in the process can help you plot a winning strategy.

They divide up the stages of all industries as follows:

Stage 1: the combined market share of the three largest companies is between 10% and 30%. Companies in stage 1 industries aggressively defend their first-in advantage by building scale, creating a global footprint and establishing barriers to entry, i.e. protecting proprietary technology or ideas. Stage 1 companies focus more on revenue than profit, working to amass market share.

Stage 2 is all about scaling. Major players begin to emerge and buy up competitors. The top three players in a stage 2 industry will own 15% – 45% of their market, as the industry consolidates. The companies that reach stage 3 must be among the first players in the industry to capture the most important markets and expand their global reach.

Stage 3: Companies focus on expanding core business and continuing to aggressively outgrow the competition. The top three industry players will control between 35% and 70% of the market with five to 12 major players remaining. This is a period of large-scale consolidation plays.

Stage 4: In stage 4 the top three companies claim as much as 70% to 90% of the market. Large companies may form alliances with their peers because growth is now more challenging. Companies in stage 4 must defend their leading positions. They must be alert to the danger of being lulled into complacency by their own dominance. Stage 4 companies must create growth by spinning off new businesses or buying into aligned fields to broaden their market presence.

When you understand this then headlines like the recent “The next three chip firms to be acquired: Atmel, Lattice and Cavium are the top take out candidates for the rest of 2015.”

As most of the segments of our industry enter late stage 3 or early stage 4 the only question is whether you will acquire or be acquired, or as Carville said “It’s the economy, stupid!” ♦



DR. PHIL GARROU,
Contributing Editor



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