

Solid State TECHNOLOGY

Insights for Electronics Manufacturing

**Fan-Out Wafer
Level Packaging**

P. 22

**Extending Tungsten
Metallization**

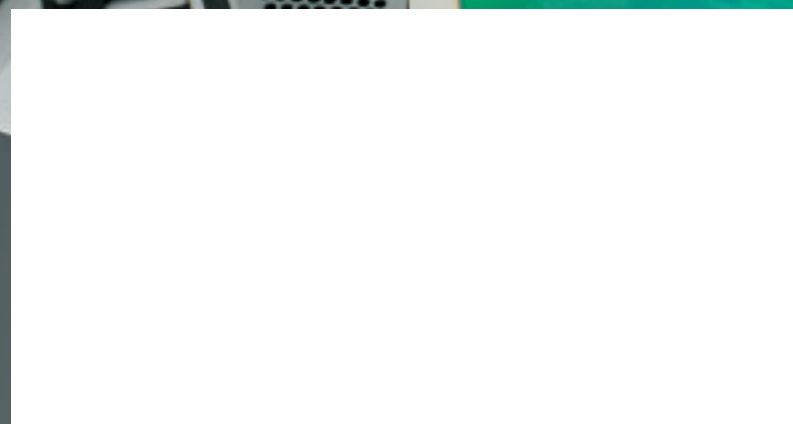
P. 26

**Ensuring Safety in
the Sub-fab**

P. 30

Uniformity Control in Plasma Etch

P.16





THIS IS EFFICIENCY

*FR Series UHP
single-stage
pressure regulators*

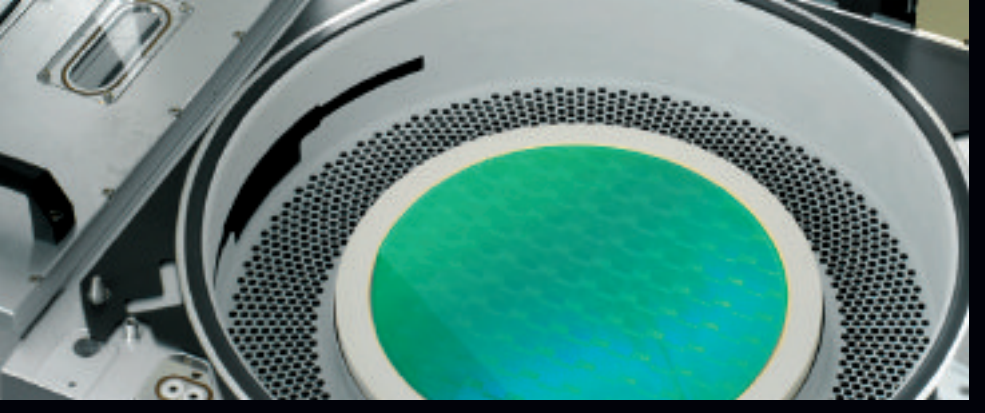
*Provides precise control
of process gas*

Parker enables its partners in the semiconductor industry to cost-efficiently control process gases in downstream point-of-use applications with its new lines of FR 1000 and FR 1400 Series UHP regulators. This reflects Parker's commitment to engineering short- and long-term costs. **Call Parker's Veriflo Division at (510) 235-9590 to learn more or visit solutions.parker.com/semicon**



ENGINEERING YOUR SUCCESS.

©2016 Parker Hannifin Corporation SS-2-1



Etch chambers have been designed to produce similar plasma conditions on every location on the wafer to achieve uniform process results. Source: Lam Research

FEATURES

16

ETCHING | [Evolution of across-wafer uniformity control in plasma etch](#)

A look at control of process uniformity across the wafer during plasma etch processes.

Stephen Hwang and Keren Kanarik, Lam Research Corporation, Fremont, CA

22

FOWLP | [Fan-Out Wafer Level Packaging \(FOWLP\): Breakthrough advantages and surmountable challenges](#)

New wafer processing technologies overcome FOWLP's technical hurdles, paving the way for a new generation of ultra compact, high I/O electronic devices.

David Butler, SPTS Technologies, an Orbotech company, Yavne, Israel

26

TUNGSTEN | [Extending tungsten metallization for next-generation devices](#)

Recent breakthroughs in materials engineering of low-resistance W barriers/liners and bulk fill are making it possible to extend W use to next-generation devices.

Jonathan Bakke, Applied Materials, Santa Clara, CA

30

SAFETY | [Ensuring safety in the sub-fab](#)

Problems frequently arise as a result of an incomplete or absent formal risk assessment when processes are modified or new materials introduced.

Alan Ifould and Andrew Chambers, Edwards, North Somerset, UK

36

PROCESS WATCH | [Process control and production cycle time](#)

Having more process control points will not immediately change the number of excursions in a fab but it will immediately improve the efficiency with which the fab reacts to them.

By Douglas G. Sutherland and David W. Price, KLA-Tencor, Milpitas, CA

40

MEASUREMENT | [Advancements in RH measurement in wafer and reticle environments](#)

A wireless wafer-like humidity sensor can simultaneously measure RH across the wafer and in critical processes

Allyn Jackson, CyberOptics Corp., Minneapolis, MN

45

SEMICON WEST | [Changing markets drive smarter manufacturing by IC sector](#)

A day-long forum will be held at SEMICON West on the future of smart manufacturing in the semiconductor supply chain.

Paula Doe, SEMI, San Jose, CA

COLUMNS

- 2 **Editorial** | HITRS roadmap aims to integrate photonics and CMOS,
Pete Singer, Editor-in-Chief
- 12 **Packaging** | X-Celeprint and RTI propose FOWLP free of mold compound,
Phil Garrou, Contributing Editor
- 13 **Semiconductors** | Applied Materials releases selective etch tool,
Ed Korczynski, Sr. Technical Editor
- 48 **Industry Forum** | Time to uncover the process mystery for IC designs,
Dr. Zhihong Liu, Chairman and CEO, ProPlus Design Solutions

DEPARTMENTS

- 4 Web Exclusives
- 6 News
- 46 Ad Index



HITRS roadmap aims to integrate photonics

A new roadmap, the Heterogeneous Integration Technology Roadmap for Semiconductors (HITRS), aims to integrate fast optical communication made possible with photonic devices with the digital crunching capabilities of CMOS.

The roadmap, announced publicly for the first time at The ConFab in June, is sponsored by IEEE Components, Packaging and Manufacturing Technology Society (CPMT), SEMI and the IEEE Electron Devices Society (EDS).

Speaking at The ConFab, Bill Bottoms, chairman and CEO of 3MT Solutions, said there were four significant issues driving change in the electronics industry that in turn drove the need for the HITRS roadmap: 1) The approaching end of Moore's Law scaling of CMOS, 2) Migration of data, logic and applications to the Cloud, 3) The rise of the internet of things, and 4) Consumerization of data and data access.

"CMOS scaling is reaching the end of its economic viability and, for several applications, it has already arrived. At the same time, we have migration of data, logic and applications to the cloud. That's placing enormous pressures on the capacity of the network that can't be met with what we're doing today, and we have the rise of the Internet of Things," he said. The consumerization of data and data access is something that people haven't focused on at all. "If we are not successful in doing that, the rate of growth and economic viability of our industry is going to be threatened," Bottoms said.

These four driving forces present requirements that cannot be satisfied through scaling CMOS. "We have to have lower power, lower

latency, lower cost with higher performance every time we bring out a new product or it won't be successful," Bottoms said. "How do we do that? The only vector that's available to us today is to bring all of the electronics much closer together and then the distance between those system nodes has to be connected with photonics so that it operates at the speed of light and doesn't consume much power. The only way to do this is to use heterogeneous integration and to incorporate 3D complex System-in-Package (SiP) architectures.

The HITRS is focused on exactly that, including integrating single-chip and multichip packaging (including substrates); integrated photonics, integrated power devices, MEMS, RF and analog mixed signal, and plasmonics. "Plasmonics have the ability to confine photonic energy to a space much smaller than wavelength," Bottoms said. More information on the HITRS can be found at: <http://cpmt.ieee.org/technology/heterogeneous-integration-roadmap.html>

Bottoms said much of the technology exists today at the component level, but the challenge lies in integration. He noted today's capabilities include Interconnection (flip-chip and wire bond), antenna, molding, SMT (passives, components, connectors), passives/integrated passive devices, wafer pumping/WLP, photonics layer, embedded technology, die/package stacking and mechanical assembly (laser welding, flex bending).

"We have a large number of components, all of which have been built, proven, characterized and in no case have we yet integrated them all. We've integrated more and more of them, and we expect to accelerate that in the next few years," he said.

—Pete Singer, Editor-in-Chief

Solid State TECHNOLOGY®

Pete Singer, Editor-in-Chief
Ph: 978.470.1806,
psinger@extensionmedia.com

Shannon Davis, Editor, Digital Media
Ph: 603.547.5309
sdavis@extensionmedia.com

Ed Korczynski, Senior Technical Editor,
edk@extensionmedia.com

Jeff Dorsch, Contributing Editor

Phil Garrou, Contributing Editor

Dick James, Contributing Editor

Vivek Bakshi, Contributing Editor

Sara Ver-Bruggen, Contributing Editor,
Semiconductor Manufacturing & Design

CREATIVE/PRODUCTION/ONLINE

LS Jerrett, Production Traffic Coordinator

Nicky Jacobson, Senior Graphic Designer

Simone Bradley, Graphic Designer

Slava Dotsenko, Senior Web Developer

Jon Franke, Media Coordinator

MARKETING/CIRCULATION

Jenna Johnson,
jjohnson@extensionmedia.com

CORPORATE OFFICERS

Extension Media, LLC

Vince Ridley, President and Publisher
vrldley@extensionmedia.com

Clair Bright, Vice President and Publisher
Embedded Electronics Media Group
cbright@extensionmedia.com

Melissa Sterling, Vice President,
Business Development
msterling@extensionmedia.com

For subscription inquiries:

Tel: 847.559.7500; Fax: 847.291.4816;
Customer Service e-mail: ssst@omeda.com;
Subscribe: www.sst-subscribe.com

Solid State Technology is published eight times a year by Extension Media LLC, 1786 Street, San Francisco, CA 94107. Copyright © 2016 by Extension Media LLC. All rights reserved. Printed in the U.S.

JULY 2016 VOL. 59 NO. 4 • **Solid State Technology** ©2016 (ISSN 0038-111X) **Subscriptions:** Domestic: one year: \$258.00, two years: \$413.00; one year Canada/Mexico: \$360.00, two years: \$573.00; one-year international airmail: \$434.00, two years: \$691.00; Single copy price: \$15.00 in the US, and \$20.00 elsewhere. Digital distribution: \$130.00. You will continue to receive your subscription free of charge. This fee is only for air mail delivery. Address correspondence regarding subscriptions (including change of address) to: *Solid State Technology*, 1786 18th Street, San Francisco, CA 94107-2343. (8 am – 5 pm, PST).

Extension
MEDIA

1786 18th Street
San Francisco, CA 94107

HEIDENHAIN – expanding horizons in semiconductor fabrication

Come see us at

**SEMICON
WEST**

BOOTH #1809

- Repeatability $\pm 0.001 \mu\text{m}$ (1 nm) @90 m/min
- 450 mm ready
- Ideal for ultra-high-precision positioning subassemblies

In the world of ultra-precise wafer lithography and inspection, HEIDENHAIN's depth of knowledge gives machine builders the ultimate competitive advantage – access to next-generation R&D that's deployable today. Case in point: our high precision LIP 400 linear and ROP 8080 angle encoders boost speed, repeatability and yield without sacrificing accuracy.

For an inside look at what's coming tomorrow contact us today.

1-847-490-1191

www.HEIDENHAIN.us

HEIDENHAIN
Angle Encoder
ROP 8080

HEIDENHAIN
Linear Encoder
LIP 400

HEIDENHAIN
Linear Encoder
LIP 400



HEIDENHAIN
The Measure of Excellence

Photo Credit: Ultra-High-Precision Positioning System from ETEL S.A.

Web Exclusives

An interview with Dr. Dongkai Shangguan

Dr. Dongkai Shangguan is currently the Chief Marketing Officer of STATS ChipPAC. Previously, Dongkai served as the founding CEO of the National Center for Advanced Packaging Co., Ltd., worked for 10 years at Ford Motor Company in various technical and management functions, and for 11 years at Flextronics as Corporate Vice President of Global Advanced Technology.

<http://bit.ly/1timOOS>

More change for the chip industry

As if scaling to 7nm geometries and going vertical with FinFETs, TSVs and other emerging technologies wasn't challenge enough, the emerging market for connected smart devices will bring more changes to the semiconductor sector. And then there's 3D printing looming in the wings.

<http://bit.ly/1JN1Tav>

Changing markets drive smarter manufacturing by IC sector

The changing market for ICs means the end of business as usual for the greater semiconductor supply chain. Smarter use of data analytics looks like a key strategy to get new products more quickly into high yield production at improved margins.

<http://bit.ly/1sEFUhw>

ASMC 2016 Conference has highest attendance ever; Chipworks achieves twelfth paper

ASMC is an annual conference focused on the manufacturing of semiconductor devices; in this it differs from other conferences, since the emphasis is on what goes on in the wafer fab, not the R&D labs, and the papers are not research papers – some are better described as “tales from the fab”! After all, it's the nitty-gritty of manufacturing in the fab that gets the chips out of the door, and this meeting discusses the work that pushes the yield and volumes up and keeps them there.

<http://bit.ly/28VWSiJ>



Insights from the Leading Edge: Samsung Electro-Mechanics enters FOWLP packaging market

Samsung Electronics System LSI and Samsung Electro-Mechanics will join forces to staff the project and launch the business. They will transform current LCD assembly lines in Cheonan KR into IC packaging lines. It is unclear whether they have developed full panel processing capability, which many packaging OSATS have been trying to accomplish, or they will work in smaller formats.

<http://bit.ly/28QQuX0>

Latest on EUVL development to be discussed in EUVL Workshop in Berkeley

This year's 2016 EUVL Workshop is being held in Berkeley, CA, organized in cooperation with CXRO. With keynotes from Intel, GlobalFoundries and ASML, along with 45 speakers and about 50 papers, we expect to hear a good bit of new information on these topics and stimulating discussion of R&D topics.

<http://bit.ly/28QQEEk>

Contact resistance and its role in limiting transistor performance

In logic devices, contacts and local interconnects form the critical electrical pathways between the transistors and the rest of the circuit. Low resistivity is therefore crucial for robust and reliable device performance. Consequently, low-resistivity CVD tungsten (W) has historically been used for logic contact and local interconnect fill. (From SemiMD.com)

<http://bit.ly/28P3nn9>

Eloquent executives ecosystem expositions

With dimensional scaling reaching economic limits, each company in the IC fab industry must rely upon trusted connections with customers and suppliers to know which way to go, and the only way to gain trusted connections is through attending live events. Fortunately, whether you are an executive, and engineer, or an investor, there is at least one must-attend event happening these days to keep you informed. (From SemiMD.com)

<http://bit.ly/28OsU3A>



Delivering Real-world Solutions



Today's lithography systems provide overlay accuracy and throughput capabilities far beyond what was previously thought possible. However, it is real-world, on-product performance that is vital to chipmakers.

Nikon combines superior stepper and scanner technology with innovative software solutions to deliver exceptional manufacturing performance and productivity—now and for the future.

Nikon. Delivering Real-world Solutions.

See Nikon at SEMICON West 2016 - **Visit booth 1705** in South Hall to learn about the latest Nikon semiconductor lithography solutions and MEMS exposure systems.

www.nikonprecision.com

worldnews

USA - Amkor Technology

received Qualcomm Technologies' 2015 Supplier of the Year award.

ASIA - GLOBALFOUNDRIES

announced plans to expand presence in China with 300mm fab in Chongqing.

EUROPE - EV Group scored its fourth consecutive triple crown win in the annual VLSI research customer satisfaction survey.

USA - Ultratech, Inc. announced its LXA melt laser annealing technology enabled the world's lowest contact resistivity for finFETs.

ASIA - Samsung introduced a new line-up of LED components for automotive lighting, featuring chip-scale packaging.

EUROPE - Leti teams have demonstrated how Fully Depleted Silicon on Insulator (FDSOI) technology can be scaled downwards and how the experience in thin-film engineering built on FDSOI development can be harnessed for innovative architectures and computing paradigms.

USA - FEI launched three new tools for next-generation semiconductor manufacturing.

EUROPE - Soitec receives Best Quality Award from NXP Semiconductors.

USA - Electronic Fluorocarbons began construction of manufacturing facility in Pennsylvania.

EUROPE - ams signed an agreement to acquire Cambridge CMOS Sensors Ltd (CCMOSS).

ASIA - Samco held a completion ceremony for its second production center on June 17.

Equipment spending up: 19 new fabs and lines to start construction

This month, SEMI announced that 19 new fabs and lines are forecasted to begin construction in 2016 and 2017, according to the latest update of the SEMI World Fab Forecast report. While semiconductor fab equipment spending is off to a slow start in 2016, it is expected to gain momentum through the end of the year.

For 2016, 1.5 percent growth over 2015 is expected while 13 percent growth is forecast in 2017.

Fab equipment spending—including new, secondary, and in-house—was down 2 percent in 2015. However, activity in the 3D NAND, 10nm Logic, and Foundry segments is expected to push equipment spending up to US\$36 billion in 2016, 1.5 percent over 2015, and to \$40.7 billion in 2017, up 13 percent. Equipment will be purchased for existing fabs, lines that are being converted to leading-edge technology, as well as equipment going into new fabs and lines that began construction in the prior year.

Table 1 shows the regions where new fabs and lines are expected to be built in 2016 and 2017. These projects have a probability of 60 percent or higher, according to SEMI's data. While some projects are already underway, others may be subject to delays or pushed into the following year. The SEMI World Fab Forecast report, published May 31, 2016, provides more details about the construction boom.

New Fabs & Lines Beginning Construction (2016 & 2017)

Region	2016	2017
Americas	1 Analog	1 Foundry
China	1 Memory 1 MEMS (200mm) 1 Foundry 1 LED (100mm)	1 Memory 1 MEMS (200mm) 3 Foundry 1 Power (200mm)
Europe & Mideast	1 Power	
Japan		1 Memory
Korea	1 Memory	
SE Asia	1 LED (150mm)	1 Analog (200mm)
Taiwan	1 Foundry	1 LED (50mm)
Potential Capacity in 300mm (excluding LED)	210,000 wspm	330,000 wspm
Probabilities 60% or higher. All 300mm unless specified differently		
Source: World Fab Forecast report, June 2016, SEMI (www.semi.org)		

Breaking down the 19 projects by wafer size, 12 of the fabs and lines are for 300mm (12-inch), four for 200mm, and three LED fabs (150mm, 100mm, and 50mm). Not including LEDs, the potential installed capacity of all these fabs and lines is estimated at almost 210,000 wafer starts per month (in 300mm equivalents) for fabs beginning construction in 2016 and 330,000 wafer starts per month (in 300mm equivalents) for fabs beginning construction in 2017.

In addition to announced and planned new fabs and lines, SEMI's World Fab Forecast provides information about existing fabs and lines with associated construction spending, e.g. when a cleanroom is converted to a larger wafer size or a different product type.

In addition, the transition to leading-edge technologies (as we can see in planar technologies, but also in 3D technologies) creates a reduction in installed capacity within an existing fab. To compensate for this reduction, more conversions of older fabs may take place, but also additional new fabs and lines may begin construction. ◀

Tiny lasers enable faster, less power-hungry next-gen microprocessors

A group of scientists from Hong Kong University of Science and Technology; the University of California, Santa Barbara; Sandia National Laboratories and Harvard University were able to fabricate tiny lasers directly on silicon — a huge breakthrough for the semiconductor industry and well beyond.

For more than 30 years, the crystal lattice of silicon and of typical laser materials could not match up, making it impossible to integrate the two materials — until now.

As the group reports in Applied Physics Letters, from AIP Publishing, integrating subwavelength cavities — the essential building blocks of their tiny lasers — onto silicon enabled them to

Continued on page 9

Long-term strategy pays off as TI maintains analog leadership

The 2015 analog market grew 2% to \$47.0 billion. Combined sales of general-purpose analog products (amplifiers/comparators, interface, power management, and signal conversion devices) increased 2% to \$19.1 billion and sales of application-specific analog devices also improved 2% to \$27.9 billion. Among analog IC products the market for signal conversion devices showed the largest increase in 2015, growing 14% to \$2.9 billion.

IC Insights' ranking of top analog IC suppliers for 2015 is shown in Figure 1. Collectively, these 10 companies accounted for 56% of global analog sales last year, down slightly from 57% in 2014. Among the top suppliers, nine had analog sales in excess of

Continued on page 10

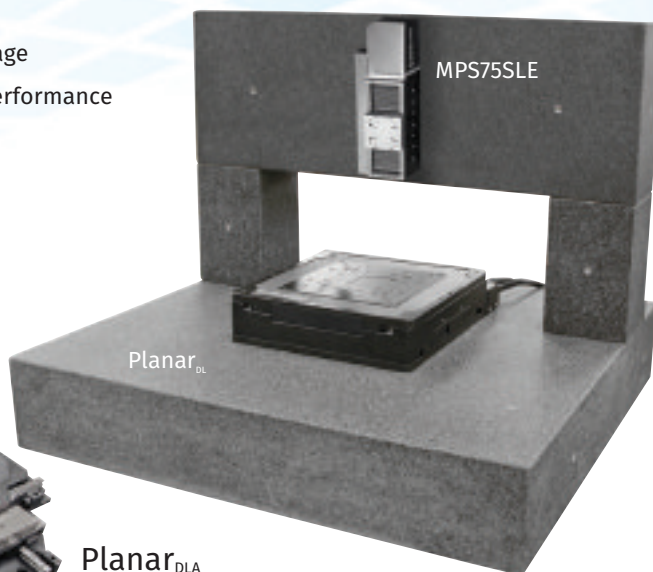
Aerotech Motion Solutions for Surface Measurement

Planar_{DL}

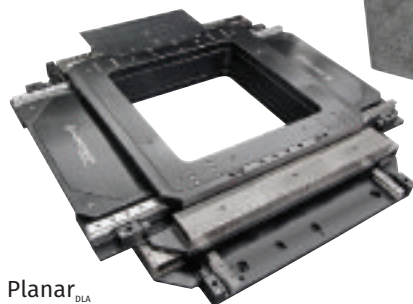
- Linear motor XY positioning stage
- Provides superior geometric performance in a low-profile package

MPS75SLE

- Compact positioning stage with direct feedback
- Allows for precise positioning of measurement sensor



Planar_{DIA}



Planar_{DIA}

- Open-frame XY positioning stage
- Allows simultaneous access to both sides of workpiece

Expert motion solutions for surface measurement that include:

- Advanced 2D calibration available with Aerotech control system
- Excellent geometric characteristics
- Low CTE encoder substrate
- Integral cable management for clean, professional appearance
- High-accuracy Z-stage with linear encoder for sensor positioning



Add an Aerotech award-winning control system for a complete motion solution.

Contact an Aerotech Engineer today to discuss your application.

Ph: 412-963-7470 • Email: sales@aerotech.com • www.aerotech.com

WORLD HEADQUARTERS: USA
THE AMERICAS • EUROPE & MIDDLE EAST • ASIA-PACIFIC



*Dedicated to the
Science of Motion*

AH05168-TMG

Automotive semiconductor market grows slightly in 2015 while ranks shift

Despite slower growth for the automotive industry and exchange rate fluctuations, the automotive semiconductor market grew at a modest 0.2 percent year over year, reaching \$29 billion in 2015, according to IHS (NYSE: IHS), a global source of critical information and insight.

A flurry of mergers and acquisitions last year caused the competitive landscape to shift, including the merger of NXP and Freescale, which created the largest automotive semiconductor supplier in 2015 with a market share of 14.3 percent, IHS said. The acquisition of International Rectifier (IR) helped Infineon overtake Renesas to secure the second-ranked position, with a market share of 9.8 percent. Renesas slipped to third-ranked position in 2015, with a market share of 9.1 percent, followed by STMicroelectronics and Texas Instruments.

“The acquisition of Freescale by NXP created a powerhouse for the automotive market. NXP increased its strength in automotive infotainment systems, thanks to the robust double-digit growth of its i.MX processors,” said Ahad Buksh, automotive semiconductor analyst for IHS Technology. “NXP’s analog integrated circuits also grew by double digits, thanks to the increased penetration rate of keyless-entry systems and in-vehicle networking technologies.”

NXP will now target the machine vision and sensor fusion markets with the S32V family of processors for autonomous functions, according to the IHS Automotive Semiconductor Intelligence Service. Even on the radar front, NXP now has a broad portfolio of long- and mid-range silicon-germanium (SiGe) radar chips, as well as short-range complementary metal-oxide semiconductor (CMOS) radar chips under development. “The fusion of magnetic sensors from NXP, with pressure and inertial sensors from Freescale, has created a significant sensor supplier,” Buksh said.

The inclusion of IR, and a strong presence in advanced driver assistance systems (ADAS), hybrid electric vehicles and other growing applications helped Infineon grow 5.5 percent in 2015. Infineon’s 77 gigahertz (GHz) radar system integrated circuit (ASIC) chip family strengthened its position in ADAS. Its 32-bit microcontroller (MCU) solutions, based on TriCore architectures, reinforced the company’s position in the powertrain and chassis and safety domains.

The dollar-to-yen exchange rate worked against the revenue ranking for Renesas for the third consecutive year. A major share of Renesas business is with Japanese customers, which is primarily conducted in yen. Even though Renesas’ automotive semiconductor revenue fell 12 percent, when measured in dollars, the revenue actually grew by about 1 percent in yen. Renesas’ strength continues to be its MCU solutions, where the company is still the leading supplier globally.

STMicroelectronics’ automotive revenue declined 2 percent year over year; however, a larger part of the decline can be attributed to the lower exchange rate of the Euro against the U.S. dollar in 2015, which dropped 20 percent last year. STMicroelectronics’ broad-based portfolio and its presence in every growing automotive domain of the market helped the company maintain its revenue as well as it did. Apart from securing multiple design wins with American and European automotive manufacturers, the company is also strengthening its relationships with Chinese auto manufacturers. Radio and navigation solutions from STMicroelectronics were installed in numerous new vehicle models in 2015.

Texas Instruments has thrived in the automotive semiconductor market for the fourth consecutive year. Year-over-year revenue increased by 16.6 percent in 2015. The company’s success story is not based on any one particular vehicle domain. In fact, while all domains have enjoyed double-digit increases, infotainment, ADAS and hybrid-electric vehicles were the primary drivers of growth.

Other suppliers making inroads in automotive

After the acquisition of CSR, Qualcomm rose from its 42nd ranking in year 2014, to become the 20th largest supplier of automotive semiconductors in 2015. Qualcomm has a strong presence in cellular baseband solutions, with its Snapdragon and Gobi processors; while CSR’s strength lies in wireless application ICs — especially for Bluetooth and Wi-Fi. Qualcomm is now the sixth largest supplier of semiconductors in the infotainment domain.

Moving from 83rd position in 2011 to 37th in 2015, nVidia has used its experience, and its valuable partnership with Audi, to gain momentum in the automotive market. The non-safety critical status of the infotainment domain was a logical stepping stone to carve out a position in the automotive market, but now the company is also moving toward ADAS and other safety applications. The company has had particular success with its Tegra processors.

Due to the consolidation of Freescale, Osram entered the top-10 ranking of automotive suppliers for the first time in 2015. Osram is the global leader in automotive lighting and has enjoyed double-digit growth over the past three years, thanks to the increasing penetration of light-emitting diodes (LEDs) in new vehicles. ▶

Tiny lasers, Continued
from page 7

create and demonstrate high-density on-chip light-emitting elements.

To do this, they first had to resolve silicon crystal lattice defects to a point where the cavities were essentially equivalent to those grown on lattice-matched gallium arsenide (GaAs) substrates. Nano-patterns created on silicon to confine the defects made the GaAs-on-silicon template nearly defect free and quantum confinement of electrons within quantum dots grown on this template made lasing possible.

The group was then able to use optical pumping, a process in which light, rather than electrical current, "pumps" electrons from a lower energy level in an atom or molecule to a higher level, to show that the devices work as lasers.

"Putting lasers on microprocessors boosts their capabilities and allows them to run at much lower powers, which is a big step toward photonics and electronics integration on the silicon platform," said professor Kei May Lau, Department of Electronic and Computer Engineering, Hong Kong University of Science and Technology.

Traditionally, the lasers used for commercial applications are quite large — typically 1 mm x 1 mm. Smaller lasers tend to suffer from large mirror loss.

But the scientists were able to overcome this issue with



ELECTRONIC FLUOROCARBONS

ELECTRONIC SPECIALTY GASES

- ADVANCED. RELIABLE. CONSISTENT.
- PURITY AND INNOVATION
- ADVANCED MATERIALS
COMING SOON



NEW Plant Location:
3266 Bergey Road
Hatfield, PA 19940

+508-435-7000
www.efgases.com

“tiny whispering gallery mode lasers — only 1 micron in diameter — that are 1,000 times shorter in length, and 1 million times smaller in area than those currently used,” said Lau.

Whispering gallery mode lasers are considered an extremely attractive light source for on-chip optical communications, data processing and chemical sensing applications.

“Our lasers have very low threshold and match the sizes needed to integrate them onto a microprocessor,” Lau pointed out. “And these tiny high-performance lasers can be grown directly on silicon wafers, which is what most integrated circuits (semiconductor chips) are fabricated with.”

In terms of applications, the group’s tiny lasers on silicon are ideally suited for high-speed data communications.

“Photonics is the most energy-efficient and cost-effective method to transmit large volumes of data over long distances. Until now, laser light sources for such applications were ‘off chip’ — missing — from the component,” Lau explained. “Our work enables

Leading Analog IC Suppliers (\$M)

2015 Rank	Company	2014	2015	% Change	% Marketshare
1	Texas Instruments	8,104	8,340	3%	18%
2	Infineon	2,770	2,885	4%	6%
3	Skyworks Solutions	2,570	2,700	5%	6%
4	Analog Devices	2,615	2,665	2%	6%
5	ST	2,836	2,465	-13%	5%
6	Maxim	2,035	1,960	-4%	4%
7	NXP	1,730	1,905	10%	4%
8	Linear Technology	1,437	1,440	0%	3%
9	ON Semi	1,291	1,155	-11%	2%
10	Renesas	910	805	-12%	2%

Source: IC Insights, company reports

on-chip integration of lasers, an [indispensable] component, with other silicon photonics and microprocessors.”

The researchers expect to see this technology emerge in the market within 10 years.

Next, the group is “working on electrically pumped lasers using standard microelectronics technology,” Lau said. ◀

Long-term strategy, Continued from page 7

\$1.0 billion; five of these had sales in excess of \$2.0 billion. Only tenth-ranked Renesas fell short of the \$1.0 billion mark. With a 10% increase, NXP’s analog sales outperformed the total analog market by the widest margin (Figure 1).

Texas Instruments was again the leading supplier of analog devices in 2015 with \$8.3 billion in sales, which was good for 18% marketshare. TI’s analog sales slightly surpassed the combined revenue of the next three-largest analog suppliers, and represented 69% of its total semiconductor revenue last year. TI has always been a major player in analog, but beginning in 2009, it doubled down on its long-term efforts to dominate this market segment. That year, TI became the first company to manufacture analog devices on 300mm equipment. It purchased 300mm manufacturing tools from defunct Qimonda and transferred it to its existing fabs in Texas to build analog ICs. In 2010, TI acquired two wafer fabs operated by Spansion in Aizu-Wakamatsu, Japan, and a fully equipped 200mm fab in Chengdu, China from Cension Semiconductor Manufacturing. Both facilities were converted and immediately put to use making analog ICs. In April 2011, TI acquired National Semiconductor—its rival in many analog markets—for \$6.5 billion.

TI also strengthened its analog position by transitioning to 300mm manufacturing capacity at its newer RFAB and its older DMOS 6 fabs. Aside from boosting its analog manufacturing capacity, moving to 300mm wafer helped reduce total production costs by 40%, according to the company.

Other changes seen in the 2015 ranking include Infineon moving up one place to become the second-largest analog supplier and Skyworks Solutions moving up two spots to #3. ST slipped from #2 in 2014 to #5 in the 2015 ranking following its 13% decline in analog sales, which it attributed to soft equipment sales (computer, consumer, automotive, industrial) among its primary customers. Collectively, Infineon, NXP, and ST—Europe’s three-largest IC suppliers—accounted for 15% analog marketshare last year.

Skyworks continues to enjoy solid analog sales due to design wins with smartphones providers around the world. Skyworks Solutions makes analog and mixed signal semiconductors for Apple, Samsung, and other suppliers of mobile devices. Many of Skyworks’ power amplifier components are found in Apple’s iPhone 6 models. It has been estimated that Skyworks supplies \$4 worth of content for every iPhone 6 handset.

Medical Electronics Symposium 2016

Multiple Track Topics Include:

Track 1 - Designs, Components and Assembly for High-Density Medical Electronics Solutions

Track 2 - Next Generation Microelectronics for Changing Healthcare Markets

Register Today at www.smta.org/medical



MARYLHURST UNIVERSITY

SEPTEMBER 14 & 15, 2015 • PORTLAND, OR

REGISTER NOW

Although highly focused in mobile markets, Skyworks plans to expand into the automotive, home, and wearable markets to develop its presence in applications linked to the Internet of Things. Analog ICs such as audio amplifiers, op amps, and analog switches are building blocks for creating wearable applications. Skyworks' wireless technology is used in General Electric health-care equipment, and the company recently sealed a deal to supply high-performance filter solutions to Panasonic.

Analog Devices' analog sales grew 2% last year. One of its key analog ICs is a device that enables 3D/Force Touch, a feature available on the Apple Watch, the latest iPhones, and new generations of the iPad, that uses tiny electrodes to distinguish between a light tap and a deep press to trigger contextually specific controls.

Y2015 Rank	Company Name	2014 Revenue	2015 Revenue	2014 Market Share	2015 Market Share	Growth (YoY)
1	NXP	1881	4178	6.4%	14.4%	124.5%
2	Infineon Technologies	2702	2850	9.3%	9.8%	5.5%
3	Renesas Electronics	3032	2671	10.5%	9.2%	-11.9%
4	STMicroelectronics	2144	2096	7.4%	7.2%	-2.2%
5	Texas Instruments	1605	1871	5.5%	6.4%	16.0%
6	Robert Bosch	1621	1478	5.6%	5.1%	-8.8%
7	ON Semiconductor	1069	1142	3.7%	3.9%	6.8%
8	Micron Technology	706	661	2.4%	2.3%	-6.4%
9	Toshiba	729	652	2.5%	2.2%	-10.6%
10	Osram	568	646	2.0%	2.2%	13.7%
	Others	12946	10785	44.7%	37.2%	-16.7%
	Total	28963	29030	100.0%	100.0%	0.2%

Source: IHS

© 2016 IHS

IC Insights forecasts the total analog market to grow 4% this year, reaching \$49.1 billion and then surpass the \$50.0 billion mark for the first time in 2017 as analog sales climb to an expected \$51.4 billion. From 2015 to 2020, the analog market is forecast to grow at a compound annual growth rate of 6%, one point higher than the total IC market. ◀

X-Celeprint and RTI propose FOWLP free of mold compound



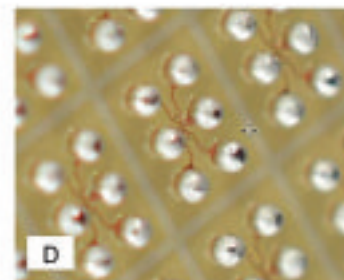
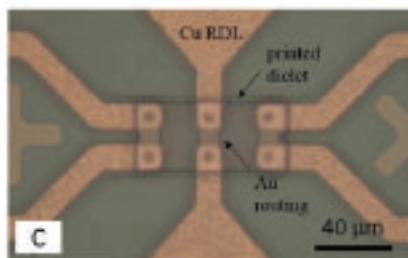
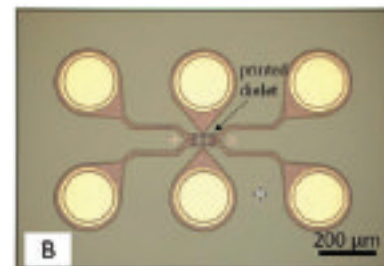
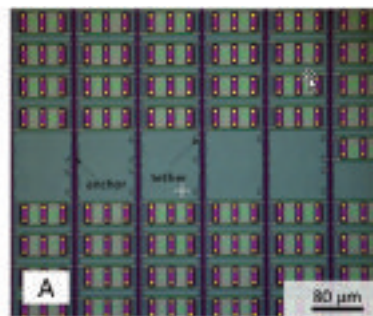
PHIL GARROU,
Contributing Editor

At the ECTC conference in May, in the “Advances in Fan Out Packaging” session, Matt Lueck of RTI International discussed the results of their joint program with X-Celeprint.

A common aspect to all fan-out packaging is the requirement to physically assemble devices into dispersed arrays, often called reconfigured wafers, which provides the real estate needed to fan-out. Devices made in sub-mm chip sizes can impose cost and performance challenges to FO-WLP using serial pick-and place assembly technologies. RTI and X-Celeprint joined forces to develop a fan out package for sub mm IC using the X-Celeprint massively parallel assembly technology called micro transfer-printing, which is well-suited for handling very thin and fragile devices.

In their micro transfer-printing technology a polymer layer is first applied to the substrate before the assembly process, and the devices are assembled in a face-up configuration. Following the formation of the reconfigured substrates, conventional redistribution layer (RDL) and solder ball processing was performed. Two different photo-imageable spin on dielectrics, HD4100 PI and Intervia 8023 epoxy, were used as the RDL dielectrics. The fan-out package contains no molding compound and is made using standard wafer-level packaging tools.

There are potential benefits from fan-out packaging strategies that do not require molding compound. The process described here does not suffer from the “die drift” that occurs during compression molded fan-out packaging which often requires special adaptive alignment techniques. It also does not suffer from the wafer and package warpage that can occur in molding compound based fan-out packages.



Micro-transfer printing was used to assemble reconfigured wafers of devices (80μm x 40μm chips with a redistribution metal and six contact pads), onto 200mm wafers. After assembly, they undergo a standard wafer level redistribution and bumping process. The final fan-out package pitch on the 200 mm wafer is 1.4mm x 1.0mm with six 250 μm solder bumps. The fan-out packages were assembled and reflowed onto FR4 test boards.

The Figure shows (A) the chiplet source wafer after partial removal of chiplets with the elastomer stamp; (B) a completed fan out package before solder ball placement; (C) close-up of the interconnect to the chip pads; (D) Final FO-WLP. Initial yields are reported to be 97%.

Two PCB test vehicles populated with 60 die each were built for thermal cycle testing. The board level thermal cycle testing was run under -40°C to 125°C. None of the die showed more than 0.2 ohm change in average resistance. ◀

Packaging



Applied Materials releases selective etch tool

Applied Materials has disclosed commercial availability of new Selectra(TM) selective etch twin-chamber hardware for the company's high-volume manufacturing (HVM) Producer® platform. Using standard fluorine and chlorine gases already used in traditional Reactive Ion Etch (RIE) chambers, this new tool provides atomic-level precision in the selective removal of materials in 3D devices structures increasingly used for the most advanced silicon ICs. The tool is already in use at three customer fabs for finFET logic HVM, and at two memory fab customers, with a total of >350 chambers planned to have been shipped to many customers by the end of 2016.

FIGURE 1 shows a simplified cross-sectional schematic of the Selectra chamber, where the dashed white line indicates some manner of screening functionality so that "Ions are blocked, chemistry passes through" according to the company. In an exclusive interview with Solid State Technology, company representative refused to disclose any hardware details. "We are using typical chemistries that are used in the industry," explained Ajay Bhatnagar, managing director of Selective Removal Products for Applied Materials. "If there are specific new applications needed than we can use new chemistry. We have a lot of IP on how we filter ions and how we allow radicals to combine on the wafer to create selectivity."

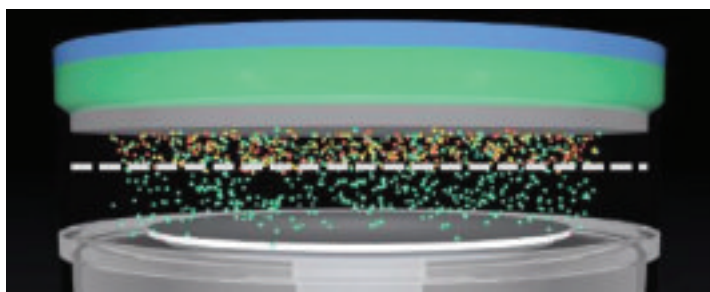
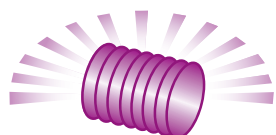


FIGURE 1: Simplified cross-sectional schematic of a silicon wafer being etched by the neutral radicals downstream of the plasma in the Selectra chamber. (Source: Applied Materials)

From first principles we can assume that the ion filtering is accomplished with some manner of electrically-grounded metal screen. This etch technology accomplishes similar process results to Atomic Layer Etch (ALE) systems sold by Lam, while avoiding the need for specialized self-limiting chemistries and the accompanying chamber throughput reductions associated with pulse-purge process recipes.

Semiconductors



"What we are doing is being able to control the amount of radicals coming

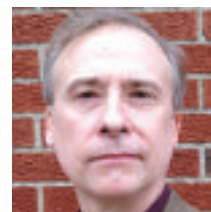
to the wafer surface and controlling the removal rates very uniformly across the wafer surface," asserted Bhatnagar. "If you have this level of atomic control then you don't need the self-limiting capability. Most of our customers are controlling process with time, so we don't need to use self-limiting chemistry." Applied Materials claims that this allows the Selectra tool to have higher relative productivity compared to an ALE tool.

Due to the intrinsic 2D resolutions limits of optical lithography, leading IC fabs now use multi-patterning (MP) litho flows where sacrificial thin-films must be removed to create the final desired layout. Due to litho limits and CMOS device scaling limits, 2D logic transistors are being replaced by 3D finFETs and eventually Gate-All-Around (GAA) horizontal nanowires (NW). Due to dielectric leakage at the atomic scale, 2D NAND memory is being replaced by 3D-NAND stacks. All of these advanced IC fab processes require the removal of atomic-scale materials with extreme selectivity to remaining materials, so the Selectra chamber is expected to be a future work-horse for the industry.

When the industry moves to GAA-NW transistors, alternating layers of Si and SiGe will be grown on the wafer surface, 2D patterned into fins, and then the sacrificial SiGe must be selectively etched to form 3D arrays of NW. The Selectra tools can etch the SiGe from alternating Si/SiGe stacks, with sharp Si corners after etch indicating excellent selectivity.

"One of the fundamental differences between this system and old downstream plasma ashers, is that it was designed to provide extreme selectivity to different materials," said Matt Cogorno, global product manager of Selective Removal Products for Applied Materials. "With this system we can provide silicon to titanium-nitride selectivity at 5000:1, or silicon to silicon-nitride selectivity at 2000:1. This is accomplished with the unique hardware architecture in the chamber combined with how we mix the chemistries. Also, there is no polymer formation in the etch process, so after etching there are no additional processing issues with the need for ashing and/or a wet-etch step to remove polymers."

Systems can also be used to provide dry cleaning and surface-preparation due to the extreme selectivity and damage-free material removal. "You can control the removal rates," explained Cogorno. "You don't have ions on the wafer, but you can modulate the number of radicals coming down." For HVM of ICs with atomic-scale device structures, this new tool can widen process windows and reduce costs compared to both dry RIE and wet etching. ◀



ED KORCZYNSKI,
Sr. Technical Editor

ONYX: A New In-Line and Non-Destructive Hybrid Technology

By **BENNY DONNER, RONI PERETZ** and **BRAD LAWRENCE**, XwinSys, Israel

XwinSys has recently launched the 'ONYX' - a novel in-line and non-destructive hybrid metrology system, uniquely integrating advanced XRF, 2D and 3D optical technologies, designed to meet the current and future metrological challenges of the semiconductor industry.



FIGURE 1: The ONYX System

This is the case where the whole is greater than the sum of its parts - the three integrated optical sensors creates an innovative synergistic approach to problem solving and product monitoring. This was only possible with off-line analytical tools in the past. By integrating components outputs, full scaled inspection parameters can be obtained.

The unique hybrid configuration of the ONYX enables a solution to challenging applications through various analytical approaches and effective SW algorithms:

- Metal film stacks thickness measurements
- Feature dimensions measuring
- Detection and analysis of voids or missing layers
- XRF thickness standards verification
- Detecting specific miss-processing out of a multi-variable metrology application
- Algorithm compensation for parameter variations of a film stack

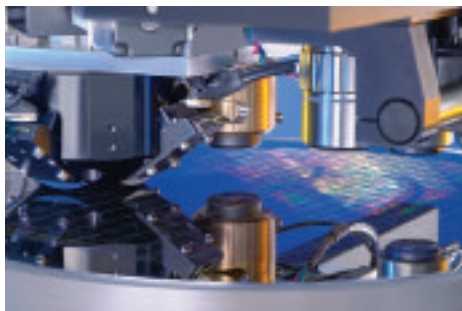


FIGURE 2: Hybrid Configuration

The ONYX's unique triple-mode technologies and capabilities, designed to meet both fast in-line and in-depth metrology challenges, without interrupting the process flow. Enabling several physical parameters to be measured across the wafer, wafer to wafer, and lot to lot - ensures the process is in control. The ONYX is dedicated and designed to serve multiple in-line and non-destructive metrology and inspection needs in the semiconductor and related micro-electronics industries.

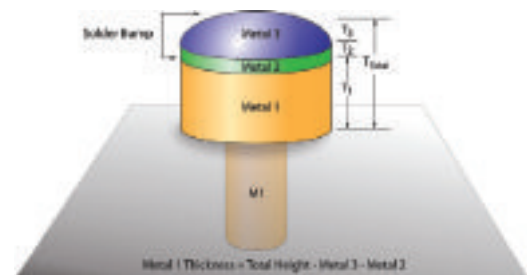


FIGURE 3: Multi-Stack Application

XwinSys Technology Development Ltd.

Website: www.xwinsys.com

Email: info@xwinsys.com

Phone: +972-4-9891313

XwinSys is dedicated to the design, manufacture and marketing of novel solutions based on improved X-ray technology combined with automated optical 3D & 2D microscopes, for the Semiconductor and related industries.

Visit us at SEMICON WEST: booth 2245

DOWNLOAD THE COMPLETE TECHNICAL PAPER NOW!

Ophiuchus

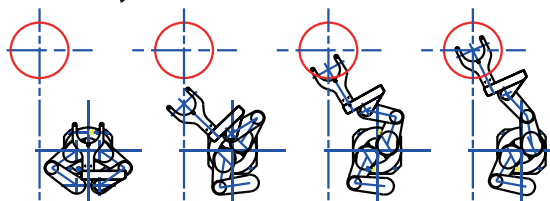
Equipment Front End Module

OPS-2300 Series



OPS-2300 2 FOUF EFEM

Cylindrical Linear Motion

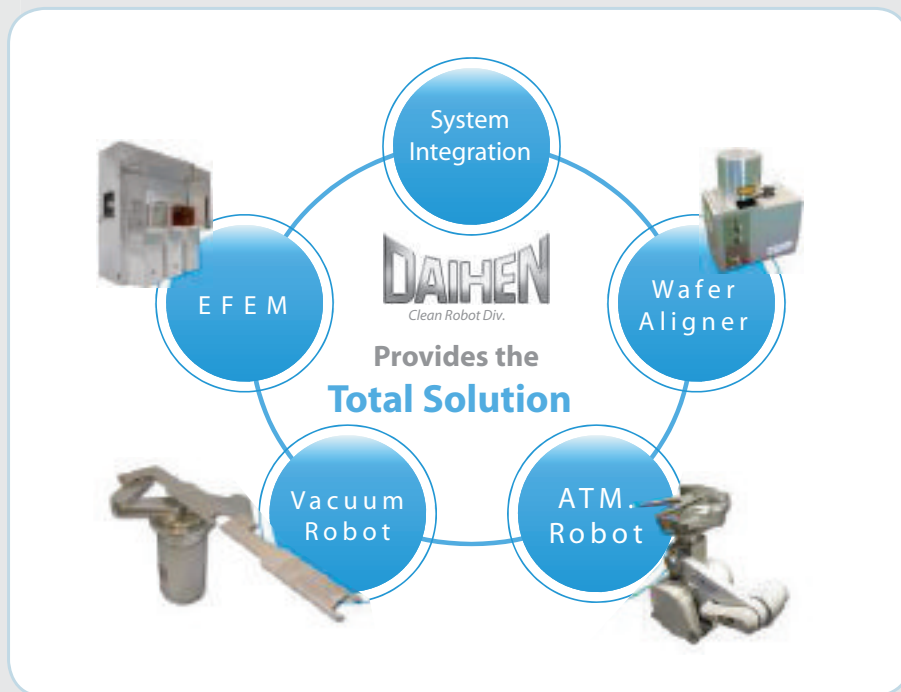
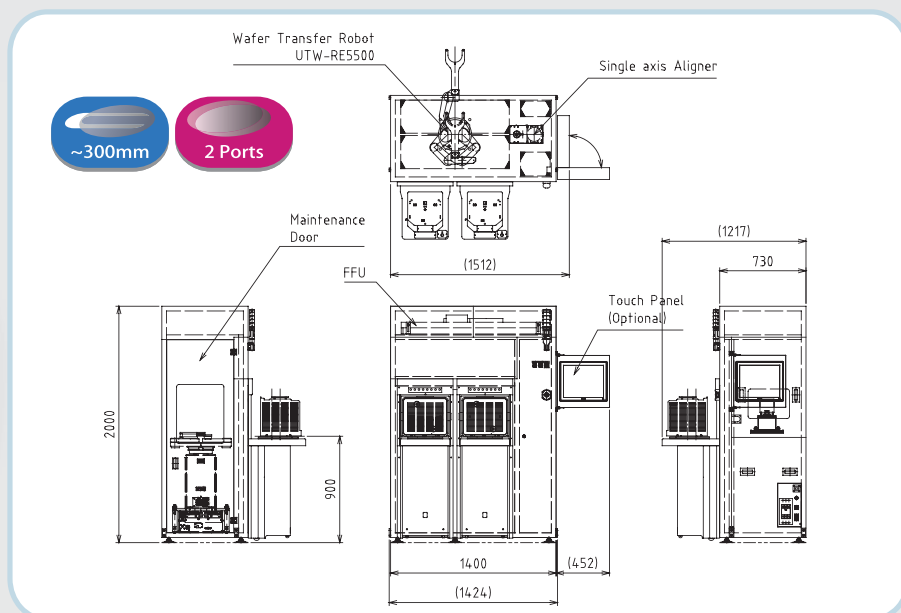


Cylindrical Linear Motion

allows Trackless Two FOUF access.

Cooperative control between robot and single-axis aligner.

Various options to meet customer's requirements.



ACTRANS
DAIHEN CLEAN ROBOT

Visit us at booth 517 during
SEMICON West 2016
Mention promo code DAC-SW16
to receive a special gift

DAIHEN Advanced Component, Inc.

1223 East Arques Ave, Sunnyvale, CA 94085

Tel: +1 408 736 2000

Fax: +1 408 736 2010

E-mail: info@daihen-ac.com

Website: www.daihen-ac.com



Evolution of across-wafer uniformity control in plasma etch

STEPHEN HWANG and **KEREN KANARIK**, Lam Research Corporation, Fremont, CA

A look at control of process uniformity across the wafer during plasma etch processes.

Controlling process variability to achieve repeatable results has always been important for meeting yield and device performance requirements. With every advance in technology and change in design rule, tighter process controls are needed. In all of these cases, there are multiple sources of variability, often generalized as: within die, across wafer, wafer to wafer, and chamber to chamber. Typically, less than one third of the overall variation is allowed for variation across the wafer. For example, at the 14 nm node, the allowable variation for gate critical dimensions (CDs) is less than 2.4 nm, of which only about 0.84 nm is allowed for variation across the wafer [1]. At the 5 nm node, the allowable variation across the wafer may be less than 0.5 nm, or equivalent to two or three silicon atoms. In this article, we will discuss control of process uniformity across the wafer during plasma etch processes, its evolution in the industry, and some key focus areas.

A fundamental challenge in controlling uniformity in etch processes is the complexity of a plasma. Achieving the desired etch result (e.g., post-etch profile with selectivity to different film materials) requires managing the ratio of different ions and neutrals (e.g., Ar^+ , C_4F_8^+ , C_4F_6^+ , O , O_2^+). Since the same plasma generates both types of species, the relative amount of ions to neutrals is strongly coupled. As a result, the impact of parameters typically used to control the plasma (e.g., source power and chamber pressure) are also interdependent.

Improving uniformity through design

Since the start of single-wafer processing in the early 1980s, etch chambers have been designed to produce similar plasma conditions on every location on the wafer to achieve uniform process results. This is especially challenging since there can be inherent electrical and chemical discontinu-

ities at the edge (**FIGURE 1**) that affect uniformity across the wafer. Voltage gradients are created at the wafer edge due to the change from a biased surface to a grounded or floating surface. This bends the plasma sheath at the wafer edge, which changes the trajectory of ions relative to the wafer. The chemical potential discontinuity is analogous and produces concentration gradients for different species

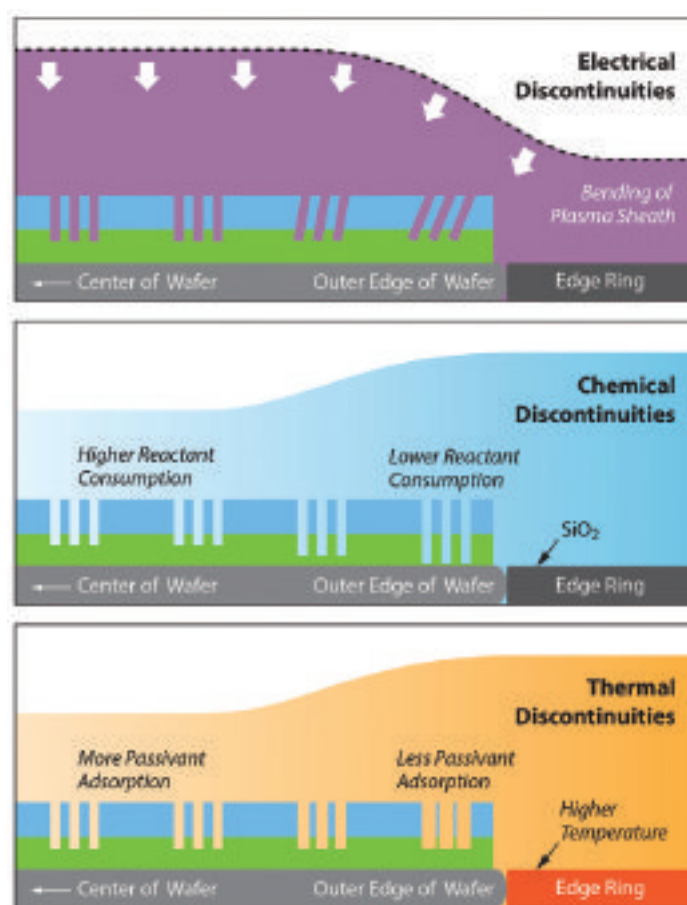


FIGURE 1. Discontinuities caused by the wafer edge create gradients that impact uniformity across the surface, with a significant impact at the edge.

STEPHEN HWANG is technical director and **KEREN KANARIK** is senior technical director, Lam Research Corporation, Fremont, CA

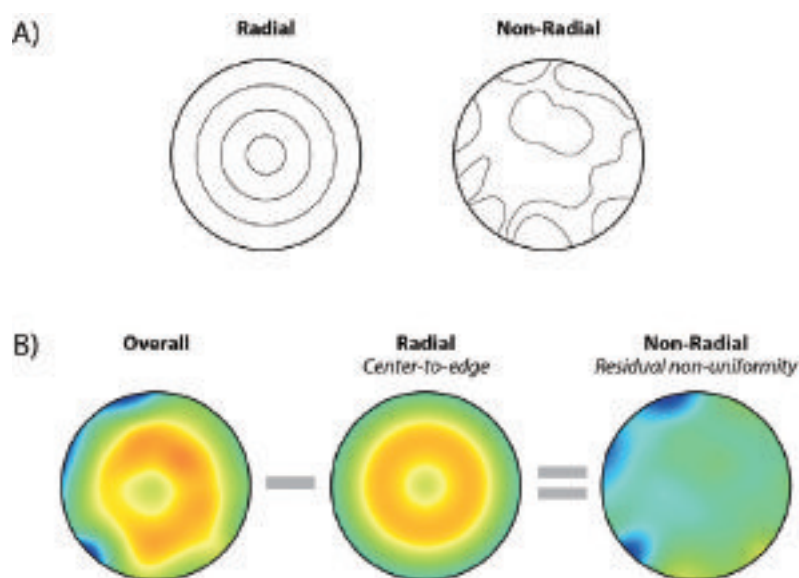


FIGURE 2. Process non-uniformity has both radial and non-radial components (A). On a wafer map showing overall non-uniformity, removal of radial asymmetry allows isolating the more challenging non-radial component (B).

across the wafer. The gradients are caused by multiple phenomena, including variation in reactant consumption and by-products emissions rates at the center relative to the edge, as well as differences in temperature between the chamber and wafer that cause different absorption rates of chemical species.

Many chamber design changes have been implemented over the years to improve radial symmetry (**FIGURE 2a**). For example, a key hardware parameter for capacitively coupled plasma (CCP) chambers is the gap between the cathode and anode. Historically, the gap would be designed to provide the most uniform etch for a given power, pressure, and mixture of gas chemistries. On inductively coupled plasma (ICP) chambers, the gas injection location was a key design feature that would vary by process. In aluminum etch chambers, the reactant gas was delivered from a showerhead above the wafer. For silicon etch, the reactant gases

PFEIFFER  **VACUUM**



A4 SERIES

Energy efficient dry multi-stage Roots process pumps for all semiconductor applications

- Low energy consumption
- Improved temperature management to optimize the pump according to your process
- Protection of the pump against precursor cracking or condensable deposition
- Corrosion resistant and high particle tolerance
- Extended monitoring functionalities

Are you looking for a perfect vacuum solution? Please contact us:

Pfeiffer Vacuum, Inc. · USA · T 800-248-8254 · F 603-578-6550 · contact@pfeiffer-vacuum.com
www.pfeiffer-vacuum.com

VISIT US AT SEMICON WEST BOOTH #1716



were injected from around the perimeter of the wafer, but then evolved so that the gas was injected from above the center of the wafer.

With continuous optimization of chamber design, non-radial patterns became more apparent. On a uniformity map, the average of all the points within every radius can be taken and subtracted from the map, which leaves the more difficult asymmetric portion (**FIGURE 2b**). With this awareness, focus shifted toward eliminating asymmetries in the chamber design.

In retrospect, some of these improvements seem obvious. For instance, up to the late 1990s, it was not uncommon to have etch chambers with the turbomolecular pump located to the side of the wafer. This design created a side-to-side pattern due to the convective flow of reactants and by-products laterally across the wafer. By moving the pumps under the wafer, the flow became radially symmetric, thereby eliminating the process asymmetry.

In other cases, the source of asymmetry was more subtle. One interesting non-uniformity corrected with design was a problematic side-to-side pattern on the wafer that had a seemingly random orientation chamber-to-chamber. After extensive investigation to eliminate possible sources in the chamber hardware, the pattern was correlated with the Earth's magnetic field (**FIGURE 3**). This example demonstrates the sensitivity of plasma processes, even to minor external influences. Although not specifically a

chamber issue, the problem was corrected by applying special shielding with high magnetic-permeability materials around the chamber.

Development of process tuning capabilities

As etch processes became more varied and complex, fixed chamber designs were not sufficiently flexible to meet increasingly stringent requirements since it was not practical to provide a specific uniformity kit optimized for each etch process. Moreover, it was more challenging to achieve uniform results when etch technology transitioned from processing 200 mm to 300 mm wafers in the early 2000s. As a result, tuning capabilities were developed to deliver the uniformity control needed for a wide range of processes and larger wafer sizes.

By the early 2000s, the first uniformity tuning knobs focused on controlling the chemistry over the wafer. This was done in several ways, for example by splitting the main reactant gases into different locations or by adding tuning gases at separate locations from the main reactant gas. Since then, a number of tunable parameters have been identified for etch processes (**Table 1**). Ideally, orthogonal (independent) tuning knobs are used in order to match compensation as closely as possible to root causes. This provides the greatest impact on the process while limiting impact on other parameters. For example, in many dielectric etch processes, the etch rate is limited by the flux of ions from the plasma. Since gas injection doesn't significantly impact plasma density uniformity, Lam Research developed tunable gap technology for CCP chambers to achieve uniform flux of ions across the wafer for a given set of process conditions.

Over the years, continued development has focused on increasing the spatial resolution for better control across the wafer. For example, gas was at first only injected from the center location above the wafer. Then, additional capability was added that allowed controlling the ratio

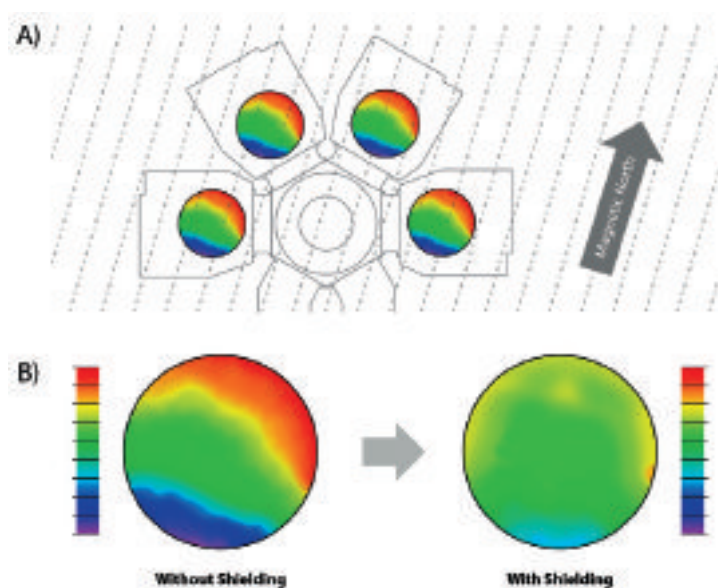


FIGURE 3. Non-uniformity induced by the Earth's magnetic field was identified in an etch process (A). Applying magnetic shielding corrected the problem and provided uniform etch results (B).

Tunable Parameter	Process Parameters Impacted
Inner/outer inductive current (ICP)	<ul style="list-style-type: none"> Neutral density Ion density
Capacitive gap (CCP)	<ul style="list-style-type: none"> Neutral density Ion density
Gas injection location	<ul style="list-style-type: none"> Chemistry control Convective transport
Wafer temperature (radial)	<ul style="list-style-type: none"> Reactant and by-product absorption
Chamber/edge temperature	<ul style="list-style-type: none"> Reactant and by-product absorption

TABLE 1. Tunable Etch Parameters

of gas directed to the center or edge of the wafer. Several years later, an additional gas injection location was added around the periphery of the wafer. To use wafer temperature as a control knob, different heating or cooling zones can be added to an electrostatic chuck (ESC), which holds the wafer. Historically, the number of temperature zones has increased from one to two (by 2002) to four radial zones (by 2006) to improve the radial uniformity of CDs. Since temperature directly affects CD uniformity (CDU), this is an effective way to tackle one of the most critical uniformity challenges.

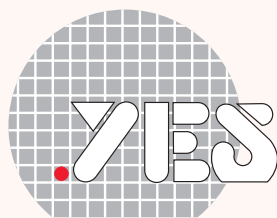
Some of the most complex process flows today rely on these sophisticated tuning capabilities. Innovations that drive continuous scaling, such as 3D FinFET devices, advanced memory schemes, and double/quadruple patterning techniques, add to the challenge of reducing variability due to the increasing number of steps within the integration flows. Even if the uniformity for individual

unit processes (including etch) are relatively good, their combined impact can be significant, and there is need to compensate somewhere in the flow.

When the uniformity profile of a step in the sequence, upstream or downstream, is known and difficult to correct, the profile of an etch step can be modified. For example, if one step is center fast, etch can compensate by being edge fast. This may sound simple, but it is actually quite difficult to achieve the level of process control that can essentially provide a mirror image of the non-uniformity in another process. Fortunately, plasma etch is one process that has matured to being capable of this level of control.

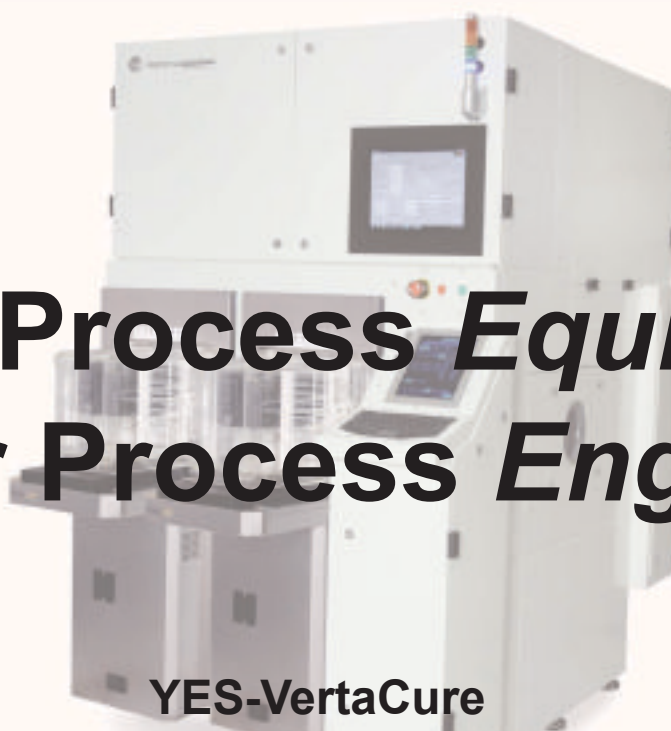
Uniformity control today

After many years of innovation, uniformity control capabilities now have the following characteristics:



Yield Engineering Systems, Inc.

Quality Process *Equipment*, Built for Process *Engineers*.



YES-VertaCure

Designed for wafer-level packaging (WLP),
fan-out wafer level packaging (FOWLP) and Redistribution layers (RDL).

Visit YES @ SEMICON West - South Hall, Booth 1610
www.yieldengineering.com

- A high degree of granularity (numerous independent tuning locations across the wafer)
- Active tuning of both radial and non-radial patterns
- The ability to compensate for non-uniformities upstream and downstream of the etch process

One strategy being used at Lam to achieve the degree of control now needed is providing numerous independent heaters or micro-zones to control the wafer temperature, which is a critical parameter impacting CD uniformity. For example, using more than 100 localized heaters on one etch chamber delivers significantly higher spatial resolution than a system using only two or four heater zones for the entire wafer. Control of numerous individual heaters tunes both radial and non-radial patterns, whereas only center-middle-edge tuning was possible in previous generations (**FIGURE 4**).

With such high granularity, it is challenging for an individual engineer to manually determine the appropriate settings for so many heaters that will achieve a target thermal pattern across the wafer. To address this issue, advanced algorithms and controls with special temperature calibrations were developed so that the system automatically controls the heaters. Moreover, it can be difficult to determine the thermal map profile that will achieve the required process uniformity. Sophisticated software algorithms have also been developed to use process trends, chamber calibration data, and wafer

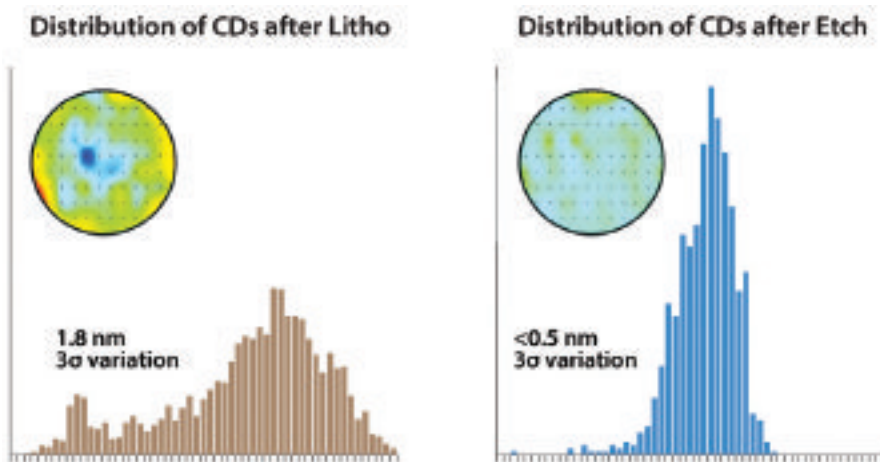


FIGURE 5. Proprietary hardware and software map incoming CDs and adjust etch process conditions in the numerous micro-zones across the wafer to compensate for variability from upstream processes.

metrology information to automatically create the appropriate thermal maps. With this capability, incoming non-uniformity can be reduced to less than 0.5 nm CDU after etch (**FIGURE 5**).

Future focus areas

Beyond the uniformity challenges discussed, performance at the edge of the wafer – the outer 10 mm, where up to 10% of the die may be located – is an increasingly important area of future focus for improving yield. In this region, uniformity control is dominated by the electrical discontinuities at the edge of the wafer that can cause sheath bending. The impacted region of sheath bending is much smaller (~10-15 mm from the edge) compared to chemical or thermal effects (50-70 or 30-50 mm, respectively). While fixed edge hardware can be redesigned for optimal uniformity, new technologies are in development to provide in situ tunability of the sheath at the wafer edge.

Looking ahead, we can expect more types of control knobs and further granularity for finer tuning along with a greater focus on automation. Compensatory process control should continue to develop and be used as process modules become increasingly complex.

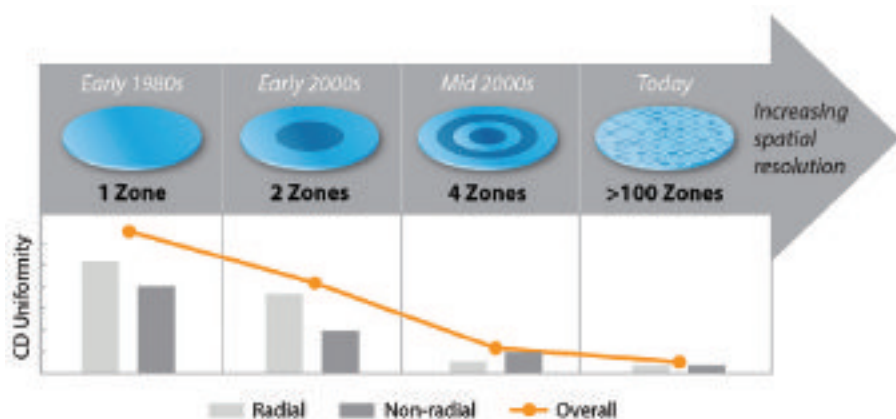


FIGURE 4. Active uniformity control has evolved from limited radial tuning of large areas of the wafer to independent tuning of ever smaller regions across the wafer, enabling control of both radial and non-radial uniformity.

REFERENCES

1. ITRS 2013: Table FEP 12 Etch Process Technology Requirements ◀

We create the future of **Motion Systems** - from top to bottom

Come see us at

**SEMICON
WEST**

HEIDENHAIN BOOTH #1809

ETEL BOOTH #1909

ADVANCED MOTION PLATFORM

addressing your most stringent requirements down to sub-nanometer levels.

ACTIVE ISOLATION SYSTEM

cancelling more than 99% of the vibration enabling unprecedented performance.

MOTION CONTROL

providing sub-nanometer stability, high acceleration as well as very short move and settle time.



ETEL is 100% dedicated to direct drive technology. Our wide range of linear and torque motors, position and motion controllers and high-end motion system products provides a portfolio to meet your needs. The key process improvements you have been looking for are now available.

www.heidenhain.us/etel

Fan-Out Wafer Level Packaging: Breakthrough advantages and surmountable challenges

DAVID BUTLER, SPTS Technologies, an Orbotech company, Hereford, UK

New wafer processing technologies overcome FOWLP's technical hurdles, paving the way for a new generation of ultra compact, high I/O electronic devices

Our ability to create ever-smaller electronic devices that maintain or surpass the performance of their physically larger predecessors – exemplified by today's wearables, smartphones and tablets – is dictated by many factors that extend well beyond Moore's Law, from the underlying embedded components to the ways in which they're packaged together. With regard to the latter, fan-out wafer level packaging (FOWLP) is quickly emerging as the new die and wafer level packaging technique of choice, and is widely anticipated to underpin the next generation of compact, high performance electronic devices.

Whereas with conventional flip-chip WLP schemes the I/O terminals are spread over the chip surface area, limiting the number of I/O connections, FOWLP embeds individual die in an epoxy mold compound (EMC) with space allocated between each die for additional I/O connection points, avoiding the use of more expensive silicon real estate to accommodate a higher I/O count. Redistribution layers (RDLs) are formed using physical vapor deposition (PVD) and subsequent electroplating and patterning to re-route I/O connections on the die to the mold compound regions on the periphery (**FIGURE 1**).

Leveraging FOWLP, semiconductor devices with thousands of I/O points can be seamlessly connected via finely-spaced lines as thin as two to five microns, maximizing interconnect density while enabling high bandwidth data transfer. Significant height and cost savings are achieved via the elimination of the substrate.

With FOWLP today we have the ability to embed heterogeneous devices including baseband

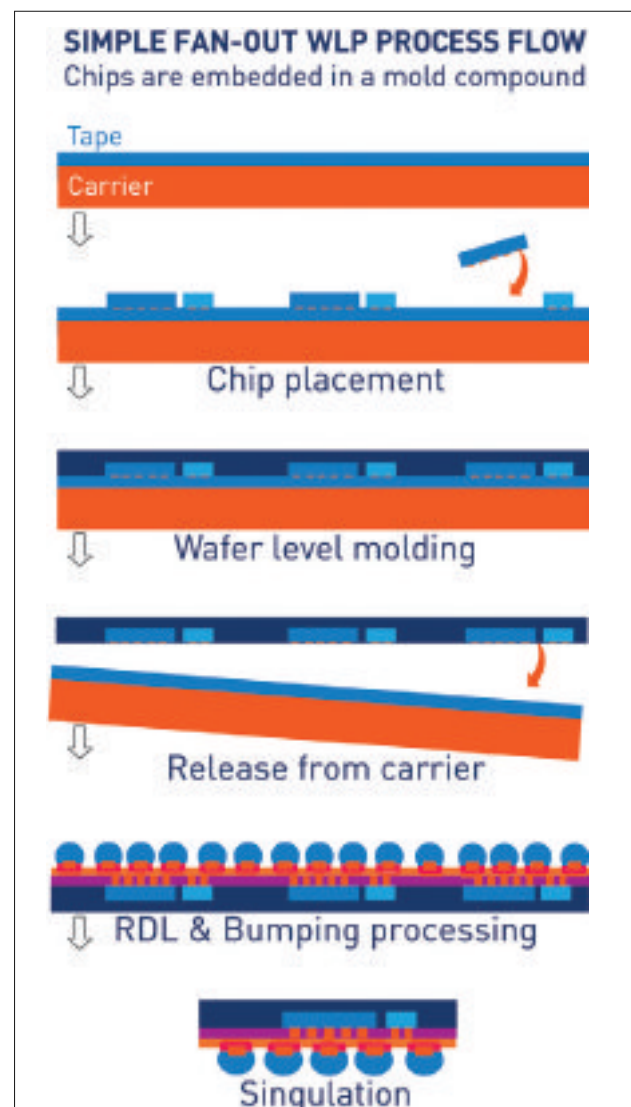


FIGURE 1. FOWLP process flow.

DAVID BUTLER is Vice President of Product Management and Marketing, SPTS Technologies, an Orbotech company, Hereford, UK.

processors, RF transceivers and power management ICs in these mold wafers, thereby enabling the latest generation of ultra-thin wearables and mobile wireless devices. With continued line and space reductions, FOWLP has the potential to accommodate higher performing devices including memory and application processors, positioning FOWLP to extend into new markets including automotive and medical applications and beyond.

Leading vendors implementing FOWLP today include Amkor, ASE, Freescale, NANIUM, STATS ChipPAC, and TSMC, with TSMC being the most high-profile vendor given its widely-reported contract win to produce A10 processors for Apple's iPhone 7 – a deal said to be attributable in part to TSMC's mature FOWLP-based InFO technology.

According to a report entitled "FO WLP Forecast update 09/2015" published by research firm Yole Développement in September 2015, the launch of TSMC's InFO format is expected to increase industry packaging revenues for FOWLP from \$240M in 2015 to \$2.4B in 2020. With a projected 54% CAGR, Yole expects FOWLP to be the fastest growing advanced packaging technology in the semiconductor industry.

Low heat, high speed processing

All fan-out wafers feature singulated die embedded in the EMC, with spin-on dielectrics surrounding the RDL. These materials present some unique challenges, including moisture absorption, excessive outgassing and a limited tolerance to elevated temperatures. If not dealt with properly, contamination at the metal deposition stage can compromise contact resistance.

Whereas conventional circuits built on silicon can withstand heat up to 400°C and can be degassed in under one minute, the EMC and dielectrics used in FOWLP have a heat tolerance closer to 120°C. Temperatures exceeding this low threshold can cause decomposition and excessive wafer warping. Degassing wafers at such low temperatures naturally takes a longer amount of time, and can drastically reduce the throughput of a conventional sputter system.

Multi-wafer degas (MWD) technology has emerged as a compelling solution to this problem, enabling up to 75 wafers to be degassed at 120°C in parallel before being individually transferred to subsequent pre-clean and sputter deposition, without breaking vacuum.

With this approach, wafers are dynamically pumped under clean, high vacuum conditions, with radiation heat transfer warming wafers directly to temperatures within the operating budget for packaging applications.

Each wafer can spend up to 30 minutes inside the MWD, but because they're processed in parallel, a "dry" wafer is outputted for metal deposition every 60 to 90 seconds, at a rate of between 30 to 50 wafers per hour. This approach increases PVD system throughput by 2-3 times compared to a single wafer degas processing technology, and as materials emerge with even lower thermal budgets based on increased passivation thickness, longer degas times can be accommodated with no impact on throughput (**FIGURE 2**).

These benefits are not readily attainable, however, unless we can overcome the attendant warping challenges. Epoxy

NEW Plasma resistant O-ring material

- Avoid over-specification
- Reduce cost of consumables
- Reduce particulation

Utilizing the latest polymer and compounding technology, PPE has developed a new cost-effective, low particulate, low erosion elastomer material as shown by independent benchmarking against the leading brands in common plasma process chemistries.

► Discover more at SEMICON WEST, booth #1345 South

SEMICON
WEST

July 12 – 14, 2016
Moscone Centre
San Francisco, CA

PPE
Precision Polymer Engineering

mold wafers can be warped after curing, and the size and shape of the warpage hinge on the different shapes, densities and placement of the embedded die. A FOWLP PVD system must therefore be able to minimize temperature-induced shape shifting, and accommodate wafers with up to a 10mm bow. The acceptable industry threshold for bowing is probably lower than 6mm, however, as it's not easy to make uniformly thick conductors on a substrate exhibiting 6mm+ warpage.

Utmost integrity

After successful degas, but prior to metal deposition, the FO wafer is pre-cleaned in a plasma etch module. This facilitates the removal of trace oxide layers from the contacts, but due to the composition of the organic dielectric surrounding the contacts, will result in carbon build-up on the chamber walls. This carbon does not adhere well to ceramic chamber surfaces, and if not carefully managed, can result in early particle failure.

New in-situ paste technologies allow these carbon deposits to better adhere to chamber surfaces during the pre-cleaning process, enabling preventative maintenance intervals that exceed 6,000 wafers. This approach can significantly improve productivity by reducing the frequency of dedicated wafer pastes, which typically require production to be paused every 10 to 20 wafers for chamber pasting when using conventional techniques.

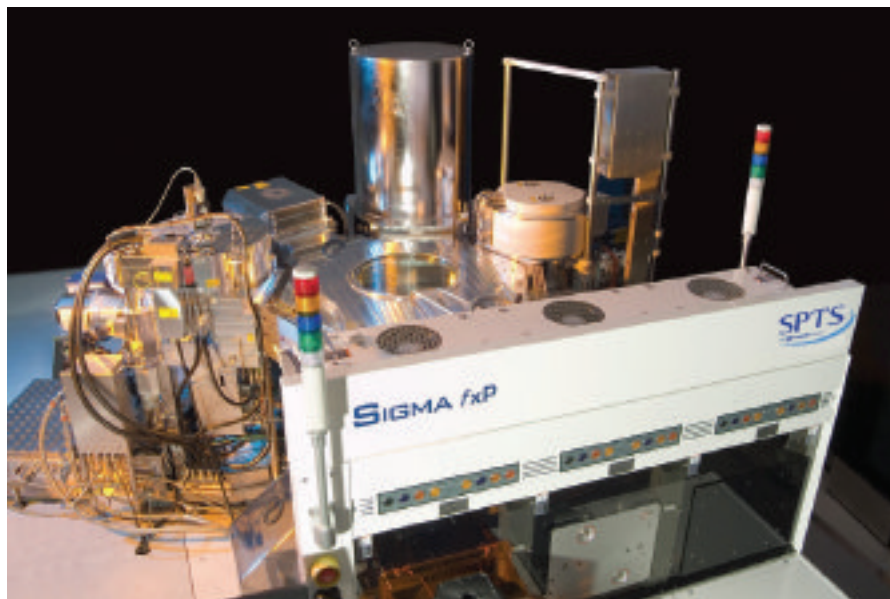


FIGURE 2. The Sigma® fxP PVD system with multi-wafer degas module from Orbotech-SPTS.

The myriad benefits that FOWLP promises for the production of ultra compact, high I/O electronic devices far outweigh the aforementioned technical barriers to mainstream FOWLP adoption. With the ability to overcome the degassing, warping, and integrity challenges that can impede FOWLP implementations, electronics manufacturers can unlock the full potential of FOWLP while eliminating frictions affecting production speeds and yields. ◀

CONNECT

Connect to the Global Semiconductor Supply Chain at SEMICON Taiwan

The Taiwan equipment and materials market is expected to remain the largest in the world, reaching more than US\$17 million in 2016. Connect to this exciting and dynamic market at SEMICON Taiwan, the most influential annual event serving the microelectronics supply chain in Taiwan. SEMICON Taiwan brings together leading international companies from across the region and around the world, with more than 700 international exhibitors, more than 1,600 booths, and more than 43,000 attendees expected making it the must-attend event of the year!

Explore Latest Trends and Emerging Markets

- AOI Pavilion
- High Tech Facility Pavilion
- Materials Pavilion
- Secondary Market Pavilion
- Taiwan Localization Pavilion
- CMP Pavilion
- Laser Pavilion
- Precision Machinery Pavilion
- Smart Manufacturing Pavilion

Expand Professional Network at Diverse Events and Activities

- International Program
- Leadership Gala Dinner
- Supplier Search Program
- TechXPOT



Co-located

SIP GLOBAL SUMMIT 2016

Follow us on Facebook



Register Online for FREE
www.semicontaiwan.org

Extending tungsten metallization for next-generation devices

JONATHAN BAKKE, Applied Materials, Santa Clara, CA

Recent breakthroughs in materials engineering of low-resistance W barriers/liners and bulk fill are making it possible to extend W use to next-generation devices.

Tungsten (W), with its low resistivity and minimal electro-migration, has long been used for a variety of applications in fabricating semiconductor devices. For instance, it is used for logic contact, local interconnect (LIC), and metal gate (MG) fill as well as DRAM buried word line and contact and 3D NAND MG and contact. Sustained scaling, however, is posing challenges to its continued use with conventional process flows. Interconnect dimensions have shrunk to the point at which contact resistance is becoming an obstacle to realizing optimum transistor performance; fill integrity degrades as aspect ratios and the degree of re-entrance increase, making it difficult to ensure high-quality metallization.

At earlier nodes, larger dimensions made W fill possible using conformal CVD deposition. Now, overhang around

the tops of ultra-small openings or bowing from the interconnect etch open preclude the conformal process from completely filling features without voids, while center seams are an inevitable result of conformal deposition, even in the absence of voids. These attributes render extremely small features vulnerable to breach during CMP, causing high resistance or complete failure of an interconnect. High feature densities and lack of via redundancy in advanced chip designs mean that a single void can cause complete device failure and significant yield loss.

Fortunately, recent breakthroughs in materials engineering of low-resistance W barriers/liners and bulk fill are overcoming these limitations and making it possible to extend W use to next-generation devices. The former lower resistance by simplifying fill film requirements and enlarging the volume available for W fill; the latter eliminates undesirable seams to create more robust structures.

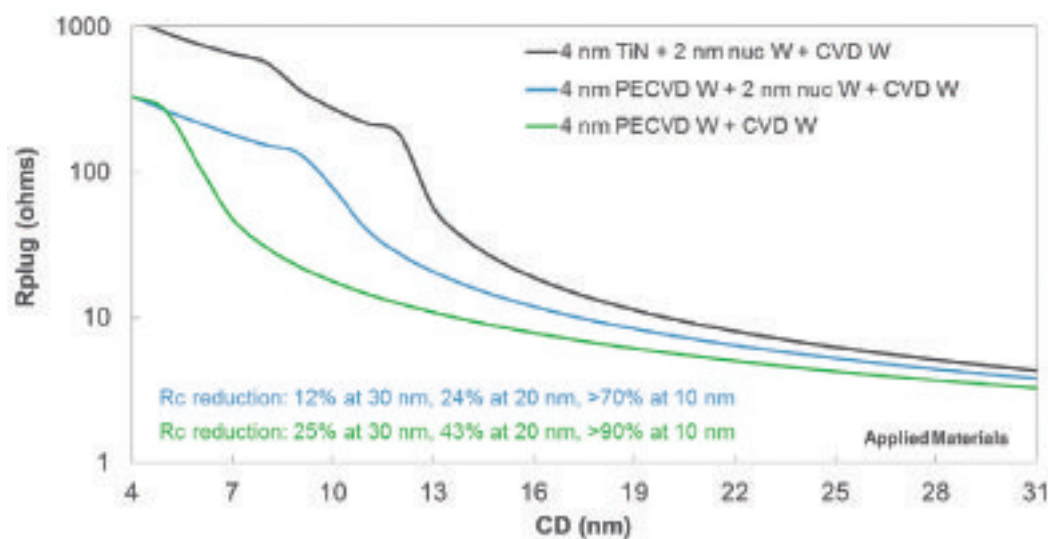


FIGURE 1. Plug resistance simulation demonstrates the significant benefit of PECVD W without a nucleation layer.

Low-resistance liners

To date, high-resistivity TiN has been predominantly used as an adhesion layer for CVD W and to block fluorine penetration during the bulk fill process. W does not grow directly on TiN; thus, it requires deposition of a nucleation layer before the fill step. As logic devices scale through the 10 nm node and beyond, the maximum critical dimension (CD) of the LIC will be <25 nm. This leaves <12 nm for low-resistance W fill after the relatively high-resistance TiN and

JONATHAN BAKKE is global product manager for Contact and Middle of Line Products in the Metal Deposition Products Business Unit of Applied Materials, Santa Clara, CA.

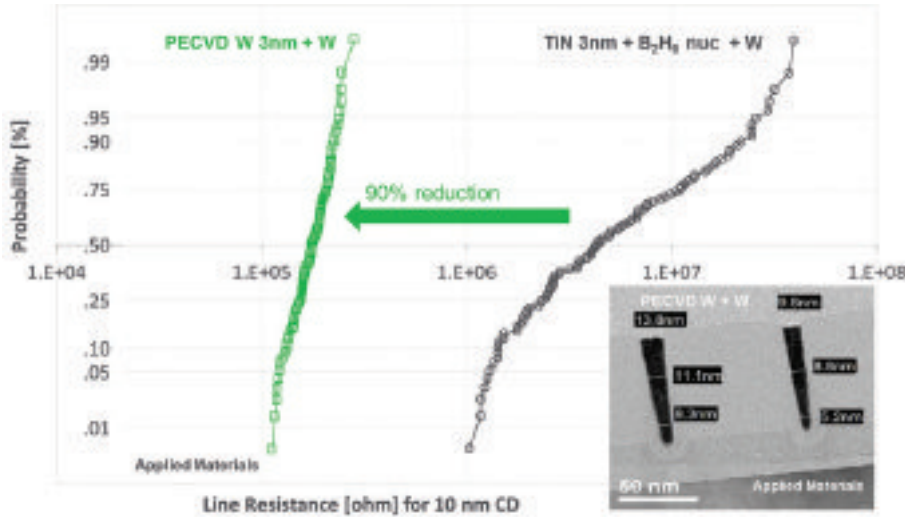


FIGURE 2. PECVD W plus gap fill reduces line resistance by nearly 90% over the conventional stack. The inset TEM shows conformal gap fill and CMP integration for PECVD W.

Metal-organic deposition of thin W-based films offers an ideal solution, because it can eliminate high-resistance liners and nucleation layers while maintaining adhesion and fluorine-barrier properties equivalent to those of the current process flow. A new W liner has been developed that lowers line resistance for further device scaling: plasma-enhanced (PE) CVD W that nucleates on metal and oxides.

The PECVD W film is produced using a specialized chemical in the presence of reactive plasma that breaks down the ligands. The film composition is primarily

W, and the atoms from the decomposed ligands are bonded to the W. The amorphous character of the film and the dopants in it from the ligand lead to good adhesion to dielectrics and fluorine barrier properties in the 20-30Å range.

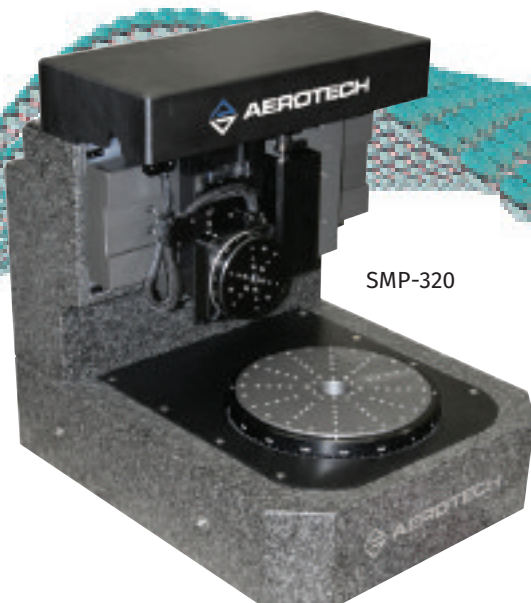
W, and the atoms from the decomposed ligands are bonded to the W. The amorphous character of the film and the dopants in it from the ligand lead to good adhesion to dielectrics and fluorine barrier properties in the 20-30Å range.

FIGURE 1 shows a simulation of a contact plug in the 4-30nm range. The model contains parallel and series resistors for the plug and through resistance. Features

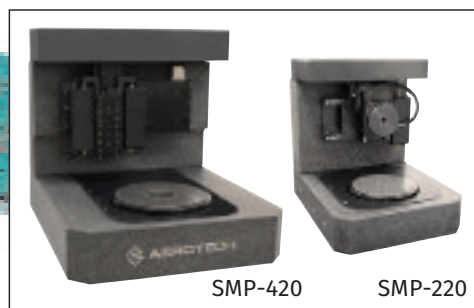
Optimize Your Surface Measurement and Inspection Motion

Save 40% Measurement Time and 60% Footprint

Traditional Cartesian systems require frequent, time-consuming motion reversals in X and Y to raster-scan a part, which necessitates longer travel ranges to account for inefficiencies in constantly starting and stopping. The vastly superior SMP design utilizes an industry-leading rotational motion profile to deliver smooth, continuous scanning of the part, with no starts and stops, resulting in significantly reduced measurement time and machine footprint.

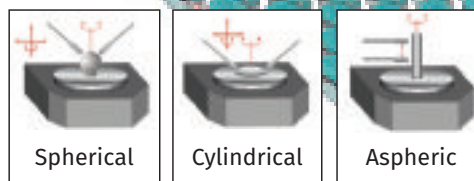


SMP-320



SMP-420

SMP-220



Spherical

Cylindrical

Aspheric

- Reduce measurement time by 40% compared to Cartesian systems
- Minimize footprint by 60% compared to Cartesian systems
- Axis repeatability in the low nanometer range
- Nanometer-level minimum incremental motion (resolution)
- Ultra-smooth motion even at very low velocities
- Easily customizable for customer-specific measurement processes

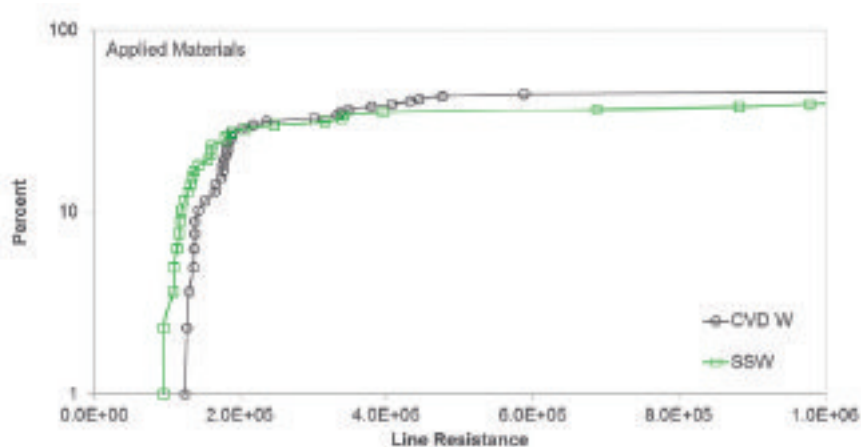


FIGURE 4. Line resistance comparison of SSW and conventional CVD W on 10nm trench.

are assumed to be straight wall trenches. Resistance of $12 \mu\Omega \cdot \text{cm}$ is used for W at all thicknesses, which underestimates the benefit of PECVD W. Scattering at film interfaces is not taken into account. The inflections in the curves (from right to left) occur when a film is removed due to volume constraints. It is clear that the benefit of PECVD W increases exponentially as CDs decrease, especially without the nucleation layer.

SiO₂ trench structures with CDs ranging from 10nm to 150nm and a depth of 100nm were used to investigate W line resistance and evaluate gap-fill performance. As shown in **FIGURE 2**, line resistance in a ~10 nm CD dropped by nearly 90% compared with the conventional stack.

Seam-suppressed gap fill

Until now, feature dimensions have made W fill integration possible using nucleation followed by

conformal CVD deposition – which always leaves a seam in features. At CDs <20 nm, however, the volume of the seam or void can be a significant portion of the W fill volume, effectively increasing resistance and also posing the risk of damage during CMP. With device densities increasing in response to demands for higher performance, the smallest flaw can lead to significant yield loss.

A new approach employs a unique, “selective” suppression mechanism that results in a bottom-up fill free of seams or voids. Pre-treating the nucleation layer creates preferred W growth from the bottom of the structure upwards and less on the field, minimizing the likelihood of void-creating pinch-off and seams (**FIGURE 3**). Experiments showed the process to be successful on structures with CDs ranging from 10nm to 150nm.

Electrical tests confirmed that SSW lowered line resistance compared to that of conventional CVD W (**FIGURE 4**). Post-CMP defect analysis by top-down view SEM revealed a narrow seam in conventional CVD W after W CMP (**FIGURE 5a**), while none is visible after SSW fill (**FIGURE 5b**).

Conclusion

For the next several nodes of logic and memory fabrication, W will remain an important material in interconnect and gate metallization. However, as scaling continues, transitions in process flows will be necessary to achieve low contact and line resistance while maintaining gap-fill integrity. A new W-based barrier/liner has been produced through precision materials engineering that improves device performance and integration while simplifying

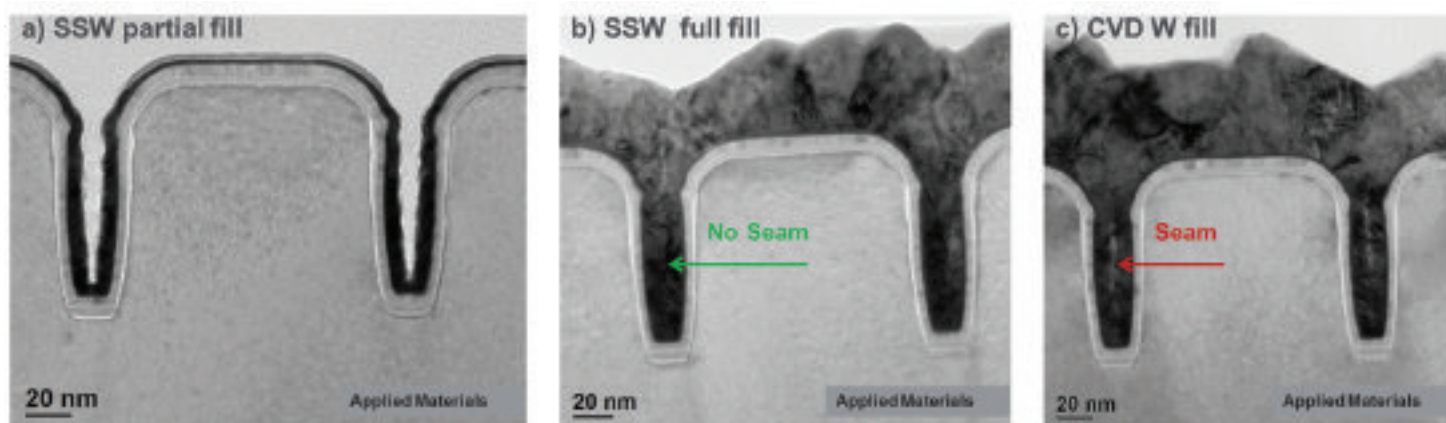


FIGURE 3. a. Cross-sectional TEM image of SSW partial fill of 30nm CD, 100nm deep trench pattern with overhang created by Ar sputter and PVD Ti. (b) TEM image of seamless SSW fill of the same structure. (c) TEM image of standard CVD W gap fill with seam.

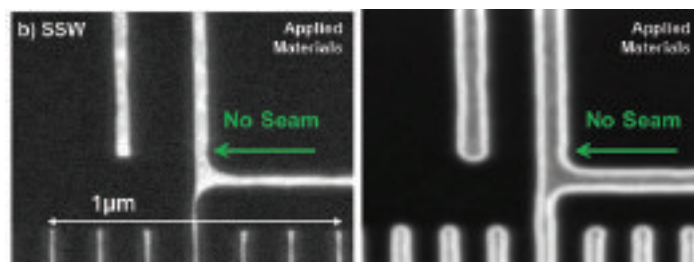
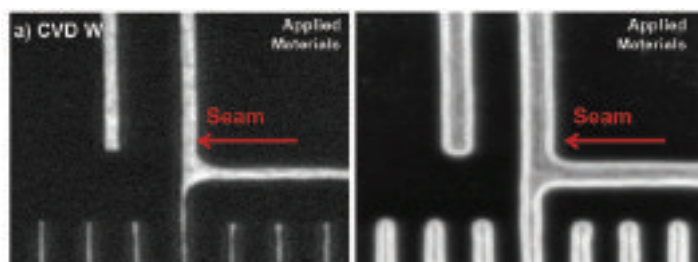


FIGURE 5. Top-down SEM image of a) conventional CVD W process with visible seam in the center of the trench and b) SSW fill on the same structure.

process flows. Similarly, a new SSW gap-fill process increases the volume of W (potentially lowering resistance), creates more robust features for post-fill integration, and relaxes requirements on CMP and dielectric etch steps, thus delivering performance, device design, and yield benefits.

For further detail on the processes presented in this article, see Bakke, J., et al., “Fluorine-Free Tungsten Films as Low Resistance liners for Tungsten Fill Applications” and Kai, W., et al., “Improving Tungsten Gap-Fill for Advance Contact Metallization,” presented at the 2016 IEEE International Interconnect Technology Conference. ◀

Cure Ovens for Dielectric Polymers



*The Equipment You Want
For the Results You Need!*

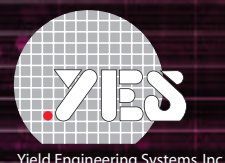
Superior yields with:

- Excellent thermal, electrical and mechanical properties
- Reliable multi-level interconnections
- Proper cross-linking
- No stress
- No cracking or lifting
- **Low cost of ownership/FAST ROI**



YES-VertaCure
YES-PB Series

Visit YES @ SEMICON West - South Hall, Booth 1610
www.yieldengineering.com



Ensuring safety in the sub-fab

ALAN IFOULD and **ANDREW CHAMBERS**, Edwards, North Somerset, UK

Problems frequently arise as a result of an incomplete or absent formal risk assessment when processes are modified or new materials introduced.

The sub-fab is home to the many pumps and abatement systems that not only help to create the pristine environments required in the process chambers of the numerous tools in the cleanroom, but also handle the exhaust gases and by-products generated by the manufacturing process. In this respect, the efficiency and efficacy of sub-fab operations directly affect the availability, productivity, total operating cost and yield of the manufacturing fab above. Perhaps more importantly, in addition to supporting the process vacuum, equipment in the sub-fab is designed to render cleanroom process wastes harmless and ready for safe disposal or, if appropriate, release into the environment. As such, they are vital to protecting the safety of the people working in the fab as well as those living and working in the surrounding community, and ultimately, all of us who share that environment. The very nature of the process materials and reaction byproducts handled in the sub fab, which may be variously corrosive, toxic, pyrophoric, flammable or environmentally damaging, creates significant risks, especially for those who must operate and maintain the equipment located there. Moreover, as device manufacturing becomes more complex, with the introduction of new materials, new precursors and new processes, the risk of mistakes with potentially catastrophic consequences in both human and financial terms will only increase.

While ultimate responsibility for personnel safety in the sub-fab lies with the fab operator, equipment manufacturers have a part to play by optimizing their products not only for efficient, effective and reliable operation, but also by ensuring any risks associated with operation, maintenance and repair are assessed and minimised to the greatest extent possible.

There is often a strong focus on technical performance and cost attributes when selecting sub-fab equipment. However, processes and procedures to ensure optimum operation and continuous mitigation of risks to service

personnel are equally critical; these demand the development of clear and effective operating procedures and guidelines – in industry jargon “best known methods” or BKM – to ensure the equipment achieves its full performance potential and safety integrity maintained. The manufacturers of sub-fab equipment are perhaps in the best position to define these guidelines since they will typically have acquired an understanding of the risks posed by hazardous materials on a case-by-case basis during the course of system optimization. Frequent development of BKM is undertaken in collaboration with the process tool manufacturer or early adopters of the process. However, defining operating and maintenance methods and procedures that are truly the best known requires a commitment to doing so at the highest levels of corporate management, and a formal process of reporting, analysis, synthesis and dissemination throughout the equipment support community.

A key component of any BKM program is the active participation of the equipment manufacturer’s service personnel who are responsible for installing, commissioning and maintaining the equipment and are also likely to have first-hand knowledge and experience of the potential hazards. Since service personnel are invariably in the front-line when safety incidents occur, they are well motivated to contribute since they themselves are often at greatest risk, and it is essential that their contribution is incorporated into product development programs to complement the technical performance with assured safety and reliability.

Even a cursory search of the internet will quickly reveal numerous examples of fab and sub-fab incidents. Amongst the lessons that can be taken from these events is that the risk management process and the resulting controls have to cover every foreseeable circumstance across the equipment lifecycle: installation, commissioning, operation, servicing and maintenance. Notable recent serious accidents include:

ALAN IFOULD is Global Market Sector Manager, Service and **ANDREW CHAMBERS** is Senior Product Manager, Edwards, North Somerset, UK, www.edwardsvacuum.com

Busch Vacuum Solutions for Semiconductor Processes

Visit us at SEMICON West!
booth# 1339 ▶ San Francisco, CA ▶ July 12-14

Reliability · Efficiency · Optimization

Busch COBRA twin screw dry vacuum pumps —
proven for the most demanding semiconductor
process applications. The COBRA value:

- ▶ Reduced facilities costs and compelling
return on investment
- ▶ Intuitive tool communication and monitoring
of pump parameters
- ▶ Increased uptime
- ▶ Small footprint

All Busch products are supported by our global
service support network, located in over 40 countries
throughout the world. We also offer service and
support for the majority of manufacturers' vacuum
products within the FAB.



marketing@buschusa.com | 1-800-USA-PUMP | www.buschusa.com

- March 2014 – A fab worker dies after a carbon dioxide leak
- January 2013 – One worker dies and four others are hospitalized after a hydrofluoric acid leak at a manufacturing facility
- September 2013 – A fire at major memory fab results in the closure of the facility with losses estimated in the range of \$1 billion and a measurable impact on global DRAM pricing
- August 2012 – A security guard and 3 firefighters are hospitalized when a fire occurs in the exhaust ducts of a photovoltaic manufacturing laboratory in Singapore. The entire facility is shut down for weeks and 35 workers are laid off

These were events with consequences visible and far-reaching enough to make the national and international news. However, experience indicates that smaller events, often with narrowly-averted disastrous consequences, occur on a much more frequent basis with adverse impacts on fab productivity. These events are typically not widely broadcast, thereby limiting the community learning that might otherwise take place.

In respect of process exhausts, three types of hazard recur repeatedly as manufacturing processes evolve and new process materials are introduced: condensation of reactive chemical precursors or reaction products, corrosion due to condensation of acidic materials, and pipe blockage due to accumulation of condensate in significant volume. The images in **FIGURES 1-3** show a few examples.

In many cases, the cause of the risk is understood and solutions exist, but problems frequently arise as a result of an incomplete or absent formal risk assessment when processes are modified or new materials introduced. For example, condensation of potentially dangerous or explosive materials can usually be prevented by carefully

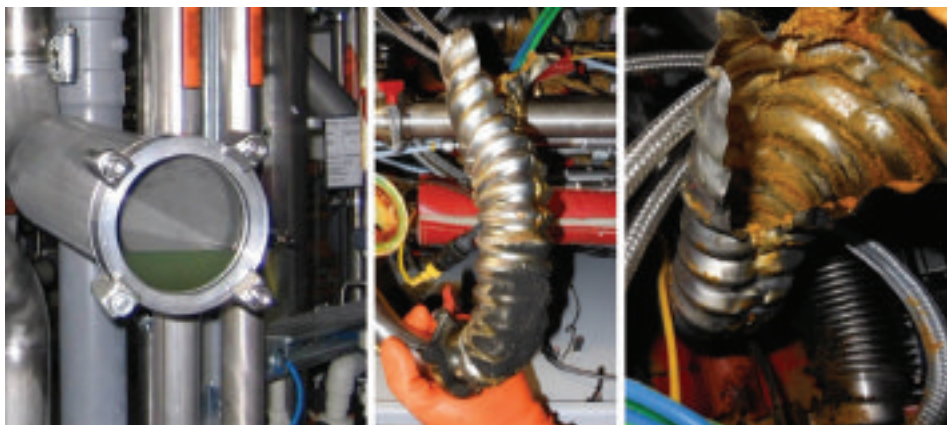


FIGURE 1. (left) Condensed explosive polysiloxane material in an epitaxial deposition system process foreline, (middle and right) CVD exhaust pipe destroyed by explosion of condensed process by-product.



FIGURE 2. (left) Acidic TEOS-based polymer with a pH of approximately 1, (middle) Condensed corrosive Br₂-based liquid, (right) Exhaust pipe damaged by exposure to condensed acidic material.



FIGURE 3. Exhaust blockage caused by various materials (left) AlCl₃ from a metal etch process, (middle) NH₄Cl from an LPCVD process, (right) Unknown material deposited in the exhaust of a metal carbide CVD process.

controlling the temperature of the exhaust gas through the pipework and pumps. Pipe heating systems are widely available for forelines and exhaust pipes, and pumps can be designed with internal thermal management, but if the risk is not properly assessed, the appropriate controls will not be put in place. Furthermore, while a risk analysis

may conclude that exhaust pipe heating is required in a specific case, it should also recognize that key to its effective implementation is the avoidance of cool spots, particularly at bends and junctions. Even a small local drop in temperature can create a hazardous situation despite the application of what is widely perceived as an effective protective measure – a subtle effect, but one with which field service personnel have become familiar through hard-won experience. At a practical level, if each process exhaust is designed in isolation, such considerations make their design and implementation a time-consuming and labor-intensive process. However, as noted in a previous publication [1] the ability to maintain effective thermal control throughout the exhaust stream can be enhanced by integrating the vacuum pumping and point-of-use abatement functions together with the interconnecting exhaust pipes into a single unified system. In this way the pipe routing can be standardized to permit optimization of the exhaust pipe heating installation for each specific process and to avoid the need for customization in the field. Integration and standardization also permits careful optimization of pump capacities and pipe diameters and routing to minimize power consumption and maximize destruction or removal efficiency (DRE). Finally, whether considering an integrated system or not, secondary enclosures for pumps, abatement and exhaust pipes provide an additional layer of protection by permitting hazardous materials to be routed away from personnel in the event of an unintended release.

In some cases, it is not possible to prevent the accumulation of hazardous materials. It then becomes essential to monitor the deposition and remove it through periodic maintenance procedures. For example, blockage can be



THIS IS COST-EFFICIENT

*UHP Metal Face Seal
and Weld Fittings*

*High integrity
enhances reliability*

Parker enables its partners in the semiconductor industry to cost-efficiently maintain valve performance in manifold box, gas cabinet, and tool hookup applications. This reflects Parker's engineering commitment to reducing short- and long-term costs. **Call Parker's Veriflo Division at (510) 235-9590 to learn more or visit solutions.parker.com/semicon**



ENGINEERING YOUR SUCCESS.

©2016 Parker Hannifin Corporation SS-1-1

Severity / Impact	Probability / Likelihood					People: Employees or third parties	Environment	Property, Process, machinery or equipment
	Unlikely But could occur	Possible Occurrences could be minimal	Unlikely Occurrences could happen	Highly Likely Occurrences expected	Certain			
1 Negligible	1	1	2	2	3	First aid only	Chemical spill, release or emission, requiring only minor clean-up and no external reporting	Non-critical equipment or facility damage
2 Moderate	1	1	3	3	4	Medical treatment or restricted work activity (Short term occupational illness)	Chemical spill, release or emission which requires limited worker cleanup and/or external reporting	Minor subsystem loss and/or moderate facility damage
3 Severe	2	2	4	4	5	Lost time or temporary disability. Long term occupational illness	Chemical spill, release or emission requiring major worker clean-up, temporary environmental or public health impact	Major subsystem loss and/or severe facility damage
4 Catastrophic	2	2	4	5	5	Fatality or major disability e.g. loss of limb	Chemical spill, release or emission requiring off-site cleanup or major lasting environmental or public health impact	Complete system loss and/or extensive facility damage

Risk Rating	Action and Timescale
1 Negligible	No action is required and no documentary records need to be kept.
2 Moderate	No additional controls are required. Consideration may be given to a more cost effective solution or improvement that imposes no additional cost burden. Monitoring is required to ensure that the controls are maintained.
3 Severe	Efforts should be made to reduce risk, but the costs of prevention should be carefully measured and limited. Risk reduction measures should be implemented within a defined time period.
4 Catastrophic	Where the moderate risk is associated with extremely harmful consequences, further assessment may be necessary to establish more precisely the likelihood of harm and basis for determining the level of the required control measures. Work should not be started until the risk has been reduced. Considerable resources may have to be allocated to reduce the risk. Where the risk involves death or serious, violent action should be taken.
5 Catastrophic	Work should not be started or continued until the risk has been reduced. If it is not possible to reduce risk even with continued resources, work has to be discontinued.

FIGURE 4. A risk assessment matrix classifies risks into various levels and specifies the type of action required for each case.

monitored by measuring the pressure drop over the length of the exhaust pipe – as material accumulates in the pipe the pressure drop increases. By monitoring for blockage, operators can ensure that the system is cleaned before its performance impacts production and at the same time avoid cleaning more frequently than required. Integrated vacuum and abatement systems often combine monitoring capabilities with automated software to alert operators of the need for maintenance.

While problems associated with accumulation of materials in process exhausts is arguably the most frequently encountered hazard faced by sub-fab maintenance personnel, another widely applied risk mitigation strategy, particularly for flammable process materials, is dilution below their lower flammability limit (LFL) with an inert gas such as nitrogen. However, it is important to understand the nature of the chemical processes occurring in the deposition chamber and to base the dilution calculation on the composition and volume of the effluent gas rather than the precursor. For example, TEOS is a precursor gas widely used in the chemical vapor deposition of silicon oxide films. The lower temperature needed for the CVD process and the absence of aggressive reaction products are the main advantages of using TEOS compared with traditional precursors such as silane and the mechanical and electrical properties of SiO₂ films deposited from TEOS are also very good. The decomposition products of TEOS in the gas phase in the absence of oxygen include organic fragments (ethanol, ethanal, ethene, methane, carbon monoxide), and in the

presence of oxygen include water vapour, carbon dioxide, ethanal and methanol [2], many of which are flammable. A dilution calculation based on the amount of TEOS entering the chamber rather than the volume of decomposition products exiting the chamber could easily lead to an underestimate of the required volume of diluent and the presence of a flammable mixture in the exhaust pipe in some circumstances. Once again, a rigorous risk assessment is required to identify such potential hazards and put corrective measures in place where needed.

Risk assessment and communication

It should be clear from the preceding discussion that a detailed technical

understanding of semiconductor manufacturing processes and materials and their impact on sub-fab equipment is a prerequisite for safe and efficient pumping and abatement of process exhaust. In particular, ensuring the safety of sub fab operations requires a formal process for risk assessment. Once determined, safe operating procedures must be codified and effectively communicated to field personnel, and a mechanism must exist to update procedures based on feed-back from the field. **FIGURE 4** is taken from the Risk Assessment Procedure [3] used at Edwards (adapted from Semi S10) and illustrates the Risk Rating Table, a matrix by which risks are evaluated and appropriate responses determined.

Once risks are assessed the information must be effectively communicated to users and field service personnel. To ensure appropriate dissemination of required information, Edwards publishes Application Notes for equipment users and Safety Application Procedures (SAP) for service engineers.

Conclusion

The hazardous nature of many of the materials present in the semiconductor manufacturing process creates significant safety risks for fab personnel and others living or working near the fab, and financial risks for manufacturers and investors. Managing those risks takes more than good intentions and common sense precautions. It requires a detailed and continuously updated technical understanding of the processes and materials based on broad experience across many different types of

applications, and ideally, partnership with process tool manufacturers during development and optimization of new processes. As in other high risk industries - nuclear, aviation, automotive, healthcare, oil, rail and military – best practice safety and risk management is heavily influenced by equipment manufacturers, who are in the best position to understand the capabilities of their products across a wide range of applications.

Ultimately the fab management team own the responsibility for managing risk and safety with the highest levels of corporate responsibility. Semiconductor equipment manufacturers, and in particular, manufacturers of pumping and abatement systems that handle and safely dispose of hazardous materials, have an invaluable supporting role to play with their continuous accumulation of know-how and formal processes for risk assessment, including a mechanism for distributing safety information to, and incorporating feedback from, the field.

References

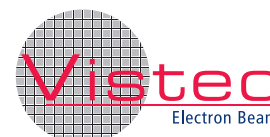
1. Andrew Chambers, Managing hazardous process exhausts in high volume manufacturing, Solid State Technology, 2016 Issue 2
2. Van der Vis, M.G.M., et al, The thermodynamic properties of tetraethoxysilane (TEOS) and an infrared study of its thermal decomposition, Colloque C3, supplement au Journal de Physique 11, Volume 3, aofit 1993, <http://dx.doi.org/10.1051/jp4:1993309>
3. Adapted from Semiconductor Equipment and Materials International (SEMI) standard S-10, <http://www.semi.org> ◆



Enjoy Infinite Possibilities.

Based on broad experience gathered over many years of developing, manufacturing and world-wide servicing field-proven electron-beam lithography systems, a team of highly-motivated employees, excellent researchers and creative engineers are constantly doing their best to fulfil our customers' requirements.

We understand E-Beam.



Process control and production cycle time

By **DOUGLAS G. SUTHERLAND** and **DAVID W. PRICE**, KLA-Tencor, Milpitas, CA

Having more process control points will not immediately change the number of excursions in a fab but it will immediately improve the efficiency with which the fab reacts to them.

In the early stages of development, having more process control can help reduce both the number and duration of cycles-of-learning (the iterations required to solve a particular problem). In high volume manufacturing a well-thought-out process control strategy can increase baseline yield and, at the same time, limit yield loss due to excursions. At all stages, an effective process control strategy is required to ensure that the fab is operating at its lowest possible cost. In addition to minimizing production costs, adding process control steps can, counterintuitively, also minimize cycle time[1-3].

FIGURE 1 shows a conceptual plot of how cycle time would vary as a function of the number of process control steps. On the left hand side of the chart where there are no metrology and inspection (M&I) steps in place, the cycle time is effectively infinite. If a lot reaches the end of the line and has zero yield there is no way to isolate the problem. Theoretically one could



FIGURE 1. Cycle Time (CT) versus the number of process control (metrology and inspection) steps. In zone 1, the fab is information starved and unable to find yield excursions and isolate the underlying problems. In zone 3, the fab is getting more information than it can use. In zone 2, the fab has achieved balance – with a number of process control steps that minimizes the cycle time.

isolate the problem by trial and error, but with only 100 process steps and only two parameters each, there would be 2100 (1.3×10^3) possible combinations. Even testing one parameter per second, it would take much longer than the age of the universe to exhaust all possible combinations of the parameter space.

As process control steps are added the cycle time comes down from an effectively infinite value to some manageable number. At some point the cycle time will reach a minimum value. Beyond this point, adding in further process control steps will actually cause the cycle time to increase linearly with the number of added steps. The optimal amount of process control will always be a trade-off between minimizing cycle time, minimizing excursion cost, and maximizing baseline yield. The latter two usually have a much greater financial impact.

Adding process control steps can reduce a fab's cycle time, but how does that work? A full treatment of cycle time (Queueing Theory) is far beyond the scope of this article, however at a high level, it can be broken down into a few manageable components. The total cycle time (CT) is the sum of the queue time (the time a lot spends waiting for a process tool to become available) and the processing time itself. Since the processing time is fixed, the only way to reduce CT is to concentrate on the queue time (Q). From Queueing Theory it can be shown that Q can be expressed by the product of three separate functions [4],

$$Q = f(u) f(a) f(v) \quad \text{eqn 1}$$

where $f(u)$, $f(a)$ and $f(v)$ are, respectively, functions of utilization, availability and variability. The first two functions will always be finite, therefore it becomes clear

DR. DAVID W. PRICE is a Senior Director at KLA-Tencor Corp. **DR. DOUGLAS SUTHERLAND** is a Principal Scientist at KLA-Tencor Corp., Milpitas, CA.

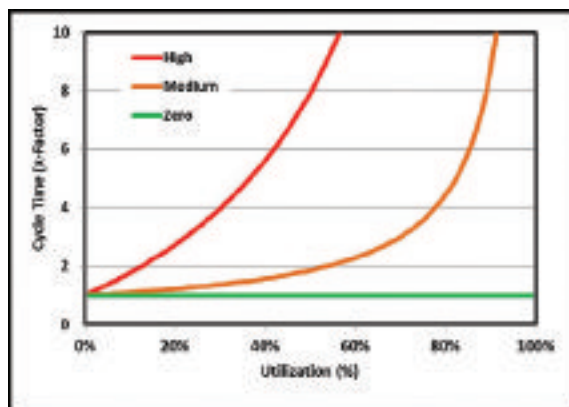


FIGURE 2. Cycle time versus Utilization for three different levels of variability: High, Medium and Zero.

that $Q = 0$ only when $f(v) = 0$. Put another way, reducing variability in the fab reduces the queue time, and if we remove all variability from the system the queue time will drop identically to zero and the CT will be equal to just the processing time.

FIGURE 2 shows a plot of CT as a function of utilization for three different levels of variability: zero, medium and high. The Y-axis measures cycle time in units of total

processing time called the X-factor. When the variability is zero all the lots move through the fab in lock-step; there is no increase in CT with increasing utilization and all tools could be run, theoretically, at 100 percent utilization. In this case the queue time is zero and the CT is equal to the total processing time for all the steps ($CT=1$). As soon as some variability is introduced, the CT starts to increase exponentially with utilization and the more variability there is, the more dramatic the increase becomes.

Variability in the fab comes from many sources: in the lot arrival rate, in the frequency of maintenance requirements, and in the time required for that maintenance to be performed are just a few of the sources. An excursion—a lot that is out of control—affects all of the above.

Having more process control points will not immediately change the number of excursions in a fab but it will immediately improve the efficiency with which the fab reacts to them.

In fact, over time, having more process control points can also reduce the number of excursions because it increases a fab's rate of learning.

PFEIFFER VACUUM



Semicon West, San Francisco
July 12 – 14, 2016
Please visit us at booth 1716

ATH 2804 M

Compact, magnetically levitated turbopumps in the pumping speed class of 3,000 l/s

- High gas throughput and high temperature operation required in harsh applications
- Tolerates exhaust pressure up to 3.4 mbar
- Low vibration operation with an automatic out-of-balance compensation

Are you looking for a perfect vacuum solution? Please contact us:

Pfeiffer Vacuum, Inc. · USA · T 800-248-8254 · F 603-578-6550 · contact@pfeiffer-vacuum.com
www.pfeiffer-vacuum.com



Consider a lot that has been flagged for having a defect count that was beyond the control limit for process step N. If, as shown in Fig. 3a, there was another inspection point between process steps N and N-1, then the problem can be immediately isolated. Only the tool at step N (the process tool the offending lot went through) needs to be put down and only the lots that went through that tool since the last good inspection need to be put on hold for disposition.

By contrast, consider what would happen in Fig. 3b where the last inspection point was five steps ago at process step N-5. Practices differ from fab to fab, however in the worst case scenario, all ten tools that the lot went through would be put down and all lots that went through any of those tools would have to be put on hold. Instead of a minor disruption involving a single process tool and a few lots, entire modules and dozens of lots can be directly affected. Indirectly, it affects the entire fab.

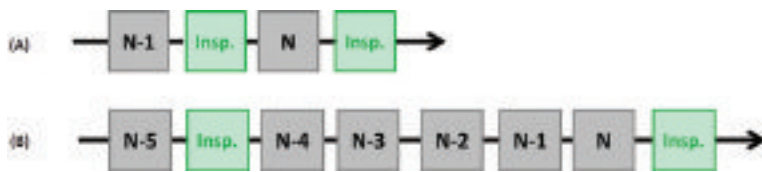


FIGURE 3. (a) One process step between inspection points.
(b) Five process steps between inspection points.

FIGURE 3 shows that implementing fewer inspection steps has a threefold impact on cycle time:

1. More process tools are involved and must be taken offline
2. Each process tool is down for a much longer period of time because it takes longer to isolate the problem
3. More wafers are in the impacted section of the production line. These wafers must be dispositioned

The variability introduced by these three impacts will also propagate through the fab; they constrict the flow of work in progress (WIP) through the fab, creating a WIP bubble that affects the lot arrival rate (increased variability) at every station downstream. All of these factors contribute to fab-wide variability and because of the re-entrant nature of the process flow, they add to the cycle time of every single lot in the fab.

When an excursion occurs, the resulting disruption impacts the cycle time of every lot in the fab and it quickly becomes a vicious cycle. The more excursions that happen during a given lot's cycle time, the longer that cycle time will be. And the longer the cycle time is, the more likely it is that that lot will be in the fab when the next excursion occurs.

Adding inspection steps will add a small, known amount of cycle time to those lots that get inspected, but due to sampling (not every lot gets inspected) it will have a much smaller impact on the average. When an excursion does occur, comparatively few process tools will have to be put down and the module owner will be able to isolate the problem much sooner. The total disruption to the fab (the variability) will be reduced and the cycle time of all lots will be improved.

This counter-intuitive concept has been borne out by several fabs that have both added inspection steps and reduced cycle time simultaneously. Adding process control steps contributes to fab efficiency on several levels: accelerating R&D and ramp phases, increasing baseline yield, limiting the duration of excursions, and reducing cycle time. In short, a better-controlled process is a more efficient process.

The next article in this series will discuss the impact of process control to cycle time on so-called "hot lots" typically run during early ramp.

Author's Note: The Process Watch series explores key concepts about process control—defect inspection and metrology—for the semiconductor industry. Following the previous installments, which examined the 10 fundamental truths of process control, this new series of articles highlights additional trends in process control, including successful implementation strategies and the benefits for IC manufacturing.

References:

1. "Process Watch: Fab Managers Don't Like Surprises," Solid State Technology, December 2014.
2. "Process Watch: Time is The Enemy of Profitability," Solid State Technology, May 2015.
3. "Economic Impact of Measurement in the Semiconductor Industry," Planning Report 07-2, National Institute of Standards and Technology, U.S. Department of Commerce, December 2007.
4. Hopp, W. J., and Spearman, M. L. *Factory Physics* (2nd ed.). (New York: Irwin, McGraw-Hill, 2001), 325. ◀



Get accurate readings and improve your yield.

Auto Multi Sensors - The world's most efficient and effective wireless multi-measurement device for semiconductor applications.



Leveling

+



Vibration

+



Humidity

It's the first wireless sensor to combine leveling, vibration and humidity measurement, available in both our WaferSense® or ReticleSense® form factors. Semiconductor fabs and equipment OEMs save time, save expense and improve yields with the Auto Multi Sensor portfolio.

CYBEROPTICS®

www.cyberoptics.com

Copyright © 2016. CyberOptics Corporation, Inc. All rights reserved.

Advancements in RH measurement in wafer and reticle environments

ALLYN JACKSON, CyberOptics Corp., Minneapolis, MN

Key IC fabrication steps are sensitive to moisture in semiconductor wafer environments. As the technology node advances, the need for characterizing and minimizing the exposure to relative humidity (RH) has become critical in all 29nm geometry fabs and below. These RH control requirements create a need for a wireless wafer-like humidity sensor which simultaneously measures RH at several points across the wafer as well as throughout the entire IC manufacturing environment.

Challenges with current methods for characterizing N2 FOUPs

Current methods for characterizing N2 Purge FOUPs have problems. These methods are typically not real time, are

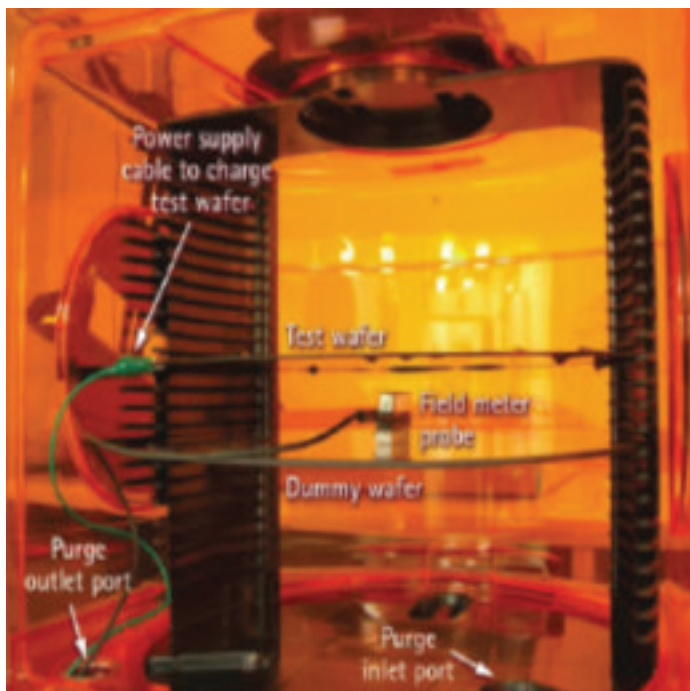


FIGURE 1. FOUP with Wired RH Sensors Attached

time consuming, are hard to use and are not able to take RH measurements under production conditions therefore are not reflective of these conditions. In addition, wired (**FIGURE 1**) hand-held RH meters (**FIGURE 2**) and single trace hand-held meters are limited to one area and cannot move throughout the process environment. Other options are hand-made alternatives (**FIGURE 3**) such as a wafer with RH sensors simply taped on. Lastly, they are often limited without data files generated so consequently statistics and quality standards cannot be established.

RH environment test target and goals

The test at the customer involved putting an RH meter inside the FOUP pointing around slot 13. The goal was to repeat the RH meter profile for testing a FOUP on one loadport without the need to open the FOUP. Starting at 40% RH (cleanroom environment), the first step was to run high purity, high volumetric

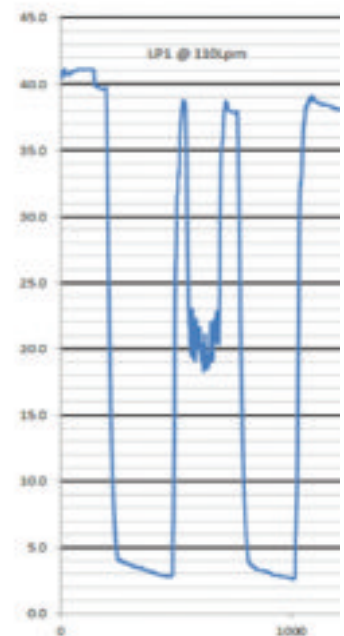


FIGURE 2. Hand-held RH Meter with Single Trace RH Reading

Many **THANKS** to the attendees, speakers and sponsors who made The ConFab 2016 a resounding success. We look forward to another great event in 2017!



Key Executives from these organizations were at The ConFab 2016:

3-WAY	International	Rogue Valley Microdevices
3MTS	IBM	Samsung
ACT International	IC Insights	Samsung SSI
Advantest	imec	SCREEN Semiconductor Solutions
Air Liquide Electronics	Infineon Technologies	Seagate
Akrometrix	Intel	SEMI
AMD	Intermolecular	SGL Carbon
Amkor Technology	Lam Research	Siemens
Applied Seals North America	Levitronix	Siemens PLM
ASML	Levitronix/Arintech	Silicon Catalyst
Astronics Test Systems	Linde	Silicon Labs
Aveni	M+W Group	SK Enterprises
Banner Industries	Maxim Integrated	SMIC
Cadence	Mentor Graphics	STATSChipPAC
Carnegie Mellon University	MicroChip Technology	SuperPhase Research, LLC
CEA Leti	Micron	SUSS MicroTec Inc.
Chipworks	Microtronic	TechInsights
Cisco Systems	MSR-FSR, LLC	Texas Instruments
Deposition Technology	Murata Machinery USA	The MAX Group
Edwards	Novati Technologies	Tosoh Quartz
Empire State Development	NVIDIA	Trebor International
Entegris, Inc.	NXP	TSMC/G450C
EV Group	NXP Semiconductors Singapore Pte Ltd	Ulvac Technologies
Flanders Investment and Trade	Pall Corporation	UMC
GE Digital	Power Integrations	Valqua America
GLOBALFOUNDRIES	PricewaterhouseCoopers	Western Digital
GPS Inventory Solutions Inc.	Process Technology	Xilinx
Headway/TDK Inc.	Qualcomm	Xycarb Ceramics
Hitech Semiconductor (Wuxi) Ltd.	QuantumClean	
Huatian Technology Group/FlipChip	RAVE LLC	

MARK YOUR CALENDAR FOR 2017!

The ConFab Conference & Networking Event
Encore at the Wynn | Las Vegas
June 11-14, 2017
www.theconfab.com



FIGURE 3. Silicon Wafer With 4 RH Recording Sensors Taped on.

N2 pre-purge for 4-5 minute and then take the reading. The second step is to conduct a maintenance purge to 5% and measure the results in 5 locations across the wafer. The next step was to run a process purge to 20% and take sample readings across various locations. The goal of the testing it to test the efficiency of the N2 purge FOUNDER (FOUP) diffusers to ensure that uniform purge levels are maintained.



FIGURE 4. WaferSense® Auto Multi Sensor Measurement Device.

In response to the need for a reliable easy to use method of qualifying N2 and XCDA environments, the WaferSense® Auto Multi-Sensor (AMS) by CyberOptics (**FIGURE 4**) was developed. WaferSense AMS is a wireless wafer-like device with five RH sensors to measure the RH profile across the entire wafer surface.

AMS is a complete and easy-to-use system which communicates wirelessly via Bluetooth to the MultiView™ application (**FIGURE 6**) and moves like a normal wafer to all locations in the

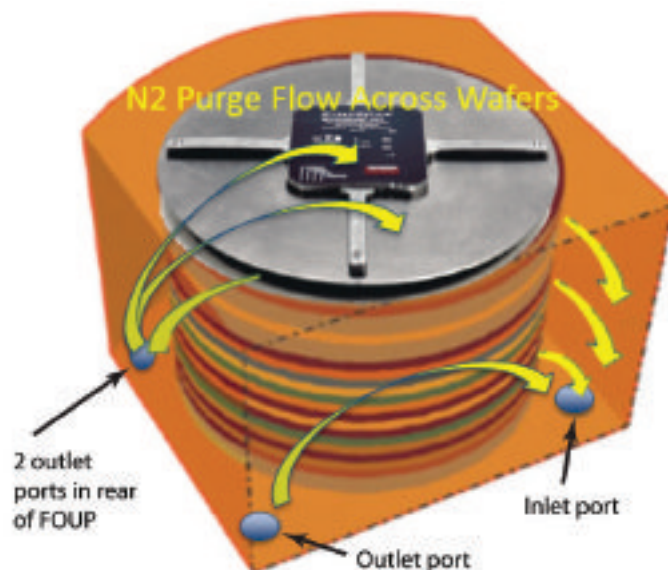


FIGURE 5. N2 Purge FOUNDER with 3 Inlet and one Outlet Ports.

wafer process environment providing a true characterization of the N2 purge uniformity. Such previously hard to accomplish tasks such as characterizing purge FOUNDER diffuser uniformity and measuring actual RH percentages are now easily accomplished with AMS. (**FIGURE 5**) AMS is a true multi-functional device which also measures vibration and can be used for leveling to ensure proper wafer handling.

29nm geometry fabs and smaller require well controlled N2 and XCDA purge environments to prevent defects and yield loss. AMS300 simultaneously measures RH in real-time at five locations on the wafer while it transfers like a wafer to qualify N2 and XCDA environments. The AMS device significantly shortens the task of qualifying

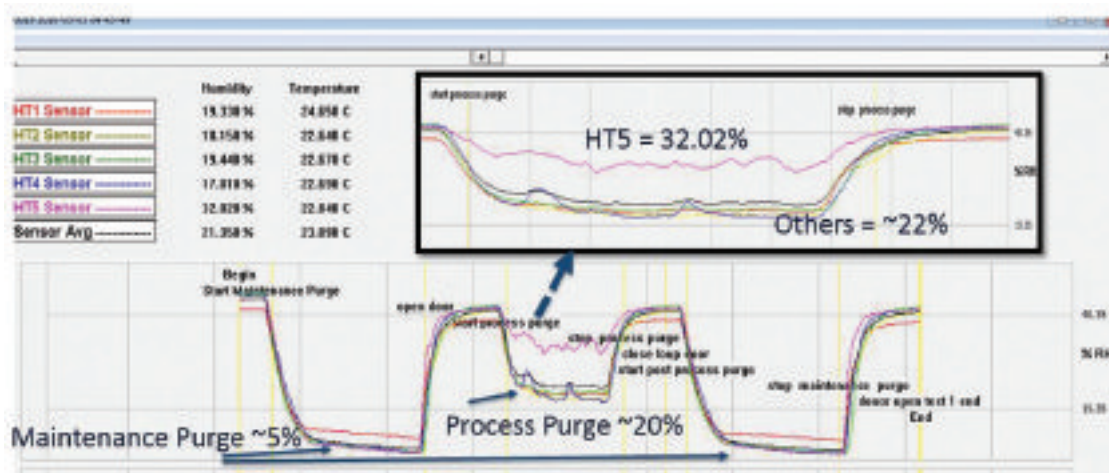


FIGURE 6. Profile of N2 Purge Using MultiView™ Software to Displays RH Measurements in 4 Sensor Locations across the Wafer Surface.

these environments. In addition, the AMS300 provides and vibration and leveling measurement capabilities to ensure proper wafer handling and reduced particles. The overall result for the fab is improved N2 purge environment uniformity which results in reduced defects and reduced labor costs.

Reducing reticle haze effects

193nm Immersion scanners are adversely affected by a phenomenon called “Reticle Haze” when proper measures are not taken to measure and control it. There are three areas that need to be controlled to reduce this haze effect on reticles, one of which is controlling RH. Reticle haze is accelerated when H₂O is present. (FIGURE 7).

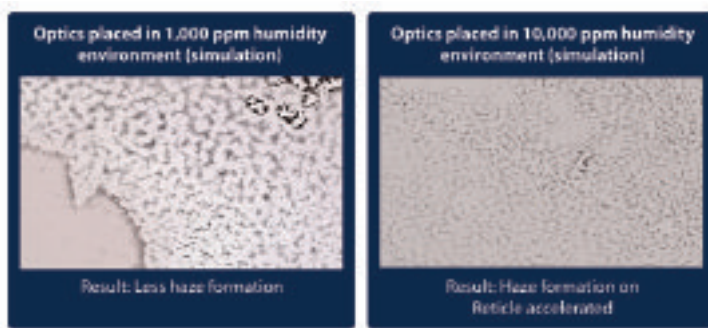


FIGURE 7. Reticle Haze Formation Accelerated with H₂O

There is a key need for a measurement device that will eliminate the inefficiencies of the current methods.

Challenges with current methods for monitoring RH in reticle environments

There are several limitations with the current reticle environment RH measurement methods, for example, hand-held RH sensors (FIGURE 9.) are inconvenient

and they can compromise the reticle environment. Plus, many areas are inaccessible by hand-held RH sensors, in-situ RH sensors or benchtop type RH sensors. (FIGURE 8.)

Additionally, the importance of particle, leveling, vibration and RH control has rarely been overlooked in reticle environment. However, the need to maximize both yields and tool uptimes in reticle mask environments requires best-in-class practices.



FIGURE 9. Wired In-Situ RH Sensor

Whether for diagnostics, qualification or preventative maintenance, equipment engineers need to efficiently and effectively make measurements and adjustments to the tools. Legacy particle, vibration, leveling and RH measurement methods are typically cumbersome, non-representative, not real time, compromise the production environment and are costly with downtime required to take the tool offline for these tasks.

By contrast, best practice methods involve collecting and displaying data in real-time, speeding equipment alignment or set-up. Real-time data also speeds equipment diagnostic processes, saving valuable time and resources. Equipment engineers can also make the right adjustments consistently by using objective and reproducible data that enhances process uniformity.

The ReticleSense® AMSR (FIGURE 10) is an actual glass reticle that measures H₂O in the reticle environment and is



FIGURE 10. ReticleSense® Auto Multi Sensor Measurement Device.



FIGURE 8. Benchtop RH Sensor

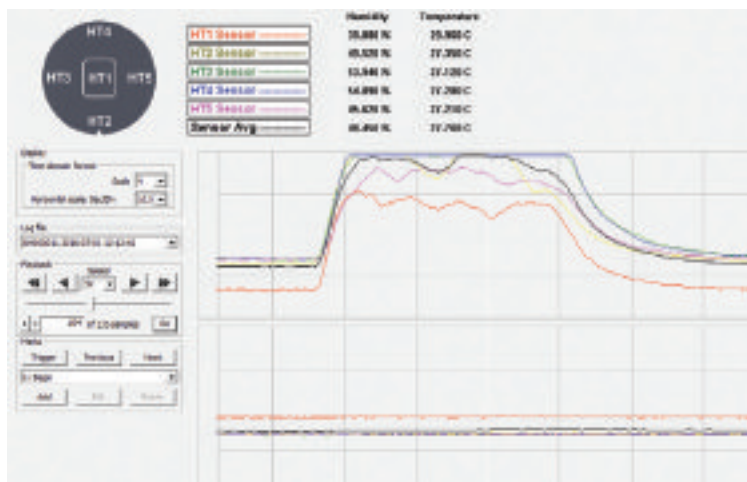


FIGURE 11. RH Measurement

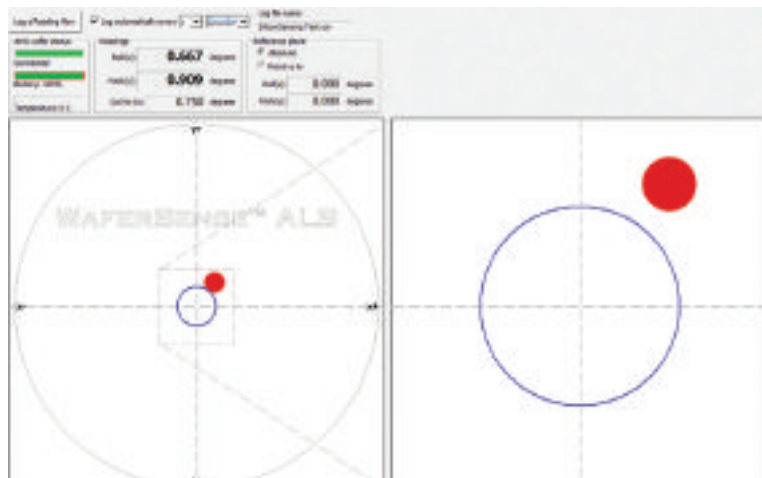


FIGURE 13. Leveling Measurement

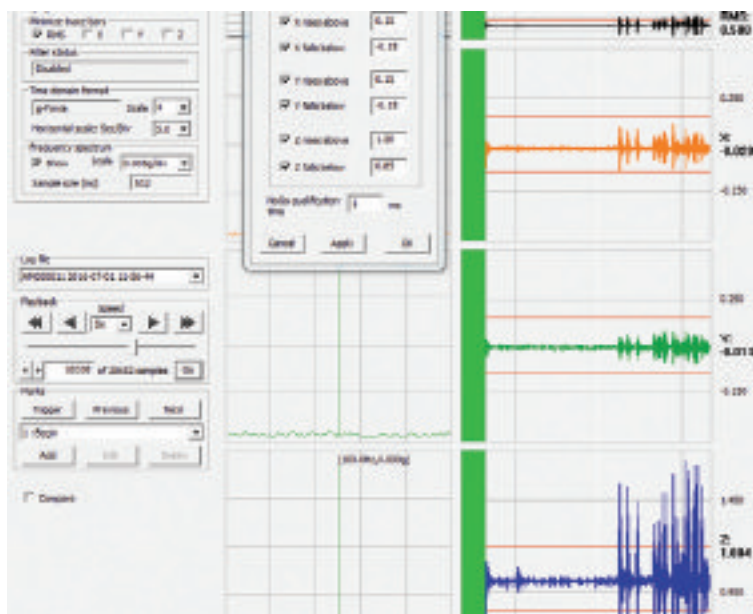


FIGURE 12. Vibration Measurement

compatible with ASML, Canon and Nikon scanners. AMSR is used to travel throughout the entire reticle environment and measures RH. (**FIGURE 11**) It helps locate the sources of the H₂O which results in increased reticle lifetime. Two additional measurement capabilities of the device include measuring X, Y and X vibration (**FIGURE 12**) and inclination. (**FIGURE 13**).

Conclusion

The AMSR travels the entire path of the reticle and can measure humidity in all locations. In immersion scanner environments, monitoring humidity is critical in reticle reducing haze. Equipment qualifications can be done faster as the same device also measures vibration and leveling. Controlling inclination, RH and vibration are all important factors in increasing yield and reducing downtime.

For RH measurements in N₂ and XCDA reticle mask environments, the use of a real-time measurement device, the Auto Multi Sensor, delivers on three compelling bottom lines for the fab – saving time, saving expense and improving yields. ◀

Changing markets drive smarter manufacturing by IC sector

PAULA DOE, SEMI, San Jose, CA

A day-long forum will be held at SEMICON West on the future of smart manufacturing in the semiconductor supply chain.

The changing market for ICs means the end of business as usual for the greater semiconductor supply chain. Smarter use of data analytics looks like a key strategy to get new products more quickly into high yield production at improved margins.

Emerging IoT market drives change in manufacturing

The emerging IoT market for pervasive intelligence everywhere may be a volume driver for the industry, but it will also put tremendous pressure on prices that drive change in manufacturing. Pressure to keep ASPs of multichip connected devices below \$1 to \$5 for many IoT low-to-mid end applications, will drive more integration of the value chain, and more varied elements on the die. "The value chain must evolve to be more effective and efficient to meet the price and cost pressures for such IoT products and applications," suggests Rajeev Rajan, VP of IoT, GLOBALFOUNDRIES, who will speak on the issue in a day-long forum on the future of smart manufacturing in the semiconductor supply chain at SEMICON West 2016 on July 14.



"It also means tighter and more complete integration of features on the die that enable differentiating capabilities at the semiconductor level, and also fewer, smaller devices that reduce the overall Bill of Materials (BOM), and result in more die per wafer." He notes that at 22nm GLOBALFOUNDRIES is looking to enable an integrated connectivity solution instead of a separate die or external chip. Additional requirements for IoT are considerations for integrating security at the lower semiconductor/hardware layers, along with the typical higher layer middleware and software layers.

This drive for integration will also mean demand for new advanced packaging solutions that deliver smaller, thinner, and simpler form factors. The cost pressure also means that the next nodes will have to offer tangible power/performance/area/cost (PPAC) value, without being too disruptive a transition from the current reference flow. "Getting to volume yields faster will involve getting yield numbers earlier in the process, with increasing proof-points and planning iterations up front with customers, at times tied to specific use-cases and IoT market sub-segments," he notes.

Rapid development of affordable data tools from other industries may help

Luckily, the wide deployment of affordable sensors and data analysis tools in other industries in other industries is developing solutions that may help the IC sector as well. "A key trend is the 'democratization' – enabling users to do very meaningful learning on data, using statistical techniques, without requiring a Ph.D. in statistics or mathematics," notes Bill Jacobs, director, Advanced Analytics Product Management, Microsoft Corporation, another speaker in the program. "Rapid growth of statistics-oriented languages like R across industries

PAULA DOE is a contributing writer at SEMI, San Jose, CA

is making it easier for manufacturers and equipment suppliers to capture, visualize and learn from data, and then build those learnings into dashboards for rapid deployment, or build them directly into automated applications and in some cases, machines themselves.”

Intel has reported using commercially available systems such as Cloudera, Aquafold, and Revolution Analytics (now part of Microsoft) to combine, store, analyze and display results from a wide variety of structured and unstructured manufacturing data. The system has been put to work to determine ball grid placement accuracy from machine learning from automatic comparison of thousands of images to select the any that deviate from the known-good pattern, far more efficiently than human inspectors, and also to analyze tester parametrics to predict 90% of potential failures of the test interface unit before they happen.

“The IC industry may be ahead in the masses of data it gathers, but other industries are driving the methodology for easy management of the data,” he contends. “There’s a lot that can be leveraged from other industries to improve product quality, supply chain operations, and line up-time in the semiconductor industry.”

Demands for faster development of more complex devices require new approaches

As the cost of developing faster, smaller, lower power components gets ever higher, the dual sourcing strategies of automotive and other big IC users puts even

more pressure on device makers to get the product right the first time. “There’s no longer time to learn with iterations to gradually improve the yield over time, now we need to figure out how to do this faster, as well as how to counter higher R&D costs on lower margins,” notes Sia Langrudi, Siemens VP Worldwide Strategy and Business Development, who will also speak in the program.

The first steps are to recognize the poor visibility and traceability from design to manufacturing, and to put organizational discipline into place to remove barriers between silos. Then a company needs good baseline data, to be able to see improvement when it happens. “It’s rather like being an alcoholic, the first step is to recognize you have a problem,” says Langrudi. “People tell me they already have a quality management system, but they don’t. They have lots of different information systems, and unless they are capturing the information all in one place, the opportunity to use it is not there.”

Other speakers discussing these issues in the Smart Manufacturing Forum at SEMICON West July 14 include **Amkor** SVP Package Products Robert Lanzone, **Applied Materials** VP New Markets & Services Chris Moran, **Intel** VP IoT/GM Industrial Anthony Neal Graves, **NextNine** US Sales Manager Don Harroll, Optimal+ VP WW Marketing David Park, **Qualcomm** SVP Engineering Michael Campbell, **Rudolph Technologies** VP/GM Software Thomas Sonderman, and **Samsung** Sr Director, Engineering Development, Austin, Ben Eynon. ◀

ad index

Advertiser	Pg
Aerotech.....	7,27
Busch.....	31
The ConFab.....	41
CyberOptics.....	9
DAIHEN Advanced Component.....	15
EAG Group.....	C4,C5
Edwards.....	C3
Electronic Fluorocarbons.....	39
Heidenhain.....	3,21
MEPTEC.....	11
Nikon Precision.....	5
Parker Hannifin Veriflo.....	C2,33
Pfeiffer Vacuum.....	17,37,47
PPE.....	23
QuantumClean.....	47
SEMI.....	25
Ulvac.....	47
Vistec.....	35
XwinSys.....	14,47
Y.E.S.....	19,29,47

The Advertiser's Index is published as a service. The publisher does not assume any liability for errors or omissions.

Solid State TECHNOLOGY

EXECUTIVE OFFICES

Extension Media 1786 18th Street, San Francisco, CA 94107-2343.

ADVERTISING

Sales Manager

Kerry Hoffman
1786 18th St.
San Francisco, CA 94107-2343
Tel: 978.580.4205
khoffman@extensionmedia.com

North America

Kerry Hoffman
Tel: 978.580.4205
khoffman@extensionmedia.com

Germany, Austria, E. Switzerland & E. Europe

Holger Gerisch
Tel: +49.0.8856.8020228
holgerg@pennwell.com

China, Hong Kong

Adonis Mak
Tel: +852.90182962
adonism@actintl.com.hk

Taiwan

Diana Wei
Tel: +886.2.23965128 ext: 270
diana@arco.com.tw

Rest of World

Kerry Hoffman
Tel: 978.580.4205
khoffman@extensionmedia.com

Webcasts

Jenna Johnson
Tel: 612.598.3446
jjohnson@extensionmedia.com

The ConFab

Kerry Hoffman
Tel: 978.580.4205
khoffman@extensionmedia.com

ADVERTISEMENT



PFEIFFER VACUUM

Harsh Process Dry Pumps

The Pfeiffer Vacuum A4 series of harsh duty, process dry pumps feature energy efficient, multi-stage Roots technology, advanced corrosion and byproduct resistance, and superior powder handling capability. Visit Pfeiffer Vacuum at Semicon Booth #1716.

www.pfeiffer-vacuum.com



Non-volatile Memory Solutions

ULVAC Technologies deposition and etching equipment provides fabrication solutions for non-volatile memory technologies. Whether it is MRAM, PCRAM, ReRAM, FeRAM, CBRAM or STT-MRAM, ULVAC has unique and novel solutions ideal for fabrication of these memory technologies. Contact: sales@us.ulvac.com or 978-686-7550.

SEMICON Booth #1229

www.ulvac.com

ONYX: A New In-Line & Non-Destructive Hybrid Technology

XwinSys has recently launched the ONYX - a novel hybrid metrology system, uniquely integrating advanced XRF, 2D and 3D optical technologies, designed to meet the current and future metrological challenges of the semiconductor industry.

SEMICON WEST: Booth #2245

XwinSys
Technology Development Ltd.



www.xwinsys.com



Cure Ovens for Dielectric Polymers

**The Equipment You Want
For the Results You Need!**

Superior yields with:

- Excellent thermal, electrical and mechanical properties
- Reliable multi-level interconnections
- Proper cross-linking
- No stress
- No cracking or lifting
- Low cost of ownership/FAST ROI

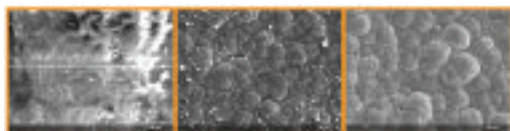
www.yieldengineering.com



INNOVATION & TECHNOLOGY LEADER™

QuantumClean® consistently achieves highly optimized cleanliness through its proprietary process chamber parts cleaning technique called **Atomically Clean Surface™ (ACS™)** which exceeds stringent OEM defectivity requirements for sub-16nm technologies.

See how ACS™ cleans SiC grain boundaries and structures without impacting the coating surface.



Pre-Clean with deposition Post-Clean without ACS™ process Post-Clean with ACS™ process

www.quantumclean.com

Magazine



Website

Six e-Newsletters

Solid State Technology

For over 50 years, Solid State Technology has been the leading independent media resource, covering:

- Semiconductors
- Advanced Packaging
- MEMS
- Displays
- LEDs

Request a **FREE** subscription to our magazine and e-Newsletters today at www.solid-state.com/subscribe

www.solid-state.com

Time to uncover the process mystery for IC designs

Semiconductor processes have long been a mystery for many circuit designers. They didn't need to worry about how chips were fabricated most of the time, thanks to the many EDA innovations that make their jobs easier and complex designs possible.

The success of the foundry-fabless business model over the past 20 years has been one of the main drivers of the booming of semiconductor industry. The cooperation between foundries and IC designs in fabless companies for process development worked so well that process engineers and circuit designers only needed to focus on their area of expertise. EDA flows simplified the interaction by using process design kits (PDKs) as the information carrier for circuit designs and sent tapeout databases (GDSII) back to the foundry for chip fabrication. Most designers didn't need to dig into the process.

That was then. The designer now is forced to understand process and devices when moving to smaller nodes in order to achieve more competitive designs. Because process is the least understood, the loose link between process and design should be enhanced to improve design and tapeout confidence.

Knowing processes and devices would help designers make better use of the process platform and improve designs. Device geometries are getting smaller and new structures such as FinFET and FD-SOI are becoming mainstream leading to complicated device characteristics and SPICE models, the most critical components in the PDK. They represent a process platform's performance and device characteristics, fundamental to good circuit design. A solid understanding of SPICE models becomes necessary to make full use of the process. This is true not only for designs at advanced nodes at 28nm beyond, such as 16nm, 14nm and 10nm, but critical for some refreshed older technologies for IoT/Wearable applications.

Running a full evaluation of process and device performance would provide guidance to better select device types, optimize device sizes and bias conditions, trade-off circuit speed and power. The same logic can be applied to generic circuit designs at any technology node, such as analog designs at 180nm or above.



This practice is used mostly within IDMs where process and design teams have

DR. ZHIHONG LIU, *Chairman and CEO,*
ProPlus Design Solutions

fairly direct channels to work cooperatively. Recently, fabless companies strengthened links with foundries to understand the process and devices to improve design output or for process-circuit co-design for high-end chip designs with more aggressive speed, power and performance specifications.

These efforts are significant. Most companies don't have the resources and time to build a dedicated team and flow and there have been no available EDA tools dedicated to helping designers understand process and facilitate process development interactions. Increasing time-to-market pressures and tough competition drive the need to a higher priority.

Without an EDA tool, current practices can easily take weeks or months to build, maintain and run a flow by creating scripts or SPICE netlists for different evaluation items. It's practically impossible to run through the cases to generate a full picture of process platform for designers within a short turnaround time.

As a result, it's hard to come up with a set standard for process evaluation before using it in design, as efforts can vary for different projects. For a big corporation with many design projects, dealing with multiple foundries, using multiple technology nodes and different process platforms, this type of work is critical to its success however becomes overloaded.

Furthermore, the complexity of SPICE models is exploding. Thousands of parameters in each model and a huge model library file with more than 100K lines of code are quite common. Macro models with complicated layout-dependent effects and random variations add more dimensions of complexity.

Complexity and time pressures are huge. An EDA tool to manage both would be indispensable.

One tool could use the PDK library as the input to explore, compare and verify models. It could help designers understand and explore the process-design space to guide process platform selection and enable quick adoption of the process and assist designs. It would help designers dig into the process from different angles, including a high-level summary of the process and device performance, device characteristics, statistical behavior and circuit performance related to the application. This should enable designers quickly adopt and make full use of a process platform that suits their needs. ◀

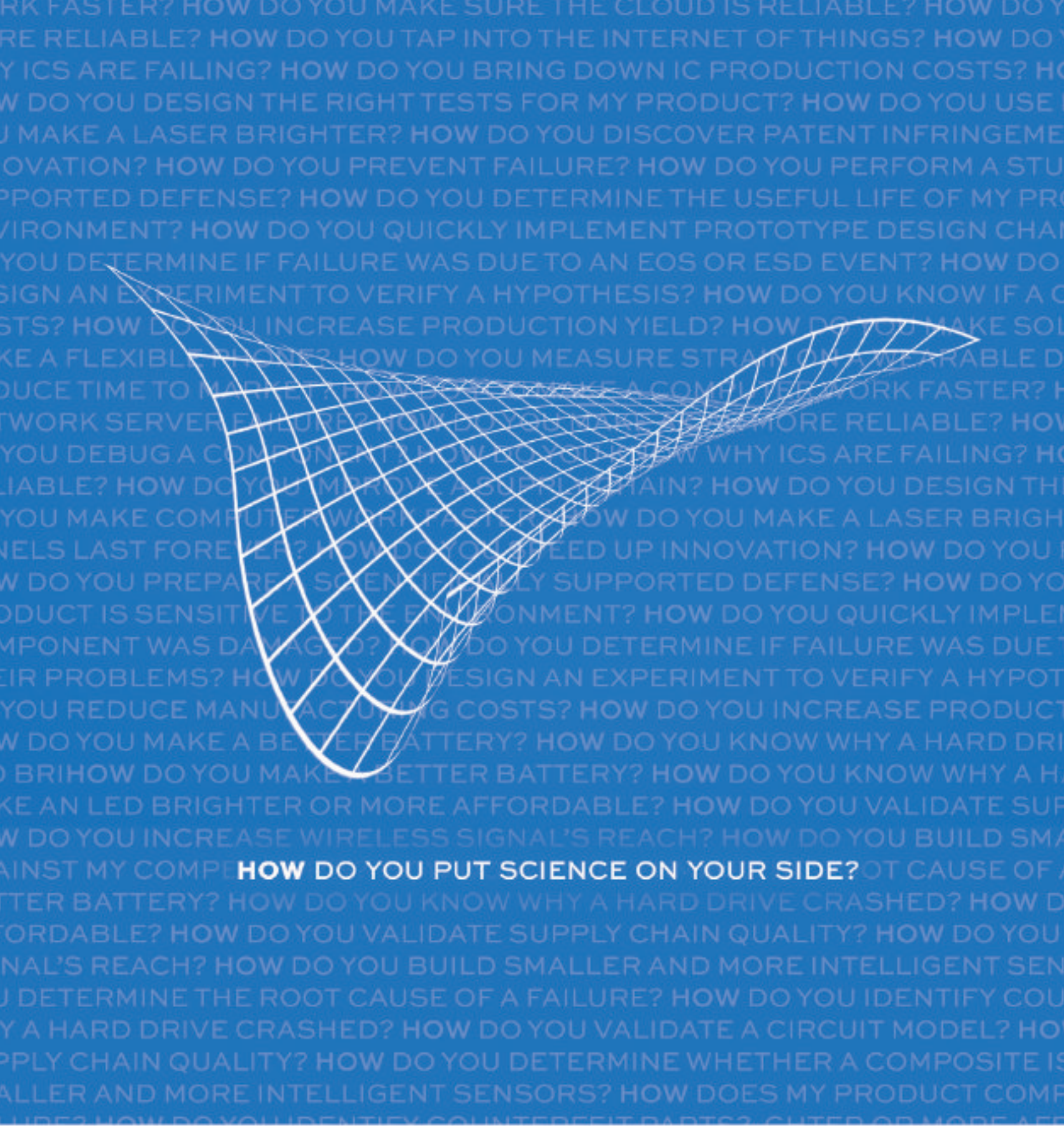
GLOBAL EXPERTISE LOCALLY APPLIED

EDWARDS SERVICE SOLUTIONS

Your business success, enabled by the optimum performance and up-time of our equipment, is our top priority.

Whether you are simply looking for help and advice, or want a long term total service partner, we are committed to providing service solutions that meet your needs and objectives.





HOW DO YOU PUT SCIENCE ON YOUR SIDE?

How do you make a product better, easier to use or less expensive? How do you ensure regulatory compliance or strengthen your legal case? How do you bring powerful scientific know-how across materials sciences, engineering sciences and life sciences to your commercial challenges? Ask EAG. **We Know How.** www.eag.com

EAG
LABORATORIES

WE KNOW
HOW

— **A GLOBAL SCIENTIFIC SERVICES COMPANY** —
MATERIALS SCIENCES • ENGINEERING SCIENCES • LIFE SCIENCES