JULY 2017

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# Solid State TECHNOLOGY Insights for Electronics Manufacturing

Overcoming Challenges in 3D NAND Volume Manufacturing

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In–line Metrology for Characterization of Bonded Wafers

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The Pervasiveness of ASICs in the IoT Era

## Laser Debonding for Ultrathin and Stacked Fan Out P12

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Solid-state UV laser debonding utilizing temporary glass carriers enables cost-effective high-volumemanufacturing (HVM) processing of ultra-thin stacked fan-out packages.

### FEATURES



#### ADVANCED PACKAGING | Laser debonding for ultrathin and stacked fan out packages

UV laser debonding solutions combine the advantages of the solid-state laser with low maintenance, low consumables costs and high pulse frequencies combined with high spatial control due to the special beam shaping optics. *Elisabeth Brandl, Thomas Uhrmann and Martin Eibelhuber, EV Group, St. Florian, Austria* 



#### 3D NAND | Overcoming challenges in 3D NAND volume manufacturing

As 3D NAND becomes the mainstream technology, its challenging roadmap poses opportunities for continued innovation. Harmeet Singh, Lam Research, Fremont, CA



#### **METROLOGY** | In-line metrology for characterization and control

### of extreme wafer thinning of bonded wafers

In-line metrology methods used during extreme wafer thinning process pathfinding and development are introduced. M. Liebens, A. Jourdain, J. De Vos, T. Vandeweyer, A. Miller, E. Beyne, imec, Leuven, Belgium, and S. Li, G. Bast, M. Stoerring, S. Hiebert, A. Cross, KLA-Tencor Corporation, Milpitas, California



**VACUUM TECH** | Enhanced vacuum security using advanced sub-fab monitoring and data analytics Sub-Fab Fault Detection and Classification (FDC) software platforms collect, integrate and analyse operational data. *Erik Collart, Edwards, Sanborn, NY* 



#### **IOT** The pervasiveness of ASICs in the IoT era

For an increasing number of designs, companies are finding it beneficial to design their own ASICs with system-on-achip (SoC) complexity.



#### **METROLOGY** | NASA's new vacuum-channel nanoelectronics rely on Park Systems AFM Using scanning capacitance microscopy with a Park Systems atomic force microscope a team at NASA successfully characterized both the spatial variations in capacitance as well as the topography of vacuum-channel nanoelectronic

Mark Andrews, Park Systems, Santa Clara, CA

### COLUMNS

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transistors

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### editorial

# What's next in leading edge semiconductor manufacturing?

Do you know what's coming? The semiconductor industry is evolving rapidly, driven by new demands from an increasingly diverse array of applications, including the IoT, 5G telecommunication, autonomous driving, virtual and augmented reality, and artificial intelligence/deep learning. Solid State Technology will be conducting a new survey will take aim at understanding what this evolution means to the semiconductor manufacturing industry supply chain in terms of the technology that will be needed.

IoT alone is expected to drive not only a huge demand for sensors, but a far more sophisticated cloud computing infrastructure that will employ the most advanced logic and memory chips available, including 7 and 5nm logic devices and 3D NAND. The survey will provide answer to questions such as:

- What new materials are going into volume production and what kind of challenges do they create in terms of availability, handling and disposal?
- How are fabs dealing with more complex devices structures such as FinFETs and 3D NAND which can create new pressures on process control, yield, and economics?

- EUV lithography is expected to be in volume production for the 5nm node, if not sooner. What new opportunities and challenges will this create in the supply chain for process equipment, materials and inspection tools?
- 200mm fabs are seeing a resurgence, in part due to the booming market for IoT devices and sensors. How will this impact the leading edge?
- What kind of new challenges and opportunities exist in heterogeneous integration and advanced packaging?

The survey will be conducted across the entire Solid State Technology audience, which includes more than 180,000 engineering and management professionals in 181 countries. The report will be compiled by Solid State Technology editors, who will add valuable insights and interpretations based on decades of experience.

Stay tuned for the survey – we welcome your input!

-Pete Singer, Editor-in-Chief

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### **Web Exclusives**

## Supply chain needs paradigm shift in how to look at defect control

The future of contamination control in the next-generation supply chain for beyond 14nm-node semiconductor processes faces stringent challenges. While Moore's Law is driving scale reduction, the industry is also facing ever-increasing process sensitivity, integration challenges of new materials and the need for unprecedented purity at process maturity. http://bit.ly/2sa0Qjb

## Volatility in electronic equipment supply chain

Understanding volatility in the electronic equipment supply chain can be valuable in forecasting future business activity. A useful way to compare relevant electronic industry data series is by using 3/12 growth rates. The 3/12 growth is the ratio of three months of data, compared to the same three months a year earlier.

http://bit.ly/2sBFzAb

### Topics from ECTC 2017: Thin Die Handling; IPD on Glass

There were a total of 335 presentations in 36 oral sessions at this year's ECTC. Since 2012 attendance is up ~ 50% to 1438 and professional development course attendance is up from 83 to 203! IFTLE feels this follows the trends that we have been sharing with you for years, i.e. scaling is slowing down and more and more front end practitioners are moving to the back end to develop customized products.

http://bit.ly/2spE7Bu

## SEMICON West preview: Equipment components and subsystems

Fabs and tool makers are starting to pay a lot more attention to suppliers of components and subsystems– as defects in these materials start to impact yields at 14nm and below. Solving these emerging issues, though, will take a collaborative effort to determine what parameters matter, how to measure them, and how to trace them back across an extended supply chain, suggests Pawitter Mangat, GLOBALFOUND-RIES director of Global Incoming Quality, one of the speakers who'll discuss these issues in the program on component impact on yields at advanced nodes, July 11, at SEMICON West 2017.

http://bit.ly/2sC3fo1



### **Global semiconductor sales increase** 21% year-to-year in April

Double-digit annual growth projected for 2017. http://bit.ly/2tw8ltd

### Insights from the Leading Edge: Bar Cohen to take Over IEEE EPS (CPMT)

At the Board of Governors meeting just held in conjunction with the 2017 ECTC conference, Avram Bar Cohen was elected as the first President of the newly named society.

http://bit.ly/2tbfx3X

### **Understanding EUV lithography basics and status – Key concepts**

For a better understanding of EUVL's status, challenges and opportunities, it is important to study its fundamental components. There are several, with the main ones being source, mask, optics, imaging and resists. They are very different from those in the current 193 nm immersion lithography, and a comprehensive overview of these components is a must. Hence, in the annual EUVL Workshop we dedicate one full day to a study of fundamentals with experts.

http://bit.ly/2synQJb

### **SUNY ranks among top 100** worldwide for patents granted in 2016

The State University of New York ranked 38th in the "Top 100 Worldwide Universities Granted U.S. Utility Patents for 2016," according to the National Academy of Inventors (NAI) and Intellectual Property Owners Association (IPO), which publishes the ranking annually based on U.S. Patent and Trademark Office data.

http://bit.ly/2tbkMQY

#### North American semiconductor equipment industry posts May 2017 billings

SEMI reports that the three-month average of worldwide billings of North American equipment manufacturers in May 2017 was \$2.27 billion. The billings figure is 6.4 percent higher than the final April 2017 level of \$2.14 billion, and is 41.9 percent higher than the May 2016 billings level of \$1.60 billion.

http://bit.ly/2twmSu1

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### worldnews

EUROPE - Imec announced that it has developed 200V and 650V normally-off/enhancement mode (e-mode) on 200mm/8-inch GaNon-Silicon wafers.

ASIA - Samsung Electronics began mass producing a new mid-power LED package, the LM301B, which features the industry's highest luminous efficacy of 220 lumens per watt.

USA - Mentor announced that it has launched the Mentor OSAT Alliance program to help drive ecosystem capabilities in support of new high-density advanced packaging technologies.

ASIA - UMC appointed senior vice presidents SC Chien and Jason Wang as co-presidents of the company, following Po-Wen Yen's retirement as UMC CEO.

USA - SEMI announced that the two-day Strategic Materials Conference (SMC) is slated for September 19-20 at San Jose's Doubletree by Hilton Hotel.

EUROPE - EV Group announced that it is expanding production capacity at its corporate headquarters in St. Florian am Inn, Austria.

**USA** - Silicon Integration Initiative Inc. announced the contribution of a new integrated circuit programming language developed by Intel Corporation for the 2D pattern analysis of sub-20nm mask layouts.

ASIA - Air Products received multiple, long-term supply awards from semiconductor and flat panel display manufacturers in China.

**USA** - Cypress Semiconductor **Corporation** announced that **Executive Chairman Ray Bingham** tendered his resignation as Executive Chairman and stepped down from the Board of Directors.

**EUROPE** - Queen's University researchers have discovered a new way to create extremely thin electrically conducting sheets, which could revolutionize the tiny electronic devices that control everything from smart phones to banking and medical technology.

### IBM Research Alliance builds new transistor for 5nm technology

IBM, its Research Alliance GLOBALFOUNDRIES and Samsung, and equip- Research Alliance at the SUNY Polytechnic ment suppliers have developed an industry-first Institute Colleges of Nanoscale Science and process to build silicon nanosheet transistors that Engineering's NanoTech Complex in Albany, NY will enable 5 nanometer (nm) chips. The details of achieved the breakthrough by using stacks of the process will be presented at the 2017 Symposia silicon nanosheets as the device structure of the on VLSI Technology and Circuits conference in transistor, instead of the standard FinFET archi-Kyoto, Japan. In less than two years since devel- tecture, which is the blueprint for the semiconoping a 7nm test node chip with 20 billion transis- ductor industry up through 7nm node technology. tors, scientists have paved the way for 30 billion switches on a fingernail-sized chip.

partners Scientists working as part of the IBM-led

The resulting increase in performance will help accelerate cognitive computing, the Internet of Things (IoT), and other data-intensive applications delivered in the cloud. The power savings could also mean that the batteries in smartphones and other mobile products could last two to three times longer than today's devices, before needing to be charged.

"For business and society to meet the demands of cognitive and cloud computing in the coming years, advancement in semiconductor technology is essential," said Arvind Krishna, senior vice president, Hybrid Cloud, and director, IBM Research. "That's why IBM aggressively pursues new and different architectures and materials that push the limits of this industry, and brings

Continued on page 9

### Long-term IoT semiconductor forecast reduced

IC Insights recently released its Update to its 2017 IC Market Drivers Report. The Update includes IC Insights' latest outlooks on the smartphone, automotive, PC/tablet and Internet of Things markets.

In the Update, IC Insights scaled back its total semiconductor sales forecast for system functions related to the Internet of Things in 2020 by about \$920 million, mostly because of lower system functions are now expected to reach revenue projections for connected cities appli- \$31.1 billion in 2020 (Figure 1) versus the prevications (such as smart electric meters and infra- ous projection of \$32.0 billion in the final year structure supported by government budgets). of the forecast. The updated forecast still shows total 2017 sales of IoT semiconductors rising about 16.2% to IC Insights' revised outlook for IoT semicon-\$21.3 billion (with final revenues in 2016 being ductor sales by end-use market categoslightly lowered to \$18.3 billion from the previ- ries shows that semiconductor revenues for ous estimate of \$18.4 billion), but the expected connected cities applications are projected to compound annual growth rate between 2015 and 2020 has been reduced to 14.9% versus the CAGR 2020 (down from 9.7% in IC Insights' original of 15.6% in IC Insights' original projection from forecast). Meanwhile, the IoT semiconductor December 2016. Total semiconductor sales for IoT



grow by a CAGR of 8.9% between 2015 and

Continued on page 9

### Lab on a chip could monitor health, germs and pollutants

Imagine wearing a device that continuously analyzes your sweat or blood for different types of biomarkers, such as proteins that show you may have breast cancer or lung cancer.

Rutgers engineers have invented biosensor technology – known as a lab on a chip – that could be used in hand-held or wearable devices to monitor your health and exposure to dangerous bacteria, viruses and pollutants.

"This is really important in the context of personalized medicine or personalized health monitoring," said Mehdi Javanmard, an assistant professor in the Department of Electrical and Computer Engineering at Rutgers University-New Brunswick. "Our technology enables true labs on chips. We're talking about platforms the size of a USB flash drive or something that can be integrated onto an Apple Watch, for example, or a Fitbit."

A study describing the invention was recently highlighted on the cover of Lab on a Chip, a journal published by the Royal Society of Chemistry.

The technology, which involves electronically barcoding microparticles, giving them a bar code that identifies them, could be used to test for health and disease indicators, bacteria and viruses, along with air and other contaminants, said Javanmard, senior author of the study.

In recent decades, research on biomarkers – indicators of health and disease such as proteins or DNA molecules – has revealed the complex nature of the molecular mechanisms behind human disease. That has heightened the importance of testing bodily fluids for numerous biomarkers simultaneously, the study says.

"One biomarker is often insufficient to pinpoint a specific disease because of the heterogeneous nature of various types of diseases, such as heart disease, cancer and inflammatory disease," said Javanmard, who works in the School of Engineering. "To get an accurate diagnosis and accurate management of various health conditions, you need to be able to analyze multiple biomarkers at the same time."

Well-known biomarkers include the prostate-specific antigen (PSA), a protein generated by prostate gland cells. Men with prostate cancer often have elevated PSA levels, according to the National Cancer Institute. The human chorionic gonadotropin (hCG) hormone, another common biomarker, is measured in home pregnancy test kits.

Bulky optical instruments are the state-of-the-art technology for detecting and measuring biomarkers, but they're too big to wear or add to a portable device, Javanmard said.



An artists' rendition of microparticles flowing through a channel and passing through electric fields, where they are detected electronically and barcode-scanned. Credit: Ella Marushchenko and Alexander Tokarev/Ella Maru Studios Electronic detection of microparticles allows for ultra-compact instruments needed for wearable devices. The Rutgers researchers' technique for barcoding particles is, for the first time, fully electronic. That allows biosensors to be shrunken to the size of a wearable band or a micro-chip, the study says.

The technology is greater than 95 percent accurate in identifying biomarkers and finetuning is underway to make it 100 percent accurate, he said. Javanmard's team is also working on portable detection of microrganisms, including disease-causing bacteria and viruses.

"Imagine a small tool that could analyze a swab sample of what's on the doorknob of a bathroom or front door and detect influenza or a wide array of other virus particles," he said. "Imagine ordering a salad at a restaurant and testing it for E. coli or Salmonella bacteria."

That kind of tool could be commercially available within about two years, and health monitoring and diagnostic tools could be available within about five years, Javanmard said.

## **news**cont

### **SEMICON West to highlight China growth surge**

SEMI announced the addition of a new high-profile program on China to its 2017 conference lineup for SEMICON West (July 11-13). Slated for July 11 at San Francisco's Yerba Buena Theater, the China Strategic Innovation & Investment Forum will focus on the extensive business opportunities resulting from the semiconductor industry's largest regional growth spurt now occurring in China.

While the global semiconductor industry continues to consolidate through large-scale mergers and acquisitions, China is embarking on a new round of expansion with heavy investment from public and private funding. China's semiconductor industry is growing at an explosive rate, leading the rest of the world with a projected increase of 68 percent in fab equipment spending year-over-year (2017 to 2018), according to the May 2017 SEMI World Fab Forecast. China will be equipping over 50 facilities through 2018, and is forecast to spend more than US\$11 billion.

The rise of the semiconductor industry in China need not be viewed as a threat to other global players, but rather as a significant driver of growth and business opportunity for suppliers worldwide. With its low indigenous market share for chips and nascent technical breadth in IC design, manufacturing, packaging, testing, equipment, and materials, China has become an enormous market for suppliers across the supply chain. In fact, ICs still top the list of all Chinese bulk imports in terms of U.S. dollar value.

At the China Strategic Innovation & Investment Forum, semiconductor and investment executives, as well as key China government and trade officials will share their views on the industry's evolution and offer insights on growth, investment opportunities, M&A, and the latest innovations emerging in China. Attendees will hear from C-Level executives from Ali Cloud, AMEC, Applied Materials Venture Capital Group, Goldman Sachs, Verisilicon, Walden International, SEMI China, and more. An hour-long panel discussion, moderated by Lung Chu, president of SEMI China, will feature speakers and a Q&A session. With access to China experts presenting and multiple networking opportunities, the China forum will offer a collaborative platform where markets, technology, talent, and funding can meet up for mutual benefit.  $\triangleleft$ 

## GLOBALFOUNDRIES on track to deliver Leading-Performance 7nm FinFET technology

GLOBALFOUNDRIES announced the availability of its 7nm Leading-Performance (7LP) FinFET semiconductor technology, delivering a 40 percent generational performance boost to meet the needs of applications such as premium mobile processors, cloud servers and networking infrastructure. Design kits are available now, and the first customer products based on 7LP are expected to launch in the first half of 2018, with volume production ramping in the second half of 2018.

In September 2016, GF announced plans to develop its own 7nm FinFET technology leveraging the company's unmatched heritage of manufacturing high-performance chips. Thanks to additional improvements at both the transistor and process levels, the 7LP technology is exceeding initial performance targets and expected to deliver greater than 40 percent more processing power and twice the area scaling than the previous 14nm FinFET technology. The technology is now ready for customer designs at the company's leading-edge Fab 8 facility in Saratoga County, N.Y.

"Our 7nm FinFET technology development is on track and we are seeing strong customer traction, with multiple product tapeouts planned in 2018," said Gregg Bartlett, senior vice president of the CMOS Business Unit at GF. "And, while driving to commercialize 7nm, we are actively developing next-generation technologies at 5nm and beyond to ensure our customers have access to a world-class roadmap at the leading edge."

GF also continues to invest in research and development for next-generation technology nodes. In close collaboration with its partners IBM and Samsung, the company announced a 7nm test chip in 2015, followed by the recent announcement of the industry's first demonstration of a functioning 5nm chip using silicon nanosheet transistors. GF is exploring a range of new transistor architectures to enable its customers to deliver the next era of connected intelligence.

GF's 7nm FinFET technology leverages the company's volume manufacturing experience with its 14nm FinFET technology, which began production in early 2016 at Fab 8. Since then, the company has delivered "first-time-right" designs for a broad range of customers.

To accelerate the 7LP production ramp, GF is investing in new process equipment capabilities, including the addition of the first two EUV lithography tools in the second half of this year. The initial production ramp of 7LP will be based on an optical lithography approach, with migration to EUV lithography when the technology is ready for volume manufacturing.

IBM Research Alliance, Continued from page 6

them to market in technologies like mainframes and our cognitive systems."

The silicon nanosheet transistor demonstration, as detailed in the Research Alliance paper Stacked Nanosheet Gate-All-Around Transistor to Enable Scaling Beyond FinFET, and published by VLSI, proves that 5nm chips are possible, more powerful, and not too far off in the future.

Compared to the leading edge 10nm technology available in the market, a nanosheet-based 5nm technology can deliver 40 percent performance enhancement at fixed power, or 75 percent power savings at matched performance. This improvement enables a significant boost to meeting the future demands of artificial intelligence (AI) systems, virtual reality and mobile devices.

#### Building a new switch

"This announcement is the latest example of the world-class research that continues to emerge from our groundbreaking public-private partnership in New York," said Gary Patton, CTO and Head of Worldwide R&D at GLOBALFOUNDRIES. "As we make progress toward commercializing 7nm in 2018 at our Fab 8 manufacturing facility, we are actively pursuing next-generation technologies at 5nm and beyond to maintain technology leadership and enable our customers to produce a smaller, faster, and more cost efficient generation of semiconductors."

IBM Research has explored nanosheet semiconductor technology for more than 10 years. This work is the first in the industry to demonstrate the feasibility to design and fabricate stacked nanosheet devices with electrical properties superior to FinFET architecture.

This same Extreme Ultraviolet (EUV) lithography approach used to produce the 7nm test node and its 20 billion transistors was applied to the nanosheet transistor architecture. Using EUV lithography, the width of the nanosheets can be adjusted continuously, all within a single manufacturing process or chip design. This adjustability permits the fine-tuning of performance and power for specific circuits – something not possible with today's FinFET transistor architecture production, which is limited by its current-carrying fin height. Therefore, while FinFET chips can scale to 5nm, simply reducing the amount of space between fins does not provide increased current flow for additional performance.

"Today's announcement continues the public-private model collaboration with IBM that is energizing SUNY-Polytechnic's, Albany's, and New York State's leadership and innovation in developing next generation technologies," said Dr. Bahgat Sammakia, Interim President, SUNY Polytechnic Institute. "We believe that enabling the first 5nm transistor is a significant milestone for the entire semiconductor industry as we continue to push beyond the limitations of our current capabilities. SUNY Poly's partnership with IBM and Empire State Development is a perfect example of how Industry, Government and Academia can successfully collaborate and have a broad and positive impact on society."

Part of IBM's \$3 billion, five-year investment in chip R&D (announced in 2014), the proof of nanosheet architecture scaling to a 5nm node continues IBM's legacy of historic contributions to silicon and semiconductor innovation. They include the invention or first implementation of the single cell DRAM, the Dennard Scaling Laws, chemically amplified photoresists, copper interconnect wiring, Silicon on Insulator, strained engineering, multi core microprocessors, immersion lithography, high speed SiGe, High-k gate dielectrics, embedded DRAM, 3D chip stacking and Air gap insulators.

#### Long-term IoT semiconductor, Continued from page 6

market for wearable systems is expected to show a CAGR of 17.1% (versus 18.8% in the previous projection). The lower growth projection in chip sales for connected cities systems is a result of anticipated belt tightening in government spending around the world and the slowing of smart meter installations now that the initial wave of deployments has ended in many countries. Slower growth in semiconductor sales for wearable systems is primarily related to IC Insights' reduced forecast for smartwatch shipments through 2020. The updated outlook nudges up semiconductor growth in the industrial Internet category to a CAGR of 24.1% (compared to 24.0% in the December 2016 forecast) and slightly lowers the annual rate of increase in connected homes and connected vehicles to CAGRs of 21.3% and 32.9%, respectively (from 22.7% and 33.1% in the original 2017 report). ◆

## 450mm equipment for WLCSPs?

On the eve of the formal ECTC presentations, the conference held a panel session pitting wafer processing vs panel processing for the low cost production of "high density" fan out WLP.

"In the left corner representing wafer processing are TSMC's Doug Yu and Nanium's (Amkor's) Stefan Krohnert and in the right corner representing panel processing are Deca's Tim Olsen and IZM Fraunhoffer's Rolf Aschenbrenner ... the referee for this match, representing user groups, is Qualcomm's Steve Bezuk.....Let's get ready to rumble..."

Basically the question is: if and when will panel processing tools be fully developed and capable of manufacturing and testing fine lines and spaces (i.e.,  $2\mu$ m) fan out packages produced in yields similar to silicon wafer lines. If/when this happens, how will silicon foundries counter such results?

Let's look at some of the key points made by the above parties during this hour plus discussion.

### Wafer processing

[Yu] InFO leverages his companies core business – i.e., silicon wafer processing

[Krohnert] capital for FOWLP is already depreciated whereas there are no panel level processing in place so new capital will have to be expended on newly developed equipment.

[Yu] Inspection of wafers is a well known process whereas panel inspection has to be developed

[Yu] technology must be face down so you can package chips of different heights (polish) Face up panel tech cannot do this. ...also passives cannot be thinned like chips can be.

[krohnert] a fully loaded high yield wafer line might be cheaper than a partially loaded low yield panel line" he went on to explain that if panel processes FOWLP only reached required yields for low-medium I/O devices there are other ways to manufacture such packages and the remaining "sweet spot" panel business may not be enough to fill panel lines.

[Yu] landed a solid right to the jaw of his opponents when asked about what the silicon foundry response will be if

### Packaging

indeed panel processing is developed and is yielding fine lines and spaces. His response was that TSMC is part



of the 450mm development team and although the equipment already developed and purchased by TSMC does not look like it will be processing leading edge node wafers any time soon, such tools and processes could easily be



PHIL GARROU, Contributing Editor

applied for  $1-2\mu m$  features. "This would be low hanging fruit for such tools and processes." Yu then indicated that a possible plan is to make such a move when they feel the panel processing is ready. He cautioned, though, that this will produce a major oversupply of capacity.

### The referee

[Bezuk] the main volume for WLFO is currently for 3-5mm pkgs

[Bezuk] InFO is currently the thinnest package you can buy today

[Bezuk] equipment for panels is being developed but having problems like shedding particles during startup which is affecting yield

[Bezuk] simple FOWLP like codec chips use a single layer of RDL, if multi layer RDL is required FOWLP becomes too costly

[Bezuk] materials costs for both technologies are  $\sim 50\%$  of the total.

### **Panel processing**

[Aschenbrenner] panel level processing shows a sweet spot for small-medium I/O devices

[Olsen] projects a 30% cost advantage for large panel processing

[Olsen] working with ASE on 300mm round today and panels in the future

[Aschenbrenner] agreed that panel processing cost reduction will only be achieved when yields are close to the same as for wafers

[Aschenbrenner] panels appear to need class 100 clean area to achieve yield on fine lines

[Olsen] agreed that panel equipment is taking a long time to "get clean"

The major new news item from this panel was certainly TSMC bringing up the potential use of 450mm wafer equipment which would continue to leverage their core business/technologies, if and when it is economically required. Was this shared insight or a clever bluff? ◆

## PCM + ReRAM = OUM as XPoint







**FIGURE 1.** XPoint PCM/OTS cross-section along bitline and wordline (Source: Intel 3D XPoint, TechInsights).

As a reminder, cross-bar ReRAM devices function by voltagedriven pulses creating resistance changes in some material. The cross-bars allow for reading and writing all the bits in a word-string in a manner similar to flash arrays.



In complete contrast, Phase Change Memory (PCM) cells—as

per the name—rely upon the change between crystalline and amorphous material phases to alter resistance. The standard way to change phases is with thermal energy from an integrated set of heater elements. The standard PCM architecture also requires one transistor for each memory cell in a manner similar to DRAM arrays.

Then we have the OUM variant of PCM as previously branded by Energy Conversion Devices (ECD) and affiliated shell-companies founded by tap-dancer-extraordinaire Stanford Ovshinsky. So-called "Ovonic" PCM cells see phase-changes driven by voltage pulses without separate heater elements, such that from a circuit architecture perspective they are cross-bar ReRAMs.

Ovshinsky et al. successfully sold this technology to the industry many times. In 2000, it was licensed to STMicroelectronics. Also in 2000, it was used to launch Ovonyx with Intel investment, at which time Intel said the technology would take a long time to commercialize. In 2005 Intel re-invested. Finally, in 2009, Intel and Numonyx showed a functional 64Mb XPoint test chip at IEDM.

In 2007, Ovonxyx licensed it to Hynix and Qimonda and others. All of those license obligations were absorbed by Micron when acquiring Ovonyx. ECD is still in bankruptcy.

So, years of R&D and JVs are behind the XPoint OptaneTM SSDs. They are cross-bar architecture ReRAM arrays of PCM materials, and had the term not been ruined by 17-years of over-promising and under-delivering they would likely have been called OUM chips. Many others tried and failed, but Intel/Micron finally figured out how to make commercial gigabit-scale cross-bar NVMs using OUM arrays. Now they just have to yield the profits... ◆

### Semiconductors



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## Laser debonding for ultrathin and stacked fan out packages

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an-out packaging is an established technology for many mobile applications. Whereas early semiconductor packages have been single-chip packages, the continuing trend of expanding the wiring surface to support increased functionality has led to more complex packages, stacked packages, systems in package as well as high-performance packages. With this development, fan-out technology is bridging a gap between cost-competitive packaging and high performance. For all aforementioned packages, temporary

bonding will be needed, either to enable the thinning of wafers to address the need for smaller form factors, to achieve cost savings on mold materials or to serve as a processing platform for redistribution-layer (RDL) first processes.

Temporary bonding requires both a bonding and debonding process. Determining the right debonding technology can be difficult and confusing as every application from fan-out wafer-level packaging

teristics fit well.

(FoWLP) to power devices has its

own requirements in terms of process

temperature, mechanical stress and thermal budget, to name just a few

considerations. In this article, we will

focus on laser debonding, where hightemperature compatible materials are available. We will point out for which

applications the laser debond charac-

To limit the thermal input associated

with debonding, UV lasers are utilized for debonding where several

materials from different temporary

Chip first Tape lamination of metal carrie RDL formation on temporary carrier Pick & place of dies Pick & place of dies Wafer level molding Wafer level molding Carrier removal/ debonding Carrier removal/ debonding Standard WLB process Singulation Singulation FIGURE 2. Chip last FoWLP

FIGURE 1. Chip first FoWLP manufacturing process.

### Chip last (RDL first)

bonding material suppliers are available. To confine the maintenance effort to a minimum, a diodepumped solid-state (DPSS) laser is the right choice in combination with beam-shaping optics for high process control and minimum heat input.

### **Challenges of temporary bonding** for FoWLP

FoWLP has gained significant industry interest in part due to

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manufacturing process.

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carrier, the requirements of the temporary bonding material in terms of chemical and thermal compatibility are high. Certain kinds of polyimides comply with this harsh environment and are also suitable for laser debonding.

By just comparing these two processes, the requirements differ significantly even though both are FoWLP processes. By looking at the wide variety of semiconductor processes for various applications, it becomes clear that no single debonding process solution is compatible with all semiconductor processes, but rather several solutions are necessary. This is the reason why a variety of debonding processes (temporary bonding is characterized by the debonding technology) have been developed and are still in use today.

### Comparison of the mainstream debonding technologies

The most common debonding methods are thermal slide-off debonding, mechanical debonding and UV laser debonding. These three methods are all in highvolume manufacturing and differ strongly in their process compatibility.

Thermal slide-off is a method that employs a thermoplastic material as an adhesive interlayer between the device and carrier wafer. The debonding method uses the reversible thermal behavior of the thermoplastic material, meaning that at elevated temperatures the material experiences a drop in viscosity, which enables debonding to be accomplished by simply sliding the wafers off of each other. The characteristics of thermal slide-off debonding is bonding and debonding at elevated temperatures, which depending on the thermoplastic material being used can range between 130 and 350°C. Temperature stability depends in large part on mechanical stress, which can be observed due to the thermoplastic's low viscosity at high temperatures [1].

Mechanical debonding is a method that is highly dependent on the surface properties of the wafers involved as well as the adhesion and cohesion of the temporary bonding material. For most material systems, a mechanical release layer is applied to achieve a controlled debonding mechanism. Key characteristics of mechanical debonding include processing at room temperature and a strong dependence on mechanical stress. Since mechanical debonding needs a low adhesion between the temporary bonding material and the wafer for a successful debond process, it can be tricky to use it for FoWLP applications. This is because the high wafer stress associated with FoWLP processing can lead to spontaneous debonding, even during the thinning process, which in turn can result in a drastic drop in yield [2].

Laser debonding is a technology that has been implemented with several different variations. The debond mechanism depends on the type of laser as well as the temporary bonding adhesive or the specific release layer used for the process. Infrared lasers work on the principle of the photo thermal process, where light is absorbed and transferred into heat, which leads to high temperatures within the bond interface. UV laser debonding typically uses the photo chemical process, where light is absorbed and the energy is used for breaking chemical bonds. Breaking the chemical bonds of a polymer results in the production of fragments of the original polymer. These fragments comprise gases, which increase the pressure within the interface to support the debonding process. For FoWLP applications, this method is a good fit due to the high adhesion of the temporary bonding adhesive to the wafers before the debonding process.

### **Optimized solution for FoWLP applications**

UV lasers are advantageous for FoWLP processing due to their limited thermal input through the debonding process. The carrier wafer must be transparent to the UV laser's wavelength to ensure efficient use of the laser energy and also ensure a higher lifetime of the carrier wafer. Two main types of UV lasers are available (solid-state laser and excimer laser), with each having several different wavelength options. Choosing a laser with a wavelength larger than 300nm



**FIGURE 3.** Conventional solid-state laser requiring high pulse overlap. The crisscross area indicates the radiant exposure used for the laser debond process while the red area indicates energy that cannot be used for debonding.

is optimal for several reasons. First, commercially available laser debond materials effectively absorb and therefore debond at wavelengths higher than 300nm. Second, it allows a standard glass wafer to be used as the carrier since glass enables high transmission in this wavelength regime.

Solid-state lasers have the advantage of lower maintenance costs because they do not need halogen gas, which must be replaced on a regular basis. For solid-state lasers, the consumables are very low, and depending on the amount of power used by the laser there are examples of lasers used for laser debonding on a 24/7 basis that have required no laser consumables in the first five years of operation. Additionally, a smaller footprint can also be achieved due to a compact optical setup. Solid-state lasers typically have Gaussian beam profiles, pictured in **FIGURE 3**.

UV laser debonding is a threshold process, meaning that debonding occurs above a certain value of radiant exposure. In Figure 3, the area with the blue crisscross lines indicates the radiant exposure, which is used for the debonding process. The energy that is below or above that value (areas in red in the picture) cannot be used for debonding and is typically transferred into heat, which can lead to carbonization and particle creation. Because of the lack of sufficient energy at the edge of the Gaussian laser beam profile, a certain overlap of the pulses is necessary, which is an additional variable that must be optimized in order to achieve successful debonding without carbonization. Additionally, the excess energy in the beam center can cause carbonization. A Gaussian beam profile is not suitable to limit thermal effects during debonding.

Gaussian beam profiles can be transferred into quasi top hat beam profiles by using a proprietary optical setup for beam shaping. By employing this optical setup, a highly reproducible beam for debonding (whereby the beam shape does not change over time) is achieved with constrained thermal input similar to what is seen in the "top hat" beam profile in **FIGURE 4**. This gives tighter process control, which in combination with the high pulse repetition rate of this laser type and the ability to scan across the surface of a fixed wafer leads to a wellcontrolled, high-throughput debonding process. The scanning process is pictured in **FIGURE 5** where -- in contrast to an excimer laser -- the wafer is fixed on a static stage and the laser spot is controlled by a galvo scanner over the wafer. leads to a well-controlled, highthroughput debonding process.

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**FIGURE 4.** Advanced UV laser solution combining high repetition rate scanning with efficient use of laser energy by using beam-shaping optics. The efficiency of the radiant exposure used for debonding is very high as noted by the large blue crisscross area.

As shown in **FIGURE 6**, a test wafer is used to determine the optimum radiant exposure for debonding. Even with a top hat beam profile, it is important to use a radiant exposure value close to the debonding threshold to minimize heat effects [3]. Small overlaps are necessary nonetheless because the adhesion between the temporary

bonding material and the wafers is very high.

### Temporary bonding for future FoWLP

Ultrathin and stacked fan-out packages, also Package called on package (PoP), are already on several industry roadmaps due to their ability to enable higher device densities. However, the need for reconstituted wafers to become even thinner for PoP versus current FoWLP will give rise to more challenges for temporary bonding. For example, the bow of the temporary bonded wafer



stack consisting of a molded wafer and a carrier wafer must be minimized to ensure uniform thinning. The

maximum total thickness variation (TTV) will also become tighter depending on the final thickness. As for every 3D application, questions regarding interconnects, such as choosing via first or via last, also arises for PoP, where several processes are also available and where no standard process exists that is employed by all fan-out packaging houses.

### Summary

UV laser debonding is a suitable method for both chipfirst and chip-last/RDL-first FoWLP processes because it offers debonding at room temperature, and because chemically stable materials are available. The UV laser debonding solutions presented in this article combine the advantages of the solid-state laser with low maintenance, low consumables costs and high pulse frequencies combined with high spatial control due to the special beam-shaping optics.

### **Further Readings**

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**FIGURE 5.** EVG laser debonding solution combining a solidstate laser with beam-shaping optics for high throughput and good process control.



**FIGURE 6.** Laser debonded test wafer. Individual tracks represent varying debonding fluence of the laser.

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## Overcoming challenges in 3D NAND volume manufacturing

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As 3D NAND becomes the mainstream technology, its challenging roadmap poses opportunities for continued innovation.

ince its introduction several years ago, 3D NAND has become a mainstream technology because of its ability to increase bit density in memory devices. Its adoption has been accelerated by advances in the underlying manufacturing processes that are enabling 3D architectures and lowering the cost per bit. With all its advantages, however, the overall complexity and capital intensity of 3D NAND manufacturing add significantly to the challenges fabs are facing in terms of process control, yield, and economics.

### Market and technology drivers for 3D NAND

The main impetus for 3D NAND was the recognition that

planar technology was approaching the end of its physical limits to deliver higher densities and a lower cost-per-bit. Past advances in conventional planar NAND technology have primarily been driven by physical scaling, where lithography capabilities determined just how many memory cells could fit within a given die size. Using multiple levels of charge within each cell by going from single- to multi-level cell designs has also enabled increased bit densities. However, these improvements typically have come at the expense of speed because of the need to differentiate between the multiple levels of charge. In addition, since the individual memory cells for these designs lie in a horizontal plane, scaling is still ultimately limited by lithography. Other challenges in scaling 2D NAND beyond the 15 nm node include cell-to-cell interference, unscalable dielectrics, and electron leakage [1].

To address these issues, 3D NAND fundamentally changes the scaling paradigm. Instead of traditional X-Y scaling in a horizontal plane, 3D NAND scales in the Z-direction by stacking multiple layers of NAND gates vertically. This allows more cells to be packed into the same X-Y space (planar area) on the die without shrinking dimensions horizontally. By easing cell size requirements, triple- and even quadruple-level cell designs are possible. As such, 3D NAND offers a significant increase in bit density over planar NAND.

Unlike planar NAND, where scaling is primarily driven by lithography, 3D NAND scaling is enabled by advances in deposition and etch processes. An incredible level of precision and repetition is required in defining complex



**FIGURE 1.** 3D NAND architecture showing some of the most challenging and critical deposition and etch processes.

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3D structures with extremely high aspect ratio (HAR) features. Achieving success with 3D NAND requires innovative deposition and etch solutions that minimize variability.

### **Overview of critical 3D NAND processes**

The 3D NAND architecture requires advanced capabilities enabling HAR and complex structures (**FIGURE 1**). Critical processes involved include multilayer stack deposition, HAR channel etch, wordline metallization, staircase etch, HAR slit etch, and stair contacts formation. The following sections look at some of these areas in more depth and describe the most critical process parameters that must be controlled.

### **Film deposition**

Creating stacked memory cells starts with depositing alternating layers of thin films. Unlike planar NAND, where cell pitch is defined by lithography, pitch in 3D NAND is determined by the film thickness. As such, precise control of layer-to-layer deposition uniformity is extremely important. Currently, commercial 3D NAND products in high-volume manufacturing have layers ranging from 32 to 48 pairs, while next-generation products with more than 60 pairs are now beginning high-volume ramps.

Critical requirements for depositing stacked films are the stress and uniformity of the individual layers within the overall stack. These requirements become more stringent and increasingly more challenging to meet as the number of layers grows. Wafer bow and local film stress (**FIGURE 2**) directly impact the ability to achieve precise lithography overlay. Film thickness and repeatability affects the active area of cell and consistency of the litho/etch performance. As a result, both film stress control and



**FIGURE 2.** As the number of layers increases in the 3D NAND device, the effect of film stress can become magnified.

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excellent uniformity are critical to wafer yields. To address these concerns, careful management of stress by tuning deposition conditions and optimizing integration is needed not only for the film stack deposition, but also throughout 3D NAND manufacturing.

### High aspect ratio channel etching

HAR channel etch is the most critical and challenging step in 3D NAND because it is key to achieving uniform hole size through multiple layers to define the channel of memory cells. More than a trillion holes must be etched simultaneously and uniformly on every wafer, each with an aspect ratio of more than 40:1. For comparison, the highest aspect ratio structure that is etched in planar NAND is less than 15:1.

Deep etch on these multilayer stacks can push the limits of physics to achieve uniformity from top to bottom. As shown in **FIGURE 3**, the high aspect ratio of this etch leads to transport limitation challenges that can generate a range of problems. These include incomplete etch wherein some holes don't reach the bottom, bowing, twisting, and CD variation between the top and bottom of the stack. Such defects can lead to shorts, interference between neighboring memory strings, and other performance issues. Solving these HAR-related transport issues requires precise control of high-energy ions during the etch process. Technologies that help deliver this capability include a symmetric chamber design for intrinsic uniformity, a proprietary high ion energy source with advanced plasma confinement and modulation, and orthogonal (independent) uniformity tuning knobs, such as multi-zone gas delivery and temperature control to achieve required uniformity across the wafer.







**FIGURE 4.** Low-fluorine tungsten ALD has demonstrated 100x lower fluorine versus CVD tungsten.

As the 3D NAND roadmap adds more layers to achieve higher bit density, channel hole etching becomes increasingly challenging due to higher aspect ratios. Managing the fundamental trade-offs among profile, selectivity, and CD requires continuous equipment innovation, not only to deliver HAR etching capabilities for more than 100 pairs, but also to do this at the productivity needed for volume manufacturing.

### Wordline tungsten metal fill

For replacement-gate 3D NAND schemes, wordline tungsten fill provides the critical conductive links between individual memory cells within layers. This process is particularly challenging because of the need to achieve void-free fill of complex, narrow, lateral structures with minimal stress on the memory stack.

Due to the structural complexity, atomic-scale engineering is required for wordline fill. Traditional

CVD tungsten films have inherent characteristics that limit capability for 3D NAND wordline fill. High tensile stress in CVD tungsten can lead to wafer bow, and fluorine in the process has been known to diffuse into adjacent layers where it can create yield-limiting defects. In addition, resistivity limits scaling: making each layer thinner would allow for more layers (more storage bits), but would also make wordline resistance too high. One approach to address these concerns is the use of a low-fluorine tungsten (LFW) ALD process. This has the ability to provide a smoother morphology that conforms better with the surface in each fill layer, thereby

minimizing stress induced by the deposition process. Stress reduction by more than an order of magnitude has been demonstrated with LFW ALD technology. This



**FIGURE 5.** Staircase etch uses repeated vertical etch and lateral trim etch passes to define the contact pads.

approach has also been shown to lower fluorine content by up to 100x (**FIGURE 4**) and reduce resistivity by over 30% compared to conventional CVD tungsten.

**Staircase etch** 

The staircase etch step creates the individual contact pads for each memory cell within the layers. A highly controlled etch process is used to define the size of each contact pad. To reduce the cost associated with lithography and improve productivity, repeated vertical etch and lateral trim etch processes are adopted to form the staircase instead of using numerous lithography steps. For each lithography pass, multiple staircase levels can be created by etching and trimming, as shown in **FIGURE 5**. The number of stairs that can be formed by this process is determined by the lateral-to-vertical (L/V) etch rate. Improving L/V etch selectivity can reduce the number of lithography steps needed.

Extreme accuracy is required to maintain the stair CD, thus avoiding misaligned contacts. If the CD for a pad is off by a few percent, that error will propagate through subsequent pads defined within the same lithography pass. Current technology can deliver uniform and repeatable stair CD precision of 1% (3-sigma) after more than five L/V trim processes. This is a critical factor for achieving high productivity and being able to scale to higher stacks with more layers economically.

### Summary

Traditional planar scaling to increase NAND density is approaching its limits due to lithography and performance challenges. As 3D NAND becomes the mainstream technology, its challenging roadmap poses opportunities for continued innovation. Stress management throughout wafer processing is crucial, and significant innovations in both deposition and etch processes are essential in forming the HAR features that dominate 3D NAND architectures. Finally, reducing variability in every critical step is a must to meet performance, yield, reliability, and cost requirements.

3D NAND completely changes the scaling paradigm by going vertical. No longer limited by lithography capabilities, 3D NAND can achieve greater levels of integrity, performance, and reliability – while building vertically for higher bit density and a lower cost-perbit – through relying on advances in deposition

and etch processes.

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METROLOGY

## In-line metrology for characterization and control of extreme wafer thinning of bonded wafers

M. LIEBENS, A. JOURDAIN, J. DE VOS, T. VANDEWEYER, A. MILLER, E. BEYNE, imec, Leuven, Belgium S. LI, G. BAST, M. STOERRING, S. HIEBERT, A. CROSS, KLA-Tencor Corporation, Milpitas, California

*In-line metrology methods used during extreme wafer thinning process pathfinding and development are introduced.* 

he pace of innovation in device packaging techniques has never been faster or more interesting as at the present time. Previously, data were sent through wires where in recent packages, components are connected directly using different 3D interconnect technologies. As the 3D interconnect density is increasing exponentially, pitches need to reduce to 5µm and below. Current interconnect technologies of 3D-SIC (3D-Stacked IC) do not offer such high densities. Parallel front-end of line wafer processing in combination with wafer-to-wafer (W2W) bonding and extreme wafer thinning steps in the 3D-SOC (3D System On Chip) integration technology schemes, as depicted in **FIGURE 1**, enable the increase of 3D interconnect density. achieve, for example, a stable via-last etch process with requirements to land on correct metal layers. Secondly, the thinning process may not induce damage on the top Si across the wafer and especially at the wafer edge which would directly impact the physical yield of the complete wafer stack. Finally, the wafer surface nanotopography (NT), shape and flatness need to be in control to ensure proper subsequent W2W bonding when going to multiwafer stacks beyond N=2. To allow us to achieve these challenging criteria the metrology systems used must cope with areas of the wafer previously deemed to be in the "minimal care zone" of 1 – 2mm from the wafer edge. The wafer edge characterization must also go hand in hand with patterned wafer topography after thinning to maximize physical wafer yield.



In this paper, the in-line metrology methods used during the extreme wafer thinning process pathfinding and development are introduced. These metrology tools supplied results

**FIGURE 1.** Illustration of a dielectric wafer-to-wafer bonding integration scheme for 3D-SOC applications. From left to right, top and bottom wafers are aligned, bonded, thinned and receive further processing, such as TSV (through silicon via) last etching, via, metal and RDL (re-distribution layers).

During the extreme wafer thinning process pathfinding and development, different thinning techniques like grinding, polishing and etching were evaluated in [1] and [2] to target a final Si thickness specification of  $5\mu$ m. For the comparison of the thinning techniques, multiple success criteria were defined to which the thinning process must initially comply. Firstly, the final Si thickness (FST) across the wafer needs to be within certain limits to that enabled us to determine where the extreme wafer thinning process can be improved. The same techniques can eventually be used to validate the improvements and to monitor process stability when processes are released for volume production.

### **Metrology methods**

Wafer Level Interferometry. For FST measurement and wafer surface shape and NT, a patterned wafer geometry system (KLA-Tencor's WaferSight<sup>™</sup> PWG) was used. This is a dual Fizeau interferometry system and simultaneously measures both the front surface and back surface height



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of patterned wafers at high spatial resolution. During the measurement, the wafer is supported in a vertical position to reduce any wafer distortion. The whole wafer acquisition is completed in a single shot allowing measurement of the front and back surface topography as well as wafer flatness and edge roll-off.

This tool is specifically designed for wafer geometry measurements with 1nm measurement precision and has previously been used to qualify the impact of wafer geometry on CMP in [3] and [4] and to determine the NT of a full wafer post CMP [5]. Using the device layout, the full-wafer NT map can be divided into individual dies and the range or peak-valley (PV) value can be the output for each individual die.

For this paper, the patterned wafer geometry (PWG) system is used to measure wafer thickness at multiple steps during W2W bonding and extreme wafer thinning to derive the final Si thickness of the top wafer after thinning. The thickness results as supplied by PWG is the relative height variation measured by interferometry, with respect to the local absolute wafer thickness measured by a capacitive sensor before the interferometry measurement is performed. The tool can supply 2D and 3D representations of the wafer thickness measurement at high spatial resolution as depicted in **FIGURE 2**.



**FIGURE 2.** Wafer stack thickness measurement represented in 3D (left) and 2D (right) color plot as measured after W2W bonding and extreme wafer thinning of the top wafer to 5µm.

Wafer Edge Inspection and Metrology. The all-surface wafer inspection and metrology system utilized (KLA-Tencor's CIRCL-AP<sup>™</sup>) contains an edge inspection module. This module uses: (1) a laser scanning setup revolving around the wafer bevel; and, (2) a lateral edge profile camera acquiring images of the wafer edge while the wafer is rotating. The laser scan comprises the laser, multi-channel optics and photodetectors/photomultiplier tube (PMT).

The lateral edge profile images are used to measure and quantify the edge shape and edge trim dimensions (see **FIGURE 3**). Based on the edge shape, an optimal trajectory of the revolving optics is calculated for profile-corrected



**FIGURE 3.** SEMI standard wafer edge shape (left) and lateral images of edge trim profile (right) that can be measured and controlled.

inspection to ensure proper incident of light on the wafer sample and to obtain good signal-to-noise ratio.

The revolving laser scanner is used to perform simultaneous edge inspection and metrology using brightfield, darkfield and phase-contrast modes to capture a broad range of wafer edge defect types with sensitivity down to  $0.5\mu$ m. Images are acquired in the different contrast modes from all zones comprising the wafer edge, i.e. top and bottom near-edge (5mm), top and bottom bevel, and apex. Part of a full wafer edge inspection image, including notch, is shown in **FIGURE 4**.



**FIGURE 4.** Part of a brightfield edge inspection image showing top and bottom near-edge (5mm), top and bottom bevel, and apex (notch can be noticed on the right side of the image).

Inspection is performed basically by comparing neighboring pixels on a tangential line. Pixels with a contrast or gray value difference exceeding a certain user-defined threshold are considered to be part of defects. Using rule-based binning techniques and by defining regions of interest and care areas, a high defect classification accuracy and purity of the defects of interest can be achieved by the implemented defect classification strategy.

Metrology is performed by detecting edge transitions on radial lines enabling characterization of coverage, concentricity and uniformity of layers, films or other line features on the wafer edge.

*Front Side Metrospection.* The all-surface wafer inspection and metrology system also contains a front side inspection module that uses: (1) time-delay-integration (TDI) technology with concurrent brightfield (BF) and darkfield (DF) inspection channels; (2) bright LED illumination





inspection detected edge chippings and classified them accordingly with high accuracy. The defect count of detected edge chippings on the wafer thinned by approach A was significantly higher than on the wafer thinned by approach B. The edge integrity was better maintained

**FIGURE 5.** An example of an interference signal detected by the front side inspection module of CIRCL-AP. The fringes are used to determine the Si-thickness at the edge of the wafers.

for precision and stability; and, (3) a set of recipe-selectable objectives to give different lateral resolutions.

The TDI camera detects an interference signal from the top and bottom surfaces of thinned Si. An example of such fringes is shown in **FIGURE 5**. The front side inspection module uses three illumination colors (RGB) that give three sets of interference signals, each has its own characteristic amplitude and frequency. By analyzing these signals, the Si thickness at the edge of the thinned wafer can be determined. The high resolution optics of the front side inspection module enables accurate thickness measurement when the edge rolls off rapidly.

### **Results**

*Edge Defectivity.* Using edge defect inspection and classification, it was possible to compare different wafer thinning process sequences with respect to grinding-induced damage, edge chipping and delamination, and to fine-tune the process by minimizing the defect count of these defects of interest.

**FIGURE 6** is showing the results from automated edge defect inspection of wafers which received two different thinning process sequences. By placing inspection care areas on the regions of interest, i.e. near the wafer edge of the top thinned wafer, and by specifying defect classification rules, the



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**FIGURE 6.** Edge defect inspection results to compare extreme wafer thinning process sequences. Thinning approach A (left) is showing higher defect count of edge chipping after thinning than approach B (right).

when wafers are thinned using approach B. The details of the process sequences can be found in [1].

When further exploring thinning approach B, a detailed edge inspection showed that the thinning process sequence induced a lateral shrinkage of the top wafer besides the normal wafer thinning, resulting in pattern exposure from the landing wafer as can be seen on the right inspection image of Fig. 6.

Global Wafer Thickness. The most important element in the extreme wafer thinning process is a precise control of the FST, and its variation, with a maximum  $3\sigma$  repeatability of 50nm to obtain a precision-to-tolerance ratio smaller than or equal to 0.1. The FST was measured by PWG and is the subtraction of the thickness measurement of the bottom wafer from the thickness measurement of the wafer stack after bonding and thinning, according to below equation.

$$FST(x, y) = #2(x, y) - #1(x, y) - 2 \times 0.59$$

The different components of this equation are depicted in **FIGURE 7**. Thickness #2(x,y) is the thickness of the total stack after W2W bonding and thinning. Thickness #1(x,y) is the thickness of the bottom wafer. Finally, to know the FST of the top wafer, the thickness of the dielectrics on top and bottom wafer are subtracted. The latter thickness is considered to be constant since the variation of the dielectric thickness is negligible compared to the variation of FST. **FIGURE 8** shows the thickness profile of the top Si layer after the thinning process sequence as measured by PWG. The FST varied about 2µm center-to-edge, with a strong gradient when approaching the wafer edge. Between wafer edge and 2mm from the wafer edge, it becomes challenging for standard wafer metrology tools to measure the thickness profile. Reasons are the wafer edge exclusion imposed by the tool and the non-opaque behavior of Si at a certain thickness in function of the wavelength applied by the metrology tool. The CIRCL-AP was used to investigate the edge profile of the top wafer to complete the full wafer characterization of the FST. Result details are elaborated in the following sections.



**FIGURE 7.** Cross-section of a permanent bonded wafer pair after extreme thinning of the top wafer. FST is the subtraction of the measured bottom wafer thickness and dielectric layers from the measured total stack thickness.



**FIGURE 8.** Top wafer FST profile along the wafer's X (blue) and Y (purple) axes. The FST varies about  $2\mu m$  center-to-edge, with a strong gradient when approaching the wafer edge.

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(metrospection) showed the thickness profile and

quantified the decrease as a function of wafer radius R

and angle  $\theta$  as depicted in **FIGURE 12**. There is a gradual

thickness decrease noticed from 3µm to 0µm indicating

The results of the PWG measurements showed a clear correlation with standard ellipsometry-based metrology measurements, as can be seen in **FIGURE 9**. The advantage of PWG over ellipsometry is that more points

on the wafer are measured at higher throughput and results are more reliable with the presence of patterns in the complex stack of 3D-SOC W2W bonded wafers.

*Edge Metrology.* For the wafer edge profile of the bonded wafer pair after thinning, it is expected to see a stepwise decrease of the FST of the top wafer due to the edge trim of the top wafer before bonding (**FIGURE 10**). However, the FST showed a slower decrease when approaching the wafer edge.

With the edge metrology function, CIRCL-AP was capable to detect and report from what radius the final Si thickness starts to decrease. as depicted in **FIGURE 11**. It is expected to see a uniform area of the top wafer top surface that extends to a radius of about 149.5mm, in case the top wafer received an edge trim width of 0.5mm. However, from radius 147.5mm, the FST started already to decrease towards the wafer edge. This decrease is the lateral shrinkage that was mentioned previously when discussing the results presented in Fig. 6.

*Edge Thickness.* The lateral shrinkage was further confirmed by detailed thickness measurements focusing on the wafer edge using the CIRCL-AP's front side inspection module. The inspection tool with metrology capabilities

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**FIGURE 9.** Correlation between PWG and standard ellipsometry-based metrology measurements.



**FIGURE 10.** Edge profile images of: (a) edge trimmed wafer on top of a bottom wafer before thinning; and, (b) after extreme wafer thinning. Image (c) shows the expected stepwise decrease (dashed line) of FST at edge trim, which was not noticed. Instead FST starts to decrease earlier (from blue dot) to zero FST (green dot).

that there is no Si left in a 2mm ring at the edge while the initial edge trim width was 0.5mm only.

### **Process improvement**

The FST profile and edge shape of the top wafer are characterized by using previously described metrology techniques. To enable a stable and robust via-last process and to realize multi-wafer stacking, the FST variation needs to decrease below 1 $\mu$ m and the lateral shrinkage needs to be minimized. The optimization of the wafer thinning process sequence is ongoing work by applying different hardware configurations, tuning the processes and validating whether requirements are met by using the same metrology techniques as described in this paper.



**FIGURE 11.** FST starts to decrease from radius 147.5mm (blue dots) to zero thickness around the edge trim width at radius 149.5mm (green dots).



**FIGURE 12.** Decrease of FST as a function of wafer radius R for different  $\theta$  angles. No Si was left in a 2mm ring at the edge while the initial edge trim width was at 0.5mm from the wafer edge.

### Conclusions

We have shown the capability of two complementary metrology tools to characterize the extreme wafer thinning process. This tool set can also be implemented to control the performance in a production environment at high throughput. Excursions can be analyzed further using techniques like in-line AFM. When thinning Si to  $5\mu$ m and below for 3D-SOC integration technology schemes, multiple challenges arise where different measurement techniques are needed to characterize the final Si thickness

**METROLOGY** 

across the full wafer. A good control of the final Si thickness as well as the total thickness variation (TTV) will become important when further scaling down 3D interconnects and increasing their density.  C. Mehanian et al., "Systems and Method for Simultaneously Inspecting a Specimen with Two Distinct Channels," US Patent 7,782,452, issued August 2010. ◆

### Acknowledgements

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VACUUM TECH

## Enhanced vacuum security using advanced sub-fab monitoring and data analytics

ERIK COLLART, Edwards, Sanborn, NY

Sub-Fab Fault Detection and Classification (FDC) software platforms collect, integrate and analyze operational data.

he ability to provide the reliable high-quality vacuum environment that most semiconductor manufacturing requires is an often and easily overlooked aspect of the whole fab process. The unexpected failure of a vacuum pump can bring significant disruption to the manufacturing process, potentially imposing a heavy penalty in lost productivity and scrapped product. The sub-fab, where vacuum and abatement systems are typically located and so named because it is located literally below the fab floor, has evolved dramatically over the years, from simply a location outside the fab in which to house supporting equipment, to an environment that is in many ways as sophisticated as the fab itself. Just as manufacturers have adopted advanced monitoring and data analytics to optimize fab operations, they are finding significant benefit in applying the same techniques to sub-fab operations. Sub-Fab Fault Detection and Classification (FDC) software platforms such as Edcentra, Edwards' newest equipment monitoring, data acquisition and analytics platform collect, integrate and analyze operational data from the sub-fab, providing a comprehensive solution to vacuum security.

#### The challenge of cost-effective innovation

The semiconductor industry faces many challenges, including the high pace of innovation and the need to constantly improve operational efficiencies, decrease costs, reduce adverse environmental impact and ensure the safety of personnel in the fab and residents of the surrounding community. Some of the ways these challenges have been met in the past no longer apply. For instance, although there is still device scaling in new technology nodes, the type of simple geometric device scaling driven by Constant-Field Scaling rules [1] – to drive innovation, improve efficiency and reduce costs per die - effectively ran out a decade ago.

Innovation has continued, though along very different lines, introducing ever more complex device architectures and increasing the use of exotic materials and manufacturing methods, such as epitaxial and atomic layer deposition. These innovations have all extended development time and time-to-market, driven up cost, reduced efficiency (lower yields, more frequent equipment preventive maintenance cycles) and brought new and higher environmental restrictions (stringent local, national and international regulations, as on CO<sub>2</sub> emissions) and safety challenges (toxic precursor materials and waste products). Delivering timely and cost-effective innovation is now a major issue for the semiconductor industry. In response to this challenge, manufacturers have recognized the strategic necessity of integrating and analyzing all the information available from their processes. These manufacturers are therefore starting to adopt an integrated fab data and information management approach that accounts for all the factors affecting time-to-market at the lowest possible costs. The sub-fab and associated support systems cannot be omitted from this approach.

#### The importance of vacuum

Most of the critical steps in a chip manufacturing process are conducted under high vacuum conditions and vacuum quality is one of the most important parameters in these process step. Vacuum quality is a combination of vacuum level and vacuum content. No vacuum is absolute, and there are always trace amounts of non-process gases present in

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process chambers that can have a major impact on the process, if not controlled.

and process downtime. Even in single wafer process, unplanned pump failure can cause significant losses as some process tools require days or weeks to requalify.

As any fab equipment or process engineer will tell

you, maintaining vacuum quality is so important that pumps are almost never shut off and process chambers are almost never brought to atmospheric pressure, even when idle for long periods of time. Maintenance activities on process chambers are performed, whenever possible, with minimal or no exposure to atmosphere. This is for a very good reason: once a chamber has been vented to atmosphere it may take a very long time to return it to the previous known-good-vacuum state, affecting equipment uptime and process yield.

The vacuum state can therefore affect wafer quality and overall fab costs through its effect on yield or through losses incurred as a result of unplanned vacuum failures during wafer processing. For example, insufficient vacuum levels or trace amounts (ppm level) of unintended gases, such as  $O_2$  or  $H_2O_2$ , in an ion implant process can greatly reduce the stability of high voltage power supplies, leading, in turn, to fluctuations in ion beam current, non-uniform implant conditions on the wafer, and ultimately to poor and non-reproducible wafer yields. A pump "crash" during a batch process that causes the scrap of an entire production batch-normally 125 wafers-is very costly in both direct product loss



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Fab managers face a difficult choice between the costs of vacuum failure and the costs of too frequent maintenance. Optimizing this choice is one area where sub-fab equipment monitoring and advanced analytics can make an important contribution. Most effective optimization occurs in an adaptive maintenance regime, where pump maintenance is performed in parallel to tool maintenance, thereby virtually eliminating vacuum pumps as a cause of lost tool time. Long prediction horizons are required for successful adaptive maintenance, enabling the longer PM intervals (months) typical of sub-fab equipment to be synchronised to the shorter PM intervals (weeks) of the fab process equipment. For this to happen, and thereby assuring sustained vacuum quality, additional types of sensors and improved predictive capabilities and time horizons will be needed. The remainder of this paper highlights Edwards' exploratory work on using mechanical vibration sensor data to obtain a reliable and long prediction horizon for mechanical failure modes [2].

### **Failure Prediction Using Vibrational Sensor Data**

Monitoring vibrations to assess the health of rotating machines has a long and successful history. Intrinsic bearings frequencies can be calculated from rotation speeds, and wear-generated perturbations to these frequencies can be detected to predict bearing failures and other mechanical failure modes. However, these existing methods do not translate well to a semiconductor environment where process-induced failure modes are more frequent. The sub-fab working environment also tends to be extremely noisy from a vibration spectrum perspective and the effects of process induced failure modes on standard vibration spectra are largely unknown.

We have developed a new method of unlocking key predictive information (Fault Detection or FD) from vibration data, based on a "fingerprinting" technique, which translates complex, noisy data into a single dynamic coefficient that can be compared easily with existing predictive maintenance parameters. Further vibrational sub-band analysis provides specific failure mode identification and root-cause analysis, thus providing a key fault classification (FC) capability. This method will be referred to as Vibration Indicator or VI from here on.

### **Results**

**FIGURE 1** shows an example of the power of VI to extend visibility of a catastrophic bearing failure in a fab working

environment. A departure of VI from zero indicates the emerging signature of mechanical bearings wear. The time horizon in this example is at least 60 days, providing extended visibility and increased process security.



**FIGURE 1.** 90 day sample data of a bearings failure in a fab environment. Data was not collected continuously.



**FIGURE 2.** Evolution of VI versus traditional pump parameters for a deposition failure mode on a production LP-CVD  $Si_3N_4$  deposition process. Key: VI (blue), DP Power (orange), DP end-cover T (green).



**FIGURE 3.** Accelerated lab testing of  $F_2$  corrosion induced mechanical failure mode. Key: Accumulated  $F_2$  flow (yellow); DP Power (orange): VI (blue and purple).

with large  $F_2$  gas flows injected into the vacuum

system and pump. The traditional power parameter

is completely insensitive to the  $F_2$  flow and resulting corrosion. The VI, by contrast, shows a linear corre-

A second fab-based production environment example, taken from an LP-CVD  $Si_{3}N_{4}$  batch deposition process and shown in **FIGURE 2**, illustrates the sensitivity and predictive power of VI compared to traditional

pump parameters: power and temperature. The ultimate cause of failure in this case was deposition-related. As can be seen, from day 60 onward changing conditions process caused a step-change in the temperature. The power curve develops patterns of spike behavior around day 120. Previously existing best-known-methods (BKM) for predictive maintenance, based on analysis of power and temperature data, can detect this emerging behavior using spikearea and frequency-based techniques, in this case with a time horizon of 40 days. The key observation in this example is that VI (blue curve) reacted immediately to an increased deposition of condensable materials, which led directly to an equipment failure 90 days later. The VI provided a time-tofailure horizon of 90 days (55% of observed pump life), more than double that of traditional parameters.

Accelerated lab testing provides further evidence of the extended time horizon VI affords. **FIGURE 3** shows the results of a lab-based accelerated fluorine  $(F_2)$  corrosion induced mechanical failure mode,



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**FIGURE 4.** RUL estimates from an accelerated bearings failure lab test using VI metric.

lation with total accumulated flow, providing both early detection and a measure of the severity of the developing problem.

A second lab-based test (not shown) investigated the effects of oil contaminants and again confirmed the ability of VI to detect and quantify failure modes inaccessible to established methods. As in the corrosion example, a linear correlation was found between accumulated contamination and VI, while power measurements proved to be completely insensitive to oil contamination levels.

These show that VI can significantly extend the time horizon of equipment failure modes, well beyond current predictive capabilities and into the regime where effective



**TABLE 1.** Time horizon, hit rate and false positives.

maintenance pooling and the resultant cost savings can be realized. Moreover, these results can be translated into precise RUL predictions using various parameter estimator techniques, complementing standard Weibull techniques. **Figure 4** shows the results of an accelerated bearings failure lab test for a dry pump, comparing VI and estimated RUL.

#### **Performance comparison**

Tables 1 and 2 compare and contrast VI performance with mainstream SPC-like control methods, such a single

parameter threshold monitoring and multi-variate analysis (BKMS-F), in terms of detection capability, sensitivity, prediction time horizon and hit rate vs. false positives. **Table 1** shows that VI considerably extends prediction time horizon and, based on data gathered to date for detectable results, has demonstrated a 100 percent hit rate with no false positives. From **table 2** we see that VI extends predictability to mechanical failures, has high sensitivity, and detects problems as soon as they begin.

### Summary and conclusions

The need for increased operational efficiency in semiconductor manufacturing is driving the development of smarter interconnected vacuum sub-systems and the adoption of integrated data and information management technologies. A case

	FAULT CONDITIONS				
	Mechanical	Process Induced			
	e.g. Bearings	Process Deposition	Pump Corrosion	Exhaust Blockage	Ingestion
			Detection Capability	y	
SPC	N	Y	Y	Y	N
BKM <sub>S-F</sub>	N	Y	Y	Y	Y
VI	Y	Y	Y	N	Y
			Sensitivity		
SPC		Can only detect critical conditions Very subject to noise			High risk of false alarms
BKM <sub>S-F</sub>		Can detect problems only when they have reached a near critical level			Can detect event but not infer severity
VI	As soon as physical change occurs			Can detect permanent	

**TABLE 2.** Fault conditions, improved detectability and sensitivity.

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study described the combined use of the EdCentra sub-fab information management system and an innovative approach to vibrational analysis. Compared to current main-stream methods, VI provided an extended, and in some cases unique, predictive maintenance capability for mechanical pump failures and a very high level of sensitivity. For the data gathered so far on detectable faults, the hit rate has been 100 percent, with no false positives. Finally, advanced analytics and VI considerably extended the prediction time horizon from weeks to months. Together with existing predictive algorithms and methodologies for pumps, abatement and ancillary equipment, the capabilities provided by advanced information management and innovative monitoring technologies like VI have the potential to significantly reduce costs and increase productivity.

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ΙΟΤ

For an increasing number of designs, companies are finding it beneficial to design their own ASICs with system-on-achip (SoC) complexity. For reasons of cost reduction, quality improvement, IP protection and security, a full turn-key ASIC can be achieved for \$1-5 million, particularly if the design can be built using mature technology nodes.

To further explore this topic, we asked questions from three leading experts in the field. Participating in the Q&A are:

- Michel Villemain, CEO, Presto Engineering, Inc.
- Guillaume Etorre, VP Engineering, Devialet
- Venkata Simhadri, CEO, Gigacom Semiconductor

**Q:** What is the decision-making process for determining which applications are best addressed with an ASIC vs standard, off-the-shelf components? How does one calculate non-recurring engineering (NRE) costs, for example, and how does the anticipated part volume impact the decision?



Guillaume Etorre, VP Engineering, Devialet

**Etorre:** In many cases, particularly for IoT or other space-constrained designs, going with multiple standard components is simply not an option. A single chip must embed the microcontrollers, sensors, battery management system, radios, etc. required by the application, in the smallest possible form factor.

When space is available, a standard component approach can be more appropriate to meet tight deadlines or to address situations where demand for the product is unproven. It can also serve as a stop-gap to serve the market immediately while a lower-cost ASIC solution is being designed. If demand for the product is proven, a net present value calculation over a range of scenarios (best, typ., worst case for volumes and schedule for instance) will provide guidance on the best approach. An ASIC typically carries higher NRE (design, tapeout, qualification, test) but yields lower unit cost than an off-the-shelf solution. Depending on anticipated volumes and cost of capital, the lower unit cost of an ASIC will outweigh the higher NRE.



Venkata Simhadri, CEO, Gigacom Semiconductor

**Simhadri:** Primarily two factors can impact a company's decision to design its own ASIC.

1. Competitive advantage – If the company is building its system using off-theshelf components, competition can quickly reproduce it and you are only left with software as the differentiating factor. In this situation, you must have your own ASIC to protect your IP.

2. Cost – When addressing large volume markets the unit cost becomes an important factor and the only way to cut down the cost is to integrate/optimize the off-the-shelf components.

The typical NRE cost includes the cost of design, prototyping (shuttle) and qualifying the part. Companies typically use a few benchmarks to justify the upfront cost.

For example, NRE cost is primarily dependent on the infrastructure (staff and tools) the customer already has in place. If the company already has a design team, EDA tools, etc. then the incremental cost might not be too high. However, without a design infrastructure already in place, it's going to be a lot more timeconsuming and costly. In this case, it is much easier to work with an ASIC design house to have all the infrastructure and some of the building blocks put in place.

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Michel Villemain, CEO, Presto Engineering, Inc.

Villemain: NRE is somewhat challenging to calculate since the duration of the project is often underestimated and unpredicted issues (who really does anticipate them!) bring additional cost to such a project. One way of mitigating this is to use external sources provided on (primarily) fixedcost engagements. Beside ROI on NRE (function of margins and volume, indeed), drivers for using ASICs include: form factor, reliability, IP, power consumption and security.

**Q:** What are the tools and supply chain partners needed to successfully design an ASIC solution, including EDA software, foundry, packaging and test house?

**Simhadri:** You need the standard EDA tools for both Analog/ Digital, if you are designing a mixed-signal chip. Typically, you will have to work with at least two EDA vendors, such as Synopsys, Cadence, or Mentor Graphics. Many of the foundries will also work with small companies, provided you show a path to volume. However, in terms of design support (pdks, libraries, etc) foundries with better design infrastructure can save significant time. If you are a start-up or doing it for the first time, it can be quite daunting to setup the relationships and you can lose quite a bit of time to get the process going. But there are ways to save time and cost by outsourcing some of the work to the right design companies and echo system partners.

**Villemain:** Success is a function of a combination of multiple competencies that need to work coherently throughout the life of the product, especially post-design: industrialization, supplier management, quality, planning, logistics and product sustaining. This typically represents more than ten different skillsets that need to be part of the extended product team.

### **Etorre**:

- Availability of proven IP (CPU, peripherals, interconnects, digital & analog I/O,...) for the chosen technology node.
- Affordable EDA software, with specific packages for companies designing only one or two chips at any given time, for specific end-user products vs. fabless

IC companies which can spread the EDA license cost over many different chip designs every year.

• Efficient turn-key supply chain partner that can abstract out the complexity of foundry, packaging, test, storage and logistics for companies that lack critical mass.

**Q:** With the rise of IoT, IIoT and wearables, there's much interest in analog/mixed-signal ASICs. How are their requirements different from traditional digital designs?

**Villemain:** Analog/RF designs tend to be smaller in size and to require less aggressive wafer fab processes. From a design standpoint, they demand less expensive EDA tools and less costly verification. However, their characterization and test is typically more complex and requires more expertise than a purely digital equivalent. Finally, yield management can be more demanding as the equation design window vs. process window is left more to the engineers than digital products, which can use semi-automated tools.

**Simhadri:** The primary difference in the requirements is power and connectivity. If the ASICs must be connected to the internet, determining which protocols you need to incorporate on to the chip makes a big difference. Power is going to be a huge differentiating factor for the wearables, and designers are looking at various power saving techniques in an effort to optimize the power. Also, the foundries are offering special process nodes like SOI to address these markets.

In addition to the standard low power techniques like voltage islands and power shut off modes, the ASIC can further optimize the power by customizing the IP blocks for the specific applications. For, example, serial interfaces that burn lot of power, can be optimized.

### **Etorre:**

- Design cycle is longer for analog IP than for digital.
  - It is therefore critical to choose a foundry and a node for which all or most of the required IP are available.
- Analog IP is typically not portable between foundries or between nodes without significant rework.

- Custom analog IP is therefore a significant investment that will be depreciated if a foundry change or node change is required.
- The best nodes for analog, MEMS, RF, highvoltage and digital are usually not the same.
  - Selecting the most appropriate node for the applications is not a trivial task.
  - Introducing new functionality in a subsequent version of an ASIC can require a node change and therefore major redesign of analog / mixed signal circuits. Anticipating future requirements can help make better technology choices.

**Q:** How do mask set costs of more mature technologies (180-40nm node) compare with those of 28nm and below, and how do mask costs enter into the overall cost equation?

**Simhadri:** I strongly advise our customers to use shuttles to prototype the ASIC and completely qualify it before spending a huge amount on the full mask. As expected, the 180-40nm shuttle costs are significantly lower than 28/16nm.

**Villemain:** With verification being less of a factor for analog/RF designs, mask sets can become a significant part of NRE below 90nm. Process technology is obviously a leading factor, but in addition, process routes can be costly because of additional options or IP, implying the addition of a mask/process layer, and thus, decreasing ROI in smaller geometries. Also, cost plateaus do exist (depending on the foundries) due to equipment transition (wafer size, lithography technologies, etc.)

**Etorre:** The mask cost ratio between older technologies and more recent ones can reach 20:1. For a 180nm design, once design, qualification and test fixtures are factored in, mask cost is not a significant contributor to the overall NRE.

**Q:** Out of the various advantages of ASIC design -cost reduction, quality improvement, IP protection and security – how would you rank their importance. Are there other advantages to ASIC solutions?

**Villemain:** What we see in the industry is a combination of those factors (cost reduction, quality

improvement, IP protection and security) as a function of the market our customers are operating in. The most common drive is, of course, that of cost (ASICs usually bring a dramatic product cost reduction), although for infrastructure applications, reliability is a key criterion, while for battery-operated applications, power consumption reduction is mandatory and all are benefits of using an ASIC.

In addition, more and more IoT segments require security in order to be even just a contender in the market, and an ASIC-based solution offers both a certifiable source of design and a cost benefit as compared to standalone secured elements.

Finally, in very competitive markets, the IP differentiation that an ASIC provides is a huge benefit.

**Simhadri:** IP protection and security shall rank first, followed by cost reduction. In some cases, off-the-shelf chips may not meet the performance requirements.

### **Etorre:**

- Real estate savings an ASIC-based design is much smaller than an off-the-shelf approach;
- 2. Cost reduction
- 3. IP protection
- 4. Quality improvement, if any combining various functions and technologies (analog, digital, RF, power, MEMS, etc.) on the same die can lead to lesser quality.

**Q:** How has your company benefitted from an ASIC approach?

**Etorre:** Devialet's Analog-Digital Hybrid (ADH) audio amplification technology was first implemented with discrete components. This discrete design is used in our high-end Expert Pro amplifiers and it supports the widest range of operating conditions.

In our Phantom speakers, we had to fit the same technology is a much smaller area. We specialized the analog circuit for the specific speaker drivers used in the Phantom and we designed an ASIC to deal with the analog part of the ADH technology.

**Simhadri:** Gigacom has been working with a company in the industrial IoT space and building systems for sensing gases and air quality. We have worked together



to architect an ASIC that replaces the discrete components in the system, which can reduce the BOM by 10x and reduce the area and power significantly at the same time.

**Q:** How has the supply chain evolved to meet this new kind of demand?

**Villemain:** The supply chain needs to evolve in order to focus more on the backend than the frontend. If SoC brought RFCMOS to mass adoption with connected product, IoT, relying on a sensor-specific package, must integrate a companion ASIC driver and a transceiver; System in Package back-end technologies are gaining tremendous momentum. More and more companies will design their own ASICs, on well-proven, stable fab processes. However, packaging, reliability, test and security will become prime drivers, defining not only product costs, but also the ability to ramp, yield and scale up in volume. Supply chains (and especially the management of supply chains) is evolving accordingly.

For example, until recently, building an ASIC for an IoT device required the assembly of a team of experts, each with expertise in a different part of the process. The design might be created in-house or through an outside firm, and large companies, like automotive manufacturers, might assemble whole organizations, often called "operations" departments, with the sole task of managing the production of the specialized devices they needed. For a small company, with a game-changing new product idea, the cost and delay of assembling such a team can be fatal. If a competitor beats you to market you might not get a second chance. This need for manufacturing expertise led to the creation of "outsourced operations" companies, like Presto Engineering, that can manage the entire semiconductor manufacturing process from the completion of the design to the delivery of the tested product. By reducing the risk, cost, and difficulty of the production process, companies, such as Presto, are playing a key role in accelerating the proliferation of application specific semiconductor solutions.

**Etorre:** By design, ASICs run in lower volumes that standard parts. The supply chain must adapt to deal with more customers running lower volumes. This creates an opportunity for companies providing turn-key supply chain services to bridge the gap between numerous mid-volume customers and traditional foundries and packaging houses who only address the largest fabless IC vendors.

**Simhadri:** The supply chain needs some improvements in the following areas. The older process nodes from 180nm to 40nm have suddenly become popular for IoT applications. However, most of the PDKs and other collateral were developed for older EDA tool versions and they need to be updated. Also, most of the IP vendors are targeting their resources for developing the IP for the latest process nodes where they get the best returns on their investment. Some of this IP has to be ported back to enable the ASICs in older nodes.

Also, to bring up these ASICs, the industry needs good support for packaging and testing facilities and all the top vendors are focused on high volume and leading-edge ASICs. Companies like Presto can potentially fill the needs.  $\diamond$ 

## NASA's new vacuumchannel nanoelectronics rely on Park Systems AFM

MARK ANDREWS, Park Systems, Santa Clara, CA

Using scanning capacitance microscopy with a Park Systems atomic force microscope a team at NASA successfully characterized both the spatial variations in capacitance as well as the topography of vacuum-channel nanoelectronic transistors.

magine the not-too-distant future when a NASA spacecraft edges silently into orbit around Mars. Its 473-million-mile journey included a trip around the sun to sling shot itself into in geosynchronous orbit. Its mission: gather new site-specific details and deploy a rover as preludes to the first human mission to the red planet. But before anyone can take 'one giant leap', the Mars Path Marker needs to supply fresh data to anxious scientists back on earth. The probe cost \$1.8 billion. Its planning, construction and flight time to Mars took eight years and thousands of work hours from all across the aerospace supply chain.

Red lights are now flashing all across screens back on earth at NASA's Jet Propulsion Laboratory in Pasadena, California. The probe remains inactive while its earthside controllers grow frantic. Path Marker should have automatically powered-up for its first mapping transit, but instead hangs quietly above the ruddy Martian landscape.



Unbeknownst to controllers on earth, Path Marker wasn't responding because of a short-circuit 'latch-up' in its silicon processors. Communications won't resume for now—maybe not ever.

Earth could not see it happen, but when Path Marker flew around Sol, its passage coincided with an unusually large solar flare on the backside of oursun. More energy than what usually strikes Mars in six months was released in a series of coronal explosions, sending cascades of lethal, heavy ions plowing through Path Marker's delicate solidstate transistors as if its shielding wasn't even there.

Despite the best of plans, precautions and preparations, thisspacecraftis stuck in perpetual 'neutral.' Mission specialistsare trying all availablemission-saving workarounds, but only time will tell.

NASA researcher Dr. Jin-Woo Han hopes to prevent a critical failure in an important mission like this fictional account of the Mars Path Marker. In reality NASA has experienced all types of solid-state electronic failures during its decades of manned and robotic explorations. In his work, Dr. Han documented nine different types of failures in 17 named missions as well as many more that did not cause a mission failure, but impeded or slowed a program.

Although the Mars Path Marker mission is fictional, the need for a better semiconductor technology for deep space exploration is very real. That need is why Dr. Han and colleagues have placed hope in a new approach to solid state transistors that utilizessome of the same principles that gave vacuum tubes their role in humanity's first electronic products more than 100 years ago.

Han is a scientist at NASA's Ames Research Center for Nanotechnology in Moffett Field, California. The center is led by Dr. Meyya Meyyappan; Dr. Han leads the vacuum device research team within the 20-person organization. One of his most recent research efforts is tied to his theories and practical applications that leverage the advantages of vacuum for creating better electron flow, but without the drawbacks in existing solid-state technology that NASA frequently faces. The new transistors, called vacuum-channel nanoelectronic devices, are not prone to disruption by cosmic radiation, solar flares, radical temperature changes or similar dangers that can be encountered once a spacecraft (or humans) leave earth's magnetic fields and dense atmosphere.

The challenges of space exploration are daunting. While loss of life tops many potentially egregious outcomes,

damage to spacecraft instruments occurs much more commonly than the general public may realize. This damage remains a source of concentrated research and engineering efforts to mitigate and remedy problems that can lead to lack-luster performance or full system failures. The efforts to ensure safe and productive operation in satellites, probes and spacecraft is second only to the agency's zeal for keeping human space flight safe.

How can early 20th century vacuum tube technology solve NASA's very 21st century problems? First of all, the vacuum nanotechnology that NASA is developing is generations beyond conventional vacuum tube engineering as it stood in the early 20th century. But vacuum-channel nanostructures and conventional vacuum tubes share essential functional similarities that make Dr. Han's devices ideal candidates to replace today's most robust silicon-based transistors.

Transistors enjoy their role in electronic technology because of their unique abilities to amplify and switch electronic signals as well as electrical power. Power or current applied to one set of terminals controls the current as it flows to another terminal pair (emitters/ collectors). And while a practical solid-state transistor was proposed in 1926 by Canadian researchers, materials science only matured enough for production in 1947; the landmark year in which researchers at the AT&T Bell Labs (New Jersey, USA), and independently a year later in France proposed designs that would become the forefathers of today's microelectronic wonders.

Practical vacuum tube components came into play before 1910, and have several important advantages compared to solid-state transistors including their superior electron mobility. Like their solid-state cousins, tube transistors function by moving electrons unidirectionally from the emitter (a cathode) to be collected by the anode across a vacuum. Tubes fell out of favor for most low and medium power applications due to the advantages of solid-state construction including much smaller size and weight, ruggedness that exceeded old-style tubes, their aggregation ability that enabled today's integrated circuits (ICs), and zero warm-up time – silicon transistors requireno cathode warming function. Solid-state devices also provide substantially greater electrical current efficiency.

It's easy to see why solid-state electronics won a place in aerospace engineering. But once we actually got into space, we learned quickly that even robust silicon transistors were no match for deep space radiation. To make the best transistors that we had "good enough" for space, NASA mastered the process of creating

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backup systems and a host of other measures to keep missions on track. It alsopartnered with other agencies like DARPA (Defense Advanced Research Projects Agency) and the US Department of Defense to develop alternate technologies such as gallium arsenide (GaAs), gallium nitride (GaN), and the latest work from Dr. Han's nanotech vacuum team. GaAs and GaN are much



more robust than silicon, but decades of research have proven them less suitable for construction complex ICs than silicon.

Although conventional solid-state transistors enjoy clear advantages in terrestrial applications, in-space damage typically comes in three forms: instantaneous, cumulative and catastrophic. While the first two effects can frequently be worked around due to NASA's extensive reliance on back-up systems, catastrophic effects can be "mission enders."

**FIGURE 1.** The most promising material and design combination is a GAA nanowire in a vacuum gate dielectric.

Dealing with likely and possible performance disruptions costs NASA dearly in terms of extra weight, design time to createmultiple backup systems that can also complicate missions whileconsuming valuable payload space. Imagine if using a laptop computer on earth required double or even triple the amount of vital components—that laptop would easily be a third larger and more expensive. For NASA, ignoring risks will impede success or in worst-case situations lead to a disaster that

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**FIGURE 2.** New transistor technology had to be manufacturable at industrial scale using existing processes and techniques.

costs millions and could even endanger lives if components weretied to a human spaceflight mission.

A common way to deal with these unknowns is to overbuild—create more circuit pathways or entire redundant subsystems because some components will almost certainly be "sacrificed" during encounters with space radiation. NASA frequently must opt for "acceptable" performance instead of what might ideally be possible simply because they cannot count of systems that have optimal performance will remain that way throughout an entire mission.

The advantage a controlled vacuum has in transistors is tied to the fact that solid-state devices can experience long-term failures resulting from additive and cumulative effects from multiple bombardments of ionizing radiation that destroys device features at nanometer scale. This most commonly occurs when the total ionizing dose causes gradual parametric shifts, resulting in on-state current reductions and an increase in off-stage current leakage. A vacuum-based device does not typically suffer from these same effects in part because the absence of material (gases or solids) in the space between emitters and collectors not only speeds the flow of electrons but in essence is protective because there is very little present in this tiny void that might be damaged by ionizing radiation.

Dr. Han's team studied several different compounds and structures that could be utilized to construct the vacuum channel nano devices that would eventually prove likely successors to conventional transistors. These materials included bulk MOS, silicon-on-insulator (SOI), gate-allaround (GAA) MOSFET and what proved to be the most promising material and design combination, a GAA nanowire in a vacuum gate dielectric (**FIGURE 1**).

To be effective and meet NASA's requirements, new transistor technology had to be manufacturable at industrial scale using existing processes and techniques common to conventional silicon fabs or similar infrastructure. The ideal design would bring the "best of both worlds" together for a solution that is electrically sound, practical and compact as well as lightweight and reliable in the face of exposure to radiation and radical temperature fluctuations.

"But we did not ever approach this as a replacement for all silicon electronics or silicon transistors at large," said Dr. Han. "While the devices could easily be used on earth—that is where we tested them in gamma radiation chambers after all—but the cost efficiencies of regular silicon MOSFET could not very likely improved by our vacuum-channel nanoelectronic designs."

To measure device performance Dr. Han and his team employed a Scanning Capacitance Microscope (SCM) with an Atomic Force Microscope (AFM) from Park Systems. They investigated the nanoscale properties of vacuumchannel devices, seeking to ascertain their viability as a transistor while also observing if fabrication methodology for gate insulators can be controlled.

"SCM with AFM is a powerful combination for investigating transistor devices—together, the two methods provide the user with a non-destructive process of characterizing both charge distribution and surface topography with high spatial resolution and sensitivity," said Byong Kim, Analytical Systems Director, Park Systems.



**FIGURE 3.** Contact mode AFM topography image of the vacuum-channel device's source-drain interface. The overlaid red line corresponds to the topography line profile displayed in Figure 4. Scan size: 450 x 800 nm.



**FIGURE 4.** Line profiles of the AFM topography (red, left y-axis in nm) and the capacitance data (green, right y-axis in  $\mu$ V) of the device area scanned in Figures 3 and 5.

Kim explained that atomic force microscopy with SCM is ideal for investigating transistor designs at the nano scale. Together, the two methods provide researchers with non-destructive processes for characterizing both charge distribution and surface topography with high spatial resolution and sensitivity. In SCM, a metal probe tip and a highly sensitive capacitance sensor augment standard AFM hardware. During testing, voltage is applied between the probe tip and the sample surface. This creates a pair of capacitors in series (when examining metal-oxide-semiconductor devices) from the insulating oxide layer on the device surface and the active depletion layer at the interfacial region located between the oxide layer and doped silicon. Total capacitance is then determined by the thicknesses of the oxide layer as well as the depletion layer, which is influenced by the level of silicon substrate dopingas well as the amount of DC voltage being applied between the tip and device's surface.

Dr. Han reported that by utilizing scanning capacitance microscopy with a Park Systems atomic force microscope the team successfully characterized both the spatial variations in capacitance as well as the topography of his vacuum-channel nanoelectronic transistors. By examining the line profiles of the topography and capacitance data acquired down an identical path along the device's source-drain interface, further insight was gained into the relationship between key physical structures and recorded changes in capacitance.

The nanoelectronic device's topography (at the sourcedrain interface) was imaged and revealed a vacuumchannel spanning 250 nm in length with peaks and valleys separated by a distance of approximately 5 nm (**FIGURES 3-5**). The electrical functionality of the device was assessed through the acquisition of a capacitance map.



**FIGURE 5.** An SCM capacitance image of the region containing the device's source-drain in-terface. Brighter colors correspond to relatively more positively charged areas on the device whereas darker colors correspond to relatively more negatively charged areas. The overlaid green line corresponds to the capacitance line profile displayed in Figure 4. Scan size: 450 x 800 nm.

This map revealed a relatively negatively charged (-1.4 to -1.8 $\mu$ V) source-drain terminal and adjacent quantum dot followed by a relatively positively charged vacuum-channel (2 $\mu$ V) and another dot-terminal structure (-1.4 to -1.8 $\mu$ V) on the other end of the source-drain interface. This alternating series of capacitance changes at key structural points suggest that the device is fully capable of functioning as an effective transistor.

NASA is now working towards next steps to investigate the potential of producing vacuum-channel nanoelectronic devices in higher volumes for further study. The team utilized standard semiconductor manufacturing techniques, so while fabrication is within existing process and materials technologies, settling on the ideal material for the transistors is also still being investigated.

"While the work initially focused on silicon as an underlying technology, we next want to explore silicon carbide and graphene as alternatives—technologies that are more robust. Also, the charge emission efficiency of silicon may not be sufficient and we saw some degradation due to oxidization," he remarked. "While we have demonstrated that a silicon vacuum-channel nanoelectronic device is possible. We now need to look at better emitter efficiency and reliability, balanced against ease of manufacturing – everything is a tradeoff in some regards."

The Ames Research Center is open to partnering through industrial and university collaboration, like the work it has done in conjunction with Park Systems. NASA is already working with additional industrial partners and welcomes further collaboration.

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