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JUNE 2012

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Insights for Electronics Manufacturing

The Next Transistor P. 13

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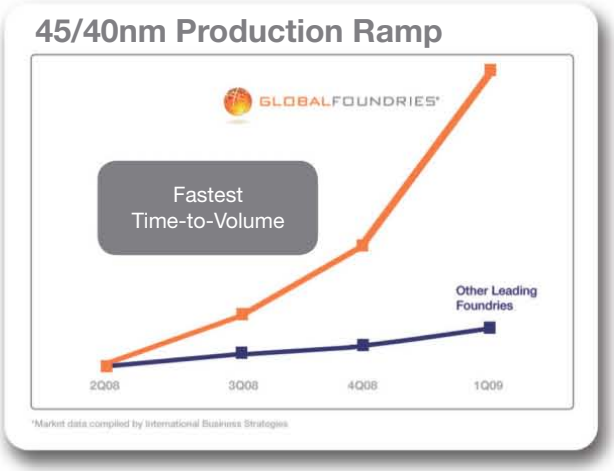
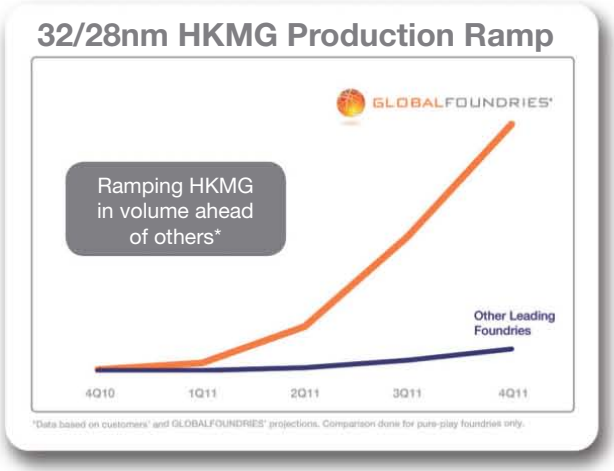
LEADING THE FOUNDRY RAMP IN 32/28nm WAFER PRODUCTION

GLOBALFOUNDRIES has shipped >250,000 32/28nm HKMG wafers to date. This milestone represents a significant lead over other foundries in 32/28nm manufacturing.





On a unit basis, cumulative **32/28nm shipments** for the first five quarters of wafer production are **more than double that achieved during the same period of the 45/40nm technology node ramp**, demonstrating that the overall HKMG ramp has significantly outpaced the 45/40nm ramp.

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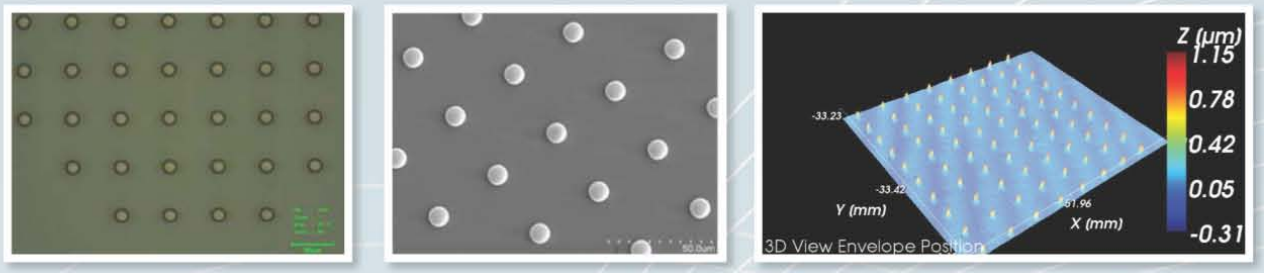
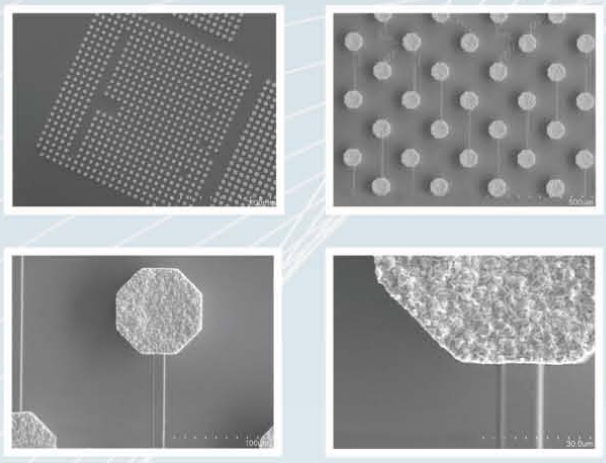
Si ETCH TO REVEAL Cu TSV

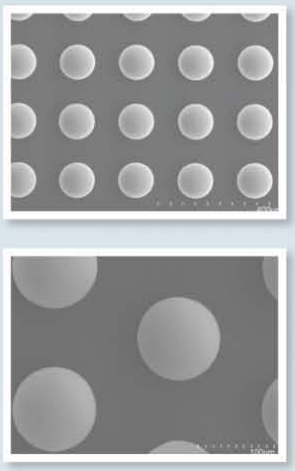


Optical | SEM | ISIS 3D

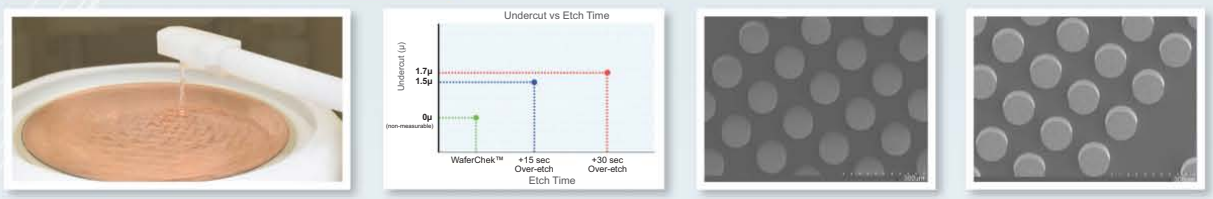
DRY FILM STRIP



FLUX CLEANING



UBM AND RDL METAL ETCH



UBM Post Etch | UBM Post Strip

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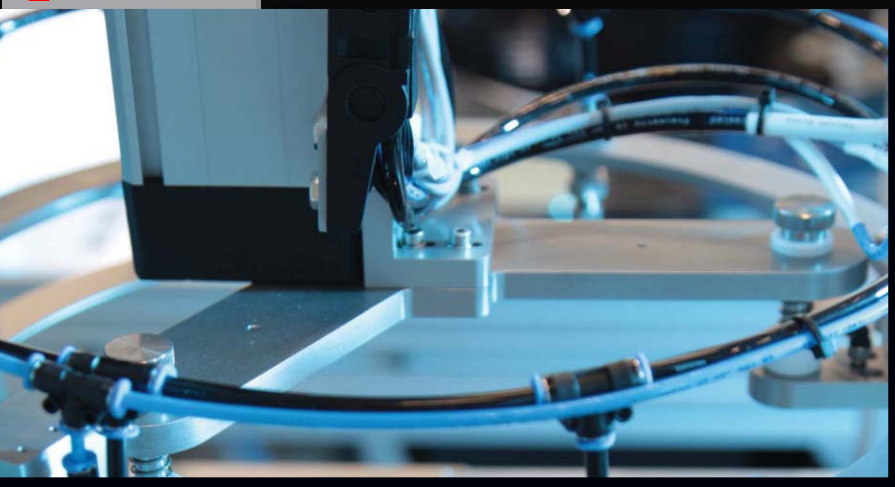

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Loading station of integrated film frame mounter in an EVG 850DB automated debonding system.

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Web Exclusives

Improving HB-LED economics

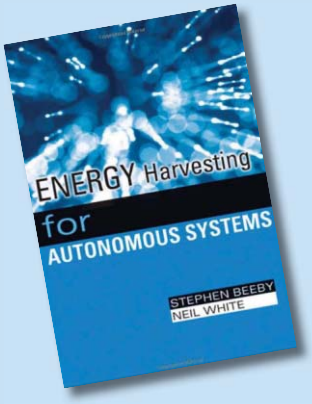
SEMI's Paula Doe covers the "commodity market" of LEDs, including capacity utilization at LED fabs, automation in manufacturing that could improve yields, LEDs fabbed on silicon and GaN instead of sapphire wafers, and more. **http://bit.ly/KNWhLx**

MEI wet process tools built to prevent contamination

MEI uses Vycom Flametec PVC-C for chemical rinse tanks and other wafer-contacting elements of its process tools, reducing tool-based contamination and protecting fab workers. Bill McGinty, MEI operations manager, discusses the benefits the new-generation plastic for semiconductor fab tools. **http://bit.ly/lwq2jz**

Book review:

Energy Harvesting for Autonomous Systems



Contributing editor Steve Groothuis reviews a book titled "Energy Harvesting for Autonomous Systems (Smart Materials, Structures, and Systems)" by Stephen Beeby (Author, Editor), and Neil White (Editor). The book highlights the progression from the basic principles behind energy harvesting to the comprehensive systems that control the sensing, actuation, and transmission of those devices. **http://bit.ly/JAE331**

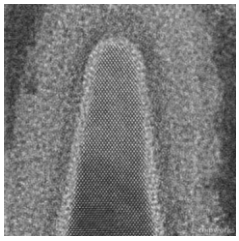
OLED makers develop new color patterning tech

OLEDs are gaining adopters in small screen sizes, and just moving into large-size displays. Mass production color-patterning technology for large-area OLED is increasingly an issue. Displaybank looks at new technologies under development at major display makers. **http://bit.ly/J3PXOl**

n&b news and blogs

Intel's 22nm trigate transistors exposed

When Intel held its Q1 results call, the company said that the 22-nm Ivy Bridge parts would make up 25% of their shipment volume in Q2. Blogger Dick James, Chipworks, managed to track some down: Xeon E3-1230 v2 CPUs, which are four-core, 3.3 GHz, 64-bit parts intended for the server market.

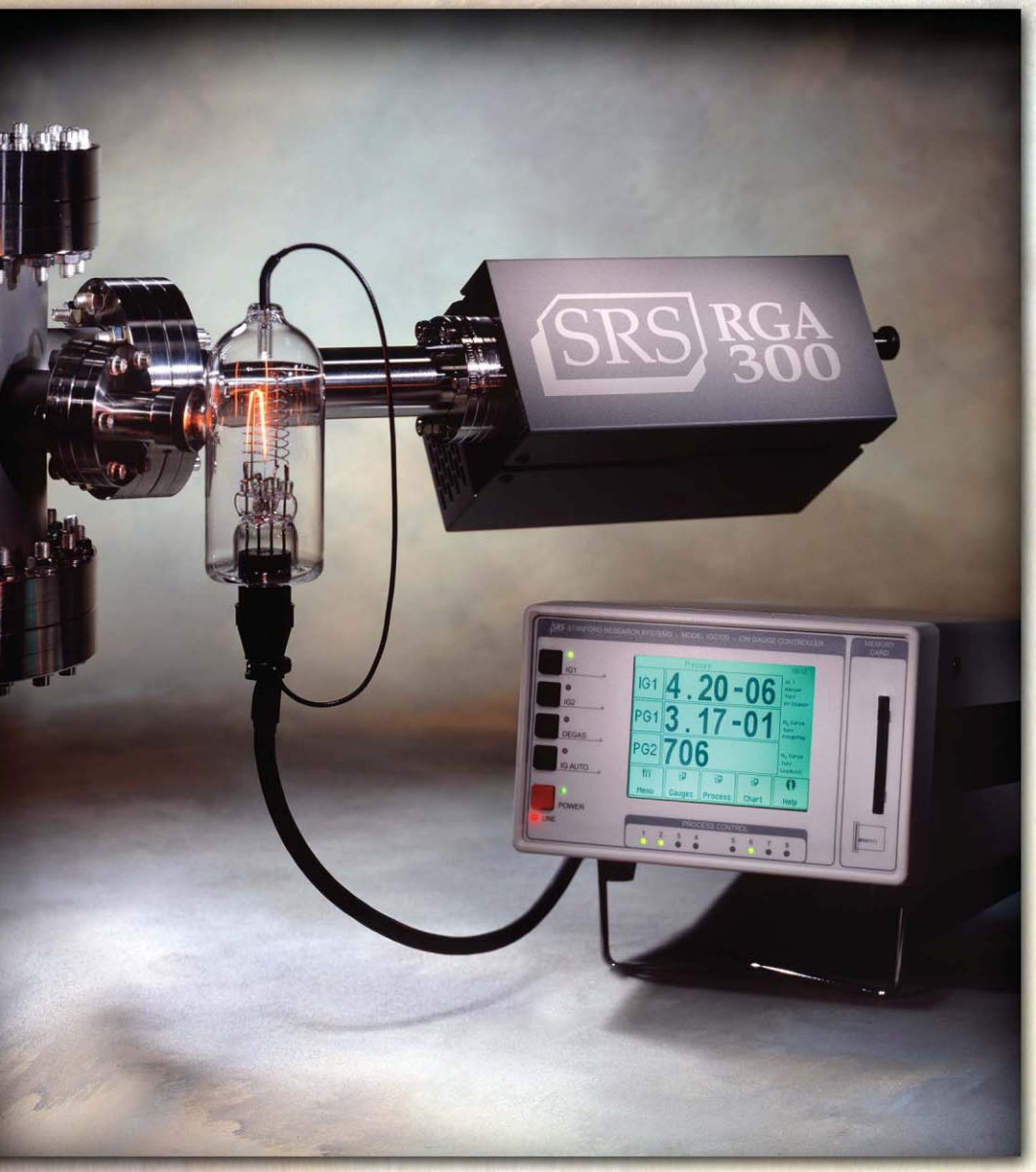


A quick cross-section reveals that Intel stayed with the nine metal layers used in the last two generations.

Looking at TEM images of the die (visit the blog URL to see images), James found that the PMOS S/D fins have epitaxial growth on them, and the fins have an unexpected slope -- a bit different from Intel's trigate schematic shown last year.

As announced by Intel, there is embedded SiGe in the source/drains, although not etched to the <111> planes as in the 32 and 45nm product. It also looks as though the tops of the gates have been etched back and back-filled with dielectric, and the contacts are self-aligned as in memory chips. **http://bit.ly/J9PGcD**

Vacuum *Pressure Measurement*



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editorial

Funding the future: Managing the cost of R&D

One of the big issues now facing the industry is to how best spend limited funding for research and development, when so much needs to be done. Continued scaling to 10nm and below, a transition to 450mm, 3D integration, device new structures such as the FinFET, a bevy of new materials with unknown integration challenges - these are all needed.

I think it's fairly clear that, with the industry's present model, it's going to be difficult to fully finance everything on the wish list. This isn't a new dilemma, of course. In a SEMI-funded reported published in 2005, Ron Leckie analyzed all the things that were noted in the International Technology Roadmap for Semiconductors (ITRS) and concluded that the funding gap could reach upwards of $9.3 billion by 2010 (which included the 450mm transition). Seven years later, Moore's Law is holding firm. The way the industry has been able to get around the funding challenge is through collaboration. Consortia such as SEMATECH and imec are great models of collaboration, enabling companies to work on "pre-competitive" research to share costs and reduce risks. The Common Platform model employed by IBM/Samsung/GLOBALFOUNDRIES is another great example. The entire CNSE/Albany Nanotech/G450C effort is perhaps the best example of university, industry, consortia and government working together.

> "A new model is needed or not everything will get funded"

But is this enough? One could argue that fabless companies could do more to support semiconductor R&D. Ditto for the likes of Microsoft, Facebook and many other entities that have built their company on the internet and electronics technology.

Perhaps the semiconductor industry will go the way of the automotive and aerospace industries, which have very different models when it comes to cost-sharing and risk-sharing. One thing is for sure: a new model is needed or not everything will get funded.

—Pete Singer, Editor-in-Chief

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EUROPE | **Infineon Technologies AG** CEO Peter Bauer will resign his post at the end of the current fiscal year due to worsening osteoporosis. **http://bit.ly/Jexoy3**

ASIA | **Micron Technology Inc. (Nasdaq:MU)** confirmed that it is engaged in discussions to take over the assets of bankrupt DRAM maker Elpida Memory. **http://bit.ly/KsofQn**

WORLD | Worldwide silicon wafer area shipments increased slightly during Q1 2012 when compared to Q4 2011 area shipments, according to SEMI. **http://bit.ly/MgXKz6**

ASIA | **Hanking Industrial Group** broke ground on a MEMS manufacturing campus in Fushun City, China, outside of Shenyang. **http://bit.ly/Kk6gJa**

WORLD | Semiconductor packaging and test services provider **Carsem** will assemble and test LED packages. **http://bit.ly/L3CpUi**

USA | The **CNSE** Smart System Technology and Commercialization Center of Excellence (STC), Canandaigua, NY, was designated as a Trusted Foundry by the US DoD. **http://bit.ly/IcA3UG**

ASIA | Many display manufacturers are transitioning tablet panel production to larger plants, including Gen 6 and Gen 8, which will lead to greater capacity for tablet displays, as well as lower prices. **http://bit.ly/JtkLPq**

USA | **Microsoft** has joined the Hybrid Memory Cube Consortium (HMCC), a collaboration of original equipment manufacturers (OEMs), enablers and integrators. **http://bit.ly/Lg0spg**

MOCVD capex disobeys fab utilization rules at LED makers

Barclays Capital analysts attended Lightfair International (May 9-11) and gleaned several trends in LEDs and OLEDs for lighting. This year's Lightfair was "almost entirely focused on LEDs," said Barclays analysts. While LED dominance in new products at the booths is not yet indicative of end market penetration, it highlights the inevitability of LED lighting adoption in the coming years.

While utilization rates are still relatively low in LED fabs, many chipmakers are reluctant to convert all of their backlighting-specific (BLU LEDs for display applications) LED tools to lighting-specific production, because they value yields honed for a specific design. Chipmakers told Barclays that they do not want to reconfigure MOCVD tools unless they are confident that this backlighting-specific production will no longer be needed. This suggests that anticipated LED lighting demand in H2 2012 and beyond will require more MOCVD tool orders, even without higher capacity utilization rates in LED fabs. Gradually improved MOCVD capex, in Q3 2012 and beyond, will be supported by a steady stabilization in LED supply/demand as 2013 approaches.

Barclays observed that LED chips still compete based on price, even among the Tier 1 LED makers, and further cost reductions are needed if margins are to survive. LED component price declines did moderate to an extent relative to last year's price cuts, but the aggressive pricing trend continues, driven in part by end customers leveraging Tier 3 quality price points in China against Tier 1 and 2 LED makers. Until yields top 80%, lower-quality LEDs will be dumped on the market at lower prices. Indeed, even in lighting-grade LEDs, there is "no rationality for price points," according to 1 Tier-1 supplier. The good news for LED revenues is that unit volume growth is offsetting the price cuts.

Only ~10 LED makers can reach 100lm/W efficacy levels in mass production, and meet Energy Star, UL, etc., specifications. Samsung is becoming a major threat to Tier-1 LED suppliers, longer term, as it focuses on quality.

While still in the early stages of development, OLED lighting was also being exhibited by several suppliers, with Philips and OSRAM appearing to be at the lead with efficacy and product quality. Philips' OLED lighting panels reached 25lm/W this year, with

Continued on page 7

the company aiming for 60lm/W next year, driven by new developments in OLED materials (Philips using RGB stack with combination of phosphorescent and fluorescent materials); new developments in the glass substrate (adding reflective element to the glass composition); and advances in the deposition and processing technology. However, while reaching 60lm/W efficacy would be a big breakthrough, the key from there would be lumen maintenance, which is still very low for the OLED lighting panels currently available on the market. And while some companies suggested that OLED lighting is now moving from a designer/architectural application to a high-end lighting application, based on the product specs and the pricing, Barclays puts OLED lighting ~5-7 years behind LED lighting.**—M.C.**

Top OSATS raise 2012 capex with test focus

The top three outsourced semiconductor assembly and test services (OSATS) providers raised 2012 capital expenditures during their earnings reports, from initial plans announced in January, report analysts at Citi.

To increase capacity due to mobility growth, Amkor (AMKR) raised capex from $300 million to $550 million; Advanced Semiconductor Engineering Incorporated (ASE) raised capex from $725 million to $800 million; and Siliconware Precision Industries Co. Ltd. (SPIL) raised capex from $350 million to $600 million. Collectively, the three companies increased 2012 capex by $575 million or 42% vs. January plans.

"Several of our major customers that sell into smartphones and tablets have substantially increased their demand forecasts with us and we are raising our estimate of 2012 capital additions...to meet these specific new opportunities. However, our sales and capital additions may vary depending on a number of factors including the supply of 28 nanometer wafers for some of our customers," said Ken Joyce, Amkor's president and CEO.

All three OSATS singled out test capacity addition as the focus of higher capex, with total test capex up from $280 million (in Jan plan) to $628 million, up 124% from the original plan. OSATS commented that baseband and power management ICs are the main driver. Citi expects Teradyne to get a sizable share of the orders due to its 60% share in mobility.

The current capex plan for these top 3 OSATS is slightly H1 loaded, with 55% of planned capex earmarked for the first half of 2012. However, with low/unstable yield at 32/28nm fabs, and a large amount of capacity entering the market starting in Q3, there is a general concern over skyrocketing test burden in H2. Citi expects this could drive the upside in H2 of OSATS test capex.**—M.C.**

news cont.

President Obama speaks on "insourcing" at Albany Nano-Tech complex

US President Barack Obama toured the University at Albany - State University of New York (SUNY) - Albany Nano-Tech Complex on May 8, speaking about the economy in the College of Nanoscale Science and Engineering's (CNSE) NanoFab Extension Building.

CNSE is a global education, research, development and technology deployment resource educating scientists and researchers in nanotechnology. It hosts myriad private-public partnerships with academia and research organizations partnering with global semiconductor equipment and materials suppliers, as well as chip makers.

> "The true engine of job creation in this country is the private sector. There are steps we can take as a nation to make it easier for companies to grow and to hire"

GLOBALFOUNDRIES CEO Ajit Manocha spoke during the event. The presidential visit had to move from GLOBALFOUNDRIES' new Fab 8 to the college for logistical reasons. Since breaking ground on Fab 8 in 2009, GLOBALFOUNDRIES has created more than 1,300 new direct jobs with the project, drawn from local talent in the region and national and international sources. Fab 8 created an additional 4,300 construction-related jobs and established the largest private Project Labor Agreement in history, generating hundreds of millions of dollars of economic development throughout upstate New York, the foundry reports. Fab 8 began production in January 2012, and should ramp to volume this year.

In January, President Obama visited Intel's Ocotillo semiconductor manufacturing location in Chandler, AZ, touring Fab 42, which is under construction. The visit carried a similar theme as the one to CNSE in May — advanced manufacturing jobs in America, and improving education to develop future technological leaders from America. Obama is emphasizing the connection between education, innovation, and manufacturing in supporting investment and bringing jobs back to the US, which the administration touts as "insourcing."

"The true engine of job creation in this country is the private sector. There are steps we can take as a nation to make it easier for companies to grow and to hire — to create platforms of success," said Obama at CNSE (a transcript of Obama's remarks is available from the White House, http://1.usa.gov/JoFqCb). He listed ways to accelerate the US economy, including tax breaks for clean-energy companies and small business owners, support for veterans in the job market, and encouraging US-based manufacturing and exports. "American manufacturers are creating new jobs for the first time since the 1990s," he said, and asserted that half of America's largest companies are considering moving manufacturing operations from China to the US. "Even when we can't make things cheaper than other countries, we can always make them better."

From the White House: "The President's visit to the College of Nanoscale Science and Engineering at SUNY-Albany demonstrates the important role that partnerships between universities and companies can play in accelerating education, innovation and U.S. manufacturing investment."

The President compared CNSE to his administration's proposed "National Network for Manufacturing Innovation" consisting of up to fifteen institutes, each bringing diverse companies, research organizations and universities, federal agencies, and states together to make US manufacturing facilities and enterprises "more competitive and encourage investment." **—M.C.**

news cont.

GLOBALFOUNDRIES joins top-20 ranks in Q1 on Elpida bankruptcy

The top 20 semiconductor suppliers in Q1 2012, compiled in IC Insights' May Update to The McClean Report, show Intel's firm hold on the top of the rankings, registering a 68% higher sales level than Samsung in Q1.

With the addition of GLOBALFOUNDRIES, 3 pure-play foundries are now in the top 20 ranking. GLOBALFOUNDRIES replaced bankrupt Elpida. If Micron takes over the bankrupt DRAM maker, it could jump 1 or 2 positions in the rankings.

Q1 sales from the top 20 semiconductor suppliers were "generally disappointing," says IC Insights, which believes that the bottom of the semiconductor market slowdown occurred for most top companies in Q4 2011/Q1 2012. IC Insights expects much improved sequential quarterly sales performance starting in 2Q12, based on company reports and analysis. Expect a 6% increase from Q1 to Q2, and even stronger growth Q2 to Q3.

The top 20 semiconductor suppliers saw a wide range of Y/Y growth in Q1. Only 3 companies registered better-than-flat Y/Y growth rates: Qualcomm, Fujitsu, and Broadcom. Each of the big four memory suppliers in the top 20 ranking — Samsung, Toshiba, SK Hynix, and Micron — saw sales decline Y/Y.—**M.C**

Q1 2012 rank	2011 rank	Company	HQ	2011 total semi	Q1 2011 total semi	Q1 2012 total semi	Q1 Y/Y % change
1	1	Intel	US	49697	11819	11874	0
2	2	Samsung	S. Korea	33483	8215	7067	-14
3	3	TSMC*	Taiwan	14600	3600	3568	-1
4	5	Toshiba	Japan	12745	3435	3232	-6
5	7	Qualcomm**	US	9828	1962	3059	56%
6	4	TI	US	12900	3167	2934	-7
7	6	Renesas	Japan	10653	2897	2344	-19
8	10	Micron	US	8571	2218	2120	-4
9	9	SK Hynix	S. Korea	9403	2499	2115	-15
10	8	ST	Europe	9631	2523	1997	-21
11	11	Broadcom**	US	7160	1752	1770	1
12	12	AMD**	US	6568	1613	1585	-2
13	13	Sony	Japan	6093	1520	1514	0
14	14	Infineon	Europe	5599	1362	1297	-5
15	15	Fujitsu	Japan	4430	1148	1216	6
16	17	NXP	Europe	4147	1071	1071	0
17	18	Nvidia**	US	3939	936	935	0
18	16	Freescale	US	4391	1155	912	-21
19	21	GLOBALFOUNDRIES*	US	3480	845	840	-1
20	20	UMC*	Taiwan	3760	995	834	-16
Top 10 Total				171511	42335	40310	-5
Top 20 Total				221078	54732	52284	-4

**foundry **fabless*

Q1 2012 Top 20 semiconductor sales leaders ($M, includes foundries). SOURCE: IC Insights.

news cont.

ST's MEMS revenues jump 82% in 2011, but TI holds onto #1 spot

Texas Instruments Inc. (TI, TXN) remained the top manufacturer of MEMS in 2011 with $779.0 million in MEMS revenues, fending off runners-up Hewlett Packard Co. and Bosch in tough competition for market share, according to an IHS iSuppli MEMS Market Brief report.

TI's MEMS revenue fell 4% from 2010 to 2011, owing in part to supply chain disruptions caused by the 3/11 Japan earthquake. Sales of digital light processing (DLP) MEMS chips kept TI on top in 2011, said Jérémie Bouchaud, director and senior principal analyst for MEMS & sensors at IHS. The DLP business was what helped propel TI to the top spot in 2010, rebounding in the business and education front-projector segment. "Sales are especially strong in China and India," Bouchard notes, where DLP-based projectors have taken market share from LCDs. While front-projection designs are growing, rear-projection DLP TVs have virtually disappeared.

TI also found success in pico-projectors, a still relatively small portion of its MEMS business at <$50 million of MEMS revenues. The company is the top supplier of pico-projectors for both accessory and embedded projectors such as those found in the Beam handset from Samsung Electronics. The product segment will be a main growth driver at TI over the next 5 years. TI also introduced a MEMS temperature sensor, or thermopile, in 2011, targeting new handsets and tablets.

Hewlett-Packard also lost 4% of revenues from 2010 to 2011, coming in with $748.4 million from its MEMS business. HP held the #1 rank from 2005 to 2009, but suffers from price erosion in its MEMS thermal actuators, used in inkjet printheads. HP has lower shipments of disposable printheads as well, since it started migrating to permanent ones in 2005.

Bosch and ST had much larger revenue jumps than the 2 top suppliers, which could indicate more competition for #1 in the near future. The Bosch Group GmbH remained #3 with revenue of $742.2 million, shooting up 15% from 2010. Bosch saw growth in automotive MEMS as new vehicle safety products ramp up with inertial and pressure sensors. STMicroelectronics saw 82% revenue growth in MEMS — the largest of any in the rankings — to $651.6 million. **—M.C.**

Rank	Company	2011 Revenue	2010 Revenue	Y/Y Growth (Decline) %
1	Texas Instruments	779.0	810.5	-4%
2	HP	748.4	782.1	-4%
3	Bosch	742.2	643.0	15%
4	STMicroelectronics	651.6	357.5	82%
5	Canon	368.7	354.7	4%
6	Panasonic	310.1	285.7	9%
7	Denso	286.4	262.5	9%
8	Knowles	270.9	191.5	41%
9	Analog Devices	250.2	204.2	22%
10	Epson	247.7	264.7	-6%
Total for Top 10		4,655.1	4,156.4	12.0%
Share of Total MEMS market		59.0%	58.5%	

Worldwide revenue forecast for MEMS IDM and fabless manufacturers, excluding foundries ($M). SOURCE: IHS iSuppli Research, May 2012.

Large-area TFT-LCD panel makers see rising shipments, revenues in Q2 2012

Large-area TFT-LCD panel shipments declined in Q4 2011 and again in Q1 2012, but should grow 11% to 189.6 million in Q2 2012, with brands and OEMs increasing orders, and panel makers increasing capacity utilization. Revenues will rebound as well, with panel prices increasing, according to NPD DisplaySearch's Quarterly Large-Area TFT LCD Shipment Report - Advanced LED.

Following a "long-standing over-supply" in the TFT LCD industry, which induced lower panel prices, panel makers are "restructuring and adding new technologies and processes" to improve costs and performance, said David Hsieh, VP, Greater China Market, NPD DisplaySearch. Hsieh sees 2012 as a year of "gradual recovery," when panel prices rebound and shipments increase. Q2 2012 is an example, with double-digit growth in shipment units, shipment area, and revenues. Large-area TFT LCD shipment revenues will grow 14% Q/Q to $20.6 million.**—M.C.**

3.5D interposers: PCB replacement?

At the 15th Symposium on Polymers for Microelectronics (May 8-10 in Wilmington, DE), TSMC and Yole Developpement gave plenary presentations on the use of polymeric materials in wafer-level packaging (WLP) from foundry and overall industry perspectives.

Dr. Phil Garrou, Contributing Editor

The most controversial comment came from TSMC's Doug Yu, senior director of front-end and back-end technology development, who challenged the current nomenclature and pronounced that the versatile interposer technology should be called "3.5D" instead of 2.5D, since it is and will be capable of much more than the simple 3D packaging stack. Yu's presentation was title "Semiconductor Paradigm Shift and Increased Foundry Roles."

The term 2.5D is usually credited to ASE's Dr. Ho Ming Tong who, around 2009 (or even earlier), declared that we might need an intermediate step towards 3D packaging, since the infrastructure and standards were not yet ready. The silicon interposer, Tong felt, would get us a major part of the way there, and could be ready sooner than 3D technology, thus the term 2.5D, which immediately caught on with other practitioners.

Yu's new position is that interposer technology actually is more versatile and thus should be called 3.5D, since it not only offers a better thermal solution than 3D integration, but "can someday replace most of the high density PC boards [PCBs]." Yu's position is that this modular silicon technology will need minimal low-density PCB substrates to connect the functions that have been fabricated on silicon and will be, in essence, the perfect "fab-centric" solution. Future smartphones and tablets could be made up of such simple 3.5D silicon modules.

Representing Yole Developpement, I presented an overview of polymeric materials in wafer level packaging (WLP), considering the pros and cons of the major material choices — epoxies, PI, PBO, BCB, siloxanes — and the offerings of 25 major suppliers. There have only been 5 major categories of polymers developed for microelectronics in the last 50 years, or one per decade. "If you think you have the next great polymer chemistry for electronics, you better also have deep pockets and patience," I warned attendees.

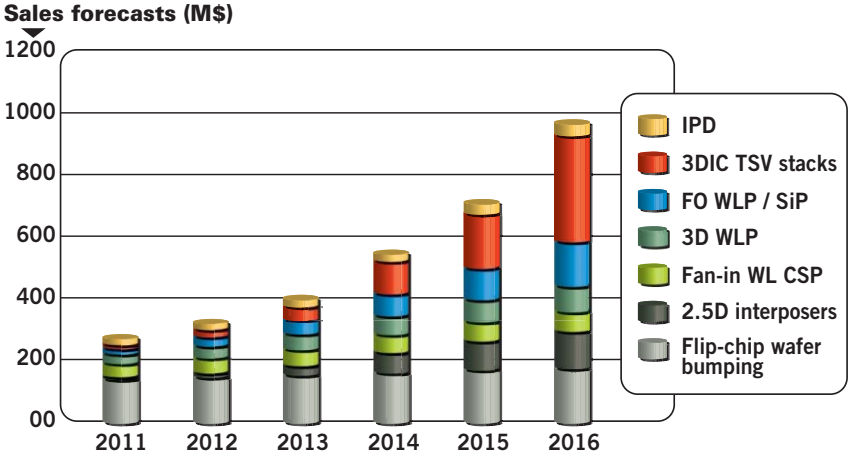


FIGURE 1. Global materials market for wafer-level packaging. SOURCE: Yole Developpement.

We also looked at the 6 key functions that these materials serve, and where they are used in the 7 key WLP applications.

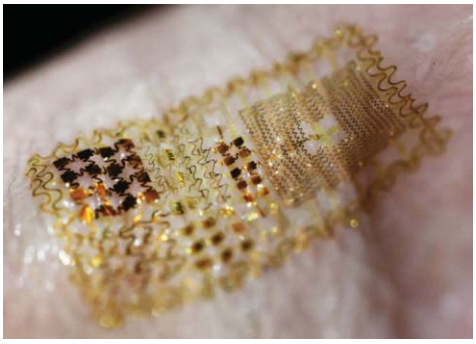
According to Yole, the polymeric semiconductor material market reached a value of $274 million last year and will see 26%+ compound annual growth rate (CAGR) over the next 5 years, fueled by the expansion of key WLP applications.

Packaging

Epidermal electronic systems

Scientists have developed a new type of ultra-thin, self-adhesive electronics device that can effectively measure data about the human heart, brain waves and muscle activity - all without the use of bulky equipment, conductive fluids, or glues.

Presenting at the MRS Spring 2012 meeting in San Francisco, Nanshu Lu (now at UT Austin) of the John Rogers group at U Illinois Urbana discussed the groups' recent achievements in epidermal electronic systems. Micro-transfer printing is the method of choice for interconnecting small rigid silicon electronics elements with thin nanoribbons of silicon or metal. Depositing onto a pre-stretched elastomer substrate provides a resting state in which the interconnects are buckled or canted and can endure up to 100% elongation while imparting ≤1% stress to the rigid circuit elements.



The trick of fabricating extremely thin silicon for flexibility applies to the PDMS polymer substrate as well when the objective is to apply the device to the skin and tolerate stretching and bending without adhesion loss. The thin polymer stability is maintained until it is applied using technology similar to that used in applying temporary tattoos. For some device types, the rigid silicon electronics can be eliminated by integrating the active device elements into the serpentine interconnects themselves. For development of integrated devices, functions that have been demonstrated include amplifiers, temperature sensors, strain gauges, solar power sources, induction couplers and wireless transmitters & receivers for device control. Current devices, however, use wires to connect to external control and power sources. The only three elements in contact with the skin are gold, silicon and polyimide, all of which are FDA approved.

Mike Fury, Techcet Group

Also presenting at MRS, Michael Melzer of IFW Dresden extended the family of stretchable electronics from silicon and optoelectronics to now include magneto electronics. Stretchable GMR multilayers are fabricated by depositing GMR thin films on a pre-strained PDMS substrate. Data indicates no loss of magnetic performance through this process to 2.5% strain even though resistance starts to rise above 1.6% strain. For greater detection sensitivity, stretchable spin valves were developed using the same process flow as for the GMR multilayers. After some refinement of the process, they were able to achieve 29% strain without losing functionality or sensitivity.

A Gaikwad of City College NY described a stretchable battery embedded in cloth with Zn and MnO_2 as the active materials. Cracking and delamination due to flexing and stretching was addressed by embedding these materials in a non-conducting nylon mesh in an earlier version. In the new version, a silver coated nylon cloth is used as the substrate for the Zn electrode and separately for the MnO_2 electrode. No delamination or electrical degradation was observed at 100% strain in either the x- or the y-direction. The capacity of 4 mAh/cm^2 was maintained even with this stretching 100% level.

MEMS

TRANSISTORS

The Next Transistor

PETE SINGER, *Editor-in-Chief*

We are in the age of the FinFET, which may soon feature III-V channels. Longer term, CNTs and graphene may come into play.

Technologies such as strained silicon, high-k metal gates and FinFETs have enabled smaller transistors, which improve packing density and lower the cost per transistor. Moving forward, the goal is to continue to increase density and reduce cost, but also to improve energy efficiency by limiting leakage and lowering the power supply.

FinFETs, which were rolled into volume production by Intel last year, will likely be the transistor of choice for many years to come, as others follow Intel's lead. Transistors with high-mobility channel materials, such as InGaAs, offer tremendous promise, particularly when implemented in a quantum-well FET (QWFET) design (but they can also be implemented in a FinFET).

Eventually, a move to the next "switch" will be required. It might be transistor – a spin-transistor or a tunneling transistor, for example — but it could be some other kind of switch, perhaps based on carbon nanotubes (CNTs) or graphene. Early work shows good results, but it's a long road from the lab to volume production, often many decades.

As Intel's Mark Bohr noted in his keynote address at the 2011 International Electron Devices Meeting (IEDM) in December, traditional MOSFET scaling has served the industry well for more than three decades by providing continuous improvements in transistor performance, power and cost. However, with the growing market interest in mobile products with long battery life, and growing need to lower the energy cost of running large data centers, there is more interest in reducing transistor leakage current and operating voltage [1].

Intel's announcement in May of last year was historic in the world of transistor evolution. The announcement was that the 3-D transistor design called tri-gate, first disclosed by the company in 2002, would be moved into high-volume manufacturing at the 22nm node in an Intel chip codenamed "Ivy Bridge." In the second quarter of this year, Ivy Bridge will ramp to nearly 25% of Intel's processor production.

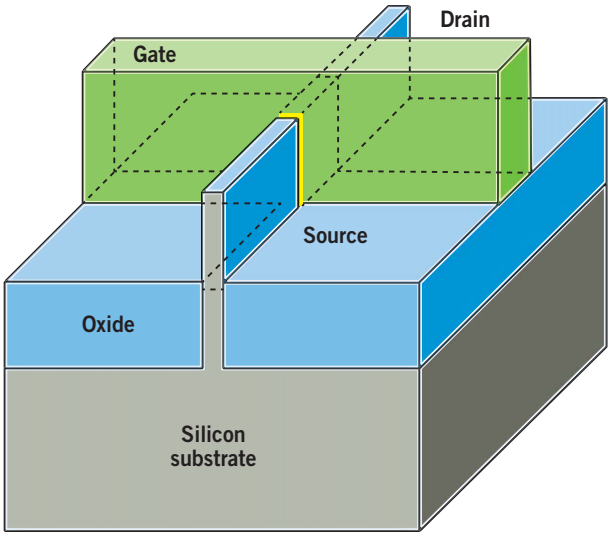


FIGURE 1. Intel's 3-D Tri-Gate transistor structure provides improvements in performance, leakage power and active power.

Offering improvements in performance, leakage power and active power, tri-gate transistors — also called FinFETs because of their "fins" as shown in **Fig. 1** and **Fig. 2** — are in the general category of multi-gate transistors that have fully depleted operation. Fully depleted devices can offer three forms of improved transistor operation: lower off-state leakage, higher performance and/or lower active power [1]. The tri-gate structure wraps

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the gate electrode around three sides of tall and narrow silicon fin, providing improved electrostatic control of the channel region compared to a traditional planar device. The improved channel control results in a steeper sub-threshold slope which can provide up to a 10X off-state leakage reduction. The improved channel control also enables gate length scaling, which benefits both area scaling and reduces gate capacitance.

Alternately, the tri-gate device can be operated at a lower threshold voltage with the same leakage as a planar device. This lower V_T can be used to provide either higher performance or allow lower operating voltage for reduced active power. 22nm tri-gate transistors provide a 37% gate delay improvement at 0.7V or a 50% active power reduction at constant performance when compared to Intel's 32 nm logic technology on a comprehensive set of benchmark circuits.

Long live the FinFET!

With the advantage of FinFETs firmly established, the rest of the industry is following suit. "Today, what the foundries are focused on, GLOBALFOUNDRIES in particular, is the FinFET," said David Bennett, vice president of alliances for GLOBALFOUNDRIES, speaking at SEMI's Advanced Semiconductor Manufacturing Forum (ASMC) in May. "The initial introduction will be around 20nm-type design rules. Once we get 'on the fins,' there's going to be an absolute, strong motivation across the entire IP ecosystem to maintain that architecture and to continue to drive price/performance and cost down. We'll do that through improved dimensional controls on heights and profiles of the fins, as well as materials, such as III-V channels. We'll also really work on V_{dd} scaling."

Subu Iyer, IBM Fellow and Chief Technologist at the Microelectronics Division, IBM Systems & Technology Group, also spoke at ASMC. "I dare say that everybody in the next generation, 14/15nm or whatever nanometer technology we're talking about, is going to be using FinFETs," he said. But he also noted that, for the first time in the industry's history, the cost per transistor has not decreased with a new technology generation. "If you look carefully, it does not buy us the density that we're used to. It's not the 0.7 scaling that doubles the number of circuits per unit area," he said. "It's also not really buying us power. If we were following Danard's scaling, which he proposed back in the late '70s, we should have been sitting around 300 or so mV of V_{dd} supply. We're not. Why? Because, from a circuit perspective, we don't have noise immunity at those low voltages. That's a problem," he said.

All of these factors have many calling for a new way of thinking. "The next step of innovation, and the next step for our R&D dollars, has to be in figuring out what are we going do to actually reduce power dramatically. If you look at where we are today, the power/circuit – even though it's very impressive for all of our handheld appliances and so on – is still way, way out of the league of biologically competing systems, for example," Iyer said. "I believe quite honestly that there is something that is going to come from some other direction that is really going to upset this whole apple cart." He noted that the supercomputer Watson may have won the Jeopardy match, but consumed 3-4 kW vs the 20W of brain power used by the two human competitors.

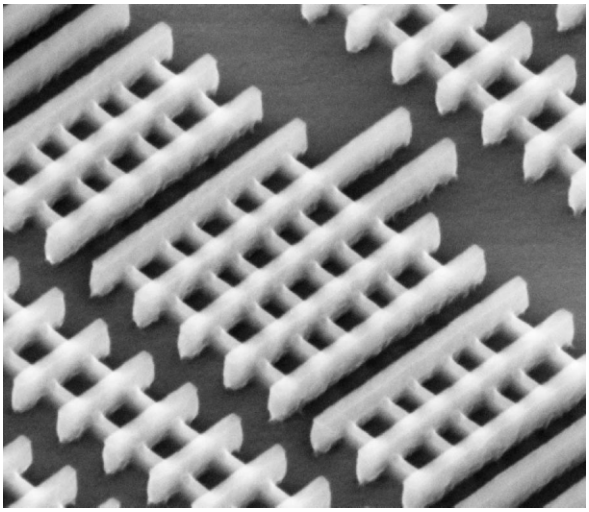

FIGURE 2. This image shows the vertical fins of Intel's tri-gate transistors passing through the gates.

Strained silicon and III-V channels

Straining semiconductor material within a transistor increases the mobility of the electrons flowing through it, leading to either faster or lower-power devices than could be built with

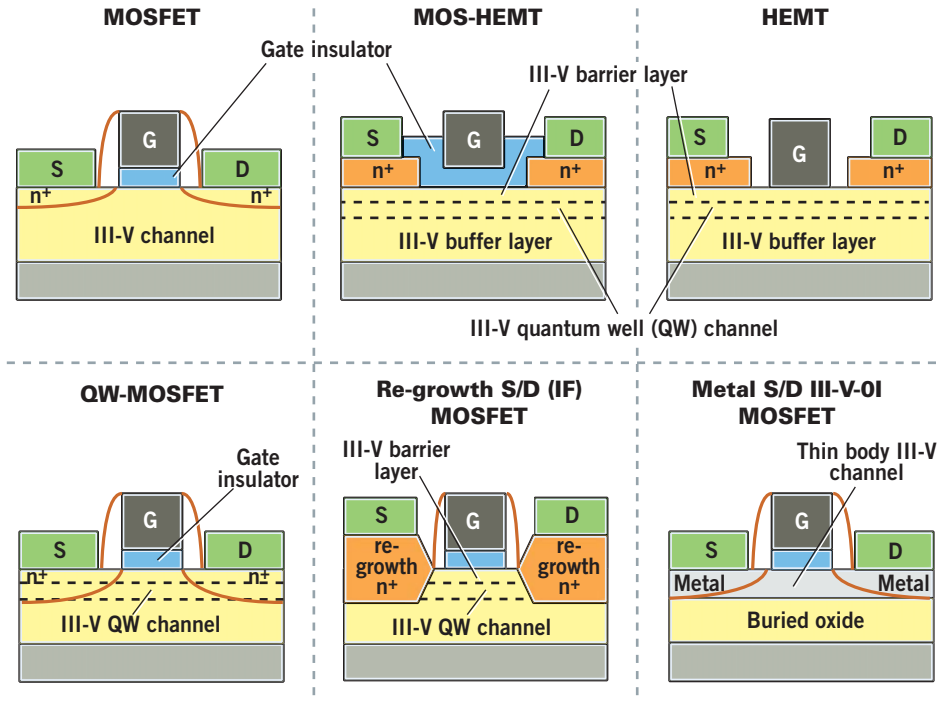

FIGURE 3. Cross-sections of common types of device structures build with III-V channels. Source: Shinichi Takagi, University of Tokyo.

unstrained silicon.

As transistors shrink to nanoscale dimensions, however, variability in performance is growing and high manufacturing yields are getting harder to achieve. According to reports provided in advanced of the VLSI Symposium, to be held June 12-15 in Honolulu, two main reasons are atomistic doping effects (i.e. the discreteness of doping becomes important in devices with nanoscale dimensions) and manufacturing-process-induced variations. In transistors for low-power applications, thin-body structures have been shown to suppress off-state leakage current without the need for doping, and also to reduce sensitivity to gate-length variations. But whether these benefits can be achieved for high-performance applications is unclear, because it is difficult to strain thin-body structures effectively to enhance performance.

At the VLSI Symposium, IBM Alliance researchers will describe how they managed to do this for transistors at the 22nm CMOS technology node. The strain was enabled by in-situ-doped raised-source/drain (implant-free) and strained-channel processes. The devices achieve record-high transistor drive currents at given off-currents. The researchers say these strain engineering techniques are extendable to even smaller transistors.

However, still higher electron mobilities are required to enhance transistor performance at lower supply voltages. **Figure 3** shows several different "flavors" of transistors with III-V channels that offer this high-mobility.

At IEDM, an Intel-led team unveiled tri-gate FinFET-type quantum-well InGaAs MOSFETs with 30-nm gates that deliver the best electrostatic performance of any III-V MOSFET. Two key metrics are subthreshold slope and drain-induced barrier lowering, or DIBL. Long-channel devices exhibited a subthreshold slope of 66 mV/decade, close to the theoretical minimum of 60 mV/decade, while DIBL of short gate length devices was significantly improved over best-in-class planar III-V MOS devices. At the upcoming VLSI Symposium, University of Tokyo researchers will report the first sub-60nm III-V n-channel MOSFETs on silicon substrates with excellent control of short-channel effects and suppression of off-state leakage current. The devices, which are made from InGaAs- and InAs-on-insulator on silicon substrates, enable higher transistor on-state current thanks to carrier mobility enhancement and to reduction of parasitic resistance.

Beyond 10nm

With current scaling approaches, gate lengths as small as 10 nm are likely to be achieved. But is that the end? A Purdue-led team decided to try to find out. Through atomistic simulations, they looked at several promising device designs and

material combinations: carbon nanotubes, graphene nanoribbons, and III-V and silicon ultra-thin-body devices and nanowires (graphene is a one-atom-thick sheet of carbon atoms with an exceptional set of properties that give it great potential for electronics applications). They performed extensive numerical simulations of intrinsic characteristics, limiting factors and design impacts. The simulations show that a) with careful engineering, good sub-threshold swing can be obtained for many of these device alternatives for gate lengths down to 8 nm; b) non-planar devices can provide good performance even at 5-nm gate lengths; and c) when the bandgaps are the same, carbon nanotube FETs and small-diameter silicon and III-V nanowires exhibit roughly the same performance, but the details of the potential profile and the onset of interband tunneling are critical.

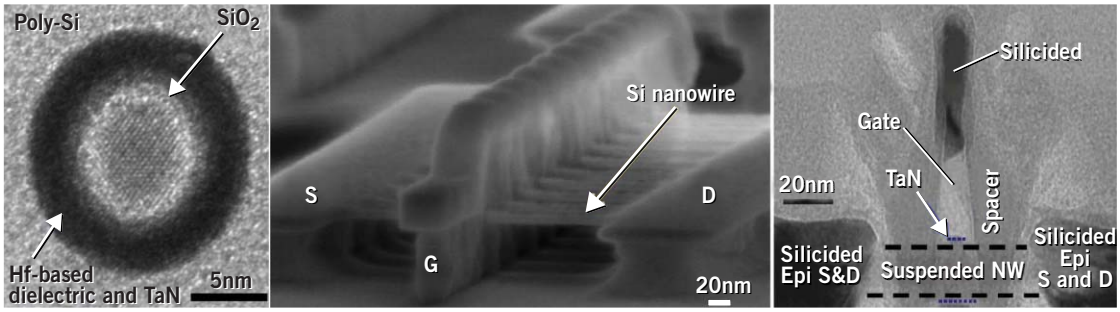

FIGURE 4. The ultimate 3D transistor might be a silicon nanowire with the gate wrapped entirely around it. The dots in the left-most image are individual atoms. Source: IBM.

In recent work, IBM used synthesized graphene to produce record radio-frequency (RF) performance from transistors (reported at IEDM 2011). The IBM team demonstrated a 280-GHz cut-off frequency in a 40-nm gate-length FET, the fastest ever reported from synthesized graphene. They also achieved record high output current (5 mA/μm) and transconductance (2 mS/μm) in synthesized graphene FETs (albeit with longer gate lengths), and explored the impact of gate dielectric selection. These devices also demonstrated an appreciable RF voltage gain of 10 dB.

The first experimental demonstration of sub-10-nm transistors made from carbon nanotubes (CNTs) was also conducted by IBM. The CNT-based transistors not only demonstrated better current-drive performance than conventional silicon devices under similar bias conditions, they performed better than theory predicts they should have. Single-walled CNTs are a possible replacement for silicon but it hasn't been clear that sub-10-nm gate length CNT-based transistors can avoid short-channel effects that degrade performance. The IBM researchers have shown that such aggressively-scaled CNT-based transistors are, in fact, feasible. They built devices that achieved more than four times the current density (2.41 mA/μm) of the best competing silicon device, at a low operating voltage of 0.5 V. The researchers speculate that theoretical predictions were exceeded because the transistor gate modulates the charge not only in the channel but in the contact regions as well, which had not been considered previously.

As exciting as the potential of new materials may be, IBM's Bernie Myerson, speaking at ISS earlier this year, sounded a cautionary note. "There are carbon nanotubes, and people have made transistors out of them. But when you really get serious about making these things into technology, you really have to start looking at the genuine dimensions you want to use them at, what you're going to do with them and how they're going to behave. It's really great to see all these picture where people make a device and they get some numbers from them, but you have to make about 10 billion of them work to be competitive with current silicon.

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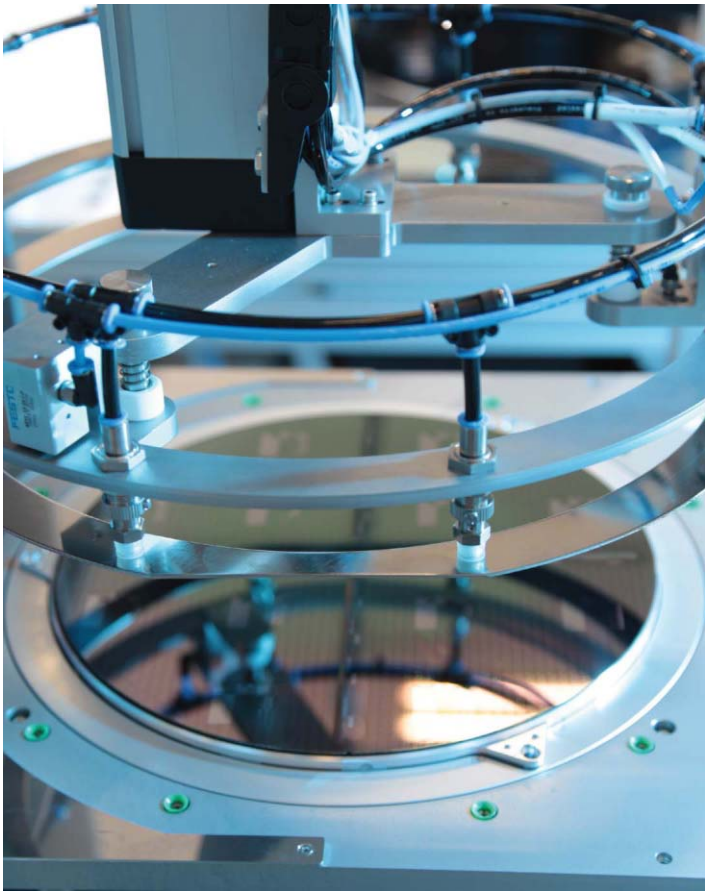
3D INTEGRATION

Thin die stacking for wide I/O memory-on-logic

THORSTEN MATTHIAS, JÜRGEN BURGGRAF, DANIEL BURGSTALLER, MARKUS WIMPLINGER, PAUL LINDNER, *EV Group, St. Florian am Inn, Austria*

Wide I/O DRAM is pushing thin wafer processing into high-volume manufacturing readiness.



Wide I/O interface memory-on-logic has the potential to be the long awaited killer application that will boost through silicon vias (TSVs) and 3D integration into high-volume manufacturing. Information transfer is rapidly transforming from text based communication to picture and video-based communication, which creates an insatiable demand for bandwidth. The convergence of smart phone and media server requires DRAM bandwidth >12GB/s in order to allow streaming of 1080p HD videos onto large displays. Conventional memory-logic interfaces ("narrow I/O interface") consume too much power at the input/outputs (I/Os) and do not allow scaling to multiple hundreds or thousands of I/Os. TSVs enable a significant power reduction at the I/O. Current DDR3 technology consumes 40mW per pin, whereas I/Os based on TSVs only consume 24µW per pin [1]. This power reduction by 1000x gives chip designers the freedom to implement 512 I/Os with the next device generation.

Wide I/O memory-on-logic is one of the most challenging 3D applications for various reasons:

- Form factor is crucial since mobile applications are the primary drivers.
- The individual memory layers require a thickness of 50µm or less.
- For memory, bandwidth and power consumption are not the only important factors; total data storage capacity is at least equally important.

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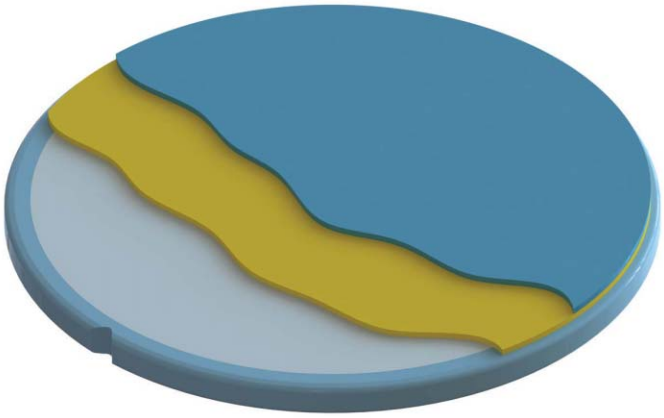
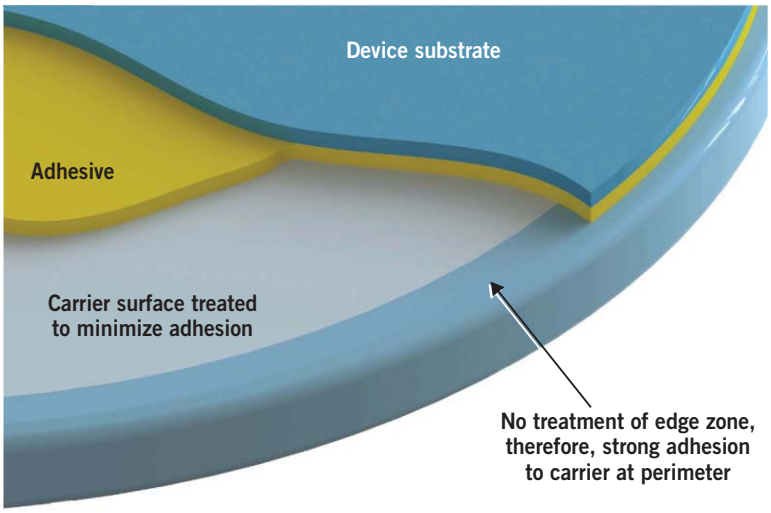


FIGURE 1. ZoneBOND™ carrier schematics and close-up



TSV integration

For these reasons, multiple memory dies have to be stacked. Initial designs require 4 layers, but 8+ layer stacks will follow very rapidly. In terms of chip stacking with TSVs, wide I/O DRAM will initially require stacking of 4 ultra-thin memory dies plus 1 logic controller. Companies have already successfully implemented manufacturing of memory-on-logic, as evidenced by recent wide I/O DRAM shipments. The key to success was a paradigm shift in TSV manufacturing. In the past, a "one solution fits all" approach had been envisioned by the industry, where an identical TSV manufacturing process would support power devices, image sensors, stacked memory and GPU-on-CPUs. For wide I/O memory-on-logic, however, specialized TSV manufacturing processes are required.

Reliable 3D integration schemes have now been developed, following system engineering principles where all aspects of the device manufacturing are considered simultaneously. In the past, engineers tried to use identical processes-of-record for frontside and backside RDL processes, leaving many integration issues to be addressed during TSV manufacturing. However, it turns out that co-engineering backside RDL and TSV manufacturing is the easier road to success. There are now multiple integration schemes for memory-on-logic.

Cost is, of course, another important factor beyond bandwidth, power and total storage capacity. The cost of TSV manufacturing correlates with the depth and the aspect ratio of the via. The cycle times for the process steps for via etching and via filling correlate with via depth and aspect ratio. For memory, silicon real estate comes at a premium so the TSV area consumption has to be minimized. The only way to minimize the TSV diameter and to keep the aspect ratio low is by reducing the TSV depth. Memory stacking with TSVs inevitably leads to the requirement to process ultra-thin wafers on front- and backside.

Thin wafer processing

Co-engineering of backside RDL, TSV and die stacking processes has changed the primary requirements for thin wafer processing. Temporarily bonding the device wafer to a carrier wafer enables wafer thinning and backside processing [2]. After backside processing, the thin device wafer is separated from the carrier. One key requirement is that this thin wafer is stackable, meaning that a) the wafer has to be particle and residue free and b) the thin wafer surface chemistry and physics has to be compatible with bonding and especially underfill processes. As memory-on-logic devices have at least 5 (without interposer) or 6 die levels (with interposer) both sides of the thin wafer have to be particle and residue free. Thermoplastic adhesives have the advantage that they allow single-wafer cleaning after debonding and that there is no modification of the device wafer passivation.

Stacking of memory sub-stack to logic controller is

usually performed by chip-to-chip (C2C) or chip-to-wafer (C2W) stacking as memory die and logic die do not necessarily have the same size. Stacking of the memory dies (i.e., the assembly of the memory "sub-stack") can be performed as C2C, C2W and also wafer-to-wafer (W2W). Stacking of memory is well suited for W2W as all the dies have the same size, the volume is high and the yield is high.

Stacking of thin wafers can be performed either after the thin wafer is debonded or while the thin wafer is still bonded onto a carrier wafer. Bonding of the thin wafer while still mounted to the carrier wafer allows comfortable and safe wafer handling, but adds some complexity to the wafer bonding process. For ultra-thin wafers, stacking before debonding might be necessary. For C2W this means dicing while the die is still on the carrier, which destroys the carrier and adds to the overall costs. W2W allows re-using the carrier wafer.

Cu-Cu bonding is the most promising process for memory stacking. Current activities are targeting a reduction of the bond temperature in order to reduce cycle time and cost of ownership, but also in order to facilitate permanent Cu-Cu bonding prior to debonding from the carrier.

Stacking of dies is typically performed by the OSAT whereas thin wafer processing is performed by the foundry. In either case, it is necessary to ship the thin wafers. Shipping of thin wafers on a film frame is quite well established, but nevertheless shipping of ultra-thin wafers with less than 50µm thickness results in small yield hits. As the wafers are very valuable at this point of the manufacturing processes (after complete front- and backside processing) the cost of yield is non-negligible.

The alternative approach is to ship the thin wafers while still securely bonded to the carrier and debond directly at the assembly site. This requires an innovative supply chain where the foundry performs temporary bonding and the OSAT performs the debonding. Such a supply chain is only feasible with the existence of standards for bonding and debonding processes and equipment.

As previously mentioned, new TSV manufacturing processes are specifically engineered for different products, such as power devices or wide I/O DRAM, which typically means that different optimized adhesives are being

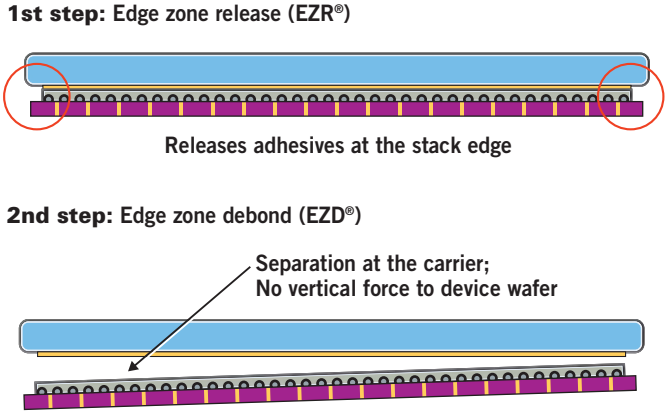


FIGURE 2. ZoneBOND™ debonding is a 2-step process: during the release step the adhesive edge zone is dissolved; the thin device wafer is separated from the carrier during the debond step.

FIGURE 3. EVG850 "XT Frame" Temporary Bonding and Debonding System

used. LowTemp® ZoneBOND™ debonding brought a revolutionary breakthrough toward standardization [2]. With this technology debonding is a function of the carrier, which makes the debonding process independent of the used adhesive. Figure 1 shows the ZoneBOND carrier wafer. In the center is a zone with reduced adhesion, whereas the edge zone provides full adhesion. Figure 2 shows the debonding process. First, the adhesive in the edge zone is dissolved in single wafer mode during the Edge Zone Release (EZR®) process. Then the device wafer is separated from the carrier wafer during the Edge Zone Debond (EZD®) process. The thin wafer is mounted on a film frame for subsequent singulation and assembly. The physical separation process happens at the interface between carrier wafer and adhesive film. During this debonding, the bumps are safely embedded in the adhesive film. No force is applied to the bumps during debonding. An open platform has been established which enables a versatile supply chain for ZoneBOND materials from multiple adhesive suppliers.

Temporary bonding/debonding was introduced for compound semiconductors more than 10 years ago, but in order to be ready for memory manufacturing, major changes to the equipment were required. The new EVG850 "XT Frame" Temporary bonding and debonding system is optimized for high volume memory manufacturing.

Wide I/O DRAM was the driving force that pushed TSV manufacturing in general and thin wafer processing in particular into high volume manufacturing readiness. For thin wafer processing, LowTemp ZoneBOND has enabled a standardization of equipment and processes. The open platform for adhesives has generated a versatile supply chain with multiple adhesive suppliers. The new equipment generation features integrated advanced process control on the module level, high throughput and optimized wafer cassette logistics.

Acknowledgement

ZoneBOND™ is a trademark of Brewer Science, Inc. LowTemp®, EZR® and EZD® are registered trademarks of EV Group.

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RELIABILITY

Bias temperature instability mechanisms

CHRISTOPHER L. HENDERSON, *Semitracks, Inc., and* **DAVID W. ROSE**, *Keithley Instruments, Inc.*

NBTI is considered to be one of the most difficult reliability challenges facing the semiconductor manufacturing community today.

Bias temperature instability (BTI), particularly negative BTI (NBTI) in p-channel transistors, affects small feature size devices and is quite difficult to reduce or eliminate. As feature sizes become smaller, the effects of NBTI become more pronounced, resulting in increases in threshold voltage and decreases in drain current and transconductance in p-channel devices. NBTI results from a positive charge buildup in p-channel transistors. It occurs at low negative gate-to-source voltages and does not result in an increase in gate leakage current. Rather, it affects off-state drain-to-source leakage and reduces the drive current. Generally, this problem is worse than standard hot carrier degradation because it results in permanent interface traps being generated, reducing device lifetime.

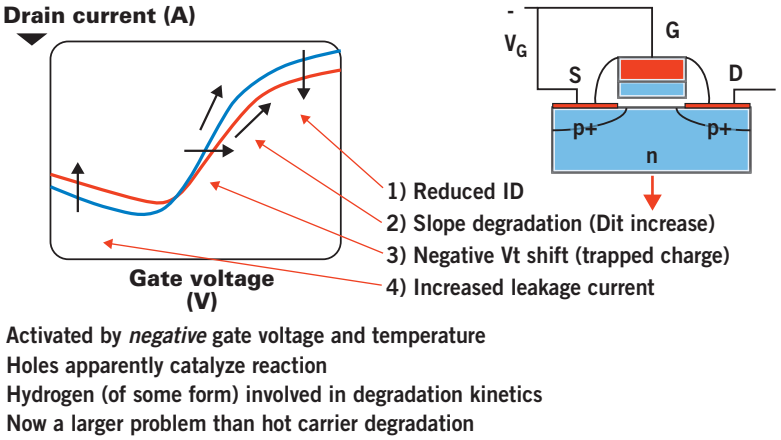

FIGURE 1. Typical results before and after a bias temperature stress on a 0.25-micron channel length transistor. Stress applied at 250°C for 50 hours at an electric field of 4.3 megavolts/cm.

Although the NBTI phenomenon has been well known for years, it was a controllable problem in earlier CMOS devices. The problem resurfaced around 1990 with the introduction of dual-doped polysilicon gates, but hot carrier effects were more dominant during that timeframe. Hot carrier effects were brought under control by drain and channel engineering, and voltage reduction. Now, aggressive scaling has made NBTI more problematic than hot carrier effects.

NBTI occurs mostly in p-channel MOSFETs when either (a) a negative bias is applied to the gate, or (b) the DUT is used at an elevated temperature. The effect is much more significant when both a negative bias AND an elevated temperature occur. It results from holes migrating to the silicon-oxide interface and is manifested by the current-voltage characteristics becoming unstable. This is accompanied by reduced drain current in the linear saturation regime, slope degradation that indicates an increase in interface trapped charge, negative threshold voltage shifts that indicate positive trapped charge, and an increase in off-state leakage current in certain instances (**Fig. 1**).

Holes apparently catalyze the reaction, so holes are needed at the silicon-oxide interface. Researchers believe that hydrogen in some form is involved in

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the degradation kinetics. This phenomenon is not as prevalent in n-channel MOSFETs because they are electron majority carriers, but they can have the less common PBTI problem. One possible reason why PBTI is less of a problem is that nitrogen is used in p-channel transistor gate oxides to block boron penetration.

NBTI typically increases with decreasing channel length. This is due to the increased contribution from the source and drain overlap regions. It can be quite pronounced in deep submicron technologies. At 90nm channel lengths, the change in threshold voltage can exceed 100mV and the change in drive current can approach 10% using the stress conditions in Fig. 1. In addition, the off-state leakage for the transistor after stressing is typically between one and two orders of magnitude higher than before stressing.

NBTI effects increase as oxide thickness decreases. For example, threshold voltage (V_{TH}) can increase by almost an order of magnitude as oxide thickness is decreased from 40 angstroms to 20 angstroms.

Important NBTI processes

Three processes associated with NBTI and its measurement should be understood:

- Relaxation processes
- Fast vs. slow measurement methodologies
- Relationship of V_{TH} shifts with interface traps

Through a charge pumping measurement technique, Vincent Huard [1] of ST Microelectronics has shown that relaxation of the interface traps is only a small part of the relaxation of the V_{TH} shift. The thermal activation energy of V_{TH} is much greater than the thermal activation of the interface traps. If the interface traps accounted for the majority of the threshold voltage shift, one would expect the two to have similar thermal processes, and therefore similar activation energies, which is not the case. This indicates that there is something else occurring involving a positive charge. As discussed below, this is closely related to measurement methodologies and conditions.

The measurement techniques for NBTI are somewhat different than for other hot carrier mechanisms. A typical measurement scenario uses a parameter analyzer, with the test taking about 10 seconds. One can then extract DV_{TH} using SPICE models and extrapolating down from the maximum slope to the x-axis. Another technique is to hold the gate voltage constant for the majority of the measurement time, change it for a few milliseconds and add a drain bias during this time, as shown in the two graphs on the lower portion of **Fig. 2**. In this scenario, the charge in the gate does not have time to relax. One can measure the drain current and then extrapolate back to get the threshold voltage. If you compare the conventional DC technique with an "on the fly" measurement, the change in threshold voltage is higher by a factor of ten when using an "on the fly" method. More importantly, there is also a change in the slope. This relates to whether the mechanism involves interface traps or fixed charge.

In contrast to a power law dependency, sometimes a linear-log time dependence in DV_{TH} is observed. This eliminates the possibility of a drift component, which researchers initially thought was occurring. Mickael Denais [2] discovered that the threshold voltage shift is correlated with the amount of hole current injected. This can be measured through carrier separation techniques. The results of his study point to a positive charge rather

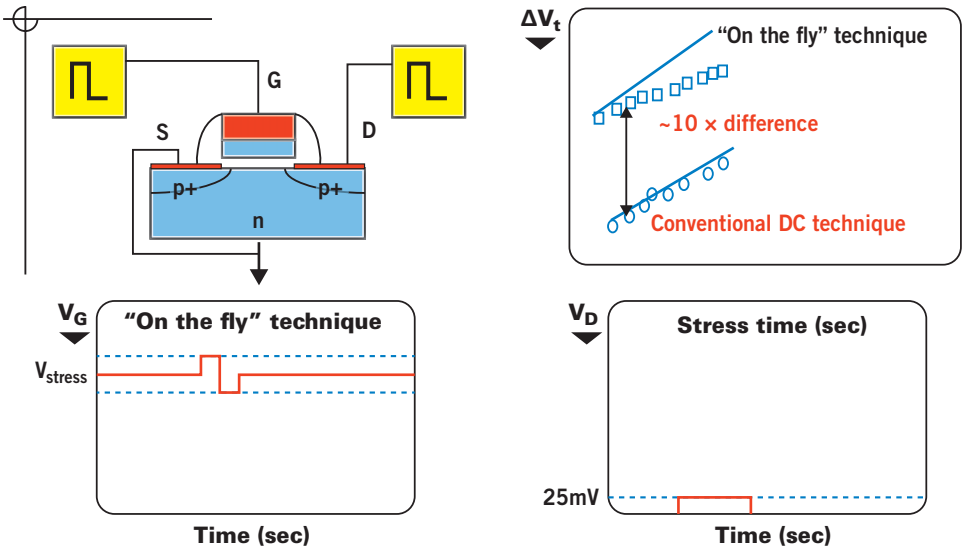

FIGURE 2. Large differences in DV_{TH} shifts are observed between "fast" and "slow" measurements. V. Huard, IRPS 2004.

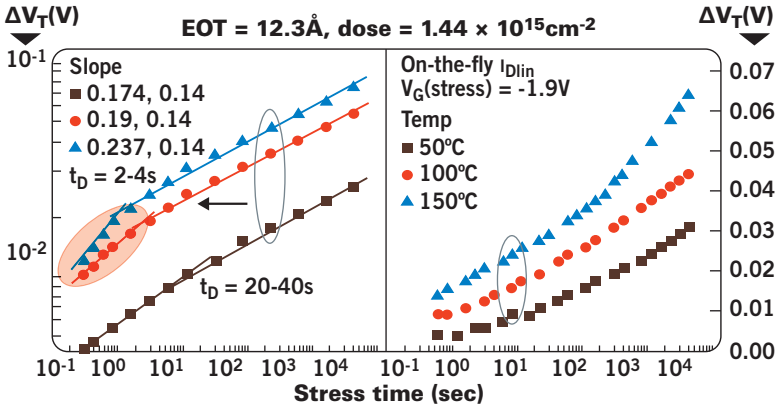

FIGURE 3. Stress-measurement delay time and test temperature clearly affect results.

than interface traps. This charge could be protons, positively charged silicon, or even H_3O+. Denais also verified relaxation of the V_{TH} shift, the magnitude of which is greater at higher positive voltage but eventually reaching a saturation level, indicating this is most likely a positive charge process.

Implications on measurement methods

Dhanoop Varghese [3] and his co-workers have studied the effects of measurement conditions on NBTI and its V_{TH} degradation. It was found that for a fixed gate voltage, the slope of the DV_{TH} vs. stress time curve varies with the drain voltage used in the measurement, stress temperature, and stress-measure delay time. The slope is greater for higher temperatures, longer delay times, and lower drain (measurement) voltages. A similar relationship is also apparent when examining the interface traps, but the effect is much less pronounced.

Varghese also found there is an Arrhenius dependency in this behavior by measuring the time delay effect at two different temperatures. He modeled this phenomenon using a Reaction-Diffusion simulation with H_2 hydrogen, showing there is good correlation between the data and the simulation. This indicates that the underlying mechanism is not hole trapping or charge trapping but rather some form of diffusion. The slopes of the lines that fit the data indicate molecular hydrogen or H_2 as the species.

These results underscore the need to make ultra-fast measurements. This can be seen clearly in **Fig. 3**, which shows the threshold voltage shift over many orders of magnitude of time. Notice that there is a change in slope below 2 to 4 seconds. The increase in slope suggests a dispersive-type process or some type of trapping and detrapping. When the time is longer, there is more of a diffusion phase, i.e., NBTI is a reaction-diffusion process. Holes react at the interface, releasing something, most likely hydrogen, which then diffuses. The process is diffusion limited rather than reaction limited. The Power Law takes over for the diffusion process. The process follows Arrhenius behavior at longer times, but the temperature effect is nonlinear.

Varghese and his group reached the conclusion that under most conditions these phenomena are strictly related to interface traps. Arrhenius plots of data collected for devices having different oxide thicknesses, different charge doses, different electric fields, and different doses of nitrogen, all fall nicely on a line that indicates a thermal activation energy of 0.6 eV. They also get an *n* value of about 1/6, which is consistent with molecular hydrogen diffusion.

Conclusions

Researchers agree on several aspects of NBTI. NBTI is a hole catalyzed reaction that has a pronounced effect on p-channel transistors, and is quite difficult to reduce or eliminate, particularly in devices with short channel lengths. NBTI field dependence is due to the reaction phase, not a field drift component. The damage increases the threshold voltage shift. Interface traps are certainly involved, but there may be another component such as fixed charge as well.

References

1. V. Huard et al, *International Reliability Physics Symposium Proceedings (42nd Annual IEEE IRPS),* 2004, pp 40-45, IEEE International.
2. M. Denais et al, presented at IEDM 2004, in *IEEE Transactions on Device Materials Reliability, vol. 4,* 2004. pp 715-722, IEEE International.
3. D. Varghese et al, "Material dependence of hydrogen diffusion: Implications for NBTI degradation," in *IEDM Technical Digest,* 2005, p. 705, IEEE International.

PACKAGING

TSV inspection in 3D advanced packaging applications

REZA ASGARI, *Rudolph Technologies, Inc., Flanders, NJ.*

Laser triangulation provides fast, accurate and repeatable 3D measurement of TSV nails and microbumps.

Three-dimensional integrated circuits (3D ICs) using through silicon vias (TSVs) are gaining momentum as more and more technology challenges are being successfully addressed. Development projects are ongoing at semiconductor companies around the globe and some manufacturers have 3D ICs in production. 3D ICs offer several advantages such as faster communication, higher I/O, smaller footprint, lower power consumption, and more. It is safe to assume 3D packaging is here to stay.

TSV technology is a key technology for 3D ICs. Vias are etched into the silicon and filled with copper. The back side of the wafer is then thinned, typically using a combination of grinding and CMP, to reveal the end of the copper fill above the wafer surface (**Fig. 1**). This is often referred to as a copper nail. The height of these nails typically varies from 1 micron to 5 micron. A copper nail on one IC and a micro bump on another are used to stack two ICs to develop a 3D device. The height and co-planarity of the nails are critical parameters that must be correct to ensure the connectivity and, therefore, require inspection and measurement (**Fig. 2**).

Laser triangulation is a measurement technique that uses a scanned laser to collect 3D data points which can then be used to build a 3D model of the surface features. The speed and accuracy of laser triangulation have made it the dominant technology for three-dimensional characterization of solder bumps

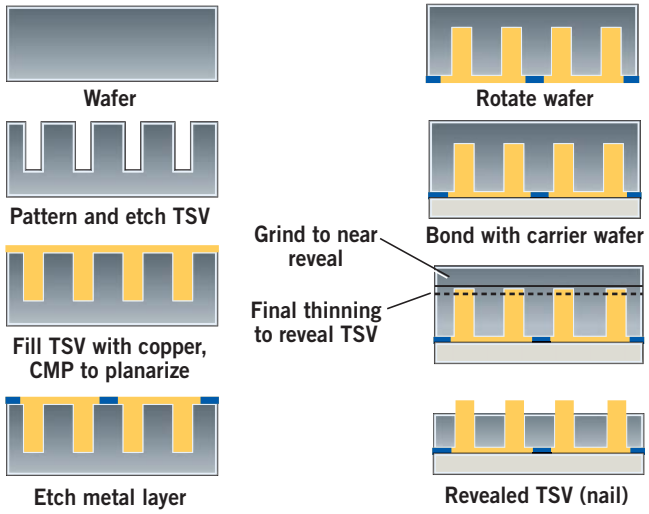

FIGURE 1. TSV nails are formed by filling vias, usually with copper, etched into the wafer. The wafer is then flipped and mounted to a carrier wafer. A combination of processes is used to remove material from the wafer surface, leaving the ends of the copper fill protruding above the surface. These TSV nails will be matched to corresponding solder bumps on a stacked wafer or die to provide electrical connections. (Courtesy of Sematech)

used in conventional packaging techniques such as flip chips. Microbumps and TSV nails used in 3D ICs are typically smaller, more closely spaced and more numerous, having diameters and heights as small as a few micrometers. The number of bumps and nails used in 3DIC schemes has grown explosively, with current roadmaps calling for as many as 1,000,000 per die and 60 million per wafer.

Existing metrology tools are significantly challenged

REZA ASGARI *is wafer scanner product manager, Rudolph Technologies, Inc., Flanders, NJ.*

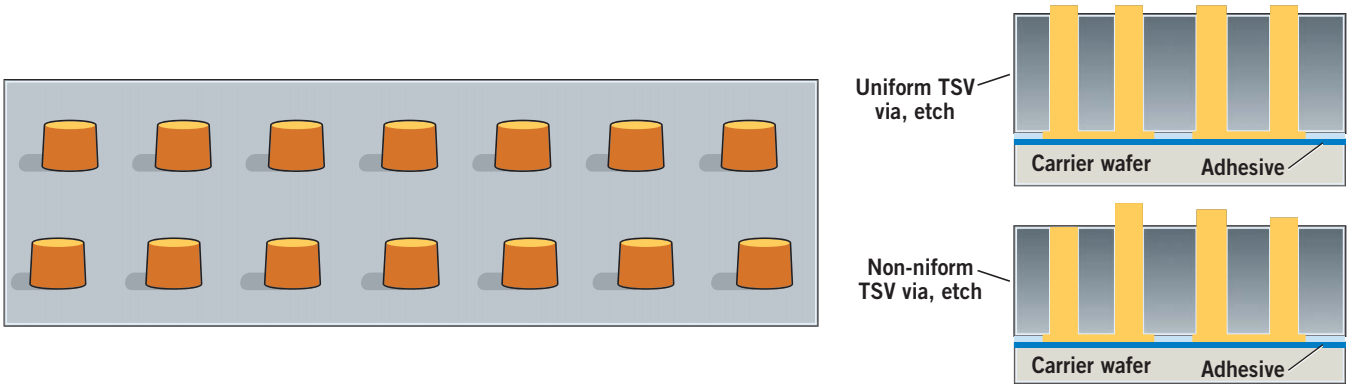

FIGURE 2. On the left is an illustration representing TSV nails. The diagrams on the right illustrate one type of fault: non-uniform etching has created vias of varying depths, causing variations in nail height and failure of some nails to reveal at all.

to provide the speed and precision required to maintain sufficiently narrow process windows and ensure high yields. Heights of only a few microns require submicron 3D measurement precision. Diameters as small as 5 microns pose equally daunting challenges for 2D measurement. The large number of features places a heavy load on data storage and processing facilities. Finally, the measurement system must strike an optimal balance between precision and throughput if it is to be used in production.

The inspection system (Wafer Scanner™ 3880, Rudolph Technologies) uses laser triangulation for 3D measurements of bump height and co-planarity (**Fig. 3**). A laser on the wafer surface at an angle of 45 degrees and focused to a spot size of 5 µm scans a line 1.4 mm in length on the wafer surface while the wafer is transported in a direction perpendicular to the scanned line. Multiple scans provide coverage of the full wafer surface. A lens collects the reflected/scattered laser light and focuses it on a position sensitive detector. Changes in the location of the collected light on the detector provide height measurements with a resolution of 54 nm. The system has a 28 µm depth of focus and an 8 MHz data acquisition rate. The combination of high scanning rate and wide scan path permits 100 percent 3D scanning of a 300 mm wafer in 23 minutes, at a throughput of nearly 2.5 wafers per hour.

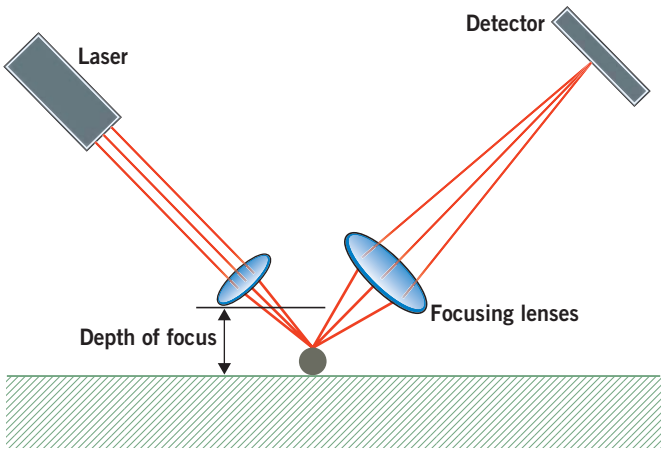

FIGURE 3. Laser triangulation uses a finely focused laser and a position sensitive detector to measure feature height.

During operation the system scans the wafer surface, simultaneously acquiring height data from both the tops of the nails and the surrounding wafer surface. The spacing of the data points can be varied to optimize efficiency. The system can display 3D data points collected on individual features as well as calculating various feature, die and wafer level results. Using data from the top of the nail and the immediately adjacent wafer surface to calculate height improves the accuracy and repeatability of the measurements.

A unique staggered scan technique further enhances the repeatability of height measurements. Staggering the scan increases the pitch in the direction of the line scan and reduces the pitch in the direction of the wafer movement, effectively spreading the data points more evenly over the wafer surface with no penalty in throughput.

Laser triangulation provides fast, accurate and repeatable 3D measurement of TSV nails and micro-

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EUV SOURCES

Laser-Produced Plasma Light Sources for EUV Lithography

DAVID C. BRANDT, **IGOR V. FOMENKOV**, **BRUNO M. LA FONTAINE** *and* **MICHAEL J. LERCEL**, *Cymer, Inc., San Diego, CA*

LPP sources are the leading source technology for EUV lithography. Today's sources have an average power of 50W at intermediate focus, at 80% duty cycle using pre-pulse technology.

Laser-produced plasma (LPP) sources have been developed as the primary approach for EUV lithography for optical imaging of circuit features at sub-22nm design rules. EUV lithography is the front runner for next generation critical dimension imaging after 193nm immersion lithography for critical layer patterning. Leading device manufacturers have taken delivery of first generation EUV scanners in 2011 and are ramping those tools to pilot-line capability in 2012.

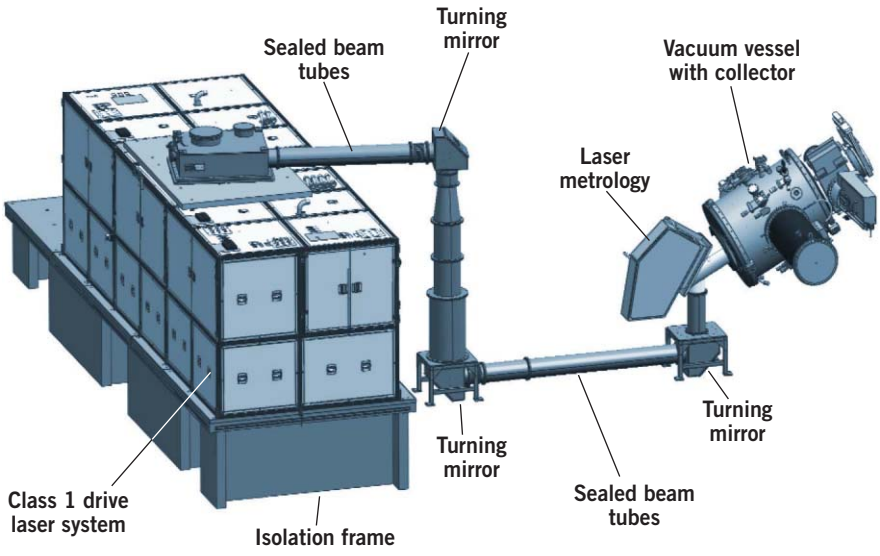

FIGURE 1. Scale drawing of laser produced plasma source.

The LPP source architecture is shown in **Fig. 1**. The three major subsystems of the source are the drive laser, the beam transport system (BTS) and the source vessel. The drive laser is a CO_2 laser with multiple stages of amplification to reach the required power level of up to 30 kW. It is operated in pulsed mode at 50 kHz with radio-frequency (RF) pumping from generators (not shown) operating at 13.56 MHz. The laser is typically installed in the sub-fab along with its RF generators. The laser beam is expanded as it leaves the drive laser to lower the energy density on the BTS mirrors. The laser and BTS are completely enclosed and interlocked to meet laser Class 1 requirements. The BTS delivers the beam to a focusing optic where the CO_2 light at 10.6 μm wavelength is focused to a minimum spot size inside the vessel. A droplet generator delivers liquid tin droplets of 30 μm diameter at 50 kHz repetition rate; both laser pulse and droplet are steered and timed to ensure proper targeting. The laser pulse vaporizes and heats the tin into a plasma cloud of critical temperature and density. The EUV light emitted by the plasma is collected and

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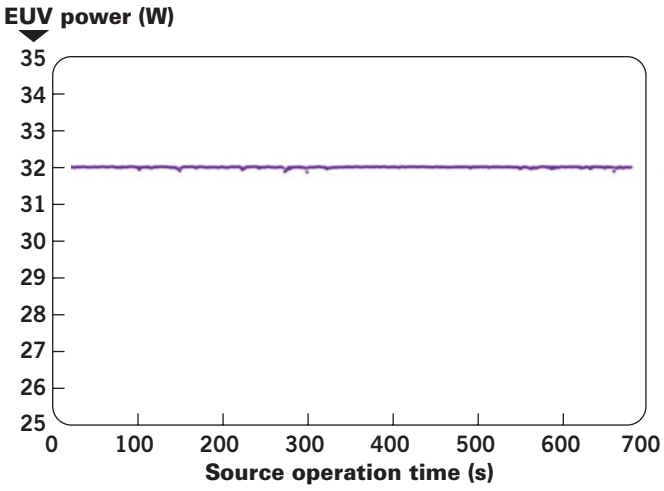

FIGURE 2A. 32W average power with better than ±0.5% dose stability.

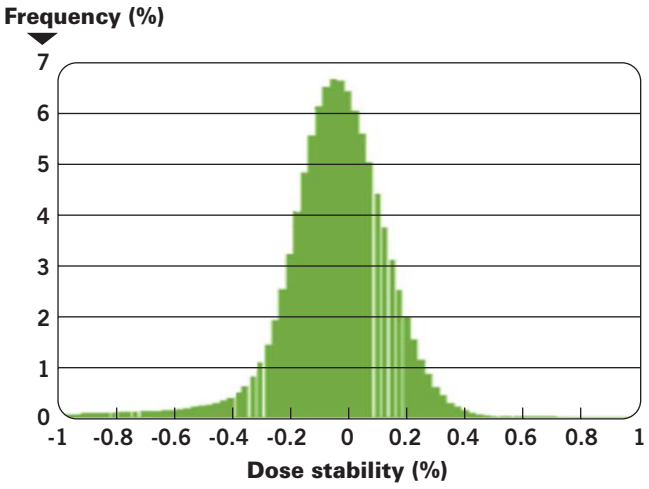

FIGURE 2B. Dose stability histogram at 32W.

reflected with a multilayer-coated ellipsoidal mirror to the intermediate focus (IF) where it passes through a small aperture into the scanner volume that houses the illumination optics.

Recent test results are shown in **Figs. 2a and 2b.** The test configuration included upgrades to the drive laser which allow continuous operation of the source during the full die scan and operation at high duty cycle. 32W average power with better than ±0.5% 3σ dose stability is shown. During this test the source was running at 92% duty cycle with burst duration of 2 seconds.

The test source configuration also includes a pre-pulse capability, which can operate at the full repetition rate of the source (50kHz). The pre-pulse technology allows the droplet to be conditioned by a first laser pulse with energy less than that of the main heating pulse, which then strikes the target after it has developed into a tin vapor cloud of lower density which enables a higher conversion efficiency (CE) into EUV energy at λ =13.5nm. Testing was conducted to characterize the pre-pulse operational mode; the results are shown in **Fig. 3a and 3b**. The duty cycle of the source was increased up to 80% where the source was operated at an average EUV power of ~50W.

At 20% duty cycle the average power in the burst was approximately 90W (open-loop operation) using pre-pulse technology, as shown in **Fig. 3b**. This corresponds to 18W average power; however, it is a significant milestone that demonstrates the capability of the

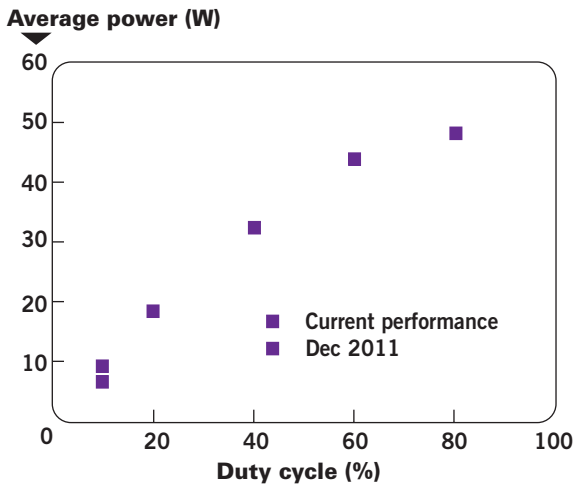

FIGURE 3A. 50W average power at 80% duty cycle using pre-pulse.

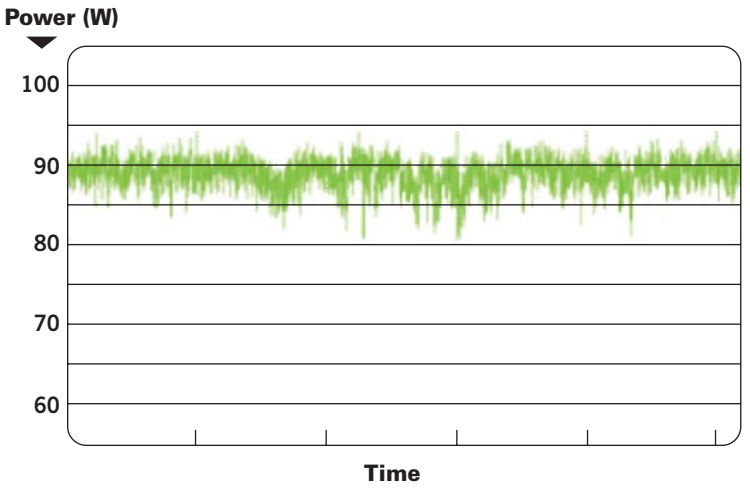

FIGURE 3B. 90W burst power at 20% duty cycle (18W average power) using pre-pulse.

EUV SOURCES

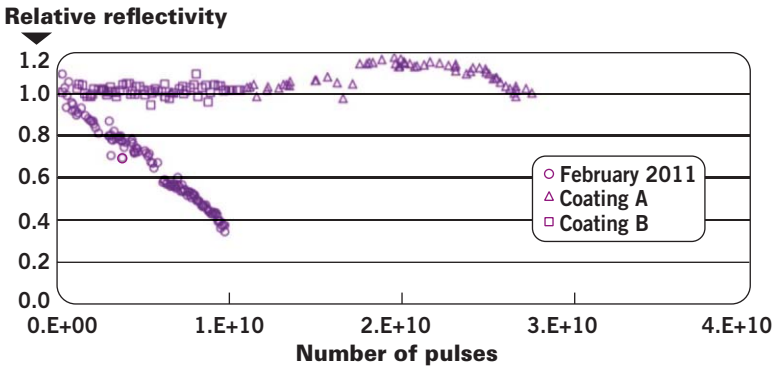

FIGURE 4. Recent collector lifetime results for sources in the field.

source to generate EUV power levels very close to the final 100W target.

Significant advancements in collector lifetime were made in 2011, as shown in **Fig. 4**. This improvement is primarily due to the increased robustness of the collector reflective coatings now being used. The open circles were the results of our original life test completed in 2010. The results of two new coatings on collectors installed on sources at chipmakers show the current performance and their associated significant lifetime improvement. Continued advancement of coatings and debris mitigation techniques are expected to enable further increases of the collector lifetime to meet the ultimate goal of one year.

LPP sources are the leading source technology for EUV lithography. Eight LPP sources have been built and are operational at leading device makers. An average power of 50W at intermediate focus at 80% duty cycle using pre-pulse technology has been shown. Collector lifetime of >30 billion pulses while maintaining high average reflectivity are being produced in volume. The combination of 10.6 μm laser light and Sn droplet source element is proving to provide reliable operation, with the sources in the field having now reached pilot line capability. ◆

PACKAGING

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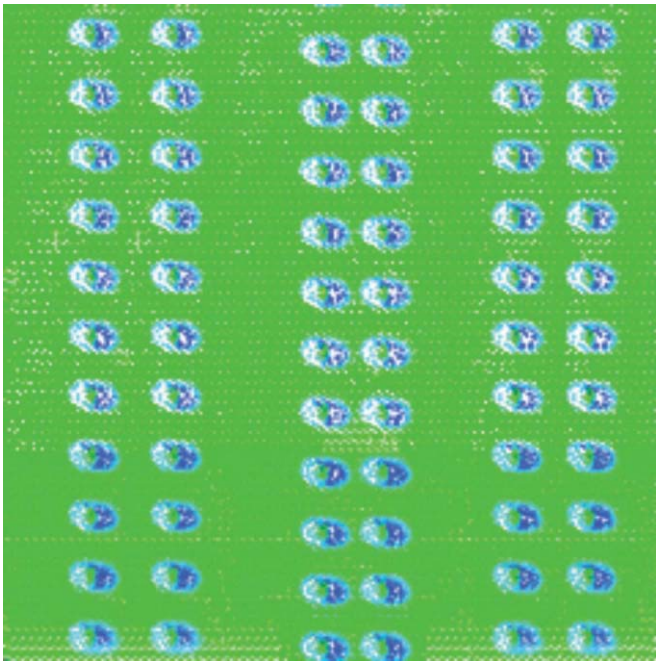

FIGURE 4. a) 3D laser top view image.

FIGURE 4. b) 3D laser side view image.

bumps. In combination with camera-based 2D measurements it provides a complete metrology and defect inspection solution. The multiplicity of data points acquired on the top of each feature by the ultra-high resolution detector ensures measurement repeatability. The system can also measure heights of closely-spaced features where shadowing prevents the acquisition of data in some areas between bumps. The 8 MHz sampling rate and over 1 mm scan width provide production worthy throughput without sacrificing accuracy and repeatability. With feature sizes and pitches sure to decrease and numbers headed for tens of millions per wafer, the ability to tightly control processes and detect defects are essential to the success of 3DIC technologies and the profitability of 3DIC manufacturers. ◆

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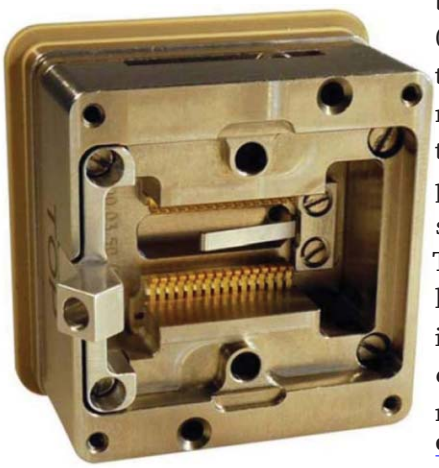
New Products

Inertial sensor development platform

The SWS61111 (formerly SWP210) tool can be used to evaluate an inertial sensor, such as a gyroscope or accelerometer, to understand sensor behavior and performance with complete interface electronics. The SWS61111's high performance inertial sensor interface ASIC, the SWS1110 (formerly SWI210) is a configurable ASIC that offers ultra-low noise front-end, highly configurable open- and closed-loop (force-feedback) operation and high voltage capabilities. MEMS and ASIC designs use SWS61111 to evaluate issues such as parasitic modes of oscillation, electrical and mechanical coupling, high-volt effects and temperature behaviors, and also to evaluate SWS's SWS1110 high performance ASIC, which is offered in die format with optional customization. The SWS61111 consists of a programming board, an ASIC daughter board with a sensor placeholder, a USB interface, and associated PC software. **Si-Ware Systems**, Cairo, Egypt, http://www.si-ware.com.

High-power Kelvin test contactor

The ecoAmp Kelvin contactor meets the needs of high-voltage/ current test with high thermal and mechanical stability, to 500+ Amperes. The contactor is based on Multitest's Cantilever technology. It has low, stable contacting resistance to achieve equal current symmetry over I/Os within the contactor. Maximum inductance is 4.5nH for 0.5mm pitch, in -60 to +175°C. Thermal management within the contactor supports temperature stability during test. The ecoAmp offers a lifespan of 1 million insertions. **Multitest**, Rosenhim, Germany, www.multitest.com/ecoAmp.

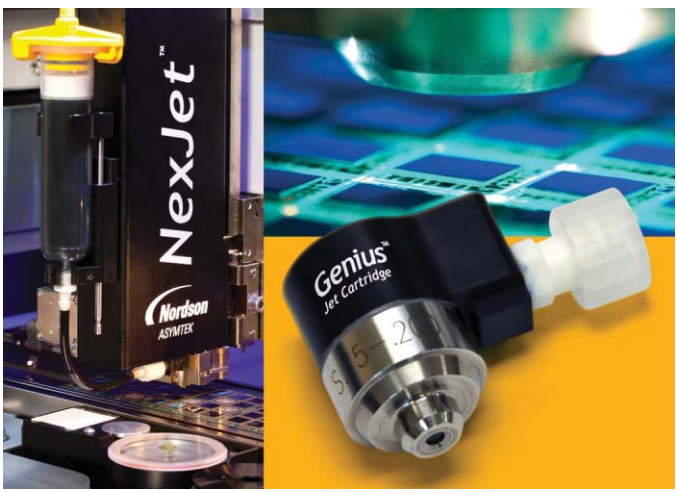


LED test suite

TEMPO 24 (Thermal Electrical Mechanical Photometric Optical) tests combine the IES LM-79-08 photometric test with nearly a dozen other LED performance tests, including binning and color point evaluation, chemical compatibility, and TM-21 lifetime projection tests to ensure reliability in LED luminaires. Cree currently provides TEMPO Services out of its Durham, NC and Santa Barbara, CA centers. **Cree**, Durham, N.C., www.cree.com.

One-piece jetting cartridge

The NexJet System for jetting uses a newly designed jet cartridge and new software control for semiconductor packaging applications such as flip chip underfill, CSP,



BGA, PoP underfill, precise coating, and adhesive dispensing. The Genius Jet Cartridge one-piece jet is quickly and easily removed without tools. The cartridge dispenses up to 50 million cycles before replacement. It has built-in memory to store usage data like the number of cycles and cartridge type, which is communicated to the jetting tool and compared to the recipe for process control. The NexJet System's precision software control enables jetting of low- and high-viscosity fluids. **Nordson ASYMTEK**, Carlsbad, CA, www.NordsonASYMTEK.com.

High-throughput defect inspection/metrology/review cluster tool

The CIRCL suite -- a new generation of KLA-Tencor's LDS front side macro defect inspection module; a new, modular edge inspection, profile and metrology module based on KLA-Tencor's VisEdge technology; a dedicated wafer backside inspection module; and a flexible optical defect review and classification module -- can be implemented at lithography, outgoing quality control, and other process modules. The cluster tool monitors the wafer's front and back side, and edge for defects. In parallel it measures wafer edge profile, edge bead concentricity, and macro overlay error. Data collection is governed by DirectedSampling, which uses results from one measurement to trigger other types of measurements as needed. The tool detects and bins macro defect types on the front side of the wafer, from particles to defocus defects spanning several die, to full-wafer defects such as missing resist. It catches low percentages of non-critical defects. A reticle ID check verifies that the correct reticle was used for printing. Macro overlay error monitoring checks layer-to-layer pattern registration. Back-side inspection finds particles and scratches, while edge defects are detected and binned. Edge Bead Removal (EBR) metrology monitors film concentricity and edge integrity to prevent delamination defects. Edge profile measurements are automated and calibrated to identify excursions that can result in water bead leakage or film delamination during immersion lithography. Automated high-resolution optical defect review and automated classification of front-side, back-side and edge defects aid in defect source identification. **KLA-Tencor Corporation,** Milpitas, CA, www.kla-tencor.com.

Ion beam deposition (IBD) tool

The SPECTOR-HT ion beam deposition (IBD) tool performs thin-film deposition for optical products. It is designed to deposit quality films at a lower cost than PVD, evaporative coatings, and ion-assisted deposition. The SPECTOR-HT reportedly offers up to 400% higher throughput, 300% better target utilization and 50% higher material uniformity over previous SPECTOR generations. The IBD tool is fully automated, achieving accelerated deposition rates at speeds comparable to PVD. It delivers an increased deposition rate on lot sizes up to twice as large as those in previous SPECTOR generations. **Veeco**, Plainview, NY, www.veeco.com.

Benchtop metrology system

The Optiv Classic 321GL tp benchtop vision-measuring metrology system suits electronics and precision parts inspection, including micro-holes, fiber optics, filters, and more. It features 6.5x motorized CNC zoom optics for 0.002mm accuracy. Touch probes can be added for multi-sensor measurement. The Classic 321GL tp boasts calibrated lighting, a high-resolution color CCD camera, a laser locator and an 8-segment LED dual angle ring light, improving edge detection. The Classic 321GL tp includes PC-DMIS Vision image processing software and full online 3D CAD capabilities for live programming of the machine to compare measured values to nominals. The software's MultiCapture feature finds all 2D characteristics in the field of view and measures them simultaneously for optimized stage movement. **Hexagon Metrology, part of the Hexagon AB Group**, North Kingstown, R.I., www.hexagon.com.

Thin wafer debond and cleaning tools

A lab-scale suite of thin wafer separation and post-debond cleaning tools target compound semiconductor device processing. Cee 1300CSX is a semi-automatic thermal debonder for high-temperature slide-off debonding of thinned III-V and CS materials (GaAs, GaN, InP, and SiC) in a laboratory setting. The ZoneBOND low-stress, room-temperature debonding separation tool has compliant seal clamps and fail-safe abort hardware to accommodate thinned III-V and CS materials. Higher precision in this generation of the tool targets highly mechanically and thermally sensitive debonding materials on 2-12" wafers. Cee 300MXD megasonic cleaning system applies uniform acoustic energy to spinning substrates, gently removing adhesive residues and contaminants without damaging fragile device structures. **Brewer Science**, Rolla, MO, http://www.brewerscience.com.

Die attach adhesives

DELOMONOPOX die attach adhesives promise strong mechanical/environmental protection, low-temperature cure, and compatibility with various chip packaging substrates

(silicon, epoxy, gold, PEI, PET and PEN). DELOMONOPOX adhesives cure in seconds at low temperatures. The adhesives can be used to bond and encapsulate die, protecting against mechanical damage, humidity, and extreme temperatures. DELO's die attach adhesives are built on the same chemical basis as its chip encapsulants for dam and fill. DELOMONOPOX products are available as unfilled non-conductive products, or filled for grounding or conductive products. **DELO**, Sudbury, MA, www.DELO.us.

Higher-throughput vacuum pumps

The STP-iXR1606 series magnetically-levitated turbo-molecular pumps (TMP) with fully integrated onboard controllers improve throughput from 40-90% with a new rotary design. The pumps' fully integrated controller eliminates connection cables and racks, and features a small power supply. The STP-iXR1606 series delivers high reliability in dirty environments with equivalent IP54 protection against dust and humidity. It has I/O remote, RS232C, RS485 and STP-link standard communication ports, with Profibus and DeviceNet available as options. The magnetically-levitated TMPs require no maintenance. **Edwards Limited**, Crawley, West Sussex, UK , http://www.edwardsvacuum.com/.

Touchscreen display manufacturing tool

The Rainbow Process Unit touchscreen display manufacturing method reportedly reduces cost and improves speed over current methods, with environmental benefits. It produces fine line circuitry down to 5µm: coating, imaging and developing a substrate in an automated process. Its proprietary etch wet resist is 100% solids- and solvent-free, and does not require pre-drying before imaging. UV LEDs and standard photo-tools create tracks and gaps of 20µm and below. Power consumption on the unit averages 3kW. The process can be done additively using an imaged seed layer to create electroless plated nickel or copper with a Rainbow imaged plating resist to create tracks. It can also be done subtractively using sputtered metal on plastic using a Rainbow imaged etch resist to create tracks. Grid patterns of 5 x 300µm pitch offer more conductivity than ITO or conductive polymers, while maintaining good transparency. **Rainbow Technology Systems,** Hillington, Scotland, www.rainbow-technology.com.

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June 2012, Volume 55, Number 5 • ***Solid State Technology*** ©2012 (ISSN 0038-111X) Periodicals postage paid at Tulsa, OK 74112, & additional mailing offices. Published 9x per year (Jan, Mar, Apr, May, Jun, Jul, Sep, Oct and Nov) by PennWell Corp., 1421 S. Sheridan Rd., Tulsa, OK 74112. **Subscriptions:** Domestic: one year: $258.00, two years: $413.00; one year Canada/Mexico: $360.00, two years: $573.00; one-year international airmail: $434.00, two years: $691.00; Single copy price: $15.00 in the US, and $20.00 elsewhere. Digital distribution: $130.00. You will continue to receive your subscription free of charge. This fee is only for air mail delivery. Address correspondence regarding subscriptions (including change of address) to: *Solid State Technology*,, PO Box 3425, Northbrook, IL 60065-9595, sst@omeda.com, ph 847-559-7500 (8 am – 5 pm, CST). PRINTED IN THE USA. GST NO. 126813153. Publication Mail Agreement No. 40052420. **POSTMASTER:** Send address changes to *Solid State Technology*, PO Box 3425, Northbrook, IL 60065-9595. Return Undeliverable Canadian Addresses to: P.O. Box 122, Niagara Falls, ON L2E 6S4.

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SEMI educates policymakers on 450mm transition

With estimates for the R&D cost of 450mm wafer transition running in the tens of billions of dollars, public-private partnerships will have a critical role throughout the world. Already, the State of New York is anticipating a $400 million investment in advanced chip research over the coming years and the European Union is funding research in a variety of Key Enabling Technologies including micro-electronics manufacturing. Many countries around the world will see next-generation 450mm wafer tools and fabs as critical features of a national competitiveness strategy. In anticipation of the increased role in government support for advanced chip manufacturing technology, SEMI has been actively engaged in education and other efforts with policymakers around the world.

As the topic of the transition to 450mm becomes more relevant at industry seminars, conferences, and boardrooms, SEMI has met with over 50 Federal and State government officials to discuss the likely impacts and requirements on a chip industry transition to 450mm wafers.

Along with a group of member company representatives, SEMI recently met with senior staff for California Governor Jerry Brown in the state capital of Sacramento.

JONATHAN DAVIS, *president, SEMI Semiconductor Business.*

With 200 SEMI member companies headquartered in California, semiconductor manufacturing is high-priority issue for the Governor Brown's office. Gov. Brown has shown great leadership in not only understanding the needs of the semiconductor equipment industry in California, but the need for a strong domestic industry infrastructure across the nation.

On the national level, Representative Mike Honda (D-CA) has been fully engaged in learning more about the semiconductor equipment industry, as he represents a large portion of Silicon Valley in the House of Representatives. Rep. Honda sits on the powerful Appropriations Committee which writes the annual bills that directly fund the federal government. The Congressman visited SEMI headquarters in February to hear directly from SEMI members about the challenges that they are facing and meet with SEMI staff to hear their policy concerns. Rep. Honda also organized a briefing for other Members of Congress and their staffs in Washington, D.C. to hear from the President of the SEMI Semiconductor IC Business Unit Jonathan Davis about the semiconductor equipment industry overall, and about the 450mm transition in particular. Rep. Honda also penned an op-ed in The Hill, a Washington political newspaper, about the need for the U.S. government to compete with other nations in supporting the 450mm transition.

> There is much work to be done before the industry fully transitions to 450mm technology.

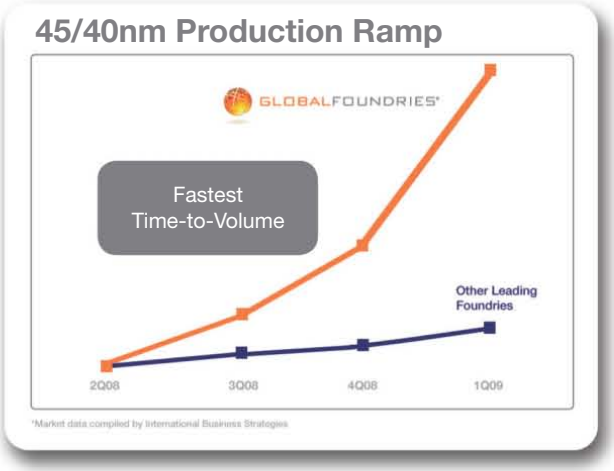
Along with Rep. Honda, SEMI has received positive support for its education efforts from Rep. Chris Gibson (R-NY) who represents a large swath of the upstate New York Capital Corridor, and whose district includes the Global Foundries Fab in Malta, NY. SEMI has also been active in working with members of both parties in the U.S. Senate including Senator Dianne Feinstein (D-CA), Senator Scott Brown (R-MA), and Senator Kirsten Gillibrand (D-NY). Each one of these Senators has significant SEMI membership in their states and has been working hard to engage on the issues surrounding the transition to 450mm.

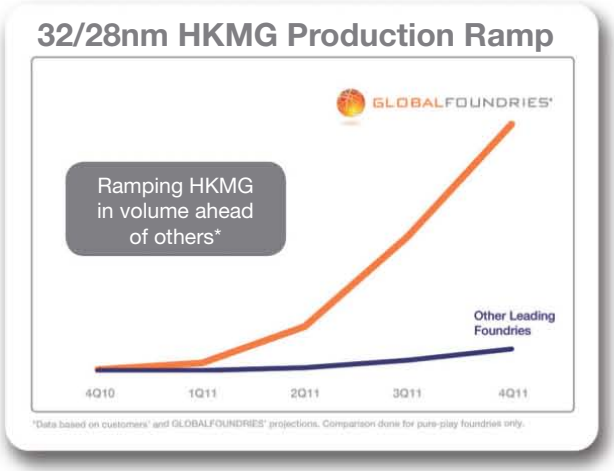
There is much work to be done before the industry fully transitions to 450mm technology. In order to be completely prepared, policymakers must be fully informed of the issues that surround the transition, and SEMI is working to ensure that they understand the ramifications of such a massive industry undertaking.

SEMI's Washington D.C. office continues to focus on key issues and holds events such as the Washington Forum and other lobbying activities to ensure that our industry's collective voice is heard. Please let us know if you would like to get involved in public policy efforts in the U.S. (contact SEMI at www.semi.org).

LEADING THE FOUNDRY RAMP IN 32/28nm WAFER PRODUCTION

GLOBALFOUNDRIES has shipped >250,000 32/28nm HKMG wafers to date. This milestone represents a significant lead over other foundries in 32/28nm manufacturing.





On a unit basis, cumulative **32/28nm shipments** for the first five quarters of wafer production are **more than double that achieved during the same period of the 45/40nm technology node ramp**, demonstrating that the overall HKMG ramp has significantly outpaced the 45/40nm ramp.

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