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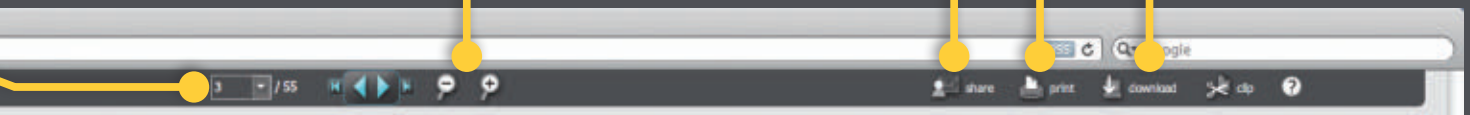

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KEYNOTE SPEAKERS

MONDAY, JUNE 24, 2013

Technologies and Business Strategies of the Future IT Industry

Mr. Yoon-Woo Lee
Executive Advisor
Samsung Electronics Co., Ltd.

TUESDAY, JUNE 25, 2013

Orthogonal Scaling to Fill Today's Fabs in the Future

Mr. Subu Iyer
IBM Fellow
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The Applied Centura AdvantEdge Mesa silicon etch system brings Angstrom-level precision to shallow trench isolation (STI), buried bit/word line, and double patterning at 32nm and below.

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How war on the Korean peninsula could affect worldwide electronics production

What would happen if half of all global production for DRAM, two-thirds of NAND flash manufacturing and 70 percent of the world's tablet display supply suddenly disappeared from the market?
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Top 10 medical applications for MEMS

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Series: Who's driving the MEMS evolution revolution?

Long-time MEMS industry insider, Howard Wisniowski takes readers with him to "visit" three exciting MEMS startups that are breaking new ground in the mobile/consumer market.
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Studying 1/f noise

In his first blog, Dr. Zhihong Liu, Executive Chairman of ProPlus 1/f noise is an important characteristic for various semiconductor devices, such as MOSFETs, BJTs, JFETs, Diode, and IC resistors.
http://bit.ly/10uhlIT

The value of innovation

Speaking at SEMI's Advanced Semiconductor Manufacturing Conference (ASMC) in Saratoga Springs, Subramani "Subi" Kengeri, vice president, advanced technology architecture, GLOBALFOUNDRIES, gave a wide-ranging overview of the challenges facing leading edge SoC semiconductor manufacturers.

He mapped out the many technical challenges facing the industry, highlighted ongoing innovations to meet those challenges, and then showed how it all meshed with market demand and cost considerations. "Everything must be related to SoC-value," he said.

In his talk, titled "Threats to Semiconductor Growth," Kengeri said huge semiconductor growth was predicted, reaching $408 billion by 2015 (from $355 billion in 2013). Mobile and foundry growth is expected to outpace the overall industry, and SoC chips designed for mobile apps are increasingly driving semiconductor technology.

> "SoC chips designed for mobile apps are increasingly driving semiconductor tech."

Yet, critical issues need to be resolved to achieve that growth, particularly in the areas of power density, BEOL RC, cost and, perhaps most importantly, time to volume. "With the technology become more and more complex, the time to volume has become a bigger and bigger challenge," he said. He said delayed time to volume equates to a delayed ROI, which could mean less revenue to build the next technology node and the next fab.

He noted SoC designs are getting larger (47% now use more than 5M gates), and they're also getting faster (37% run at 750MHz and above). There are also a larger number of clock domains, which means managing multiple macros operating at different frequencies, and more voltage domains across the chip (five different ones on average). A problem with large complex designs is that product life can be shorter than development time. He said automating design through EDA helps, but there is still a gap.

The good news is that R&D innovations, including improvements in the gate stack, stress engineering, silicides, lithography, middle- and backend-of line, and low-k dielectrics are bringing value to the overall SoC in terms of performance, power, area and cost/complexity (PPAC). "The innovation engine is running," Kengeri said.

—Pete Singer, Editor-in-Chief

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US - **MEMSIC, Inc.,** a MEMS solution provider, announced that it has agreed to be acquired by **IDG-Accel China Capital II, L.P.** and its affiliates.

EUROPE - **Silex Microsystems** joined the international European Union-funded program PROMINENT to develop new low-cost technologies for TSVs, hermetic high-vacuum seals for wafer-to-wafer bonding including advanced material deposition, advances in piezo-MEMS fabrication, and more.

ASIA - **Freescale Semiconductor** announced that the company plans to open ten new sales offices across China.

UK - **University of Manchester** researchers reported that they have developed the first graphene-based transistor with bistable characteristics.

ASIA - **Yole Développement** reported that **TSMC's** MEMS foundry business enjoyed approximately 80 percent growth in 2012, making it the largest of any MEMS open foundry.

EUROPE - **Morgan Advanced Materials** joined **SEMATECH's** International SEMATECH Manufacturing Initiative (ISMI), a program designed to improve semiconductor equipment manufacturing productivity, yield, and cost.

EUROPE - **LFoundry** confirmed the completion of the acquisition of **Micron's** manufacturing facility in Avezzano, Italy.

US - **GT Advanced Technologies** announced that it has acquired substantially all of the business of Thermal Technology LLC.

Combo MEMS inertial sensors report brisk growth in automotive market

Combo MEMS sensors for automotive applications are off to another exhilarating ride this year as revenue continues to climb, spurred by rapidly accelerating use in car safety systems, according to an IHS iSuppli MEMS and Sensors Report from information and analytics provider IHS.

Global revenue in 2013 for combo inertial sensors used in motor vehicles will reach a projected $163 million, up a notable 77 percent from $92 million last year. The anticipated increase continues a hot streak for the market, which saw a phenomenal 338 percent surge last year from just $10 million in 2011.

MEMS combo sensors

Combo inertial sensors are multiple-sensor devices integrating accelerometers, gyroscopes into a single package, providing inertial inputs to the electronic stability control (ESC) system in cars to prevent or minimize skidding.

"ESC systems are mandated in North America, Europe and in other areas where the edicts are maturing, such as Australia, Japan, Canada and South Korea," said Richard Dixon, Ph.D., principal analyst for MEMS and Sensors at IHS. "But a huge growth opportunity exists in untapped territories like China, which would significantly impact the penetration of ESC worldwide given the vast size of the Chinese market. Such gains, in turn, would provide tremendous impetus and momentum for automotive combo sensors overall."

Why combos?

Three architectures are currently possible for ESC systems in cars: on a printed circuit board as a separate ESC engine control unit (ECU); attached to the brake modulator to save cabling; or collocated in the airbag ECU. Of these three usable locations, the current trend favors placing ESC systems in the airbag ECU to achieve a smaller footprint and greater efficiency, given that there is a space constraint for the ECU in this position near the cup holder in a vehicle, which favors an architecture of reduction.

All told, as much as a fivefold reduction in space could be achieved for the sensors in a combo-sensor ESC system made by a manufacturer like Continental, compared to the same accomplished via separate sensors.

A non-combo solution also exists in the form of the sensors separately mounted on the printed circuit board. But deploying the sensors in a combo form factor saves not only on packaging cost but also on expensive real estate for the semiconductors being used, since the two sensors in the combo package share the same application-specific integrated circuit.

Cost is a factor

A paramount issue for ESC systems is cost. Cost is especially important because ESC formerly was considered an optional feature—but since being mandated by governments—it now has attained the same required status as the seat belt.

As a result, the entire supply chain and price structure for automotive combo sensors has been experiencing huge pressure, exerted from car makers down the chain. Tier 1 companies then pass on this pressure to their suppliers, accounting for the accelerated move to provide efficient combo sensor solutions for inertial sensors in the system.

Because of such pressure, some top-tier companies have indicated that only legacy businesses will use older arrangements featuring separate sensors—not a combo solution—on a printed circuit board in the future. All new car models will use combo sensors.

Top suppliers identified

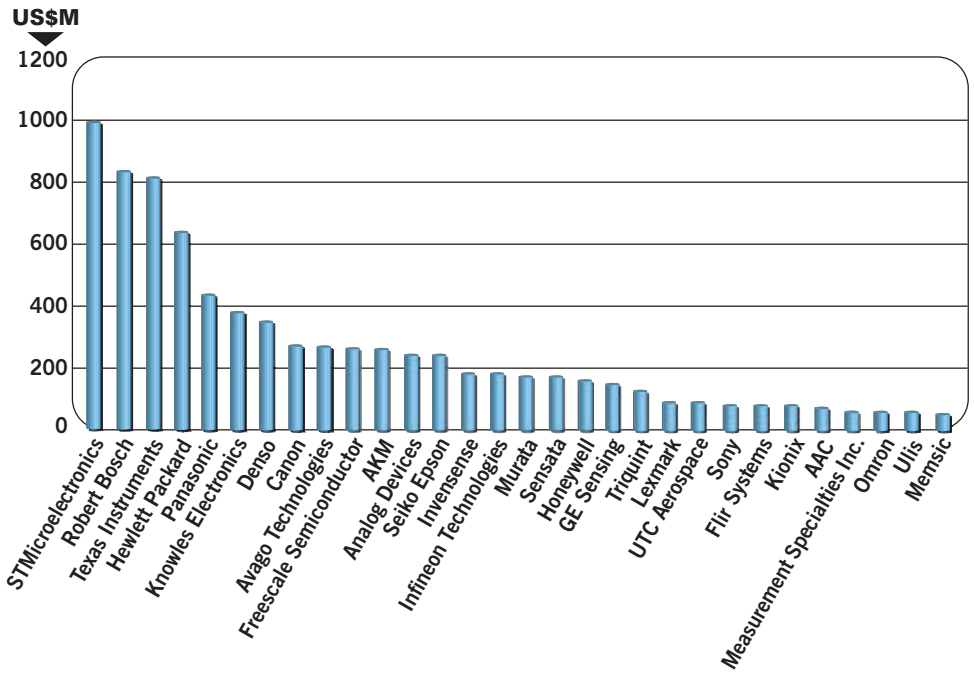
The major suppliers of automotive combo inertial sensors are Bosch of Germany and Japan's Murata (formerly VTI). Two other potential manufacturers, Panasonic of Japan and Massachusetts-based Analog Devices, will need to develop similar solutions to have a chance in the market.

For its part, Panasonic has indicated that a product will be available by 2014. Panasonic Industrial makes the gyroscope part of the solution, while Panasonic Electric Works makes the accelerometer component.

However, the two entities do not have a good track record of working together, so it remains to be seen how soon a unified combo sensor solution from Panasonic will come to market.

Meanwhile, Analog Devices is divulging little information, but it will almost certainly develop a combo sensor solution, IHS iSuppli believes, based on an analysis of developments surrounding the competition.

Top 30 MEMS companies of 2012



Source: Status of the MEMS Industry report, Yole Développement, to be released Q2, 2013 © April 2013

The fast growing market for sensors for smart phones is re-shuffling the ranks of MEMS suppliers. For the first time, suppliers of inertial sensors have surpassed the major makers of micro mirrors and inkjet heads that have long dominated the industry on Yole Développement's annual ranking of the Top 30 MEMS companies.

STMicroelectronics increased MEMS sales by ~10 percent in 2012, to become the first company with $1 billion in MEMS revenue, moving past Texas Instruments to become the sector's largest company. Robert Bosch saw 14 percent growth, to ~$842 million in MEMS sales, pushing ahead of both Texas Instruments and Hewlett Packard for the first time to become the second ranking player, according to Yole's figures. Both ST and Bosch have been aggressively expanding their consumer product lines to offer customers a broad range of sensors, and increasingly also combinations of sensors in a single package for easier integration at lower cost. Their growing volumes also help keep their fabs running more efficiently, for the assured manufacturing capability that volume users demand. ST, Bosch and other major inertial sensor suppliers saw strong revenue growth despite the 20-30 percent drop in average selling prices for accelerometers and gyroscopes over the year--because of even bigger ramps in unit volume.

"ST increased unit production by 58 percent, to 1.3 billion MEMS devices in 2012, up to some 4 million units a day—not counting its foundry business," notes Yole Market & Technology Analyst, Laurent Robin. "It's hard for many companies to match that."

Yole calculates the MEMS industry overall saw another ~10 percent growth in 2012 to become an ~$11 billion business—in a year when the semiconductor industry saw a ~2 percent decline. The Top 30 companies account for nearly 75 percent of that total MEMS market.

The traditional gap between the big four MEMS makers and the rest of the pack narrowed this year, as strong demand for more MEMS sensors in both consumer and automotive markets drove strong growth across a range of suppliers. Knowles Electronics saw better than 20 percent growth to climb into fourth place with some $440 million in revenues from MEMS microphones, closing

in on HP. Panasonic and Denso were close behind with more than $350 million in MEMS sales in their largely automotive markets.

Mobile phones and tablets were the real sweet spot for big growth opportunities, though. Chinese electret microphone supplier AAC made the top companies ranking for the first time as its MEMS microphone sales jumped ~90 percent to ~$65 million, as it became the second source for the iPhone. InvenSense saw some 30 percent growth as it ramped up production of its inertial sensors. Triquint saw a 27% increase in revenues from its BAW filters.

Murata moved sharply up the ranking as its acquisition of VTI created ~$179 million in combined MEMS revenue.

Meanwhile, the traditional major MEMS markets for micromirrors and inkjet heads have matured and slowed, with demand for inkjet heads particularly hit by the consumer printer market's rapid turn away from replaceable heads to page-wide and fixed-head technologies. That hit revenuesat both the inkjet companies and their manufacturing partners.

Yole defines MEMS as three dimensional structures made by semiconductor-like processes, with primarily mechanical, not electronic, function. We also include magnetometers, as they are now so closely integrated with MEMS inertial sensors, and all microfluidics, including those on polymer. Yole figured MEMS units and value at the first level of packaged device. For companies that do not release MEMS revenues, Yole estimate the figures based on data for product market size, market share, product teardowns, reverse costing, and discussions with the companies.

Personal computer shipments post worst quarter on record, says IDC

In another sign of the worldwide shift in preferred personal devices, PC shipments posted the steepest decline ever in a single quarter, according to the International Data Corporation Worldwide Quarterly PC Tracker (IDC).

Worldwide PC shipments totaled 76.3 million units in the first quarter of 2013, down -13.9 percent compared to the same quarter in 2012 and worse than the forecast decline of -7.7 percent, according to the IDC. Despite some mild improvements in the economic environment, PC shipments were down significantly across all regions compared to a year ago, marking the worst quarter reported since IDC began tracking the PC market in 1994. The results also marked the fourth consecutive quarter of year-on-year shipment declines.

The reduction in shipments isn't entirely shocking, given the obvious cannibalization from tablets and smartphones. Smartphones shipments are expected to continue their historic rise at a rate of 24 percent CAGR from 2011 to 2016, according to Andy Oberst, Strategic Vice President of Qualcomm, and PC makers are collectively bracing for the change, as other indicators have risen throughout the past year. DRAM content growth is reported slowing, as slim notebooks have limited space for it, and tablets and smartphones have no use for it at all. Instead, its low-power variant, mobile DRAM, is seeing an increase. Additionally, the chip market outlook was downgraded in 2012, with the weak PC market mostly to blame.

"Although the reduction in shipments was not a surprise, the magnitude of the contraction is both surprising and worrisome," said David Daoud, IDC Research Director, Personal Computing. "The industry is going through a critical crossroads, and strategic choices will have to be made as to how to compete with the proliferation of alternative devices and remain relevant to the consumer. Vendors will have to revisit their organizational structures and go to market strategies, as well as their supply chain, distribution, and product portfolios in the face of shrinking demand and looming consolidation."

PC makers had pinned their hopes on the launch of Microsoft's Windows 8 OS, which is a complete overhaul

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GLOBALFOUNDRIES demonstrates 3D TSV capabilities on 20nm technology

GLOBALFOUNDRIES announced the accomplishment of a key milestone in its strategy to enable 3D stacking of chips for next-generation mobile and consumer applications. At its Fab 8 campus in Saratoga County, N.Y., the company has demonstrated its first functional 20nm silicon wafers with integrated Through-Silicon Vias (TSVs). Manufactured using GLOBALFOUNDRIES' leading-edge 20nm-LPM process technology, the TSV capabilities will allow customers to stack multiple chips on top of each other, providing another avenue for delivering the demanding performance, power, and bandwidth requirements of today's electronic devices.

TSVs are vertical vias etched in a silicon wafer that are filled with a conducting material, enabling communication between vertically stacked integrated circuits. The adoption of three-dimensional (3D) chip stacking is increasingly being viewed as an alternative to traditional technology node scaling at the transistor level. However, TSVs present a number of new challenges to semiconductor manufacturers.

GLOBALFOUNDRIES utilizes a "via-middle" approach to TSV integration, inserting the TSVs into the silicon after

the wafers have completed the Front End of the Line (FEOL) flow and prior to starting the Back End of the Line (BEOL) process. This approach avoids the high temperatures of the FEOL manufacturing process, allowing the use of copper as the TSV fill material. To overcome the challenges associated with the migration of TSV technology from 28nm to 20nm, GLOBALFOUNDRIES engineers have developed a proprietary contact protection scheme. This scheme enabled the company to integrate the TSVs with minimal disruption to the 20nm-LPM platform technology, demonstrating SRAM functionality with critical device characteristics in line with those of standard 20nm-LPM silicon.

"Our industry has been talking about the promise of 3D chip stacking for years, but this development is another sign that the promise will soon be a reality," said David McCann, vice president of packaging R&D at GLOBALFOUNDRIES. "Our next step is to leverage Fab 8's advanced TSV capabilities in conjunction with our OSAT partners to assemble and qualify 3D test vehicles for our open supply chain model, providing customers with the flexibility to choose their preferred back-end supply chain."

As the fabless-foundry business model evolves to address the realities of today's dynamic market, foundries are taking on increasing responsibility for managing the supply chain to deliver end-to-end solutions that meet the requirements of the broad range of leading-edge designs. To help address these challenges, GLOBALFOUNDRIES is engaging early with partners to jointly develop solutions that will enable the next wave of innovation in the industry. This open and collaborative approach will give customers maximum choice and flexibility, while delivering cost savings, faster time-to-volume, and a reduction in the technical risk associated with developing new technologies.

Intel board elects Brian Krzanich as CEO, Renée James as President

Intel Corporation announced in May that the board of directors has unanimously elected Brian Krzanich as its next chief executive officer (CEO), succeeding Paul Otellini. Krzanich assumed his new role at the company's annual stockholders' meeting on May 16. The board of directors also elected Renée James, 48, to be president of Intel. She also assumed her new role on May 16, joining Krzanich in Intel's executive office.

Krzanich, Intel's chief operating officer since January 2012, will become the sixth CEO in Intel's history. As previously announced, Otellini will step down as CEO and from the board of directors on May 16.

"After a thorough and deliberate selection process, the board of directors is delighted that Krzanich will lead Intel as we define and invent the next generation of technology that will shape the future of computing," said Andy Bryant, chairman of Intel.

"Brian is a strong leader with a passion for technology and deep understanding of the business," Bryant added. "His track record of execution and strategic leadership, combined with his open-minded approach to problem solving has earned him the respect of employees, customers and partners worldwide. He has the right combination of knowledge, depth and experience to lead the company during this period of rapid technology and industry change."

Krzanich, 52, has progressed through a series of technical and leadership roles since joining Intel in 1982.

As chief operating officer, Krzanich led an organization of more than 50,000 employees spanning Intel's Technology and Manufacturing Group, Intel Custom Foundry, NAND Solutions group, Human Resources, Information Technology and Intel's China strategy.

James, 48, has broad knowledge of the computing industry, spanning hardware, security, software and services, which she developed through leadership positions at Intel and as chairman of Intel's software subsidiaries -- Havok, McAfee and Wind River. She also currently serves on the board of directors of Vodafone Group Plc and VMware Inc. and was chief of staff for former Intel CEO Andy Grove. ◆

Computer Shipments

Continued from page 8

of the operating system with touch-screen capabilities. Unfortunately, these new shipment trends are indicating that the upgraded operating system has not had the desired effect on consumers.

Bob O'Donnell, IDC Program Vice President, believes it is clear that Windows 8 not only failed to provide a positive boost, but also appears to have slowed the market.

"While some consumers appreciate the new form factors and touch capabilities of Windows 8, the radical changes to the UI, removal of the familiar Start button, and the costs associated with touch have made PCs a less attractive alternative to dedicated tablets and other competitive devices," said O'Donnell. "Microsoft will have to make some very tough decisions moving forward if it wants to help reinvigorate the PC market."

Microsoft, at least in public, does not appear to be on the verge of making tough decisions at the moment, however. A Microsoft spokesperson told the Wall Street Journal that, along with their partners, they planned "to continue to bring even more innovation to market across tablets and PCs." ◆

IBM announces $1B investment in flash memory R&D

IBM announced plans to invest $1 billion in flash memory research and development and launch a series of systems that will use solid state drives.

At an event in New York, IBM's Steve Mills, head of IBM's software and systems division, said Flash is at a key tipping point and IT will see all-solid state data centers sooner than later.

Corporate servers have struggled to keep up with the substantial growth in data use from smartphones and tablets. IBM believes there is a solution in flash memory, which is faster, more reliable, and uses less power than a traditional hard disk drive. The $1 billion investment will be put to use in research and development to design, create and integrate new flash-based products in its portfolio of servers, storage systems and middleware.

"The economics and performance of flash are at a point where the technology can have a revolutionary impact on enterprises, especially for transaction-intensive applications," said Ambuj Goyal, IBM's general manager of systems storage. "The confluence of Big Data, social, mobile and cloud technologies is creating an environment in the enterprise that demands faster, more efficient, access to business insights, and flash can provide that access quickly."

As part of its commitment to flash development, IBM said it plans to open 12 Centers of Competency around the globe, which will allow customers to test IBM flash products in real-word scenarios.

"Clients will see first-hand how IBM flash solutions can provide real-time decision support for operational information, and help improve the performance of mission-critical workloads, such as credit card processing, stock exchange transactions, manufacturing and order processing systems," IBM said in a news release.

Second phase of Nanoelectronics Research Initiative to focus on post-CMOS electronics

Semiconductor Research Corporation (SRC) and the National Institute of Standards and Technology (NIST) in May announced the second phase of the Nanoelectronics Research Initiative (NRI). SRC and NIST will provide a combined $5 million in annual funding for three multi-university research centers tasked with demonstrating non-conventional, low-energy technologies that outperform current technologies on critical applications in 10 years and beyond.

The second phase of NRI also features joint projects with the National Science Foundation

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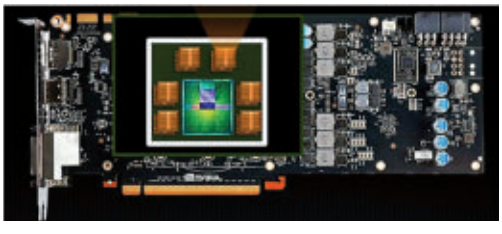
NVIDIA's GPUs; Patent analysis

Dr. Phil Garrou, contributing editor

NVIDIA has publically updated their roadmap with the announcement of the GPU family that will follow 2014's Maxwell family. That new family is Volta which will use stacked DRAM, which will be connected to the GPU with TSV.

NVIDIA is targeting a 1TB/sec bandwidth rate for Volta, which, to put things in perspective, is over 3x what GeForce GTX Titan currently achieves with its 384bit, 6Gbps/pin memory bus (288GB/sec). This would imply that Volta is shooting for something along the lines of a 1024bit bus operating at 8Gbps/pin, or possibly an even larger 2048bit bus operating at 4Gbps/pin. Volta is still years off, but this at least gives us an idea of what NVIDIA needs to achieve to hit their 1TB/sec target. At the GPU Technology Conference in San Jose, CEO Jen-Hsun Huang spoke about the Volta. "Volta is going to solve one of the biggest challenges facing GPUs today, which is access to memory bandwidth," Huang told the attendees.



Nvidia's Volta with stacked DRAM.

The Volta GPU will include stacked DRAM. Figure 1 is a shot of the Volta with stacked DRAM (drawn to scale).

Huang didn't provide a timeline for Volta's release, but 2016 seems reasonable since Nvidia debuts new GPU architectures every two years. Huang said that Nvidia will be putting the stacked DRAM and the GPUs onto the same silicon substrate and inside of the same packaging before it welds that package to a peripheral card.

Packaging

New patent report

In other news, Yole Développement announced its 2.5D, 3DIC and TSV Interconnect Patent Investigation report. Yole Développement's investigation aims at providing statistical analysis of existing IP to give a landscape overview together with an in-depth investigation on five player portfolios selected by the analyst.

For this analysis of 3D packaging technology patents, more than 1800 patent families were screened. Fifty-two percent of the families have been classified as relevant and further studied.

"The in-depth analysis quickly revealed that the overall patent landscape was pretty young with 82 percent of patents filed since 2006," explained Lionel Cadix, technology and market analyst of the Advanced Packaging division at Yole Développement. "Actually about 260 players are involved in 3DIC technology while the top 10 assignees represents 48 percent of patents filed in the 3DIC domain."

In this report, Yole Développement selected five companies from these 10 most active players to focus on and lead an accurate analysis of their patent portfolios.

Yole Développement also found main types of business models among the top 10 assignees involved in this mutating middle end area:

- Foundries and IDM: IBM, Samsung, Intel
- OSATs: STATS ChipPAC, Amkor
- Memory IDM/Foundries: Micron, SK Hynix, Elpida
- Research centers: ITRI

It is also interesting to note that the USA is the early player increasingly involved in 3DIC since 1969. China and Korea are new players since 2005.

Inside biomedical devices

Denise Rael, Contributing Editor

The interface of human physiology with electronic processing provides a market for medical devices whose applications are boundless. The convergence of scientific and medical research, new materials, wireless communication and evolving healthcare policies create an expanding market opportunity for medical devices that detect and analyze biological functions.

The ability to unobtrusively monitor vital signs and stress biomarkers can save lives. For military personnel or first responders to an emergency situation, new technology will sense when rescue workers are in danger. For the chronically ill, elderly, newborn or other high risk patients, these monitoring devices can save lives and dramatically reduce health care costs.

Lux Research estimates the worldwide medical device market is over $300 billion. The advent of smaller, more conformable components enabled by organic electronics is fueling additional market opportunities and will lead to more cost-effective medical care.

Biosensors and microfluidic devices are core components for bio-monitoring devices. These technologies will help detect early signs of infection, the onset of a stroke or heart attack and eventually provide early diagnosis of chronic diseases that can be detected with biomarkers.

A biosensor generally consists of three parts. First is the sensitive biological element such as microorganisms, enzymes or nucleic acids. Next is the transducer element which transforms a biological reaction into a measurable signal. The final stage is the electronics and signal processors that communicate the results. Several sophisticated, micro-sized and flexible biosensors are under development. For example, Massachusetts-based startup MC10 is developing a new class of catheters embedded with ultra-low profile, nanometer-thin sensors. These sensors provide physicians with real-time feedback during procedures.

MEMS

Microfluidic devices work by moving liquids from one location to another. They can be used to collect bio-fluids for analysis or to dispense medication automatically. Microfluidics are especially useful in biomedical applications because they perform tests such as detecting toxins or DNA analysis using just a small amount of bodily fluids.

While microfluidic devices have been around for decades, the technology has historically involved large equipment in a lab setting for analysis. Currently, a number of organizations are working on bringing a Lab-on-a-Chip to market. For instance, researchers at Harvard University and the University of Washington have actually formed paper microfluidic devices. The Microfluidic Paper-based Analytical Devices (μPADs) are made from paper patterned into hydrophilic channels or paper cut into channels with controlled geometry using laser cutters. They are inexpensive, simple-to-use, and equipment-free - easily adaptable to remote locations.

Innovative sensor and microfluidics technologies enable the next generation of medical devices with the potential to improve both the economics and outcomes of healthcare. However, organizations interested in bringing a medical device to market need to be aware of regulatory considerations.

"You want to understand the pathway to market as early as possible," says Nathan A. Beaver, Partner at Foley & Lardner LLP. Medical devices are subject to regulation by numerous regulatory bodies, including the Food and Drug Administration (FDA). Companies must comply with laws and regulations governing the testing, manufacturing, labeling, marketing and distribution of medical devices. Devices are subject to varying levels of regulatory control, the most comprehensive of which requires that a clinical evaluation be conducted before a device receives approval for commercial distribution.

The challenges of sub-20nm shallow trench isolation etching

HUI ZHOU, XIAOSONG JI, SUNIL SRINIVASAN, JIM HE, XUEFENG HUA, ANKUR AGARWAL, SHAHID RAUF, VALENTIN N. TODOROW, JINHAN CHOI, AND ANISUL KHAN, *Applied Materials, Inc., Santa Clara, CA*

Major challenges for sub-20nm STI etching include intra-cell depth loading, across-wafer uniformity, etch profile control near the wafer edge, and propensity for pattern collapse.

Shallow trench isolation (STI) is used for device isolation in state-of-the-art semiconductor process technologies [1]. For optimal transistor performance and desired yield, the line critical dimension (CD) and the trench depth must be tightly controlled [2]. As feature sizes scale below 20nm, the aspect ratio of the isolation trench can be as high as 20:1. Given the small space CD, variation in trench width (e.g., from double patterning) is no longer negligible, and the subsequent aspect ratio dependent etching effect can lead to non-uniform trench depths [3]. Consequently, minimizing intra-cell depth loading is crucial.

As feature sizes scale, profile uniformity across the wafer and, in particular, near the wafer edge assume greater importance. The outer edge (10mm) of a 300mm wafer accounts for over 10% of total devices that yield. But the edge area is characterized by discontinuities of materials (wafer to focus ring/process kit transition), and electrical and thermal properties (due to the wafer overhang on the electrostatic chuck). Consequently, the plasma sheath characteristics are not necessarily similar to those over the center of the wafer, leading to significant impact on STI features near the wafer edge. Both of these aspects must be managed simultaneously for sub-20nm features.

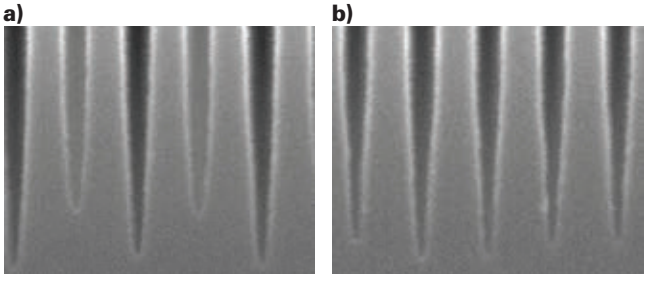


FIGURE 1. STI etching profiles using 13MHz bias power with (a) continuous wave plasma and (b) pulsed plasma (processes are not fully optimized).

Aside from the above challenges for sub-20nm features, some new issues also arise. One is the potential for line collapse, which can substantially reduce production yield. Pattern collapse has been a major problem for lithography resist, and numerous research papers addressing this issue have been published [4-7]. Owing to their low Young's modulus of 1-5 GPa, lithography resist patterns succumb to capillary pressure during the drying process [8]. Silicon, unlike a typical resist material, is much more rigid with a Young's modulus of ~150 GPa [9] and is usually immune to pattern collapse for STI etching when line widths are on the order of 100s nm. However, line collapse has been increasingly observed in sub-20nm STI features, especially after wet cleaning.

HUI ZHOU, XIAOSONG JI, SUNIL SRINIVASAN, JIM HE, XUEFENG HUA, ANKUR AGARWAL, SHAHID RAUF, VALENTIN N. TODOROW, JINHAN CHOI, *and* **ANISUL KHAN,** *Applied Materials, Inc., Santa Clara, CA*

In this paper, we discuss the above four challenges (intra-cell depth loading, wafer edge profile, across-wafer etch uniformity, and line collapse) in etching sub-20nm STI features, using experimental results from the Applied Materials inductively coupled plasma silicon etcher. Some general guidelines to overcome these challenges are also reviewed.

Intra-cell depth loading

In most cases, high aspect ratio features etch more slowly than low aspect ratio features due to the transport limit of etchant in the trenches [3]. In other words, the etching rate of a wider trench is higher than that with a smaller CD. As the CD scales below 20nm, any space CD variation is no longer negligible compared to the CD and leads to depth loading with plasma etching. Ions are less affected by trench shadowing due to their higher directionality resulting from acceleration within the sheath. Therefore, shadowing of neutral species — the radicals, molecules, and the etching products — dominates aspect ratio dependent etching. Through our process developments, we identified three general rules that are most effective for minimizing intra-cell depth loading during sub-20nm STI etching:

1. Prevent further space CD variation by maintaining a clear trench with thin sidewall protection film.
2. Alleviate the transport limit of neutral species between wider and less open trenches by using pulsed plasmas.
3. Make the process less radical driven and more ion driven by using high-energy etchant ions, such as Cl^+ or Br^+.

Sidewall protection is critical in high aspect ratio etching [10]. The passivation layer protects the trench sidewall from etchant species and helps maintain a straight sidewall profile. The efficiency of the protection layer depends on the film composition and its thickness. However, a thicker film also reduces the space CD, which can have a significant impact in sub-20nm STI etching. A thin sidewall passivation layer is therefore desired for minimal reduction of the space CD. Note that during silicon etching, the trench can get blocked due to deposition of the etching radicals or redeposition of etching byproducts. The trench therefore also needs periodic cleaning. A practical approach is to have alternating trench cleaning, passivation, and silicon etch steps. The exact order may vary, but throughout the process, a clear trench should be maintained with a thinnest possible sidewall protection film.

Continuous wave plasma etching technology has served microelectronic fabrication very well in most applications, but with the transport limit of neutral species for STI etching, we must consider an alternative plasma etching regime, namely, a pulsed plasma. Pulsed plasma is transient, which is different from continuous wave operation [11], alleviates the transport limit. During the off cycle, the radicals/ions/byproducts have extra time to move out of the trench or act independently on the sidewall, for better sidewall polymer deposition management. **FIGURE 1** shows an example of improved intra-cell depth loading using pulsed plasma. STI features etched using continuous wave plasma etching **(Fig. 1a)** have large intra-cell depth loading due to space CD variation while those etched using a pulsed plasma **(Fig. 1b)**

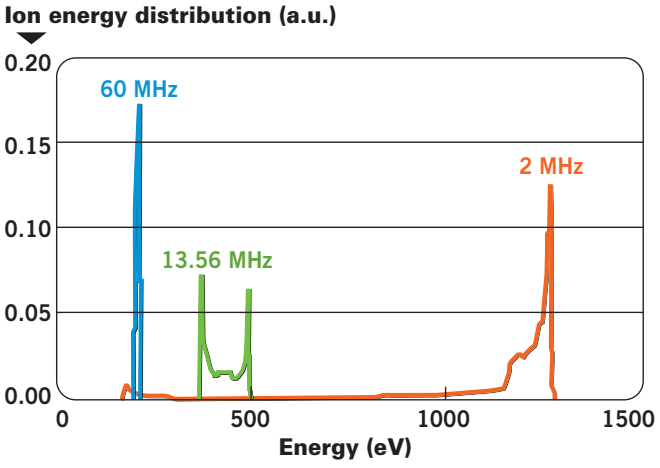


FIGURE 2. Modeling results of ion energy distribution versus bias frequency.

have significantly less intra-cell depth loading in spite of the same space CD variation.

Unlike neutral species, ions are less susceptible to shadowing effects due to their acceleration by the sheath electric field, which leads to more directionality. Consequently, intra-cell depth loading can be reduced if the silicon trench formation were dominated by ions (Cl^+ or Br^+) instead of radicals. Ion dependent etching can be realized by increasing ion energy or ion density. To increase ion energy, one can elevate the bias power or lower the bias frequency. As shown in **FIGURE 2**, model-predicted ion energy distributions for varying bias frequencies at constant bias power indicate that ion energies can be increased with lower bias frequency. In fact, pulsed plasma and lower bias frequency can be combined to reduce depth loading. **FIGURE 3** shows STI etching profiles with 2 MHz bias power operated in continuous wave or pulsed plasma mode. While the high ion energy approach with lower bias frequency of 2 MHz reduced the intra-cell depth loading (compared to the trench profiles in **Fig. 1**), the pulsed plasma with 2 MHz bias power showed the least depth loading. Besides decreasing the intra-cell loading, the high ion energy etching approach has another benefit of maintaining a flat trench bottom. This facilitates a uniform etching front, which is desirable for achieving a high production yield.

By following the three guidelines, we minimized intra-cell depth loading of STI trenches with similar CD, for such applications as NAND STI. The three rules also have the potential to significantly reduce depth loading between dense areas and wide open regions. For example, a typical DRAM STI pattern, as shown schematically in **FIGURE 4**, is designed to have trenches with narrow openings between the cells and wide open regions at the cell ends as illustrated in [12, 13]. We have also applied the three general rules for DRAM STI etching and achieved promising results.

Edge profile and uniformity

Two other issues are also challenging for sub 20nm STI etching. These are edge profile control and uniformity tuning across the wafer. These two issues originate from the nature of plasma distribution inside the reaction chamber, which is often beyond the capability of process tuning. The fundamental solution would be implementing novel hardware to achieve more uniformly distributed plasma.

Three main kinds of discontinuities occur at the wafer edge: 1) material discontinuity from the silicon wafer to the support ring; 2) geometrical disconti-

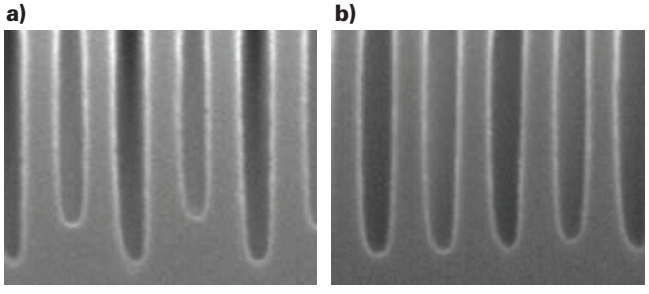


FIGURE 3. STI etching profiles using 2MHz bias power with (a) continuous wave plasma and (b) pulsed plasma (processes were not fully optimized).

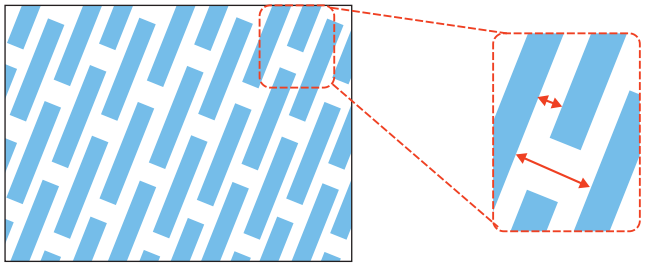


FIGURE 4. Plan view of a typical DRAM STI pattern, with narrow open area between cells and wide open region at the cell ends, as illustrated in [12, 13].

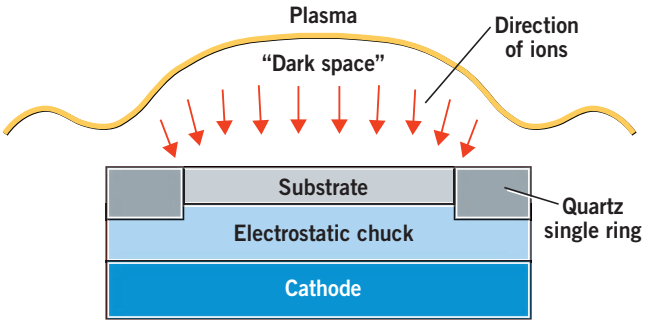


FIGURE 5. Schematic of plasma sheath curvature due to discontinuities at the wafer edge.

nuity from the wafer level to the ring level; and 3) electrical discontinuity due to RF coupling termination at the wafer edge. Because of these three discontinuities, the plasma sheath profile at the wafer edge becomes curved, resulting in off-normal incidence of ions **(FIGURE 5)**. Consequently, for certain processes, the trench profile at the wafer edge may tilt in the direction of ion incidence, as shown in **FIGURE 6a.** One innovation for improving the edge profile is our advanced edge control (AEC) kit. The AEC kit alleviates electrical discontinuity by optimizing the cathode to extend uniform RF coupling beyond the edge of the wafer. Sheath bending is thereby corrected and the ions are normally incident (i.e., are no longer tilted), resulting in straighter trench profiles **(FIGURE 6b)**.

Mainstream commercial inductively coupled plasma (ICP) sources utilize planar or helical coil geometries [14]. For either type, radial distribution of the electromagnetic fields are not homogenous, leading to non-uniformities in plasma generation that in turn introduce non-uniformity in the etching rate across the wafer. As plasma uniformity is mainly related to the plasma source and gas delivery, tweaking the source coil configurations and gas delivery systems can help improve uniformity. This is achieved in our silicon etcher's source by using two helical coils where both the current ratio between the coils can be independently controlled and the phase between the currents can be tuned **(FIGURE 7a)** [15,16]. When the inner and outer coil currents are in phase, the characteristic donut shape in the etch rate distribution across the wafer is observed **(FIGURE 7b)**. Note that varying the current ratio improves the uniformity slightly, but not significantly enough to be production worthy. When the inner and outer currents are out of phase by 180 degrees, etch rate distribution can be tuned from being edge-high to center-high **(FIGURE 7c)**. By optimizing the inner-to-outer coil current ratio, a very uniform etch rate can be achieved.

Pattern collapse

Pattern collapse becomes a significant problem as STI line widths shrink and aspect ratios increase. STI lines may bend when an external force is applied, and the bending distance depends on the magnitude of the force and the stiffness of the line. The external forces might arise from electrical charges, mechanical movement, or capillary forces during wet cleaning. The multiplicity in the origins of the force makes the pattern collapse issue complicated and each case different. In the case where electrostatic forces dominate, plasma etching processes must be tuned to prevent charging. For mechanical shocks, wafer transfer procedures must be adjusted. If the pattern collapse derives from wet cleaning, an alternative cleaning solution or method (e.g. dry cleaning) must be adopted. In summary, external forces should be eliminated or minimized.

From the point of view of line stiffness, the line profile is also important to prevent line sticking. Senturia [17] showed that the stiffness of a line is a function of the material properties and the pattern geometries:

$$k \propto E \cdot AR^{-3} \quad (1)$$

Where, k is the line stiffness, E is the Young's modulus, and AR is the aspect ratio of the line. The high Young's modulus of silicon makes it less subject

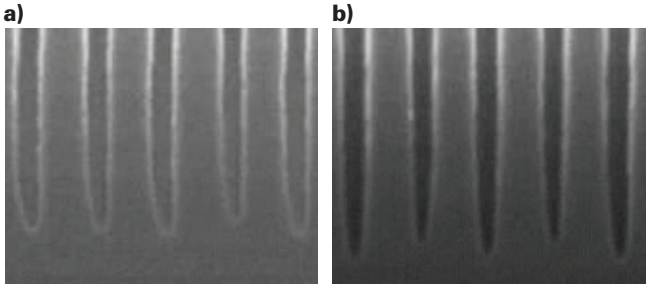


FIGURE 6. STI profiles at 3mm from the wafer edge (147mm radius) (a) without AEC kit and (b) with AEC kit (processes were not fully optimized).

to pattern collapse than the resist in photo lithography; before the sub-20nm era, line collapse was not a significant issue for STI etching. However, as shown in Eq. 1, the stiffness of a line is inversely proportional to the cube of the line aspect ratio. Thus, as the aspect ratio increases, the propensity for silicon lines to stick to each other increases even under constant external force magnitudes. Moreover, any profile defect, such as local bowing, could significantly decrease the line stiffness. And if the device design and the integration process allow, a tapered line profile might be preferred to prevent line collapse as the feature sizes shrink further.

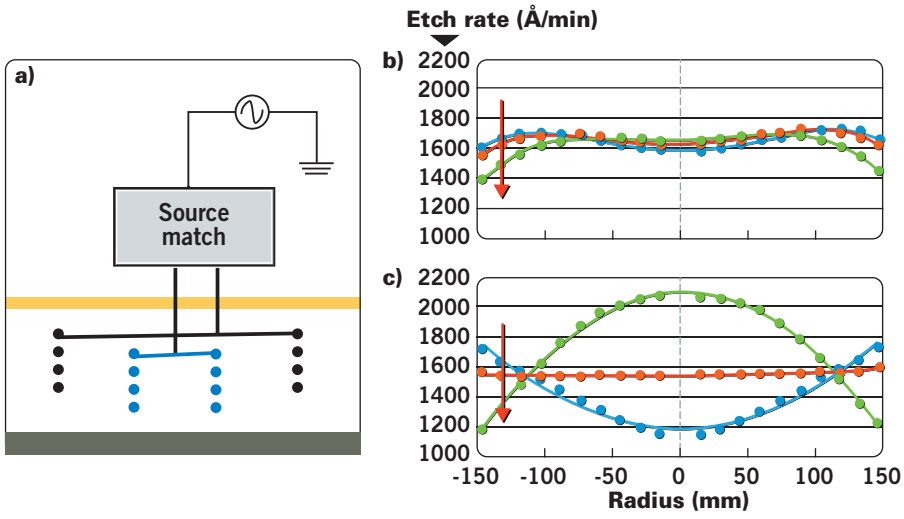


FIGURE 7. Uniformity improvement with reverse source (a) schematic of Mesa source with inner and outer coils, (b) the etching rate distribution with the inner/outer coil currents in phase, and (c) the etching rate distribution with the inner/outer coil currents out of phase by 180 degrees. Arrows in (b) and (c) indicate increased inner/outer source current ratio.

Conclusion

STI etching has become very challenging in the sub-20nm era. Four major challenges were reviewed in this paper. Intra-cell depth loading could be managed with advanced process tuning, and three general process development rules for avoiding this issue were provided. A combined solution of hardware innovation and process tuning achieved across-wafer etching rate uniformity and uniformity control over profiles near the wafer edge. Sub-20nm node STI features are susceptible to pattern collapse; aside from eliminating or minimizing external forces, a reasonable STI profile should be obtained if bowing is avoided during the plasma etching process. ◆

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Statistical variation monitoring for production control

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The sources of parametric variation are reviewed, with an eye on why these issues become worse as the technology is scaled and how this variation can be monitored and controlled.

As semiconductor technologies become smaller, the processes become more complex. This is a long established trend in the semiconductor industry. Unfortunately, it is not a linear relationship. The relationship is exponential. As we approach the limits of scaling, this exponential effect becomes nearly vertical. In his presentation "Beyond 28nm: New Frontiers and Innovations in Design for Manufacturability at the limits of the scaling roadmap," Luigi Capodieci [1] describes the significant increases in technology required to move from 28 to 20nm. He describes multiple new layers, double patterning and extensive error corrections and review procedures required to achieve the new scaling targets.

Monitoring and controlling the variation in a semiconductor process during production has long been the task of parametric testing. These are electrical tests performed on semiconductor wafers at the end of the production cycle. The parametric variation increases with the square of the number of sources of the variation. Thus, the parametric testing function is stretched even more than the process by the exponential increase in complexity.

In chapter 1 of the book "Low Power Variation-Tolerant Design for Nanometer Silicon" [2] A. Bansai and R. Rao point out sources of manufacturing variation, intrinsic variation and design variation. Design variation is not an issue for parametric test. Process variation has long been the focus of parametric test. However, this focus has long been on lot-to-lot variation, wafer to wafer variation within a lot and site-to-site variation across a wafer (typically center-to-edge variation). Unfortunately, at the nanoscale level, transistor-to-transistor or metal line-to-metal line variation is also a concern.

This is a significant departure from historic techniques for parametric test where the structures tested were typically one transistor or one via. To address the element to element variation, statistical structures tabulating the variation of hundreds or thousands of circuit elements is necessary.

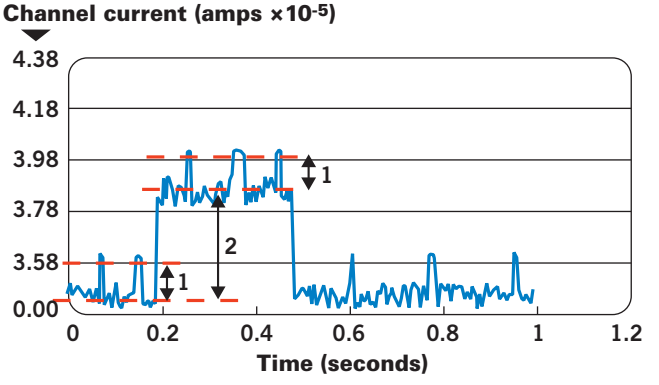

FIGURE 1. Charge trapped in the gate oxide modulates the channel current. Shown are two traps: 1 and 2. The peak magnitude of the noise is the sum of all traps.

Since about the 2 micron generation, parametric test has been limited to scribe lanes. At that technology

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node, single elements were all that would fit in the scribe lanes. Now, it is possible to place thousands of transistors in a scribe lane structure beside a die that might hold billions of transistors.

Statistical test structures are required to monitor the changes in variation that are critical to designers. Consider the impact of Random Telegraph Noise. This issue was first identified as a future issue back in the 1980's. Van der Zeil [3] pointed out that Random Telegraph Noise (RTN) was proportional to the inverse of the size of the gate area on the transistor. RTN is caused by traps in the gate dielectric. As shown in **FIGURE 1**, trapped charge in the dielectric modulates both the number of carriers and the mobility of the carriers under the gate [4]. Large transistors with perhaps hundreds of trap sites per transistor show little impact when one trap fills or emits. At the 45nm node, Realov and Shepard [5] showed that almost half of the transistors contained no traps, but the rest contained as many as five traps per transistor. The probability of holding one or more traps decreased with the gate area, but with a billion transistors on a die, 0.1% would leave 1 million transistors with multiple traps per die.

With 45nm transistors, a single trap caused on the order of a 10% change in the channel current at the worst case bias [5].

Realov and Shepard also showed that van der Zeil was an optimist concerning the scaling implications. They showed that a reduction in channel length could not be compensated by an increase in channel width (**FIGURE 2**). With identical effective gate dielectric areas (effective length times effective width), the shorter length transistor would always show a higher amplitude for the noise.

Further adding to the problem is the reduction in signal levels required to scale the gate dielectric voltage when the transistor is scaled. The trap is a fixed charge. Its impact is set by that charge. As we lower the signal level, we increase the percent impact of that charge.

Waltl, Wagner, Reisinger, Rott and Grasser [6] characterized the traps using a technique called Time Dependent Defect Spectroscopy (TDDS). This technique uses a short (1ms) gate voltage pulse to fill the traps, then biases the channel so as to measure the emission of the traps. The traps are characterized by the voltage step when the trap emits and the time since the gate pulse was turned off when the trap emits. This was shown to be a repeatable characterization for each transistor, providing a characterization of the traps in that transistor. This technique allows not only the measurement of the number of transistors that show traps, but a further characterization of the traps.

TDDS can identify 1/f noise sources as well as RTN. When a large number of transistors are measured, a spectrum of the traps available at that site on the wafer is provided. This spectrum can be an important process control tool.

For instance, Pobegen, Nelhieel and Grasser showed the impact of local hydrogen concentration on interface hole traps. This suggests that TDDS could be used to monitor the local hydrogen concentration across

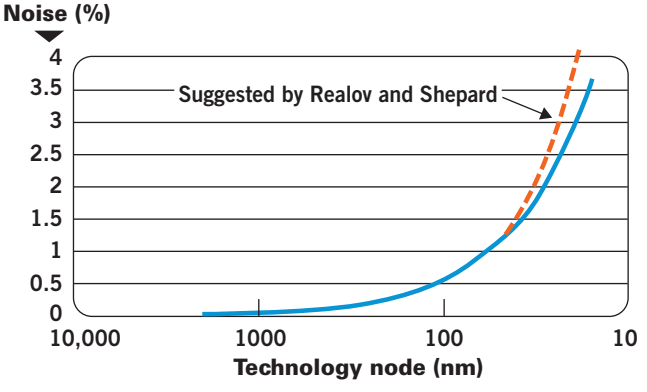

FIGURE 2. RTN increases with the inverse of the gate area. Realov and Sheppard showed that below 45nm, this increase can be greater, more a function of length than area.

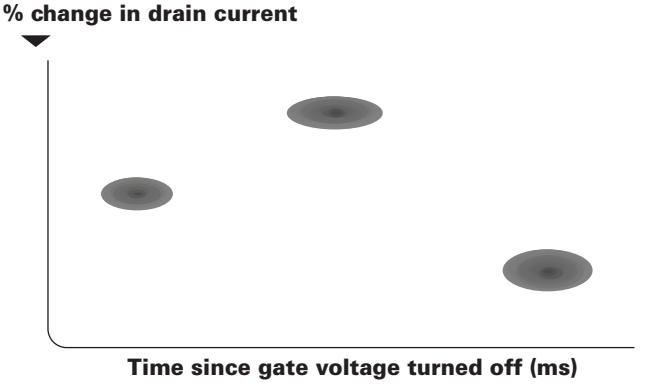

FIGURE 3. TDDS – Charge emitted from traps after a gate voltage pulse is removed. Multiple charge and discharge repetitions generate the probability clouds around different magnitude and time points [6].

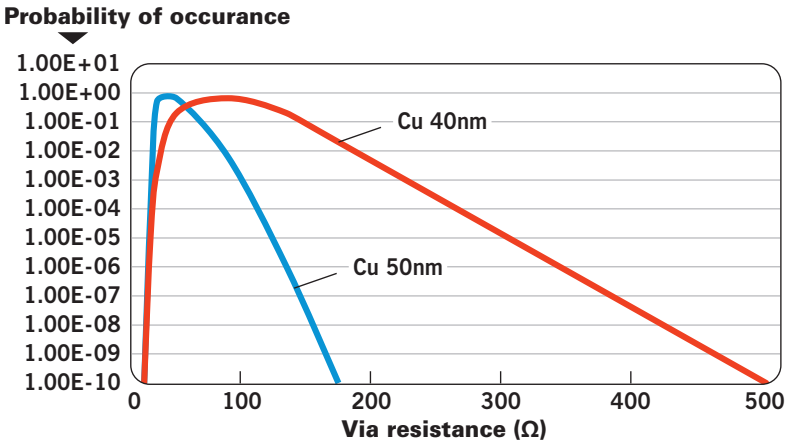

FIGURE 4. Via Resistance Distribution for different via sizes (J. W. Sleight et. Al. [7])

a wafer (**FIGURE 3**). Other issues such as radiation damage, charge damage and interface stress may be correlated with TDDS spectra.

Contact resistance is another statistically distributed function. As shown in **FIGURE 4**, Sleight et. Al. [7] observed that the contact resistance followed an analytical cone model due to variation in the bottom diameter, height and angle of a contact stud. If we now add the process changes projected by Capodieci [1] for 20nm technology, we may see the variation caused by stacking up to 4 via layers below metal 1 (**FIGURE 5**). The variation of each via layer will be a much more tightly distributed parameter than what results when 4 of these layers are stacked.

Line Edge Roughness (LER) is another source of variation [8]. LER on a gate electrode can modify the local channel length resulting in a variation in the transistor's performance. Since this variation provides an effective variation in the transistors

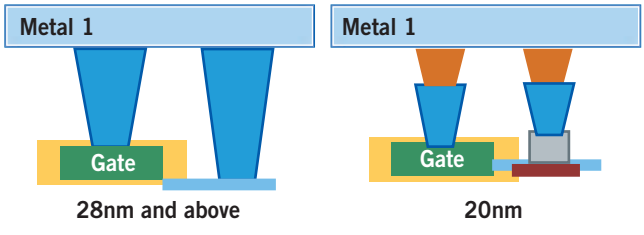

FIGURE 5. 20nm technology will require more process steps than previous technology. This will increase the variability in the process parametrics. (Capodieci[1])

channel length and a shorter channel length provides a higher Random Telegraph Noise, LER will introduce still more variation in the RTN.

LER also impacts metal lines. In this case, the resistance of the line will always show the average line width. The metal line resistance is most important for long lines. Long lines tend to average out any line width variation making line resistance insensitive to LER. Unfortunately, linewidth variation correlates with line spacing variation. Line spacing will have a lifetime limited by the shortest space.

Measuring the leakage between two long lines is not an effective way to measure the variation in the line width. The best way to directly measure the variation is to measure the variation in the voltage required to induce a very low amount of leakage between a large number of shorter metal lines. This will provide the desired statistical variation in the line to line space.

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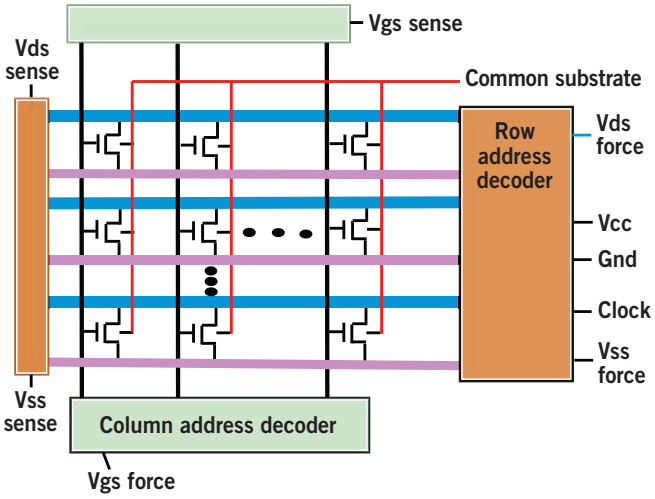

FIGURE 6. Array of Transistors for Characterization. For instance, the row and column addresses could be generated by two six bit counters allowing the independent characterization of 4096 transistors using only 8 probe pads (Vdsforce, Vdssense, Vgsforce, Vgssense, Vsub, Clock, Vcc, Gnd, Vsforce and Vssense). Adding an on chip A/D converter would decrease measurement time while reducing noise and adding only one serial data port.

Detection and elimination of a yield-critical non-visual residue defect

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A post-wet clean residue that was causing a yield issue was found and eliminated.

Integrated circuit manufacturers rely heavily on optical inspection techniques to monitor and control manufacturing processes. Optical inspection has proven effective in detecting and classifying a wide range of physical defects on semiconductor wafers, such as pits, particles and scratches. In recent years, circuit features have continued to shrink while semiconductor manufacturers have been introducing many new materials, processes and structures for advanced technologies, such as high-k metal gates, low-k dielectrics and stressed silicon channels. The accelerating pace of change has introduced new types of yield-limiting defects, some of which are not detectable using optical inspection techniques. These defects are sometimes referred to as Non Visual Defects (NVDs), and include sub-monolayer residues, surface contamination and process-induced charging of dielectric films [1-4].

Samsung Electronics and Qcept Technologies previously presented a case study where a charge-based NVD was identified as a precursor to a physical "pitting" defect in the gate oxide process [5]. In this article we describe the detection and elimination of a post-wet clean residue on a logic device. The residue defect correlated to a known yield issue from end-of-line (EOL) electrical test. The failed die were clustered in a semicircular arc across the top of the wafer. The defect was believed to occur at the front end of line (FEOL) gate module, but no matching defect pattern was detected by the existing optical inspection tools. The residue defect was ultimately determined

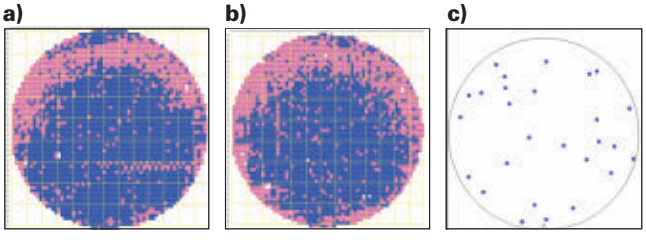

FIGURE 1. Images (a) and (b) are sample EOL failure maps that show a common pattern of failed (pink) die across the top of the wafer. Image (c) is a brightfield optical inspection defect map at After Clean Inspect (ACI). Optical inspection provided no indication of the defect causing the yield loss.

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to be an NVD as detected by a unique, non-optical inspection technique.

The problem was initially noticed when a leading-edge-node logic device was experiencing increased yield loss at EOL electrical test. A large number of die on random wafers from random lots were failing for low grounded voltage of the collector (V_{cc}). The failures occurred in an arc pattern across the top of the wafer (**FIGURE 1**), and the failure mode suggested that the defect was happening somewhere in the gate and spacer module. A review of the existing brightfield optical wafer inspection data from the gate and spacer module did not identify a physical defect pattern that matched the yield-loss signature. In an effort to detect and diagnose the problem, inspection was initiated at several process steps within the gate and spacer module using a unique, non-optical inspection technology that is sensitive to a wide range of NVDs, including sub-monolayer contamination and process induced charge.

The inspection system used was the ChemetriQ system from Qcept Technologies. ChemetriQ is a scanning probe system that produces a full wafer image showing changes in the work function of the wafer. The resulting differential data can be numerically integrated and thresholded to detect regions of the wafer with relatively high or low work function. Changes in work function can result from a variety of surface conditions, including changes in surface chemistry, such as residues or contamination. This technique is sensitive to low-level, sub-monolayer contamination that does not scatter light and cannot be detected using traditional optical means.

ChemetriQ inspection was initiated at several process steps in the gate and spacer module, including post gate photo, post gate etch / clean, post spacer deposition, and post spacer etch / ash / clean. These types of partition studies are facilitated by the fact that the ChemetriQ system can scan wafers at many different process steps without modifying the scan recipe, so no time is spent optimizing recipes for each process step. NVD inspection data detected strong spots of increased work function (+WF) at the top portion of the wafer after the spacer etch, ash, and clean steps. The NVDs detected at the spacer process

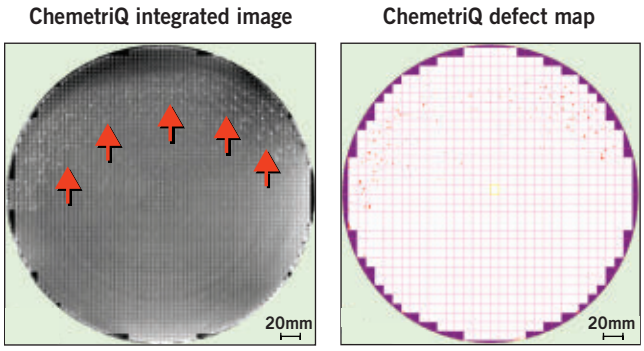

FIGURE 2. The image on the left is a ChemetriQ image showing a residue pattern across the top of the wafer after spacer deposition, etch, ash and clean (red arrows). Areas of increased work function (+WF) appear bright in the image. The image on the right is a defect map created by thresholding the integrated image. The pattern of defects across the top of the wafer closely matched the pattern of EOL yield loss.

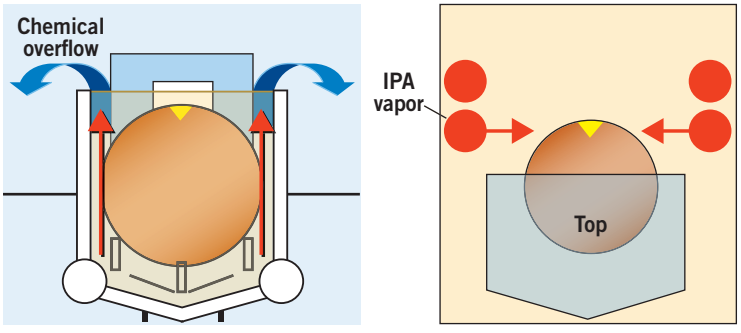

FIGURE 3. Diagram of the batch tool used to clean wafers after spacer etch. The wafers were extracted from the bath with the notch up so the rinse water flowed from the bottom (notch side) of the wafer to the top.

were thresholded into Defect Maps as shown in **FIGURE 2**. The number and spatial location of the NVDs correlated with failed die at EOL and closely matched the top of wafer yield-loss pattern.

The partition study provided strong evidence that the defect occurred at spacer etch and clean. The batch wet clean process was targeted as the most likely source of the NVD defect. During the clean process, the wafers were extracted from the batch tool notch-edge up, so the rinse water flowed from the notch (bottom) to top of the wafer as shown in **FIGURE 3**. It was suspected that this process might result in less effective rinsing on the top of the wafer.

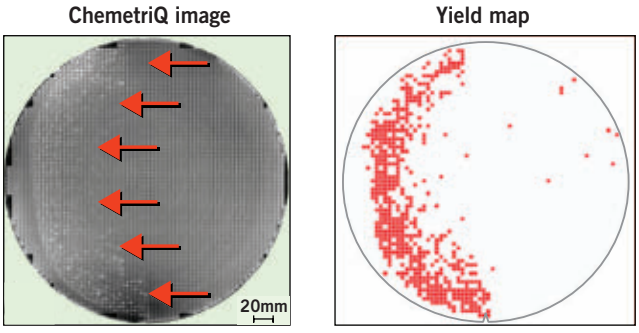

FIGURE 4. Sample results from an experiment with wafers rotated 90 degrees in the batch clean tool. Rotating the wafers also rotated the NVD pattern detected by the ChemetriQ inspection system and the pattern of yield loss at EOL test.

An experiment was designed to determine if the defect could be caused by the flow of liquid as the wafers were extracted from the batch wet clean tool. Wafers were loaded in the tool with the notch at 90 degrees. The ChemetriQ images after clean showed that the +WF NVD pattern was rotated by 90 degrees. EOL electrical tests showed that the pattern of failed die was also rotated by 90 degrees (**FIGURE 4**). These results provided convincing evidence that the batch clean tool rinse was leaving a residue on the wafer surface that was causing the yield loss.

Different options were evaluated to eliminate the NVD from the batch wet clean process, including modifying the existing process and switching to a single-wafer clean process. One promising option was to use a new linear, single-wafer clean process for a more robust cleaning process and to eliminate the NVDs. ChemetriQ inspection results on wafers processed with the new linear, single-wafer clean process showed a cleaner and more uniform surface. EOL data also exhibited a significant increase in yield and elimination of the characteristic yield-loss pattern as shown in **FIGURE 5**.

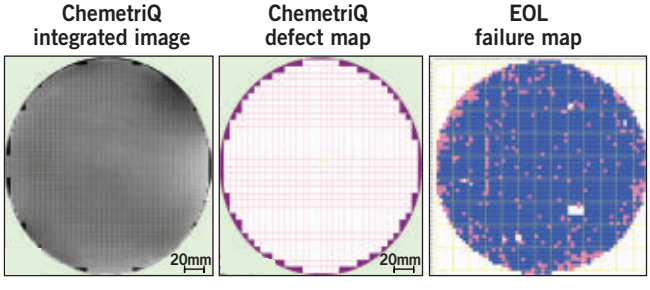

FIGURE 5. Sample inspection and test results for a wafer cleaned with a linear single-wafer clean process. The pattern of positive work function defects was eliminated from the ChemetriQ inspection image and defect map, and EOL yield was increased significantly.

As a result of this work, a linear, single-wafer clean approach was implemented after spacer etch, and the ChemetriQ tool was used to monitor production wafers to insure that the problem did not recur. In addition, Samsung engineers performed parametric tests and device modeling, which confirmed that a negative ionic contaminant was consistent with both the shift in electrical parameters for failed devices and the increase in work function detected by the ChemetriQ system.

Summary

In this paper we have presented the detection and elimination of a yield-critical residue at the FEOL gate and spacer module. The contamination responsible for the yield loss is an example of an NVD, which could not be detected using optical inspection. In this case the residue was detected using a scanning probe technique that detects changes in surface work function, which can be induced by chemical contamination or charging of dielectric films. Surface work function inspection results were used to identify and modify the clean process responsible for the defect. As a result, the defect was eliminated and yield was increased. The inspection system was subsequently used to monitor the process to insure that the defect did not recur. ◆

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Multiphysics simulation accelerates the development of electrochemical etching

JENNIFER A. SEGUI, *COMSOL, Inc., Burlington, MA.*

A team of researchers from Germany use multiphysics simulation to elucidate the impact of important process variables in the electrochemical etching of silicon and make progress toward the integration of the process for commercial applications.

Electrochemical etching, also referred to as anodization, represents a flexible process that is used to produce well-controlled three-dimensional structures in silicon. There are many variables that affect the etching process and therefore complicate the integration of the technique into mass production. In their work, Alexey Ivanov of Furtwangen University, Ulrich Mescheder of Furtwangen University, and Peter Woias of the University of Freiburg-IMTEK (all located in Germany) are developing an approach to further understand the electrochemical etching of silicon through the use of multiphysics simulation. Their work can ultimately facilitate the efficient integration of electrochemical etching into large-scale silicon wafer process. In correspondence with Alexey Ivanov, he explains that the "...process has some properties, such as high surface quality and electrically controlled formation of 3D forms, which make this process unique for some applications where other micro structuring techniques are not applicable."

Two specific modes of operation for the electrochemical etching of silicon in hydrofluoric acid (HF) have been identified that are particularly relevant to industry-scale process. These modes, depicted in **FIGURE 1**, are selected through control of the electrical current density and electrolyte solution concentration governing the electrochemical reaction. In the first mode, a low current density and high concentration solution result in an electrical current dominated process that creates a porous silicon layer.

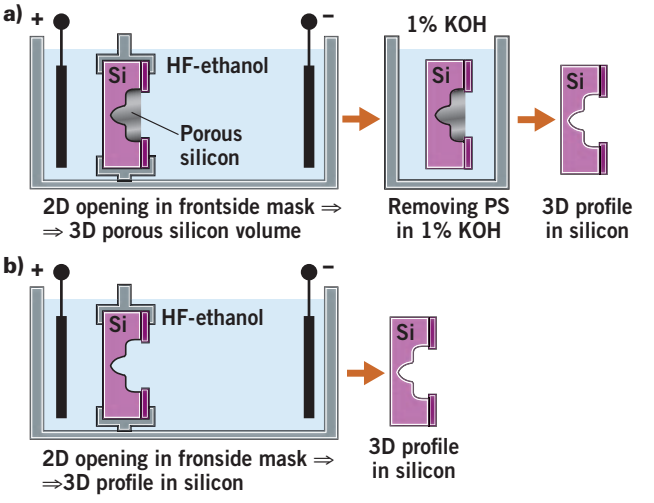

FIGURE 1. Two modes of electrochemical etching of silicon wafer include (a) porous silicon formation and (b) electropolishing.

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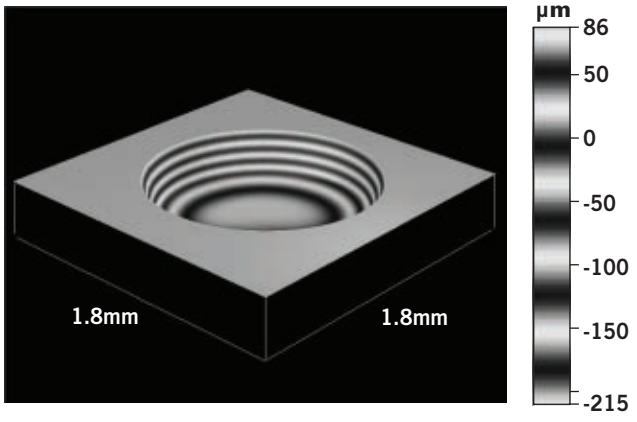


FIGURE 2. Smooth and well-controlled electrochemical etching of a silicon wafer to produce a master mold for polycarbonate optical lenses.

This porous silicon can be incorporated as a microchannel filter in microfluidics, according to Ivanov.

The second mode of operation is achieved through application of a high current density and low concentration solution where the result is a diffusion controlled electropolishing process. The electropolishing of silicon using this technique creates surfaces with roughness on the order of nanometers enabling its use in the most demanding optics and microfluidics applications as shown in **FIGURE 2**.

Parameters that affect the resulting etch forms in silicon include the electrolyte concentration and temperature, silicon substrate dopant type and concentration, magnitude of applied current, and mask opening dimensions. In this article, we further explain the electrochemical etch process and mechanism, etch form development particularly for the two primary modes of operation, and the use of multiphysics simulation to better understand the impact of each parameter on the etching process.

Electrochemical etching of silicon

The electrochemical etching of silicon is performed using an HF-ethanol electrolyte solution. A silicon substrate with insulating stress-free silicon nitride (SiN_x) layer on the front side is submerged into an HF-stable tank containing the electrolyte solution and two platinum electrodes as shown in Fig. 1. A positive electric potential is applied to the anode while the cathode remains grounded. The SiN_x layer on the front side of the silicon substrate serves as a mask or template to guide the formation of structures during the etch process. For clarity, we explain the process and mechanism of electrochemical etching for p-type silicon (10-20 Ohm·cm, (100)-Si, and ~ 520µm thickness), however, the technique can also be modified for use on other substrate types. For p-type silicon of this low resistivity, the back side of the wafer should be highly doped in order to form an ohmic contact with the electrolyte.

At low current density (low supply of holes) and high HF concentration (high supply of fluoride-ions) silicon atoms are directly dissolved with consumption of two holes per silicon atom (e.g. with a reaction valence of 2):

$$Si + 4HF_2^- + h^+ \rightarrow SiF_6^{2-} + 2HF + H_2 + e^-$$

In this mode, silicon atoms are dissolved selectively from the substrate producing pores of various shapes that are etched into the silicon. The skeleton of porous silicon remains crystalline.

At higher current densities (higher supply of holes from silicon) and lower HF concentration in the electrolyte (lower supply of fluoride-ions), the mechanism of silicon dissolution has two steps. In the first step, anodic oxidation takes place under the supply of four holes per silicon atom:

$$Si + 2H_2O + 4h^+ \rightarrow SiO_2 + 4H^+$$

The second step runs without consumption of positive charge from the substrate and consists of silicon dioxide dissolution in HF:

$$SiO_2 + 2HF_2^- + 2HF \rightarrow SiF_6^{2-} + 2H_2O$$

Thus, dissolution of silicon in electropolishing mode runs with a reaction valence of 4.

The current flow through a p-type silicon (p- Si) sample with front side SiN_x masking layer is shown schematically in **FIGURE 3A**. In the beginning of the process, there is a higher etch rate near the edges of the mask, and a so-called edge-effect (convex) shape is observed as indicated in Figure 3b. Etch form transformation from convex to concave, in Figure 3c, has been observed in the experiments for longer etching times.

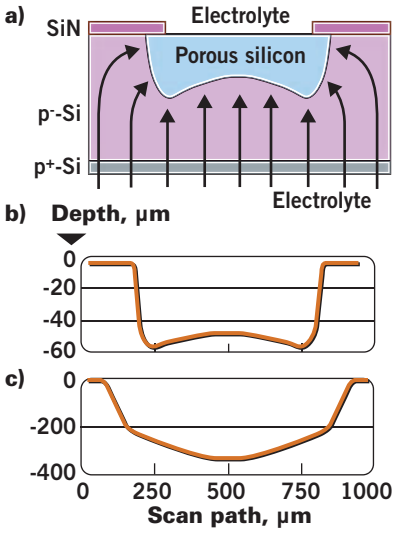


FIGURE 3. Etch form development during the electrochemical etching of silicon: (a) schematic cross-section of a silicon sample, arrows represent current flow, (b,c) profile of structure etched through a 600 µm circular opening in a SiNx masing layer in 30 wt% HF at 2.5 A/cm2 for (b) t = 1 min and (c) t = 10 min; measured with a stylus profilometer; straight regions on both sides of the concave profile are measurement artifacts.

Two mechanisms are proposed to explain shape development. First, the specific current density distribution in silicon leads to the formation of a convex shape at the beginning of the process. The current is more concentrated at the edge when compared with the center of the structure. Etching deeper into the substrate will lead to formation of a more concave shape assuming that the conductivity of the electrolyte and substrate are similar.

Additionally, the shape conversion can be assisted by ionic transport in the electrolyte for the particular case of a diffusion-controlled etching process. The resulting concentration of reacting ions is then critically dependent on geometric parameters such as mask thickness and opening size. The ion concentration will change during etching and will convert the etch shape from convex to concave (isotropic). This is a well-known phenomenon in wet chemical etching.

Simulation of the electrical and diffusion etch processes

The two mechanisms of shape transformation described in the previous section appear to play different roles in the etching process depending on the applied current and electrolyte concentration. As a first step on the way to a full model of the electrochemical etching process, Ivanov and his colleagues simulated the electrical and diffusion mechanisms separately. The respective models are presented in this section.

For both cases, the models have been simulated in 2D with axial symmetry. The geometry of the models consists of the computational domains shown in **FIGURE 4d**.

The movement of the etch front was implemented with the *moving mesh* feature demonstrated in Figures 4a-c, where the dynamic deformation

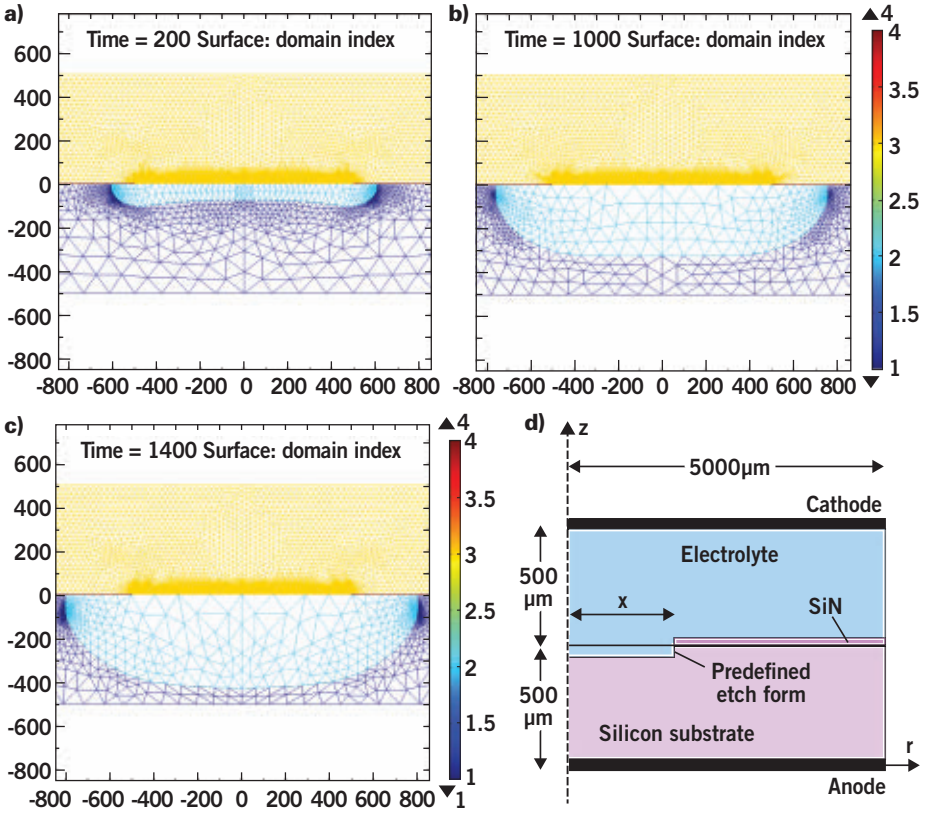


FIGURE 4. Model geometry and demonstration of the moving mesh feature available in COMSOL Multiphysics. (a-c) Moving mesh front changing from convex to concave etch form as time lapses; (d) computational domains defined in the model including a predefined etch form as an initial condition that is necessary for the simulation to proceed.

of the interface between the silicon substrate and the "predefined etch form" is driven by the electrochemical reactions. A further enhancement of the simulation process for deep etch forms was achieved by applying the automatic remeshing feature. The simulation was performed in COMSOL Multiphysics.

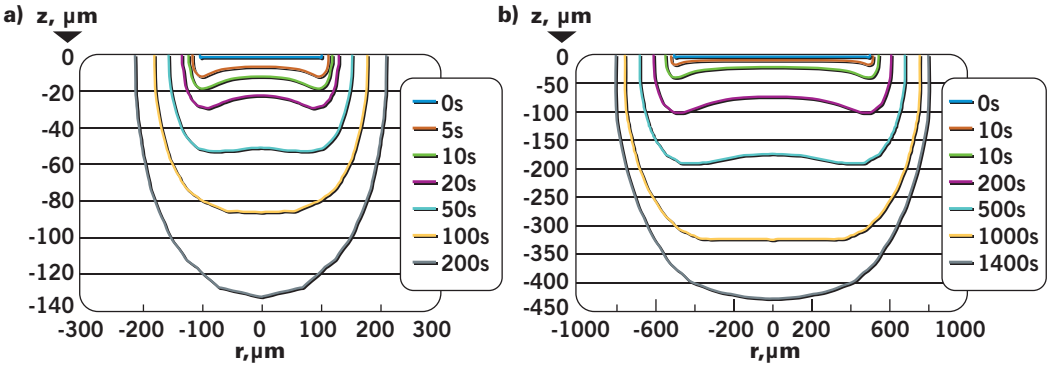


FIGURE 5. Resulting etch forms from the electrical models with low electrolyte conductivity and opening diameter in the masking layer of 200 µm (left) and 1000 µm (right).

The *Electric Currents* physics available in COMSOL Multiphysics has been applied to all domains for simulation of the current flow in the model. Etch front movement for two values of electrolyte conductivity were simulated. The parameters defined for the domains are summarized in Table 1. For the boundary between the initial etched region and the silicon substrate (etch front), a *prescribed mesh velocity* in cylindrical coordinates is defined by:

$$\upsilon_r = -K_E \cdot j_r$$
$$\upsilon_z = -K_E \cdot j_z$$

where j_r and j_z are the r and z components of the current density vector, and K_E is a constant for the electrical model that takes into account the density of silicon and the reaction valence. If we assume electropolishing mode, i.e. no porous silicon formation, then:

$$K_E = \frac{1}{z \cdot e} \cdot \frac{M_{Si}}{\rho_{Si} \cdot N_A}$$

where z is the reaction valence, e is the elementary charge, M_{Si} is the molar mass of silicon, ρ_{Si} is the density of silicon and N_A is the Avogadro constant. For the reaction valence of 4:

$$K_E = 3{,}1234 \cdot 10^{-11} \frac{\mathrm{m}^3}{A \cdot s}$$

During simulation, an electric potential of 1 V was applied to the anode while the cathode was grounded.

TABLE 1. Material properties of the domains in the electrical model

Domain	Electrical conductivity [S/m]	Relative permittivity
Electrolyte	High = 10^4, Low = 10	80.1
Silicon	10	11.1
Silicon nitride	0	7.5

As an example, the resulting etch forms for opening diameters of 200 µm and 1000 µm in the SiN_x masking layer are shown in **FIGURE 5**. Corresponding current and potential distributions for the models with an opening diameter of 1000 µm are shown in **FIGURE 6**.

For the electrical model, the researchers note that in the beginning of the process there is higher current density near the edges of the SiN_x masking layer leading to the formation of the convex edge effect etch form. However, there is a discrepancy in the further development of the etch shapes. In the electrolyte with low conductivity, convex shapes transform into concave during the etching process as shown Figures 5 and 6. In the highly conductive electrolyte, however, deeper parts of the etch form near the edges of the opening lead to a further increase in current. This is due to a lower resistance in regions that are filled with highly conductive electrolyte and causes the edge effect to become self-amplifying.

The *Transport of Diluted Species* physics available in COMSOL Multiphysics interface has been applied to the simulation of diffusion in electrolytes.

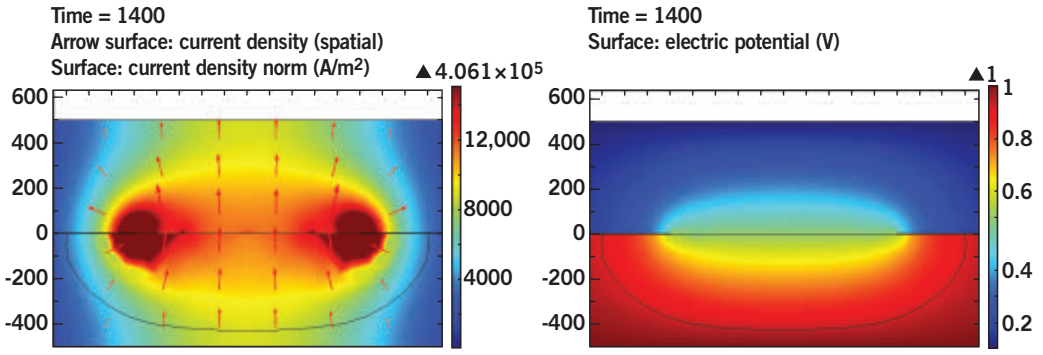


FIGURE 6. Current density (left) and potential distribution (right) for the electrical model with the low conductivity electrolyte and mask opening diameter of 1000µm at the end of the process. Arrows on the current density plot represent current flow.

The following parameters have been used in the model:
- initial electrolyte concentration

$$c_0 = 5.7483 \text{ M}$$

- diffusion coefficient for HF and HF_2^-

$$D = 3 \cdot 10^{-9} \text{ m}^2/\text{s}$$

- reaction rate variable defined for the boundary between electrolyte and the silicon substrate for the 1st order reaction (where a reaction rate constant k = 1 m/s is assumed in order to provide a diffusion-controlled process)

$$R = k \cdot c$$

For the boundary between the electrolyte and the silicon substrate domains (etch front), a prescribed mesh velocity is defined as follows:

$$\upsilon_r = R \cdot K_D \cdot n_r$$
$$\upsilon_z = R \cdot K_D \cdot n_z$$

Where *nr* and *nz* are normal vectors and K_D is a constant for the diffusion model:

$$K_D = \frac{M_{Si}}{m \cdot \rho_{Si}}$$

where *m* is a number of fluorine atoms needed for dissolution of one atom of silicon. In the electropolishing mode, six atoms of fluorine are required in the reaction of silicon dioxide dissolution. Then:

$$K_D = 2{,}01 \cdot 10^{-6} \frac{\text{m}^3}{\text{mol}}$$

For the boundary between the electrolyte and the silicon substrate, an *inward flux* equal to -*R* has been defined. The concentration was fixed to c_0 for the top, left, and right side boundaries of the electrolyte.

For all opening diameters in the SiN_x masking layer, the formation of a convex shape in the beginning of the process with subsequent transformation to a concave shape was observed.

Due to diffusion limits, concave isotropic form is achieved when the distance from the opening in the masking layer to the etch front becomes comparable to the diameter of the opening. For opening diameters of 40µm and 800µm, concave form is observed at depths of 10.5µm and 276µm, respectively. Further supply of chemical species to the reaction site through the opening in the masking layer after this depth can be regarded as a point source that is equally distant from all the points in the etch front. This creates a uniform etch rate along the etch front.

The diffusion model is limited in scope in that it only considers diffusion transport in electrolytes. There are other transport phenomena in the process such as convection and drift and so their influence on etch form will need to be evaluated in further work.

Summary

The electrochemical etching of silicon in HF represents a versatile process that depends on many variables. The use of multiphysics simulation to investigate the impact of process variables will lead to a viable commercial process that is relevant for a range of substrate types and applications. This article is based on an article by A. Ivanov and U. Mescheder, "Dynamic Simulation of Electrochemical Etching of Silicon with COMSOL," presented at the COMSOL Conference 2012, October 10-12, 2012, Milan, Italy.

A Preview of Semicon West 2013

DEBRA VOGLER, *SEMI, San Jose, CA*

Semicon West 2013, to be held July 9-11 at the Moscone Center in San Francisco, will feature over 500 exhibitors, 50 hours of conference programs and more than 30,000 industry attendees. Hot topics to be discussed at the show include dynamic changes to R&D processes, tools, technical challenges, and funding/business models.

The critical processes and technologies necessary to continue Moore's Law are currently more uncertain than ever before in the history of advanced semiconductor manufacturing. At Semicon West, SEMI will provide multiple forums to assess these uncertainties and provide the latest information on EUV lithography, 3D transistors, 450mm wafer processing, and other challenges.

Intel's Shekhar Borkar talks at a TechXPOT session.

Although progress to take EUV lithography into the realm of high-volume manufacturing continues to be made, the readiness of source technologies, mask infrastructure and resist performance are still not known with a high degree of certainty. Until EUV Lithography is ready for high-volume manufacturing, the industry will continue to rely on double-patterning and even multiple-patterning lithography schemes using 193 immersion technology to take it beyond 22nm. How the industry will address these barriers, uncertainties and alternatives will be the focus the lithography session at SEMICON West — including the following speakers and topics:

- Skip Miller, ASML — NXE Platform Performance and Volume Introduction
- Stefan Wurm, Ph.D., SEMATECH — Mask and Resist Infrastructure Gaps
- Ben Rathsack, Tokyo Electron — Advances in Directed Self-Assembly Integration and Manufacturability on 300mm Wafers

DEBRA VOLGER *is a contributing editor to SEMI, San Jose, CA and president of Instant Insights.*

- Mike Rieger, Synopsys — Collaboration to Deliver Lithography Solutions
- Nikon Precision — ArF Lithography Extension Through Advanced Overlay and Imaging Solutions

The mobile market is driving the move to novel transistor architectures that offer greater performance and power benefits than traditional planar architectures. Memory and logic manufacturers are pursuing different strategies including leveraging innovations in design rules, new channel materials and processes (e.g., MOCVD) and inspection and metrology challenges. Speakers and topics on the challenges of nonplanar transistor processing include:

- Gary Patton, Ph.D., IBM Semiconductor Research and Development Center — Meeting the Challenges of Next-Generation Scaling
- Subramani Kengeri, GLOBALFOUNDRIES — Enabling SoC Level Differentiation Through Advanced Technology R&D
- Michel Haond, STMicroelectronics — Main Features and Benefits of 14nm Ultra Thin Body and BOX (UTBB) Fully Depleted SOI (FD-SOI) Technology
- Paul Kirsch, Ph.D., SEMATECH — Non-Silicon R&D Challenges and Opportunities
- Adam Brand, Applied Materials — Precision Materials to Meet FinFET Scaling Challenges Beyond 14nm
- Joe Sawicki, Mentor Graphics — New Approaches to Improving Quality and Accelerating Yield Ramp for FinFET Technology

While materials, architecture and processing technologies are undergoing revolutionary change, wafer processing platforms are also being radically transformed with a planned transition to 450mm wafers. For chip manufacturers and suppliers, this will involve increased levels of collaboration, further advancements in tool prototypes, and increased visibility into related supply chain implications. The SEMICON West 450 Transition Forum will provide the latest updates on the status of 450 R&D, as well as a review of key technology considerations and a discussion of implications and opportunities for the supply chain.

Each of these programs will take place in the TechXPOT conference sessions on the exhibit floor. Other TechXPOT programs include sessions on 2.5D and 3D IC Packaging, Productivity Innovation at Existing 200mm/300mm Fabs, Silicon Photonics, Lab-to-Fab Solutions, MEMS, LED Manufacturing, and Printed and Flexible Electronics.

Sub-20nm front-end challenges

In advance of the 2013 SEMICON West TechXPOTs on lithography and nonplanar transistors beyond 20nm, SEMI asked some of the speakers to comment on the challenges they wanted to highlight.

Just as a boxer avoids a surprise shot to the head or torso by using a "duck and weave" maneuver, so to must front-end technologists confront the challenges associated with extending optical lithography while planning for EUV lithography's eventual high-productivity solution. For the industry, particularly foundries that generally need to handle multiple platforms for a variety of customers — there is the added pile-on arising from developing the two paths to accomplish control of short channel effects and leakage in transistors beyond 20nm, i.e., ultra-thin silicon-over-insulator (SOI)-based technologies and FinFETs. This year's SEMICON West front-end processing TechXPOTs on lithograph and transistors below 20nm will provide critical updates on how technologists are coping with these "contenders."

Channel materials: a progression of SiGe alloys

Whether an IC manufacturer chooses to make the giant leap to 3D transistors (e.g., the tri-gate), or takes an evolutionary approach (e.g., using SOI-based technology as a bridge), all roads lead to the implementation of 3D transistor architectures. No matter the path, however, new channel materials will have to be developed. Paul Kirsch, director of the Front-end Process Division at SEMATECH, anticipates that there will be a progressive range of Germanium (Ge) being added to Si – from perhaps 25 percent Ge up to 100 percent Ge — to form channels in pMOS FETs first, followed by nMOS FETs for logic applications. "Industry has a great deal of experience with SiGe already," notes Kirsch. "It's understood how to handle that material in the fab and it's well understood and had good performance benefits in the pMOS FET." What does need more attention,

however, is making SiGe work for the nMOS FET — particularly for contacts and gates. Kirsch further anticipates seeing SiGe entering the roadmap between the 14nm, 10nm, and 7nm nodes, with the possibility that some IC manufacturers could start even sooner than 14nm.

A major hurdle that has to be overcome in the implementation of III-V materials is being able to engineer out the defects from the epitaxial material and the surrounding architecture of the fin to reduce the leakage current. Molecular beam epitaxy (MBE) is too expensive mainly because of its low throughput. This will mean improving what Kirsch says is the preferred process — metalorganic chemical vapor deposition (MOCVD). In addition to engineering out defects, the industry will have to fully understand ESH issues because the source materials for this process are toxic and pyrophoric. "That's not to say they can't be understood and handled safely because we have toxic and pyrophoric materials in the fab already, but every process is a little different and attention needs to be given to these materials to make sure that we are handling them very safely," says Kirsch.

Staying with a planar solution

STMicroelectronics' marketing director of Technology R&D for the Digital Sector, Giorgio Cesana, told SEMI that regardless of the many techniques to extend the technology roadmap, conventional planar bulk technology is reaching its limits. "The last node will be 20nm because it is unable to provide the traditional speed/power gain vs. the 28nm node," said Cesana. To continue to follow the Moore's Law roadmap, the industry has developed new techniques to produce fully-depleted transistors that overcome traditional bulk planar limits. There are two possibilities: stay on a planar (2D) transistor structure obtaining fully-depleted devices using a thin SOI substrate, or move to FinFET 3D structures.

"STMicroelectronics has opted for the planar solution built on a thin silicon film above a thin buried oxide layer, which is simpler to manufacture while still offering the same fully-depleted benefits," explained Cesana. With the company's 28nm FD-SOI node in production, it is now focusing on the development of the next node. "At 14nm, this will implement a set of new features for further increasing performances while optimizing power consumption and operating at reduced voltage levels."

Test and diagnosis at 16/14nm and beyond

As the industry moves to 3D transistor architectures, Joe Sawicki, VP and GM of the Design-to-Silicon Division at Mentor Graphics, observes that at 16/14nm, "You're not just dealing with scaling, you're dealing with fundamental changes in the transistor and cell architectures. How defects will manifest themselves and behave in these new architectures is still an unknown." The key, he pointed out, is going after potential defects at the transistor level using a test generation technology that looks into the standard cell itself (i.e., cell-aware automatic test pattern generation (ATPG)). "Unlike the standard test pattern generation used today that just looks at the logical boundary of the cell and tries to ensure that all the interconnects are wired correctly, cell-aware ATPG takes that one step further by looking into the standard cell transistor structures to test and ensure that all the individual transistors and the connections between them are functional."

Though defects that might be unique to FinFET structures below 16nm are still to be determined, Sawicki explains that cell-aware ATPG is capable of defining both static and dynamic fault models on the transistor structures, as well as on the cell-internal interconnect. "It has already been successful in finding defects at other nodes that the traditional fault models miss," said Sawicki.

As cell-aware testing goes from 20nm to 14nm, Sawicki anticipates that the only evolution in going to the next node will be in the SPICE level model characterization to create the initial cell-aware fault models. "Defects in FinFET transistors may cause different behaviors and require slightly different fault models to detect them," said Sawicki. "Since the cell-aware technology starts with a transistor level cell characterization step to create the fault model, it's expected that from a usage and ATPG process point of view, there should be little additional evolution to the technology for FinFET technology."

Industrial picosecond laser

Spectra-Physics introduced Spirit ps 1040-10, an industrial-grade picosecond laser for precision micromachining applications. The new laser delivers high finesse with exceptional beam quality (M2< 1.2), high stability (<1% rms over 100 hours), and short pulse widths (13 ps). The laser is also highly flexible with user-adjustable repetition rates from single shot to 1 MHz and an integrated pulse picker for fast pulse selection and power control. With >10 W average power, the laser is ideal for precision picosecond micromachining applications such as semiconductor and LED manufacturing, flat panel display processing, thin film ablation, and nano structuring.

Spectra-Physics' Spirit ps 1040-10 laser is based on the field-proven Spirit industrial ultrafast laser platform. With high quantities of deployed systems in demanding 24/7 applications, this rugged product platform has consistently demonstrated high reliability.

Spectra-Physics, Stahnsdorf, Germany,
www.newport.com/cms/brands/spectra-physics

Automated measuring for semiconductor device images

It can be very time-consuming for engineers to measure the various features of an X-SEM image of a semiconductor device. These manual measurements of trenches, pillars, lines and spaces can also be inaccurate and there is frequently inconsistency between how engineers do the manual measurements. The collection of data is often very time-consuming as well.

With the new PCI-AM (Automated Measurement) module, engineers simply click inside the feature and the measurement is done automatically with increased accuracy and consistency among all engineers. The measurement results are displayed on the image and in a spreadsheet grid. The data in the grid can be easily exported into a CSV file suitable for importation into other software such as Microsoft Excel. The images and data can also be easily included in standard Quartz PCI reports with just a few clicks.

Quartz Imaging, Vancouver, BC Canada,
www.quartzimaging.com

Latest version of automated resist processing system

EV Group (EVG) introduced the latest version of its EVG120 automated resist processing system. The EVG120 automated resist processing system features a new robot with dual arms for fast wafer swapping and additional processing chambers, which result in enhanced throughput and overall productivity. To further optimize throughput and overall productivity, the new EVG120 runs the same EVG CIM Framework software as EVG's high-end XT Frame systems and offers full software integration with SECS/GEM standards. Two customizable wet processing bowls are complemented by 10 stacked modules for vapor prime, soft and hard bake, and chill processes. Like its predecessor, the EVG120 system can accommodate wafers up to 200mm in diameter.

Other new features of the EVG120 system include EVG's innovative CoverSpin rotating bowl cover that allows improved coating uniformity across the substrate regardless of substrate shape. A new, temperature-controlled chuck further enhances EVG's proprietary OmniSpray coating technology, which specifically

allows conformal coating of high-topography surfaces via its proprietary ultrasonic nozzle. OmniSpray coating is ideally suited for ultra-thin, fragile or perforated wafers and can result in an 80-percent or greater reduction in material consumption compared to traditional spin coating.

EV Group, St.Florian am Inn, Austria, **www.evgroup.com**

A new way to discover and monitor defects

In the world of optical defect inspection, finding on defect on a 300mm wafer can be like trying to find a single coin on the island of Taiwan. Now imagine being able to find that coin in just an hour, along with any other coins that look exactly like it. That's what NanoPoint will allow manufacturers to do. KLA-Tencor's NanoPoint is a new family of patented technologies for its 2900 series defect inspection system.

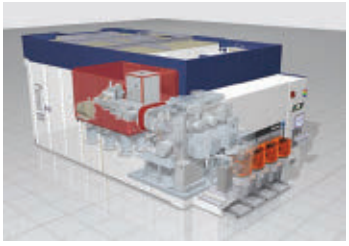
"[NanoPoint is] a new algorithm," said Satya Kurada, product marketing manager at KLA-Tencor. "We now have the ability to generate care areas significantly smaller to inspect smaller areas, and remove noise from the pattern of interest. This will focus inspection resources on critical patterns."

KLA-Tencor believes that NanoPoint represents an entirely new way to discover and monitor defects, at optical speed and on existing optical defect inspection equipment. By automatically generating millions of very tiny care areas based on user-defined patterns of interest, NanoPoint focuses the resources of the optical inspection system on critical patterns, as identified either by circuit designers or by known defect sites. During chip development, NanoPoint can reveal the need for mask re-design within hours, potentially accelerating the identification and resolution of design issues from months to days. During volume production, NanoPoint can selectively track defectivity within critical patterns—allowing process monitoring with sensitivity and speed far beyond the industry's experience to date.

KLA-Tencor, Milpitas, California, **www.kla-tencor.com**

Next generation single wafer high energy implanter

Axcelis Technologies, Inc. announced the introduction of the Purion XE next generation single wafer high energy implanter, the second tool in its expanding family of



Purion ion implanters. The Purion XE is an evolution of the Optima XEx, combining the process and productivity advantages of the Optima XEx linear accelerator and beamline technology with the reliability, precision, process flexibility, and performance options that define the Purion platform. The Purion Platform enables high yield manufacture of sub 16nm planar and 3-D devices. All Purion implanters incorporate advanced filtration systems, for beam purity, so even the most sensitive devices are implanted for optimized device performance. The platform's angle control system and constant focal length scanning deliver the most precise and repeatable dopant placement available today. The scanned spot beam architecture designed into the platform enables control of damage engineering as well as other advanced process enabling implants using materials modification techniques required in leading edge device processes.

Axcelis Technologies, Beverly, Massachusetts, **www.axcelis.com**

High power contractor, ecoAmp, approved for automotive applications

Multitest's ecoAmp is a high power contactor that allows for testing at the full temperature range from -60°up to 175°C, which is a standard requirement for automotive applications. The ecoAmp is able to stand the high thermal stress and support temperature stability during test. Thermal energy dissipation requires thermal management within the contactor.

The ecoAmp specifically responds to the challenging requirements of high voltage/high current test. All typical packages and modules for power applications are covered by the ecoAmp, including MOSFETs, drivers, IGBTs, power modules, and power packages such as TO, SO and DIP. The ecoAmp is designed for an electrical performance of 500+ amperes with an inductance of 1.0 nH and below for 0.5mm pitch.

Multitest, Rosenheim, Germany, **www.multitest.com**

Nanoelectronics *Continued from page 11*

(NSF) and the multi-university research network involves 34 universities in 17 states.

"In 2012, the first phase of NRI culminated with a comprehensive assessment of the various NRI device concepts through performance benchmarking," said Tom Theis, the new SRC program executive director. "NRI 2.0 will focus on key research opportunities identified in the benchmarking study and will explore the ultimate scalability of emerging digital device concepts and their functionality beyond digital logic. For example, researchers will explore magnetoelectric devices that promise improved energy efficiency and the ability to combine memory and logic."

NRI 2.0 is the successor to an earlier multi-year collaboration between NRI and NIST that focused on the long-term goal of "developing the next logic switch." The NRI initiative was originally launched by the Semiconductor Industry Association (SIA) in 2005. The Nanoelectronics Research Initiative is one of three research program entities of SRC aimed at extending the frontiers of semiconductor electronics.

Statistical variation is difficult to measure using traditional parametric test methods where each transistor is attached to four probe pads. Statistical variation measurements require the use of on-chip multiplexers and may be enhanced by on chip measurement techniques.

On chip multiplexers using kelvin measurement techniques can build arrays of hundreds and even thousands of transistors, metal lines or vias accessed using only a few pads (**FIGURE 6**). A power supply, a pulse generator and a voltmeter or DAQ is all that is required to measure these arrays. An array of 500 transistors could be measured with as few as 4 probe pads.

On board A/D converters will accelerate the throughput of these tests, allowing parallel testing with few probe pads while the close space between the transistor and the instruments gives less measurement noise. ◆

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A new era in equipment product development

Over the past few years the semiconductor market has provided some breathing space on the development of next generation manufacturing equipment. Capacity, rather than technology, has been the driver as manufacturers try to leverage prior investments in a period of global uncertainty. That period has come to an end. The reality of 450mm production combined with the 10nm technology driver will require the development or redevelopment of many tools from the ground up.

This alignment of technology leaps is hitting the semi-equipment industry when it is still recovering. The brutal downturn of 2008 directly hit engineering; and the current semi-equipment business landscape is still no prettier. Engineering is much smaller, less experienced, and more geographically dispersed. Much of the past decade was focused on doing more with less. A larger amount of engineering emphasis has been on more cost-effective sustaining engineering and less on cutting-edge product development. Retention of experienced engineers has been challenging - especially with the explosion of mobile, cloud and social media vying for the brightest engineering talent. Exacerbating the situation is the limited experience most organizations have in new product development utilizing engineering teams distributed across time zones.

The pressures for 450mm are strong. Most extant 300mm tools were developed in the late 90s. The step from 200mm to 300mm was painful from a technical and business perspective. The efforts came in the middle of a large ramp in the semi-equipment industry and development efforts were staffed with less experienced engineers. Schedules and budgets overran – often by many hundreds of percent. Initial reliability was poor, driving up retentions and field support costs. In many cases, the delays stabilizing 300mm products imperiled corporate viability. Dramatic improvement in productive capacity limited the number of tools shipped, further eroding the economics.

The next few years will be no less complex. The process shrink to 14nm, then 10nm in 2016, on 450mm wafers will present extremely complex challenges and require sophisticated new equipment and analytics. The reliability expectations of the fabs are also daunting; no less up time than the current generation.

> The skills to develop new products are very different than those to make incremental improvements. Failing to address this limitation will put equipment companies' plans – and market shares – at serious risk.

Experienced engineering is critical to successfully completing these product development efforts. Repeating the lessons of the 1990s will dramatically impact schedules and budgets; a repeat of the 300mm experience, but with much less financial leeway.

Tool makers' engineering organizations have been optimized for incremental improvements on a mature technology foundation. Now more than 15 years old, they need to be reviewed, revised and updated. The skills to develop new products are very different than those to make incremental improvements. Failing to address this limitation will put equipment companies' plans – and market shares – at serious risk.

Successful development of your next generation semi tool will either provide the foundation for the next 10-plus years or financially threaten your organization. The technical challenges are extreme. They require a dedicated, experienced, highly skilled development capability in order to be successful. Addressing these organizational development needs holistically, before embarking on the product development process, will provide executives the opportunity to avoid mistakes of 300mm migration during the evolution to 450mm equipment.

TIM BOWE *CEO of Foliage*

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