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An operator makes an adjustment on an ASML TWINSCAN lithography system. Source: ASML.

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First quarter semiconductor trends

Industry trends show the first quarter of this year being generally stronger than the first quarter of one year ago. SEMI's Dan Tracy reviews the trends and updates.

http://bit.ly/1wlVbRR

DAC panels tackle giga-scale design

The ProPlus blog here on Solid State Technology has looked at giga-scale design challenges and, this year, so will the Design Automation Conference (DAC). Dr. Lianfeng Yang of ProPlus Design Solutions blogs on the upcoming DAC.

http://bit.ly/1kpMctq

Improving financial predictability: Chasing a mirage?

Prakash Arunkundrum, PwC Strategy and Operations Consulting Director, says there is continued evidence that despite spending several millions on IT transformations, improving internal planning processes, maturing supply chains, and streamlining product development processes- several companies still struggle with predicting their financial and operational performance.

http://bit.ly/QZOZxV

Can legacy fabs keep up with IoT demand?

The Internet of Things (IoT) is set to drive demand and innovation in the semiconductor market over the next decade. While some consumer IoT applications will require semiconductors manufactured using cutting-edge technologies to deliver fast performance and low power consumption, the vast majority of chips for IoT applications will be utilized in client-side applications. These chips, such as a sensor monitoring room temperature in a connected HVAC system, require processing capabilities that can be met using legacy process (90 and 45nm) technologies manufactured on 200mm wafers. Applied Materials' Jeremy Read writes on this opportunity and challenge for legacy manufacturing.

http://bit.ly/1tVGaFc

n&b news and blogs

Insertion of EUVL into fab: Challenges for 7nm insertion

While two chipmakers are reported to be working on inserting EUVL into fabs for manufacturing at the 10nm node, many others expect to insert EUVL into manufacturing at the 7nm node or later. It takes a large infrastructure to make EUVL a manufacturing technology. So many tool suppliers, large and small, want to know when EUVL will be inserted into fabs for production and how and how much it will be used. Vivek Bakshi and Sushil Padiyar discuss the challenges of EUVL insertion in this SST blog.

http://bit.ly/1qxeC9N

Insights from the Leading Edge: More on IBM / GF; SEMI Singapore part 3: Nanium, Fujitsu, EVG

Dr. Phil Garrou blogs on the latest news from GLOBALFOUNDRIES and IBM, and continues his review of Semicon Singapore.

http://bit.ly/1knO7zn

Thoughts on MIG Conference Japan

MIG Executive Director Karen Lightman is finally over her jet lag and shares her thoughts from the MEMS Industry Group Conference Japan, MIG's inaugural conference in Asia that was held on April 24.

http://bit.ly/1ixng2G

editorial

The next big thing: IoT

The semiconductor industry has greatly benefited from the push to mobile technology, but what's next? It could well be the Internet of Things (IoT), which includes smart homes, smart cars, smart TVs, wearable electronics and beacons. According to an analysis by Business Insider, the Internet of Things alone will surpass the PC, tablet and phone market combined by 2017, with a global internet device installed base of around 7,500,000,000 devices.

> "The future IoT will need better image sensors, embedded DRAMs, high-voltage power ICs, RF, analog, and embedded flash."

In a keynote talk at the Advanced Semiconductor Manufacturing Conference (ASMC), John Lin gave some insight into the technology challenges the IoT will create. John is the Vice President and General Manager of Operation of G450C Consortium. Prior to joining G450C, Dr. Lin was the Director of Manufacturing Technology Center in TSMC.

"What is the next big thing?," he asked? In 2014, after mobile computing, we believe it is the Internet of things. Many of the devices needed to connect to the internet will grow very fast. We need to prepare the technology for that." John said the ultra-low power will be a primary concern. Processors, sensors and connectivity will also be key. "To support this at TSMC, we will continue with our ultra-low power efforts and continue to support advanced nodes, from 28, 20, 16 to 10nm." He also said the company will focus on "special" technologies such as image sensors, embedded DRAMs, high-voltage power ICs, RF, analog, and embedded flash. "All this will support all of the future Internet of Things," he said.

The Business Insider report also notes that the wearables, connected car and tv markets will equal the tablet market by 2018. Smart appliances are already going mass market. More than 250,000 Nest thermostats, for example, have already shipped this year. Connected TVs are overtaking traditional TVs: A connection to the internet will become common in fully loaded cars. US regulators are slowly allowing more aerial drones. Also expect to see more "beacons" in retailer establishments, such as Apple's iBeacons, which are used to communicate with shoppers in-store. And the list goes on... are you ready?

—Pete Singer, Editor-in-Chief

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USA | **GLOBALFOUNDRIES** introduced an optimized semiconductor manufacturing platform aimed specifically at meeting the stringent and evolving needs of the automotive industry.

USA | **Avago** completed its acquisition of LSI.

ASIA | **SMIC,** Wuhan Xinxin, Tsinghua University, Beijing University, Fudan University and the Chinese Academy of Sciences and Microelectronics have collaborated to setup the "IC Advanced Technology Research Institute" to create the most advanced IC technology research and development institution in China.

USA | **BASF** opened facility in Hillsboro, Oregon. The new facility is a strategic step towards establishing a North American footprint to supply materials for semiconductor manufacturing applications related to the electronics industry.

EUROPE | **Brooks Automation** announced a definitive agreement to acquire Dynamic Microsystems Semiconductor Equipment, based in Radolfzell, Germany.

EUROPE | **Element Six** announced that its Gallium Nitride (GaN)-on-Diamond wafers have been proven by Raytheon Company to significantly outperform industry standard Gallium Nitride-on-Silicon Carbide (GaN-on-SiC) in RF devices.

USA | **Mentor Graphics** announced that it has acquired Nimbic, Inc., a provider of Maxwell-accurate, 3D full-wave electromagnetic (EM) simulation solutions.

Applied Materials introduces the biggest materials change to interconnect technology in 15 years

In May, Applied Materials, Inc. announced its Applied Endura Volta CVD Cobalt system, the only tool capable of encapsulating copper interconnects in logic chips beyond the 28nm node by depositing precise, thin cobalt films. The two enabling applications, a conformal cobalt liner and a selective cobalt capping layer, provide complete enclosure of the copper lines, improving reliability by an order of magnitude. The introduction of cobalt as a superior metal encapsulation film marks the most significant materials change to the interconnect in over 15 years.

"The reliability and performance of the wiring that connects the billions of transistors in a chip is critical to achieve high yields for device manufacturers. As wire dimensions shrink to keep pace with Moore's Law, interconnects are more prone to killer voids and electromigration failures," said Dr. Randhir Thakur,

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Google Glass is far more than the sum of its parts, IHS Teardown reveals

Teardown analysis is a useful tool for understanding the component and manufacturing cost of electronics devices—but it doesn't always tell the whole story of the value of a product.

Case in point is Google Glass, which sells for $1,500—but has hardware and manufacturing costs that amount to just $152.47, according to a dissection of the product conducted by the Teardown Analysis Service at IHS Technology. Does that mean that Google is pocketing a sky-high margin of 90 percent on each Glass sale? Not by a long shot.

"As in any new product—especially a device that breaks new technological ground—the bill of materials (BOM) cost of Glass represent only a portion of the actual value of the system," said Andrew Rassweiler, senior director, cost benchmarking services for IHS. "IHS has noted this before in other electronic devices, but this is most dramatically illustrated in Google Glass, where the vast majority of its cost is tied up in non-material costs that include non-recurring engineering (NRE) expenses, extensive software and platform development, as well as

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SEMATECH achieves breakthrough defect reduction in EUV mask blanks

SEMATECH announced this month that researchers have reached a significant milestone in reducing tool-generated defects from the multi-layer deposition of mask blanks used for extreme ultraviolet (EUV) lithography, pushing the technology another significant step toward readiness for high-volume manufacturing (HVM).

Following a four-year effort to improve deposition tool hardware, process parameters and substrate cleaning techniques, technologists at SEMATECH have, for the first time, deposited EUV multilayers with zero defects per mask at 100nm sensitivity (SiO2 equivalent). Eliminating these large "killer" defects is essential for the use of EUV in early product development. These results were achieved on a 40 bi-layer Si/Mo film stack and measured over the entire mask blank quality area of 132×132 mm2.

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SRC and UC Berkeley pursue more cost-effective approach to 3D chip integration

University of California, Berkeley researchers sponsored by Semiconductor Research Corporation (SRC) are pursuing a novel approach to 3D device integration that promises to lead to advanced mobile devices and wearable electronics featuring increased functionality in more low-profile packages.

The research focuses on integrating extra layers of transistors on a vertically integrated 3D monolithic chip using printing of semiconductor "inks" as compared to the current method of

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Strengthening recovery: Fab equipment spending

After two years of decline, fab equipment spending for Front End facilities in 2014 is expected to increase 24 percent in 2014 (US$35.7 billion) and about 11 percent (US$39.5 billion). In terms of equipment spending, 2015 may reach or even surpass historic record year 2011 (about US$39.8 billion). For the May 2014 SEMI World Fab Forecast publication, SEMI tracked more than 200 major projects involving equipment spending for new equipment or upgrades, as well as projects to build new facilities or refurbish existing facilities. In the last three months, 265 updates were made to the database (Figure 1).

In 2014, the three largest regions for fab equipment spending will be Taiwan with over US$10.3 billion, the Americas with over US$6.8 billion, and Korea with over US$6.3 billion. In 2015, these same regions will lead in spending: Taiwan will spend over US$11 billion, Korea over US$8 billion, and the Americas almost US$7 billion.

Fab Equipment Spending Change Rates

	2012	2013	2014	2015
Americas	-15%	-34%	36%	2%
China	-40%	32%	69%	-6%
Europe & Mideast	-38%	-33%	79%	21%
Japan	-43%	8%	11%	15%
Korea	0%	-37%	23%	27%
SE Asia	-49%	53%	-43%	44%
Taiwan	4%	13%	11%	7%
SUM	-18%	-12%	24%	11%

(For Front End Facilities includes new, used, in-house).
Source: SEMI World Fab Forecast reports (May 2014)

Although in sixth in regional equipment spending this year, the Europe/Mideast region will show the strongest rate of growth, about 79 percent compared to the previous year. The same region will continue to grow fast in 2015, with an increase of about 20 percent.

Worldwide installed capacity is very low for both 2014 and 2015 and the SEMI data does not suggest that this will change over the next four years. Because of the increased complexity of leading-edge nodes, such as more process steps and multiple patterning, fabs experience a decline in capacity as the same fab space produces less. Worldwide, installed capacity grew by less than 2 percent in 2013 and is expected to grow just 2.5 percent in

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executive vice president and general manager of the Silicon Systems Group at Applied Materials. "The Endura Volta system builds on Applied's precision materials engineering leadership by delivering CVD- based cobalt liner and selective cobalt capping films that overcome these yield-limiting issues to enable our customers to scale copper interconnects to beyond the 28nm node."

The Endura Volta CVD system, with its two new process steps, represents a major technology extension for copper interconnects beyond 28nm. The first step involves the deposition of a thin, conformal CVD cobalt liner to increase the gap fill window of copper in narrow interconnects. This process improves the performance and yield of the device by integrating the pre-clean, PVD barrier, CVD cobalt liner and copper seed processes under ultra-high vacuum on the same platform.

The second step, a new "selective" CVD cobalt capping step, is deposited after CMP to encapsulate the copper lines for enhanced reliability performance. Complete envelopment of copper lines with cobalt creates an engineered interface that demonstrates over 80x improvement in device reliability.

"Applied's unique CVD cobalt processes represent an innovative materials-enabled scaling solution," said Dr. Sundar Ramamurthy, vice president and general manager of Metal Deposition Products at Applied Materials. "It is deeply satisfying that these materials and process innovations in development for almost a decade are now being adopted by our customers for their high-performance mobile and server chips." ◆

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tooling costs and other upfront outlays. When you buy Google Glass for $1,500, you are getting far, far more than just $152.47 in parts and manufacturing."

Looking through the Glass

Google Glass carries a BOM of $132.47. When the $20.00 manufacturing expense is added, the cost to produce the head-mounted computer rises to $152.47.

The attached table presents the preliminary BOM of Google Glass. Note that this teardown assessment is preliminary in nature, accounts only for hardware and manufacturing costs, and does not include other expenses such as software, licensing, royalties or other expenditures.

Prototypical

Although thousands of units are in the hands of users, Google Glass is not yet generally available through retail. The pre-mass-market status of Google Glass is evident by examining its design.

"Today's Google Glass feels like a prototype," Rassweiler said. "The design employs many off-the-shelf components that could be further optimized. If a mass market for the product is established, chip makers are expected to offer more integrated chipsets specific to the application that will greatly improve all aspects

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In addition, by subtracting out incoming substrate defects, SEMATECH has demonstrated that the multilayer deposition process itself can achieve zero defects down to 50nm sensitivity. Coupled with novel improvements to the mask substrate cleaning process to remove incoming defects, this represents the capability to both extend EUV to future nodes by eliminating smaller "killer" defects, and as a step to reducing smaller defects (which can be mitigated) to a level where improved yield and mask cost make EUV a more cost-effective HVM technology.

"SEMATECH's comprehensive programs continue to produce the results that our members and the industry need to show that EUV lithography is manufacturable," said Kevin Cummings, SEMATECH's Lithography manager. "Our Advanced Mask Development program continues to demonstrate practical results for mask blank defect reduction, more efficient deposition and cleaning, effective reticle handling, and other areas that the industry will need for successful EUV lithography manufacturing."

Defects are generally created by the deposition process or formed by decoration of substrate defects during the multilayer deposition process. These types of defects have prevented the quality of mask blanks from keeping pace with roadmap requirements for the production of pilot line and high-volume manufacturing EUV reticles. Reducing defects in the EUV mask blank multilayer deposition system is one of the most critical technology gaps the industry needs to address to enable cost-effective insertion of this technology at the 16nm half-pitch.

"A low defect density reflective mask blank is considered to be one of the top two critical technology gaps for the commercialization of EUV," said Frank Goodwin, manager of SEMATECH's Advanced Mask Development program. "Through sophisticated defect analysis capabilities and processes, the goal of our work is to enable model-based prediction and data-driven analysis of defect performance for process improvement and component learning. We then use these models to feed into the new deposition tool design."

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chip-stacking through 3D interconnect solutions.

The new process technology could help semiconductor manufacturers develop smaller and more versatile components that are less expensive and higher performing by enabling cost-effective integration of additional capabilities such as processing, memory, sensing and display. The low-temperature process is also compatible with polymer substrates, enabling potential new applications in wearable electronics and packaging.

Current efforts on 3D integration have used transfer of thin single crystal semiconductor layers, polycrystalline silicon deposited by chemical vapor disposition, or other growth techniques to realize integrated devices.

"Compared to these approaches, we believe our approach is simpler and potentially with significantly lower cost," said Vivek Subramanian, professor of Electrical Engineering and Computer Sciences at UC Berkeley. "Our goal in this work is to maximize performance, with the hope that this will make the cost versus performance tradeoff worthwhile relative to other approaches."

Specifically, the UC Berkeley team is developing directly-printed transparent oxide transistors as a path to realizing additional layers of active devices on top of CMOS metallization.

To fabricate such devices, new material and process methodologies are needed for depositing nanoparticles for semiconductors, dielectrics and conductors. The research is particularly focused on solution-based processing due its low temperature compatibility with CMOS metallization as well as the potential for lower cost manufacturing.

"Initial results from the Berkeley team show that reasonably high performance can be obtained from ink-jet printed devices with process temperatures that are compatible with post-CMOS metallization, thus enabling a new route to monolithic 3D integration," said Bob Havemann, Director of Nanomanufacturing Sciences at the SRC.

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of performance, including processing speed, energy efficiency, weight and size. Future product revisions are sure to make strides in all of these areas."

IHS Figure: Major Components in Google Glass (Preliminary Pricing in US Dollars)*

Direct Material Costs	$	132.47
Conversion Costs	$	20.00
Total Cost	$	152.47

Price	Description
$ 22.00	Frame assembly, titanium assumed
$ 20.00	LCOS panel, color sequential, 0.22 inch, 640 x 360 resolution, with embedded timing controller and thermal sensor
$ 12.50	Budget estimate for all box contents including stitched cloth case, premium USB cable, custom charger, earpiece, packaging and literature
$ 10.00	Flash, eMMC NAND, 16GB, MLC
$ 8.85	Apps processor, TI OMAP4, Dual
$ 8.35	Prism optics and LCOS-related films, plus budgetary subtotal for hinge assembly and plastic case
$ 7.50	SDRAM, mobile DDR2, 1GB, PoP
$ 6.65	Budget estimate for plastics and other mechanical shell components
$ 5.25	Camera module, 5MP
$ 4.10	Budget estimate for rest of PCB components and PCB substrate

Source: IHS Technology, May 2013

*Consists only of top 10 components

Last year's model

Most of the integrated circuits (ICs) in Google Glass are mature when compared with recent flagship smartphone designs. For example, the Texas Instruments Inc. OMAP4430 apps processor used in Google Glass is made with 45nm semiconductor manufacturing technology—two generations behind the 28nm chips employed in the latest flagship smartphones.

The use of more cutting-edge ICs could yield future Google Glass products that are smaller, lighter, more energy-efficient and less costly to produce than the current model.

High cost for LCOS

The second most expensive single component in Google Glass is also its most defining feature: its head-mounted liquid-crystal on silicon (LCOS) projector display. IHS estimates the cost of the Himax Technologies Inc. LCOS projection element made by Taiwan's Himax Technologies Inc. at $20.00, accounting for 15 percent of the total Glass BOM.

"The LCOS display is the sine qua non of the Glass," Rassweiler noted. "Just as e-readers wouldn't exist without their e-Ink screens, Glass wouldn't be possible with the LCOS display. The display is pretty slick, providing a near-eye viewing experience that must be seen to be believed."

Texas Instruments inside

Texas Instruments components dominate the Glass design, with the semiconductor supplier contributing the apps processor, power management IC, audio codec, battery fuel gauge and regulator ICs. Altogether, TI accounts for an estimated $37.90 worth of components identified so far in the Glass, representing 29 percent of the BOM.

Sensory overload

Glass includes two accelerometers: one from STMicroelectronics and another from InvenSense Inc. Accelerometers are commonly used to detect motion in electronic devices, such as smartphones and video-game controllers. Given that smartphones generally incorporate just one multiaxis accelerometer, the use of two of these devices represents an interesting and unusual design choice that must be further investigated to be understood.

Premium rush

The frame of the Glass represents the single most expensive component of the device, at $22.00, or 17 percent of the BOM. The frame is made of titanium, a highly durable and expensive material used in high-performance military aircraft and in some eyeglass frames. However, titanium is rarely used in commercial electronic devices analyzed by the IHS Teardown Analysis Service.

"The frame is just one aspect of how Google is presenting Glass as a premium product," Rassweiler noted. "The quality of the packaging and accessories, along with how the box contents are staged, gives the whole Google Glass experience a very high-end feel and appeal."

Continued from page 6

2014 and 3 percent in 2015.

SEMI's detailed data predict that Foundry capacity continues to grow at 8-10 percent yearly (a steady pace since 2012) and Flash is up 3 to 4 percent for 2014. Although DRAM equipment spending is expected to grow by 40 percent in 2014 as many fabs upgrade to a leading-edge process, installed capacity for DRAM is expected to stay flat or even drop 2 percent. SEMI's reports also cover capacity changes for other product segments: MPU, Logic, Analog/Mixed signal, Power, Discretes, MEMS, and LED and Opto.

The SEMI World Fab Forecast uses a bottom-up approach methodology, providing high-level summaries and graphs, and in-depth analyses of capital expenditures, capacities, technology and products by fab. Additionally, the database provides forecasts for the next 18 months by quarter. These tools are invaluable for understanding how the semiconductor manufacturing will look in 2014 and 2015, and learning more about capex for construction projects, fab equipping, technology levels, and products.

The SEMI Worldwide Semiconductor Equipment Market Subscription (WWSEMS) data tracks only new equipment for fabs and test and assembly and packaging houses. The SEMI World Fab Forecast and its related Fab Database reports track any equipment needed to ramp fabs, upgrade technology nodes, and expand or change wafer size, including new equipment, used equipment, or in-house equipment. ◆

Synopsys, STMicroelectronics and Samsung to collaborate on adoption of 28nm FD-SOI

Synopsys extended its collaboration with STMicroelectronics to include Samsung Electronics, enabling broader market adoption of ST's 28nm FD-SOI technology for SoC design. This collaboration extends the Galaxy design flow to Samsung in support of their strategic agreement to offer dual sourcing of ST's 28nm FD-SOI technology. Developed over a multiyear collaboration with ST, the design flow enables concurrent area, power and timing optimizations to enable engineers to optimize their designs for the ST 28nm FD-SOI process.

"The close collaboration between ST design teams and Synopsys led to advanced silicon-proven design enablement solutions that fully leverage the performance and power promise of FD-SOI technology and provide the foundation needed to meet tight time to market windows," said Philippe Magarshack, executive vice president, Design Enablement and Services, STMicroelectronics. "Our close collaboration with Synopsys has already enabled many successful tapeouts with mutual customers using Synopsys' Galaxy Design Platform and Lynx Design System."

The Synopsys design flow for ST's 28nm FD-SOI is compatible with the Lynx Design System, a full-chip design environment providing innovative automation and visualization capabilities that enable higher designer productivity and faster design closure. A technology plug-in using ST's 28nm FD-SOI Process Design Kit (PDK), standard cells and memories, adapts the production-proven Galaxy Design Platform-based RTL-to-GDSII flow for 28nm FD-SOI SoC designs, accelerating project setup and execution. Lynx automation simplifies and accelerates many critical implementation and validation tasks, including back-bias management across the flow, special connection checks, In-Design physical verification for well connections and UPF supply set management for N-wells and P-wells.

Faster electronic device architectures are in the offing with the unveiling of the world's first fully two-dimensional field-effect transistor (FET) by researchers with the Lawrence Berkeley National Laboratory (Berkeley Lab). Unlike conventional FETs made from silicon, these 2D FETs suffer no performance drop-off under high voltages

Ali Javey, a faculty scientist in Berkeley Lab's Materials Sciences Division and a UC Berkeley professor of electrical engineering and computer science, led this research in which 2D heterostructures were fabricated from layers of a transition metal dichalcogenide, hexagonal boron nitride and graphene stacked via van der Waals interactions.

"Our work represents an important stepping stone towards the realization of a new class of electronic devices in which interfaces based on van der Waals interactions rather than covalent bonding provide an unprecedented degree of control in material engineering and device exploration," Javey says. "The results demonstrate the promise of using an all-layered material system for future electronic applications."

Javey is the corresponding author of a paper describing this research in ACS Nano titled "Field-Effect Transistors Built from All

Two-Dimensional Material Components". Co-authors are Tania Roy, Mahmut Tosun, Jeong Seuk Kang, Angada Sachid, Sujay Desai, Mark Hettick and Chenming Hu.

FETs, so-called because an electrical signal sent through one electrode creates an electrical current throughout the device, are one of the pillars of the electronics industry, ubiquitous to computers, cell phones, tablets, pads and virtually every other widely used electronic device. All FETs are comprised of gate, source and drain electrodes connected by a channel through which a charge-carrier – either electrons or holes – flow. Mismatches between the crystal structure and atomic lattices of these individual components result in rough surfaces – often with dangling chemical bonds – that degrade charge-carrier mobility, especially at high electrical fields.

"In constructing our 2D FETs so that each component is made from layered materials with van der Waals interfaces, we provide a unique device structure in which the thickness of each component is well-defined without any surface roughness, not even at the atomic level," Javey says. "The van der Waals bonding of the interfaces and the use of a multi-step transfer process present a platform for making complex devices based on crystalline layers without the constraints of lattice parameters that often limit the growth and performance of conventional heterojunction materials."

Javey and his team fabricated their 2D FETs using the transition metal dichalcogenide molybdenum disulfide as the electron-carrying channel, hexagonal boron nitride as the gate insulator, and graphene as the source, drain and gate electrodes. All of these constituent materials are single crystals held together by van der Waals bonding.

For the 2D FETs produced in this study, mechanical exfoliation was used to create the layered components. In the future, Javey and his team will look into growing these heterogeneous layers directly on a substrate. They will also look to scale down the thickness of individual components to a monolayer and the lengths of the channels to molecular-scale dimensions.

Global semiconductor industry posts highest-ever first quarter sales

The Semiconductor Industry Association this month announced that worldwide sales of semiconductors reached $78.47 billion during the first quarter of 2014, marking the industry's highest-ever first quarter sales. Global sales reached $26.16 billion for the month of March 2014, an increase of 11.4 percent from March 2013 when sales were $23.48 billion and a slight uptick of 0.4 percent compared to last month's total of $26.04 billion. Regionally, sales in the Americas increased by 16.1 percent compared to last March, and year-to-year sales increased across all regions. All monthly sales numbers are compiled by the World Semiconductor Trade Statistics (WSTS) organization and represent a three-month moving average.

"The global semiconductor market has demonstrated consistent momentum in recent months, and sales are well ahead of last year's pace through the first quarter of 2014," said Brian Toohey, president and CEO, Semiconductor Industry Association. "Perhaps most impressively, sales in March increased across all regions and every semiconductor product category compared to last year, demonstrating the market's broad and diverse strength."

Regionally, year-to-year sales increased in the Americas (16.1 percent), Asia Pacific (12.9 percent), Europe (8 percent), and Japan (0.4 percent), marking the first time in more than three years that year-to-year sales increased across all regions. Sales were up compared to the previous month in Europe (3.9 percent), Asia Pacific (1.4 percent), and Japan (0.3 percent), but down slightly in the Americas (-4.3 percent).

"Although recent semiconductor sales are encouraging, one threat to the semiconductor market's continued growth and America's overall economic strength is the innovation deficit – the gap between needed and actual federal investments in research and higher education," Toohey continued. "Policymakers should act swiftly to close the innovation deficit by committing to robust and sustained investments in basic scientific research and higher education."

SEMI's 3DIC standards activities

Dr. Phil Garrou,
Contributing Editor

I have said many times that it will be impossible for a complicated technology like 3DIC to ever become commercial without standardization. SEMI has been working on this now for 3+ years. Let's take a look at their recent update from their SEMICON Singapore presentation.

So far, they have published the following standards:

SEMI 3D1-0912, Terminology for Through Silicon via Geometrical Metrology

– Clear and commonly accepted definitions are needed for efficient communication and to prevent misunderstanding between buyers and vendors of metrology equipment and manufacturing services.

– The purpose of this Document is to provide a consistent terminology for the understanding and discussion of metrology issues important to through silicon vias (TSV).

SEMI 3D2-1113, Specification for Glass Carrier Wafers for 3DS-IC

– This Specification describes dimensional, thermal, and wafer preparation characteristics for glass starting material that will be used as carrier wafers in a temporary bonded state;

– Methods of measurements suitable for determining the characteristics in the specifications indicated.

SEMI 3D3-0613, Guide for Multi-Wafer Transport and Storage Containers for 300 mm, Thin Silicon Wafers on Tape Frames

–Address the methods for shipping thin wafers on tape frames.

SEMI 3D4-0613, Guide for Metrology for Measuring Thickness, Total Thickness Variation (TTV), Bow, Warp/Sori, and Flatness of Bonded Wafer Stacks

– Control of bonded wafer stack (BWS) thickness, total thickness variation (TTV), bow, warp/sori, and flatness metrology, is essential to successful implementation of a wafer bonding process.

– This std provides a description of tools that can be used to determine these key parameters before, during, and after the process steps involved in wafer bonding.

SEMI 3D5-0314, Guide for Metrology Techniques to be used in Measurement of Geometrical Parameters of Through- Silicon Vias (TSVs) in 3DS-IC Structures

– This std assists in the selection and use of tools for performing measurements of geometrical parameters of an individual TSV (through-silicon via), or of an array of TSVs.

SEMI 3D6-0913, New Standard: Guide for CMP and Micro-bump Processes for Frontside Through Silicon Via (TSV) Integration

– This std provides a generic middle-end process flow to define acceptable TSV and CMP quality criteria as well as to develop methodology and measuring procedures for micro-bump.

SEMI 3D7-0913, New Standard: Guide for Alignment Mark for 3DS-IC Process

– Photo alignment mark configuration is the key to ensure consistent and precise alignment of layers, chips and wafers.

– This standard provides an alignment mark strategy for chip to chip, chip to wafer, and wafer to wafer stacking.

SEMI also has organized task forces in North America, Taiwan and Japan focused on various aspects of 3DIC manufacturing and testing. The North America task force is focused on:

Bonded Wafer Stacks – Create and/or modify specifications that reflect bonded wafer stacks parameters and the wafer bonding process.

Inspection & Metrology – Develop standards for metrology and inspection methods to be used for measuring TSV properties, bonded wafer stacks, and dies used in the 3DIC manufacturing process.

Thin Wafer Handling – Develop standards for reliable handling and shipping of thin wafers, dies (e.g., Micro-pillar Grid array -MPGA) used in 3DIC high-volume manufacturing (HVM). ◆

Packaging

Challenges of EUVL HVM

Vivek Bakshi,
EUV Litho, Inc.

Most of the papers at this year's EUVL Conference during SPIE's 2014 Advanced Lithography program focused on topics relating to EUVL's entrance into high volume manufacturing (HVM).

In their paper, GLOBALFOUNDRIES compared EUVL and ArF immersion scanners for 20/14nm metal lines and found equal yields for both lithography techniques. They did note an additional issue of EUV mask backside contamination, which I believe can be addressed. For 10/7nm metal lines, they believe they need to address issues of overlay, mask defects, integration and line width roughness (LWR) through focus, in order to bring EUVL into production.

Imec presented a preliminary cost of ownership (COO) study that concluded that at the 7 nm node, 75 wafers per hour (WPH) throughput will be needed for EUVL to show better COO than ArF immersion (ArFi) multiple patterning (MP). This throughput corresponds to 100 W of source power at the intermediate focus.

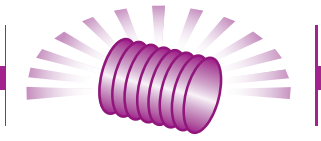
HVM-related metrics such as yield and availability (mean time to failure [MTTF], mean time to repair [MTTR], etc.) are now the focus. It was evident from the talk by TSMC, which reported ~10 W of power instead of the expected 30 W for their planned insertion of EUVL into the 10 nm node. A laser misalignment caused a source breakdown and a two-week unexpected downtime for the tool. Although some saw this as a setback, a brand new tool's first installation in the field can be expected to have glitches and downtime. TSMC reconfirmed their commitment to bring EUVL into HVM at the 10 nm node.

Mark Philips of Intel, in his talk, outlined the 1-D grating and cuts approach of Yan Borodovsky. EUVL is the preferred choice for cuts as EUVL offers advantages in terms of number of masks and edge placement error (EPE). Intel still plans to insert EUVL at the 7 nm node in 2017, but needs a mature COO for EUVL. It will be either mix and match with ArFi MP or EUVL alone, depending upon the cost drivers. As the mix and match approach faces the issue of overlay, he presented a detailed model, developed with Mike Hanna of ASML, that identifies the root cause of machine to machine overlay values and will help minimize it. Current machine to machine overlay (EUVL and ArFi) is 5 nm but needs to be 3.5 nm at 10 nm nodes and 3.0 nm at 7 nm node. My perception is that with the amount of effort going into it, those goals can be achieved.

Hynix, in their paper on EUVL development efforts, made a comment that self-aligned quadruple patterning (SAQP) has 5x more steps than EUVL and that many multiple patterning steps take away any benefit that one can expect from it, and hence are not beneficial.

ASML currently has three NXE 3300B, HVM level scanners being installed in the field, including one at TSMC. They reported 30 W power (down from 50 W reported in the lab last year) with 100 W planned for this year and 250 W for next year. We know that TSMC had only 10 W at the time of conference. With ASML acquiring Cymer, I expected a change in how data is presented, with more realistic roadmaps. I understand that to predict the readiness of source is very hard, as there are many new technologies that may do well in the lab with a dozen PhDs fine-tuning them, but aren't necessarily ready for the field where they have to perform 24 x 7 while being operated by technicians.

My personal opinion is that if we can get 50 W with decent availability in the field this year for 3300 B, it will be a great achievement. 100 W will follow over the coming years and I cannot predict yet when 250 W sources will be ready. With the data that I currently have seen, I will stick with my predictions.



Scaling to 5nm: A plethora of paths

DEBRA VOGLER, *SEMI, San Jose, CA*

Continued shrinks will require a mix of different approaches to lithography, device structures and 3D integration.

Previous semiconductor technology generations developed more clearly defined "winners" in terms of process technologies and materials choices. As the industry goes below 14nm, however, it appears that there will be multiple technologies used along the way. For lithography, that includes the further extension of 193i, plus the inclusion of EUVL, directed self-assembly (DSA), maskless lithography (ML2), and more. For transistor scaling, it could be some combination of nonplanar device structures and non-silicon materials (e.g., III-V), but it could also mean that, depending on the application, a company might want to choose a nontraditional scaling path such as 3D integration.

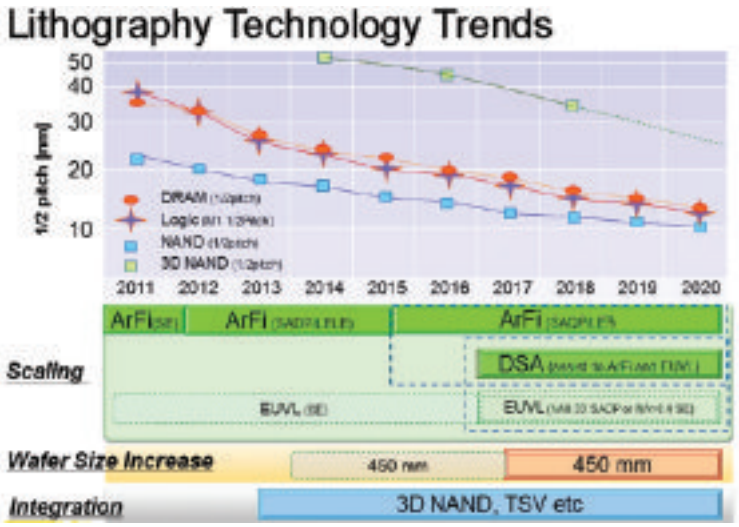


FIGURE 1. Lithography technology trends. Source: Nikon

Lithography: keeping all options open

Immersion lithography at 193nm is still very much alive — and while the industry works to ready EUVL for high-volume manufacturing (HVM), Nikon's position has been to maintain the 193 infrastructure and keep improving 193 tools to support multiple patterning and other technologies that are coming into play. "It was premature to declare 193i dead," according to Stephen Renwick, senior research scientist at Nikon Research Corporation of America. "It's still very much alive and a viable option as we go into 10nm and 7nm **(FIGURES 1, 2)**." As part of its immersion lithography extension pipeline, the company's model S622D is shipping now and is being used at 14nm, with end users looking to extend it to the 10nm logic node. "The S630D is coming soon and is intended to be used at 10nm and extended to the 7nm logic node," said Renwick, who will present at the "Readiness of Advanced Lithography Technologies for HVM" session (part of the new Semiconductor Technology Symposium) at SEMICON West 2014 (www.semiconwest.org).

One next-generation lithography (NGL) technology that Nikon has been evaluating is directed self-assembly (DSA). It is the scanners that make the guide patterns used to guide the block copolymers that self-assemble, so the company was interested in anticipating what might be needed in terms of additional performance requirements on 193 immersion scanners (e.g., overlay, CD uniformity) to make the guide patterns. Rathsack, et al., (Adv. Litho. 2012, Proc. SPIE, #8323) have achieved 12.5nm lines/spaces using 100nm guide patterns, which are approximately the 7nm node requirements. According to Renwick, to meet these DSA requirements at 7nm, a 193i scanner needs an overlay ≤2nm and single-digit CDU — requirements the company can fulfill. The company's S630D is already able to meet the requirements and the S622D is coming along, noted Renwick.

Also working to extend 193i lithography with complementary solutions such as DSA and maskless lithography (ML2) is CEA-Leti, with its IMAGINE (for ML2)

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and IDEAL (for DSA) programs. The IMAGINE Program is charged with developing and industrializing electron beam high-throughput maskless lithography developed by MAPPER Lithography. Members include: MAPPER, TSMC, STMicroelectronics, Nissan Chemical, TOK, JSR Micro, Sokudo, TEL, Mentor Graphics, and Aselta Nanographics. According to Serge Tedesco, lithography program manager at CEA-Leti, ML2 offers a production price reduction for low- and mid-volume applications. "This technique appears quite attractive for coping with the increasing difficulties relative to the patterning of critical levels, such as contact layers, and the cut level in the case of complementary lithography," Tedesco told SEMI.

At the present time, the IMAGINE program's pre-production Matrix 1.1 platform is making steady progress. The installation at Leti began in July 2013 and the first exposure is scheduled for June 2014. The Matrix 1.1 comprises 1300 x 49 beams to reach a throughput target of 1wph. The specifications on this pre-production platform are identical to the production version (i.e., 32nm L/S, 10nm overlay). To build up the infrastructure to support the platform, Leti has interfaced the tool with the Sokudo DUO track. Work is on-going with resist suppliers and the data base infrastructure for e-beam proximity correction (EPC) is being handled by Aselta — a Leti start-up. Additionally, Mentor Graphics and Mapper announced a partnership to support the Matrix data format.

The next phase of the pre-production IMAGINE program is getting the platform to 10wph (Matrix 10.1) using 13000 beams. The Matrix platform roadmap places the 10.1 phase starting at about Q4/14 and going until Q1/15. After that comes development of an HVM tool — the Matrix 10.10 — that will have 10 clustered 10wph/module modules for a throughput of 100wph **(FIGURE 3)**.

Regarding Leti's DSA activities, Tedesco reports that its IDEAL program is making progress on both the materials and process integration fronts. "Resolution, CD control and defectivity are in the range of what will be needed for implementation of the technology," said Tedesco. He added that the addition of partners such as TOK, ASML, and Mentor Graphics will ensure the infrastructure will be ready. Tedesco will also present at the "Readiness of Advanced Lithography Technologies for HVM" session.

Also on the DSA front, another European project called PLACYD was launched earlier this year by Arkema, Leti, and 9 other European partners. The project will set up a dedicated materials pilot line at Arkema (in Lacq, France) to supply block copolymers for DSA lithography. The objective is to provide such materials that are precisely defined, with high purity, and that are highly reproducible on an industrial scale.

Regarding ML2 and DSA, Tedesco is rather upbeat about the future. "Complementary and cost-effective

	Fin/Act	Gate	Metal	Via
193i 10nm	SADP+Cut SAQP+Cut DSA	SAQP+Cut LELE	SADP LELE	LELE DSA
193i 7nm	SAQP+Cut DSA	LELE+Cut SADP+Cut	SAQP DSA	LELELE DSA
EUV 7nm	SADP+Cut DSA	SE+Cut	SE+Cut DSA	SE DSA

FIGURE 2. Options for different nodes. Source: Nikon

solutions, such as DSA and ML2 could help extend 193i much further than originally anticipated," he said.

Scaling transistors: a matter of function

It may be less clear what will be sorted out for transistor scaling as the industry gets closer to the 5nm node. There are many choices that will need to be made just for materials, i.e., substrate, channel, and gate. Add in the different types of device architectures — FinFET, gate-all-around, and even unconventional choices such as tunnel FETs and nanowires — and you have a toss-up delimited by device application. An Chen, senior member of the technical staff

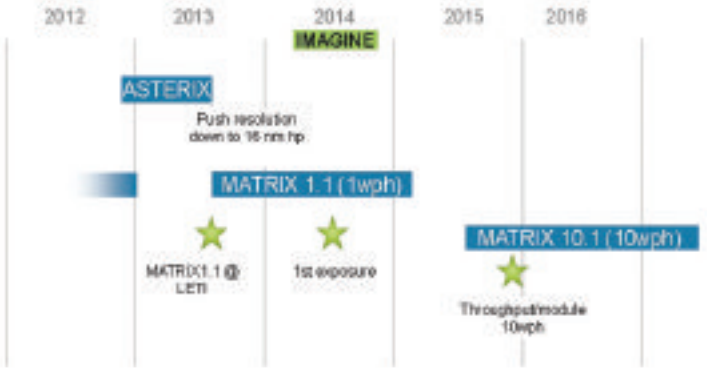

FIGURE 3. IMAGINE roadmap. Source: CEA-Leti

at GLOBALFOUNDRIES and Chair of the ITRS Emerging Research Devices Working Group, told SEMI that there is no consensus on the device/material choices. Will building a consensus even make sense? It seems unlikely. "Companies may run into different challenges and reach different conclusions on the same technology," said Chen. "The maturity level of technology development among different companies will also affect their opinions on technology options." Adding to the mix is the fact that different applications require different device characteristics, so a particular company's focus could affect its preferences on technology options, he observed. Chen will present at the "Getting to 5nm Devices: Evolutionary Scaling to Disruptive Scaling and Beyond" STS session at SEMICON West.

The plethora of directions and choices is not the only wrench in the works. "The increasing cost of R&D and decreasing return in the semiconductor industry do not appear to be sustainable," stated Chen. Still, he doesn't think that development will slow down because of funding challenges, though he does believe that fewer and fewer companies will be able to afford the high cost of R&D for scaling. Indeed, even some consortia are collaborating with each other and more companies may start looking for alternatives, he observed. "There is a lot of research on beyond-CMOS technologies, but they seem to be more suitable to augment CMOS rather than to replace CMOS. And low power has been a common feature of many beyond-CMOS devices, which could become increasingly useful because of applications driven more and more by portability and mobility." Chen further observed that functional diversification or enhancement — e.g., 3D integration — may enable better system functionalities without relying on scaling.

The term "functional diversification" has been used by ITRS participants when they started to look into the "More than Moore" (MtM) directions the industry could take, explained Chen. "Instead of being driven by scaling (or nodes), MtM focuses more on functionalities that may be enabled by technologies beyond digital computing," said Chen. Examples of such functionalities are analog, sensing, and energy harvesting.

Regarding funding sources and possible disruptive technologies, Chen noted that a few years ago, the industry was talking about what technology can be found to extend scaling substantially beyond extreme CMOS. Research funded by programs such as DARPA, SRC, etc., might not be the most appropriate uses for such technologies. "Many of them may be better used — together with a CMOS platform — to create new functions or improve efficiency," said Chen. But such programs might not necessarily help with physical scaling.

Hear from the experts — live! This year, SEMI announced the new Semiconductor Technology Symposium (STS), to be held July 8-10 as part of the SEMICON West 2014 technical and business program agenda. The new paid program addresses the most important and critical issues facing the future of semiconductor manufacturing in a new and more technical conference format. More information and pricing for the STS sessions is available at www.semiconwest.org/sts.

Learn more about the new Semiconductor Technology Symposium sessions and other front-end programs at SEMICON West 2014 (www.semiconwest.org). Free registration for SEMICON West is available — includes free access to the exhibition hall plus all TechXPOT sessions, keynotes and executive panels. Register for SEMICON West 2014: www.semiconwest.org/register.

Wafer-level packaging of ICs for mobile systems of the future

ED KORCZYNSKI, *Senior Technical Editor*

Wafer-level packaging continues to gain slow IC market share, and novel fan-out redistribution drives the need for improvements in existing packaging materials within tight cost and reliability constraints.

The most functionality at the least cost is the promise of wafer-level packaging (WLP) when dealing with complex integrated circuits (IC) with a high number of input/output connections to the outside world. Integration of heterogeneous circuit functions -- such as micro- and graphics-processing, field-programmable gate array (FPGA) logic, dynamic and static memory, radio-frequency (RF) and analog, and sensing and actuating --may also be needed at the package-level to be able to deliver complete systems **(FIGURE 1)**.

In particular, electronic systems for high-growth mobile applications require low-power and low-volume per element which dis-allows circuit integration at the printed-circuit board (PCB) level. Instead, heterogeneous integration must occur as either a system-in-package (SIP) or a system on-chip (SOC). Dr. Eric Mounier of Yole Dévelopement, presented at the recent European 3D TSV Summit 2014 held in Grenoble, and showed Yole forecasts that total world-wide semiconductor IC wafers packaged at the wafer-scale will be 19% this year, raising to 20% in 2015.

One way of looking at the history of the IC industry is to examine the dynamic between SIP and SOC approaches. New functionalities tend to be first integrated into hardware as dedicated additional chips, to be connected in to the rest of the system as part of a PCB or SIP. Since different functionalities often require different fab processes, it is generally less expensive at the chip-level to divide functionalities into different chips, but then the packaging costs tend to be higher. Relatively low-volume parts may be most economically delivered as SIP, while higher-volume parts can often justify the additional design and test expenses of delivering the same functionality as a single SOC.

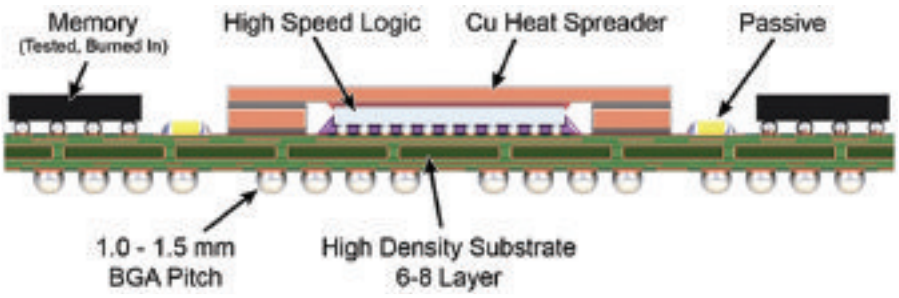

FIGURE 1. Heterogeneous System-in-Package (SiP) as an extension of proven flip-chip (FC) packaging technology. (Source: Amkor)

The other major reason to go with an SIP is to improve the yield of large area chips at the leading edge of fab processing. Since defects/area tend to be relatively high with a new fab process, very large chip designs will have relatively low yield at first but then will improve as the fab learns how to reduce both random and systematic yield limiters. The recent

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excellent example of this trend is the Xilinx Vertex-7 FPGA which splits the chip into four sub-chips and then uses a silicon interposer for SIP re-integration. We may expect that a next-generation of the

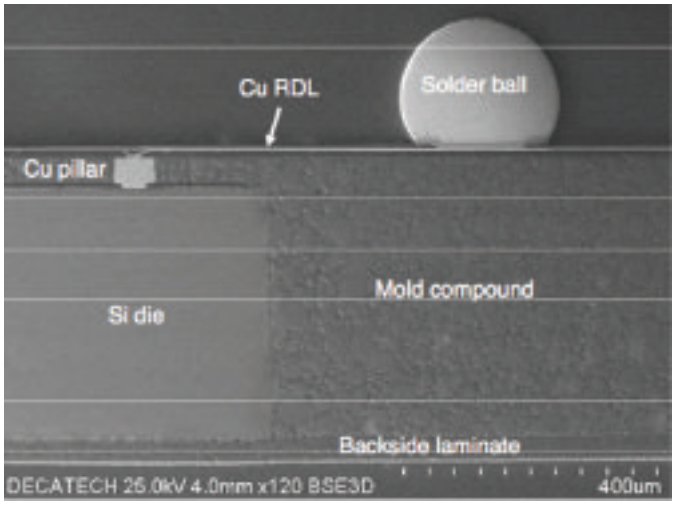

FIGURE 2. Cross-section of edge of FO-WLP using Cu-pillars and over-mold approach. (Source: Deca Technologies)

product would be built in a single SOC after the yield improves, at which point Xilinx would be expected to extend the product line with additional functionality added in using multi-chip SIP.

Fan-Out WLP

Steffen Kroehnert, director of technology for Nanium S.A., gave a recent presentation at SEMICON/Singapore 2014 titled "Wafer Level Fan-Out as Fine-Pitch Interposer." Fan-In WLP uses layout package connections within the chip area, and when the scale and count of on-chip bond pads does not match with standard packaging scales, a Re-Distribution Layer (RDL) of metal interconnect can be used to Fan-In to ball-grid or pillar-grid arrays (BGA/PGA) within the chip-area. However, when the needed number of connections cannot be made within the chip area, packaging filler materials can be used to provide physical area adjacent to an original chip such that package connections can be arranged to Fan-Out WLP solutions use "Fan-Out" out from the chip center when seen from above.

Chip-Package-Board simultaneous co-design and co-development are becoming important instead of serial work, according to Kroehnert. The penalty for re-design costs and losing strategic time-to-market for a new SiP is too high for allow for iterative R&D, such that products must be co-designed properly the first time.

FO-WLP leveraging PV fab tricks

Deca Technologies, the electronic interconnect solutions provider to the semiconductor industry owned by Cypress Semiconductor, recently announced that it has shipped its 100-millionth component. The company attributes this milestone to strong demand from portable electronics manufacturers for wafer-level chip scale packages (WLCSP) manufactured using Deca's unique, integrated Autoline production platform, which is designed to achieve faster time-to-market at lower cost.

Leveraging volume production technologies from leading silicon PV manufacturer SunPower Corp., Deca quickly achieved this milestone by addressing cycle time and capital cost challenges that semiconductor device manufacturers have struggled with using conventional approaches to WLCSP manufacturing. Deca claims that other FO-WLP technologies suffer from inherent manufacturing and reliability issues due to discontinuity at the silicon:mold-compound interface, which are avoided by the company's use of copper-pillars and an over-mold approach **(FIGURE 2)**.

Demand for WLCSP is being driven by manufacturers of wireless connectivity, audio, and power management components for mobile markets. Demand fluctuations in these markets can lead to challenges in managing inventories. "Congratulations to the Deca team on achieving this significant milestone," said Brent Wilson, senior vice president of the Global Supply Chain Organization at ON Semiconductor. "Deca's innovative technologies and focus on customer service have made the company a valuable part of our supply chain."

"Reaching 100 million units is an important milestone for Deca because it validates our unique approach to WLCSP manufacturing," said Chris Seams, CEO of Deca Technologies. "Based on the demand forecasted by our customers, we anticipate passing the half-billion mark in unit shipments this year."

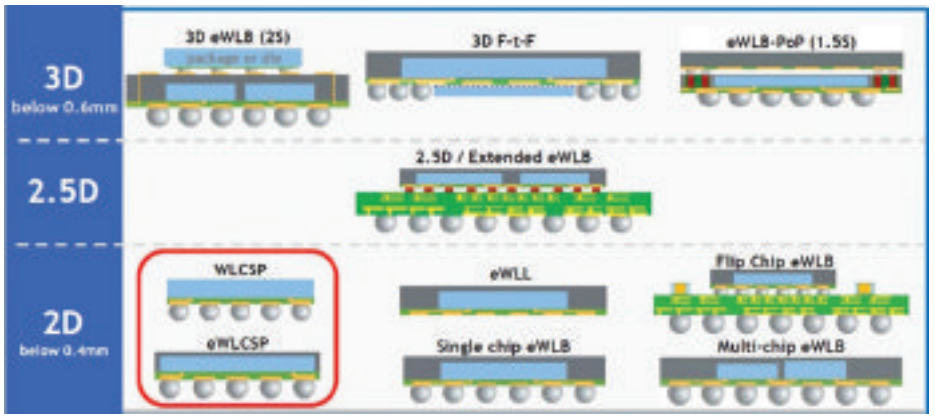

FIGURE 3. Schematic cross-sections of various Fan-Out WLP packages. (Source: STATSChipPAC).

FO-WLP for the future

STATSChipPAC (SCP) recently announced FlexLine™ FO-WLP. The FlexLine flow dices and reconstitutes incoming wafers of various sizes to a standard size, which results in wafer level packaging equipment becoming independent of incoming silicon wafer size. The SCP FlexLine process flow is based on the SCP commercial eWLB FO-WLP process **(FIGURE 3)**. Single and multi-die fan-out package solutions have been in high-volume manufacturing since 2009 with more than a half-billion units shipped.

Earlier this year, Digitimes provided a brief English translation of some Chinese-language Economic Daily News (EDN) saying that Taiwan Semiconductor Manufacturing Company (TSMC) plans to increase IC packaging revenues to US$1 billion in 2015 and to US$2 billion in 2016. TSMC co-CEO C.C. Wei reportedly acknowledged that the production cost for silicon-substrate SIP (TSMC's variant termed "chip-on-wafer-on-substrate" or "CoWoS") packages is relatively high, and so the world's leading IC foundry intends to invest in FO-WLP technologies to be able to offer advanced packaging at a reduced price.

Wafer-level packaging continues to gain slow IC market share, and novel fan-out redistribution drives the need for improvements in existing packaging materials within tight cost and reliability constraints. With silicon-interposers and copper-interconnects part of WLP technology, the lines between chip and package have never been less clear. Managing all of this complexity is business as usual when designing mobile systems of the future.

450mm transition toward sustainability: Facility and infrastructure requirements

ADRIAN MAYNES *and* **FRANK ROBERTSON,** *G450C, Albany, NY.*

Design and construction professionals are showing unprecedented levels of collaboration through the G450C.

Hard data and strong collaboration are proving effective in solving the challenges inherent in building 450mm semiconductor fabs. In the past year, the Facilities 450mm Consortium (F450C) -- the facilities-focused off-shoot of the Global 450mm Consortium — has provided the unified forum to test and analyze utility requirements, overhead conveyance systems and energy-efficiency strategies. The Global 450mm Consortium (G450C), a New York-based public/private program with leadership from GLOBALFOUNDRIES, IBM, Intel, Samsung, TSMC and the College of Nanoscale Science and Engineering is housed on SUNY's University at Albany campus and maintains focus on 450mm process and equipment development **(FIGURE 1)**. Combined, preliminary results from these consortia are building the framework for this next-generation fab.

The F450C came into existence in 2013 facing a series of significant technical hurdles.

The purpose of the 450mm fab is to manufacture more advanced integrated circuits at lower cost with a lighter environmental footprint. However, the initial 450mm tool guidelines point to a greater cost per square foot (meter) of cleanroom space, much heavier structural loads and significantly larger tool sizes, which can detract from the manufacturing flexibility the industry seeks. The potential for competing visions among industry leaders and the cyclicality of semiconductor demand in the marketplace add head winds on the path toward widespread 450mm adoption. These factors pose challenges that will need to be managed to ensure 450mm program objectives are achieved.

- All key players are coming together
- CNSE is providing a uniquely neutral and technologically advanced home for critical research
- Work of the F450C is being guided by a strict application of an inside-out design approach
- Key advances have been made in utility requirements, overhead conveyance systems and energy-efficiency strategies

Data are pointing to promising advantages of the 450mm model, which may support broad industry adoption

A collaborative approach

When the complexity of the semiconductor manufacturing process adds the scale of a 450mm wafer, the facility requirements can seem immense. The current scale of today's 300mm factories indicates that managing the size and complexity is key to attaining the efficiencies needed for 450mm adoption. Driving to GLOBALFOUNDRIES' massive facility in upstate New York, for example, feels more like approaching a coliseum than a manufacturing fab **(FIGURE 2)**.

Naturally, the industry is closely examining impacts

ADRIAN MAYNES *was appointed as the M+W U.S., Inc. Program Manager for the Facility 450mm Consortium (F450C) in August of 2013.* **FRANK ROBERTSON** *is an Intel Corporation assignee to G450C.*

to the facility infrastructure along with the increase in wafer size, since merely scaling the manufacturing process is not practical. The size of the 450mm fab and its associated utility consumption projections would exceed affordability and exacerbate sustainability concerns without close focus on potential efficiencies.

The facility experts involved in establishing and implementing 450mm infrastructure requirements are facing a similar degree of challenges as the integrated circuit and equipment manufacturers.

Design and construction professionals are showing unprecedented levels of collaboration through the G450C to deconstruct semiconductor facility matter associated with 450mm adoption. This consortium formed in the summer of 2013 to unite collective industry expertise to tackle pressing 450mm facility and infrastructure issues. With a special focus on safety, cost, schedule, sustainability and environmental footprint, this group aims to: reduce production cost; increase manufacturing productivity; and reduce the environmental load associated with each chip manufactured.

FIGURE 1. The College of Nanoscale Science and Engineering NanoFab Xtension, which houses 25,000 ft2 of cleanroom for 450mm research and development. Source: CNSE.)

Everything starts at the process level

Early development of 450mm silicon and infrastructure began before the turn of the decade, yet it wasn't until 2013 that 450mm and 300mm process tools began to progress synchronously through technology development at CNSE. The function, operation and shape of a semiconductor facility are driven by the process technology and its corresponding manufacturing requirements. Design progresses from the inside out, starting with the process, in this sequence:

1. Process: the early development of silicon and infrastructure defines the utility process requirements
2. Equipment & Automation: process requirements dictate the process equipment/tools
3. Production Environment: process equipment defines the manufacturing environment and critical process systems (power,

FIGURE 2. GlobalFoundries Fab8.1 located in Malta, NY.

water, vacuum, chemicals and gases)

4. Site Infrastructure: the facility and its corresponding site requirements are developed

Equipment suppliers have begun providing tools so that G450C can create a 450mm baseline. Industry guidance is for some 450mm tools to maintain 300mm footprint normalized to throughput. Through working with original equipment manufacturers (OEMs) and suppliers, it becomes clear that some tools required to manufacture wafers are bigger and many components are heavier than their 300mm counterparts. This led members of Semiconductor Equipment and Materials International (SEMI) to prioritize the topic of "cranes and hoists" in a survey of potential 450mm standardization focus areas in late 2012. Members of the G450C agreed that industry alignment was needed to deal with the handling of components for 450mm equipment that might be larger and heavier than those currently lifted manually.

In March 2014, a multifaceted work group consisting of IC makers, OEMs, and facility systems suppliers published an initial set of component lifting systems for 450mm fab equipment. The Component Lift working group addressed a number of IC maker concerns around interference with overhead track automation systems, ceiling loading and fab layout flexibility. This led to almost immediate determination that ceiling-mounted cranes generally would not work for wafer fabs. Three broad classes of component lifting were then identified:

1. Generally light-duty custom fixtures integrated with and often mounted on the tools for specific component handling operations
2. Aisle-based mobile lift mechanisms operating from the periphery of the tools, capable of multiple configurations for somewhat heavier payloads
3. Gantry-like structures addressing the full span of large (e.g., cluster) tools, capable of heavy lifting and conveying payloads beyond the tool periphery

In a 10-month span, the Component Lift working group published a cost of ownership model, safety imperatives, productivity suggestions and other key considerations in their March 2014 guidelines. While more work awaits, this effort is indicative of a new era in which industry collaboration lays the foundation for 450mm success.

Correctly sizing utilities

Vital to the 450mm program's success is the ability to create an efficient manufacturing facility that builds upon industry know-how and lessons learned from prior technologies. Yesterday's approach of examining singular utility systems and then searching for ways to improve their individual efficiency is not sufficient. Facility designers must consider how process equipment and facility systems interact as a whole.

In the fall of 2013, the F450C conducted a survey with all aforementioned 450mm consortium member companies to build a roadmap based on the industry's priority focus areas. A plurality of polled members identified 450mm factory utility right-sizing as the top priority for the F450C. Simply stated, we want smarter utility consumption data to enable more efficient 450mm factories, not singular systems, but as a whole factory.

A "utility right-sizing" focus group was created and has been working since the fall of 2013 to characterize true 450mm utility consumption and requirements. Using the inside-out design process, the first step is to conduct real-time measurements for all critical 450mm process tools.

A critical step in the semiconductor manufacturing process is that of wet process, in which liquid chemicals remove materials from a wafer. This step is well known for its high usage of power, water, drains and chemicals. The G450C and F450C members are installing a series of monitoring devices on CNSE's first 450mm wet process tool.

Haws Corporation, a F450C member company, has donated a series of effluent monitoring systems

that enable utility characterization for acid waste neutralization drains, HF drains and exhaust. By characterizing drain effluents, the industry can more intelligently identify opportunities for reuse, reclaim and recycling. M+W Group, CH2M Hill and the G450C are collaborating to install power and flow meters on this same tool. In the second quarter of 2014, the group will conduct real-time utility measurements at idle, operational and peak modes, and combine the data with 300mm benchmarks to assemble the most comprehensive factory utility model in the history of our industry.

To illustrate why this initiative is a priority, consider that a 10 percent decrease in process equipment power consumption would reduce facility construction capex by ~2 percent. For a $1 billion dollar fab, this equates to an impact of approximately $20 million. A 10 percent decrease in process equipment ultra-pure water (UPW) consumption would reduce UPW system cost by approximately 7 percent and facility construction CAPEX by 0.3 percent.

Wet process is the start. This monitoring methodology will be repeated for all critical tool sets within the 450mm process in the coming years.

Just the beginning

Designing a safe way to install and work on 450mm process tools, combined with measuring and characterizing utilities, are two vital priorities for improving facility sustainability and efficiency. But it is just the beginning.

Edwards Vacuum, an original member of the F450C, is also providing its expertise to advance a "Green Mode" project, focusing on resource reduction and energy savings. About half of the process tools in a semiconductor facility use vacuum pumps and abatement systems to treat exhaust gases. The abatement systems were designed to run at full process capacity, even when the tool is not processing wafers. These "sub-fab" systems have significant impact on utility usage (power, process cooling water, acid wastewater treatment and nitrogen). Putting sub-fab systems into idle or green mode when there are no wafers processed can represent substantial reductions in operating and infrastructure costs. The Green Mode project is a multi-equipment supplier collaboration with the following goals:

1. Identify the impacts of vacuum operation changes at the process chamber, i.e., Green Mode
2. Consider other monitoring parameters that could provide information on vacuum system "health" and performance
3. Collect data to better understand correlation between process conditions and vacuum performance

Tool-Related Fab Design Guidelines – Change from 300 mm to 450 mm Technology	
Individual Equipment Footprint	+ 20 to 40%
Specific Utility Consumption per m² of cleanroom (*)	+ 0 to 20%
Cleanroom Height	No increase
Roof Truss Load (**)	May increase
Waffle Table Floor Load Capability (***)	+ 20 to 30%
Waffle Table Stiffness (***)	May increase
Vibration Classification	No Change

TABLE 1.

(*) Increase is mainly driven by new processes and equipment technology, e.g. EUV, single wafer processing etc.
(**) Pending AMHS concept and preference for floor mounted or ceiling suspended maintenance cranes
(***) Mainly driven by simultaneous introduction of new lithography technology, not by wafer size transition
Source: M+W Group, 2013

Results from this project will drive SEMI standards that minimize process risk while adding to utility consumption savings.

From suppliers to scientists, the path to realizing 450mm affordability will continue to require unparalleled industry collaboration. In addition to the facility and infrastructure challenges featured in this article, leaders of the semiconductor industry continue to prioritize roadmap items that will further reduce capex for future 450mm fabs.

The G450C and F450C are also working with global airborne molecular contamination organizations and forums to examine how facility-related design (automated material handling system/stocker evaluation, parts-cleaning design, etc.) can reduce defectivity and improve product yield.

And as the roadmap for 450mm is further defined, there will be more facility and infrastructure projects to come.

The G450C and F450C will continue to coordinate globally to ensure a cost-effective facility transition from 300mm to 450mm. In uncertain economic times, it is electrifying to witness unparalleled collaboration where companies that normally compete in the free market have joined together to deliver a safe, cost-efficient and sustainable fab of the future.

Scouting report for materials at the end of the road: 2013 ITRS

ED KORCZYNSKI, *Senior Technical Editor*

When pavement ends the terrain gets rough, as documented in the Emerging Research Materials chapter of newest ITRS.

The IC fabrication industry is approaching the end of the road for device miniaturization, with both atomic and economic limits looming on the horizon. New materials are widely considered as key to the future of profitable innovation in ICs, so everyone from process engineers to business pundits needs to examine the Emerging Research Materials (ERM) chapter of the just published 2013 edition of the International Technology Roadmap for Semiconductors (ITRS).

The 2013 ITRS covers both near-term (2014-2020) and long-term (2020 onward) perspectives on what materials and processes would be desired to build ideal ICs (**FIGURE 1,** Table ERM15). However, to properly understand the information in the current edition we need to consider the changes in the IC fab industry since 1992 when the first edition of the ITRS's predecessor was published as the U.S. National Technology Roadmap for Semiconductors (NTRS).

Twenty-two years ago, the industry had dozens of fabs working on next-generation technology, and with lithographic scaling dominating innovation there was broad consensus on gradual materials evolutions. Today, the industry has 3 logic fabs and about as many memory lines pushing processes to smaller geometries, and each fab may use significantly different revolutionary materials. The result today is that there is little consensus on direction for new materials, and at best we can quantify the relative benefits of choosing one or another of the many options available.

In fact, with just a few players left in the game, there is much to lose for any one player to disclose strategic plans such as the use of revolutionary materials. Mark Thirsk, managing partner with

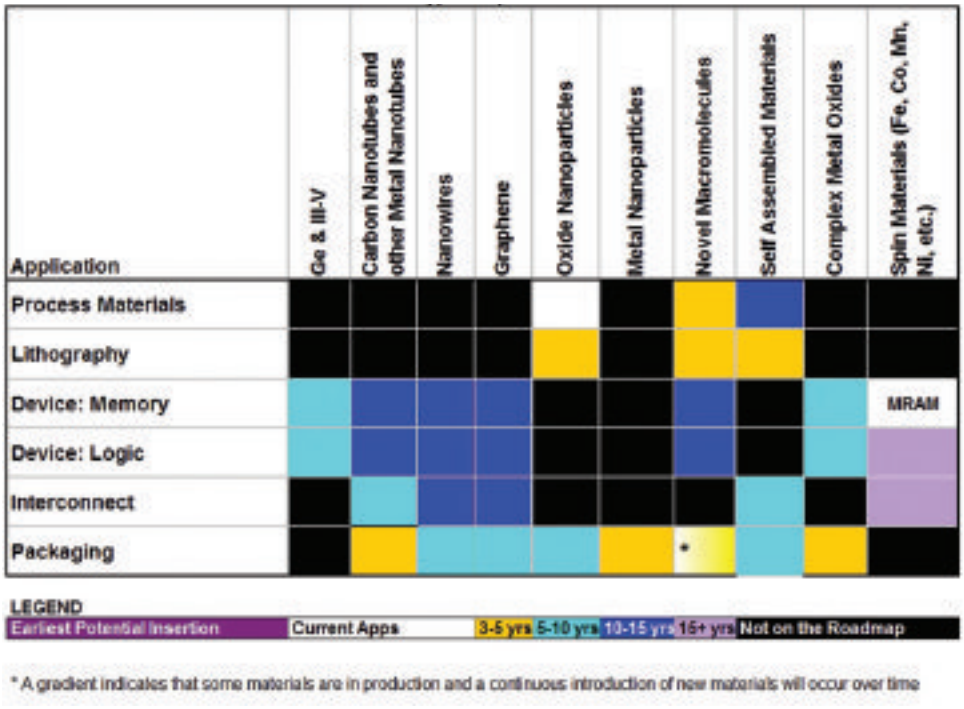

FIGURE 1. Opportunities for earliest potential insertion of emerging research materials.

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specialty materials analysts Linx Consulting, commented, "We built our business based on anonymizing and generalizing the world, and then predicting the future based on big categorical buckets. But now there are a very few number of people pushing the boundaries and we're being asked to model specific fab processes such as those for Intel or TSMC."

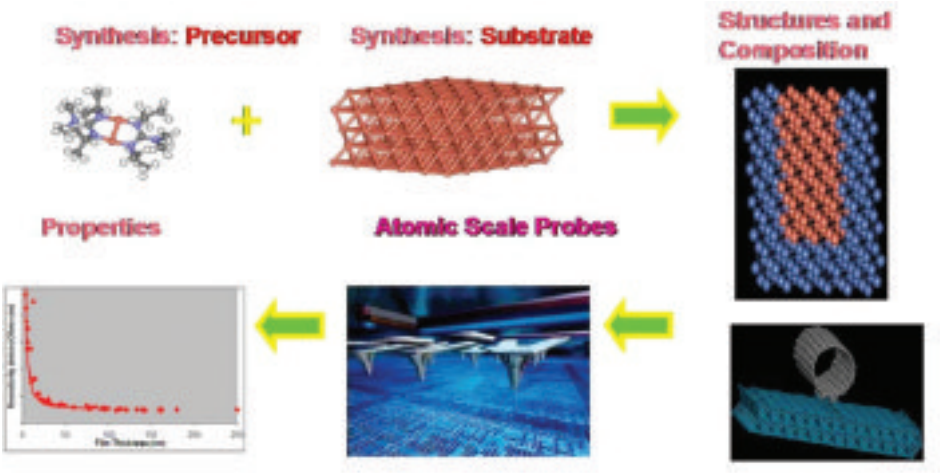

FIGURE 2. The stages of developing a new chemical precursor for use in commercial IC production.

For all of the above reasons, the current ITRS might be better understood as a scouting report that quantifies the roughness of the terrain when our current roads end. Exotic materials such as graphene and indium-gallium-phosphide may be used as alternate materials for the Si channels in transistors, novel stacks of atomic-layers may be used as electrical contacts, and spintronics and single-electron devices may one day replace DRAM and Flash chips for solid-state memory chips. However, "significant challenges" exist in integrating any of these new technologies into high-volume manufacturing.

In the near-term, Cu wires clad with various metal barriers are projected to provide the best overall performance for on-chip interconnects. As stated in the 2013 Executive Summary, "Unfortunately no new breakthroughs are reported for interconnections since no viable materials with resistivity below copper exist. However, progress in manipulation of edgeless wrapped materials (e.g., carbon nanotubes, graphene combinations etc.) offer the promise of 'ballistic conductors,' which may emerge in the next decade."

Specialty materials suppliers

FIGURE 2 (Figure ERM5) shows the inherent complexity involved in the stages of developing a new chemical precursor for use in commercial IC production. The chapter summarizes the intrinsic difficulty of atomic-scale R&D for future chips as follows:

A critical ERM factor for improving emerging devices, interconnects, and package technologies is the ability to characterize and control embedded interface properties. As features approach the nanometer scale, fundamental thermodynamic stability considerations and fluctuations may limit the ability to fabricate materials with tight dimensional distributions and controlled useful material properties.

In addition to daunting technical issues with pre-cursor R&D, the business model for chemical suppliers is being strained by industry consolidation and by dimensional shrinks. Consolidation means that each fab has unique pre-cursor requirements, so there may be just one customer for a requested chemistry and no ability to get a return on the investment if the customer decides to use a different approach.

Shrinks down to atomic dimensions means that just milliliters instead of liters of chemistry may be needed. For example, atomic-layer deposition (ALD) precursor R&D requires expertise and investment in molecular- and chemical-engineering, and so significant sunk costs to create any specialty molecule in research quantities. "We'll have an explosion of precursors required based on proprietary IP held by different companies," reminds Thirsk. "The people who are being asked to develop the supply-chain of ever increasing specifications are simultaneously being squeezed on margin and volumes."

For materials such as Co, Ru, La, and Ti-alloys to be used in fabs we need to develop more than just deposition and metrology steps. We will also likely require atomic-level processes for cleaning and

etch/CMP, which can trigger a need for yet another custom material solution.

Established chemical suppliers -- such as Air Liquide, Dow, DuPont, Linde, Praxair, and SAFC -- run international businesses serving many industries. IC manufacturing is just a small portion of their businesses, and they can afford to simply walk-away from the industry if the ROI seems unattractive. "We're finding more and more that, for example in wet cleaning chemistry, the top line of the market is flat," cautioned Thirsk. "You can find some specialty chemistries that provide better profits, but the dynamics of the market are such that there's reduced volume and reduced profitability. So where will the innovation come from?"

Alternate channel materials

With finFETs and SOI now both capable of running in fully-depleted mode, alternative materials to strained silicon are being extensively explored to provide higher MOSFET performance at reduced power. Examples include III-V semiconductors, Ge, graphene, carbon nanotubes, and other semiconductor nanowires (NW). To achieve complimentary MOS high performance, co-integration of different materials (i.e. III-V and Ge) on Si may be necessary. Significant materials issues such as defect reduction, interface chemistry, metal contact resistivity, and process integration must be addressed before such improvements can be achieved.

Nano-wire transistors

Top down fabricated nanowires (NW) are one-dimensional structures that can be derived from two-dimensional finFETs. Patterned and etched <5nm Si NW have been reported to have room temperature quantum oscillatory behavior with back-gate voltage with a peak mobility approaching ~900 cm2/Vs. Despite extensive R&D, grown Si NW demonstrate no performance improvements over patterned-and-etched NW, and controlled growth in desired locations remains extraordinarily challenging. Overall, significant challenges must be overcome for NW to be integrated in high density, particularly when targeting laterally placed NW with surround gates and low resistance contacts.

Subatmospheric gas storage and delivery: Past, present and future

KARL OLANDER, PH.D., *and* **ANTHONY AVILA,** *ATMI, Inc., an Entegris company, Billerica, MA*

Storing gas on a sorbent provides an innovative, yet simple and lasting solution.

The period following the introduction of subatmospheric pressure gas storage and delivery was punctuated by continuous technical innovation. Even as the methodology became the standard for supplying ion implant dopants, it continued to rapidly evolve and improve. This article reflects on the milestones of the last 20 years and considers where this technology goes from here.

From the beginning, the semiconductor industry's concern over using highly toxic process gases was evident by the large investment being made in dedicated gas rooms, robust ventilation systems, scrubbers, gas containment protocols and toxic gas monitoring. While major advances have been made in the form of automated gas cabinets and valve manifold boxes, gas line components, improved cylinder valves and safety training, the underlying threat of a catastrophic gas release remained.

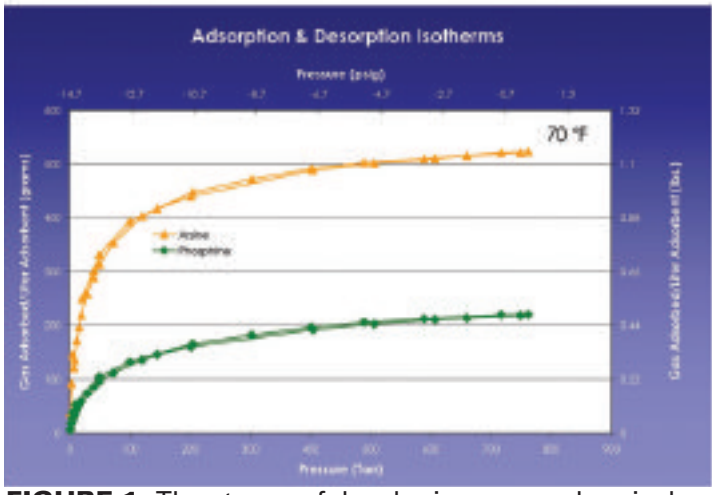

FIGURE 1. The stages of developing a new chemical precursor for use in commercial IC production.

Risk factors targeted

The underlying risk with compressed gases is twofold: high pressure, which provides the motive force to discharge the contents of a cylinder, and secondly, a relatively large hazardous production material inventory, which can be released during a containment breach. Pressure also is a factor in component failure and gas reactivity, e.g., corrosion. Mitigating these issues would considerably increase safety.

Analysis of the risks suggested an on-demand, point-of-use gas generator would improve safety by both reducing operating pressure and gas inventory[1]. The challenges associated with this approach include complexity of operation and gas purity, especially in a fab or process tool setting. Chemical generation of arsine, while possible, per equation [A], also substituted a highly reactive toxic solid for arsine[2]. Considerable safety and environmental issues accompanied the operation of such a generator. An on-demand, point-of-use electrochemical approach for supplying arsine, per equation [B], would also eliminate the need for high pressure storage if the associated operational issues could be overcome. Numerous attempts at developing a commercial electrochemical generator just never proved successful[3].

[A] $KAsH_2 + H_2O \rightarrow AsH_3/H_2O + KOH$

[B] $As(s) + 3H_2O + 3e(-) \rightarrow AsH_3(g) + 3OH(-)$

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Innovation from a simple(r) solution

Pressure swing adsorption processes utilize the selective affinity between gases and solid adsorbents, and are widely used to recover and purify a range of gases. Under optimal conditions, the gas adsorption process releases energy and produces a material that behaves mores like a solid than a gas.

Early work at reversibly adsorbing toxic materials on a highly porous substrate showed promise. In 1988, the Olin Corporation described an arsine storage and delivery system where the gas was [reversibly] adsorbed onto a zeolite, or microporous alumino-silicate, material[4]. A portion of the stored gas could be recovered by heating the storage vessel to develop sufficient arsine pressure to supply a process tool. In 1992, ATMI supplied a prototype system based on the Olin technology to the Naval Research Lab in Washington, D.C.

The breakthrough that lead to the first commercial subatmospheric pressure gas storage and delivery system occurred when ATMI reported the majority of the adsorbed gas could be supplied to the process by subjecting the storage vessel to a strong vacuum. Using vacuum rather than thermal energy simplified the process, providing the means for an on-demand system[5]. Using a sorbent had the effect of turning the gas into something more akin to a "solid." That characteristic, coupled with the absence of a pressure driver, delivered an inherently safe condition. The vacuum delivery condition also helped define where the technology would find its first application: ion implantation[6].

Safe and efficient gas storage and delivery

In 1993, prototype arsine storage and delivery cylinders based on vacuum delivery were beta tested at AT&T in Allentown, PA[g] [f]. The system was trademarked Safe Delivery Source®, or SDS®. Papers were presented on safe storage and delivery of ion implant dopant gases the following year in Catania, Sicily at the International Ion Implant Technology Conference[7].

The goal to find a safer method to offset the use of compressed gases was realized: (1) gas is stored at low pressure (ca. 650 Torr at 21°C) and (2) the potential for large and rapid gas loss is averted. Leaks, if they occur, whether by accidental valve opening or a containment breach, would be first inward into the cylinder. Once the pressure equalizes, gas loss to the environment would be governed mainly by diffusion as the gas molecules remain associated with the sorbent. The SDS package, while not a gas generator per se, effectively functions like one.

FIGURE 2. Cutaway view of SDS3 carbon pucks within a finished cylinder.

While subatmospheric pressure operation is an artifact of having to "pull the gas" away from the sorbent, it has become synonymous with safe gas delivery. The optimization work which followed focused on reducing pressure drop in the gas delivery system by improving conductance in valves, mass flow controllers and delivery lines. A restrictive flow orifice was no longer required. The new gas sources proved to work best when in close proximity to the tool.

The years after this technology introduction also saw considerable efforts to improve the sorbent; ultra-pure carbon replaced the zeolite-based material used in the first generation SDS (SDS1), roughly doubling the deliverable quantities of gas per cylinder. These granular carbon sorbents in the SDS2 were later replaced by solid, round monolithic carbon "pucks" in SDS3 **(FIGURE 2)**, which necessitated the cylinder be built around the sorbent[8]. This improvement again roughly doubled gas cylinder capacity.

Recognized in international standards

In 2012, the United Nations (U.N.) recognized the uniqueness of adsorbed gases and amended the Model Regulation for the Transport of Dangerous Goods by creating a new "condition of transport" for gases adsorbed on a solid and assigning a total of 17 new identification numbers and shipping names to the Dangerous Good List. Adoption is expected to occur by 2015. A few of the additions are noted here.

Arsine	UN 2188	compressed
Arsine, adsorbed	UN 3522	SDS
Phosphine	UN 2199	compressed
Phosphine, adsorbed	UN 3525	SDS

In recent years, fire codes have been updated through the definition and classification of subatmospheric Gas Systems, or SAGS, based on the internal [storage] pressure of the gas.9 Systems based on both sub-atmospheric pressure storage and delivery are designated as Type 1 SAGS. It is important to note that the UN definition for adsorbed gases, and the resulting new classifications mentioned above, only applies to Type 1 SAGS, defined as follows:

> **3.3.28.5.1 Subatmospheric Gas Storage and Delivery System (Type 1 SAGS).** A gas source package that stores and delivers gas at sub-atmospheric pressure and includes a container (e.g., gas cylinder and outlet valve) that stores and delivers gas at a pressure of less than 14.7 psia at NTP.

It is also worth mentioning that sub-atmospheric pressure gas delivery can also be achieved using high pressure cylinders by embedding a pressure reduction and control system. The Type 2 SAGS typically employs a normally closed, internal regulator[s] that requires a vacuum condition to open. This is not a definition of sub-atmospheric storage and delivery, but of sub-atmospheric delivery only.

> **3.3.28.5.2 Subatmospheric Gas Delivery System (Type 2 SAGS).** A gas source package that stores compressed gas and delivers gas subatmospherically and includes a container (e.g., gas cylinder and outlet valve) that stores gas at a pressure greater than 14.7 psia at NTP and delivers gas at a pressure of less than 14.7 psia at NTP.

In general, Environmental Safety and Health managers, risk underwriters and authorities having jurisdiction recognize the importance of SAGS and recommend their use whenever process conditions allow[10].

FIGURE 3. The evolution of a SAGS Type 1 gas package.

Expanding SAGS into new applications

Taking the lessons learned from SDS2/SDS3 in ion implant operations, along with key findings from other applications like HDP-CVD (the SAGE package) and combined with sorbent purification and carbon nanopore size tuning, SAGS Type 1 packages are poised

to offer their safety advantages in new and emerging areas, as well as add even more safety and efficiency benefits. Currently, a new package called Plasma Delivery Source™ (PDS™) is available for high flow rate applications, while maintaining all the safety attributes of the SAGS Type 1 package.

Also, in addition to the inherent safety, PDS employs a pneumatic operator (valve) to the cylinder which further minimizes the opportunity for human error. In an emergency, such as a toxic gas alarm, pressure excursion, loss of exhaust, etc., gas flow at the source can be quickly stopped and the cylinder isolated. Cycle/purge operations are made safer as human involvement is minimized. Human-initiated events, like over-torqueing the valve, failing to close the valve or even back-filling a cylinder with purge gas, are prevented.

	SDS1	SDS2	SDS3
Arsine	200	559	835
Phosphine	85	198	385

TABLE 1. Deliverable quantities in grams from a similarly sized JY cylinder when evacuated to a final pressure of 5 torr at NTP, illustrating the increased capacity enabled by each SDS package generation (Arsine and Phosphine shown as examples)

Expanding the use of SAGS beyond the domain of ion implant involves successfully navigating key process factors such as operating pressure, flow rates, proximity to the tool and purity. One approach includes coupling the PDS cylinder and gas cabinet together to yield a plug and play "smart" delivery system. Unlike high pressure systems, which are more concerned with excess flow situations, knowing and controlling pressure allows a SAGS cabinet to operate at a reduced risk. This enables linking cabinet ventilation rates with the system operating pressure. During normal operating conditions, the exhaust rate could be reduced by up to 80% because the system is operating subatmospherically. Should the operating pressure exceed a preset threshold, the exhaust flow would automatically revert to a higher range or the cylinder valve would close.

The future, therefore, could see these PDS packages extended to another level by incorporating them into smart delivery systems, which will further reduce risk, maximize efficiency, improve cost of ownership and expand the footprint for SAGS into new applications like plasma doping, solar, epitaxy and etch.

Summary

During the last 20 years, the semiconductor industry undertook a large effort to develop safer gas delivery technologies to reduce risks associated with dopants used in ion implant. Many technologies were considered, including chemical and electrochemical gas generators, complexing gases with ionic liquids or mechanically controlling cylinder discharge pressure using embedded regulator devices.

In the end, storing gas on a sorbent provided an innovative, yet simple and lasting solution. Gas-sorbent interactions are well understood, reproducible and can be achieved with a minimum of moving parts. Gas release risks, driven by pressure, are all but removed from consideration. And any potential for human error continues to be a target for improvement wherever toxic gases are used.

References

1. Proc. Natl. Acad. Sci. USA 89 pp 821-826, 1992.
2. Appl. Phys. Lett., 60 1483
3. Electron Transfer Technology, US Patent 59225232
4. Olin Corporation, US Patent US4744221A
5. Advanced Technology Materials, US Patent US5518528
6. Many thanks to Dan McKee and Lee Van Horn for being the first of many early adopters.
7. Proceedings of the Tenth International Conference on Ion Implantation Technology, 1994, pp 523-526.
8. DOT-SP 13220.
9. NFPA 318, Standard for the Protection of Semiconductor Fabrication Facilities 2012 Edition.
10. SAGS in the FAB, SST reference

HVM production and challenges of UHP PDMAT for ALD-TaN

LEIJUN HAO, RAVI K. LAXMAN *and* **SCOTT A. LANEMAN,** *Digital Specialty Chemicals, Toronto, Ontario, Canada.*

For sub-22nm device generations, device manufacturers are likely to adopt PDMAT precursor for ALD-TaN barrier films for copper interconnect structures.

At sub-micron device technology, copper is the interconnect metal of choice because of low resistivity, 1.7μΩ-cm, high current densities and excellent thermal conductivity. These characteristics of copper are increasingly important for supporting sub-22nm lines with high device density and speed. Deposition of copper lines can be achieved by a variety of techniques. A standard method generally involves physical vapor deposition (PVD) and electrochemical deposition (ECD). Because copper diffuses into silicon, silicon dioxide, and other low k dielectric materials, which can "poison" the device, Ta/TaN films are used as copper diffusion barriers. Copper integration schemes at sub-22nm use low-k dielectric PVD Ta/TaN barrier/ PVD copper seed/ ECD-Cu material stack [1].

Conventionally, tantalum nitride has been deposited by physical vapor deposition. As conformality becomes crucial for interconnect applications PVD or CVD processes are challenged to achieve aspect ratio of 5:1, due to directional limitations and form "pinch off" resulting in a void formation. When aspect ratio exceeds 5:1 a large amount of effort is focused in the formation of void and seam-free thin layers.

These difficulties with PVD and CVD motivate TaN-atomic layer deposition (ALD) process. At very tight geometries ALD is preferred over other techniques due to excellent conformality [2]. ALD of a tantalum nitride barrier layer involves sequentially pulses of pentakis(dimethyl-amino)tantalum (PDMAT), a tantalum nitrogen-containing precursor followed by reaction with ammonia to a process chamber. Deposition of ALD TaN films is also reported [3] using a mixed remote hydrogen (H_2) and ammonia (NH_3) plasma to reduce PDMAT at 275°C. As the (CD) features are scaled below 22nm BEOL, along with integration challenges, tight precursor composition and manufacturing of ultrahigh purity ALD precursors are desired for successful metallization.

ALD deposition for very thin conformal barrier films (<25 Å) could potentially reduce via resistance and does not impact electromigration of copper. Low via contact resistance at the contact area is also dependent on several factors such as trace impurities in the precursors, morphology of the barrier, deposition process, film nucleation and surface interface. In one study, a 10Å PEALD TaN reduced via resistance by 50% compared to the PVD TaN [3]. ALD growth rate also varies with the underlying layers, W < ULK< Cu. From a film property characterization point of view,

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FIGURE 1. Improved methods of purification have been used to produce microcrystalline pale yellow PDMAT with purity of >99.99995% (determined by trace metals and other spectroscopic methods) with extremely low chloride (<10ppm), low oxygen and total trace metals.

the density and resistivity of PEALD TaN film is about 11.6 g/cm^3 and ~2000 μΩ-cm. Ta-rich PVD TaN has a higher density of about 15.0 g/cm3 and a resistivity around 250 μΩ-cm. It was observed that density of thermal ALD TaN using PDMAT is ~90% of the density of PEALD TaN (thermal ALD TaN < PEALD TaN < PVD TaN). With appropriate precursor, ALD TaN also supports desired α-Ta and suppresses more resistive β-Ta nucleation [5].

At film thickness of 10-25Å trace metal impurities in the precursors play detrimental role in the density, resistivity and nucleation properties. Among the impurities tight control of oxygen concentration in the precursors and deposited films are extremely important. Especially, in the case of tantalum metal, being an electropositive metal it forms strong bonds with oxygen; the resulting "Ta-O" behaves as a capacitor in deposited films rather than a conductive barrier with low resistance. Hence low oxygen concentrations in precursor play an important role in ALD film properties.

The manufacturing of extremely high purity in high volume poses several challenges. PDMAT is extremely sensitivity to oxygen and water. For this and other reasons, the chemical synthesis of the PDMAT involves important sequence of purification technologies under inert conditions. We have developed novel purification methods and successful production of highly oxygen and moisture sensitive ALD precursor in High Volume Manufacturing (HVM). The yellow crystalline end product is shown in **FIGURE 1**, and **TABLE 1** lists common properties.

Table 1. Physical Properties

Color	Pale yellow crystalline
Molecular weight (g/mol)	401.3
Boiling point(°C)	>150-160(decomp)
Vapor Pressure (°C)	72~0.2torr
Sublimation Point (°C)	90@0.8mmHg
Density(g/cc)	1.2

Challenges in manufacture of PDMAT

PDMAT is synthesized in HVM by well-established metathesis reaction between $TaCl_5$ and $LiNMe_2$ as reported in the literature (equation 1).

$$TaCl_5 + 5LiNMe_2 \rightarrow 5LiCl + Ta(NMe_2)_5$$

PDMAT is relatively stable. However, high conversion to $Ta(NMe_2)_5$ presents several challenges because the reaction tends to give a mixture of $Ta(NMe_2)_5$, $TaCl(NMe_2)_4$, and $Ta_2(\mu\text{-}Cl)_2(NMe_2)_6Cl_2$ due to the equilibrium between them. Unfortunately, the use of large excess of $LiNMe_2$ causes the formation of $Me_2NCH_2N(H)Me$; this results in the formation of the byproduct $Ta(NMe_2)_4(\eta^2\text{-}MeNCH_2NMe_2)$. On the other hand, due to the abundant chloride ions available in the reaction solution, $Ta(NMe_2)_5$ can undergo chloride metathesis to produce byproducts such as $TaCl(NMe_2)_4$. Due to this complication of the by-products and the equilibrium between them, the isolated yield of PDMAT from TaCl5 and LiNMe2 is low at ~50%. Digital Specialty Chemicals has studied extensively the synthesis of PDMAT by metathesis between $TaCl_5$ and $LiNMe_2$. At optimized reaction conditions, in situ PDMAT yield, as high as 99% can be achieved. Typically, the crude PDMAT isolated from the reaction has a purity of 90-96%. Sublimation of the crude material under high vacuum gave orange crystalline solid with a purity of only 95-96% as determined by ^{1}H NMR

spectroscopy.

Isolation and purification of PDMAT presented another challenge because PDMAT is extremely sensitive to both air and trace oxygen. Organometallic precursor with low halide content is required because halides in the barrier layer may attack the copper layer and cause corrosion. PDMAT obtained by crystallization method usually contains high levels of chloride (>80ppm), lithium (>40ppm) and other metals. Although PDMAT has an adequate vapor pressure and can be sublimed, sublimation can only reduce chloride, lithium, and other impurities to a certain degree, because some of the impurities also co-sublime. Purification can be performed by a series of sequential steps and ultra-high purity PDMAT (>99.6% as determined by ^{1}H NMR spectroscopy, **FIGURE 2**) was achieved by following these processes in an in-house developed reactor. Our manufacturing processes produce micro crystalline pale yellow crystalline solid with purity of >99.99995% (determined by trace metals and other spectroscopic methods) with extremely low chloride (<10ppm), low oxygen and total trace metal analysis. Ultra high purified pentakis(dimethylamido) tantalum having less than about 10 ppm of chloride and extremely low oxygen content can be used as an effective barrier layer for copper. In our high volume production we have developed unique purification processes that allow production of highly crystalline material. Crystalline material is extremely useful in controlling the carryover of small amorphous particles through carrier gas stream. PDMAT is typically introduced as a vapor dissolved in a carrier gas by flowing a carrier gas through a canister containing solid precursor. The canister is heated uniformly to allow clean evaporation of precursor dissolved in the carrier gas (e.g. nitrogen, helium). Optical characterization of PDMAT vapor in an ALD pulse process was recently published [6], the low PDMAT partial pressure is due to low PDMAT vapor pressure and loss of heat of vaporization of the PDMAT powder, and also low carrier gas saturation. High carrier gas mass flow rates do not necessarily result in a higher mass transport of precursor. A microcrystalline PDMAT may help in better contact and resonance time for cleaner and less particulate delivery.

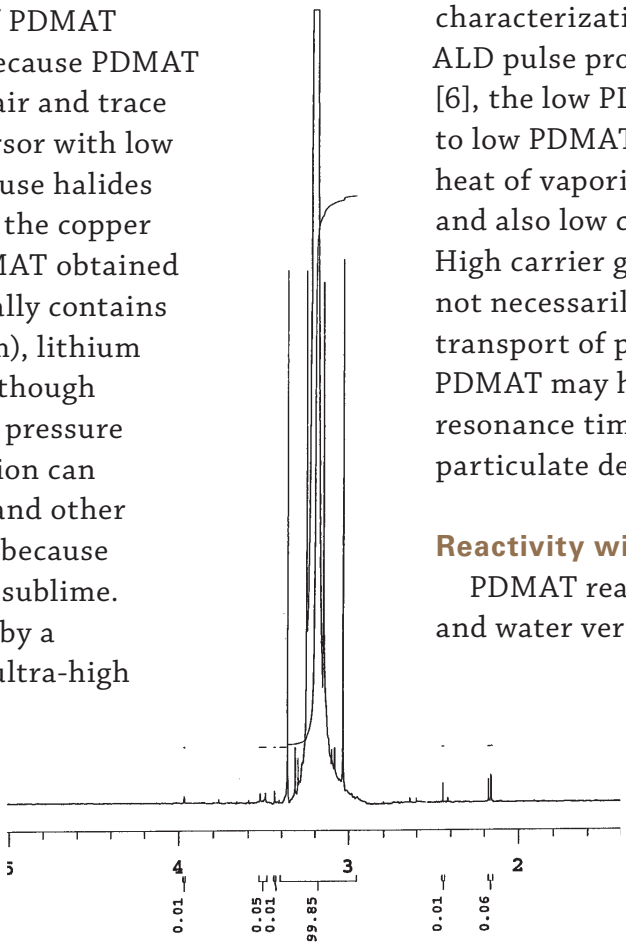


FIGURE 2. 400 MHz ^{1}HNMR (X10) spectroscopy indicates the ultra-high purity of the materials, <99.6%.

Reactivity with oxygen and moisture

PDMAT reacts with both oxygen and water very easily and is extremely sensitive to oxygen contamination. With moisture it results in several tantalum oxo amide compounds. In our high volume manufacturing we have observed that the tantalum oxo amide compounds are not easily removed from the PDMAT only by sublimation. Several of these tantalum oxo amide compounds sublime themselves and ultra-high purity PDMAT cannot be achieved. Moreover high volume sublimation systems are unavailable to handle extremely air and water sensitive organometallic chemistry. Chen et al. [4] in an excellent publication provided detailed X-ray structural and spectroscopic evidence that indicates formation of unusual oxo-amino complexes of PDMAT. They have also independently isolated and characterized these impurities by both 1H-NMR and X-ray structure determination.

Analysis of high purity PDMAT

Ultra High purity PDMAT is analyzed for trace metal impurities by ICPMS, ^{1}H NMR and 13C{1H} 400MHz NMR are used for organic and Ta-Oxo impurities characterization **(TABLE 2)**. The product

is further characterized by TGA (for residual %, <0.5%) indicating clean evaporation of the product. Analysis of trace amounts of oxygen content in highly purified PDMAT is very difficult but can be estimated at ppm level based on high resolution ^{1}HNMR spectroscopy and other techniques. Since Chen et al. have clearly identified each of the oxo-tantalum species in PDMAT, impurities in PDMAT that contain only tantalum-oxygen species can be identified. Typically a 400MHz ^{1}H NMR provides a good estimate on Ta-O content; these impurities species are well resolved from the product for accurate estimation. Alternatively, one can estimate the oxygen content by analysis of deposited tantalum nitride films by Auger, SIMS and other techniques.

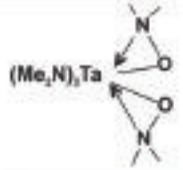
Tantalum-Oxo Impurities	Chemical Shift δ ppm (*C_6D_6,^{5}D_8Tol)
	*3.25, 2.47 impurity sublimes
	*3.41, 3.05, 2.94, 2.56 impurity sublimes
	*4.19, 3.51, 3.22, 2.39
	^{5}3.93-4.14, 3.71, 3.64, 3.60, 3.39, 3.32, 3.31, 3.17, 3.08, 2.31, 2.21, 2.12

TABLE 2. 400MHz ^{1}HNMR Chemical Shifts for major Tantalum-Oxo impurities.

Conclusions

At the sub-22nm device generation, device manufacturers are likely to adopt PDMAT precursor for ALD-TaN barrier films for copper interconnect structures. PDMAT is an extremely sensitive material and significant improvements have been made from the standpoint of synthesis, purification and consistent production of high purity of PDMAT (>99.99995%) in HVM.

References:

1. B. B. Burton, A. R. Lavoie and S. M. George, Journal of the Electrochemical Society, 155, 7, D508-D516 (2008)
2. Ville M, M. Leskelä, M. Ritala, and R. L. Puranen, Journal of Applied Physics 113, 21301 (2013)
3. J. Nag, A. Simon, Oscar V. Straten, A. Madan, P. DeHaven, L. Tai, J. C. Rowland, M.A. Zaitz, S. Molis, R. Murphy, F. Baumann, T. Bolom, J.Y. Lee, C. Niu, H.Kim, S. Krishna, X. Zhang, ALD Conference, 2013.
4. Shu-Jian Chen, Xin-Hao Zhang, Xianghua Yu, He Qiu, Glenn P. A., Yap, I. A. Guzei, Z. Lin, Yun-Dong Wu, and Zi-Ling Xue, J. Am. Chem. Soc. 129, 14408-14421, 2007
5. M. Stangl, A. Fletcher, J. Acker, H. Wendrock and K. Wetzigi, Journal of Electronic materials, Vol. 36, No. 12, 2007
6. J.E. Maslar, W.A. Kimes, B.A. Sperling, P.F. Ma, J. Anthis, J.R. Bakke, R. Kanjolia
ALD Conference, 2013.

Flexible glass firms branch into new applications

JUILA GOLDSTEIN, *Senior Associate Analyst, NanoMarkets, Glen Allen, VA*

Ultrathin glass is well suited for use as interposers in semiconductor packaging applications.

Flexible glass seemed like a natural fit for the display industry, combining the impermeability of glass with the flexibility of plastic. In 2012 it appeared as though flexible and ultrathin glass companies were going to benefit from the explosion of touch screens in displays of all sizes, but the market made an abrupt turnaround. Now suppliers of ultrathin and flexible glass are looking for applications beyond displays to bring in revenue in the next few years, and one of the places they are looking is in semiconductor packaging.

For those who approach flexible glass from the point of view of a display, an application where the glass is hidden between layers of silicon and other materials may not seem to make a lot of sense. As far as NanoMarkets can tell, no one really thought about semiconductor packaging as a use for flexible glass until the display application began to fail. The flexible glass sector itself was firmly focused on displays until then and the semiconductor packaging sector had probably never considered flexible glass as an option.

Nonetheless, using ultrathin glass in semiconductor packaging may actually be a very good idea, even though its optical properties and flexibility may be irrelevant in this application.

The Role of glass in interposers

For many years the semiconductor packaging industry has been developing packages that are smaller, thinner, and lighter than what has come before. Ultrathin glass, 30 to 100 µm, may be able to further progress toward this goal.

The target application is 2.5D or 3D multi-chip or chip scale packages (CSP), where semiconductor chips are placed in close proximity or stacked on top of each other to provide a space-saving configuration. Such packages traditionally use a layer of thinned silicon as an interposer to connect chips to each other and to the underlying organic substrate. Silicon has the advantage of being a familiar material with a well-established infrastructure in the semiconductor packaging industry, but it does have some drawbacks, the major one being cost.

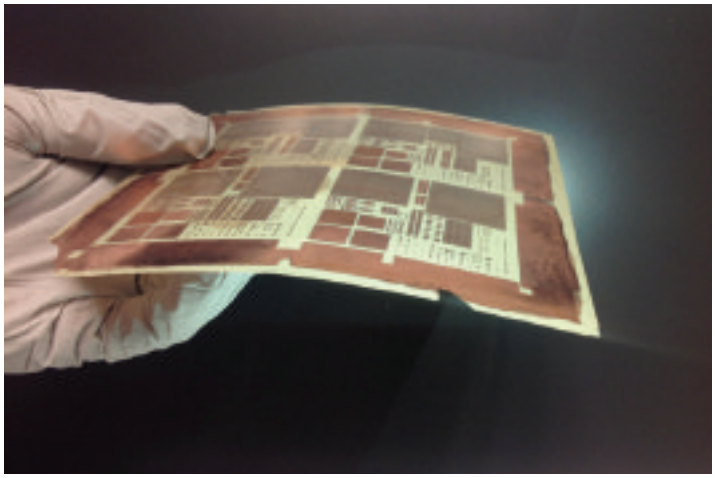


FIGURE 1. A 30 µm thick flexible glass interposer made by Schott Glass.

Glass may be preferable to silicon as an interposer because it is a less expensive material, it can be provided in thin sheets (silicon has to be ground and polished to the proper thickness) and it is thermally insulating. Silicon is a semiconductor, not an electrical insulator, which can cause problems with crosstalk between chips. FIGURE 1 shows a 30 µm thick flexible glass interposer made by Schott Glass.

Silicon conducts heat better than glass, making the semiconductor industry a bit suspicious of the ability of glass

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to conduct heat sufficiently to avoid hot spots in sensitive ICs. The answer is in the through-glass vias (TGV), channels drilled through the interposer that are filled with metal (usually copper) and form electrical connections between the chip and the organic substrate. Solid filled vias act like heat pipes to provide a path for heat conduction.

The potential cost advantages of glass can best be achieved using large sheets of glass, thus allowing facilities to process more units in parallel than is possible with silicon wafers. The largest possible cost savings of using flexible glass is realized if it can be integrated into a roll-to-roll production process. Several suppliers are producing flexible glass on rolls, but the semiconductor industry is not necessarily prepared to process it.

Re-evaluating the supply chain

While glass may be a compelling interposer material from the point of view of glass makers, lack of infrastructure in this application is a real problem. In order for glass to be useful as an interposer, someone needs to drill vias through the glass and metallize them, and it is not yet clear who that would be. Several industries could participate in the supply chain, but there are barriers in all cases:

- Semiconductor packaging houses: This industry is not used to working with glass and is not inclined to do so. It is very resistant to change and may be especially averse to implementing R2R processing. Convincing semiconductor packaging facilities to process glass will clearly be an uphill battle.
- Flat-panel display manufacturers: These companies have experience with glass but have not historically had anything to do with semiconductor packaging. It may be possible to build awareness in this sector, but the flat panel display industry prefers to sell large pieces of glass.
- Printed circuit board manufacturers: The PCB industry currently makes organic interposers, geared toward applications where fine pitch is not required. Glass suppliers might be able to work with the PCB industry, which is used to large panels, if they want to supply sheets of glass. It still may be difficult, however, to implement very thin glass using this approach. It also will probably be difficult to integrate TGV production into a PCB-like process flow.

Organizations that are promoting ultrathin glass interposers are attempting to address the infrastructure challenge:

- Georgia Tech: The Packaging Resource Center (PRC) at Georgia Tech has been working with industry partners on glass interposers since 2010 and has moved from initial trials with 180-μm thick glass down to the thinnest products that today's glass suppliers are producing. The PRC is working with major glass suppliers such as Corning and Schott, who are interested in flexible glass interposers.

The PRC has been working on transferring the technology from prototype to low volume, and perhaps eventually high volume, commercial production. It has made some real progress in developing the technology and moving prototyping from labs into industry, but admits that the greatest challenge in moving forward is lack of infrastructure to support the transition.

- Triton: Triton Micro Technologies, a subsidiary of nMode solutions that is partially funded by Asahi Glass Company, is providing some missing segments in the supply chain. Triton has developed a production process to create through glass vias (TGVs) that is sufficient for today's 2.5D applications and it is making interposers for MEMS, RF, and optics at its manufacturing facility in Carlsbad, CA. According to Triton, the major advantage it provides over silicon is the ability to produce solid filled, hermetic TGVs.

Existing commercial products use glass interposers from Triton, but this is much thicker glass, typically 0.3mm or greater. The glass is cut into wafers, matching the form factor of silicon but not requiring backgrinding. This provides the convenience of a process that fits easily into existing manufacturing lines but doesn't take advantage of glass' potential to provide thinner interposers at much lower cost than silicon. Triton can make large panels of 0.1-mm glass with TGVs, but customers do not know how to handle it and may not be inclined to learn.

NanoMarkets understands the potential advantage thin glass would have as an interposer, but is not especially optimistic about its future, especially in the near term. It seems very unlikely that flexible glass will be able to generate large revenues in this space, even if penetration rates get large. Each product uses a very small amount of glass compared to what would be needed for even a smart phone display.

The semiconductor packaging industry may be an even more difficult environment for introducing new processes than the display industry, and we know flexible glass has had challenges there. Still, we feel this sector is worth keeping an eye on to see if glass has an opportunity to succeed where silicon has not.

Noise cancellation: The new failure and yield analysis superpower

GEIR EIDE, *Mentor Graphics, Wilsonville, OR*

Root cause deconvolution is a quick and cost effective way to determine the underlying root causes represented in a population of failing devices from test data alone.

With 22nm FinFET-powered laptops now available and foundries announcing timelines for single-digit manufacturing nodes, it's clear not everybody got the memo declaring Moore's law dead and obsolete. While each new manufacturing node introduces new defect mechanisms, one notable trend is the dramatic increase in number and complexity of design-sensitive defects. This means that in addition to the low yield seen initially as a new manufacturing process is introduced, variability from design to design makes yield a continuing challenge even as the process matures.

The obvious question to ask when you stare at a pile of failing devices is: Why are these devices failing? The pile can represent a number of different defect mechanisms (or root causes). Some may be familiar, while others are new. Some may be easy to find, while others are virtually invisible. Physical failure analysis (PFA) is used to find defects in failing devices, but this is a very costly and time consuming process. Determining what to submit to PFA is therefore a balancing act between controlling expense and finding the relevant defect. Wouldn't it be great if you could determine the underlying root causes early, and pick the die for PFA that represents the causes of interest in an effective and low cost manner? This is the promise of a new scan test diagnosis technology called root cause deconvolution.

Software-based diagnosis of test failures is an established method for localizing defects in digital semiconductor devices. Diagnosis software determines the defect type and location for each failing device based on the design description, scan test patterns, and tester fail data. But diagnosis results contain ambiguity or noise. The diagnosis result for one specific die may point to more than one possible location. Each location may in turn have multiple properties or root causes. For example, the suspect location can span multiple layers (metal3, via4, metal4) while the true root cause is an open defect in just one of these layers. You may observe that many diagnosis results call out net segments

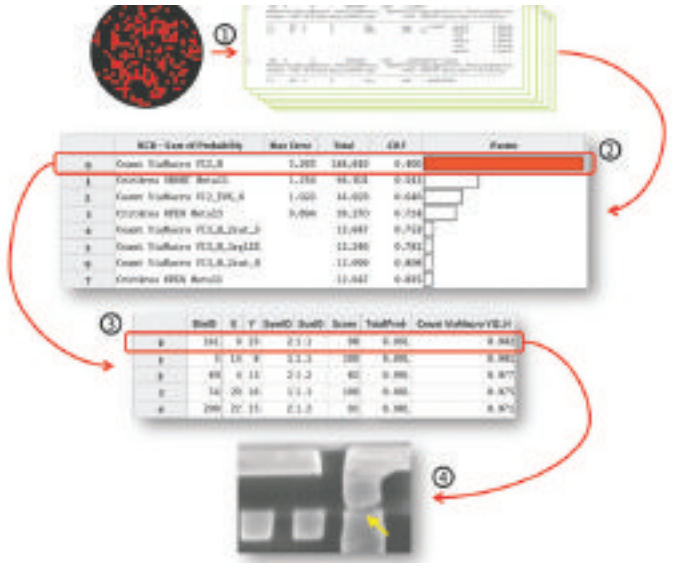

FIGURE 1. Typical application: Root Cause Deconvolution determines root cause distribution and devices most likely to fail for each root cause. Defect courtesy [2].

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that include a particular via type. What you cannot see from the diagnosis results alone is whether that is to be expected or not, i.e. whether this is a common via type or not. This means that plain diagnosis results cannot be used to determine the underlying root cause distribution. Similarly, you may see more bridges in metal3 than metal4, not knowing whether that is to be expected or if it points to a systematic defect. A method called zonal analysis manages this noise by finding relative differences in the diagnosis reports. This method is most effective for identifying hidden systematic defects at fairly high yields, such as the last 1%-2% in high volume manufacturing [1].

But until now there has not been a way to effectively eliminate the noise in the diagnosis results and determine the underlying root causes represented in a population of failing devices. The new root cause deconvolution (RCD) technology is based on Bayesian probability analysis, which is well-known in machine learning applications. It leverages design statistics such as critical area per net segment per metal layer and count of tested cells per cell type. The technology uses a probabilistic model that calculates the probability of observing a set of diagnosis results for a given defect distribution. This model is then used to determine the most likely defect distribution for a given set of diagnosis results.

A typical application of RCD is shown in **FIGURE 1.** For one wafer, the failing cycles are recorded for devices that failed scan test patterns, and then layout-aware diagnosis is performed (1). RCD analysis is done on the diagnosis results, identifying the underlying root cause distribution (2). This result can then be compared with equivalent distributions from the same design or comparable designs. Having this data available before any devices are submitted to PFA significantly accelerates the analysis time. You can then select the root cause of interest, in this case the most significant contributor. The RCD analysis will then identify the die that have the largest probability of failing because of this defect mechanism. Before submitting a die to PFA (4), you know where to look for the defect, and also what to look for.

In a comprehensive experiment [3], RCD results for four lots of failing devices correlated to the conclusions reached through inline inspection, failure analysis, and known process changes. RCD is a quick and cost effective way to determine the underlying root causes represented in a population of failing devices from test data alone. This provides significant value to the yield and failure analysis process at fabless semiconductor companies.

References

1. W. Yang, C. Hao, "Diagnosis-Driven Yield Analysis Improves Mature Yield", Chip Design Magazine, Fall 2011.
2. M. Sharma, et.al., "Efficiently Performing Yield Enhancements by Identifying Dominant Physical Root Cause from Test Fail Data", IEEE International Test Conference, 2008
3. B. Benware, et.al., "Determining a Failure Root Cause Distribution From a Population of Layout-Aware Scan Diagnosis Results", IEEE D&T of Computers, Volume 29, Issue 1. ◆

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The sustainable manufacturing imperative

Companies in the microelectronics manufacturing supply loop see "sustainability" as an important objective in their operations as well as their business strategy. This trend has progressed far beyond the niche players that traditionally positioned themselves as "green," and, in our industry, now includes virtually every significant IC manufacturer as well as a broad base of their suppliers. While sometimes seen as a social, legal and regulatory obligation, sustainability is increasingly considered a differentiating factor in global competitiveness relative to the technologies and products being provided.

Sustainable manufacturing is the creation of manufactured products through economically-sound processes that minimize negative environmental impacts while conserving energy and natural resources. Sustainable manufacturing also enhances employee, community, and product safety. A large and growing number of manufacturers are realizing substantial financial and environmental benefits from sustainable business practices and are driving requirements through the supply chain.

One example cited by the U.S. Environmental Protection Agency pertains to two of Freescale Semiconductor's major energy-using systems that were assessed for energy efficiency. Following the assessment, the company implemented projects which included adjustments to water pumping and compressed air systems. As a result, the company's Oak Hill Fabrication plant in Austin, Texas reduced its annual energy consumption by 28 million kWh of electricity and 26,000 million Btu of natural gas over a three year period, with more than $2 million in annual savings.

Now, key industry trends that influence facilities purchasing decisions pertain to issues such as energy efficiency, pollution control, water conservation, environmental impact, climate protection, conflict minerals in supply chains, as well as the ongoing attention to safety and ergonomics.

Intel Corporation says that technological advancement and environmental sustainability should go hand in hand. The company incorporates environmental performance goals throughout their operations, seeking continuous improvement in energy efficiency, emissions reduction, resource conservation, and other areas. As delineated on the company's web site, Intel strives to minimize the environmental impact of its products—from design through disposal—and seeks innovative ways that technology can help address long-term sustainability challenges. According to their environmental reporting, TSMC requires equipment vendors to consider water, power, and material conservation when designing new generations of equipment, and also requires a long-term blueprint for carbon reduction and future environmental strategy. TSMC also verifies that the energy performance of each tool meets or exceeds conditions set in the procurement contract after tool installation is completed. GLOBALFOUNDRIES also states that environmental sustainability is at the core of high-volume silicon manufacturing.

Recently, SEMI presented its Environment, Health and Safety (EHS) leadership award to Dr. Tzu-Yin (TY) Chiu, CEO of SMIC for minimizing its environmental impact by using resources efficiently, reducing pollution substantially, disposing of hazardous materials responsibly, and upgrading facilities regularly (article: www.semi.org/en/node/49356).

Accordingly, SEMI members see an increasing amount and complexity of EHS performance and reporting requirements from both customers and regulators. Throughout the electronics supply chain there is increased scrutiny of environmental performance and SEMI has long maintained an EHS program that encompasses the industry's broadest network of EHS and purchasing professionals dedicated to collaborating on regulatory, manufacturing and fab facilities issues related to environmental impact.

Now we are extending the spotlight on this important area. In conjunction with SEMICON West and INTERSOLAR North America, SEMI is organizing a four-day Sustainable Manufacturing Forum to share information about the latest technologies, products, and management approaches that promote sustainable manufacturing. The Forum will feature twenty hours of seminars/workshops/roundtable discussions in twelve distinct Sessions as well as many structured opportunities for professional networking. ◆

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