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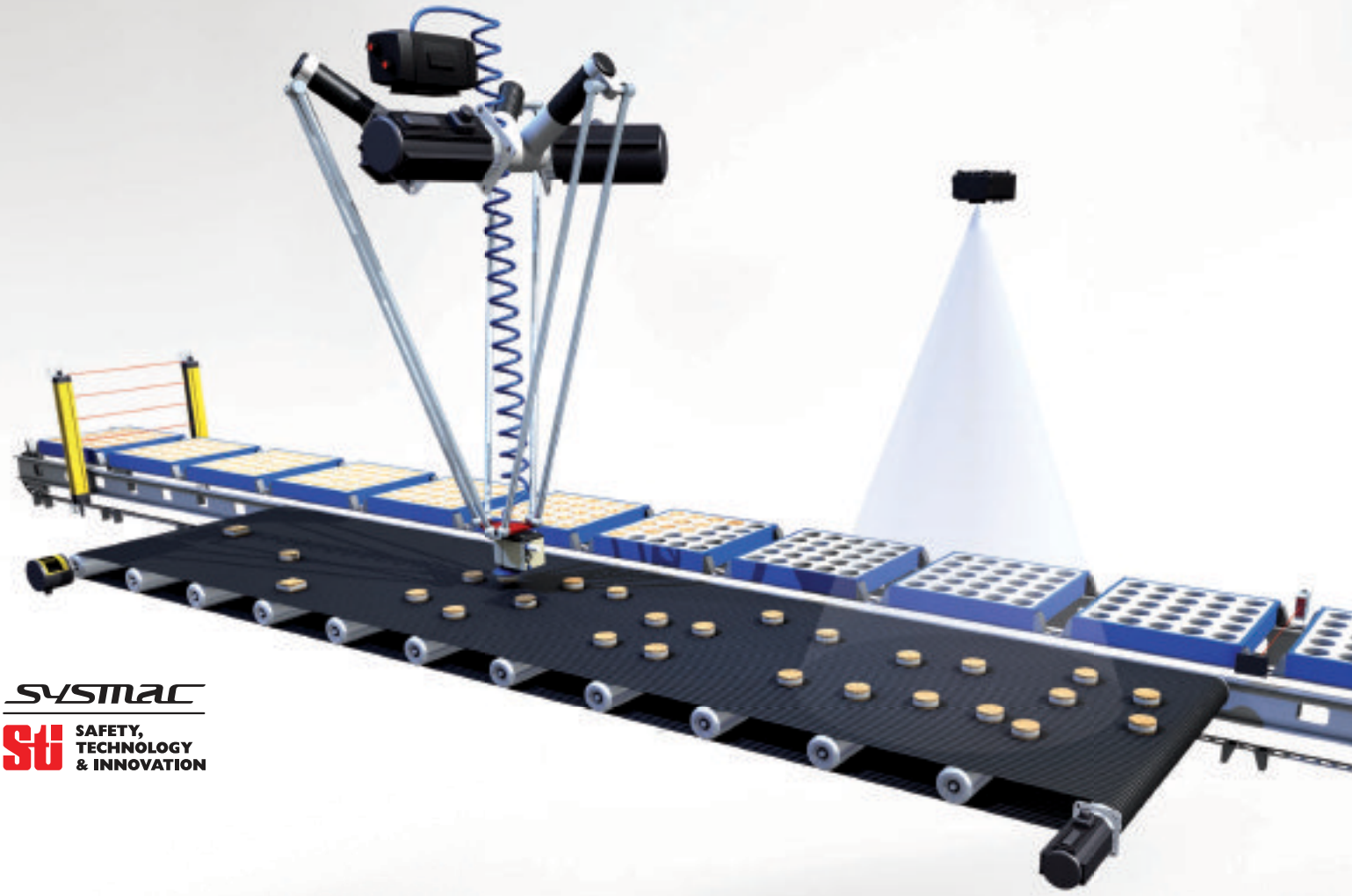

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editorial

IoT, Healthcare and 5G: Are We Ready?

Imagine the world in 2020, only five years from now. If predictions hold true, more than 50 billion devices will be connected to the Internet (creating the Internet of Things), through smart homes, smart cities, smart factories, smart everything.

Two recent Cisco studies show that $19 trillion in IoT value is at stake in the private ($14.4 trillion) and public ($4.6 trillion) sectors. The studies see, for example, $2.5 trillion in value from better use of assets, improving execution and capital efficiency, and reducing expenses and cost of goods sold.

In 2020, cars could be driving themselves and people could be monitoring their health through a variety of smartwatches and other wearables. And, of course, smartphones will continue to proliferate.

5G could also become a reality as early as 2020 (some estimate it will be later, perhaps 2025). Carriers' base stations can handle hundreds of simultaneous users now, but that's not enough to accommodate the billions of new devices that will hook into the Internet of Things. Some estimate that equipment makers will need to increase base station connectivity capacity by a factor of 1,000.

How all of this will impact the semiconductor industry remains to be seen. Certainly, it will be a boon to the trailing-edge technology (i.e., 65nm and above). It will also be beneficial to the RF and microwave arena. Consider RF chips in smartphones. Instead of 30-40 cents for RF chips in a 2G phone, chipmakers will see $2 to $3 in a lower-end 3G smartphone. It then rises to $4 to $6 for a mid-tier LTE smartphone and $10-plus for high-end global LTE smartphones. No estimate yet on 5G smartphones, but it's sure to be more.

It's almost sure to create even more demand for the very leading edge semiconductor chip, such as those found in the high end servers used to crunch huge amounts of data in "the cloud."

Where companies seem to be struggling now is with integration and packaging. It's not yet clear if the existing infrastructure will be able to adequately address the rapidly evolving needs of new markets, such as wearables. But that's a good kind of problem to have.

—Pete Singer, Editor-in-Chief

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Web Exclusives

Trends in Materials: The Smartphone Driver

View on-demand this free webcast where John Borland reviews the current doping and Fin/channel mobility enhancement techniques used for 22nm FinFET production by Intel for both high performance logic and SOC devices and the changes they made for their 2nd generation 14nm FinFET. Apple A6 and A7 used Samsung/Foundry's 32nm and 28nm technology while the A8 uses TSMC's 20nm technology. Later this year, Apple will introduce the A9 which will switch from 2-D planar to 3-D FinFET using both Samsung's 14nm FinFET and TSMC's 16nm FF+ technologies.

http://bit.ly/1HoYOMt

Apple Watch launch confirms WiFi and NFC inside

Dick James at Chipworks takes a look at what's inside the new Apple Watch. He says they won't be going for the gold Edition model, even so some of us here would like to; the Sport version should be quite good enough.

http://bit.ly/1El99z0

Insights from the Leading Edge

Eighteen months after announcing a deal to Tokyo Electron, Applied Materials has announced that the $7B deal will not go through due to regulatory concerns. The two companies said the decision for terminating the deal came after the U.S. Department of Justice told the companies that their proposals for a combined business were not good enough to replace the competition lost from a merger.

http://bit.ly/1bY6l3y

Moore's Law to keep on 28nm

Scaling is now bifurcating – some scaling on with 28/22nm, while other push below 14nm. In his famous 1965 paper Cramming more components onto integrated circuits, Moore wrote: "The complexity for minimum component costs has increased at a rate of roughly a factor of two per year". Dimensional scaling below 28nm will only increase the 'component cost' as we described in Moore's Law has stopped at 28nm and is detailed in the following tables published recently by IBS.

http://bit.ly/1A0vM5k

n&b news and blogs

Innovation in semiconductors provides hope

A new study coauthored by Wellesley economist, Professor Daniel E. Sichel, reveals that innovation in an important technology sector is happening faster than experts had previously thought, creating a backdrop for better economic times ahead.

http://bit.ly/1F2Ath0

IEDM announces 2015 Call for Papers

The 61st annual IEEE International Electron Devices Meeting (IEDM) has issued a Call for Papers seeking the world's best original work in all areas of microelectronics research and development. The paper submission deadline is Monday, June 22, 2015 at 23:59 p.m. Pacific Time.

http://bit.ly/1FbOebp

It's blue skies for Jabil and its customers

While making printed circuit boards is still a big business for the St. Petersburg, Fla.-based Jabil, which boasts 90 plants in 24 countries around the world, the Blue Sky Center emphasizes that Jabil has progressed from being a board manufacturer to a full-service supply chain management firm. (From SemiMD)

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EUROPE – **imec** and **JSR Corporation** signed a letter of intent to partner in enabling manufacturing and quality control of EUV lithography materials.

USA – **Micron Technology** announced that the company has appointed Ernie Maddock as Chief Financial Officer and Vice President, Finance, effective June 1, 2015.

ASIA – **A*STAR's Institute of Microelectronics** has formed a High-Density Fan-Out Wafer Level Packaging (FOWLP) consortium.

USA – **Microchip** signed a definitive agreement to acquire **Micrel** for $14.00 per share.

USA – **SEMATECH** and **Exogenesis Corp.** announced an agreement to commercialize Exogenesis' Accelerated Neutral Atom Beam (ANAB) technology and their nAcceltm accelerated particle beam equipment platform.

ASIA – **GaN Systems Inc.** announced it has signed an agreement with Japanese semiconductor and electronic component distributor, **Value Integrated Technology**.

EUROPE – **Cambridge Nanotherm** appointed Howard Ford as chairman.

USA – **Applied Materials** announced the Applied Centura Tetra Z Photomask Etch system for etching next-generation optical lithographic photomasks.

ASIA – **MagnaChip Semiconductor Corporation** announced that Tae Young Hwang has resigned as the company's president and CEO, and Young-Joon Kim, the company's Interim CEO and general manager, will assume Mr. Hwang's duties.

Applied Materials and Tokyo Electron terminate merger

Applied Materials, Inc. and Tokyo Electron Limited today announced that they have agreed to terminate their Business Combination Agreement (BCA). No termination fees will be payable by either party.

The decision came after the U.S. Department of Justice (DoJ) advised the parties that the coordinated remedy proposal submitted to all regulators would not be sufficient to replace the competition lost from the merger. Based on the DoJ's position, Applied Materials and Tokyo Electron have determined that there is no realistic prospect for the completion of the merger.

"We viewed the merger as an opportunity to accelerate our strategy and worked hard to make it happen," said Gary Dickerson, president and chief executive officer of Applied Materials. "While we are disappointed that we are not able to pursue this path, our existing growth strategy is compelling. We have been relentlessly driving this strategy forward and we have made significant progress towards our goals. We are delivering results and gaining share in the semiconductor and display equipment markets, while making meaningful advances in areas that represent the biggest and best growth opportunities for us.

"I would like to thank our employees for their focus on delivering results throughout this process. As we move forward, Applied Materials has tremendous opportunities to leverage our differentiated capabilities and technology in precision materials engineering and drive a significant increase in the value we create for our customers and investors." ◆

Top 10 2015 semiconductor sales leaders forecast to include NXP/Freescale

IC Insights released its April Update to the 2015 McClean Report, and the update includes the final 2014 company sales rankings for the top 50 semiconductor and top 50 IC companies, and the leading IC foundries. Also included are 2014 IC company sales rankings for various IC product segments (e.g., DRAM, MPU, etc.).

In 2014, there were only two Japanese companies—Toshiba and Renesas—that were among the top 10 semiconductor suppliers (Figure 1). Assuming the NXP/Freescale merger is completed later this year, IC Insights forecasts that Toshiba will be the lone Japanese company left in the top 10 ranking. Anyone who has been involved in the semiconductor industry for a reasonable amount of time realizes this is a major shift and a big departure for a country that once was feared and revered when it came to its semiconductor

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Novel cellular sensing platform for biotech applications

Researchers from the Georgia Institute of Technology have developed a novel cellular sensing platform that promises to expand the use of semiconductor technology in the development of next-generation bioscience and biotech applications.

The research is part of the Semiconductor Synthetic Biology (SSB) program sponsored and managed by Semiconductor Research Corporation (SRC). Launched in 2013, the SSB program concentrates on synergies between synthetic biology and semiconductor technology that can foster exploratory, multi-disciplinary, longer-term university research leading to novel, breakthrough solutions for a wide range of industries.

The Georgia Tech research proposes and demonstrates the world's first multi-modality cellular sensor arranged in a standard low-cost CMOS process. Each sensor pixel can concurrently monitor multiple different physiological parameters of the same cell and tissue samples to achieve holistic and real-time physiological characterizations.

"Our research is intended to fundamentally revolutionize how biologists and bioengineers can interface with living cells and tissues and obtain useful information," said Hua Wang, an assistant professor in the School of Electrical and Computer Engineering (ECE) at Georgia Tech. "Fully understanding the physiological behaviors of living cells or tissues is a prerequisite to further advance the frontiers of bioscience and biotechnology."

Wang explains that the Georgia Tech research can have positive impact on semiconductors being used in the development of healthcare applications including the more cost-effective development of pharmaceuticals and point-of-care devices and low-cost home-based diagnostics and drug testing systems. The research could also benefit defense and environmental monitoring applications for low-cost field-deployable sensors for hazard detections.

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sales presence in the global market.

Figure 1 traces the top 10 semiconductor companies dating back to 1990, when Japanese semiconductor manufacturers wielded their greatest influence on the global stage and held six of the top 10 positions. The six Japanese companies that were counted among the top 10 semiconductor suppliers in 1990 is a number that has not been matched by any country or region since (although the U.S. had five suppliers in the top 10 in 2014). The number of Japanese companies ranked in the top 10 in semiconductor sales slipped to four in 1995, fell to three companies in 2000 and 2006, and then to only two companies in 2014.

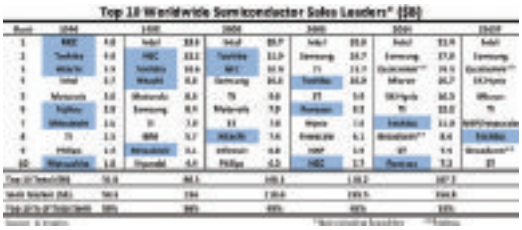

FIGURE 1.

Figure 1 also shows that, in total, the top 10 semiconductor sales leaders are making a marketshare comeback. After reaching a marketshare low of 45 percent in 2006, the top 10 semiconductor sales leaders held a 53 percent share of the total semiconductor market in 2014. Although the top 10 share in 2014 was eight points higher than in 2006, it was still six points below the 59 percent share they held in 1990. As fewer suppliers are able to achieve the economies of scale needed to successfully invest and compete in the semiconductor industry, it is expected that the top 10 share of the worldwide semiconductor market will continue to slowly increase over the next few years. ◆

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FIGURE 1. A CMOS multi-modality cellular sensor array chip being developed at Georgia Tech is hosted on a standard printed circuit board (PCB) and is packaged using low-cost polydimethylsiloxane (PDMS) material to ensure biocompatibility and electrical insulation. A standard 35 mm cell culture dish with drilled-out bottom is mounted on the PCB to host the cells and medium, and expose cells to the CMOS sensing surface. (Georgia Tech Photo: Rob Felt)

Specifically, in the case of the more cost-effective development of pharmaceuticals, the increasing cost of new medicine is largely due to the high risks involved in the drug development. As a major sector of the healthcare market, the global pharmaceutical industry is expected to reach more than $1.2 trillion this year. However, on average, only one out of every ten thousand tested chemical compounds eventually become an approved drug product.

In the early phases of drug development (when thousands of chemical candidates are screened), in vitro cultured cells and tissues are widely used to identify and quantify the efficacy and potency of drug candidates by recording their cellular physiology responses to the tested compounds, according to the research.

Moreover, patient-to-patient variations often exist even under the administration of the same type of drugs at the same dosage. If the cell samples are derived from a particular patient, patient-specific drug responses then can be tested, which opens the door to future personalized medicine.

"Therefore, there is a tremendous need for low-cost sensing platforms to perform fast, efficient and massively parallel screening of in vitro cells and tissues, so that the promising chemical candidates can be selected efficiently," said Wang, who also holds the Demetrius T. Paris Junior Professorship in the Georgia Tech School of ECE. "This existing need can be addressed directly by our CMOS multi-modality cellular sensor array research."

Among the benefits enabled by the CMOS sensor array chips are that they provide built-in computation circuits for in-situ signal processing and sensor fusion on multi-modality sensor data. The chips also eliminate the need of external electronic equipment and allow their use in general biology labs without dedicated

electronic or optical setups.

Additionally, thousands of sensor array chips can operate in parallel to achieve high-throughput scanning of chemicals or drug candidates and real-time monitoring of their efficacy and toxicity. Compared with sequential scanning through limited fluorescent scanners, this parallel scanning approach can achieve more than 1,000 times throughput enhancement.

The Georgia Tech research team just wrapped its first year of research under the 3-year project, with the sensor array being demonstrated at the close of 2014 and presented at the IEEE International Solid-State Circuits Conference (ISSCC) in February 2015. In the next year, the team plans to further increase the sensor array pixel density while helping improve packaging solutions compatible with existing drug testing solutions.

"Georgia Tech's research combines semiconductor integrated circuits and living cells to create an electronics-biology hybrid platform, which has tremendous societal and technological implications that can potentially lead to better and cheaper healthcare solutions," said Victor Zhirnov, director of Cross-Disciplinary Research and Special Projects at SRC.

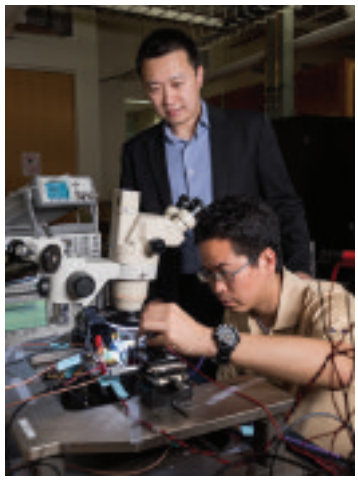

FIGURE 2. Georgia Tech Ph.D. student Jong Seok Park (right) is performing electrical testing of the CMOS sensor chip with Assistant Professor Hua Wang (left). (Georgia Tech Photo: Rob Felt)

SRC names former Freescale CTO Ken Hansen as new president and CEO

Semiconductor Research Corporation (SRC) announced that Ken Hansen has been appointed SRC's new President and Chief Executive Officer (CEO), effective June 1.

Hansen's professional experience includes serving as Vice President and Chief Technology Officer (CTO) at Freescale Semiconductor since 2009. Hansen replaces retiring SRC President and CEO Larry Sumney who guided the organization for more than 30 years since its inception in 1982. SRC's many accolades over the years include being the recipient of the National Medal of Technology in 2007.

"SRC under Larry Sumney's leadership has made an indelible impact on the advancement of technology during the past three decades, and we congratulate Larry on his retirement and salute him for his contributions to the semiconductor industry," said Mike Mayberry, Intel Corporate Vice President and Director of Components Research who is SRC Board Chairman. "We also welcome Ken Hansen to his new role guiding SRC, and we look forward to Ken's leadership helping SRC reach new heights in an era where basic research and development is as critical as ever."

Prior to his CTO role at Freescale, Hansen led research and development teams for more than 30 years in multiple senior technology and management positions at Freescale and Motorola. Hansen holds Bachelor and Master of Science degrees in Electrical Engineering from the University of Illinois where he has been recognized as an ECE (Department of Electrical and Computer Engineering) Distinguished Alumni.

In his new role at SRC, Hansen intends to build on the consortium's mission of driving focused industry research to both advance state-of-the-art technology and continue to create a pipeline of qualified professionals who will serve as next-generation leaders for the industry.

"SRC also has an opportunity to strengthen its core by recruiting new members to gain more leverage to fund industry wide solutions for some of the challenging technology roadblocks that are ahead of us," said Hansen.

"The model that SRC has developed is unmatched in the industry and has proven to be extremely significant. The industry would not be where it is today without the contributions of SRC under the leadership and vision of Larry Sumney," Hansen continued.

Meanwhile, Sumney's decorated career began in 1962 at the Naval Research Laboratory. He later directed various other research programs at Naval Electronics Systems Command and the Office of the Undersecretary of Defense — including the Department of Defense's major technology initiative, Very High Speed ICs (VHSIC) —before agreeing to lead SRC following its formation by the Semiconductor Industry Association.

Under his leadership, SRC has also formed wholly owned subsidiaries managing the Nanoelectronics Research Initiative (NRI), the Semiconductor Technology Advanced Research network (STARnet) and the SRC Education Alliance, among other programs. Sumney received a Bachelor of Physics from Washington and Jefferson (W&J) College, which recognized him with the 2012 Alumni Achievement Award, and a Master of Engineering Administration from George Washington University.

"I have enjoyed a front row seat in the development of today's technology-based economy and advancement of humanity through the semiconductor industry," said Sumney. "I am completely confident that SRC is well positioned and will continue to flourish, to seed breakthrough innovation and help provide the people and ideas to keep the U.S. semiconductor industry competitive and prosperous in years to come."

IBM's silicon photonics technology ready to speed up cloud and Big Data applications

IBM announced a significant milestone in the development of silicon photonics technology, which enables silicon chips to use pulses of light instead of electrical signals over wires to move data at rapid speeds and longer distances in future computing systems.

For the first time, IBM engineers have designed and tested a fully integrated wavelength multiplexed silicon photonics chip, which will soon enable manufacturing of 100 Gb/s optical transceivers. This will allow datacenters to offer greater data rates and bandwidth for cloud computing and Big Data applications.
"Making silicon photonics technology ready for widespread commercial use will help the semiconductor industry keep pace with ever-growing demands in computing power driven by Big Data and cloud services," said Arvind Krishna, senior vice president and director of IBM Research. "Just as fiber optics revolutionized the telecommunications industry by speeding up the flow of data — bringing enormous benefits to consumers — we're excited about the potential of replacing electric signals with pulses of light. This technology is designed to make future computing systems faster and more energy efficient, while enabling customers to capture insights from Big Data in real time."

Silicon photonics uses tiny optical components to send light pulses to transfer large volumes of data at very high speed between computer chips in servers, large datacenters, and supercomputers, overcoming the limitations of congested data traffic and high-cost traditional interconnects. IBM's breakthrough enables the integration of different optical components side-by-side with electrical circuits on a single silicon chip using sub-100nm semiconductor technology.

IBM's silicon photonics chips uses four distinct colors of light travelling within an optical fiber, rather than

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traditional copper wiring, to transmit data in and around a computing system. In just one second, this new transceiver is estimated to be capable of digitally sharing 63 million tweets or six million images, or downloading an entire high-definition digital movie in just two seconds.

The technology industry is entering a new era of computing that requires IT systems and cloud computing services to process and analyze huge volumes of Big Data in real time, both within datacenters and particularly between cloud computing services. This requires that data be rapidly moved between system components without congestion. Silicon photonics greatly reduces data bottlenecks inside of systems and between computing components, improving response times and delivering faster insights from Big Data.

IBM's new CMOS Integrated Nano-Photonics Technology will provide a cost-effective silicon photonics solution by combining the vital optical and electrical components, as well as structures enabling fiber packaging, on a single silicon chip. Manufacturing makes use of standard fabrication processes at a silicon chip foundry, making this technology ready for commercialization.

Silicon photonics technology leverages the unique properties of optical communications, which include transmission of high-speed data over kilometer-scale distances, and the ability to overlay multiple colors of light within a single optical fiber to multiply the data volume carried, all while maintaining low power consumption. These characteristics combine to enable rapid movement of data between computer chips and racks within servers, supercomputers, and large datacenters, in order to alleviate the limitations of congested data traffic produced by contemporary interconnect technologies.

Silicon photonics will transform future datacenters

By moving information via pulses of light through optical fibers, optical interconnects are an integral part of contemporary computing systems and next generation datacenters. Computer hardware components, whether a few centimeters or a few kilometers apart, can seamlessly and efficiently communicate with each other at high speeds using such interconnects. This disaggregated and flexible design of datacenters will help reduce the cost of space and energy, while increasing performance and analysis capabilities for users ranging from social media companies to financial services to universities.

Most of the optical interconnect solutions employed within datacenters as of today are based upon vertical cavity surface emitting laser (VCSEL) technology, where the optical signals are transported via multimode optical fiber. Demands for increased distance and data rate between ports, due to cloud services for example, are driving the development of cost-effective single-mode optical interconnect technologies, which can overcome the bandwidth-distance limitations inherent to multimode VCSEL links.

IBM's CMOS Integrated Nano-Photonics Technology provides an economical solution to extend the reach and data rates of optical links. The essential parts of an optical transceiver, both electrical and optical, can be combined monolithically on one silicon chip, and are designed to work with with standard silicon chip manufacturing processes.

IBM engineers in New York and Zurich, Switzerland and IBM Systems Unit have demonstrated a reference design targeting datacenter interconnects with a range up to two kilometers. This chip demonstrates transmission and reception of high-speed data using four laser "colors," each operating as an independent 25 Gb/s optical channel. Within a full transceiver design, these four channels can be wavelength multiplexed on-chip to provide 100 Gb/s aggregate bandwidth over a duplex single-mode fiber, thus minimizing the cost of the installed fiber plant within the datacenter.

Further details will be presented by IBM at the 2015 Conference on Lasers and Electro Optics (May 10-15) in San Jose, California, during the invited presentation entitled "Demonstration of Error Free Operation Up To 32 Gb/s From a CMOS Integrated Monolithic Nano-Photonic Transmitter," by Douglas M. Gill, Chi Xiong, Jonathan E. Proesel, Jessie C. Rosenberg, Jason Orcutt, Marwan Khater, John Ellis-Monaghan, Doris Viens, Yurii Vlasov, Wilfried Haensch, and William M. J. Green.

IBM Research has been leading the development of silicon photonics for more than a decade, announcing a series of technology milestones beginning in 2006. Silicon photonics is among the efforts of IBM's $3 billion investment to push the limits of chip technology to meet the emerging demands of cloud and Big Data systems. ◆

FOWLP and embedded packaging

Phil Garrou,
Contributing Editor

At the recent IMAPS conference, Yole's Jerome Alzemer updated the audience on the Fan Out and Embedded die marketplace, based on his new report "Fan out and Embedded Die: Technology and Market Trends."

Embedded packaging refers to many different concepts, IP, manufacturing infrastructures and related technologies. The two main categories of embedded packages are (1) those based on a molded wafer infrastructure such as FOWLP and (2) those based on a PWB/PCB laminate panel infrastructure.

Fan-out WLP are "re-configured" by placing known good ICs active face down on a foil and by over-molding them. These wafers are then flipped and processed in the wafer fab with RDL/ball placing and diced.

For chip embedding in laminate, known good ICs are picked and placed on top of an organic layer of Printed circuit board and subsequent layers are laminated on top. Regular PCB manufacturing operations then take place on the panel containing the embedded ICs.

Fan Out WLP (FOWLP)

Unlike Fan In WLP, which has been commercialized since the late 1990's, FOWLP is not constrained by die size, and thus can offer an unlimited number of interconnects for maximum connection density. One can also achieve finer line/spacing, improved electrical and thermal performance and small package dimensions to meet the relentless form factor requirements and performance demands of the mobile market.

Commercialization of the Infineon e-WLB (embedded wafer level BGA) technology started in 2009 with single die packages for cell phone baseband chips. The Infineon technology was later licensed to OSATS Nanium, STATSChipPAC and ASE, thus creating a multi-sourced infrastructure.

A similar process called Redistributed Chip Packaging (RCP) was developed by Freescale during the same time period. It was subsequently licensed to NEPES but has not yet reached HVM. Other developing FOWLP technologies -- including those of TSMC (called InFO), SPIL and J- Devices -- are approaching commercialization but will initially lack the multi-sourcing available with eWLB.

The second generation of FOWLP are multichip packages including PoP and SiP configurations. These are generating increased interest in this packaging approach.

As of 2014 Yole estimates that the market is ~ $174MM. With the expected entry of several major players like TSMC, Yole envisions the market growing at a 30% CAGR to > $600MM by 2020.

Technical challenges such as warpage, die shift, chip-to-mold non planarity and topography remain significant limitations. ◆

Safe CMP slurries

Ed Korczynski, Sr. Technical Editor

New chemical-mechanical planarization (CMP) processes for new materials planned to be used in building future IC devices are now in research and development (R&D). Early data on process trade-offs as well as on environmental, health, and safety (EHS) aspects were presented at the CMP Users Group (of the Northern California Chapter of The American Vacuum Society) meeting, held in Albany, New York on April 16 of this year in collaboration with the College of Nanoscale Science and Engineering (CNSE) SUNY Polytechnic Institute and SEMATECH.

Mike Corbett, principle with Linx Consulting, presented his company's forecast on CMP consumable materials growth for both logic and memory. "We're no longer in the era of 2D scaling. Right now the semiconductor industry is scaling through the use of novel materials and 3D structures. It started with memory cells going vertical for storage structures. All of these technologies rely on CMP as a key enabler: for 3D NAND there'll be new tungsten, TSV need new copper, and transistors need CMP for high-k/metal-gate processing."

Corbett estimates the current global market for pre-interconnect CMP consumables—slurries, pads, and conditioning disks—at >$US1.5B annually with steady growth on the horizon. While the fabricated cost/wafer at the leading edge is estimated to increase by 25-60% when moving to the next leading-edge node, the cost of CMP consumables should only increase by 12-14%. **FIGURE 1** shows the specific example of 2D NAND wafer cost increasing by 60% in moving from 20nm- to 16nm-node production, while the fab's CMP costs increase just ~12%. Until the IC HVM industry begins using materials other than Si/SiGe for transistor channels it seems that CMP costs will be well controlled.

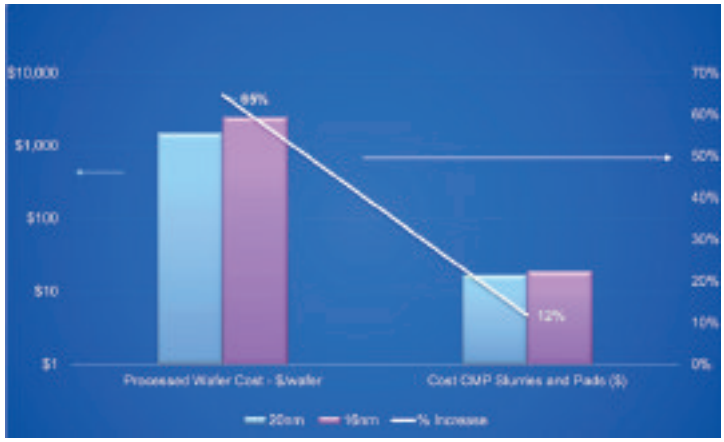

FIGURE 1. Cost modeling shows that 2D NAND memory fab cost/wafer increases 65% when moving from 20nm- to 16nm-node production, while the cost of CMP consumable materials may increase only 12% for that fab. (Source: Linx Consulting)

Alternate channel materials toxicity in CMP

With alternate channel materials on the horizon for future logic transistor, III-V materials such as gallium-arsenide (GaAs), gallium-indium-phosphide (GaInP), and indium-phosphide (InP) are now in R&D which leads to questions regarding direct process costs as well as indirect EHS costs. Hsi-An Kwong, SEMATECH EHS Program Manager, provided an important overview of these issues in his presentation on "Out-gassing from III-V Wafer Processing." Much of the concern involves the possible reaction and release of toxic hydrides such as arsine, and phosphine. SEMATECH worked with imec to monitor hydrides produced during CMP processes for high-mobility compound semiconductors.

With 1.5% H_2O_2 in a relatively low-pH slurry, phosphine was measured on the tool from InP but not from GaInP. Use of higher pH with the same 1.5% H_2O_2 resulted in no phosphine from InP, but arsine outgassing from GaAs. Use of the highest pH resulted in no outgassing of phosphine or arsine. "When we develop the CMP process, particularly when moving to HVM we need to study the layers on the wafer and the slurry used to evaluate if outgassing will be an issue," explained Kwong. "FTIR is the metrology instrument needed to be able to distinguish between different evolved hydride species." HVM fab personnel working on or near CMP tools would have to wear personal breathing apparatus if processes evolve hydrides; for example, the SEMATECH/CNSE continuous exposure EHS specification allows a maximum human exposure level of just 1.25 ppb arsine.

Reduced Defectivity and Cost of Ownership Copper CMP Cleans

CHRISTOPHER ERIC BRANNON, *Texas Instruments, Dallas, TX*

A new, low pH, BTA free, noble-bond chemistry produced equivalent yield at substantially lower costs.

The 2010 economic downturn affected many industries, semiconductor manufacturing notwithstanding. Many fabrication facilities had to layoff employees and curtail spending, all the while managing lower wafer output. This effect caused many semiconductor companies to rethink how they spend on resources. Everything was considered, from the cost of the wafers to the cost of the tool consumables and chemistries.

Texas Instruments (TI) copper chemical-mechanical planarization (Cu CMP) was no different. All spending had to be reduced and copper hillock defect had to be eliminated. The CMP Team proposed developing a process based on the new third generation clean chemistry on the market for a number of economic and logistical reasons. The first rationale for this strategy was cost and second was time - most of the clean chemistries on the market were considerably cheaper than the current process of record (POR). CMP had also seen many defects due to via-to-via shorts caused by Cu hillocking (localized Cu protrusion into the above interlayer dielectric; see **FIGURE 1**).

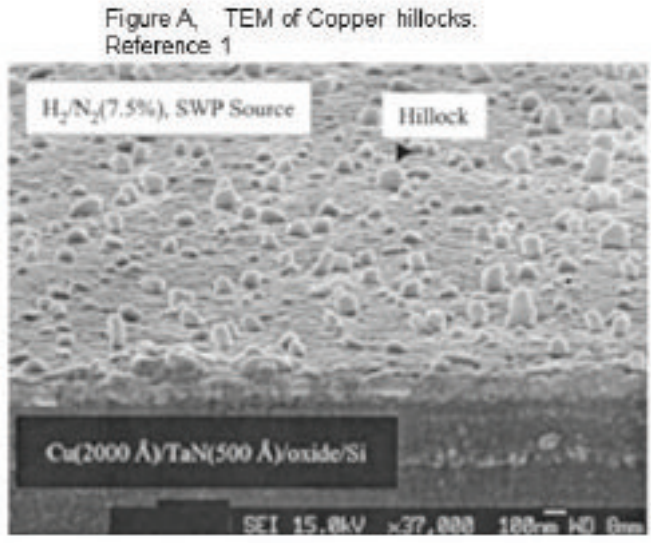

FIGURE 1. TEM of copper hillocks [1].

A successful Cu cleaning CMP process

There were two key reasons that TI succeeded in developing a Cu cleaning process: detailed engineering work and strong vendor support. Process development went through four generations of refinement before it was ready for high volume manufacturing. The first version focused on new clean chemistry improvements such as third generation low pH, high acid clean chemistry and an array of design of experiments (DOE) continuous improvement through optimization of the process controls and equipment modification followed in the second. The third generation attempted to adapt an existing Mirra-Desica process using a previous qualified process. A final successful attempt was made during the fourth cycle to develop a lower cost, higher throughput multi-copper platen cleaning process using a commercial chemistry from Air Products, COPPEREADY®CP72B. This paper will discuss the work that went into building TI's successful Cu cleaning CMP process.

TI Cu CMP

Neutral pH clean chemistries using Benzotriazole (BTA) were the first generation application on most

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Cu CMP dual damascene back end of the line process at TI. This was dependent on using dry-in wet-out Cu CMP AMAT tools with spray acid Vertec hoods for cleaning and drying. It was also very high in cost and low in consumable life compared to most conventional CMP clean process (e.g. Tungsten, STI, Oxide). The TI POR was no different, a first generation Cu clean using three different chemistries, BTA, Electra Clean™ and ESC774™. These chemistries were very expensive to use and were not very efficient at cleaning or passivating the polished copper surface. They were able to passivate the copper surface but were prone to leave many types of incompatible carbon residue defects on the wafers. Cu hillocking was very prevalent with this type of cleaning solution and via-to-via shorts in the back end of the line (BEOL) were the top defect pareto for TI.

Clean chemistry identification

To reduce the time to develop a new Cu CMP clean process, most of the development cycle focused on Cu cleans leveraging a Mirra-Desica™ DIDO Cu polishing process using existing pads, conditioning pucks, and heads. Early on, it was decided that to achieve maximum throughput, the wafers would need to be processed through the tool's onboard scrubber and dry station as quickly as possible. With time running out, the Cu CMP team had contacted the major players in Cu clean chemistry to obtain their specific information and prepare a white paper screening to determine the correct path. The four candidates were evaluated on chemistry type, makeup, pH, passivation (BTA), cost, and compatibility to our current Cu and barrier slurry. Two of the chemistries fit the bill for the criteria and were selected for further testing. Chemistry 1 was a novel approach for Cu CMP and was from our current clean chemistry vendor, Chemistry 2 was similar to the current TI process of record.

The initial criteria used to judge the chemistries were blanket test wafer performance (Cu, Teos, Ta, and Nitride): etch rate, passivation, cleaning tunability via recipe parameter windowing, and defectivity. Experimental designs were run on the basic process controls with these chemistry's with respect to the polish process: carrier speed, table speed, down-force, carrier position, carrier oscillation, and chemical flow. Both cleans performed well on the blanket experiments and were advanced to short loop, patterned wafer tests. These patterned wafer tests were used to study product behavior in the polisher and brush cleaner. A significant amount of time was spent adjusting recipe parameters to eliminate defects. The team contacted both vendors to do lifetime experiments with consumables at their facilities. The data that was collected revealed many issues with each candidate, one more so than the other (**FIGURE 2**).

Chemistry A was a second generation Cu clean that had high pH but had chemical additives that would aid in cleaning, still a very basic approach to wafer cleaning. The overall defectivity was sufficient on the product test wafers but would degrade after a short time window after polish. It also had to be paired with another chemistry to achieve the same Cu passivation as the POR. This chemistry was disqualified due to this reason.

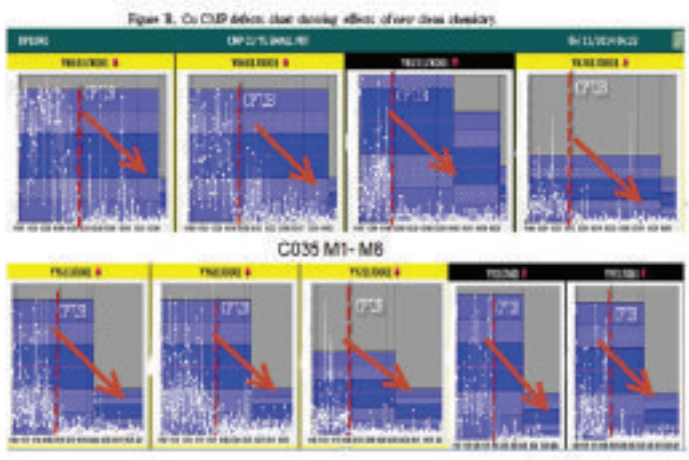

FIGURE 2. Charts of Cu CMP defects showing effects of new clean chemistry.

Chemistry B is a third generation Cu clean that had low pH (about ~2.1) and it is BTA-free, unlike any other Cu cleans on the market at that time. This chemistry is an organic acid blend, which helps ionize Cu2O and CuO to form water and soluble Cu complex, used for passivation. This forms a strong bond with the Cu to make the surface nobel. The low pH helps to dissolve the surface defects resulting in a step function decrease in defectivity compared to baseline (see Figure B). The chemistry was also scalable, depending on concentration making cost of ownership low. This chemistry was selected for qualification at TI Cu CMP.

Vendor support

TI's internal polishing engineering staff was augmented with exceptional support from several consumable vendors during development. Together TI engineers developed proprietary and patent-pending technologies to enhance the Mirra Desica cleaner performance on Cu BEOL CMP. TI also benefited from strong relationships with its contact clean brush suppliers. Rippy™ was instrumental in brush evaluations and consultation on process developments. To improve the tool's performance, DOW™ was pivotal in adding additional functionality to the process through end of life evaluations. Perhaps most important of all relationships that developed was with Air Products, who provided an invaluable education into Cu cleaning process development.

Solving defect issues

During process development, TI engineers encountered several defect related issues. Some issues like photo-induced corrosion were resolved quickly after some technical research. There were two others that took more troubleshooting: carbon residue defects and Cu hillock formation.

The presence of gross surface defects, like carbon residue is an obvious yield killer. The Cu CMP Engineers come to the conclusion through EDX (Energy-dispersive X-ray spectroscopy) and much lab analysis that the current Cu slurry still had traces of BTA in it and were causing this residue defect to form on the wafers after polish. Many DOE later determined that extending the clean chemistry buff polish would eliminate this defect.

With residue defects effectively eliminated, the next major technical challenge was Cu hillock formation. TI had been experiencing higher defectivity due to back end of the line via to via shorts on the previous Cu CMP clean chemistry process. It was understood that the formation of Cu hillocks were the cause for this signature. To solve this problem, a completely different wafer cleaning chemistry was needed to passivate the copper surface. TI Cu CMP Engineers looked for one that did not use BTA or other

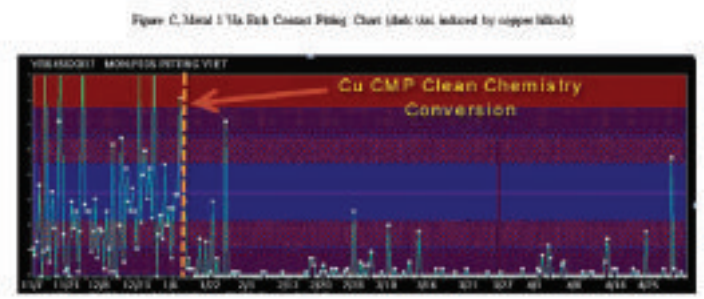

FIGURE 3. Metal 1 via etch contact pitting chart (dark vias induced by copper hillock).

high pH chemistries, but, would coat the wafer surface and not allow native oxides to grow on the Cu. The new chemistry (CoppeReady®CP72B) proved to form a nobel bond with the Cu (CuO2) and eliminated hillock growth formation, thereby reducing via-to-via shorts (see **FIGURE 3**).

Further process development

One of the last stages of development on the new process was a project to develop a faster through-put process. Although this work was successful, it highlights some of the challenges in pursuing this type of strategy. The motivation for this work was to dramatically boost the throughput and to further cut process expense. The POR process was limited by the cleaner and was much slower causing higher cost and higher wafer-per-hour rates. To maximize throughput, the new process would have two components: speed up the on board cleaner, brush box 1&2 throughput, as well decrease the platen 2&3 process times but include a clean chemistry buff. Because of the high down forces employed to achieve a flat removal profile, the Cu polishing component of this work, platen 1, was surprisingly fast but was the intended bottle neck. These changes allowed for a 10 percent increase in overall wafer through put compared to the baseline process. This had an alternate effect on the Cu polish process. TI's current Cu slurry is thermally driven, with making platen 1 the bottle neck it kept that platen at one constant temperature throughout the lot, causing the overall end point times (EPD) to be reduced and streamlined. This further increased the tools throughput by 2 percent and reduced wafer to wafer EPD variation down to 2 to 3 seconds; previous was 10 to 12 sec between wafers (see **FIGURE 4)**.

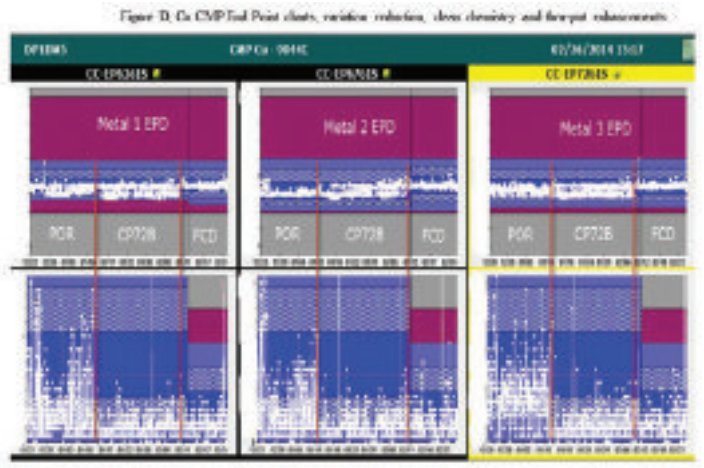

FIGURE 4. Cu CMP end point charts, variation reduction, clean chemistry and throughput enhancements.

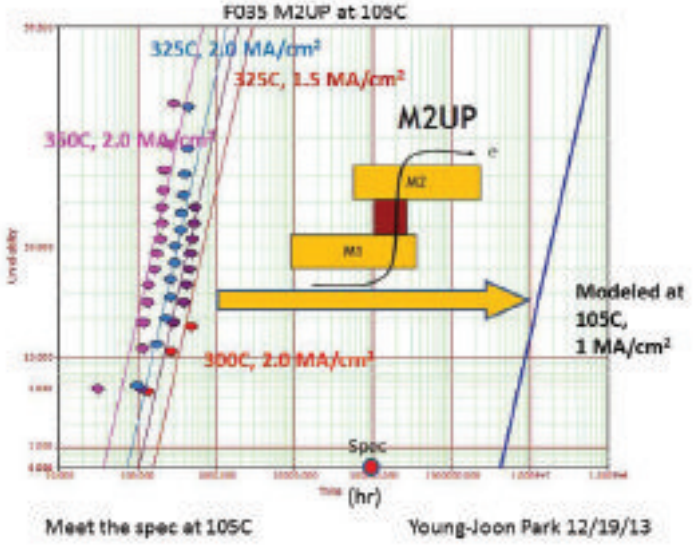

FIGURE 5. Electromigration (EM) stress test, new clean vs baseline.

Benchmarking performance

For initial qualification and benchmarking, TI installed and setup the best known method (BKM) Cu polishing process on an Applied Materials Mirra-Desica™. To bring the new clean process into production, Cu Polish engineers needed to demonstrate equivalent or better yield between the two competing process. The new clean chemistry needed to be tested for EM (electro migration), which is a stress test of Cu interconnects between two metal lines. This test had to be outsourced to a third party company that specializes in oven-baking stress tests (**FIGURE 5**). After extensive electrical and yield testing, the new clean process was fully released. Sample yield comparisons consistently demonstrated that the

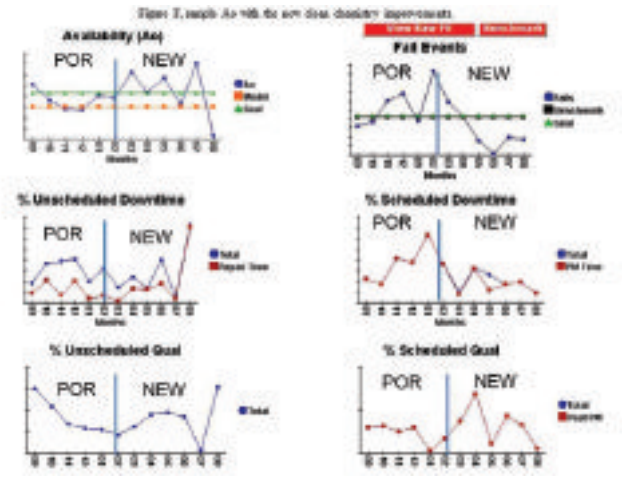

FIGURE 6. Sample availability with the new clean chemistry improvements.

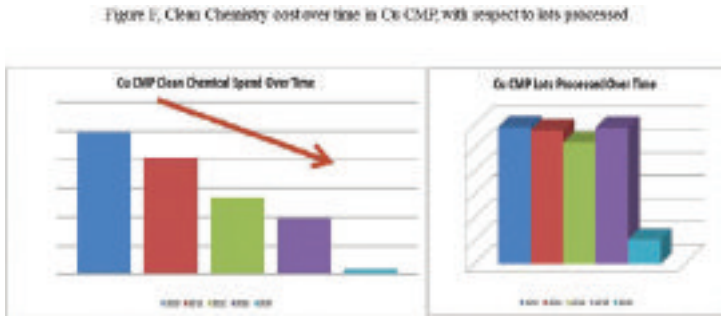

FIGURE 7. Clean chemistry cost over time in Cu CMP in terms of lots processed.

performance is equivalent to slightly better and the new process has higher through-put (~12 percent). The chemical costs (dilute 60 to 1 CP72B®) are 68 percent less per wafer pass than the competing process. The pad/conditioner life had increased by 13 percent from the previous process due to thermal driven Cu slurry through put modification (**FIGURES 6 AND 7**).

Conclusion

TI engineers developed a Cu CMP cleaning process using new third generation low pH Cu chemistry. Despite the tool's many limitations, the engineering staff successfully delivered an integrated process capable of producing equivalent yield at substantially lower costs over the best alternative method. There were undoubtedly challenges along the way, only a fraction of which have been described in this paper. By leveraging an existing deep reservoir of engineering, maintenance, and operational talent, an existing and efficient supply chain, and the outstanding support of numerous vendors, TI Polish module was able to realize its goal of making efficient use of its assets to achieve a competitive advantage.

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1. Tsung-Kuei Kanga, and Wei-Yang Choub Author. 'Avoiding Cu Hillocks during the Plasma Process' Journal of The Electrochemical Society, 151

A novel characterization technique unveils the 3D structure of conductive filaments in resistive switching memories

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Imec researchers have developed a novel technique – termed conductive atomic force microscopy tomography (or scalpel C-AFM) – that enables a three-dimensional characterization of emerging logic and memory devices.

With the introduction of three-dimensional devices (such as FinFETs) and stackable architectures (such as vertical NAND Flash memories), there is a growing need for 3D characterization techniques. These techniques should not only be capable of probing in three dimensions and examining the topological properties. They should also enable an analysis of the electrical properties of the 3D nano-sized volumes.

A shining example illustrating the need for this technique are conductive bridging random access memory (or CBRAM) devices. These devices belong to the emerging class of resistive RAM (or RRAM) memories which exhibit a fast operation, low power consumption, high endurance and high scalability. They are currently seen as a candidate memory technology for application in storage class memories and embedded non-volatile memories. Their operation basically relies on the formation of a highly conductive path, the conductive filament, in a poorly conductive medium. But the formation of this filament in an integrated device has so far never been observed with the techniques available today. A full 3D characterization of the conductive filament would considerably enhance our understanding of the filament growth dynamics and the underlying physical mechanisms. And it would enable a further optimization of the memory device.

Umberto Celano, using the novel scalpel C-AFM tool.

Scalpel C-AFM, extending the 2D capabilities of C-AFM

A well-known characterization technique for advanced logic and memory devices is scanning probe microscopy

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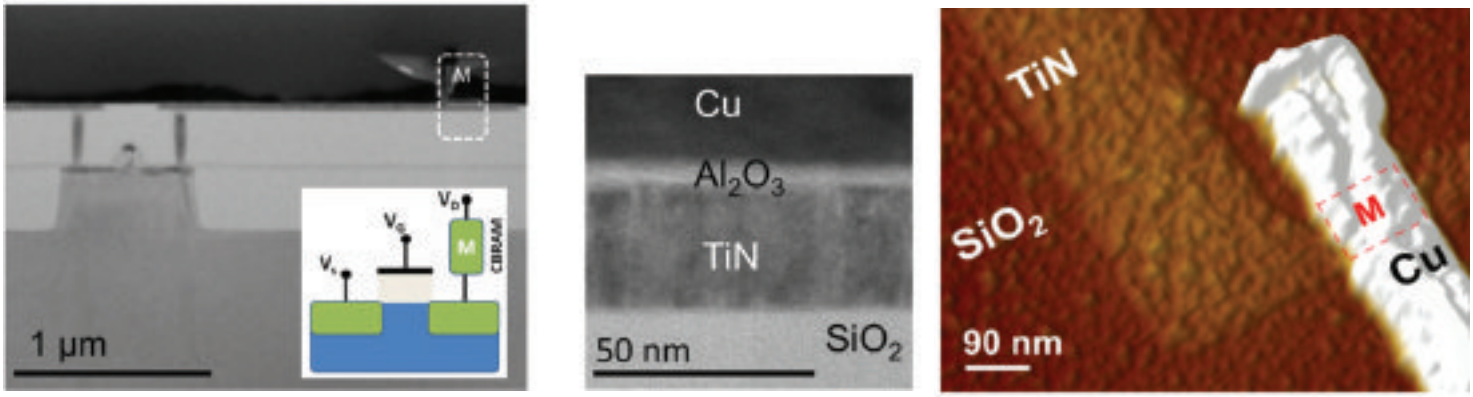

FIGURE 1. CBRAM device: Cross-section transmission electron microscopy (TEM) image of the CBRAM memory device (left) and the device stack (middle), and AFM image of the cross-point area (right).

(or SPM), where a sharp tip slides on a flat surface. The 2D-maps of electrical properties provided by this technique have for many years enabled the understanding and development of advanced planar technologies at the nanoscale. SPM comes in several flavors, such as scanning tunnel microscopy (STM), atomic force microscopy (AFM), and a whole range of secondary analysis modes such as conductive AFM (or C-AFM). C-AFM is based on contact-mode AFM using a (biased) conductive tip. The topography is measured in contact-mode, while the current flowing between the biased sample and the tip is recorded simultaneously.

Researchers at imec have now evolved the C-AFM technique into a 3D characterization tool, suited to probe very confined volumes at the nanoscale. The new method consists in collecting the C-AFM images of the sample at different depths. The sectioning is induced by a controlled material removal. This is done by applying a strong pressure (GPa) between the (biased) conductive-diamond tip and the sample during the C-AFM scan. This way, sub-nm vertical removal rates are obtained. Since the diamond tip acts as a scalpel, the new method is referred to as scalpel C-AFM. The technique can be used for a wide variety of materials, and can be extended to other contact-mode AFM methods such as scanning spreading resistance microscopy.

Case: CBRAM memory devices

The imec researchers have used the scalpel C-AFM technique for studying the conductive filament formation in CBRAM memory devices. In these devices, an abrupt change in electrical resistance occurs when the device is subjected to a voltage pulse. The different resistance states are induced by the formation or dissolution of a highly conductive filament into a poorly conductive medium.

The heart of the CBRAM memory cell is a thin dielectric (e.g., Al_2O_3) that is sandwiched between the active electrode (Cu or Ag) and an inert counter electrode (e.g., TiN). When a positive voltage is applied to the active electrode, a field-assisted injection and transport of cations begins. This leads to the creation of the conductive filament inside the Al_2O_3 oxide layer. The presence of this filament dramatically lowers the resistance of the device, leaving it in a low resistive state (LRS). The conductive filament can be dissolved by applying a negative voltage to the active electrode and thus restoring a high resistance state (HRS). The two different resistance states are used as the logic values 1 or 0 for data storage applications. The overall performance of the device is highly related to the properties of the conductive filament, which has so far not been observed in 3D on scaled devices.

Observation of the conductive filament

The memory device under investigation is a Cu/5nm Al2O3/TiN-based memory, integrated in a one-transistor-one-resistor configuration. The device is placed at the cross-point between the bottom and top electrode. The scalpel C-AFM technique was applied to memory devices programmed in both the low and high resistive state. An in-house fabricated conductive-diamond tip was used for probing and removing the material.

By using the scalpel C-AFM technique, the researchers were able to observe, for the first time ever, the conductive filament formation which is responsible for the resistive switching behavior in CBRAM devices

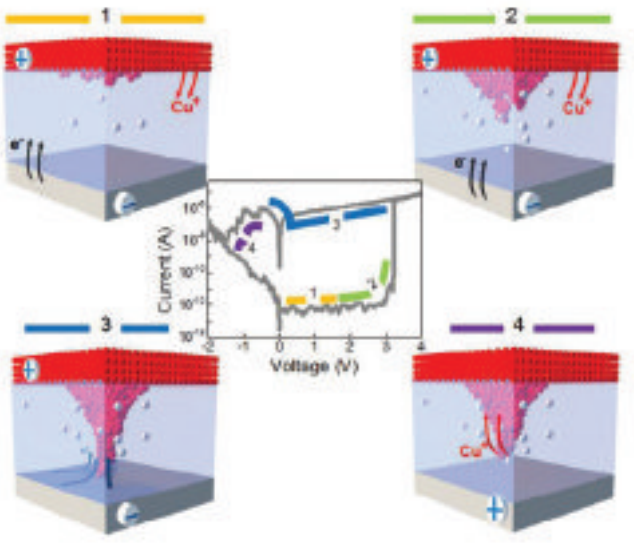

FIGURE 2. filament growth model: Illustration of the eletrochemical processes during resistive switching. (1) First, the Cu oxidizes and Cu+ ions are injected in the Al_2O_3. Second, the high electric field might lead to the formation of oxygen vacancies in the dielectric layers (white balls in the cartoon). (2) The slow migration of Cu+ ions in the switching layer implies that a reduction reaction occurs before the Cu+ reaches the inert-electrode. (3) The conductive filament (CF) growth continues and the CF eventually shorts the two electrodes thereby creating the low resistive state. (4) When the bias is reversed, a Joule-heating assisted electrochemical reaction is responsible for the rupture of the CF in the point of max power dissipation, that is, CF constriction.

(**FIGURE 1**). The observed conductive filament, embedded in the Al_2O_3 oxide, shows a conical shape: it shrinks moving from the active electrode (Cu) towards the inert electrode (TiN). The low resistive state is created when the conductive filament eventually shorts the two electrodes.

The experiments suggest that the dynamics of the conduction filament growth are limited by the mobility of the Cu cations in the electrolyte (**FIGURE 2**). When the bias is reversed, a Joule-heating assisted electrochemical reaction is responsible for the rupture of the conductive filament (the high resistive state).

The study also demonstrates the close correlation between the programming current, the physical volume of the conductive filament and the resistance. A larger programming current induces a larger physical volume and a lower resistance value of the conductive filament. Hence, by controlling the programming current, the resistance can be modulated. This opens the possibility of creating multiple resistance sates in one single memory cell, which can considerably enhance the memory density of non-volatile CBRAM devices.

Scalpel C-AFM will rapidly find applications in other emerging technologies as well. At imec, the technique is currently being used for investigating vertical NAND Flash memory devices and oxide-based RRAM memory devices.

Suggested additional reading

'Three-dimensional observation of the conductive filament in nanoscaled resistive memory devices', U. Celano et al., Nano Letters, 2014. http://pubs.acs.org/doi/abs/10.1021/nl500049g.

'The memory roadmap, a paradigm shift from 2D to 3D', interview with imec's Jan Van Houdt in imec magazine, March issue. http://magazine.imec.be/data/57/reader/reader.html#preferred/1/package/57/pub/63/page/4.

The impact of consumer demand for cutting-edge display technology on the gases market

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How gases are used in the manufacture of displays is being impacted by new technologies, consumer demand, and the burgeoning China market.

While the display market is no longer enjoying double-digit annual growth rates, it is experiencing resurgence due to increasing customer demands for larger flat-panel displays, OLED and 4K technology, ultra-slim form factor, curved and wearable displays, automotive displays, and more. This growth is particularly conspicuous in China, a late comer to the market, which is now the fastest growing region in display manufacturing.

These new technologies and markets require very large quantities of ultra-high purity bulk and electronic specialty gases and a dependable supply chain for these gases. This article will explore the impact of these technologies, consumer demand, and the burgeoning China market on the gases used in the manufacture of display.

Display market

According to IHS DisplaySearch, in 2014 the global display market saw revenue of $134 billion and is expected to grow 6% in 2015. The demand is being driven in large part due to new technologies and new uses for existing display technologies such as 4K, OLED, curved, and flexible displays.

Gases used in display

This love affair that consumers have of interacting with devices large and small not only increases the volume of displays to be manufactured, it also increases the volume of gases needed to make the displays. In the 20 years since the initial development and commercialization of the first Thin Film Transistor (TFT) LCD display panel, the gases market for the display sector has grown to around $450 million.

As shown in **FIGURE 1**, display manufacturing today uses a wide variety of gases, which can be categorized into two types: Electronic specialty gases (ESGs) and Electronic bulk gases (EBGs).

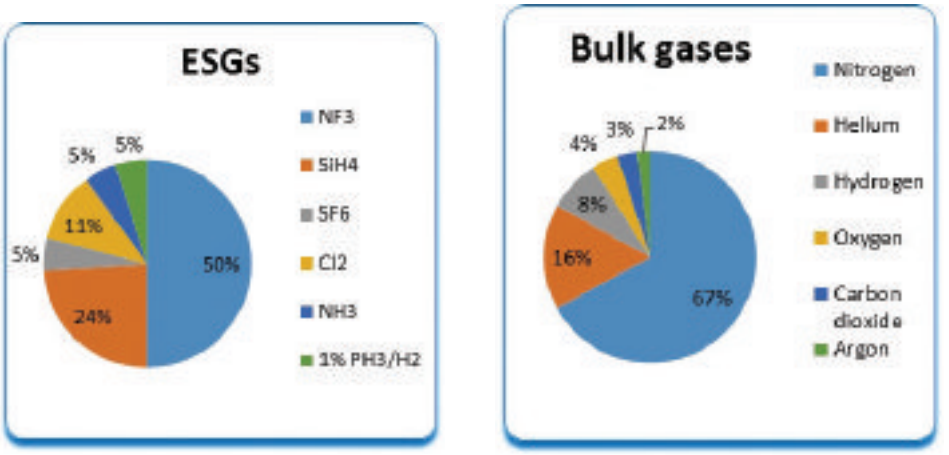

FIGURE 1. Market breakdown for the two types of gases used in display manufacturing.

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TABLE 1.

Gases used in manufacture of display				
	◊ = nominal amount ▾ = less than nominal X = not typically used	a-Si	LTPS	MO
Thin Film	SiH_4 (Silane)	◊	◊	▾
	NH_3 (Ammonia)	◊	▾	▾
	N_2O (Nitrous oxide)	x	◊	◊
	TEOS (Tetraethyl orthosilicate)	◊	◊	▾
Doping	1% B_2H_6/H_2 (Diborane/Hydrogen)	x	◊	x
	15% B_2H_6/H_2 (Diborane/Hydrogen)	x	◊	x
	1% PH_3/H_2 (Phosphine/Hydrogen)	◊	◊	x
	20% PH_3/H_2 (Phosphine/Hydrogen)	◊	◊	x
	1% PH_3/SiH_4 (Phosphine/Silane)	◊	◊	x
Clean	NF_3 (Nitrogen trifluoride)	◊	◊	◊
	F_2 (Fluorine)	◊	◊	◊
Etch	CF_4 (Carbon tetrafluoride)	◊	◊	◊
	C_2HF_5 (Ethyl chloride)	x	◊	x
	SF_6 (Sulfur hexafluoride)	◊	◊	◊
	Cl_2 (Chlorine)	◊	▾	▾
	C_4F_8 (Octafluorocyclobutane)	x	◊	x
	BCl_3 (Boron tricholoride)	◊	▾	▾
Laser	4.5% HCl/1% H_2/Ne (Hydrogen chloride/Hydrogen/Neon)	x	◊	x
	Xe (Xenon)	x	◊	x
	Ne (Neon)	x	◊	x
	5% F_2/He (Fluorine/Helium)	x	◊	x
	Kr (Krypton)	x	◊	x
Bulk	H_2 (Hydrogen)	◊	◊	◊
	O_2 (Oxygen)	◊	◊	◊
	N_2 (Nitrogen)	◊	◊	◊
	He (Helium)	◊	◊	◊
	Ar (Argon)	◊	◊	◊
	Co_2 (Carbon dioxide)	◊	◊	◊

Electronic specialty gases (ESGs)

Silane, nitrogen trifluoride, fluorine (on-site generation), sulfur hexafluoride, ammonia, and phosphine mixtures make up 52% of the gases used in the manufacture of displays and are available in both cylinder and bulk supply.

Of the major countries that manufacture displays, Taiwan and China import most of their ESGs while Korea and Japan have robust domestic production of ESGs.

Silane: SiH_4 is one of the most critical molecules in flat panel manufacturing. Silane is used for deposition of amorphous Si (silicon), the most critical layer in the TFT transistor.

Nitrogen trifluoride: NF_3 is the single largest Electronic Material from spend and volume standpoint for flat panel display (FPD) production. NF_3 is used for cleaning the PECVD (plasma-enhanced chemical vapor deposition). This gas requires scalability to get the cost advantage necessary for the highly competitive market. Over 70% of the global capacity of NF_3 comes from Korea and Japan.

Electronic bulk gases (EBGs)

Nitrogen, hydrogen, helium, oxygen, carbon dioxide, and argon make up 48% of the gases used in the manufacture of displays.

Nitrogen: For a typical large TFT-LCD fab, nitrogen demand can be as high as 30,000 Nm^3/hour so an on-site generator, such as the Linde SPECTRA®-N 30,000, is a cost-effective solution that has the added benefit of an 8% reduction in CO_2 footprint over conventional nitrogen plants.

Helium is used for cooling the glass during and after processing. Manufacturers are looking at ways to decrease the usage of helium because of cost and availability issues due it being a non-renewable gas.

New technologies and implications for gases

Currently about 20% of smartphones – the ones with lower resolution displays – use a-Si display process. Higher resolution devices and new effects such as curved displays require higher performance transistors and improvements in electron mobility. This can be achieved by switching from amorphous silicon (a-Si) transistors to low temperature

TABLE 2.

Transistor type	Electron mobility (m^2/Vs)	Cost	Manufacturing challenges
a-Si	<1	low	low
MO	1-50 (typically 5-10)	low	high
LTPS	50-300	high	medium

polysilicon (LTPS) or metal oxide (MO), also known as transparent amorphous oxide semiconductor (TAOS).

LTPS is used in about 44% of high-end LCD smartphone displays as it has the highest performance. Due to its higher costs and scalability limitations, LTPS is less suited for large screen displays.

Small displays with very high pixel resolution are produced with LTPS. High-definition large displays can be made using MO. Metal oxide semiconductors can remain in an active state longer than traditional LCD and can cut power consumption by up to 90%, which is a huge benefit.

New process requirements

Metal Oxide TFT and LTPS: To meet the changes in technology, N2O, C2HF5, C4F8, BF3, and laser gases are replacing or at least reducing the requirement of NH3, BCl3, and SiH4.

The use of N_2O is expected to double from 5,000 TPA (tons per annum) in 2013 to 10,000 TPA in 2017. Why nitrous oxide? The move from a-Si to MO requires a change in the TFT device structure where the a-Si layers (g-SiNx, a-Si, n+) are being replaced by the MO layers (g-SiOx + indium gallium zinc oxide). This requires a change from NH_3 to high-volume, high-purity N_2O.

LTPS process also uses N_2O for its oxide layer deposition. In addition, LTPS uses XeCl (xenon monochloride) excimer lasers for annealing after the silicon deposition to change the silicon structure to polysilicon. High-performance laser gases, such as Ne, Xe, and Kr from Linde, are well-suited for this process.

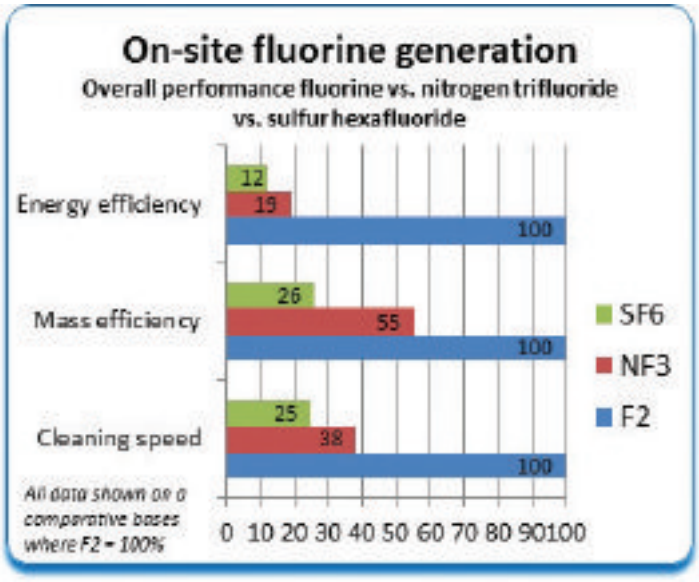

FIGURE 2. Switching to fluorine reduces environmental footprint, material costs cleaning time.

Transparent Conductive Films (TCF) and ITO Replacements: TCFs are used in most high-tech displays and touchscreens, and particularly in displays that are bent or curved. Currently the electronics industry relies primarily on Indium Tin Oxide (ITO) to make electro-conductive films for display. ITO presents challenges: it is brittle and cracks so new TCFs are needed for structural flexibility.

New materials to potentially replace ITO are metal mesh, Ag nanowire (agNW), and carbon nanotube (CNT), which are all highly flexible with comparable transparency and resistance to ITO. Metal mesh is good for large displays, but is restricted on small and medium displays due to its wire width (typically 6 µm). AgNW demonstrates excellent transmittance and flexibility with small wire diameter (20 – 100 nm), but haze is an issue. CNT has excellent conductivity, transmittance, and flexibility, but the supply chain needs to be developed. Single walled carbon nanotubes (SWNT) technology from Linde uses liquid ammonia to produce solubilized carbon nanotubes in the form of inks, which can then be deposited as films and has the added benefit of zero carbon footprint.

F_2 as replacement for NF_3 and SF_6: For a typical large TFT-LCD fab, chamber cleaning gas demand can exceed 300 tons per year. Traditionally NF_3 has been used. The GWP100 (100-year Global Warming Potential) for NF_3 is 17,200; for the replacement F_2, the GWP100 is 0.

Switching to fluorine not only significantly reduces environmental footprint, but also leads to material

cost savings and up to 50% reduction in cleaning time, increasing productivity (**FIGURE 2**).

Fluorine can also be used to replace Sulfur hexafluoride (SF_6), which is used in dielectric etching. The GWP_{100} for SF_6 is 22,800, which surpasses that of NF_3. Significant improvements in etch rate and etch uniformity have been measured with the shift to F_2.

On-site fluorine generation, like that available from Linde, eliminates large-volume, high-pressure storage, and modular generators meet all flow and volume requirements for the largest scale fabs.

The China factor

Currently Korea is the leader in display manufacturing, with Taiwan and China on its heels and Japan a distant fourth (**FIGURE 3**). This is changing, though, as China rapidly gains market share. China, which started in most traditional manufacturing industries as "factory to the world," is a relative late comer in the display sector due to technology barriers.

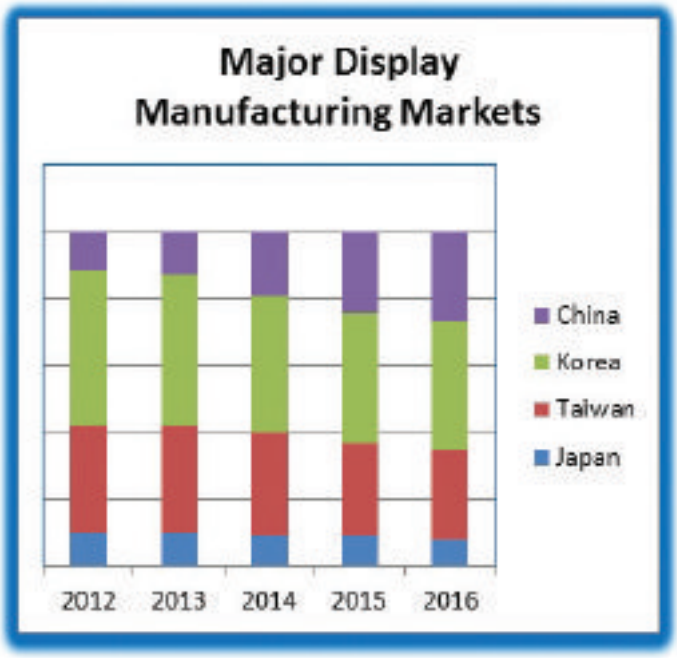

FIGURE 3. Currently Korea is the leader in display manufacturing, with Taiwan and China on its heels and Japan a distant fourth. This is changing, though, as China rapidly gains market share. Source: IHS Displaysearch and Linde Internal.

Currently there are about five major domestic display manufacturers in China; they cater primarily to domestic mobile display and large screen markets. China has been aggressively investing in display fabs over the last five years and has gained market share from other regions.

It is expected that China will account for more than 50% of display capacity investment in the next four years. China capacity is expected to double with aggressive investments especially in the leading technology Low Temperature Polysilicon (LTPS) and Metal Oxide (MO).

Gas supply issues in China

Bulk gases are produced in China, mostly by large international gas companies. There are domestic producers of some ESGs (NH_3, N_2O, and SF_6); other gases currently are mostly imported.

Silane (SiH4): Silane, primarily extracted as an interim process gas during poly silicon production, is one of the most critical molecules in FPD manufacturing. Chinese producers have a very small capacity of silane as they entered the market late. Considering the need for extensive qualification, technical support to achieve that, and the lack of scalable production base, local Chinese poly silicon producers are not able to offer a complete package and thus China still imports more than 80% of its silane and produces locally only 2% of the global capacity of silane.

The current consumption of silane in China display manufacturing is about 300 TPA, which is 7.5% of the global demand, and is expected to double in the next four years. Considering the complexity of the supply chain, import regulations, and storage requirements, companies are actively moving towards local transfilling and analytical capability.

Nitrogen trifluoride (NF3): Similar to silane, the China display manufacturing consumption of NF_3 is expected to double to greater than 2000 TPA in the next four years. Considering the volume used and spend on NF_3 and the rapid expansion of FPD manufacturing in China, more production will be done locally to minimize customs duties and to support domestic sourcing requirements. NF_3 is relatively easy to qualify for chamber cleaning, but ISO supply to

large customers is the biggest challenge since most producers do not have large-scale production and equipped facilities to make NF_3 cost-effective to make. This is a major area of investment for local producers.

LTPS, Metal Oxide, and the Increase in Demand for N_2O: N_2O is a regional and localized product due to its low cost, making long supply chains with high logistic costs unfeasible. Currently, in the region, Korea manufactures about 63% of high-purity N2O, Taiwan about 30%, and China only about 7%. As China leap frogs its display industry into the cutting-edge metal oxide, or LTPS nodes, the demand for N_2O will triple from its current requirement to 3,000 TPA in 2017 with the adoption of LTPS and MO.

Enablers of the growth of the China display industry

The key priorities for materials manufacturers to enable the growth of the China display industry are:

- Commitment to invest in local infrastructures such as on-site bulk gas plants
- Localization of production facilities for high-purity gas and chemical manufacturing
- Collaboration with global materials suppliers for development of new materials

Conclusion

To accommodate the boundless appetite that consumers have for the latest, most innovative, and highest definition displays – both large and small – display manufacturers must partner with gas suppliers to:

- Identify the most appropriate gas and display technology match-up
- Globally source electronic materials to provide customers with stable and cost-effective gas solutions
- Develop local sources of electronic materials
- Improve productivity
- Reduce carbon footprint and increase energy efficiency through on-site gas plants

Going organic: The cost-down route to foldable display manufacture

DR. MICHAEL COWIN, *SmartKem Ltd, St Asaph, Wales*

Organic semiconductors now offers the performance, cost and route to adoption, for foldable displays, from ultra-thin, conformal, wearables to truly foldable smartphones and tablets.

Buoyed by consumer demand for fresh innovation and fierce industry competition, the display industry exists in a cycle of continuous improvement.

Today a new breed of semiconductors – a key enabling component in the evolution of active matrix displays – are competing to offer manufacturers a route to the production of high performance curved, foldable and even roll-able displays.

There are two key factors that define the impact and adoption of any new enabling technology like this; namely how will it perform and what will be the cost.

This article demonstrates that the performance of organic thin-film transistors (OTFT) for display backplane application has reached a tipping point into market adoption. OTFTs are now equal and arguably greater than competitive technology solutions while also offering ultra-flexibility and a significant cost advantage in production and ownership over the more traditional inorganic equivalents. OTFTs are now a serious contender to fill a critical gap in the market for high performance, ultra-flexible TFT backplanes to drive the next generation of conformal displays.

At first, low-temperature polysilicon (LTPS) was considered the most likely solution to replace hydrogenated amorphous silicon (a-Si:H) as the TFT channel layer for rigid flat panel display backplanes, until the advent of indium gallium zinc oxide (IGZO). While the vastly superior mobility of LTPS gave uplift in mobility over traditional a-Si TFT, it came at a price of significantly higher manufacturing costs through high CAPEX, complicated processing and much lower yields, some of which were as low as 20% in early 2014.[1]

However, the recent aggressive drive to manufacture OLED, EPD and LCD display product with new form factors so they are lightweight, conformal or flexible has placed new challenging demands on the TFT material characteristics. This has allowed new technology platforms such as OTFTs to enter into the supply chain to compete head on with LTPS and IGZO as a TFT channel material based on the same metrics of performance and cost.

Electrical performance: It's all about power

While a semiconductor technology's cost of ownership outlines the market entry opportunities, no TFT platform will even be considered a viable alternative to incumbent semiconductors unless it meets, and surpasses key criteria. When defining these criteria it is vital that context to the end application and how this might improve the user experience is considered. Power consumption is one such aspect becoming critical in defining the battery life of mobile and wearable displays and any new TFT channel material, such as OTFT needs to demonstrate either equal or better performance to add value to the user experience in end product form.

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Property	a-Si	LTPS	IGZO	OTFT
VT uniformity	good	fair	fair	good
VT stability	poor	good	poor	good
Leakage Current	poor	poor	good	good
Mobility	1	50-100	10-30	5-10
Mobility Uniformity	good	fair	fair	Good
Device Type	NMOS	CMOS	NMOS	PMOS
Process Complexity	Low	high	low	Low
Flexibility	poor	poor	poor	good
Process Temperature	200-380°C	<450°C	200-350°C	100°C
Cost	fair	poor	fair	good
Yield	good	poor	fair	good

TABLE 1: Thin-film transistor channel material benchmark comparison

The progression from a-Si semiconductors to alternative materials for rigid displays was originally driven by the charge carrier mobility bottleneck, as manufacturers tried to move to higher resolution active matrix LCD displays. The same requirement exists for AMOLED displays, and as such a parallel can be drawn to the arguments for and against the competing materials systems, but with the increasingly important necessity for physical flexibility.

Each semiconductor platform has its own advantages and disadvantages. For instance while LTPS has a very high carrier mobility it could be debated whether it's necessary in the average pixel driver circuit for a high quality LCD or OLED display where a mobility of 5-10 $cm^2/V.s$ is more than adequate. Indeed IGZO and the latest generation of OTFTs meet this requirement with ease. In contrast TFT electrical (bias stress) stability is an issue with IGZO, usually resulting in more complexity in the TFT drive circuitry for each pixel to compensate for this short coming. From a general perspective each of the above mentioned three contenders are more than suitable as a channel semiconductor. However, these options also need to be considered in context; which of these offers the potential to add real uplift in the user experience at a price point the market will accept?

Most displays today are mobile-enabled and are soon to become wearable with the advent of the smartwatch. The power consumption of these displays and its impact on battery life may well be a defining factor in the choice of TFT channel semiconductor for many manufacturers.

An important contribution to this argument was made by Sharp with the introduction to the market of IGZO. Sharp highlighted the importance of TFT leakage current which led to a clearer understanding of the mechanisms responsible for these leakage currents. The causes are found to be predominantly dependent on the smoothness of the interface between the insulator and the channel semiconductor.

So while LTPS has a rough polycrystalline surface its leakage current is higher; IGZO in contrast has smooth amorphous surfaces at this key interface and as such much lower leakage currents.

The context of lower leakage currents is that it will become a very desirable quality since less current is dissipated when the TFT is off and as such the TFT switch capacitor/s can retain an internal charge for a longer period of time. Thus the display refresh rate can be reduced which leads to a potentially dramatic reduction in power consumption – especially for displays that will have static images – ideal for wearable and mobile based displays. As such IGZO has a clear advantage over LTPS for this display based application.

However, recent advances in OTFT technology reported here for the first time show the potential for low leakage currents equivalent IGZO; but achieved using OTFTs.

By designing into solution based organic semiconductor 'inks' the preferred features of the single-crystal organic semiconductor combined with semiconducting polymers or 'binders' an amorphous semiconductor layer can be achieved. This material combination offers the high mobility of single crystals but with highly uniform processing characteristics required for device uniformity. Furthermore, the amorphous nature of these materials offers very smooth interfaces between the solution processed insulator and solution processed semiconductor.

The results in **FIGURE 1** demonstrate that the low leakage current levels achieved by a single gate OTFT. This could be lowered further by use of a dual gate OTFT stack as with commercial IGZO TFTs.

Therefore OTFTs represent serious competition to IGZO as a channel material in the context for application to wearable and mobile displays for extended battery life. Coupled with the further advantages of excellent bias stress stability and low temperature processing, the case for OTFT adoption rather than IGZO becomes more attractive from a performance perspective.

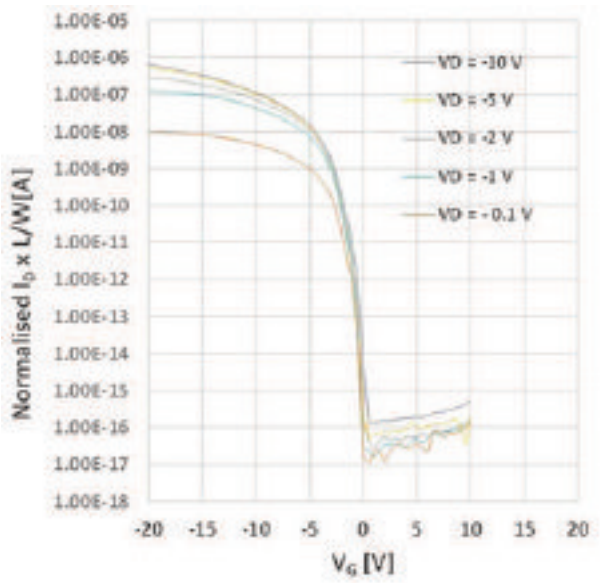

FIGURE 1. TEM of copper hillocks [1].

Physical performance: The foldable frontier

Recently there have been a number of commercial products launched based on curved AMOLED displays such as the Galaxy Round, LG G Flex and Galaxy Note Edge with curved features (and slight flex in the case of the G Flex), all based on LTPS TFT backplanes on plastic. When the user context is taken into account it could be suggested that these products have not offered much value differentiation from glass based equivalent devices.

As such the real 'wow' factor in the consumer experience or user value-add has yet to be achieved. Next generation smart and wearable technology will come with the introduction of flexible and foldable devices such as wearables, smartphones and tablets; but this demands a semiconductor platform with entirely new physical properties and a form factor capability which in turn raises a unique set of challenges for traditional and new TFT technologies to overcome.

The current limiting factor is the inability of LTPS and IGZO technologies to offer robust and acute bend capability in TFT form. Even with the use of exotic and expensive strain management layering techniques the maximum bend radius of these technologies have hit a roadblock at around 5 mm.

To genuinely offer a differentiated product with a compelling value-add proposition to the consumer experience, manufacturers must turn to the use of material technologies that enable truly foldable mobile devices or fully bendable, robust and lightweight smartwatches (**FIGURE 2**). The solution to the limitations presented by LTPS and IGZO in bend capability is the use of OTFTs. It has long been understood that the polymeric nature of OTFTs is ideally suited for bendable applications, and it has widely been reported that products such as Smart-Kem's tru-FLEX® can withstand 10,000 bends below 1mm with minimal effect on device performance. As such OTFT technology is now considered a key enabler for a wide range of highly robust bendable and foldable display based products; and the market timing could not be better with the recent upturn in demand for smartwatch based products.

FIGURE 2: Display form factor dependency on bend radius.

In the context of performance it may be suggested that while the initial market entrants in curved display products have been manufactured with LTPS, and that there is further development potential in the IGZO platform, a complete technology solution already exists – OTFT.

The OTFT technology platform offers the transistor performance for exciting new applications while also holding two 'aces' when it comes to product-specific performance for this new generation of wearable and mobile displays; low leakage for significant battery life extension and ultra-flexibility for foldable mobile devices and bendable smartwatches.

How much will it cost?

Beyond the performance benefits of OTFTs, a commercially viable TFT channel semiconductor must provide favourable characteristics for integration into a robust and cost-effective semiconductor manufacturing process. The savings in manufacturing costs compared with inorganic materials as well as the low risk approach of re-purposing existing a-Si production lines to pilot OTFT backplanes on plastic is an appealing prospect.

One of the major advantages of organic semiconductors comes from their ease of application. Solution based semiconductor inks can be applied to substrates through a range of additive processes and print production systems such as slot dye coating as well as low temperature process (**FIGURE 3**).

Although modern organic semiconductors are stable up to 300oC the ease by which these solution-based materials can be processed at low temperatures offers manufacturers a wide range of cost effective stack materials and substrates, and easier bond/de-bond and inter-layer alignment due to less expansion and contraction. This all adds up to significantly improving production yield (over high temperature processing) and thereby reducing production costs over any area of substrate.

An independent study has been commissioned by SmartKem comparing the cost of key features within the TFT stack that would show the maximum variance between technology platforms;

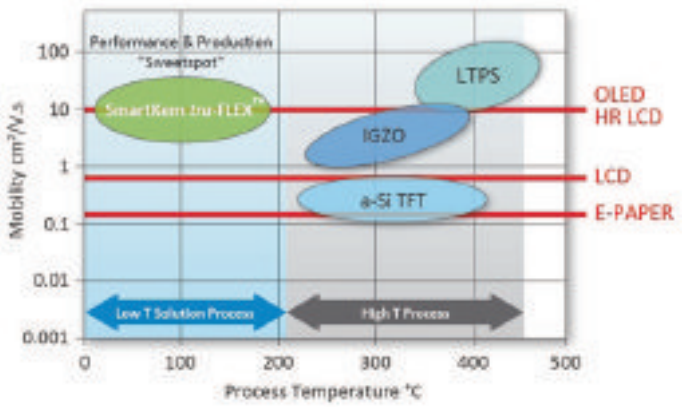

FIGURE 3. Commercial organic semiconductors, such as SmartKem's tru-FLEX® material, offer a total technology solution, combining high performance mobility, low temperature processing and true flexibility.

the semiconductor and gate dielectric layer.

This will ensure a complete understanding of the difference in the cost of ownership and cost of production for the alternate TFT channel materials for backplane manufacture for flexible displays.

The four technology platforms chosen for the TFT array devices were: a-Si, LTPS, IGZO and SmartKem's OTFT semiconductor tru-FLEX®. The overall cost of TFT device manufacture included manufacturing overheads to produce the two layers, depreciation of equipment (amortized over five years of production of 1.8 million substrates) and the direct materials costs.

The CAPEX for each fabrication process is determined from the type and quantity of equipment needed for producing the semiconductor and gate insulator layers with an assumed input capacity of 30,000 substrates per month. In this study, the assumed equipment and materials are shown in Table 2.

Material	Equipment	Size	Materials	Thickness
a-Si	PECVD	(G8)	n+ a-Si:H a-Si:H SiNx	20nm 150nm 350nm
LTPS	PECVD Anneal Excimer-Laser Annealing (ELA) Ion Doping	(G6)	a-Si(Low-H) SiOx	50nm 100nm
IGZO	PECVD Physical vapour deposition (PVD)	(G8)	a-IGZO Low-H SiOx	50nm 300nm
OTFT	Slot Die Coating Drying	(G6, G8)	tru-FLEX® Hyflon®	20nm 300nm

TABLE 2. Details of assumptions for cost analysis

The summary findings of the on-going study have shown the cost of manufacturing TFT arrays with organic semiconductors is almost half that of LTPS and a third lower than a-Si and IGZO. The most significant findings (to be published in a white paper) were that the manufacturing overheads and depreciation costs for OTFT were ten times less than LTPS and four times less than a-Si and IGZO.

It was found that the depreciation cost of production for a 'greenfield' OTFT line is vastly smaller than competing technologies and could be further reduced by the re-purposing of an a-Si production line; OTFTs thus offer an easy route to adoption for the cost-down manufacture of superior performance flexible TFT backplanes.

The future is organic

The value proposition of organic semiconductors now makes sense to an industry eager for differentiated products that can be adopted and scaled with low risk. From a performance and cost perspective the immediate value-add to the consumer is longer battery life and fully foldable mobile displays. While the cost of production is reduced with OTFT, the extremely low cost of ownership offers a low risk industrialization strategy through the building of a 'greenfield' line or by the re-purposing of an existing a-Si line.

One of the most exciting and eagerly awaited outputs of this rapid evolution in material performance and cost is the advancement and commercialization of bendable and foldable displays. From ultra-thin, conformal, wearables to truly foldable smartphones and tablets, organic semiconductors now offers the performance, cost and route to adoption for the manufacture of a new generation of OLED, EPD and LCD displays with entirely new physical properties and form factors.

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Drive profitability through better forecasting

JITESH SHAH, *Integrated Device Technology, San Jose, CA*

Different forecasting algorithms are highlighted and a framework is provided on how best to estimate product demand using a combination of qualitative and quantitative approaches.

Nothing in the world of forecasting is more complex than predicting demand for semiconductors, but this is one business where accurate forecasting could be a matter of long-term survival. Not only will the process of forecasting help reduce costs for the company by holding the right amount of inventory in the channels and knowing what parts to build when but implementing a robust and self-adaptive system will also keep customers happy by providing them with products they need when they need. Other benefits include improved vendor engagements and optimal resource (labor and capital) allocation.

Talking about approaches…

There are two general approaches to forecasting a time-based event; qualitative approach and quantitative or a more numbers-based approach. If historical time-series data on the variable of interest is sketchy or if the event being forecasted is related to a new product launch, a more subjective or expert-based predictive approach is necessary, but we all intuitively know that. New product introductions usually involve active customer and vendor engagements, and that allows us to have better control on what to build, when, and in what quantity. Even with that, the Bass Diffusion Model, a technique geared towards helping to predict sales for a new product category could be employed, but that will not be discussed in this context.

Now if data on past information on the forecasted variable is handy and quantifiable and it's fair to assume that the pattern of the past will likely continue in the future, then a more quant-based, algorithmic and somewhat automated approach is almost a necessity.

But how would one go about deciding whether to use an automated approach to forecasting or a more expert-based approach? A typical semiconductor company's products could be segmented into four quadrants (**FIGURE 1**), and deciding whether to automate the process of forecasting will depend on which quadrant the product fits best.

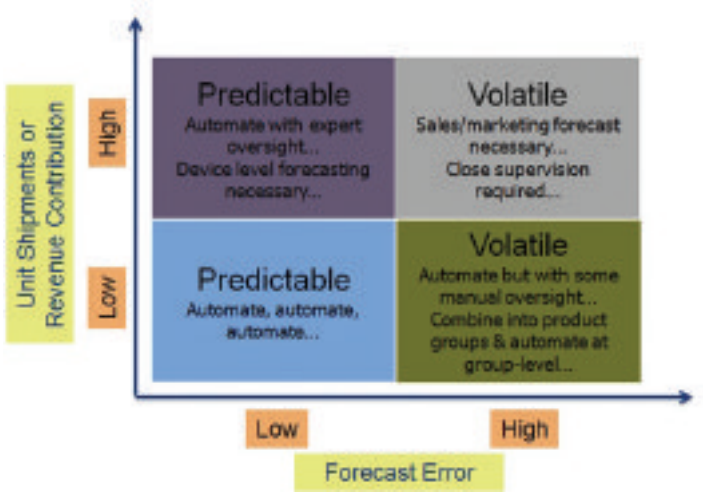

FIGURE 1.

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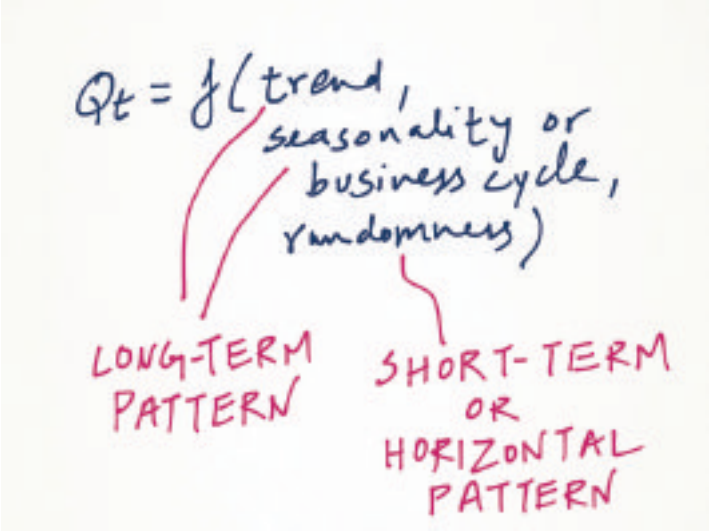

FIGURE 2.

Time series modeling

Past shipment data over time for a product, or a group of products you are trying to forecast demand for is usually readily available, and that is generally the only data you need to design a system to automate the forecasting process. The goal is to discover a pattern in the historical, time-series data and extrapolate that pattern into the future. An ideal system should be built in such a way that it evolves, or self-adapts, and selects the "right" algorithm from the pre-built toolset if shipment pattern changes. A typical time-series forecasting model would have just two variables; an independent time variable and a dependent variable representing an event we are trying to forecast.

That event Qt (order, shipment, etc.) we are trying to forecast is more or less a function of the product's life-cycle or trend, seasonality or business cycle and randomness, shown in the "white board" style illustration of **FIGURE 2**.

Trend and seasonality or business cycle are typically associated with longer-range patterns and hence are best suited to be used to make long-term forecasts. A shorter-term or horizontal pattern of past shipment data is usually random and is used to make shorter-term forecasts.

Forecasting near-term events

Past data exhibiting randomness with horizontal patterns can be reasonably forecasted using either a Naïve method or a simple averaging method. The choice between the two will depend on which one

Week	Actual Sales (x 1k units)	Forecast Sales	Forecast Error	Absolute Forecast Error	Absolute % Error
1	26				
2	23	26	-3	3	0.13
3	28	23	5	5	0.18
4	22	28	-6	6	0.27
5	20	22	-2	2	0.10
6	27	20	7	7	0.26
7	21	27	-6	6	0.29
8	24	21	3	3	0.13
9	28	24	4	4	0.14
10	23	28	-5	5	0.22
				41	1.71

FIGURE 3.

gives lower Mean Absolute Error (MAE) and Mean Absolute % Error (MAPE).

Naïve Method The sample table in **FIGURE 3** shows 10 weeks' worth of sales data. Using the Naïve approach, the forecasted value for the 2nd week is just what was shipped in the 1st week. The forecasted value for the 3rd week is the actual sales value in the 2nd week and so on. The difference between the actual value and the forecasted value represents the forecast error and the absolute value of that is used to calculate the total error. MAE is just the mean of total error. A similar approach is used to calculate MAPE, but now each individual error is divided by the actual sales volume to calculate % error, which are then summed and divided by the number of forecasted values to calculate MAPE.

Averaging Instead of using the last observed

Week	Actual Sales (x 1k units)	Forecast Sales	Forecast Error	Absolute Forecast Error	Absolute % Error
1	26				
2	23	26.00	-3.00	3.00	0.13
3	28	24.50	3.50	3.50	0.13
4	22	25.67	-3.67	3.67	0.17
5	20	24.75	-4.75	4.75	0.24
6	27	23.80	3.20	3.20	0.12
7	21	24.33	-3.33	3.33	0.16
8	24	23.86	0.14	0.14	0.01
9	28	23.88	4.13	4.13	0.15
10	23	24.33	-1.33	1.33	0.06
				27.05	1.15

FIGURE 4.

FIGURE 5.

FIGURE 6.

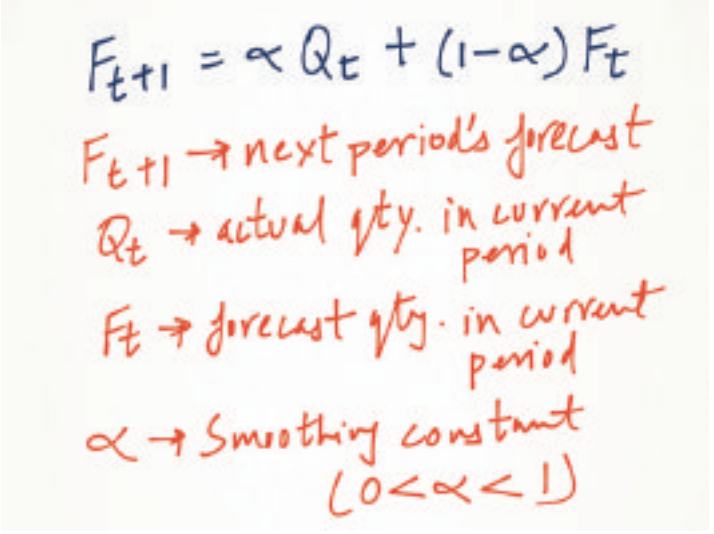

FIGURE 7.

event and using that to forecast the next event, a better approach would be to use the mean of all past observations and use that as the next period's forecast. For example, the forecasted value for the 3rd week is the mean of the 1st and 2nd week's actual sales value. The forecasted value for the 4th week is the mean of the previous three actual sales values, and so on (**FIGURE 4**).

MAE and MAPE for the Naïve method are 4.56 and 19% respectively, and the same for the averaging method are 3.01 and 13% respectively. Right there, one can conclude that averaging is better than the simple Naïve approach.

Horizontal Pattern with Level Shift But what happens when there is a sudden shift (anticipated or not) in the sales pattern like the one shown in **FIGURE 5**?

The simple averaging approach needs to be tweaked to account for that, and that is where a moving average approach is better suited. Instead of averaging across the entire time series, only 2 or 3 or 4 recent time events are used to calculate the forecast value. How many time periods to use will depend on which one gives the smallest MAE and MAPE values and that can and should be parameterized and coded. The tables in **FIGURE 6** compare the two approaches, and clearly the moving average approach seems to be a better fit in predicting future events.

Exponential Smoothing But oftentimes, there is a better approach, especially when the past data exhibits severe and random level shifts. This approach is well suited for such situations because over time, the exponentially weighted moving average of the entire time series tends to deemphasize data that is older but still includes them and, at the same time, weighs recent observations more heavily. That relationship between the actual and forecasted value is shown in **FIGURE 7**.

Again, the lowest MAE and MAPE will help decide the optimal value for the smoothing constant and, as always, this can easily be coded based on the data you already have, and can be automatically updated as new data trickles in.

But based on the smoothing equation above, one must wonder how the entire time series is factored in when only the most recent actual and forecasted

$$F_1 = Q_1$$
$$F_2 = \alpha Q_1 + (1-\alpha) F_1 = Q_1$$
$$F_3 = \alpha Q_2 + (1-\alpha) F_2 = \alpha Q_2 + (1-\alpha) Q_1$$
$$F_4 = \alpha Q_3 + (1-\alpha) F_3 = \alpha Q_3 + \alpha(1-\alpha) Q_2 + (1-\alpha)^2 Q_1$$

FIGURE 8.

FIGURE 9.

FIGURE 10.

values are used as part of the next period's forecast. The math in **FIGURE 8** explains how.

The forecast for the second period is assumed to be the first observed value. The third period is the true derived forecast and with subsequent substitutions, one quickly finds out that the forecast for nth period is a weighted average of all previous observed events. And the weight ascribed to later events compared to the earlier events is shown in the plot in **FIGURE 9**.

Making longer term forecasts

A semiconductor product's lifecycle is usually measured in months but surprisingly, there are quite a few products with lifespans measured in years, especially when the end applications exhibit long and growing adoption cycles. These products not only exhibit shorter-term randomness in time-series but show a longer-term seasonal / cyclical nature with growing or declining trend over the years.

The first step in estimating the forecast over the longer term is to smooth out some of that short-term randomness using the approaches discussed before. The unsmoothed and smoothed curves might resemble the plot in **FIGURE 10**.

Clearly, the data exhibits a long-term trend along with a seasonal or cyclical pattern that repeats every year, and Ordinary Least Square or OLS regression is the ideal approach to forming a function that will help estimate that trend and the parameters involved. But before crunching the numbers, the dataset has to be prepped to include a set of dichotomous variables representing the different intervals in that seasonal behavior. Since in this situation, that seasonality is by quarters representing Q1, Q2, Q3 and Q4, only three of them are included in the model. The fourth one, which is Q=2 in this case, forms the basis upon which to measure the significance of the other three quarters (**FIGURE 11**).

The functional form of the forecasted value by quarter looks something like what's shown in **FIGURE 12**.

The intercept b0 moves up or down based on whether the quarter in question is Q2 or not. If b2, b3 and b4 are positive, Q2 will exhibit the lowest expected sales volume. The other three quarters

Actual Quarterly Sales (x 1k units)	Quarter	Q=1	Q=3	Q=4
327.17	1	1	0	0
288.12	2	0	0	0
332.59	3	0	1	0
394.67	4	0	0	1
392.23	5	1	0	0
345.72	6	0	0	0
399.11	7	0	1	0
473.61	8	0	0	1
470.68	9	1	0	0
414.86	10	0	0	0
478.93	11	0	1	0
568.33	12	0	0	1
564.81	13	1	0	0
497.83	14	0	0	0
574.72	15	0	1	0
682.00	16	0	0	1
677.78	17	1	0	0
597.40	18	0	0	0
689.67	19	0	1	0
818.40	20	0	0	1

FIGURE 11.

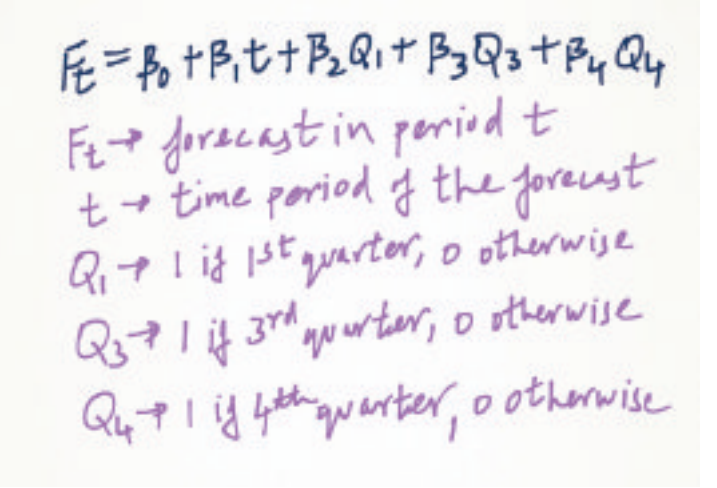

FIGURE 12.

will show increasing expected sales in line with the increase in the respective estimated parameter values. And this equation can be readily used to reasonably forecast an event a few quarters or a few years down the road.

So there you have it. This shows how easy it is to automate some features of the forecasting process, and the importance of building an intelligent, self-aware and adaptive forecasting system. The results will not only reduce cost but help refocus your supply-chain planning efforts on bigger and better challenges. ◆

How emerging IoT impacts the semiconductor sector

PAULA DOE, *SEMI, San Jose, CA*

At Semicon West in July, a big focus will be on how the Internet of Things explosion could potentially impact the semiconductor industry.

In this 50th year anniversary of Moore's Law, the steady scaling of silicon chips' cost and performance that has so changed our world over the last half century is now poised to change it even further through the Internet of Things, in ways we can't yet imagine, suggests Intel VP of IoT Doug Davis, who will give the keynote at SEMICON West (July 14-16) this year. Powerful sensors, processors, and communications now make it possible to bring more intelligent analysis of the greater context to many industrial decisions for potentially significant returns, which will drive the first round of serious adoption of the IoT. But there is also huge potential for adding microprocessor intelligence to all sorts of everyday objects and connecting them with outside information, to solve all sorts of real problems, from saving energy to saving babies' lives (**FIGURE 1**). "We see a big impact on the chip industry," says Davis, noting the needs to deal with highly fragmented markets, as well to reduce power, improve connectivity, and find ways to assure security.

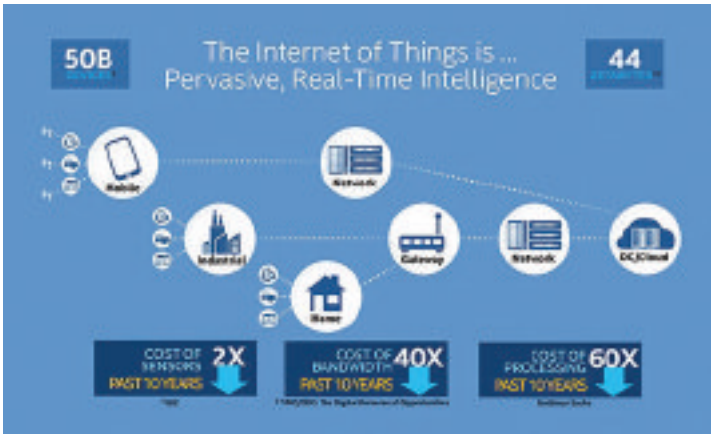

FIGURE 1. There is huge potential for adding microprocessor intelligence to all sorts of everyday objects. Source: Intel, 2015

The end of the era of custom embedded designs?

The IoT may mean the end of the era of embedded chips, argues Paul Brody, IBM's former VP of IoT, who moves to a new job this month, one of the speakers in the SEMICON West TechXPOT program on the impact of the IoT on the semiconductor sector. Originally, custom embedded solutions offered the potential to design just the desired features, at some higher engineering cost, to reduce the total cost of the device as much as possible. Now, however, high volumes of mobile gear and open Android systems have brought the cost of a loaded system on a chip with a dual core processor, a gigabit of DRAM and GPS down to only $10. "The SoC will become so cheap that people won't do custom anymore," says Brody. "They'll just put an SoC in every doorknob and window frame. The custom engineering will increasingly be in the software."

Security of all these connected devices will require re-thinking as well, since securing all the endpoints, down to every light bulb, is essentially impossible, and supposedly trusted parties have turned out not to be so trustworthy after all. "With these SoCs everywhere, the cost of distributed compute power will become zero," he argues, noting that will drive systems towards more distributed processing. One option for security

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then could be a block chain system like that used by Bit Coin, which allows coordination with no central control, and when not all the players are trustworthy. Instead of central coordination, each message is broadcast to all nodes, and approved by the vote of the majority, requiring only that the majority of the points be trustworthy.

While much of the high volume IoT demand may be for relatively standard, low cost chips, the high value opportunity for chip makers may increasingly be in design and engineering services for the expanding universe of customers. "Past waves of growth were driven by computer companies, but as computing goes into everything this time, it will be makers of things like Viking ranges and Herman Miller office furniture who will driving the applications, who will need much more help from their suppliers," he suggests.

Adding context to the data from the tool

The semiconductor industry has long been a leader in connecting things in the factory, from early M2M for remote access for service management and improving overall equipment effectiveness, to the increased automation and software management of 300mm manufacturing, points out Jeremy Read, Applied Materials VP of Manufacturing Services, who'll be speaking in another SEMICON West 2015 program on how the semiconductor sector will use the IoT. But even in today's highly connected fabs, the connections so far are still limited to linking individual elements for dedicated applications specifically targeting a single end, such as process control, yield improvement, scheduling or dispatching. These applications, perhaps best described as intermediate between M2M and IoT, have provided huge value, and have seen enormous growth in complexity. "We have seen fabs holding 50 TB of data at the 45nm node, increasing to 140 TB in 20nm manufacturing," he notes.

Now the full IoT vision is to converge this operational technology (OT) of connected things in the factory with the global enterprise (IT) network, to allow new ways to monitor, search and manage these elements to provide as yet unachievable levels of manufacturing performance. "However, we've learned that just throwing powerful computational resources at terabytes of unstructured data is not effective – we need to understand the shared CONTEXT of the tools, the process physics, and the device/design intent to arrive at meaningful and actionable knowledge," says Read. He notes that for the next step towards an "Internet-of-semiconductor-manufacturing-things" we will need to develop the means to apply new analytical and optimizing applications to both the data and its full manufacturing context, to achieve truly new kinds of understanding.

With comprehensive data and complete context information it will become possible to transform the service capability in a truly radical fashion – customer engineers can use the power of cloud computation and massive data management to arrive at insights into the precise condition of tools, potentially including the ability to predict failures or changes in processing capability. "This does require customers to allow service providers to come fully equipped into the fab – not locking out all use of such capabilities," he says. "If we are to realize the full potential of these opportunities, we must first meet these challenges of security and IP protection."

Besides these programs on the realistic impact of the IoT on the semiconductor manufacturing technology sector, SEMICON West 2015, July 14-16 in San Francisco, will also feature related programs on what's coming next across MEMS, digital health, embedded nonvolatile memory, flexible/hybrid systems, and connected/autonomous cars. ◆

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50 Years of Moore's Law

For 50 years, Moore's Law has served as a guide for technologists everywhere in the world, setting the pace for the semiconductor industry's innovation cycle. Moore's Law has made a tremendous impact not only on the electronics industry, but on our world and our everyday life. It led us from the infancy of the PC era, through the formative years of the internet, to the adolescence of smartphones. Now, with the rise of the Internet of Things, market researchers forecast that in the next 5 years, the number of connected devices per person will more than double, so even after 50 years we don't see Moore's Law slowing down.

As chipmakers work tirelessly to continue device scaling, they are encountering daunting technical and economic hurdles. Increasing complexity is driving the need for new materials and new device architectures. Enabling these innovations and the node-over-node success of Moore's Law requires advancements in precision materials engineering, including precision films, materials removal, materials modification and interface engineering, supported by metrology and inspection.

Though scaling is getting harder, I am confident Moore's Law will continue because equipment suppliers and chipmakers never cease to innovate. As we face the increasing challenges of new technology inflections, earlier engagement in the development cycle between equipment suppliers and chipmakers is required to uncover new solutions. Such early and deep collaboration is critical to delivering complex precision materials engineering solutions on time. In fact, in the mobility era, earlier and deeper collaboration across the entire value chain is essential (applications, system/hardware, fabless, foundry/IDM, equipment supplier, chemical supplier, component supplier, etc.) to accelerate time to market and extend Moore's Law.

"Though scaling is getting harder, I am confident Moore's Law will continue because equipment suppliers and chipmakers never cease to innovate."

Today, new 3D architectures, FinFET and 3D NAND, are enabling the extension of Moore's Law. Dense 3D structures with high aspect ratios create fundamental challenges in device manufacturing. Further, the industry has shifted much of its historical reliance from litho-enabled scaling to materials-enabled scaling, requiring thinner precision films with atomic-scale accuracy. The emphasis on thin conformal films, which can be 2000 times smaller than a human hair, makes it increasingly critical to engineer film properties and manage film interactions between adjacent film surfaces. Selective processing is also a growing requirement, particularly for the deposition and removal of films. We expect more selective applications beyond Epitaxy and Cobalt liner deposition. There will also be a major expansion of new materials in addition to the key inflection of high-k metal gate that helped to reduce power leakage issues associated with scaling.

Gordon Moore's prediction that ignited an industry will continue to influence our way of life through a combination of architecture and material changes. New process designs and new ways to atomically deposit materials are needed. More processes will be integrated on the same platform without vacuum breaks to create pristine interfaces. As an equipment supplier, we have to manage longer R&D cycles to support the industry's roadmap, and plan for faster ramp and yield curves. Of utmost importance is staying close to our customers to ensure we deliver solutions with the desired economic and technical benefits.

Looking at the electronics industry from where it is today out to 2020, many more devices will be in use, the world will be more connected and, particularly in emerging markets, there will be greater consumer appetite for more products with advanced features. Given these transformations and demand, I think the growth and excitement in our industry will continue for many more years, thanks to Moore's Law.

DR. RANDHIR THAKUR, *Executive Vice President, General Manager, Silicon Systems Group,* **APPLIED MATERIALS, INC.**

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