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Solid State TECHNOLOGY

Insights for Electronics Manufacturing

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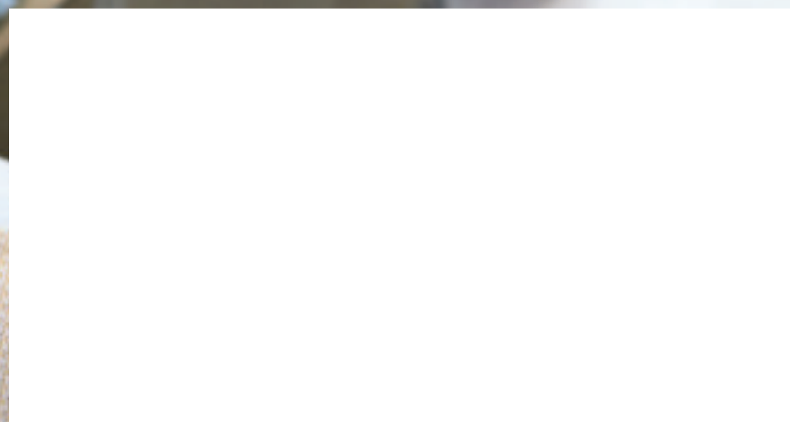

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Engineering illumination system, cleanroom building 4, Veldhoven campus at ASML.

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New roadmap, new strategy

I never thought it would happen, but it's officially the end of the road for The International Technology Roadmap for Semiconductor (ITRS). A final report is coming, but the Semiconductor Industry Association has informed roadmap participant that there will be no funding for ITRS roadmapping efforts moving forward.

Signs of the end were evident last year, when the focus of the ITRS was dramatically changed with a new goal. Instead of being primarily focused on manufacturing challenges that needed to be overcome to enjoy the benefits of continued scaling, the focus in the relabeled "ITRS 2.0" was to start with a system level approach and then figure out what was required at the chip and transistor level.

The good news is that a new roadmap, led by long-time chief ITRS roadmapper Paolo Gargini is underway, sponsored by IEEE, the Institute of Electrical and Electronic Engineers. With the launch of the IRDS program, IEEE is taking the lead in building a comprehensive, end-to-end view of the computing ecosystem, including devices, components, systems, architecture, and software. The Methods of governance, reports, and strategic roadmaps developed by the ITRS and ITRS 2.0 will inform the IRDS within the IEEE-SA IC program.

"Over the past decade, the structure and requirements of the electronics industry have evolved well beyond the semiconductor's industry requirements. In line with the changes in the new electronics ecosystem, the IRDS will build upon the past groundwork and move up a level to identify challenges and include recommendations on possible solutions," said Paolo A. Gargini, IEEE Fellow and chairman, of IRDS. "The IRDS will deliver a 15-year vision that encompasses systems and devices, setting a new direction for the future of the semiconductor, communications, IoE and computer industries."

Participants in the IRDS convened last month at imec in Leuven, Belgium. Over the course of the two-day workshop, the group reviewed the roadmap activities of the Focus Teams (FT) and of the International Technology Working Groups (ITWG) and lay out plans for additional activities in 2016. Some of the fields of discussion include System Integration, Heterogeneous Integration, Connectivity, Future IC Devices and Factory Integration. White papers will be coming soon, and the first report will be out in a year.

—**Pete Singer,** Editor-in-Chief

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Web Exclusives

North America vital to semiconductor manufacturing

North America has a long and rich history of semiconductor manufacturing and innovation. SEMI's Fab Forecast shows that North America accounts for 14 percent of Worldwide Installed Fab capacity.

http://bit.ly/253EquV

IBM keynoter outlines disruptive "Economy of Things" at SEMI's ASMC 2016

Opening keynoter Don O'Toole of IBM's Watson IoT Alliances & Ecosystem Business Development group highlighted the economic implications of the emerging Internet of Things and discussed how cognitive IoT is driving new business models. He pointed to significant macroeconomic impacts as well as disruption and necessary change at the micro/strategic level within all enterprises.

http://bit.ly/1WDgCwU

Packaging materials: Strong growth rates for small form factors

While much of the recent attention has been focused on the growth of wafer level packages (WLPs), specifically fan-out WLPs, this is not the only segment forecast to undergo strong unit growth. In total, IC leadframe shipment growth will trend in the low single-digit range; the growth is entirely attributed to the chip-scale package (CSP) leadframe form factor. Combined, the more traditional IC leadframe segments are expected to experience flat shipments trends, while leadframe CSP shipments continue to growth.

http://bit.ly/1VbOa3w

Roll-to-roll coating: It's a different ball of wax

Manufacturing flexible electronics and coatings for a variety of products has some similarities to semiconductor manufacturing and some substantial differences, principally roll-to-roll fabrication, as opposed to making chips on silicon wafers and other rigid substrates. This interview is with Neil Morrison, senior manager, Roll-to-Roll Coating Products Division, Applied Materials. (From SemiMD.com)

http://bit.ly/1WEIX6c

Intel Q1 revenue, profit rise; Chipmaker will cut up to 12,000 jobs

Intel reported net income of $2.0 billion in the first quarter, up 3 percent from a year earlier, while revenue rose 7 percent to $13.7 billion, compared with $12.8 billion one year ago. (From SemiMD.com)

http://bit.ly/1XCToWO

Rhines expounds on the deconsolidation of the semiconductor industry

"By 2020, we are all going to work for the same company," Wally Rhines, chairman and chief executive officer of Mentor Graphics, said Tuesday morning (April 26) in his keynote presentation at Mentor's U2U user conference in Santa Clara, Calif. (From SemiMD.com)

http://bit.ly/1OC9V60

Insights from the Leading Edge: SMIC ups the ante on packaging

Following the lead of global foundry leader TSMC, SMIC, in two separate moves has put an additional $0.5B into JCET (Jiangsu Changjiang Electronics Technology), mainland China's largest semiconductor packaging assembly and test business, uping their ownership position to $14.25% and making it the biggest shareholder in JCET.

http://bit.ly/22hu34Y

Worldwide semiconductor capital spending to decline 2 percent in 2016

"While the first quarter 2016 forecast has improved from a projected decline of 4.7 percent in the previous quarter's forecast, the 2 percent decline in the market for 2016 is still bleak," said David Christensen, senior research analyst at Gartner. "Excess inventory and weak demand for PCs, tablets, and mobile products continue to plague the semiconductor industry, resulting in a slow growth rate that began in late 2015 and is continuing into 2016."

http://bit.ly/1RbGB6a

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news

worldnews

EUROPE **- The CEA (Atomic Energy Commission)** announced an expanded R&D collaboration with Intel.

ASIA **- Samsung** announced that it has begun mass producing the industry's first 10-nanometer (nm) class, 8-gigabit (Gb) DDR4 (double-data-rate-4) DRAM chips and the modules derived from them.

USA **- ClassOne Technology** announced the completion of a major new round of funding from Salem Investment Partners of Winston-Salem, North Carolina.

EUROPE - At the Quantum Europe conference, **imec** announced that it is ramping-up its R&D activities focused on quantum computing.

USA - Researchers from the **University of Illinois at Urbana-Champaign** have developed a one-step, facile method to pattern graphene by using stencil mask and oxygen plasma reactive-ion etching, and subsequent polymer-free direct transfer to flexible substrates.

EUROPE **- STMicroelectronics** reveals advanced silicon-carbide power devices for hybrid and electric vehicles.

ASIA **- STATS ChipPAC** announced its fan-out wafer level packaging shipments exceeded 1 billion units.

USA **- POET Technologies Inc.** announced that it has signed a definitive agreement to acquire all the shares of BB Photonics Inc.

EUROPE **- Cartamundi, imec** and **Holst Centre** won the "Best Product" - Award at Printed Electronics Europe for their ultra-thin plastic RFID technology integrated into Cartamundi's playing cards.

ASIA **- TowerJazz** began mass production on a new integrated SiGe-based "front-end module on a chip" RF platform for IoT applications.

IBM scientists achieve storage memory breakthrough

For the first time, scientists at IBM Research have demonstrated reliably storing 3 bits of data per cell using a relatively new memory technology known as phase-change memory (PCM).

The current memory landscape spans from venerable DRAM to hard disk drives to ubiquitous flash. But in the last several years PCM has attracted the industry's attention as a potential universal memory technology based on its combination of read/write speed, endurance, non-volatility and density. For example, PCM doesn't lose data when powered off, unlike DRAM, and the technology can endure at least 10 million write cycles, compared to an average flash USB stick, which tops out at 3,000 write cycles.

This research breakthrough provides fast and easy storage to capture the exponential growth of data from mobile devices and the Internet of Things.

Applications

IBM scientists envision standalone PCM as well as hybrid applications, which combine PCM and flash storage together, with PCM as an extremely fast cache. For example, a mobile phone's operating system could be stored in PCM, enabling the phone to launch in a few seconds. In the enterprise space, entire databases could be stored in PCM for blazing fast query processing for time-critical online applications, such as financial transactions.

Continued on page 6

Seven Top-20 semiconductor suppliers show double-digit declines

IC Insights will release its May Update to the 2016 McClean Report later this month. This Update includes a discussion of the 1Q16 semiconductor industry market results, an update of the capital spending forecast by company, a review of the IC market by electronic system type, and a look at the top-25 1Q16 semiconductor suppliers (the top 20 1Q16 semiconductor suppliers are covered in this research bulletin).

1Q16 Top 20 Semiconductor Sales Leaders ($M, Including Foundries)

1Q16 Rank	1Q15 Rank	Company	Headquarters	1Q15 Tot Semi	1Q16 Tot Semi	1Q16/1Q15 % Change
1	1	Intel*	U.S.	12,067	13,115	9%
2	2	Samsung	South Korea	9,336	9,340	0%
3	3	TSMC (1)	Taiwan	6,995	6,122	-12%
4	7	Broadcom Ltd. (2)*	Singapore	3,679	3,550	-4%
5	4	Qualcomm (2)	U.S.	4,434	3,337	-25%
6	5	SK Hynix	South Korea	4,380	3,063	-30%
7	6	Micron	U.S.	4,063	2,930	-28%
8	8	TI	U.S.	2,940	2,804	-5%
9	10	Toshiba	Japan	2,629	2,446	-7%
10	9	NXP*	Europe	2,638	2,224	-16%
11	12	Infineon	Europe	1,666	1,776	7%
12	13	MediaTek (2)	Taiwan	1,506	1,691	12%
13	11	ST	Europe	1,700	1,601	-6%
14	14	Renesas	Japan	1,470	1,415	-4%
15	17	Apple (2)**	U.S.	1,260	1,390	10%
16	15	GlobalFoundries (1)*	U.S.	1,436	1,360	-5%
17	20	Nvidia (2)	U.S.	1,118	1,285	15%
18	16	Sony	Japan	1,272	1,125	-12%
19	18	UMC (1)	Taiwan	1,140	1,034	-9%
20	21	AMD (2)	U.S.	1,030	832	-19%
—	—	Top 20 Total	—	66,745	62,443	-6%

(1) Pure-play foundry (2) Fabless supplier
* Includes Intel/Altera, Avago/Broadcom, NXP/Freescale, and GlobalFoundries/IBM sales for 1Q15 and 1Q16.
**Custom processors for internal use made by TSMC and Samsung foundry services.
Source: Companies, IC Insights' Strategic Reviews Database

The top-20 worldwide semiconductor (IC and O S D—optoelectronic, sensor, and discrete) sales ranking for 1Q16 is shown in Figure 1. It includes eight suppliers headquartered in the U.S., three in Japan, three in Taiwan, three in Europe, two in South Korea, and one in Singapore, a relatively broad representation of geographic regions.

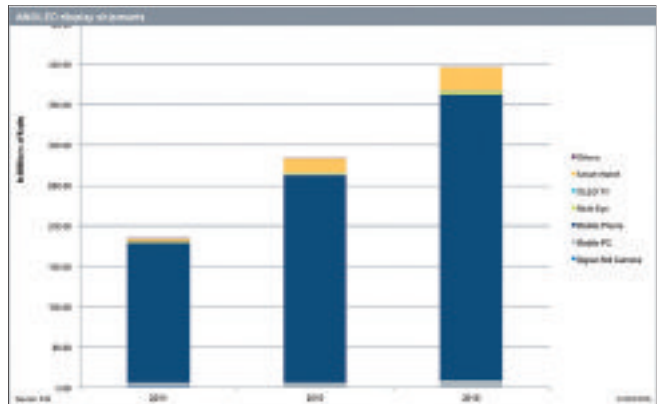
The top-20 ranking includes three pure-play foundries (TSMC, GlobalFoundries, and UMC) and six fabless companies. If the three pure-play foundries were excluded from

Continued on page 8

AMOLED growth is a bright spot for the display industry

Active matrix organic light-emitting diode (AMOLED) displays are rising fast, thanks to lowering costs, wider use in end-market consumer electronics devices and the ramp-up of new manufacturing capacities. While liquid crystal display (LCD) technology is still the dominant technology in the display industry, AMOLED display shipments will grow 40 percent, year over year, to reach 395 million units in 2016. AMOLED display revenue is expected to increase by 25 percent, to reach $15 billion in 2016, according to IHS Inc. (NYSE: IHS), a global source of critical information and insight.

"AMOLED is becoming the shiniest spot in the flat-panel display industry," said David Hsieh, senior director, displays at IHS Technology. "AMOLED has a simpler structure than LCD, as well as a thinner and lighter form factor, better color saturation, greater contrast ratio, faster response time and easier integration with touch functions. In addition, AMOLED is formed on a polymer base substrate, allowing it to be flexible, bendable and even foldable. The organic electro-luminescence materials can be formed using a soluble printing process, which means AMOLED has the potential to be produced at a very low cost."



Many of the obstacles to AMOLED development, such as production inefficiencies, yield-rate management issues, higher investment costs and a short lifetime for light emitting materials, were also resolved in 2015, improving the production. OLED has started to find its niche in many applications, especially in smartphones, smartwatches, automotive displays, home appliances, near-eye

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Imec honors Dr. Gordon Moore with "Lifetime of Innovation Award"

Nanoelectronics research center imec has announced that Dr. Gordon E. Moore, creator of the famous Moore's law theory and co-founder of Intel, is the recipient of its lifetime of innovation award. Imec's annual award recognizes Dr. Moore's visionary view, unrivalled innovation, and his profound impact on the global electronics industry.

In 1965, Dr. Moore predicted that the number of components on an integrated circuit (IC) would double every year for the coming 10 years, thereby making ICs and computer processing simultaneously faster, cheaper, and more powerful. In 1975, Dr. Moore revised the forecast rate to approximately every two years. Moore's law turned out to be incredibly accurate, growing beyond its predictive character to become an industry driver that holds true today, 50 years later. Keeping up with Moore law's progression has required a tremendous amount of engineering and commitment from the global semiconductor industry. While its meaning has evolved over generations, it has had a profound impact in many areas of technological change and progress.

"It is truly an honor to present imec's lifetime innovation award to Dr. Moore, on behalf of all our global partners and our researchers," stated Luc Van den hove, president and CEO of imec. "Dr. Moore's name is synonymous with progress, and his vision has inspired and given direction to the entire semiconductor industry, which has revolutionized the way we compute, communicate, and interact. As the industry upholds this prediction and brings forth new innovations in chip technology, the future of Moore's law will impact such things as healthcare, a sustainable climate, and safer transport all for the better."

Dr. Moore began his career at Johns Hopkins University. He cofounded Fairchild Semiconductor in 1957 and launched Intel in 1968 together with Robert Noyce and Andy Grove. Today, Intel is a world leader in the design and manufacturing of integrated circuits and is the largest semiconductor company. Dr. Moore served as Intel CEO from 1975-1987, and then became its chairman of the board until his retirement in 1997.

"Although Moore's law was created more than 50 years ago, it remains extremely valid and serves as a guide to what we innovate at imec," continued Van den hove. "Throughout our organizations' 32-year existence, we've worked at enabling Moore's law and helping our partners innovate and develop the modern technology that society has embraced and demands. Dr. Moore's legacy continues to be our mission and we are privileged to honor him."

Imec's Lifetime of Innovation award was awarded to Dr. Moore on May 24, 2016 at its annual ITF Brussels, the flagship of imec's worldwide ITF events. ◈

***IBM scientists**, Continued from page 4*

Machine learning algorithms using large datasets will also see a speed boost by reducing the latency overhead when reading the data between iterations.

How PCM Works

PCM materials exhibit two stable states, the amorphous (without a clearly defined structure) and crystalline (with structure) phases, of low and high electrical conductivity, respectively.

To store a '0' or a '1', known as bits, on a PCM cell, a high or medium electrical current is applied to the material. A '0' can be programmed to be written in the amorphous phase or a '1' in the crystalline phase, or vice versa. Then to read the bit back, a low voltage is applied. This is how re-writable Blue-ray Discs* store videos.

Previously scientists at IBM and other institutes have successfully demonstrated the ability to store 1 bit per cell in PCM, but today at the IEEE International Memory Workshop in Paris, IBM scientists are presenting, for the first time, successfully storing 3 bits per cell in a 64k-cell array at elevated temperatures and after 1 million endurance cycles.

"Phase change memory is the first instantiation of a universal memory with properties of both DRAM and flash, thus answering one of the grand challenges of our industry," said Dr. Haris Pozidis, an author of the paper and the manager of non-volatile memory research at IBM Research – Zurich. "Reaching 3 bits per cell is a significant milestone because at this density the cost of PCM will be significantly less than DRAM and closer to flash."

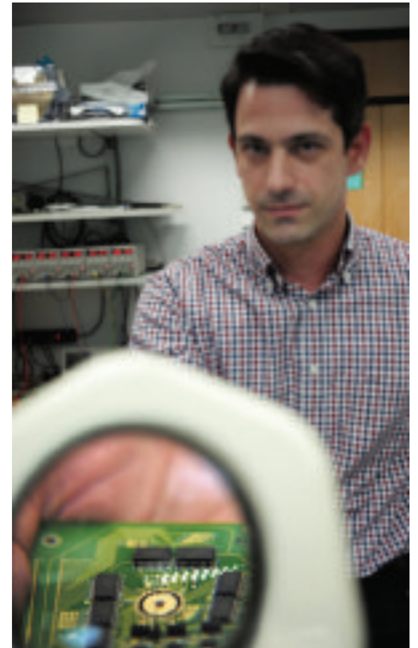
To achieve multi-bit storage IBM scientists have developed two innovative enabling technologies: a set of drift-immune cell-state metrics and drift-tolerant coding and detection schemes.

More specifically, the new cell-state metrics measure a physical property of the PCM cell that remains stable over time, and are thus insensitive to drift, which affects the stability of the cell's electrical conductivity with time. To provide additional robustness of the stored data in a cell over ambient temperature fluctuations a novel coding and detection scheme is employed. This scheme adaptively modifies the level thresholds that are used to detect the cell's stored data so that they follow variations due to temperature change. As a result, the cell state can be read reliably over long time periods after the memory is programmed, thus offering non-volatility.

"Combined these advancements address the key challenges of multi-bit PCM, including drift, variability, temperature sensitivity and endurance cycling," said Dr. Evangelos Eleftheriou, IBM Fellow.

The experimental multi-bit PCM chip used by IBM scientists is connected to a standard integrated circuit board. The chip consists of a 2 × 2 Mcell array with a 4- bank interleaved architecture. The memory array size is 2 × 1000 μm × 800 μm. The PCM cells are based on doped-chalcogenide alloy and were integrated into the prototype chip serving as a characterization vehicle in 90 nm CMOS baseline technology.

OpenPOWER



At the 2016 OpenPOWER Summit in San Jose, CA, last month, IBM scientists demonstrated, for the first time, phase-change memory attached to POWER8-based servers (made by IBM and TYAN® Computer Corp.) via the CAPI (Coherent Accelerator Processor Interface) protocol. This technology leverages the low latency and small access granularity of PCM, the efficiency of the OpenPOWER architecture and the CAPI protocol. In the demonstration the scientists measured very low and consistent latency for 128-byte read/writes between the PCM chips and the POWER8 processor. ◈

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Seven Top-20, *Continued from page 4*

the top-20 ranking, U.S.-based IDM ON Semiconductor ($817 million), China-based fabless supplier HiSilicon ($810 million), and Japan-based IDM Sharp ($800 million) would have been ranked in the 18th, 19th, and 20th positions, respectively.

IC Insights includes foundries in the top-20 semiconductor supplier ranking since it has always viewed the ranking as a top supplier list, not a marketshare ranking, and realizes that in some cases the semiconductor sales are double counted. With many of our clients being vendors to the semiconductor industry (supplying equipment, chemicals, gases, etc.), excluding large IC manufacturers like the foundries would leave significant "holes" in the list of top semiconductor suppliers. As shown in the listing, the foundries and fabless companies are identified. In the April Update to The McClean Report, marketshare rankings of IC suppliers by product type were presented and foundries were excluded from these listings.

Overall, the top-20 list shown in Figure 1 is provided as a guideline to identify which companies are the leading semiconductor suppliers, whether they are IDMs, fabless companies, or foundries.

In total, the top-20 semiconductor companies' sales declined by 6% in 1Q16/1Q15, one point less than the total worldwide semiconductor industry decline of 7%. Although, in total, the top-20 1Q16 semiconductor companies registered a moderate 6% drop, there were seven companies that displayed a double-digit 1Q16/1Q15 decline and three that registered a ≥25% fall (with memory giants Micron and SK Hynix posting the worst results). Half of the top-20 companies had sales of at least $2.0 billion in 1Q16. As shown, it took $832 million in quarterly sales just to make it into the 1Q16 top-20 semiconductor supplier list.

There was one new entrant into the top-20 ranking in 1Q16—U.S.-based fabless supplier AMD. AMD had a particularly rough 1Q16 and saw its sales drop 19% year-over-year to $832 million, which was about half the $1,589 million in sales the company logged just over two years ago in 4Q13. Although AMD did not have a good 1Q16, Japan-based Sharp, the only company that fell from the top-20 ranking, faired even worse with its 1Q16/1Q15 sales plunging by 30%!

In order to allow for more useful year-over-year comparisons, acquired/merged semiconductor company sales results were combined for both 1Q15 and 1Q16, regardless of when the acquisition or merger occurred. For example, although Intel's acquisition of Altera did not close until late December of 2015, Altera's 1Q15 sales ($435 million) were added to Intel's 1Q15 sales ($11,632 million) to come up with the $12,067 million shown in Figure 1 for Intel's 1Q15 sales. The same method was used to calculate the 1Q15 sales for Broadcom Ltd. (Avago/Broadcom), NXP (NXP/Freescale), and GlobalFoundries (GlobalFoundries/IBM).

Apple is an anomaly in the top-20 ranking with regards to major semiconductor suppliers. The company designs and uses its processors only in its own products—there are no sales of the company's MPUs to other system makers. Apple's custom ARM-based SoC processors had a "sales value" of $1,390 million in 1Q16, up 10% from $1,260 million in 1Q15. Apple's MPUs have been used in 13 iPhone handset designs since 2007 and a dozen iPad tablet models since 2010 as well as in iPod portable media players, smartwatches, and Apple TV units. Apple's custom processors—such as the 64-bit A9 used in iPhone 6s and 6s Plus handsets introduced in September 2015 and the new iPhone 6SE launched in March 2016—are made by pure-play foundry TSMC and IDM foundry Samsung.

Intel remained firmly in control of the number one spot in 1Q16. In fact, it increased its lead over Samsung's semiconductor sales from 29% in 1Q15 to 40% in 1Q16. The biggest moves in the ranking were made by the new Broadcom Ltd. (Avago/Broadcom) and Nvidia, each of which jumped up three positions in 1Q16 as compared to 1Q15.

As would be expected, given the possible acquisitions and mergers that could/will occur this year (e.g., Microchip/Atmel), as well as any new ones that may develop, the top-20 semiconductor ranking is likely to undergo a significant amount of upheaval over the next few years as the semiconductor industry continues along its path to maturity. ◈

AMOLED growth, *Continued from page 5*

virtual reality (VR) devices and televisions. "Improvements in production and lowering costs are attracting more device makers to install AMOLED displays in their products," Hsieh said.

For example, Samsung Electronics has been using AMOLED as an important differentiator in its proprietary Galaxy smartphones. Since the second half of 2015, more smartphone brands — especially manufacturers in China — have installed AMOLED displays in their devices, such as Google, Microsoft, Meizhu, Blackberry, Huawei, HTC, ZTE, Oppo and Coolpad. The 5-inch high-definition (HD), 5.5-inch full high definition (FHD), 5.5-inch and 6-inch wide quad high definition (WQHD) will be the major AMOLED smartphone display driving forces in 2016.

AMOLED penetration in smartphone displays is expected to rise from 17 percent in 2015 to 21 percent this year. Apple is reported to be considering AMOLED as a display source for its new iPhone in late 2017, replacing the current low-temperature polysilicon (LTPS)

thin-film transistor (TFT) LCD display. "If Apple actually starts using AMOLED displays, the transition will be viewed as a milestone in flexible form factor development," Hsieh said.

According to the IHS OLED Display Market Tracker, OLED TV shipments will further expand in 2016, thanks to process improvements and production efficiency enhancements, as well as improvements in organic light emitting materials layers. In fact, LG Display is already expanding its AMOLED TV panels to 65 inches with ultra-high definition (UHD), which will bring AMOLED into the high-end TV segment. IHS expects OLED TV display shipments will grow 125 percent, year over year, to reach 900,000 units in 2016.

Tablet and notebook PCs is another important venue for AMOLED, for its slim and light form factor, and high resolution. We expect to see 8-inch and 9.7-inch quad extended graphics array (QXGA) displays and 12-inch AMOLED panels begin to emerge in the mobile PC arena this year. Many PC brands are planning to use AMOLED in notebook PCs and two-in-one convertible mobile PC models beginning in 2016. AMOLED mobile PC panels are expected to grow 63 percent year over year, to reach to 8.6 million units in 2016.

AMOLED is also leading other display technologies when it comes to response time and power consumption, which is extremely useful in near-eye display devices, including VR and augmented reality (AR) devices. AMOLED display and OLED on silicon projection displays, which are both used in near-eye displays are forecast to grow 119 percent, year over year, to reach 3.6 million units in 2016.

"The central information display in cars will also feature AMOLED within the next couple of years," Hsieh said, "AMOLED displays provide features that are useful in automotive display applications, because of their high contrast ratio, flexible and curved form factors as well as better color gamut. Aside from these applications, AMOLED also presents great opportunities for industrial applications, home appliances, digital signage and broadcasting."

AMOLED, as a rapidly emerging display technology, will be a key theme in the coming SID Display Week 2016 Business Track, which is co-organized by IHS and the Society for Information Display. For more information, visit SID Display Week. ◆

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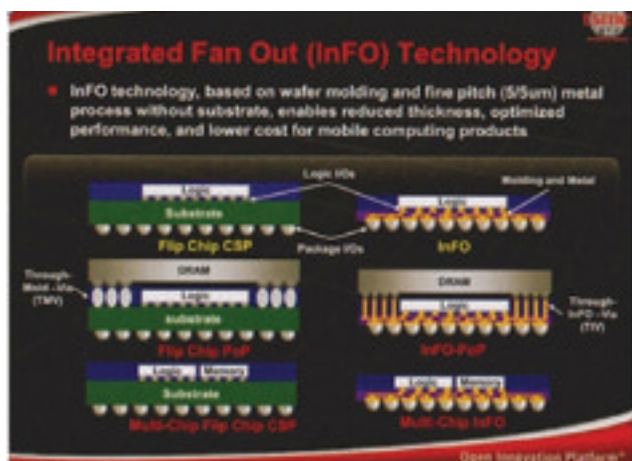
Will packaging make the difference for TSMC?

PHIL GARROU,
Contributing Editor

Earlier this year, a Taipei Times headline read "New packaging may spur TSMC growth" adding that despite its weak revenue growth guidance for this quarter, TSMC, might see stronger growth from next quarter thanks to its InFO (integrated fan out) packaging technology (see FIGURE).

The Times reports that InFO could help TSMC beat rival Samsung and win more A10 application processor orders from Apple, because the technology offers "...lower costs, higher speed and thinner form factor when compared to conventional flip chip packaging." TSMC is preparing a complete InFO portfolio aimed at different package sizes and applications. In a conference call with investors in April, TSMC CEO C.C. Wei stated that they have almost completed equipment installation and expect to complete customer product qualification shortly. They plan to ship volume production shortly. Estimates are that the revenue contribution from InFO packaging could total US$300 million this year.



I have previously reported that TSMC had purchased a facility in Longtan, Taiwan (from Qualcomm for $85MM) and was turning it into a facility devoted to the manufacturing of integrated fan-out wafer-level packaging (InFO-WLP) technology.

Apple is expected to unveil its new iPhone in the second half of this year. Daiwa Capital Markets analysts estimates that Apple's order split for A9 processors (last generation) was 45% for TSMC and 55% for Samsung, but projects TSMC could take more than 50% of the A10 processor business, due in part to the superior packaging technology now being offered by TSMC. Other smartphone chip vendors are reportedly looking at adopting TSMC InFO packaging technology in the near future.

I have also previously reported that TSMC lost the chance for making Apple A3 processors to Samsung because it lacked the capability to package and test the chips.

YSIC (Yuanta Securities Investment Consulting) claims the InFO technology is at least 20 percent cheaper than flip chip packaging. YSIC notes that "... it is becoming more difficult to solely rely on front-end tech node migration to drive better performance and cost," a statement that should be very familiar to readers of this column.

In 2014, I discussed TSMCs announced ambition of becoming a major player in full back-end packaging services with their plans to ramp IC packaging revenues to US $1 billion in 2015 and $2B in 2016 Based on this roadmap, TSMC would become the 3rd leading packaging company in Taiwan by 2016, trailing only ASE and SPIL. ◆

Packaging

CoolCube 3D transistor stacking improves

ED KORCZYNSKI,
Sr. Technical Editor

CEA-Leti in France has been developing monolithic transistor stacking based on laser re-crystallization of active silicon in upper layers called "CoolCube" (TM). Leading mobile chip supplier Qualcomm has been working with Leti on CoolCube R&D since late 2013 and based on preliminary results have opted to continue collaborating with the goal of building a complete ecosystem that takes the technology from design to fabrication.

"The Qualcomm Technologies and Leti teams have demonstrated the potential of this technology for designing and fabricating high-density and high-performance chips for mobile devices," said Karim Arabi, vice president of engineering, Qualcomm Technologies, Inc. "We are optimistic that this technology could address some of the technology scaling issues and this is why we are extending our collaboration with Leti." As part of the collaboration, Qualcomm Technologies and Leti are sharing the technology through flexible, multi-party collaboration programs to accelerate adoption.

Process step	Planar technology		Top FET process	
Dopant activation	Thermal activation	>1000°C spike	Solid Phase Epitaxy (SPE)	600°C 30s
			Nanosecond laser anneal (λ=308nm, 150ns)	<700°C, 100ns
Epitaxy	Si ($SiCl_2$+HCl)	750°C, min	Si Cyclic Deposition Etch Growth Si_2H_6 Etch : HCl + GeH_4	600°C, min
	SiGe ($SiCl_2$+GeH_4+HCl)	650°C, min	SiGe Deposition Etch Growth Si_2H_6 +GeH_4 Etch : HCl + GeH_4	500°C, min
Offset nitride spacer	ALD	600°C, h	Low k dielectrics	500°C, min
Substrate bonding	NA	NA	SOI bonding and substrate etch	200°C, h
			SMART CUT ™	200°C, h 400°C, 1h

Table: Critical thermal budget steps summary in a planar FDSOI integration and CoolCube process for top FET in 3DVLSI. (Source: VLSI Symposium 2015)

Olivier Faynot, micro-electronic component section manager of CEA-Leti, in an exclusive interview with Solid State Technology and SemiMD explained, "Today we have a strong focus on CMOS over CMOS integration, and this is the primary integration that we are pushing. What we see today is the integration of NMOS over PMOS is interesting and suitable for new material incorporation such as III-V and germanium."

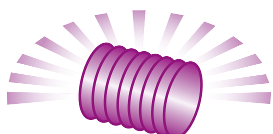
The Table shows that CMOS over CMOS integration has met transistor performance goals with low-temperature processes, such that the top transistors have at least 90% of the performance compared to the bottom. Faynot says that recent results for transistors are meeting specification, while there is still work to be done on inter-tier metal connections. For advanced ICs there is a lot of interconnect routing congestion around the contacts and the metal-1 level, so inter-tier connection (formerly termed the more generic "local interconnect") levels are needed to route some gates at the bottom level for connection to the top level.

"The main focus now is on the thermal budget for the integration of the inter-tier level," explained Faynot. "To do this, we are not just working on the processing but also working closely with the designers. For example, depending on the material chosen for the metal inter-tier there will be different limits on the metal link lengths." Tungsten is relatively more stable than copper, but with higher electrical resistance for inherently lower limits on line lengths. Additional details on such process-design co-dependencies will be disclosed during the 2016 VLSI Technology Symposium, chaired by Raj Jammy.

When the industry decides to integrate III-V and Ge alternate-channel materials in CMOS, the different processing conditions for each should make NMOS over PMOS CoolCube a relatively easy performance extension. "Three-fives and germanium are basically materials with low thermal budgets, so they would be most compatible with CoolCube processing," reminded Faynot. "To me, this kind of technology would be very interesting for mobile applications, because it would achieve a circuit where the length of the wires would be shortened. We would expect to save in area, and have less of a trade-off between power-consumption and speed."

"This is a new wave that CoolCube is creating and it has been possible thanks to the interest and support of Qualcomm Technologies, which is pushing the technological development in a good direction and sending a strong signal to the microelectronics community," said Leti CEO Marie Semeria. "Together, we aim to build a complete ecosystem with foundries, equipment suppliers, and EDA and design houses to assemble all the pieces of the puzzle and move the technology into the product-qualification phase." ◆

Semiconductors



EUVL: Taking it down to 5nm

DEBRA VOGLER, *SEMI, San Jose, CA*

At Semicon West, a team of experts will tackle the status of advanced lithography options that can get the industry from node 10 to node 5.

The semiconductor industry is nothing if not persistent — it's been working away at developing extreme ultraviolet lithography (EUVL) for many years. Though its production insertion target has slipped over the years, some say that the industry is getting closer to its introduction at the 5nm node. But it's also true that some may be hedging their bets.

Whatever camp you fall into, the discussion is sure to be lively as a team of experts tackles the status of advanced lithography options that can get the industry from node 10 to node 5 (session "Lithography: Charting a Path, or Paths, between Nodes 10 and 5", part of the Advanced Manufacturing Forum) at SEMICON West 2016 (July 12, 10:30am-12:30pm). Confirmed speakers for this event include Robert Aitken (ARM), Stephen Renwick (Nikon Research Corporation of America), Ben Rathsack (TEL), Mike Lercel (ASML), Mark Slezak (JSR Micro, Inc.), and Harry Levinson (GLOBALFOUNDRIES). The session will be moderated by Lithoguru's Chris Mack. SEMI interviewed some of the session speakers to get a preview of the issues most likely to be addressed.

Equipment status

Mike Lercel, director of product marketing at ASML, told SEMI that his company is very confident that EUVL will be ready for next-generation nodes, having demonstrated progress on the NXE:3350B, which is intended for volume production: achieving 1,368 wafers per day at the ASML factory, and excellent imaging and overlay performance at >80W. He further noted that the company's logic customers will take EUV into production in 2018-2019, so it needs to ship in volume a year before — likewise for DRAM. "We believe that EUV is cost-competitive around 1,500 good wafers per day, but the crossover point may be lower depending on the customer and the application."

Having already achieved the productivity milestone of 1,368 wafers per day makes EUVL cost-competitive or break-even for many applications, said Lercel, primarily because multiple patterning is becoming too difficult and EUV is needed to reduce this complexity. "Additionally, we've exposed more than 300,000 wafers on multiple NXE:3300 scanners at customer sites and that has accelerated our rates of learning. A 125W EUV source setting has been qualified and is ready for field rollout, and we demonstrated 200W source power at ASML." He also noted that the company has a robust EUVL product roadmap, including a high-NA EUV scanner, which will take it into the next decade and beyond. "As long as the industry continues to scale and we are not close to reaching devices' physical limits, there will be a need for EUV."

Lercel acknowledged that EUVL productivity must continue to be improved and throughput is closely connected to source power and tool reliability. "We've derived new understandings from plasma modeling and computational lithography that have enabled us to significantly increase our conversion efficiency," said Lercel. "This was a key contributing factor in our latest 200W achievement and builds confidence in our ability to reach 250W by the end of the year, which is the source power required for 1,500 wafers per day."

Materials and infrastructure for EUVL

There are still a number of challenges remaining for the infrastructure needed to support EUVL. Among them are actinic inspections for blanks and resists. "Deposition tools and post-pellicle mask inspection must catch up to support EUVL," said Lercel, who told SEMI that notable progress has already been made on E-beam mask inspection high-volume manufacturing (HVM) tools and on an actinic blank inspection tool development program led by the EUVL Infrastructure Development Center (EIDEC).

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In other developments reported by Lercel, Zeiss is working on an AIMS tool for defect disposition; and at imec's EUV Resist Manufacturing & Qualification Center (EUV RMQC), the industry-wide manufacturing infrastructure and quality control capabilities needed to take EUVL into HVM are being finalized. Other R&D efforts are continuing to improve EUV blank quality process and yield — defects are now reaching single digits said Lercel. ASML is also in the process of commercializing a pellicle. Significant gaps still exist with respect to a blank multi-layer deposition tool that needs to have improved defect results. "Multiple deposition techniques are being evaluated to define the HVM tool approach," said Lercel. "And post-pellicle mask inspection (APMI) is not on timeline for insertion," so the industry needs other options.

Regarding EUVL resists, Mark Slezak, executive vice-president, at JSR Micro, Inc., told SEMI that short-term, the materials industry is continuing to evolve and improve chemically amplified systems that are allowing technical requirements to be met at 7nm (see **FIGURE 1** for examples of recent performance data). "Longer term, the industry is focused on new alternative approaches to chemically amplified systems with a variety of techniques, including molecular resists, nano-particles, and advanced sensitizers," said Slezak, who will also present at SEMICON West 2016. "Additionally, in the case of both 193i and EUV, the material industry is working on post-development solutions, such as chemical shrink, pattern collapse mitigation, and combinations with DSA (directed self-assembly) that enable further imaging extensions."

As a company, JSR Micro is preparing to provide scaled-up EUV materials in a HVM setting, including advanced quality control, as early as the end of 2016, Slezak told SEMI. "However, we see that the most likely insertion point for significant volumes is in the 2018 time period."

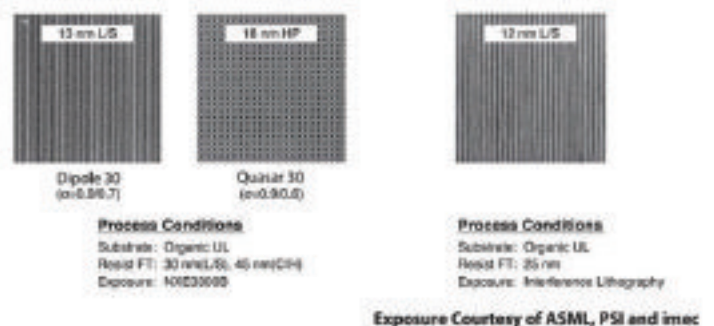

FIGURE 1. Examples of recent progress in patterning materials. Courtesy: ASML, PSI, and imec

Overall outlook

Chris Mack summed up the industry's current dilemma with respect to EUVL and getting from node 10 to node 5. "The whole idea of continuing on the Moore's Law progression is to reduce the cost of a transistor by shrinking it," Mack told SEMI. "We've seen a flattening of the cost/transistor trends over time lately, and I think there are some serious questions as to whether or not any specific new technology node from 10nm on will actually result in a lower cost/transistor — and if it doesn't, there won't be much motivation for designs to migrate to these nodes."

Mack further observed that the cost of lithography already accounts for more than 50% of the cost of making a chip, and possibly even as high as 70% depending on the design. "As those costs escalate with each node, we worry that the cost savings won't be enough to compensate for the higher design costs." Citing conventional wisdom, Mack noted that the rule-of-thumb with respect to the break-even point for deciding to use EUVL is that it has to be able to cost-effectively replace three 193nm immersion steps (or masks). While there are a lot of assumptions that go into the cost-of-ownership models, Mack explained that if throughput levels can get to around 60-90wph, that would make one EUV layer cost-competitive with three 193nm immersion exposures. "I think most people agree that EUV would then be worthwhile to do. The hope is to be able to do that at the 5nm node."

Aside from the actual technical challenges that remain to be solved before EUVL can be inserted into HVM, the major hurdle is time. "People are planning the 7nm logic node right now," said Mack, "and no one is willing to commit to EUV for 7nm because it's not ready." He further explained that TSMC has said publicly it plans to exercise EUV in parallel with 193i manufacturing for the 7nm node and then implement EUV in manufacturing at the 5nm node. That would place it at around the 2020 time frame. "If EUV hits its schedule between now and 2018/2019, then we may see TSMC commit to using EUV at 5nm." Conversely, if the EUV schedule slips and is still too risky to implement, then when 2019 comes around, it could very well be that EUVL will be pushed out even further. "Because foundries have to accept design rules about two years before manufacturing begins, and because the design rules for multiple-patterning 193 immersion are very different from single-patterning EUV, TSMC and other foundries will have to make their call about two years from now."

For DRAM, Mack says there is still a desire for EUV to be successful, but the window is rapidly disappearing. "We might see more chip stacking as a solution going forward for DRAM," said Mack, but "then we could see 193nm immersion SADP (single immersion double-patterning) for 20nm DRAM." Below 20nm DRAM, If EUV isn't ready, Mack says that chip stacking would be the solution, which leaves EUV for logic, primarily at 5nm.

"Here's where an interesting phenomenon happens," Mack told SEMI. "The classic view of Moore's Law — a doubling of the number of components on a chip every two years — has been carrying on for over 50 years. Current trends are redefining the meaning of Moore's Law (**FIGURE 2**)."

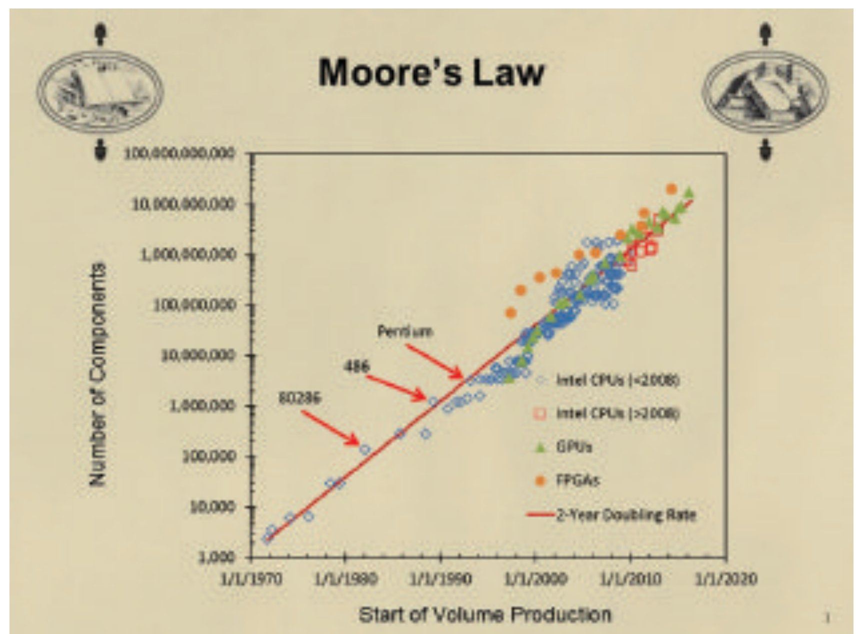

FIGURE 2. Moore's Law trend. Courtesy: Chris Mack

The industry is seeing a slow-down in, i.e., 3-year cycles instead of 2-year cycles. "If that trend continues and EUV is late, that would give some breathing room for EUV to catch up. So it might be ready in time for the 5nm node."

These speakers and more will present at SEMICON West 2016 (July 12-14) in San Francisco, Calif. The new SEMICON West offers eight forums: Extended Supply Chain, Advanced Manufacturing Chain Forum, Advanced Packaging Forum, Test Forum, Sustainable Manufacturing Forum, Silicon Innovation Forum, Flexible Hybrid Electronics Forum, and World of IoT Forum.

Process Watch: Yield management turns green

DAVID W. PRICE, **DOUGLAS G. SUTHERLAND** *and* **KARA L. SHERMAN**

As IC manufacturers look for more creative ways to reduce environmental impact, they are turning to advanced process control solutions to reduce scrap and rework.

As we celebrate Earth Day 2016, we commend the efforts of companies who have found ways to reduce their environmental impact. In the semiconductor industry, fabs have been building Leadership in Energy and Environmental Design (LEED)-certified buildings [1] as part of new fab construction and are working with suppliers to directly reduce the resources used in fabs on a daily basis.

As IC manufacturers look for more creative ways to reduce environmental impact, they are turning to advanced process control solutions to reduce scrap and rework, thereby reducing fab resource consumption. Specifically, fabs are upgrading process control solutions to be more capable and adding additional process control steps; both actions reduce scrap and net resource consumption per good die out (**FIGURE 1**).

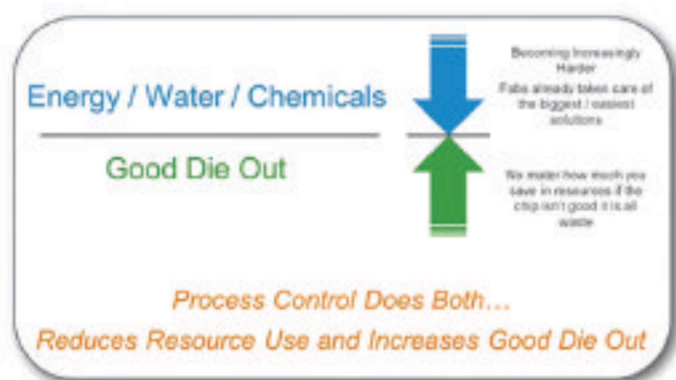

FIGURE 1. The basic equation for improving a fab's environmental performance includes reducing resource use and increasing yield. Capable process control solutions help fabs do both by identifying process issues early thereby reducing scrap and rework.

Improved process control performance

Process control is used to identify manufacturing excur-

DR. DAVID W. PRICE, DR. DOUGLAS SUTHERLAND, and **MS. KARA L. SHERMAN** are Senior Director, Principal Scientist, and Director, respectively, at KLA-Tencor Corp. Over the last 10 years, this team has worked directly with more than 50 semiconductor IC manufacturers to help them optimize their overall inspection strategy to achieve the lowest total cost.

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sions, providing the data necessary for IC engineers to make production wafer dispositioning decisions and to take the corrective actions required to fix process issues.

For example, if after-develop inspection (ADI) data indicate a high number of bridging defects on patterned wafers following a lithography patterning step, the lithography engineer can take several corrective actions. In addition to sending the affected wafers back through the litho cell for rework, the engineer will stop production through the litho cell to fix the underlying process issue causing the yield-critical bridging defects. This quick corrective action limits the amount of material impacted and potentially scrapped.

To be effective, however, the quality of the process control measurement is critical. If an inspection or metrology tool has a lower capture rate or higher total measurement uncertainty (TMU), it can erroneously flag an excursion (false alarm), sending wafers for unnecessary rework, causing additional consumption of energy and chemicals and production of additional waste. Alternatively, if the measurement fails to identify a true process excursion, the yield of the product is negatively impacted and more dies are scrapped—again, resulting in less desirable environmental performance.

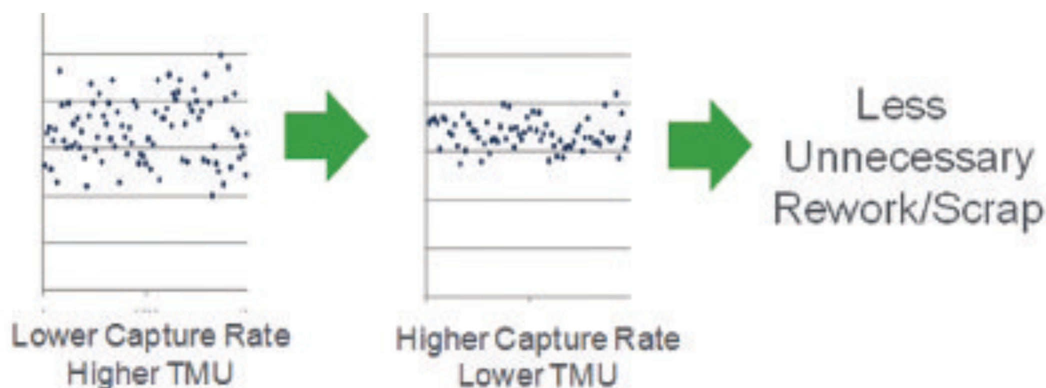

FIGURE 2. Higher quality process control tools produce better process control data within the lithography cell, enabling a 0.1 percent reduction in unnecessary rework that results in better environmental performance.

The example shown in **FIGURE 2** examines the environmental impact of the process control data produced by two different metrology tools in the lithography cell. By implementing a higher quality metrology tool, the quality of the process control data is improved and the lithography engineers are able to make better process decisions resulting in a 0.1 percent reduction in unnecessary rework in the litho cell. This reduced rework results in a savings of approximately 0.5 million kWh of power and 2.4 million liters of water for a 100k WSPM fab—and a proportional percentage reduction in the amount of resist and clean chemicals consumed.

As a result of obtaining increased yield and reduced scrap, many fabs have upgraded the capability of their process control systems. To drive further improvements in environmental performance, fabs can benefit from utilizing the data generated by these capable process control systems in new ways.

Traditionally, the data generated by metrology systems have been utilized in feedback loops. For example, advanced overlay metrology systems identify patterning errors and feed information back to the lithography module and scanner to improve the patterning of future lots. These feedback loops have been developed and optimized for many design nodes. However, it can also be useful to feed forward (**FIGURE 3**) the metrology data to one or more of the upcoming processing steps [2]. By adjusting the processing system to account for known variations of an upcoming lot, errors that could result in wafer scrap are reduced.

For example, patterned wafer geometry measurement systems can measure wafer shape after processes such as etch and CMP and the resulting data can be fed back to help improve these processes. But the resulting wafer shape data can also be fed forward to the scanner to improve patterning [3-5]. Likewise, reticle registration metrology data can be used to monitor the outgoing quality of reticles from the mask shop, but it can also be fed forward to the scanner to help reduce reticle-related sources of patterning errors. Utilizing an intelligent combination of feedforward and feedback control loops, in conjunction with fab-wide, comprehensive metrology measurements, can help fabs reduce variation and ultimately obtain better processing results, helping reduce rework and scrap.

Earlier excursion detection reduces waste

Fabs are also reducing process excursions by adding process control steps. **FIGURE 4** shows two examples

FIGURE 3. Multiple data loops to help optimize fab-wide processes. Existing feedback loops (blue) have existed for several design nodes and detect and compensate for process variations. New, optimized feedback loops (green) provide earlier detection of process changes. Innovative feed forward loops (orange) utilize metrology systems to measure variations at the source, then feed that data forward to subsequent process steps.

of deploying an inspection tool in a production fab. In the first case (left), inspection points are set such that a lot is inspected at the beginning and end of a module, with four process steps in between. If a process excursion that results in yield loss occurs immediately after the first inspection, the wafers will undergo multiple processing steps, and many lots will be mis-processed before the excursion is detected. In the second case (right), inspection points are set with just two process steps in between. The process excursion occurring after the first inspection point is detected two days sooner, resulting in much faster time-to-corrective action and significantly less yield loss and material wasted.

Furthermore, in Case 1, the process tools at four process steps must be taken off-line; in Case 2, only half as many

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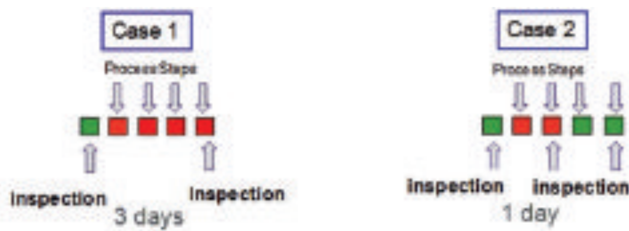

FIGURE 4. Adding an additional inspection point to the line will reduce the material at risk should an excursion occur after the first process step.

process tools must be taken offline. This two-day delta in detection of a process excursion in a 100k WSPM fab with a 10 percent yield impact results in a savings of approximately 0.3 million kWh of power, 3.7K liters of water and 3500 kg of waste. While these environmental benefits were obtained by sampling more process steps, earlier excursion detection and improved environmental performance can also be obtained by sampling more sites on the wafer, sampling more wafers per lot, or sampling more lots. When a careful analysis of the risks and associated costs of yield loss is balanced with the costs of additional sampling, an optimal sampling strategy has been attained [6-7].

Conclusion

As semiconductor manufacturers focus more on their environmental performance, yield management serves as a critical tool to help reduce a fab's environmental impact. Fabs can obtain several environmental benefits by implementing higher quality process control tools, combinations of feedback and feedforward control loops, optimal process control sampling, and faster cycles of learning. A comprehensive process control solution not only helps IC manufacturers improve yield, but also reduces scrap and rework, reducing the fab's overall impact on the environment.

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Author's Note: The Process Watch series explores key concepts about process control—defect inspection and metrology—for the semiconductor industry. Following the previous installments, which explored the 10 fundamental truths of process control, this new series of articles highlights additional trends in process control, including successful implementation strategies and the benefits for IC manufacturing. For this article, we are pleased to include insights from our guest author, Kara Sherman. ◈

IoT demands: Are we ready?

ED KORCZYNSKI, *senior technical editor*

Leading companies within critical industry segments answer questions about the state of technology preparedness for the Internet-of-Things.

The Internet-of-Things (IoT) is expected to add new sensing and communications to improve the functionality of all manner of things in the world: bridges sensing and reporting when repairs are needed, parts automatically informing where they are in storage and transport, human health monitoring, etc. Solid-state and semiconducting materials for new integrated circuits (IC) intended for ubiquitous IoT applications will have to be assembled at low-cost and small-size in High Volume Manufacturing (HVM). Micro-Electro-Mechanical Systems (MEMS) and other sensors are being combined with Radio-Frequency (RF) ICs in miniaturized packages for the first wave of growth in major sub-markets.

To meet the anticipated needs of the different IoT application spaces, we asked leading companies within critical industry segments about the state of technology preparedness:

- Commercial IC HVM - GLOBALFOUNDRIES,
- Electronic Design Automation (EDA) - Cadence and Mentor Graphics,
- IC and complex system test - Presto Engineering.

Korczynski: Today, ICs for IoT applications typically use 45nm/65nm-node which are "Node -3" (N-3) compared to sub-20nm-node chips in HVM. Five years from now, when the bleeding-edge will use 10nm node technology, will IoT chips still use N-3 of 28nm-node (considered a "long-lived node") or will 45nm-node remain the likely sweet-spot of price:performance?

Timothy Dry, product marketing manager, GLOBALFOUNDRIES

In five years' time, there will be a spread of technology solutions addressing low, middle, and high ends of IoT applications. At the low end, IoT end nodes for applications like connected smoke detectors, security sensors will be at 55, 40nm ULP and ULL for lowest system power, and low cost. These applications will be typically served by MCUs <50DMIPs. Integrated radios (BLE, 802.15.4), security, Power Management Unit (PMU), and eFlash or MRAM will be common features. Connected LED lighting is forecasted to be a high volume IoT application. The LED drivers will use BCD extensions of 130nm—40nm—that can also support the radio and protocol-MCU with Flash.

In the mid-range, applications like smart-meters and fitness/medical monitoring will need systems that have more processing power <300DMIPS. These products will be

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implemented in 40nm, 28nm and GLOBALFOUNDRIES' new 22nm FDSOI technology that uses software-controlled body-biasing to tune SoC operation for lowest dynamic power. Multiple wireless (BLE/802.15.4, WiFi, LPWAN) and wired connectivity (Ethernet, PLC) protocols with security will be integrated for gateway products.

High-end products like smart-watches, learning thermostats, home security/monitoring cameras, and drones will require MPU-class IC products (~2000DMIPs) and run high-order operating systems (e.g. Linux, Android). These products will be made in leading-edge nodes starting at 22FDX, 14FF and migrating to 7FF and beyond. Design for lowest dynamic power for longest battery life will be the key driver, and these products typically require human machine Interface (HMI) with animated graphics on a high resolution displays. Connectivity will include BLE, WiFi and cellular with strong security.

Steve Carlson, product management group director, Cadence

We have seen recent announcements of IoT targeted devices at 14nm. The value created by Moore's Law integration should hold, and with that, there will be inherent advantages to those who leverage next generation process nodes. Still, other product categories may reach functionality saturation points where there is simply no more value obtained by adding more capability. We anticipate that there will be more "live" process nodes than ever in history.

Jon Lanson, vice president worldwide sales & marketing, Presto Engineering

It is fair to say that most IoT devices will be a heterogeneous aggregation of analog functions rather than high power digital processors. Therefore, and by similarity with Bluetooth and RFID devices, 90nm and 65nm will remain the mainstream nodes for many sub-vertical markets, enabling the integration of RF and analog front-end functions with digital gate density. By default, sensors will stay out of the monolithic path for both design and cost reasons. The best answer would be that the IoT ASIC will follow eventually the same scaling as the MCU products, with embedded non-volatile memories, which today is 55-40nm centric and will move to 28nm with industry maturity and volumes.

Korczynski: If most IoT devices will include some manner of sensor which must be integrated with CMOS logic and memory, then do we need new capabilities in EDA-flows and burn-in/test protocols to ensure meeting time-to-market goals?

Nicolas Williams, product marketing manager, Mentor Graphics

If we define a typical IoT device as a product that contains a MEMS sensor, A/D, digital processing, and a RF-connection to the internet, we can see that the fundamental challenge of IoT design is that teams working on this product need to master the analog, digital, MEMS, and RF domains. Often, these four domains require different experience and knowledge and sometimes design in these domains is accomplished by separate teams. IoT design requires that all four domains are designed and work together, especially if they are going on the same die. Even if the components are targeting separate dice that will be bonded together, they still need to work together during the layout and verification process. Therefore, a unified design flow is required.

Stephen Pateras, product marketing director, Mentor Graphics

Being able to quickly debug and create test patterns for various embedded sensor IP can be addressed with the adoption of the new IEEE 1687 IP plug-and-play standard. If a sensor IP block's digital interface adheres to the standard, then any vendor-provided data required to initialize or operate the embedded sensor can be easily and quickly mapped to chip pins. Data sequences for multiple sensor IP blocks can also be merged to create optimized sequences that will minimize debug and test times.

Jon Lanson, vice president worldwide sales & marketing, Presto Engineering

From a testing standpoint, widely used ATEs are generally focused on a few purposes, but don't necessarily cover all elements in a system. We think that IoT devices are likely to require complex testing flows using multiple ATEs to assure adequate coverage. This is likely to prevail for some time as short run volumes characteristic of IoT demands are unlikely to drive ATE suppliers to invest R&D dollars in creating new purpose-built machines.

Korczynski: For the EDA of IoT devices, can all sensors be modeled as analog inputs within established flows or do we need new modeling capability at the circuit level?

Steve Carlson, product management group director, Cadence

Typically, the interface to the physical world has been partitioned at the electrical boundary. But as more mechanical and electro-mechanical sensors are more

deeply integrated, there has been growing value in co-design, co-analysis, and co-optimization. We should see more multi-domain analysis over time.

Nicolas Williams, product marketing manager, Mentor Graphics

Designers of IoT devices that contain MEMS sensors need quality models in order to simulate their behavior under physical conditions such as motion and temperature. Unlike CMOS IC design, there are few standardized MEMS models for system-level simulation. State of the art MEMS modeling requires automatic generation of behavioral models based on the results of Finite Element Analysis (FEA) using reduced-order modeling (ROM). ROM is a numerical methodology that reduces the analysis results to create Verilog-A models for use in AMS simulations for co-simulation of the MEMS device in the context of the IoT system.

Korczynski: For test of IoT devices which may use ultra-low threshold voltage transistors, what changes are needed compared to logic test of a typical "low-power" chip?

Steve Carlson, product management group director, Cadence

Susceptibility to process corners and operating conditions becomes heightened at near-threshold voltage levels. This translates into either more conservative design sign-off criteria, or the need for higher levels of manufacturing screening/tests. Either way, it has an impact on cost, be it hidden by over-design, or overtly through more costly qualification and test processes.

Jon Lanson, vice president worldwide sales & marketing, Presto Engineering

We need to make sure that the testability has also been designed to be functional structurally in this mode. In addition, sub-threshold voltage operation must account for non-linear transistor characteristics and the strong

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impact of local process variation, for which the conventional testability arsenal is still very poor. Automotive screening used low voltage operation (VLV) to detect latent defects, but at very low voltage close to the transistor threshold, digital becomes analog, and therefore if the usual concept still works for defect detection, functional test and @speed tests require additional expertise to be both meaningful and efficient from a test coverage perspective.

Korczynski: Do we have sufficient specifications within "5G" to handle IoT device interoperability for all market segments?

Rajeev Rajan, Vice President of Internet of Things (IoT) at GLOBALFOUNDRIES

The estimated timeline for standardization availability of 5G is around 2020. 5G is being designed keeping three classes of applications in mind: Enhanced Mobile Broadband, Massive IoT, and Mission-Critical Control. Specifically for IoT, the focus is on efficient, low-cost communication with deep coverage. We will start to see early 5G technologies start to appear around 2018, and device connectivity,

interoperability and marshaling the data they generate that can apply to multiple IoT sub-segments and markets is still very much in development.

Korczynski: Will the 1st-generation of IoT devices likely include wide varieties of solution for different market-segments such as industrial vs. retail vs. consumer, or will most device use similar form-factors and underlying technologies?

Rajeev Rajan, Vice President of Internet of Things (IoT) at GLOBALFOUNDRIES

If we use CES 2016 as a showcase, we are seeing IoT "Things" that are becoming use-case or application-centric as they apply to specific sub-segments such as Connected Home, Automotive, Medical, Security, etc. There is definitely more variety on the consumer front vs. industrial. Vendors / OEMs / System houses are differentiating at the user-interface design and form-factor levels while the "under-the-hood" IC capabilities and component technologies that provide the atomic intelligence are fairly common.

Steve Carlson, product management group director, Cadence

Right now it seems like everyone is swinging for the fence. Everyone wants the home-run product that will reach a billion devices sold. Generality generally leads to sub-optimality, so a single device usually fails to meet the needs and expectations of many. Devices that are optimized for more specific use cases and elements of purchasing criteria will win out. The question of interface is an interesting one.

Korczynski: Will there be different product life-cycles for different IoT market-segments, such as 1-3 years for consumer but 5-10 years for industrial?

Rajeev Rajan, Vice President of Internet of Things (IoT) at GLOBALFOUNDRIES

That certainly seems to be the case. According to Gartner's market analysis for IoT, Consumer is expected to grow at a faster pace in terms of units compared to Enterprise, while Enterprise is expected to lead in revenue. Also the churn-cycle in Consumer is higher / faster compared to Enterprise. Today's wearables or smart-phones are good reference examples. This will however vary by the type of "Thing" and sub-segment. For example, you expect to have your smart refrigerator for a longer time period compared to smart clothing or eyewear. As ASPs of the "Things" come down over time and new classes of products such as disposables hit the market, we can expect even larger volumes.

Jon Lanson, vice president worldwide sales & marketing, Presto Engineering

The market segments continue to be driven by the same use cases. In consumer wearables, short cycles are linked to fashion trends and rapid obsolescence, where consumer home use has longer cycles closer to industrial market requirements. We believe that the lifecycle norms will hold true for IoT devices.

Korczynski: For the IoT application of infrastructure monitoring (e.g. bridges, pipelines, etc.) long-term (10-20 year) reliability will be essential, while consumer applications may be best served by 3-5 year reliability devices which cost less; how well can we quantify the trade-off between cost and chip reliability?

Steve Carlson, product management group director, Cadence

Conceptually we know very well how to make devices more reliable. We can lower current densities with bigger wires, we can run at cooler temperatures, and so on. The difficulty is always in finding optimality for a given criterion across the, for practical purposes, infinite tradeoffs to be made.

Korczynski: Why is the talk of IoT not just another "Dot Com" hype cycle?

Rajeev Rajan, Vice President of Internet of Things (IoT) at GLOBALFOUNDRIES

I participated in a panel at SEMICON China in Shanghai last month that discussed a similar question. If we think of IoT as a "brand new thing" (no pun intended), then we can think of it as hype. However if we look at the IoT as as set of use-cases that can take advantage of an evolution of Machine-to-Machine (M2M) going towards broader connectivity, huge amounts of data generated and exchanged, and a generational increase in internet and communication network bandwidths (i.e. 5G), then it seems a more down-to-earth technological progression.

Nicolas Williams, product marketing manager, Mentor Graphics

Unlike the Dot Com hype, which was built upon hope and dreams of future solutions that may or may not have been based in reality, IoT is real business. For example, in a 2016 IC Insights report, we see that last year $63.4 billion in revenue was generated for IoT systems and the market is growing at about 20% CAGR. This same report also shows IoT semiconductor sales of over $15 billion in 2015 with a CAGR of 21.1%.

Jon Lanson, vice president worldwide sales & marketing, Presto Engineering

It is the investment needed up front to create sensing agents and an infrastructure for the hardware foundation of the IoT that will lead to big data and ultimately value creation.

Steve Carlson, product management group director, Cadence

There will be plenty of hype cycles for products and product categories along the way. However, the foundational shift of the connection of things is a diode through which civilization will only pass through in one direction. ◈

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The Symposium on VLSI Technology: Technical highlights

Papers that address the theme "Inflections for a Smart Society" are highlighted.

The 2016 Symposium on VLSI Technology is part of a premiere international conference that defines the pace, progress and evolution of microelectronics, scheduled from June 13-16, 2016 in Honolulu, Hawaii and held in conjunction with the Symposium on VLSI Circuits (June 14-17, 2016). The Symposia's overall theme "Inflections for a Smart Society," reflects the industry's transition point as "smart" system level applications help to transform the industry.

Samsung Electronics will present a 10nm logic technology developed using 3rd generation Si FinFETs for low power, high performance applications, demonstrating a speed improvement of 27% with a 40% reduction in power compared to 14nm process, achieved with multi-threshold voltage devices and reduced contact resistance (**FIGURE 1**). Overcoming process challenges such as multiple patterning, high aspect ratio etching, niche gate replacements, and advanced isolation, the authors demonstrated yield analysis of a 0.04μm2 SRAM with 128Mb cell size and observed a static noise margin of 190mV at 0.75V.

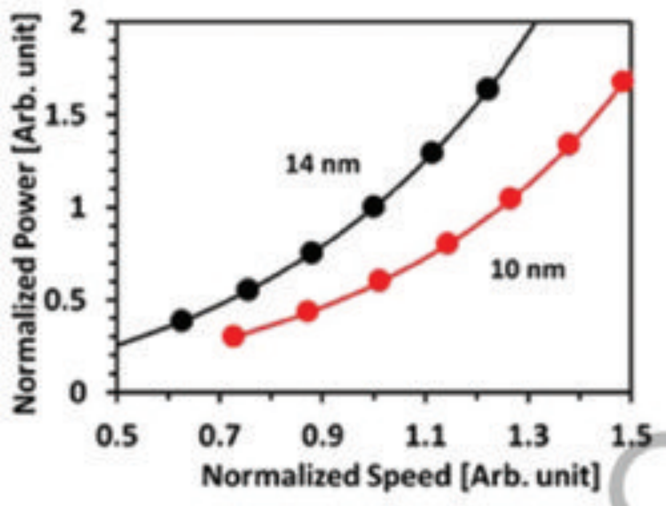

FIGURE 1. "Si FinFET-based 10nm Technology with Multi Vt Gate Stack for Low Power and High Performance Applications," Cho et al., Samsung Electronics.

TSMC will demonstrate a fully functional 32Mb 6-T high density SRAM with smallest reported size of sub-0.03μm2 using bulk CMOS FinFETs scaled beyond the 10nm node (**FIGURE 2**). This presentation also reports improved transistor performance and electrostatic control through process and CET optimization of scaled FinFETs with competitive performance: DIBL of <45mV/V, sub-threshold swing of <65mV/decade, and static noise margin of ~90mV for the high density SRAM operated at 0.45V.

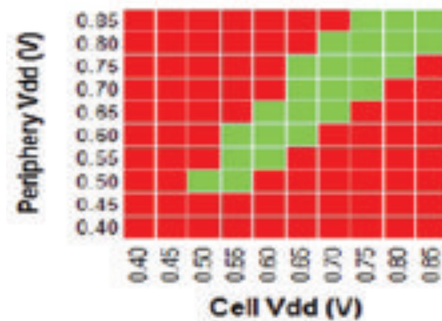

FIGURE 2. "Demonstration of a Sub-0.03 um2 High Density 6-T SRAM with Scaled Bulk FinFETs for Mobile SOC Applications Beyond 10nm Node," Wu et al., TSMC.

IBM and GLOBALFOUNDRIES developed the fundamental and disruptive enhancement of transistor mobility needed to continue expected power and performance scaling at 10nm and beyond, with the introduction of high mobility SiGe channel (20%Ge) into the PFETs to achieve 35% hole mobility increase, and thus ~17% PFET Ieff enhancement. The presentation will demonstrate for the first time10nm FinFET CMOS technology featuring SiGe channel PFETs with superior NBTi reliability and defect control.

TSMC will present a systematic study of the material properties, dimension effects and device characteristics of its In0.53Ga0.47As FinFETs, manufactured on 300mm Si substrates that demonstrate high performance with good uniformity across the wafer. High electron mobility III-V semiconductors are one potential path for continuing Moore's Law to meet the high performance and low power requirements of future logic applications. Creating high

quality hetero-epitaxial of III-V material on large scale Si platforms with good HK/III-V interfaces are critical hurdles to overcome for fabricating HP devices capable of replacing Si FF as scaling continues beyond 7nm.

Significantly, the devices fabricated on 300mm Si show similar characteristics in SS and Ion when benchmarked with equivalent devices fabricated on lattice-matched InP substrates. The current drive of the III-V FinFETs is Ion=44.1uA per fin for a fin-height of 70nm and a fin-width of 25nm. These results are among the highest values reported for In0.53Ga0.47As FinFETs.

Researchers at IBM will demonstrate for the first time high Ge content (HGC) SiGe FinFETs in a replacement mode high-k and metal gate (RMG) process flow with an aggressive equivalent oxide thickness (EOT) scaling down to 0.7nm. IBM's first of its kind HGC SiGe pMOS FinFETs exhibits high mobility, record-low RMG long channel SS=66mV/dec and good short channel behavior down to Lg=21nm.

The devices are characterized down to 4nm fin widths with excellent mobility (μeff=220cm2/V-s) and reliability at 0.7nm. A 10-year lifetime target is achieved for sub-10nm FinFET widths.

This work demonstrates best mobility values compared to state-of-the-art FinFETs, ultra thin body Si or Ge alternatives, as well as to strained SiGe quantum well options, showing that high performance SiGe FinFETs are feasibile at these aggressive dimensions, with results that outperform all previously reported data.

A team from imec reports on vertically stacked gate-all-around (GAA) n- and p-MOSFETs of 8nm diameter with nanowire stacking and replacement metal gate (RMG) processing, which is relevant for continuing scaling beyond sub-10nm technology (**FIGURE 3**).

Stacking nanowire GAA devices is a promising path to maximize current drive per footprint. Fabricated by adapting a RMG FinFET process, these devices represent an evolutionary approach to extend the learning achieved with FinFET manufacturing. The nanowires exhibit excellent short channel characteristics (SS=65mV/dec, DIBL=42mV/V for Lg=24nm) at performance levels comparable to FinFET devices. The parasitic channel below the nanowires is suppressed by a groundplane doping technique prior to nanowire specific processing.

Intel's corporate research group shows performance, area, and energy efficiency are improved by novel tunnel FET (TFET) library circuits, redesign of logic at low-VDD and CMOS/TFET heterogeneous logic. The TFET/CMOS logic with low-overhead level-shifters improves performance 50% while reducing energy 42% for non-critical performance logic. Performance and power are benchmarked by design synthesis using industry test cases, libraries and interconnect.

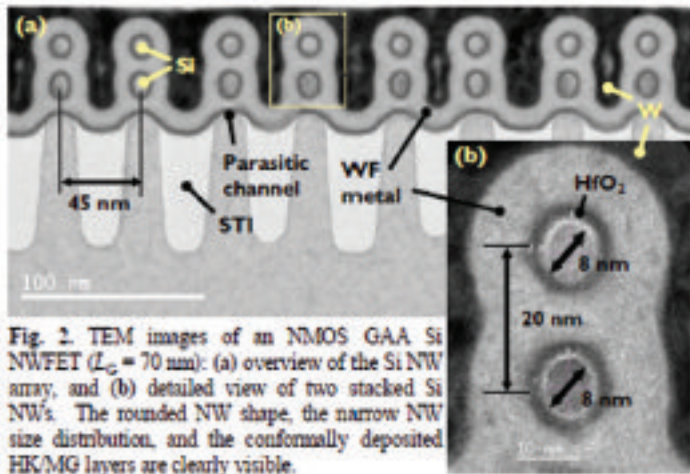

FIGURE 3. "Gate-All-Around MOSFETs Based on Vertically Stacked Horizontal Si Nanowires in a Replacement Metal Gate Process on Bulk Si Substrates" by H. Mertens et al., IMEC

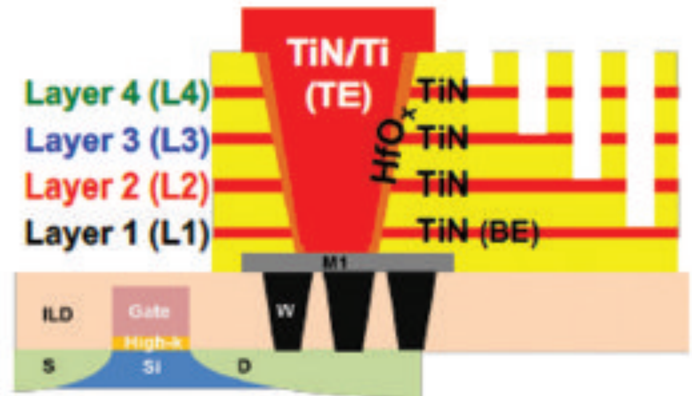

FIGURE 4. Paper T18.2

TDK Headway Technologies returns to the VLSI Symposium to present advances in writing speed of their perpendicular spin-transfer torque magnetic memory (pSTT-MRAM), which can be reduced to a pulse width of 750ps without compromising functionality and data retention. The switching of the full 8MB array with 80nm devices can be achieved with 3ns pulses without use of error-correcting code (ECC), with the array level data retention showing a 10-year lifetime at 1ppm at 125°C.

They demonstrate sub-ns switching of pSTT-MRAM over a large temperature range after optimization of the magnetic tunnel junction (MTJ) stack, with single devices switched reliably using write pulse length down to 750ps while preserving functionality and data retention @125°C.

This pSTT-MRAM with improved writing speed is a viable candidate for replacement of LCC cache for advanced technology nodes, as well as a possible replacement for non-volatile memory.

A novel perpendicular magnetic tunnel junction (MTJ) is demonstrated by Toshiba with a high speed cache memory operation around 1ns, low power switching less than sub-100μA and size scalability of write current down to 16nm diameter MTJ. This novel MTJ is suited for embedded NVRAM solutions for sub-20nm high-performance CMOS SoC technology.

Macronix and IBM investigate methods of reducing programming power in phase change memories (PCM) for new storage class memory (SCM) applications. The researchers demonstrate a new low power phase change memory using inter-granular switching (IGS), a novel 3D network of crystallites with phase change confined to grain intersections. Contrary to conventional phase change memories, for which an entire volume of chalcogenide glass is amorphized or crystallized to achieve high or low resistance, they propose a multi-grained structure where the phase change occurs only in the inter-grain regions. By localizing the phase- change to the inter-grain area, the reset power is substantially reduced to 20μA, as well as the thermal disturbance to the neighboring bits, with set speed and cycling endurance also enhanced.

CEA Leti and STMicroelectronics demonstrate for the first time a full 3D VLSI CMOS-over- CMOS integration, CoolCube™, on 300mm wafers, with the top level CMOS devices fabricated using low temperature (less than 650°C) processes. A functional 3D inverter with either PMOS over NMOS or NMOS over PMOS is demonstrated to achieve compatible performance with state-of-the-art high performance FDSOI devices. Furthermore, the Leti/STM work demonstrates the integration feasibility of CoolCube™ by transferring a high quality Si layer over the 28nm devices with W-M1 and then returning to the front end of the line for processing the top CMOS devices.

For the first time, researchers at Stanford and National Nano Device Laboratories have developed a four-layer HfOx-based 3D vertical RRAM, the "tallest" one ever reported, integrated with FinFET selector (**FIGURE 4**). The four-layer 3D RRAM is a versatile computing unit for (a) brain- inspired computing and (b) in-memory computing. Uniform memory performance across four layers is obtained (±0.8V switching, 106 endurance, 104s @125°C). The 3D architecture with dense and balanced neuron-synapse connections provides 55% energy delay product (EDP) savings and 74% VDD reduction (enhanced robustness) as compared with conventional 2D architecture.

Comprehensive performance evaluation of UHP pressure transducers

YANLI CHEN *and* **MATTHEW MILBURN**, *UCT, Hayward, CA*

Do you really know how good your UHP pressure transducers are based on the manufacturer-provided datasheet as end users?

As a widely-used components in the semiconductor industry, the performance of UHP pressure transducers are very important for process control and process monitoring. Selecting a proper UHP pressure transducer with good performance for specific application is challenging, because different UHP pressure transducers manufacturers have different parameters listed in their datasheet/specification. For example, **FIGURE 1, 2** and **3** are displaying the published specification of UHP pressure transducers from three major manufacturers. Manufacturer A states "BFSL" (Best-fit straight line) method in its accuracy. However, manufacturer C uses "BFSL" in its non-linearity. Except accuracy, manufacturer B and C list non-linearity and hysteresis in their datasheet as well, but those parameters are not shown in manufacturer A's datasheet. Behinds the datasheet/specification, it was found that they have different test procedure and data processing methods to determine performance characteristics, such as non-linearity, hysteresis, non-repeatability, and accuracy. So, for neither the specifier nor the end users is it possible to compare the performance of different brands of pressure transducers without standardized test methods. To date, the industry has not recognized the full scope of the specification problem nor developed a standardized testing and reporting program.

Accuracy:	± 0.25% full scale (BFSL)

FIGURE 1. Product specification of pressure transducer manufacturer A.

Accuracy	% of span	≤ 0.15(≤ 0.4 with pressure range ≤ 2 bar) RSS (Root Sum Squares) ≤ 0.3[1] (≤ 0.6[1] with pressure range ≤ 2 bar) (corresponds to error of measurement per IEC 61298-2)
Non-linearity	% of span	≤ 0.1 (≤ 0.15 for pressure range ≤ 2 bar) BFSL according to IEC 61298-2
Hysteresis	% of span	≤ 0.14
Non-repeatability	% of span	≤ 0.12

1) Including non-linearity, hysteresis, zero point and full scale error

FIGURE 2. Product specification of pressure transducer manufacturer B.

Accuracy RSS[1] (at constant temp)	± 0.25%
Non-Linearity, (BFSL)	± 0.15% FS
Hysteresis	0.20% FS

1) RSS of Non-Linearity, Non-Repeatability and Hysteresis

FIGURE 3. Product specification of pressure transducer manufacturer C.

Technical data and their definition

Before conducting any test, it is necessary to understand the definition of technical data. The common used parameters in the datasheet, such as non-repeatability, non-linearity, hysteresis, and accuracy$_{RSS}$ are explained in the following sections.

Non-repeatability error is defined as the largest deviation between the highest and lowest measurements of the same pressure taken under identical conditions. Non-repeatability characterizes the extent to which the

MATTHEW MILBURN *is a principal engineer at UCT, Hayward, CA. UCT provides OEMs manufacturers with an array of services including design, engineering, system assembly, testing, and global supply chain management. The company does not manufacture pressure transducers.*

output signals for successive measurements of the same pressure vary, and it is an important parameter to judge the design and manufacturing quality of the instrument. High repeatability (i.e., a small non-repeatability error) is a basic requirement of every dependable sensor system. Sometimes, it is expressed as repeatability in percent of full scale.

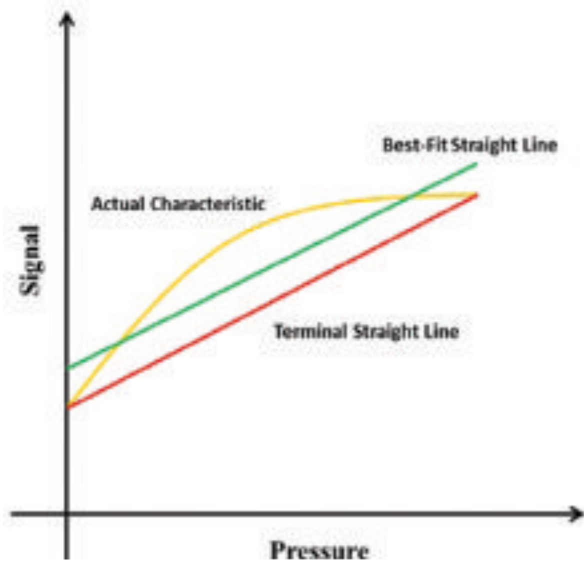

FIGURE 4. Demonstration of linearity.

Non-linearity is defined as the largest deviation (positive or negative) between the actual-characteristic curve and a reference straight line. There are several ways to determine the reference straight line. The two most common are the terminal straight line (TSL) and the best-fit straight line (BFSL) as shown in **FIGURE 4**. In the TSL method, the zero error and span error are ignored and an ideal line connecting the zero and full-scale test is drawn and used as the reference straight line (red line in Figure 4). In the BFSL method, the reference straight line is positioned in relation to the measured characteristic curve in such a way that the sum of squares of the deviations is minimal (green line in Fig. 4). There is no requirement for this line to be parallel or in any other way related to the ideal line of the TSL method. The BFSL method is the standard data fitting method used by the major pressure transducer manufacturers in the United States. Sometimes, non-linearity is expressed by linearity in percent of full scale.

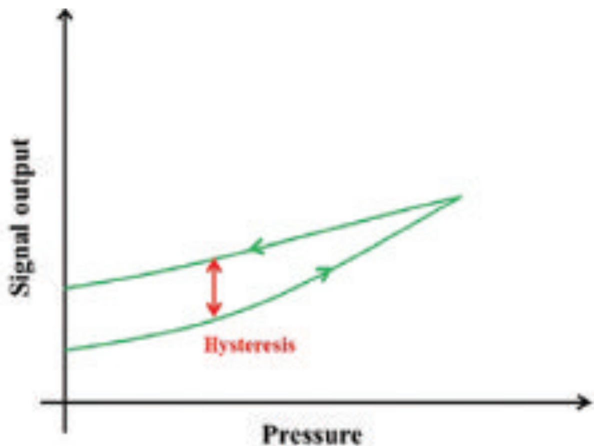

FIGURE 5. Plot of hysteresis curve.

Hysteresis is defined as the maximum deviation between the increasing and decreasing characteristic curves as shown in **FIGURE 5**, which is caused by the applied pressure. Due to the nature of hysteresis, the output readings during rising pressure typically lower than the readings on the return path to zero.

Accuracy$_{RSS}$, **Uncertainty**$_{RSS}$ and **Inaccuracy** Historically, most major manufacturers are using a traditional root sum squares (RSS), defined as the square root of the sum of the squares of non-linearity/linearity, non-repeatability/repeatability and hysteresis, as a method to quantify the accuracy of a pressure transducer. In reality, the RSS method cannot truly reflect the accuracy/inaccuracy behavior of a pressure transducer which can be proved by the test results in the following sections.

A new term, inaccuracy, is introduced. It is defined as the worst case performance or absolute value of the maximum deviation at any measured value from the ideal value across the full pressure range of a transducer. Inaccuracy is much more representative of a device's performance.

In order to be able to compare the test results with the manufacturers' published specification, a new term, "uncertainty$_{RSS}$", is introduced based on the "uncertainty" definition from SEMI International Standards: Compilation of Terms. Actually, it is the same as the historical accuracy$_{RSS}$ listed in most manufacturers' published specification.

Experimental

Three UHP pressure transducer manufacturers (MFG A, MFG B and MFG C) participated in this comprehensive performance evaluation project by providing their products as test samples. **FIGURE 6** shows the

Manufacturer	MFG A	MFG B	MFG C
Pressure Range	0–250 psia	-14.7–235.3 psig	-14.7–235.3 psig
Output Voltage (VDC)	0-10	0-10	10-Feb
Excitation Voltage (VDC)	13-32	14-30	30-Dec
Fitting Type	VCR-M	VCR-F	VCR-M
Sample Quantity	4	4	4

FIGURE 6. Detailed information of DUTs.

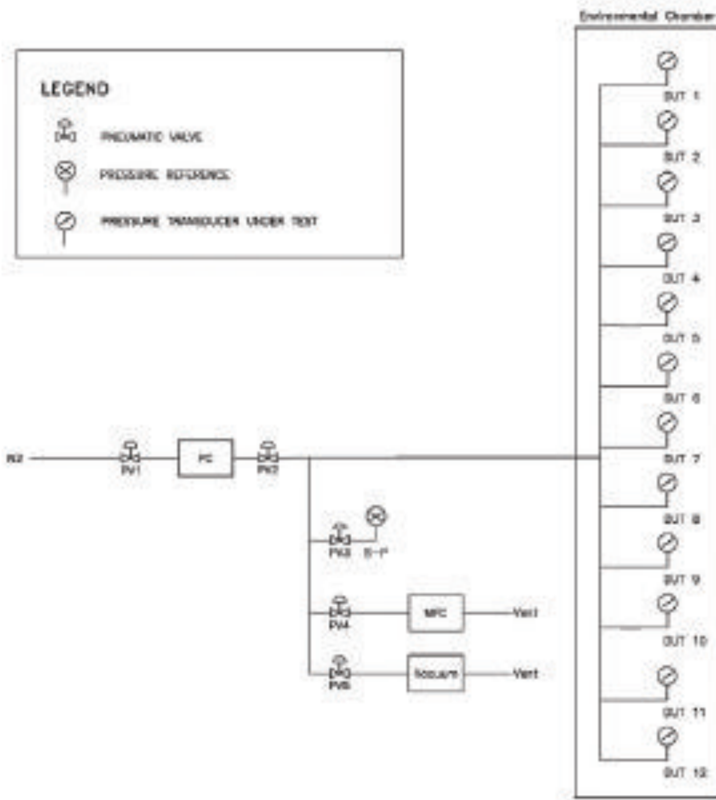

FIGURE 7. Schematic of the test fixture.

detailed information of devices under tests (DUTs). Twelve DUTs were installed in a test fixture designed by UCT for running simultaneous tests. The schematic of the test fixture is shown in **FIGURE 7**. The benefit of this design is to save significant amounts of time for assembly, disassembly, and testing, and eliminate potential setup errors occurring in the sequential tests.

The tests were conducted in a temperature controlled environment (20 ± 2°C). **FIGURE 8** shows the DUTs in the environmental chamber. The tests were completed by running total ten ascending (from 0%FS to 100%FS in 10%FS steps with a rate of change setpoint every 200 seconds) and descending (from 100%FS to 0%FS in 10%FS steps with a rate of change setpoint every 200 seconds) cycles.

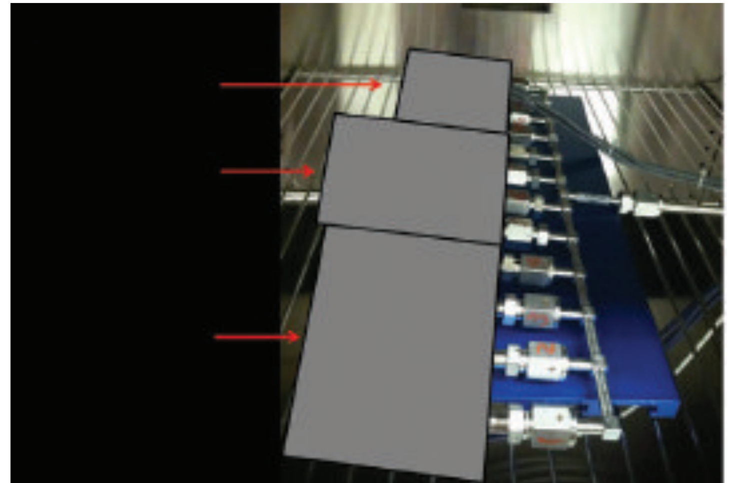

FIGURE 8. Picture of all DUTs inside the environmental chamber.

Test results and discussion

The test results are summarized in **FIGURE 9**. In each sample group, the highest test value is highlighted in red and the lowest test value is highlighted in green. For each testing parameter, the best case is not always the same DUT in each sample group; the worst case is not always the same DUT in each sample group, either. For better comparison, the test results are graphically shown in **FIGURE 10**. As shown in Fig. 10, repeatability and hysteresis of the twelve DUTs do not have obvious fluctuations and all of the twelve DUTs have similar values for hysteresis and repeatability.

However, linearity, $uncertainty_{RSS}$ and inaccuracy of the twelve DUTs have dramatic fluctuations, especially

MFG	Tag#	Repeatability (%FS)	Linearity (%FS)	Hysteresis (%FS)	$Uncertainty_{RSS}$ (%FS)	Inaccuracy (%FS)
A	DUT 1	0.032	0.126	0.057	0.142	0.270
	DUT 2	0.039	0.121	0.036	0.132	0.141
	DUT 3	0.050	0.101	0.044	0.121	0.272
	DUT 4	0.043	0.079	0.039	0.098	0.382
B	DUT 5	0.039	0.069	0.036	0.087	0.178
	DUT 6	0.039	0.065	0.049	0.090	0.238
	DUT 7	0.019	0.064	0.036	0.076	0.074
	DUT 8	0.034	0.069	0.026	0.081	0.122
C	DUT 9	0.036	0.357	0.038	0.341	1.132
	DUT 10	0.042	0.166	0.032	0.174	2.420
	DUT 11	0.036	0.372	0.038	0.376	0.758
	DUT 12	0.037	0.328	0.030	0.332	0.869

FIGURE 9. Test Results of all DUTs.

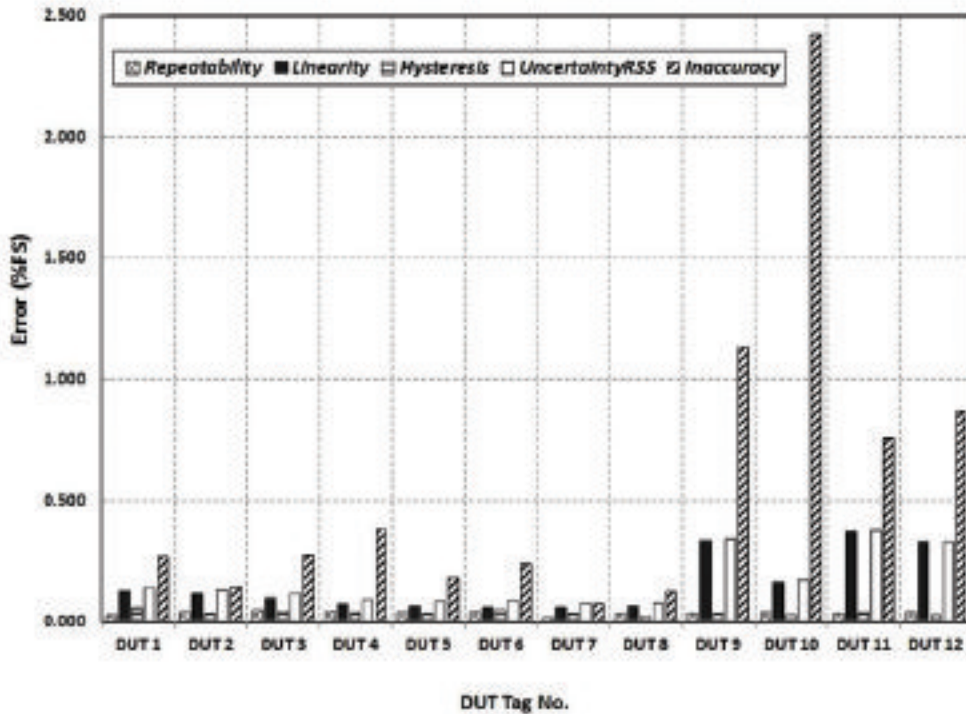

FIGURE 10. Test results comparison between all DUTs.

MFG	Repeatability (%FS)	Linearity (%FS)	Hysteresis (%FS)	Uncertainty_{RSS} (%FS)	Inaccuracy (%FS)
A	0.050	0.126	0.057	0.142	0.382
B	0.039	0.069	0.049	0.090	0.238
C	0.042	0.372	0.038	0.376	2.420

FIGURE 11. Test results of manufacturers' product.

inaccuracy. Four DUTs from manufacturer C shows higher inaccuracy than the rest of other DUTs. Specifically, DUT 10 is showing extremely high inaccuracy (2.420%FS), which is about thirty-three times worse than the best case (0.074%FS). Four DUTs from manufacturer C also shows poorer linearity than the rest of other DUTs. For the uncertainty_{RSS} values, three DUTs from manufacturer C have much higher values than the rest of DUTs. Devices from manufacturer B have the best repeatability (0.039%FS), linearity (0.069%FS), inaccuracy (0.238%FS), and uncertainty_{RSS} (0.090%FS). A device from manufacturer C has the best hysteresis (0.038%FS). Devices from manufacturer A have the worst repeatability (0.050%FS) and hysteresis (0.057%FS) values. Devices from manufacture C have the worst linearity (0.372%FS), uncertainty_{RSS} (0.376%FS), and inaccuracy (2.420%FS) values. It can be concluded that the devices from manufacturer B have the best overall performance compared to devices from manufacturer A and C.

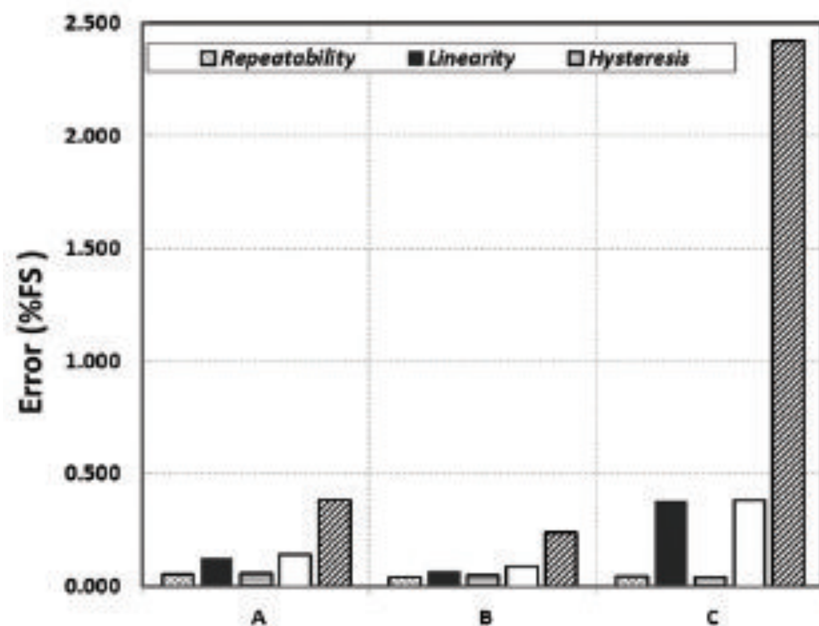

FIGURE 12. Test results comparison between manufacturers.

In order to conduct the side by side comparison of each manufacturer's product, the worst case of each manufacturer's sample for repeatability, linearity, hysteresis, uncertainty_{RSS}, and inaccuracy is summarized in **FIGURE 11** and graphically shown in **FIGURE 12**.

The worst case value is reported as the representative values of that brand's pressure transducer. For each testing parameter, the highest value is highlighted in red and the lowest value is highlighted in green. As shown in Fig. 11, MFG A has the highest repeatability (0.050%FS) and MFG B has the lowest repeatability (0.039%FS); MFG C has the highest linearity (0.372%FS) and MFG B has the lowest linearity (0.069%FS); MFG A has the highest hysteresis (0.057%FS) and MFG C has the lowest hysteresis (0.038%FS); MFG C has the highest uncertainty_{RSS} (0.376%FS) and MFG B has the lowest uncertainty_{RSS}

(0.090%FS); MFG C has the highest inaccuracy (2.420%FS) and MFG B has the lowest inaccuracy (0.238%FS).

When compared with the manufacturers' published specification, the DUTs of MFG B meet the published specification of repeatability, linearity, hysteresis and $uncertainty_{RSS}$; the DUTs of MFG C meet their hysteresis specification, but do not meet their published linearity and $uncertainty_{RSS}$ specification except that DUT 10 meet the $uncertainty_{RSS}$ specification. However, DUT 10 has the highest inaccuracy value among the twelve DUTs, which totally supports our findings that $uncertainty_{RSS}$ or $accuracy_{RSS}$ cannot reflect the true accuracy/inaccuracy behavior.

Conclusions

The results of this study prove that the performance indicator "$accuracy_{RSS}$" used by most the pressure transducer manufacturers cannot truly reflect the performance. Based on this study, transducers marketed as comparable to each other display dramatically difference performance levels which could lead to process reproducibility challenges. It also demonstrates that the manufacturers' published specification needs to be improved in order to truly reflect the performance of a UHP pressure transducer. Also, and of critical value, a proper test procedure and data processing method needs to be adopted in the industry. The pressure measurement task force of SEMI North America Gases and Facilities Committee is developing a new pressure transducer measurement standard based on this study.

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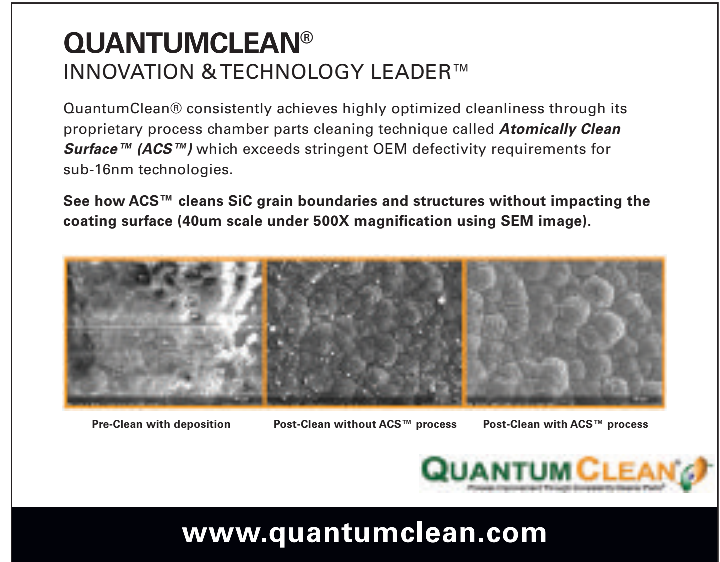

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Fan out from niche to mainstream

When most people in packaging hear the term "Fan Out," they usually think of the eWLB type of "chips first" fan out process/structure. This was the first of the embedded chips first structures to be taken into volume production by Infineon and ASE in Q1 2009. But this was not the end of the story. Today we speak of a chip first process and a chip last process building almost the same fan out structure.

Chips first fan out process describes a process where the singulated die are held in some form of matrix, followed by overmolding and the formation of the redistribution trace structure in situ on the surface of the die/matrix formation.

In contrast, chips last fan out process describes a process where the redistribution trace structure is formed first, sometimes on some type of temporary carrier, and then the singulated die are bonded using a flip chip assembly process onto this trace pattern, followed by overmolding of the package.

To the end user, it is the fan out package structure for the devices – active and passive – and the performance, cost and robustness of that package that really matters. How that fan out package structure is manufactured (i.e. processed) is of less importance. Packaging engineers are nothing but ingenious. Give them a challenge and they will find a way. For Fan Out, the good news is that there are two basic processes, Chip First and Chip Last, providing manufacturing capacity to serve the end users.

As an example, ASE brought out a high volume chip last panel fan out solution to market in 2014 that provides a very similar fan out structure to the eWLB fan out structure. And since that time, ASE has been in high volume production for several devices. In fact, one paper at ECTC 2016 describes the comparative similarity and differences of the Fan Out product for the same die built from these two different processes – chip first and chip last.

The Infineon Baseband chip was the first embedded chip first type of fan out to go into mass production and was well suited to the relatively low density, single chip requirements of that package. However, with the evolution of smart phone mobile devices, and the need for greater packaging densities, there is now a need for higher density fan out, often with multiple die, and the inclusion of passive devices within the fan out package structure. And it is this expanded application space for Fan Out – both for chip first and for chip last – that is getting the industry excited.

In January of this year, using a chip first wafer fan out solution, ASE released a high density fan out hybrid package structure with more than a thousand I/O, and multiple trace layers with very fine lines and spaces into production. It is clear that similar structures will also be built using a chip last process.

We can see that there are advantages and disadvantages in using each of these fan out process technologies, depending on the specific applications. Fan out chip last, however, has the advantage of an existing manufacturing infrastructure, with the promise of faster ramp up to high manufacturing yields. This is because the trace pattern can be inspected, and tested, and nearly known good die can be placed only on known good trace patterns. In contrast, for chip first, the die are committed by the time the trace pattern yield is determined, and any bad trace patterns include the cost of these die in yield losses. Chip Last has also shown the promise of increased versatility in meeting the more complex requirements of System in Package (SiP) applications.

We are seeing the transition of what had been a niche technology going into mainstream. The ingenuity and creativity of the packaging engineers are being tested as never before. And they have come out on top. As fan out comes of age, we shall find that there are applications and uses for more than one variation of structure and more than one variation of process. In the end, the market will help us to decide the most manufacturable and lowest cost solutions for each of the many different applications. ◆

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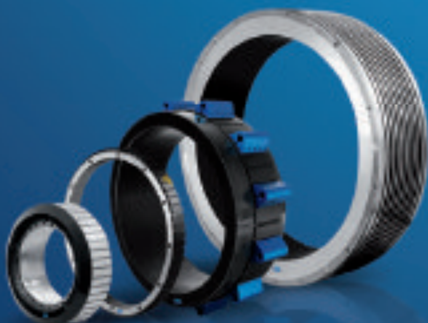

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