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Solid State TECHNOLOGY

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Toyota Concept-i (shown at this year's CES) early interior sketch. Source: Toyota

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AUTOMOTIVE | The automotive electronics market: A view from a material supplier

With the increasing sophistication of future vehicles, new and more advanced semiconductor technologies will be used and vehicles will become technology centers.

Dr. Jean-Charles Cigal and Greg Shuttleworth, Linde Electronics, Taipei, Taiwan

METROLOGY | Fast and precise surface measurement of back-grinding silicon wafers

A new type of scattered light measurement method will be presented, capable of measuring the full wafer surface of a 300 mm wafer in less than 30 seconds. Besides the roughness, the sensor simultaneously measures warpage, waviness and defects. R. Brodmann, B. Brodmann, K. Konovalenko, and C. Wiehr, OptoSurf GmbH, and Ching-Hsien Huang, Ya-Leng Chen, Amkor Technology, Inc.



PROCESS WATCH | Having confidence in your confidence level Did you take enough measurements to be confident in the result? Douglas G. Sutherland and David W. Price, KLA-Tencor, Milpitas, CA



TECH TRENDS | What TechInsights analysts are watching in 2017

TechInsights analysts share their view on where technology is going, how it's changing, and what new developments are emerging. Stacey Wegner, Jeongdong Choe and Ray Fontaine, TechInsights, Ottowa, ON

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It's difficult to cheat physics and make a profit. Ed Korczynski, Sr. Technical Editor

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SEMICON | SEMICON West Preview: MEMS

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editorial

It's time for new innovation

What if the automotive industry had achieved the incredible pace of innovation as the semiconductor industry during the last 52 years? A Rolls Royce would cost only \$40, go around the world eight times on a gallon of gas, and have a top speed of 2.4 million miles per hour.

That point was made by Subi Kengeri speaking at The ConFab in May. Kengeri is vice president, CMOS Business Unit, at GlobalFoundries. He also noted that if one of today's high performance graphics chips were produced using 1960 vs now "it would be the size of a football field."

Clearly, no other industry can match the pace of innovation of the semiconductor industry. "The transistor count per square inch in 1965 was roughly 100. In 52 years, if you follow Moore's Law of 2 years per innovation cycle, that gives 26 innovation cycles. That's 100 millionX improvement (2X26)," Kengeri noted.

Of course, there has been plenty of innovation in the automotive industry. Interestingly, most of the exciting new innovations such as backup cameras, collision avoidance, navigation/ infotainment, self-parking, and anti-lock brakes are only possible because of semiconductor technology.

Kengeri said that Moore's Law scaling will continue – "there's no question about it," he said – but there's a growing need for new innovation to address the increasingly diverse array of semiconductor applications. These are driven by growth in mobile computing, development in IoT computing, the emergence of intelligent computing and augmented/virtual reality. "Leading edge innovation will continue and all the leading manufacturers continue to invest, whether it is litho scaling in terms of EUV, or device archicture," Kengeri said. "What is really important is how to do we continue to innovate, how do we continue to get the value at competitive costs? Trying to get the scaling at any cost is not what is needed in the majority of the markets. It's still okay at the very high end, for CPUs and servers, but in all markets, managing cost is really critical."

"On top of all of that, we have to continue to deliver on time. Because of the complexity, things aren't getting slower. We're doing everything we can do continue to keep the same pace as we used to," he added.

Kengeri said continued advances mean changing the way we think about innovation. It will require continued technical Innovation (materials and processes, device architecture and design-technology co-optimization), but – perhaps more importantly – it will business model innovation. This includes new thinking about long-term R&D focus/ investment, shared investments/learning/reuse, and consolidation and collaboration.

-Pete Singer, Editor-in-Chief

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Solid State Technology is published eight times a year by Extension Media LLC, 1786 Street, San Francisco, CA 94107. Copyright © 2017 by Extension Media LLC. All rights reserved. Printed in the U.S.



1786 18th Street San Francisco, CA 94107

June 2017 VOL. 60 NO. 4 • Solid State Technology ©2017 (ISSN 0038-111X) Subscriptions: Domestic: one year: \$258.00, two years: \$413.00; one year Canada/Mexico: \$360.00, two years: \$573.00; one-year international airmail: \$434.00, two years: \$691.00; Single copy price: \$15.00 in the US, and \$20.00 elsewhere. Digital distribution: \$130.00. You will continue to receive your subscription free of charge. This fee is only for air mail delivery. Address correspondence regarding subscriptions (including charge of address) to: Solid State Technology, 1786 18th Street, San Francisco, CA 94107-2343. (8 am – 5 pm, PST).

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Web Exclusives

China's semiconductor industry and "winwin" growth

Lung Chu, President of SEMI China, writes that to be successful, it is critical that China's semiconductor industry speed up its integration into the global industry supply chain. The goal is to achieve sustainable growth through "win-win" collaboration with global partners and leveraging industry platforms to become a significant player and partner in the international semiconductor manufacturing industry ecosystem. http://bit.ly/2rGySw1

Worldwide semiconductor revenue grew 2.6% in 2016, reports Gartner

Worldwide semiconductor revenue totaled \$343.5 billion in 2016, a 2.6 percent increase from 2015 revenue of \$334.9 billion, according to final results by Gartner, Inc. The top 25 semiconductor vendors' combined revenue increased 10.5 percent, a significantly better performance than the overall industry's growth; however, most of this growth resulted from merger and acquisition (M&A) activity.

http://bit.ly/2qR19P8

Record fab spending for 2017 and 2018

The latest update to the World Fab Forecast report, published on May 31, 2017 by SEMI, reveals record spending for fab construction and fab equipment. Korea, Taiwan, and China all see large investments, and spending in Europe will also increase significantly. In 2017, over US\$49 billion will be spent on equipment alone, a record for the semiconductor industry. http://bit.ly/2rZ20y2

Infineon rides automotive wave into Top-10 semi supplier ranking

IC Insights released its May Update to the 2017 McClean Report. This Update includes a discussion of the 1Q17 semiconductor industry market results, an update of the capital spending forecast by company, a review of the IC market by electronic system type, and a look at the top-25 1Q17 semiconductor suppliers. There was one new entrant into the top-10 ranking in 1Q17—Germany-headquartered Infineon. http://bit.ly/2q6QVtp



Insights from the Leading Edge: ISHM to IMAPS; IEEE CPMT to IEEE EPS?

Dr. Phil Garrou provides a historical perspective on the two major name changes of our key International Microelecronic Packaging & Interconnect Societies. One occurred 20 years ago and one that is occurring as we speak. http://bit.ly/2qqyE7i

MEMS mirrors for LIDAR

Clever integration of new microelectronic/ nanoelectronic technologies will continue to provide increased functionalities for modern products. Light Imaging, Detection, And Ranging (LIDAR) technology uses lasers to see though fog and darkness, and smaller less expensive LIDAR systems are needed for autonomous driving applications now being developed by dozens of major companies around the world. A significant step in the right direction has been taken by the US government's Lawrence Livermore National Laboratory (LLNL) after working with AMFitzgerald on a MEMS mirror Light-field Directing Array (LDA) prototype.

http://bit.ly/2rXHWK2

How critical area analysis optimizes memory redundancy design

As any design engineer knows, the farther downstream a design goes, the less likely a manufacturing problem can be corrected without a costly and time-consuming redesign. And it doesn't matter if you are a fabless, fab-lite, or independent device manufacturer (IDM) company—reducing a design's sensitivity to manufacturing issues should ideally be handled by the design teams. By identifying and resolving design for manufacturing (DFM) problems while the design is still in its early stages, many manufacturing ramp-up issues can be avoided altogether.

http://bit.ly/2nkuXPe

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worldnews

USA - Micron appointed Sanjay Mehrotra as President and CEO.

ASIA - WIN Semiconductors Corp., the world's largest pureplay compound semiconductor foundry, increased wafer manufacturing capacity by 20%.

USA - North America-based manufacturers of semiconductor equipment posted \$2.17 billion in billings worldwide in April 2017 according to SEMI.

EUROPE - EV Group announced a milestone: More than 1100 wafer bond chambers installed worldwide.

USA - Lam Research appointed Dr. Y.B. Koh to its Board of Directors. Dr. Koh held many executive positions at Samsung Electronics in South Korea.

USA - ON Semiconductor won the **Gold Stevie American Business** Award for Large Manufacturing Company of the Year.

EUROPE AND ASIA - Soitec named Stephen Lin new VP of Strategic Business Development in China, a newly created position.

ASIA - SMIC transitioned CEO responsibility to Dr. Haijun Zhao, replacing Dr. Tzu-Yin Chiu, who will continue to serve as Vice Chairman and Non-Executive Director of the Board.

USA - Florida-based UnitySC receives multiple orders for wafer thinning inspection systems from an unnamed IDM.

EUROPE and ASIA - Tianma selected Orbotech's ArrayChecker and Automated Optical Inspection (AOI) solutions solutions for its flex AMOLED Gen 6 fab in China.

USA - SiFive, the first fabless provider of customized, opensource-enabled semiconductors, secured \$8.5M in funding to advance RISC-V based semiconductors.

USA - Researchers at North Carolina State University have developed a new approach for manipulating the behavior of cells on semiconductor materials, using light to alter the conductivity of the material itself.

GLOBALFOUNDRIES and Chengdu partner to expand FD-SOI ecosystem in China

GLOBALFOUNDRIES and the Chengdu municipality announced an investment to spur innovation in China's semiconductor industry. The partners plan to build a worldclass FD-SOI ecosystem including multiple design centers in Chengdu and university programs across China. The investment of more than \$100 million is expected to attract leading semiconductor compa-

for designing next-generation chips in mobile, systems companies in developing products Internet-of-Things (IoT), automotive and other using 22FDX for mobile, connectivity, 5G, IoT, high-growth markets.

GF and Chengdu recently launched a joint China to develop relevant FD-SOI coursework, venture to build a 300mm fab to meet accel- research programs and design contests. erating global demand for GF's 22FDX FD-SOI technology. Connected to this manufacturing "China is the largest semiconductor market and partnership, Chengdu is now focusing on devel- is leading the way with a nationwide commitoping the city as a center of excellence for 22FDX ment to smart cities, IoT, smart vision and design. The partners plan to establish multiple other advanced, mobile or battery-powered centers focused on IP development, IC design connected systems" said Alain Mutricy, and incubating fabless companies in Chengdu, with the expectation of hiring more than 500

nies to Chengdu, making it a center of excellence engineers to support semiconductor and and automotive. There will also be a focus on creating partnerships with universities across

Continued on page 9

Amkor Technology completes acquisition of NANIUM

Amkor Technology, Inc. announced that it has Steve Kelley, Amkor's president and chief execucompleted the acquisition of NANIUM S.A., a tive officer. "With the acquisition of NANIUM, we provider of wafer-level fan-out (WLFO) semicon- will have an equally compelling value proposiductor packaging solutions.

In its press release, Amkor said that the acqui- as well as a very capable manufacturer, having sition of NANIUM will strengthen its position in the fast growing market of wafer-level packaging for smartphones, tablets and other applications. NANIUM has developed a high-yielding, reliable WLFO technology, and has successfully ramped that technology to high volume production.

"Amkor is a leader in wafer-level CSP and highdensity integrated fan-out technologies," said

tion in the low-density fan-out area. NANIUM is widely viewed as the fan-out technology leader shipped more than one billion WLFO packages utilizing a state-of-the-art 300mm wafer-level packaging production line."

NANIUM employs approximately 650 people and is based in Porto, Portugal. 🔶



Sensor/actuator sales take off as price erosion eases

After several years of low and inconsistent growth rates primarily because of intense pricing pressure, the market for semiconductor sensors and actuators finally caught fire in 2016 with several of its largest product categories acceleration/yaw and magnetic-field sensors and actuator devices—recording strong double-digit sales increases in the year, according to IC Insights' new 2017 O-S-D Report—A Market Analysis and Forecast for Optoelectronics, Sensors/ Actuators, and Discretes. In addition to the easing of price erosion, substantial unit-shipment growth in sensors and actuators continues to be fed by the spread of intelligent embedded control, new wearable systems, and the expansion of applications connected to the Internet of Things, says the 2017 O-S-D Report.

The new 360-page report shows worldwide sensor sales grew 14% in 2016 to a record-high \$7.3 billion, surpassing the previous annual peak of \$6.4 billion set in 2015, when revenues increased 3.7%. Actuator sales climbed 19% in 2016 to an all-time high of \$4.5 billion from the previous record of \$3.8 billion in 2015. The 2017 O-S-D Report forecasts total sensor sales rising by a compound annual growth rate (CAGR) of 7.5% in the next five years, reaching \$10.5 billion in 2021, while actuator dollar volumes are expected to increase by a CAGR of 8.4% to nearly \$6.8 billion in the same timeframe. Figure 1 shows the relative market sizes of the five main product categories in the sensors/ actuator segment, along with the projected five-year growth rates for the 2016-2021 forecast period.

The sensor/actuator market ended four straight years of severe price erosion in 2016 and finally benefitted from strong unit growth. The average selling price (ASP) of sensors and actuators declined by -0.9% in 2016 versus an annual average of -9.3% during the four previous years (2012-2015), says IC Insights' new O-S-D Report. All sensor product categories and the large actuator segment registered double-digit sales growth in 2016. It was the first time in five years that sales growth was recorded in all sensor/ actuator product categories, partly due to the easing of price erosion but also because of continued strong unit demand worldwide. Sensor/actuator shipments grew 17% in 2016 to a record-high of 20.3 billion units from 17.4 billion in 2015, when the volume also increased 17% (see Figure).

Strong 2016 sales recoveries occurred in acceleration/ yaw-rate motion sensors (+15%), magnetic-field sensors and electronic compass chips (+18%), and the miscellaneous

Continued on page 9



newscont.

Primary automotive display systems market valued at \$11.6B globally in 2017

The primary automotive display systems market will reach \$11.6 billion in tier one supplier revenue globally in 2017, according to new analysis from business information provider IHS Markit.

The market is set to increase drastically over the next few years, says the latest Automotive Display Systems Forecasts from IHS Markit. The most valuable are the Center Stack Displays and Instrument Cluster Displays, representing global revenues of \$6.1 and \$4.8 billion respectively. Head-Up Displays (HUD) account for only \$731 million today, but show the largest growth potential in terms of percentage going forward through 2022. In 2022, combined value from the Center Stack Display, Instrument Cluster Display and Head-Up Display system markets total more than \$20.8 billion, an increase of \$9.2 billion in annual revenue in just five years, according to IHS Markit.

"There are a few different sources of this increase in display value within the automotive sector," said Brian Rhodes, automotive technology analyst for IHS Markit. "First are simple volume increases, with more vehicles adding new displays to the instrument cluster and center stack, along with Head-Up Display deployments becoming more common. The second area of growth is in the technology value itself, as these displays are becoming larger and more capable – and therefore more expensive."

Continental leads display system suppliers

Continental is expected to be the top supplier of primary automotive display systems in 2017 based on global revenue forecasts, the IHS Markit research says. Visteon follows closely behind, as the only other supplier with a double-digit market share in this space. Panasonic, Denso and Bosch round out the remaining market share leaders in the top five. Combined, these suppliers account for more than \$6 billion in revenue resulting from Center Stack Display, Instrument Cluster Display and Head-Up Display systems in 2017.

"The top five primary display system suppliers command more than half of the total automotive display systems market," Rhodes said. "While this is certainly a large portion of revenue for a handful of large players, it still means there is an incredible amount of fragmentation left over offering opportunity for the rest of the supply base — both in today's market and in the foreseeable future based on our forecasts."

Safety information related display panels offer strong growth potential

Thin film transistor liquid crystal display (TFT LCD) automotive display panel market shipments are expected to grow from 135 million units in 2016 to 200 million units in 2022. This technology will represent more than 67 percent share of total automotive display shipments, according to the Automotive Display Market Tracker from IHS Markit.

"The market growth momentum has shifted from center stack display, rear seat entertainment and other infotainment displays, to safety system displays, namely instrument cluster display, head-up display and eMirror systems," said Stacy Wu, principal analyst for IHS Markit. While today's volumes are large for infotainment display panels, safety-critical display panels will see double-digit growth through 2022, according to IHS Markit forecasts.

Japan Display, Innolux top tier two automotive display panel manufacturers

Based on the latest findings from IHS Markit, Japan Display, Innolux, Sharp, AU Optronics and LG Display are the top five TFT LCD automotive display panel manufacturers, representing more than 65 percent of the market in 2016.

"However, we expect to see increasing share gains from new entrants and possible ranking switches as well," Wu said. "Stagnant panel demand from consumer electronics segments like notebooks, tablets, and smartphones, together with excess production capacity, is forcing display panel makers to enter the fast growing automotive market." \blacklozenge

Organic electronics: Semiconductors as decal stickers

No more error-prone evaporation deposition, drop casting or printing: Scientists at Ludwig-Maximilians-Universitaet (LMU) in Munich and FSU Jena have developed organic semiconductor nanosheets, which can easily be removed from a growth substrate and placed on other substrates. Electronic components normally consist of semiconductor material, insulator, substrate, and electrode. A dream of many scientists is to have each of these elements available as transferable sheets, which would allow them to design new electronic devices simply by stacking. This has now become a reality for the organic semiconductor material pentacene: Dr. Bert Nickel, a physicist at LMU Munich, and Professor Andrey Turchanin (Friedrich Schiller University Jena), together with their teams, have, for the first time, managed to create mechanically stable pentacene nanosheets. which would make them ideal as biosensors, for example". "Another promising application is their implementation in flexible electronics for manufacturing of devices for vital data acquisition or production of displays and solar cells," Turchanin says.

The researchers describe their method in the journal Advanced Materials. They first cover a small silicon wafer with a thin layer of a water-soluble organic film and deposit pentacene molecules upon it until a layer roughly 50 nanometers thick has formed. The next step is crucial: by irradiation with low-energy electrons, the topmost three to four levels of pentacene molecular layers are crosslinked, forming a "skin" that is only about five nanometers thick. This crosslinked layer stabilizes the entire pentacene film so well that it can be removed as a sheet from a silicon wafer in water and transferred to another surface using ordinary tweezers.

Apart from the ability to transfer them, the new semiconductor nanosheets have other advantages. The new method does not require any potentially interfering solvents, for example. In addition, after deposition, the nanosheet sticks firmly to the electrical contacts by van der Waals forces, resulting in a low contact resistance of the final electronic devices. Last but not least, organic semiconductor nanosheets can now be deposited onto significantly more technologically relevant substrates than hitherto.

Of particular interest is the extremely high mechanical stability of the newly developed pentacene nanosheets, which enables them to be applied as free-standing nanomembranes to perforated substrates with dimensions of tens of micrometers. That is equivalent to spanning a 25-meter pool with plastic wrap. "These virtually freely suspended semiconductors have great potential," explains Nickel. "They can be accessed from two sides and could be connected through an electrolyte,



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NEV/Scont.

'Valleytronics' advancement could help extend Moore's Law

A new field of physics called "valleytronics" is seeking to exploit the electron's "valley degree of freedom" for data storage and logic applications. Simply put, valleys are maxima and minima of electron energies in a crystalline solid. A method to control electrons in different valleys could yield new, super-efficient computer chips.

A University at Buffalo team, led by Hao Zeng, PhD, professor in the Department of Physics, worked with scientists around the world to discover a new way to split the energy levels between the valleys in a two-dimensional semiconductor. The work is described in a study published online in May 2017 in the journal Nature Nanotechnology.

The key to Zeng's discovery is the use of a ferromagnetic compound to pull the valleys apart and keep them at different energy levels. This leads to an increase in the separation of valley energies by a factor of 10 more than the one obtained by applying an external magnetic field.

"Normally there are two valleys in these atomically thin semiconductors with exactly the same energy. These are called 'degenerate energy levels' in quantum mechanics terms. This limits our ability to control individual valleys. An external magnetic field can be used to break this degeneracy. However, the splitting is so small that you would have to go to the National High Magnetic Field Laboratories to measure a sizable energy difference. Our new approach makes the valleys more accessible and easier to control, and this could allow valleys to be useful for future information storage and processing," Zeng said.

The simplest way to understand how valleys could be used in processing data may be to think of two valleys side by side. When one valley is occupied by electrons, the switch is "on." When the other valley is occupied, the switch is "off." Zeng's work shows that the valleys can be positioned in such a way that a device can be turned "on" and "off," with a tiny amount of electricity.

Zeng and his colleagues created a two-layered heterostructure, with a 10 nm thick film of magnetic EuS (europium sulfide) on the bottom and a single layer (less than 1 nm) of the transition metal dichalcogenide WSe2 (tungsten diselenide) on top. The magnetic field of the bottom layer forced the energy separation of the valleys in the WSe2.

Previous attempts to separate the valleys involved the application of very large magnetic fields from outside.

Zeng's experiment is believed to be the first time a ferromagnetic material has been used in conjunction with an atomically thin semiconductor material to split its valley energy levels. "As long as we have the magnetic material there, the valleys will stay apart," he said. "This makes it valuable for nonvolatile memory applications."

Athos Petrou, a UB Distinguished Professor in the Department of Physics, measured the energy difference between the separated valleys by bouncing light off the material and measuring the energy of reflected light. "We typically get this type of results only once every five or 10 years," Petrou said.

Extending Moore's law

The experiment was conducted at 7 degrees Kelvin (-447 Fahrenheit), so any everyday use of the process is far in the future. However, proving it possible is a first step. "The reason people are really excited about this, is that Moore's law [which says the number of transistors in an integrated circuit doubles every two years] is predicted to end soon. It no longer works because it has hit its fundamental limit," Zeng said.

"Current computer chips rely on the movement of electrical charges, and that generates an enormous amount of heat as computers get more powerful. Our work has really pushed valleytronics a step closer in getting over that challenge."

The researchers describe their method in the journal Advanced Materials. They first cover a small silicon wafer with a thin layer of a water-soluble organic film and deposit pentacene molecules upon it until a layer roughly 50 nanometers thick has formed. The next step is crucial: by irradiation with low-energy electrons, the topmost three to four levels of pentacene molecular layers are crosslinked, forming a "skin" that is only about five nanometers thick. This crosslinked layer stabilizes the entire pentacene film so well that it can be removed as a sheet from a silicon wafer in water and transferred to another surface using ordinary tweezers.

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GLOBALFOUNDRIES, Continued from page 4

senior vice president of product management at GF. "FDX is especially well suited for Chinese customers, and the FD-SOI ecosystem in Chengdu will provide the support system necessary to help chip designers take full advantage of the technology's capabilities. We are committed to extend our partnership with Chengdu to accelerate adoption of FDX in China."

"Following the ribbon cutting marking the signing of our Investment Cooperation Agreement, and to deepen our cooperation and attract more best-in-class semiconductor companies to Chengdu, the Chengdu Municipal Government is delighted to cooperate with GlobalFoundries on this FD-SOI ecosystem action plan," said Gou Zheng Li, Vice

Sensor/actuator sales, Continued from page 5

other sensor category (+20%) after market declines were registered in 2015. Sales growth also strengthened in pressure sensors, including MEMS microphone chips, (+10%) and actuators (+19%) in 2016. The new O-S-D Report forecasts sales of acceleration/yaw sensors growing 9% in 2017 to about \$3.0 billion, magnetic-field sensors (and compass chips) rising 8% to nearly \$2.0 billion, and pressure sensors increasing 8% to \$2.7 billion this year. Actuator sales are projected to grow 8% in 2017 to about \$4.9 billion.

About 82% of the sensors/actuators market's revenues in 2016 came from semiconductors built with microelectromechanical systems (MEMS) technology—meaning pressure sensors, microphone chips, acceleration/yaw motion sensors, and actuators that use MEMS-built transducer structures to initiate physical action in a wide range of devices, including inkjet printer nozzles, microfluidic chips, micro-mirrors, and surface-wave filters for RF signals. MEMS-built products represented 48% of total sensor/actuator shipments in 2016, or about 9.8 billion units last year.

MEMS-based product sales climbed 15.4% in 2016 to a record-high \$9.7 billion after rising 5.1% in 2015 and 5.8%

Mayor of City of Chengdu. "Over the next six years, we aim to build a world-class ecosystem for FD-SOI and make Chengdu a Center of Excellence for the design and manufacturing of integrated circuits."

GF's 22FDX technology employs a 22nm Fully-Depleted Silicon-On-Insulator (FD-SOI) transistor architecture to deliver the industry's best combination of performance, power and area for wireless, battery-powered intelligent systems. Construction of the new Chengdu fab has commenced and is on schedule with an expected completion date in early 2018. The fab will begin production of mainstream process technologies in 2018 and then focus on manufacturing 22FDX, with volume production expected to start in 2019. ◆

in 2014. Some inventory corrections and steep ASP erosion in MEMS-built devices have suppressed revenue growth in recent years, but this group of products—like the entire sensors/actuator market—is benefitting from increased demand in new wearable systems, IoT, and the rapid spread of intelligent embedded control, such as autonomous automotive features rolling into cars. MEMS-based sensors and actuator sales are forecast to rise 7.9% in 2017 to \$10.5 billion and grow by a CAGR of 8.0% in the 2016-2021 period to \$14.3 billion, says the new O-S-D Report. ◆



Source: IC Insights

FIGURE. A snapshot of the sensors/actuators market.

HPC, chiplets and interposers

The need for ever more computational power continues to grow and exaflop (1018) capabilities may soon become necessary. A paper by AMD on "Design and Analysis of an APU for Exascale Computing" presented at the IEEE High Performance Computing Architectures Conference (HPCA) gave the AMD vision for an exascale node architecture for exascale computing including low-power and high-performance CPU cores, integrated energy-efficient GPU units, in-package high-bandwidth 3D memory, die-stacking and chiplet technologies, and advanced memory systems.

Two of the building blocks for this exascale node architecture are (1) it's chiplet-based approach that decouples performance-critical processing components like CPUs and GPUs from components that do not scale well with technology (e.g., analog components), allowing fabrication in individually optimized process technologies for cost reduction and design reuse in other market segments and (2) the use of in-package 3D memory, which is stacked directly above highbandwidth-consuming GPUs.

The exascale heterogeneous processor (Figure 1) is an accelerated processing unit (APU) consisting of CPU and GPU compute integrated with in-package 3D DRAM. The overall structure makes use of a modular "chiplet" design, with the chiplets 3D-stacked on other "active interposer" chips. "The use of advanced packaging technologies enables a large amount of computational and memory resources to be located in a single package." The exascale targets for memory bandwidth and energy efficiency are incredibly challenging for off-package memory solutions. Thus AMD proposes to integrate 3D-stacked DRAM into the EHP package.

In the center of the EHP are two CPU clusters, each consisting of four multi-core CPU chiplets stacked on an active interposer base die. On either side of the CPU clusters are a total of four GPU clusters, each consisting of two GPU chiplets on a respective active interposer. Upon each GPU chiplet is a 3D stack of DRAM. The DRAM is directly stacked on the GPU chiplets to maximize bandwidth. The interposers underneath the chiplets provide interconnection between the chiplets

along with other functions such as external I/O interfaces,

PHIL GARROU, Contributing Editor

maintain high-bandwidth connectivity among themselves by utilizing wide, short distance, point-to-point paths.

Interposers

power distribution and system

management.



Chiplets

The performance requirements require a large amount of compute and memory to be integrated into a single package. Rather than build a single, monolithic system on chip (SOC), AMD proposes to leverage advanced die-stacking technologies to decompose the EHP into smaller components consisting of active interposers and chiplets. Each chiplet houses either multiple GPU compute units or CPU cores. The chiplet approach differs from conventional multi-chip module (MCM) designs in that each individual chiplet is not a complete chip. For example, the CPU chiplet contains CPU cores and caches, but lacks memory interfaces and external I/O.

A monolithic SOC imposes a single process technology choice on all components in the system. With chiplets and interposers, each discrete piece of silicon can be optimized for its own functions. It is expected that smaller chiplets will have higher yield due to their size, and when combined with KGD testing, can be assembled into larger systems at reasonable cost.

It is expected that the decomposition (or disintegration as I prefer to call it) of the EHP into smaller pieces will enable silicon-level reuse of IP (note – this is one of the main drivers of the DARPA CHIPS program). \clubsuit

Packaging



Mechanistic modeling of silicon ALE for FinFETs

The gate etch in a finFET process requires that 3D corners be accurately resolved to maintain a uniform gate length along the height of the fin. In so doing, the roughness of the etch surface and the exact etch depth per cycle (EPC) are not as critical as the ability of ALE to be resistant to aspect ratio dependent etching (ARDE).



Simulated profiles resulting from etching finFET gates with (a)–(c) a continuous etching process, or (d)–(f) an optimized ALE process. Time increases from left to right, and images represent equal over-etch (as a percentage of the time required to expose the bottom SiO2) not equal etch times. Times listed for the ALE process in (d)–(f) represent plasma-on, ignoring any purge or dwell times. (Source: J. Vac. Sci. Technol. A, Vol. 35, No. 3, May/Jun 2017)

Researchers Chad Huard et al. from the University of Michigan and Lam Research recently published "Atomic layer etching of 3D structures in silicon: Self-limiting and nonideal reactions" in the latest issue of the Journal of Vacuum Science & Technology A. Proper control of sub-cycle pulse times is the key to preventing gas mixing that can degrade the fidelity of ALE.



The Figure shows that the geometry modeled was a periodic array of

vertical crystalline silicon fins, each 10nm wide and 42nm high, set at a pitch of 42 nm. For continuous etching (a-c), simulations used a 70/30 mix of Ar/Cl gas and RF bias of 30V. Just before the etch-front touches the underlying SiO2 (a), the profile has tapered away from the trench sidewalls and the etch-front shows some micro-trenching produced by ions (or hot neutrals) specularly reflected from the tapered sidewalls. After a 25% over-etch (b), a significant amount of Si remains in the corners and on the sides of the fins. Even after an over-etch of 100% (c), Si still remains in the corners.

In comparison, the ALE process (d-f) shows that after 25% over-etch (e) the bottom SiO2 surface would be almost completely cleared with minimal corner residues, and continuing to 100% over-etch results in little change to the profile. The ALE process times shown here do not include the gas purge and fill times between plasma pulses; to clear the feature using ALE required 200 pulses and assuming 5 seconds of purge time between each pulse results in a total process time of 15–20 min to clear the feature. This is a significant increase in total process time over the continuous etch (2 min).

One conclusion of this ALE modeling is that even small deviations from perfectly self-limited reactions significantly compromise the ideality of the ALE process. For example, having as little as 10 ppm Cl2 residual gas in the chamber during the ion bombardment phase produced non-idealities in the ALE. Introducing any source of continuous chemical etching into the ALE process leads to the onset of ARDE and roughening of the etch front. These trends have significant implications for both the design of specialized ALE chambers, and also for the use of ALE to control uniformity. ◆

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The automotive electronics market: A view from a material supplier

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With the increasing sophistication of future vehicles, new and more advanced semiconductor technologies will be used and vehicles will become technology centers.

arge efforts are being deployed in the car industry to transform the driving experience. Electrical vehicles are in vogue and governments are encouraging this market with tax incentives. Cars are becoming smarter, capable of self-diagnostics, and in the near future will be able to connect with each other. Most importantly, the implementation of safety features has greatly reduced the number of accidents and fatalities on the roads in the last few decades. Thanks to extensive computing power, vehicles are now nearing autonomous driving capability. This is only possible with a dramatic increase in the amount of electronic devices in new vehicles.

Recent announcements regarding acquisitions of automotive electronics specialists by semiconductor giants and strategic plans from foundries highlight the appetite from a larger spectrum of semiconductor manufacturers for this particular market. Automotive electronics has become a major player in an industrial transformation.

Automotive electronics is, however, very different from the consumer electronics market. The foremost focus is on product quality, and the highest standards are used to ensure the reliability of electronics components in vehicles. This has also an impact on the quality and supply chain of materials such as gases and chemicals used in the manufacturing of these electronics devices.

Automotive electronics market: size and trends

When you include integrated circuits, optoelectronics, sensors, and discrete devices, the automotive electronics market reached around USD 34 billion in 2016 (**FIGURE 1**).



2

3

4

Source: IC Insights

5

Compound annual growth rate for electronics systems (2015-2020)

FIGURE 1. Compound annual growth rate for electronics systems (2015-2020).

1

0

While this represents less than 10% of the total semiconductor market, it is predicted to be one of the fastest growing markets over the next 5 years.

There are several explanations for such growth potential:

- The vehicle market itself is predicted to steadily grow on an average 3% in the coming 10 years and will be especially driven by China and India, although other developed countries will still experience an increase in sales.
- The semiconductor content in each car is steadily increasing and it is expected that the share of electronic systems in the vehicle cost could reach 50% of the total car cost by 2030 (**FIGURE 2**).

While it is clearly challenging to describe what the driving experience will be in 10 to 15 years, some clear trends can be identified:

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FIGURE 2. Electronic systems as % of total car cost.

• **Safety:** The implementation of integrated vision systems, in connection with dozens of sensors and radars, will allow thorough diagnoses of surrounding areas of the vehicles. Cars will progressively be able to offer, and even take decisions, to prevent accidents.

- **Fuel efficiency:** The share of vehicles equipped with (hybrid) electrical engines is expected to steadily grow. For such engines, the electronics content is estimated to double in value compared to that of standard combustion engines.
- **Comfort and infotainment:** Vehicle drivers are constantly demanding a more enhanced driving experience. The digitalization of dashboards, the sound and video capabilities, and the customization of the driving and passenger environment should heighten the pleasure of time spent in the vehicle.

In order to coordinate all these functions, communication systems (within the vehicle, between vehicles, and between vehicles and infrastructures) are critical and large computing systems will be necessary to treat large amount of data.

Quality really makes automotive electronics different

Automotive electronics cannot be defined by specific technologies or applications. They are currently

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Electronic systems as % of total car cost

consumer	Industrial	Automotive
0 to 40°C	-10 to 70°C	-40 to 160°C
2 to 5 years	5 to 10 years	Up to 15 years
Low	Environment	0% to 100%
Average 1 year	2 to 5 years	Up to 30 years
<10%	<<10%	Target: 0% failure
	0 to 40°C 2 to 5 years Low Average 1 year <10%	0 to 40°C -10 to 70°C 2 to 5 years 5 to 10 years Low Environment Average 1 year 2 to 5 years <10%

Typical operating conditions for different electronics market segments

FIGURE 3. Typical operating conditions for different electronics market segments.

characterized by a very large portfolio of products based on mature technologies, spanning from discrete, optoelectronics, MEMS and sensors, to integrated circuits and memories.

Until now, the automotive electronics market has been the preserve of specialized semiconductor manufacturers with long experience in this field. The reason for this is the specific know-how required for quality management.

A component failure that appears harmless in a consumer product could have major safety consequences for a vehicle in motion. Furthermore, operating conditions of automotive electronics components (temperature, humidity, vibration, acceleration, etc.), their lifetime, and their spare part availability are differentiators to what is common for consumer and industrial devices (**FIGURE 3**).

Currently, some of the most technologically advanced vehicles integrate around 450 semiconductor devices. As they become significantly more sophisticated, the semiconductor content will drastically increase, with many components based on the most advanced semiconductor technology available. Introducing artificial intelligence will require advanced processors capable of computing massive amount of data stored in high-performance and high capacity memory devices. This implies that not only the most advanced semiconductor devices will be used, but that these will need to achieve the highest degree of reliability to allow a flawless operation of predictive algorithms.



FIGURE 4. There are essentially two fields where the material supplier can support its customer: quality and supply chain.

AUTOMOTIVE

It is expected that smart vehicles capable of fully autonomous driving will employ up to 7,000 chips. In this case, even a failure rate of 1ppm, already very low by any standard today, would lead to 7 out of 1,000 cars with a safety risk. This is simply unacceptable.

The automotive electronics industry has therefore introduced quality excellence programs aimed at a zero defect target. Achieving such a goal requires a lot of effort and all constituents of the supply chain must do their part.

The automotive electronics industry is one of the most conservative in terms of change management. Long established standards and documentation procedures ensure traceability of design and manufacturing deviations. Qualification of novel or modified products is generally costly and lengthy. This is where material suppliers can offer competence and expertise to provide material with the highest quality standards.

What does this mean for a material supplier?

As a direct contact to its customer, the material supplier is responsible for the complete supply chain from the source of the raw material to the delivery at the customer's gate. The material supplier is also accountable for long-term supply in accordance with the customer's objectives.

There are essentially two fields where the material supplier can support its customer: quality and supply chain (**FIGURE 4**).

Given the constraints of the automotive electronics market, material qualification must follow extensive procedures. While a high degree of material purity is a prerequisite, manufacturing processes are actually much more sensitive to deviations of material quality, as they potentially lead to process recalibration. Before qualification starts, it is critical that candidate materials are comprehensively documented. This







of quality monitoring and traceability. Certificate of analysis (COA) or consistency checks are not sufficient anymore; more data is required. In case deviation is detected, the investigation and response time must be drastically reduced and allow intervention before delivery to the customer. Finally, the whole supply chain must be monitored.

Measurement systems analysis (MSA), Statistical process/Quality control (SPC/SQC)



includes the manufacturing process, the transport, the storage, and, where appropriate, the purification and transfill operations. Systematic auditing must be regularly performed according to customers' standards. As a consequence, longer qualification times are expected. Any subsequent change in the material specification, origin, and packaging must be duly documented and is likely to be subject to a requalification process.

Material quality is obviously a critical element that must be demonstrated at all times. This commands the usage of high-quality products with a proven record. Sources already qualified for similar applications are preferred to mitigate risks. These sources must show long-term business continuity planning, with process improvement programs in place. Purity levels must be carefully monitored and documented in databases. State-of-the-art analysis methods must be used. When necessary, containment measures should be deployed systematically. Given the long operating lifetime of automotive electronic components, failure can be related to a quality event that occurred a long time before.

Because of the necessary long-term availability of the electronics components and the material qualification constraints, manufacturers and suppliers will generally favor a supply contract over several years. Therefore, the source availability and the supply chain must be guaranteed accordingly.

Material suppliers are implementing improved quality management systems for their products in order to fulfill the expectations of their customers, in terms Several tools must be implemented in order to maintain

a reliable supply chain of high-quality products (**FIGURE 5**): statistical process and quality controls (SPC/SQC), as well as measurement systems analysis (MSA), allow systematic and reliable measurement and information recording for traceability. Implementing these tools particularly at the early stages of the supply chain allows an "in-time" response and correction before the defective material reaches the customer's premises. Furthermore, some impurities that were ignored before may become critical, even below the current detection limits. Therefore, new measurement techniques must be continuously investigated in order to enhance the detection capabilities.

Finally, a robust supply chain must be ensured. It is imperative for a material supplier to be prepared to handle critical business functions such as customer orders, overseeing production and deliveries, and other various parts of the supply chain in any situation. Business continuity planning (BCP) was introduced several years ago in order to identify and mitigate any risk of supply chain disruption.

Analyzing the risks to business operations is fundamental to maintaining business continuity. Materials suppliers must work with manufacturers to develop a business continuity plan that facilitates the ability to continue to perform critical functions and/or provide services in the event of an unexpected interruption. The goal is to identify potential risks and weakness in current sourcing strategies and supply chain footprint and then mitigate those risks.

Because of the efforts necessary to qualify materials, second sources must be available and prepared to be shipped in case of crisis. Ideally, different sources should be qualified simultaneously to avoid any further delay in case of unplanned sourcing changes. Material suppliers with global footprint and worldwide sourcing capabilities offer additional security. Multiple shipping routes must be considered and planned in order to avoid disruption in the case, for instance, of a natural disaster or geopolitical issue affecting an entire region.

Material suppliers need to be aware and monitor regulations specific to the automotive electronics industry such as ISO/TS16949 (quality management strategy for automotive industries). This standard goes above and beyond the more familiar ISO 9001 standard, but by understanding the expectations of suppliers to the automotive industry, suppliers can ensure alignment of their quality systems and the documentation requirements for new product development or investigations into non-conformance.

Future of automotive electronics

With the increasing sophistication of future vehicles, new and more advanced semiconductor technologies will be used and vehicles will become technology centers. These technologies will allow communication and guidance computing. Most of these components (logic or memory) will be built by manufacturers relatively new to the automotive electronics world either integrated device manufacturers (IDM) or foundries.

In order to comply with the current quality standards of the automotive industry, these manufacturers will need to adhere to more stringent standards imposed by the automobile industry. They will find support from materials suppliers like Linde that are capable of delivering high-quality materials associated with a solid global supply chain who have acquired global experience in automotive electronics.

For more information about this topic or Linde Electronics, visit www.linde.com/electronics or contact Francesca Brava at francesca.brava@linde.com. ◆



METROLOGY

Fast and precise surface measurement of backgrinding silicon wafers

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A new type of scattered light measurement method will be presented, capable of measuring the full wafer surface of a 300 mm wafer in less than 30 seconds. Besides the roughness, the sensor simultaneously measures warpage, waviness and defects.

he trend towards very small and high-density electronics requires advanced processes to meet the specifications of thickness and thermal properties of the devices. This means that the processed silicon wafers have to be thinned from their original thickness of more than 700 μ m down to 50 μ m or less. The most common and relative low cost thinning method is back grinding by means of mechanical removal of the residual silicon. The wafer is fixed on a porous vacuum chuck with the IC (integrated circuit) side down. The rotation axis of the grinding wheel is positioned off-axis to the rotation axis of the wafer (distance is the radius of the wafer). The chuck has a slightly conical shape which deforms the wafer with a very little tilt to ensure that the grinding wheel only contacts half of the wafer during the grinding process. Due to the rotation of the chuck and simultaneously rotation of the grinding wheel a typical spiral pattern of scratches on the wafer surface is generated.

Depending on the grit size of the grinding wheel and the machining parameters as rotation speed and feed rate, this mechanical impact is responsible for the roughness, stress and induced subsurface damage. Therefore, a modern wafer grinding machine begins with a coarse grinding wheel to get a fast removal of the silicon and



FIGURE 1. Set-up (left) of the WaferMaster scattered light measurement machine (right).



at the end follows a fine grinding process

or not uniformly distributed on the wafer surface, the later process steps as wire bonding, flip chip assem-

bling, molding and testing can damage the thin chip through breakage. Besides a low surface roughness, the fracture strength of the die after dicing also depends on the orientation of the grinding marks. The correlation of die strength with roughness and surface texture is described in Ref. 1 and 2.

The interaction of the grinding wheel with its large number of single cutting edges, undergoing non-uniform wear, and the silicon surface, in particular when applying the fine grinding procedure is a rather complex process. Therefore, it is not possible to predict the quality of the entire wafer surface after grinding by means of a few small area roughness measurements with an AFM, a WLI or CFM, which is the standard today. Typically, the assessed area of one single measurement is 20 µm x $20\ \mu m$ in case of an AFM and 160 μ m x 160 μ m with a CFM or WLI. Each measurement takes about 20 s-30 s and requires anti-vibration equipment to avoid influence from environmental mechanical noise.

In order to get information of the entire wafer surface, much faster and more robust measurement techniques are necessary. Scattered light measurement is the only method which can achieve these requirements. In the present paper, results of a new measurement machine (WaferMaster 300) are discussed which uses a scattered light sensor [4] to measure the roughness of a full 300 mm wafer surface in less than 30 s. Due to a special design of the sensor the WaferMaster can measure in addition the warpage, waviness and defects.

Measurement principle and surface characterization

Using scattered light to measure surface defects and roughness is already well known for CMP polished bare wafers, pattered wafer, hard disks, mirror surfaces and high quality fine machined automotive parts. The new type of scattered light sensor to measure back- grinding wafer is shown in **FIGURE 1**.

The light source (1) illuminates nearly perpendicular the wafer surface with a 670 nm red LED spot of 0.9







the entire wafer surface and assesses on a 300 mm wafer in the standard modus (0.9 mm spot) about 60.000 single roughness measurements in 30 s. Very important is an additional rotation (7) of the sensor because the linear detector should be always orientated normal to the grinding marks to get the maximum roughness value. As roughness parameter, the variance of the scattered light distribution Aq is calculated (**FIGURE 2**). ψ i are the single scattered angles, M is the center

of gravity and $p(\psi)$ is the distribution curve.

The advantage of Aq is the close relation with the profile slope parameter Rdq which describes surface friction very well. To follow the Semi standards in which the mean roughness Ra is established as roughness value, the Aq parameter was correlated with Ra by comparison measure- ments of different wafers with a confocal microscope. Due to the stochastically property of the amplitude distribution of the ground surface there is a rather good correlation between Aq and Ra even when using different grit size of the grinding wheel. But it should be taken into account that Aq is a more versatile parameter, because it reacts on both the vertical and lateral structures of a profile whereas Ra only measures the mean vertical height. This property of Aq could be interesting for characterizing







FIGURE 5. Back grinding 200 mm wafer. Left: Roughness Ra, middle: warpage; right: waviness.

FIGURE 2. Geometrical model of scattered light. Above: roughness, below: form measurement.

mm spot size (2). This is the standard modus for fast measurement with medium lateral resolution. For high lateral resolution, another spot with 0.03 mm diameter from a laser source with the same wavelength can be switched on. The optics (3) collect the scattered light in an angle range of 32° and guides it to the linear detector (4). In contrast to other scattered light sensors this sensor measures the specular light (0°-part of the surface) together with the scattered light created by the microstructures of the surface. The advantage of this set-up is the capability to use the center of gravity of the scattered light distribution (5) as signal of the local geometrical deformation of the surface. Knowing the local slope angle of the surface and measuring continuously the surface in equal distance (created by an encoder signal) the local height can be calculated and, by integration of all angles, the entire profile of the surface.

The chuck with the wafer (6) rotates continuously during the measurement and the sensor moves linearly from the wafer edge to the center. Subsequently the sensor measures



FIGURE 3. Correlation measurements Ra (nm) = f(Aq).



die strength and should be investigated in more details in the future. In **FIGURE 3** the measured correlation is shown. Several wafers were in- vestigated on different areas and ground with different grit sizes from #2000 to #8000. In addition, a CMP polished wafer with a Ra value <1nm was measured to check the accuracy of the system. In order to calculate the Ra-value the fitted correlation equation is used in the WaferMaster machine.

As already mentioned, the scattered light sensor has a second evaluation channel to measure warpage and waviness by means of slope angle analysis. As shown in Fig. 2, the measurement beam is deflected under 2x the local slope angle θ . Therefore, the scattered light distribution is shifted on the linear detector by the angle value M. θ can be measured by using the first statistical moment of the scattered light distribution curve. Knowing the step size Δx from an encoder and the focal length of the optics, the local height Δy can be calculated and by sum up, the height profile can be generated.

Results

In **FIGURE 4** the roughness results of 3 wafers are shown, each 300 mm size. They all were ground with the same grinding wheel (grit size #4000), but using different grinding machines. In total 40.000 measurements were taken in 25 s with the 0.9 mm spot. Besides the difference in the mean roughness value, it demonstrates in particular that the machines did leave its own characteristic pattern. The interpretation might be interesting to analyze in detail the grinding parameters as feed rate, chuck geometry, rotation speed, and others.

An example of the simultaneous measurement of roughness, form (warp) and waviness of a 200 mm back grinding wafer can be seen in **FIGURE 5**. Although the grinding wheel was also grit size #4000, the mean Ra value is a bit higher. From the grinding marks pattern, it can be seen that the rotation was counterclockwise which changes the orientation from left to right. The warp is



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FIGURE 6. Roughness Ra (left) and waviness map (right) of a wafer ground with a #2000 grit size grinding wheel.

rather high because no vacuum was used. The waviness was calculated by applying a 50 waves high-pass filter. The filter is working on the circumference which means that the center area is filtered strongly than at the edge and middle area. Different filter method will be used in the future. The waviness structure follows the roughness pattern, but there are also visible some superimposed weak linear stripes from left to right. These stripes are more prominent in the following measurement (FIGURE 6), which is the result of another 200 mm wafer but ground with a #2000 grit wheel. The interesting point is not the higher roughness, which is induced by the coarser grinding wheel, but that the stripes here are more prominent than the waviness pattern of the grinding marks. The peak to valley height evaluated from A to B is more than $1 \mu m$, which is about 10 times the profile height of the grinding marks waviness.

The linear stripes are probably caused by the previous wire sawing process, which did not vanish after the grinding

process. This could happen, because the wafer is fixed by vacuum on the chuck during grinding which makes the surface temporarily flat. When the wafer is released after the grinding process the waviness structures return. This phenomenon is investigated and described by Pei et al [3]. Furthermore, if the chuck is not cleaned very well the same characteristic can create bumps and dimples. An example of dimples is shown in **FIGURE 7**. The waviness map of a 300 mm polished wafer is covered with 2 larger and some smaller dimples. By using the 0.03 mm sensor spot the larger dimples where measured again with higher local resolution and represented in a 3D map. The width is in the mm range whereas the depth does not exceed 1 μ m.

Another example of high resolution measurement can be seen in Fig. 8 These measurements were done with an x/y-scanning module covering an area of 40 mm x 20 mm, also by using the small spot size of 0.03 mm. The measurements represent the waviness structures (after applying a 25 waves high pass filter). The mean roughness is 5 nm Ra. Near the center of this section another dimple is visible. The selected profile (a) shows the general waviness with a peak to valley height of



FIGURE 7. 300 mm polished wafer with dimples (right). High resolution measurement with 0.03 mm measurement spot in 3D representation (left).



FIGURE 8. Fine-grinding silicon wafer surface measured with high lateral resolution (0.03 mm spot) left: 20mm x 40 mm area waviness measurement with profile. Right: same area but profile selection across a dimple.

about 30 nm. Repeatability measurements have shown that structures of 1 nm height could be resolved.

This makes the WaferMaster moreover interesting for the assessment of nanotopography structures to measure the planarization quality after CMP processes. Also, as can be seen in the 3D graphic, the small spot is able to detect single defects (red peak at the right side) and it has to be investigated, what the limit of lowest defects is. Certainly, it cannot compete with the much more powerful scattered light systems, especially designed for small defect detection in the front-end industry, but it is sufficient to use this function in backend processes.

Summary

A new scattered light sensor technique was presented to measure wafer surfaces, particular in the field of back grinding. The sensor combines surface roughness measurement by means of evaluating the variance (Aq) of the scattered light distribution and use additionally the method of deflectometry to assess form (warpage) and waviness. The Ra evaluation is based on correlation measurements with a confocal microscope. It could be shown that the sensitivity of roughness measurements is going down to Ra = 1 nm with an accuracy of 0.1 nm. The advantage of this technique is the speed (25 s for a whole 300 mm wafer scan) and the ruggedness against environmental mechanical noise. The capability of the full area representation of roughness, warpage and waviness opens new possibilities to characterize and improve the grinding processes as well as checking the quality from the edge area to the center completely.

Depending on the packaging design and the sensitivity of the processes which follow after the back grinding, the difference of the roughness from edge to the center and along the circumference, as well as strong warpage, waviness and defects can influence the final function and performance of the singulated chips. Die breakage e.g. directly depends on the roughness and in particular on the grinding marks orientation. Therefore, a fast and continuous measurement of the back-grinding quality can help to improve the yield in the backend process.

Acknowledgement

We would like to give special thanks to Kevin Hsu from Sanpany and Ian Chen, Honjang Global Technology for their kindly support in organizing the wafer samples and to confirm our CFM measurements with an WLI microscope.

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Having confidence in your confidence level

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Did you take enough measurements to be confident in the result?

hile working at the Guinness[®] brewing company in Dublin, Ireland in the early-1900s, William Sealy Gosset developed a statistical algorithm called the T-test [1]. Gosset used this algorithm to determine the best-yielding varieties of barley to minimize costs for his employer, but to help protect Guinness' intellectual property he published his work under the pen name "Student." The version of the T-test that we use today is a refinement made by Sir Ronald Fisher, a colleague of Gosset's at Oxford University, but it is still commonly referred to as Student's T-test. This paper does not address the mathematical nature of the T-test itself but rather looks at the amount of data required to consistently achieve the ninety-five percent confidence level in the T-test result.

A T-test is a statistical algorithm used to determine if two samples are part of the same parent population. It does not resolve the question unequivocally but rather calculates the probability that the two samples are part of the same parent population. As an example, if we developed a new methodology for cleaning an etch chamber, we would want to show that it resulted in fewer fall-on particles. Using a wafer inspection system, we could measure the particle count on wafers in the chamber following the old cleaning process and then measure the particle count again following the new cleaning process. We could then use a T-test to tell if the difference was statistically significant or just the result of random fluctuations. The T-test answers the question: what is the probability that two samples are part of the same population?

However, as shown in **FIGURE 1**, there are two ways that a T-Test can give a false result: a false positive or a false negative. To confirm that the experimental data is actually different from the baseline, the T-test usually has to score less than 5% (i.e. less than 5% probability of a false positive). However, if the T-test scores greater than 5% (a negative result), it doesn't tell you anything about the probability of that result being false. The probability of false negatives is governed by the number of measurements. So there are always two criteria: (1) Did my experiment pass or fail the T-test? (2) Did I take enough measurements to be confident in the result? It is that last question that we try to address in this paper.

Changes to the semiconductor manufacturing process are expensive propositions. Implementing a change that doesn't do anything (false positive) is not only a waste of time but potentially harmful. Not implementing a change that could have been beneficial (false negative) could cost tens of millions of dollars in lost opportunity. It is important to have the appropriate degree of confidence in your results and to do so requires that you use a sample size that is appropriate



FIGURE 1. A "Truth Table" highlights the two ways that a T-Test can give the wrong result.

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FIGURE 2. Both charts show the same absolute change, before and after, but 2B (right) has much lower standard deviation. When the change is small relative to the standard deviation as in 2A (left) it will require more data to confirm it.

for the size of the change you are trying to affect. In the example of the etch cleaning procedure, this means that inspection data from a sufficient number of wafers needs to be collected in order to determine whether or not the new clean procedure truly reduces particle count.

In general, the bigger the difference between two things, the easier it is to tell them apart. It is easier to tell red from blue than it is to distinguish between two different shades of red or between two different shades of blue. Similarly, the less variability there is in a sample, the easier it is to see a change 2. In statistics the variability (sometimes referred to as noise) is usually measured in units of standard deviation (σ). It is often convenient to also express the difference in the means of two samples in units of σ (e.g., the mean of the experimental results was 1σ below the mean of the baseline). The advantage of this is that it normalizes the results to a common unit of measure (σ). Simply stating that two means are separated by some absolute value is not very informative (e.g., the average of A is greater than the average of B by 42). However, if we can express that absolute number in units of standard deviations, then it immediately puts the problem in context and instantly provides an understanding of how far apart these two values are in relative terms (e.g., the average of A is greater than the average of B by 1 standard deviation).

FIGURE 2 shows two examples of data sets, before and after a change. These can be thought of in terms of the etch chamber cleaning experiment we discussed earlier. The baseline data is the particle count per



wafer before the new clean process and the results data is the particle count per wafer after the new clean procedure. Fig. 2A shows the results of a small change in the mean of a data set with high standard deviation and Fig. 2B shows the results of the same sized change in the mean but with less noisy data (lower standard deviation). You will require more data



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FIGURE 3. The Standard Error (SE) in the average of two samples with different means. In this case the standard deviation is the same in both data sets but that need not be the case. With greater than x measurements the error bars no longer overlap and one can state with 95% confidence that the two populations are distinct.

(e.g., more wafers inspected) to confirm the change in Fig. 2A than in Fig. 2B simply because the signalto-noise ratio is lower in 2A even though the absolute change is the same in both cases.

The question is: how much data do we need to confidently tell the difference? Visually, we can see this when we plot the data in terms of the Standard Error (SE). The SE can be thought of as the error in calculating the average (e.g., the average was X +/- SE). The SE is proportional to σ/\sqrt{n} where n is the sample size. **FIGURE 3** shows the SE for two different samples as a function of the number of measurements, n.

For a given difference in the means and a given standard deviation we can calculate the number of measurements, x, required to eliminate the overlap in the Standard Errors of these two measurements (at a given confidence level).

The actual equation to determine the correct sample size in the T-test is given by,

$$n = \frac{2(Z_{\beta} + Z_{1-\alpha/2})^2}{\text{Delta}^2}$$

EQUATION 1.

where n is the required sample size, "Delta" is the difference between the two means measured in units of standard deviation (σ and Z_x is the area under the T distribution at probability x. For α =0.05 (5%)

chance of a false positive) and β =0.95 (5% chance of a false negative), $Z_{1\text{-}\alpha/2}$ and Z_{β} are equal to 1.960 and 1.645 respectively (Z values for other values of α and β are available in most statistics textbooks, Microsoft[®] Excel[®] or on the web). As seen in Figure 3 and shown mathematically in Eq 1, as the difference between the two populations (Delta) becomes smaller, the number of measurements required to tell them apart will become exponentially larger. FIGURE 4 shows the required sample size as a function of the Delta between the means expressed in units of σ . As expected, for large changes, greater than 3σ , one can confirm the T-test 95% of the time with very little data. As Delta gets smaller, more measurements are required to consistently confirm the change. A change of only one standard deviation requires 26 measurements before and after, but a change of 0.5σ requires over 100 measurements.



FIGURE 4. Sample size required to confirm a given change in the mean of two populations with 5% false positives and 5% false negatives.

The relationship between the size of the change and the minimum number of measurements required to detect it has ramifications for the type of metrology or inspection tool that can be employed to confirm a given change. **FIGURE 5** uses the results from figure 4 to show the time it would take to confirm a given change with different tool types. In this example the sample size is measured in number of wafers. For fast tools (high throughput, such as laser scanning wafer inspection systems) it is feasible to confirm relatively small improvements ($<0.5\sigma$) in the process because they can make the 200 required measurements (100 before and 100 after) in a relatively short time. Slower tools such as e-beam inspection systems are limited to detecting only gross changes in the process, where the improvement is greater than 2σ . Even here the measurement time alone means that it can be weeks

PROCESS WATCH



FIGURE 5. The measurement time required to determine a given change for process control tools with four different throughputs (e-Beam, Broadband Plasma, Laser Scattering and Metrology).

before one can confirm a positive result. For the etch chamber cleaning example, it would be necessary to quickly determine the results of the change in clean procedure so that the etch tool could be put back into production. Thus, the best inspection system to determine the change in particle counts would be a high throughput system that can detect the particles of interest with low wafer-to-wafer variability.

Experiments are expensive to run. They can be a waste of time and resources if they result in a false positive and can result in millions of dollars of unrealized opportunity if they result in a false negative. To have the appropriate degree of confidence in your results you must use the correct sample size (and thus the appropriate tools) that correspond to the size of the change you are trying to affect.

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Author's Note: The Process Watch series explores key concepts about process control—defect inspection and metrology—for the semiconductor industry. Following the previous installments, which examined the 10 fundamental truths of process control, this new series of articles highlights additional trends in process control, including successful implementation strategies and the benefits for IC manufacturing. ◆





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TECH TRENDS

What TechInsights analysts are watching in 2017

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TechInsights analysts share their view on where technology is going, how it's changing, and what new developments are emerging.

n 2016, wearables were extremely interesting mainly because there was so much uncertainty around whether or not the market will be viable. The year saw some truly low-cost smart and fitness devices, and some market surprises like Fitbit buying Pebble. The Apple Watch 2 was an improvement over the Watch 1. However, the Huawei watch is remarkably designed with a nice round face, and functional, making the decision on which smartwatch to buy difficult.

While wearables will remain intriguing, even more interesting to watch is the wearables market. Hearables can be as simple as ear buds and basic hearing aids or as complex as devices that correct and amplify sound, sync with wireless devices for virtually any application, and even measure biometric outputs. That's just the beginning. New sensors being packed into small devices are bringing us devices with nearly 30 sensors per device. Our recent AirPod teardown (**FIGURES 1** and **2**) sheds even more light on what's happening in this area. The W1 chip found in the Beats Studio wireless headphone has the package mark 343S00131. Meanwhile, the W1 chip torn down from the Apple AirPods has the package mark 343S00130. They have a slight difference in the last digit in the package marks. TechInsights has confirmed that both 343S00131 and 343S00130 have the same die. This die measures 4.42 mm x 3.23 mm = 14.3 mm2 . TechInsights has been tracking Internet of Things (IoT) SoCs for over a year and our observations indicate that this new W1 SoC is very competitively placed when comparing its die size and connectivity specification of Bluetooth 4.2 or greater.

Another extremely interesting technology to watch is the rise of intelligent personal or family assistants. This market started with the introduction of the popular Alexa and Echo. Sony may release their assistant this year with more sure to follow. As far as timing, we will have to wait



FIGURE 2. The W1 chip found in the Beats Studio wireless headphone is the same as that torn down from the Apple AirPods.

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and see. One issue that needs to be addressed is data collection and usage vs. persona privacy in a manner similar to Vizio's issues with the FTC. In addition, more changes are coming for artificial intelligence or assistants on mobile devices with Samsung announcing Bixby ahead of its G8 launch.

Of course there are a slew of IoT technologies to watch like the acceptance of Zigbee, Z-Wave, LoRa, and Bluetooth 5.0, all of which seem to be vying aggressively for consumer IoT/connected home market. Rumors are gaining strength around how the Samsung S8 will have Bluetooth 5, which could mean a new WiFi modem, from whom we are not certain. Samsung and Wisol have been aligned for a while, but it would be a big statement to see a Samsung/Wisol WiFi/ Bluetooth modem design supporting a new technology like Bluetooth 5.0 in a flagship phone. Based on our knowledge of the Bluetooth Special Interest Group, we don't believe that Bluetooth 5.0 has to be declared for a product. If fact, it would almost seem as if the SiG is asking OEMs to not make a declaration of the Bluetooth 5 in the device.

Image sensors

2016 was an exciting year for smartphone cameras, which should be considered as one of the biggest hardware differentiators between mobile handset platforms. Dual camera systems have reached the mainstream and are forecasted to drive growth for CMOS image sensor IDMs and foundries. Samsung introduced full chip Dual Pixels implemented in chips from its team and from Sony. Each Dual Pixel photosite is available as an autofocus (AF) point, and this complements traditional contrast AF methods and the emerging laser + time-of-flight (ToF) systems.

In 2017, ToF is expected to be a key differentiator in mobile platforms, both for AF and for new 3D/ranging functionality. Sony has introduced first generation direct bond interconnect (DBI) as a through silicon via (TSV) replacement and we expect tighter pitch DBI and eventually full chip active DBI going forward. On the image signal processor (ISP) side we are seeing a big push to lower nodes (28 nm ISPs are the state-of-the-art for high end stacked CIS chips). The flexibility offered by chip stacking should lead to new and disruptive partnerships between CMOS image sensor specialists and mixed signal advanced CMOS specialists. Finally, we expect new entrants to the digital imaging and sensing landscape. Machine vision, robotics, ranging, surveillance/security, and automotive vision and sensing applications are all positioned for growth due to enabling functionality and continued performance



FIGURE 3.

gains. It's certainly an exciting time for all involved in designing and fabricating imaging and sensing pixel arrays and camera systems!

Memory devices

Last year virtually every vendor, device manufacturers, R&D engineer and market analyst we talked to was focused on DRAM and NAND technology roadmaps. We still talk to clients today who are focused on the future of these technologies. Today, 32L and 48L 3D NAND products are common and all the NAND players are eager to develop the next generation 3D NAND products such as 64L and 128L or even more (FIGURE **3**). TechInsights has been analyzing and comparing these devices regularly. We found that 3D NAND is a kind of revolution for memory devices, and because of it, big data or data center, SSD/SD and related technologies like controller, interface and board/package, are moving forward. In addition, they may be able to keep pace for more than the next five years until any new emerging memory devices are commercialized.

The memory products/technologies we are anticipating this year are 3D NAND technology with 64L, 72L and 128L and 1x and 1y nm DRAM technology. As always, 3D NAND technology is competitive with emerging memory including X-point memory regarding on the performance, reliability, retention, process integration and cost since X-point memory and crossbar devices such as ReRAM, CBRAM, MRAM and PCRAM are likely not cost effective (bit cost).



While Samsung has already revealed 1x nm DRAM, in 2017, we believe there will be another big area of competition in DRAM technology (**FIGURE 4**). DRAM cell has 1T1C architecture with a cylindrical capacitor, however, nowadays, the cell capacitance cannot meet the capacitance spec (20fF/ cell). Commercial DRAM products such as Samsung's 18nm DRAM have just about 12fF/cell. With smaller cell



nodes, it is absolutely harder to get the sufficient cell capacitance. Nevertheless, Samsung and SK-hynix are confident in developing n+1 (1y nm) and n+2 (1z nm). We anticipate that in 2017, every DRAM maker will be developing 1x and 1y nm commercial DRAM products. How these rollout and perform remains to be seen.

Finally, we are anticipating a commercial product using X-point memory from Micron and Intel.

FIGURE 4. DRAM cell size for Samsung, SK Hynix and Micron.

Conclusion

These represent some of the major technologies we have our eye on this year, although we fully anticipate seeing new technologies we can only imagine today emerge. After all, change is truly the only constant in our world. As our analysts continue to examine and reveal the innovations other can't inside advanced technology, we will continue to share our findings on the technologies noted above, how they are used, and how they will be changed by the next discovery or invention. ◆

Edge placement error control in multi-patterning

ED KORCZYNSKI, Sr. Technical Editor

SPIE presentations show materials dominate patterning.

PIE Advanced Lithography remains the technical conference where the leading edge of minimum resolution patterning is explored, even though photolithography is now only part of the story. Leading OEMs continue to impress the industry with more productive ArFi steppers, but the photoresist suppliers and the purveyors of vacuum deposition and etch tools now provide most of the new value-add. Tri-layer-resist (TLR) stacks, specialty hard-masks and anti-reflective coatings (ARC), and complex thin-film depositions and etches all combine to create applicationspecific lithography solutions tuned to each critical mask.

Multi-patterning using complementary lithography using argon-fluoride immersion (ArFi) steppers to pattern 1D line arrays plus extreme ultra-violet (EUV) tools to do line cuts—is under development at all leading edge fabs today. **FIGURE 1** shows that edge placement error (EPE) in lines, cut layers, and vias/ contacts between two orthogonal patterned layers can result in shorts and opens. Consequently, EPE control is critical for yield within any multi-patterning process flow, including litho-etch-litho-etch (LELE), self-aligned double-patterning (SADP) and self-aligned quadruplepatterning (SAQP).





Happening the day before the official start of SPIE-AL, Nikon's LithoVision event featured a talk by Intel Fellow and director of lithography hardware solutions Mark Phillips on the big picture of how the industry may continue to pattern smaller IC device features. Regarding the timing of Intel's planned use of EUV litho technology, Phillips re-iterated that, "It's highly desirable for the 7nm node, but we'll only use it when it's ready. However, EUVL will remain expensive even at full productivity, so 193i and multi-patterning will continue to be used. In particular, we'll need continued improvement in the 193i tools to meet overlay."

Yuichi Shibazaki— Nikon Fellow and the main architect of the current generation of Nikon steppers explained that the current generation of 193i steppers, featuring throughputs of >200 wafers per hour, have already been optimized to the point of diminishing returns. "In order to improve a small amount of performance it requires a lot of expense. So just improving tool performance may not decrease chip costs." Nikon's latest productivity offering is a converted alignment station as a stand-alone tool, intended to measure every product wafer before lithography to allow for feed-forward tuning of any stepper; cost and cost-of-

> ownership may be disclosed after the first beta-site tool reaches a customer by the end of this year.

"The 193 immersion technology continues to make steady progress, but there are not as many new gamechanging developments," confided Michael Lercel, Director of Strategic Marketing for ASML in an exclusive interview with SemiMD. "A major theme of several SPIE papers is on EPE, which traditionally we looked at

as dependent upon CD and overlay. Now we're looking at EPE in patterning more holistically, with need to control



the complexity with different error-variables. The more information we can get the more we can control."

At LithoVision this year, John Sturtevant—SPIE Fellow, and director of RET product development in the Design to Silicon Division at Mentor Graphics discussed the challenges of controlling variability in multi-layer patterning. "A key challenge is predicting and then mitigating total EPE control," reminded Sturtevant. "We've always paid attention to it, but the budgets that are available today are smaller than ever. Edge-placement is very important." At the leading edge, there are multiple steps within the basic litho flow that induce proximity/local-neighbor effects which must be accounted for in EDA: mask making, photoresist exposure, post-exposure bake (PEB), pattern development, and CD-SEM inspection (wherein there is non-zero resist shrinkage).

Due to the inherent physics of EUV lithography, as well as the atomic-scale non-uniformities in the reflective mirrors focusing onto the wafer, EUV exposure tools show significant variation in exposure uniformities. "For any given slit position there can be significant differences between tools. In practice, we have used a single model of OPC for all slit locations in all scanners in the fab, and that paradigm may have to change," said Sturtevant. "It's possible that because the variation



FIGURE 2. 3D schematics (top) and plan view SEM images (bottom) showing that control of plasma parameters can tune the byproducts of etch processes to significantly reduce the line-width roughness (LWR) of minimally scaled lines. (Source: Applied Materials)

across the scanner is as much as the variation across the slit, it could mean we'll need scanner-specific cross-slit computational lithography." More than 3nm variation has been seen across 4 EUVL steppers, and the possible need for tool-specific optical proximity correction (OPC) and source-mask optimization (SMO) would be horrible for managing masks in HVM.

Thin Films Extend Patterning Resolution

Applied Materials has led the industry in thin-film depositions and etches for decades, and the company's production proven processing platforms are being used more and more to extend the resolution of lithography. For SADP and SAQP MP, there are tunable unit-processes established for sidewall-spacer depositions, and chemical downstream etching chambers for mandrel pull with extreme material selectivity. CVD of dielectric and metallic hard-masks when combined with highly anisotropic plasma etching allows for devicespecific and mask-specific pattern transfers that can reduce the line width/edge roughness (LWR/LER) originally present in the photoresist. **FIGURE 2** from the SPIE-AL presentation "Impact of Materials Engineering on Edge Placement Error" by Regina Freed, Ying Zhang, and Uday Mitra of Applied Materials, shows LER reduction from 3.4 to 1.3 nm is possible after etch. The company's Sym3 chamber features very high gas conductance to prevent etch byproducts from dissociation and re-deposition on resist sidewalls.

TEL's new SAQP spacer-on-spacer process builds on the work shown last year, using oxide as first spacer and TiO2 as second spacer. Now TEL is exploring silicon as the mandrel, then silicon-nitride as the first spacer, and titanium-oxide as second spacer. This new flow can be tuned so that all-dry etch in a single plasma etch chamber can be used for the final mandrel pull and pattern transfer steps.

Coventor's 3D modeling software allows companies to do process integration experiments in virtual space, allowing for estimation of yield-losses in pattern transfer due to variations in side-wall profiles and LER. A simulation of 9 SRAM cells with 54 transistors shows that photoresist sidewall taper angle determines both the size and the variability of the final fins. The final capacitance of low-k dielectric in dual-damascene copper metal interconnects can be simulated as a function of the initial photoresist profile in a SAQP flow. ◆

Lithographic stochastic limits on resolution

ED KORCZYNSKI, Sr. Technical Editor

It's difficult to cheat physics and make a profit.

he physical and economic limits of Moore's Law are being approached as the commercial IC fab industry continues reducing device features to the atomic-scale. Early signs of such limits are seen when attempting to pattern the smallest possible features using lithography. Stochastic variation in the composition of the photoresist as well as in the number of incident photons combine to destroy determinism for the smallest devices in R&D. The most advanced Extreme Ultra-Violet (EUV) exposure tools from ASML cannot avoid this problem without reducing throughputs, and thereby increasing the cost of manufacturing.

Since the beginning of IC manufacturing over 50 years ago, chip production has been based on deterministic control of fabrication (fab) processes. Variations within process parameters could be controlled with statistics to ensure that all transistors on a chip performed nearly identically. Design rules could be set based on assumed in-fab distributions of CD and misalignment between layers to determine the final performance of transistors.

As the IC fab industry has evolved from micron-scale to nanometer-scale device production, the control of lithographic patterning has evolved to be able to bendlight at 193nm wavelength using Off-Axis Illumination (OAI) of Optical-Proximity Correction (OPC) mask features as part of Reticle Enhancement Technology (RET) to be able to print <40nm half-pitch (HP) line arrays with good definition. The most advanced masks and 193nm-immersion (193i) steppers today are able to focus more photons into each cubic-nanometer of photoresist to improve the contrast between exposed and non-exposed regions in the areal image. To avoid escalating cost and complexity of multi-patterning with 193i, the industry needs Extreme Ultra-Violet Lithography (EUVL) technology. Dr. Britt Turkot, who has been leading Intel's integration of EUVL since 1996, reassured a standing-room-only crowd during a 2017 SPIE Advanced Lithography keynote address that the availability for manufacturing of EUVL steppers has been steadily improving. The new tools are close to 80% available for manufacturing, but they may need to process fewer wafers per hour to ensure high yielding final chips.

The KLA-Tencor Lithography Users Forum was held in San Jose on February 26 before the start of SPIE-AL; there, Turcot also provided a keynote address that mentioned the inherent stochastic issues associated with patterning 7nm-node device features. We must ensure zero defects within the 10 billion contacts needed in the most advanced ICs. Given 10 billion contacts it is statistically certain that some will be subject to 7-sigma fluctuations, and this leads to problems in controlling the limited number of EUV photons reaching the target area of a resist feature. The volume of resist material available to absorb EUV in a given area is reduced by the need to avoid pattern-collapse when aspect-ratios increase over 2:1; so 15nm half-pitch lines will generally be limited to just 30nm thick resist. "The current state of materials will not gate EUV," said Turkot, "but we need better stochastics and control of shot-noise so that photoresist will not be a long-term limiter."

CONTACT HOLE DIAMETER	24nm	16nm
INCIDENT EUV PHOTONS	4610	2050
# ABSORBED IN AREAL IMAGE	700	215

TABLE 1. EUVL stochastics due to scaled contact hole size. (Source: Intel Corp.)

From the LithoGuru blog of gentleman scientist Chris Mack: One reason why smaller pixels are harder to control is the stochastic effects of exposure: as you decrease the



number of electrons (or photons) per pixel, the statistical uncertainty in the number of electrons or photons actually used goes up. The uncertainty produces line-width errors, most readily observed as line-width roughness (LWR). To combat the growing uncertainty in smaller pixels, a higher dose is required.

We define a "stochastic" or random process as a collection of random variables and a Wiener process as a continuous-time stochastic process in honor of Norbert Wiener. Brownian motion and the thermallydriven diffusion of molecules exhibit such "randomwalk" behavior. Stochastic phenomena in lithography include the following:

- Photon count,
- Photo-acid generator positions,
- Photon absorption,
- Photo-acid generation,
- Polymer position and chain length,
- Diffusion during post-exposure bake,
- Dissolution/neutralization, and
- Etching hard-mask.

FIGURE 1 shows the stochastics within EUVL start with direct photolysis and include ionization and scattering within a given discrete photoresist volume, as reported by Solid State Technology in 2010.



FIGURE 1. Discrete acid generation in an EUV resist is based on photolysis as well as ionization and electron scattering; stochastic variations of each must be considered in minimally scaled areal images. (Source: Solid State Technology)

Resist R&D

During SPIE-AL this year, ASML provided an overview of the state of the craft in EUV resist R&D. There has been steady resolution improvement over 10 years with Photo-sensitive Chemically-Amplified Resists (PCAR) from 45nm to 13nm HP; however, 13nm HP needed 58 mJ/cm2, and provided DoF of 99nm with 4.4nm LWR. The recent non-PCAR Metal-Oxide Resist (MOR) from Inpria has been shown to resolve 12nm HP with 4.7 LWR using 38 mJ/cm2, and increasing exposure to 70 mJ/cm2 has produced 10nm HP L/S patterns.

In the EUVL tool with variable pupil control, reducing the pupil fill increases the contrast such that 20nm diameter contact holes with 3nm Local Critical-Dimension Uniformity (LCDU) can be done. The challenge is to get LCDU to <2nm to meet the specification for future chips. ASML's announced next-generation N.A. >0.5 EUVL stepper will use anamorphic mirrors and masks which will double the illumination intensity per cm2 compared to today's 0.33 N.A. tools. This will inherently improve the stochastics, when eventually ready after 2020.

The newest generation EUVL steppers use a membrane between the wafer and the optics so that any resist out-gassing cannot contaminate the mirrors, and this allow a much wider range of materials to be used as resists. Regarding MOR, there are 3.5 times more absorbed photons and 8 times more electrons generated per photon compared to PCAR. Metal hard-masks (HM) and other under-layers create reflections that have a significant effect on the LWR, requiring tuning of the materials in resist stacks.

Default R&D hub of the world imec has been testing EUV resists from five different suppliers, targeting 20 mJ/cm₂ sensitivity with 30nm thickness for PCAR and 18nm thickness for MOR. All suppliers were able to deliver the requested resolution of 16nm HP line/space (L/S) patterns, yet all resists showed LWR >5nm. In another experiment, the dose to size for imec's "7nm-node" metal-2 (M2) vias with nominal pitch of 53nm was ~60mJ/cm₂. All else equal, three times slower lithography costs three times as much per wafer pass. \blacklozenge



How SEMI Standard E175 is saving energy and cutting costs

Industry experts answer questions about the new standard in a virtual roundtable.

n recent years, energy consumption has decreased due to several innovations that have helped to improve the energy efficiency of process tools and sub-fab equipment, but an increase in the number of processes and the growing complexity of processing at the current node has resulted in a spike in energy consumption in the fab. Approximately 43% of the energy consumed in the fab is due to the processing equipment and, of this, 20% is vacuum and abatement (8% overall).

A new standard from SEMI, E175, defines energy saving modes, which combined with the EtherCAT signaling standard, can help fabs save energy and other gas/utility costs when the tool is not processing and with no impact on subsequent wafer processing.

EtherCAT, based on industrial Ethernet, provides highspeed control and monitoring. It is the communication standard of choice for the latest semiconductor tool controllers to connect to sensors and actuators around the tool, including vacuum and abatement systems.

SEMI E175 defines how process tools communicate with sub-fab equipment, such as vacuum pumps and gas abatement systems, to reduce utility consumption at times when wafers are not being processed by the tool, and returning to full performance when the tool is again required to process wafers. It builds on SEMI E167, which defines communication between the fab host/ WIP controller and the process tools for the purpose of utility saving.

Collaboration between the E175 and EtherCAT groups has seen a harmonization of the communication standards to provide co-ordinated energy saving across devices in the fab.

We invited experts in this area to answer a few questions in a virtual roundtable. The participants are:

- **GERALD SHELLEY**, Senior Product Manager Communication and Control at Edwards, and the EtherCAT Chair Abatement / Roughing pump working groups, E175 task force.
- **MIKE CZERNIAK**, Environmental Solutions Business Development Manager at Edwardsm Co-Chair of E167 & E175, and campaigner for energy saving
- **GINO CRISPIERI**, Applied Materials Past Co-chair of E175 (originally SEMATECH/ISMI, then independent consultant, prior to Applied Materials)
- **MARTIN ROSTAN**, Executive Director, EtherCAT Technology Group

Q: Please explain what drove the standards work on energy saving and the achievements to date.

SHELLEY: There is increased pressure on the industry to reduce energy and utility saving from both a cost and environmental standpoint. Subfab equipment is a major consumer of utilities, which is wasted when a tool is not in use. Different manufacturers have implemented energy saving solutions, with minimal direct connection to the tool. However, direct tool connection has emerged as the best way to maximize saving without any risk to wafer processing.

CZERNIAK: This work originated in the ISMI part of SEMATECH as a follow-on to generic work aimed at reducing the overall utilities footprint of modern fabs. In response to this and requests from customers, Edwards developed vacuum pumps and gas abatement systems that had energy-saving functionality. However, it soon became clear that the limitation to implementing such savings was the absence of standardised signalling between the process tool and sub-fab equipment.

CRISPIERI: A SEMATECH project around 2009 started to look into opportunities for saving energy in the semiconductor factories. At that time, suppliers of pumps

and abatement systems already had started initiatives to provide their own solutions to the initiative. Since that time, the industry has adopted two new standards: SEMI E167 Specification for Equipment Energy Saving Mode Communication (between factory and semiconductor equipment) and SEMI E175 Specification for Subsystem Energy Saving Mode Communication (between semiconductor equipment and subsystems).

Q: Please describe how the energy saving task force was born and why you decided to get involved.

CRISPIERI: Back in 2009 while working for SEMATECH in Austin, Texas, prior to SEMATECH's move the New York, Thomas Huang an assignee for GlobalFoundries to the EHS Program approached and asked me if I would be interested in helping him drive a standard for equipment suppliers to enable their equipment to save energy during idle times. Because of my previous experience working with equipment suppliers and developing standards for equipment and factory communication, I accepted to chair a task force to drive the equipment supplier's new capability requirement into a standard. At first, we thought it would be an easy task and that everyone would jump to help create and approve the standard in a short amount of time because of its benefits. A two phase approach was defined to drive the standardization process and engage semiconductor and sub-fab equipment suppliers accordingly. It took almost three years to complete the Phase I (2013) and another three to complete the Phase II (2016) standards.

SHELLEY: The task force was an extension of E167 which previously defined the communication into the tool from the supervisory systems, however to achieve maximum benefit signalling to tool subsystems was key and the E175 task force was the result.

CZERNIAK: Following-on from the above, the ISMI working group became a SEMI Standards Task Force and began work at developing a standard, initially for Host to process tool (E167) and then from tool to sub-fab (E175), which I was co-chair for to ensure continuity and clear the signalling "roadblock".

Q: How have suppliers collaborated on E175?

CRISPIERI: Compared with the suppliers who participated in SEMI E167 development, the suppliers involved in the development and approval of SEMI E175 were more committed to make it happen and helped drive the standardization process to conclusion much more efficiently. Edwards, AMAT, TEL, Hitachi-Kokusai and DAS-Europe regularly participated and provided inputs to standardize behavior and requirements for their own equipment. We run into some difficulty getting aligned with other standard activities that were driven by SEMI's EHS Committee because their changes affected our standardization process. I must note that the overall participation was excellent in particular from Edwards Vacuum and AMAT.

ROSTAN: Within the ETG Semiconductor Technical Working Group individual task groups already had multiple suppliers collaborating on the detail of the EtherCAT profiles for all devices, with technical support from the EtherCAT Technical Group. We were fortunate to have a delegate from Edwards in both the Semi E175 Task Force and key EtherCAT Task Groups to informally broker agreement between the teams.

SHELLEY: The suppliers were able to use their collective experience to work through a number of options to find the optimum way of controlling subfab equipment, tackling variability in wakeup time and control architectures between device types and equipment technology.

CZERNIAK: Suppliers, automation providers, tool OEMs and end-users have all collaborated to help develop a standard that works for everyone and aligns with earlier standards like S23.

Q: How was the EtherCAT collaboration beneficial to E175?

SHELLEY: By sharing information and understanding in real time we demonstrated the E175 concept is achievable using the favored protocol for new tool platforms and defined how it would be implemented. We co-operated to take both these standards to alignment in one simultaneous step, saving considerable committee time on both sides that would have been necessary to resolve any divergence of the detail.

ROSTAN: By devising the implementation of E175 in parallel the EtherCAT Task Groups involved were able to feedback detailed technical proposals and show the E175 standard could be implemented relatively easily within the existing EtherCAT standards.

CRISPIERI: Participation and collaboration from the EtherCAT Working Group was critical to accelerate the implementation and adoption of the standard. Dry Contacts and EtherCAT communication protocol messages were added to two Related Information sections

ROUNDTABLE

and included in the SEMI E175 standard at the time of its publication.

CZERNIAK: This enables a "richer" signalling environment than simple dry contacts (which are also supported) that enables even greater utility savings to be made.

Q: How has EtherCAT been able to support the requirements of the tool and Semi E175?

CZERNIACK: By providing timing information; the longer the time the tool is inactive, the greater the savings possible.

ROSTAN: As the control network of choice for the latest semiconductor tools, EtherCAT has been ideally placed to support enhancements, such as the energy saving connectivity increasingly being requested by the fabs. In particular, it was good to see the Pump and Abatement Task Groups of the existing Semiconductor Technical Working Group formulate an E175 compliant solution within the timescales of the second release of the EtherCAT semiconductor device profiles. The EtherCAT Technology Group was also more than happy to support the publication of extracts of the EtherCAT standards being used as protocol examples in the Implementation guidelines of the Semi E175 document.

SHELLEY: EtherCAT has the fast / deterministic connectivity and proven integration with tool controllers that allows E175 functionality to be easily added without any loss of performance. By including the requirements of Semi E175 in the EtherCAT standards, both equipment suppliers and tool vendors can establish energy saving communication quickly and easily.

CRISPIERI: The coordination between EtherCAT Working Group and the SEMI ESEC task force group was conducted by Mr. Gerald Shelley from Edwards Vacuum. With his help and leadership, we reached effortlessly agreement and acceptance for the required messages, parameters and values into the EtherCAT respective Pump and Abatement Profile documents. Having working usage scenarios and support from the EtherCAT Working Group has been invaluable.

Q: Why is energy saving important to the industry?

ROSTAN: In the industrial world, EtherCAT users are increasingly using our communication and control technologies to drive down energy consumption. The semiconductor industry operates in parts of the world where energy is a limited and expensive resource, whilst the latest wafer processing requires more power. The manufacturers are therefore in great need for energy saving opportunities, such as when the tool subsystems are not in use.

SHELLEY: The fabs are being squeezed by an increase in the complexity and number of processes involved in manufacturing a wafer, driving consumption up and increasing scarcity of energy supply. This is further complicated with associated cost and government pressure to "keep the lights on".

CRISPIERI: It is not hard to see why is so important for device makers or the semiconductor manufacturing industry to adopt and require energy conservation capabilities in their factories. Energy consumed by many equipment components and support systems, such as pumps and abatement systems, never stop from running even when the equipment is idle and waiting for product to be delivered for processing. These components and support systems can save millions of dollars each year if their power consumption is reduced. This energy consumption reduction extends their life cycle thus reducing costs of maintenance and parts replacement. Any effort to reduce energy consumption helps lower costs and adds gains to not only the manufacturer but to those who have to generate the energy for consumption.

CZERNIACK: Cost reduction is always important, but electrical supply is limited in some areas. **•**



SEMICON West Preview: MEMS

PAULA DOE, SEMI, Fremont, CA

As Demand for Sensors Soars with IoT, Opportunities Increase with Smart Functionality

utonomous automobiles, smart manufacturing, smart buildings, mobile human health monitoring, and 4G+ communications hardware for connecting all these devices will drive strong 24 percent growth in units and 14 percent in value for the MEMS sector, according to Yole Développement. "These emerging markets will give a noticeable boost to MEMS growth going forward," says Yole Founder and President Jean Christophe Eloy, who will discuss the changes coming to the sector at SEMICON West 2017, on July 11.

These emerging applications are changing what's required from MEMS suppliers. We are seeing bigger building blocks with higher value, integration of more functions and more processing power in the package, and increased demand for software intelligence to turn the sensor data into useful information, Eloy notes. This probably also means a shake up in the players, as it's not clear who will capture the value of this growth opportunity, as the key skills move even more towards integration and software to enable functions.

Demand for smart audio, smart visual and more RF

The demand for RF filters required by the increasing complexity of communicating all this data with high-



FIGURE 1. Emerging smart autos, manufacturing, healthcare and increasingly complex high speed communications will boost MEMS market to more than \$25 billion in the next six years. Source: Yole Développement.

speed 4G/4G+ mobile technology will make RF MEMS BAW filters the fastest-growing segment of the MEMS business, likely seeing some 35 percent compound annual growth, jumping from \$2.2 billion in 2017 to a \$10.2 billion market in 2022, according to Yole analysts.

Demand for audio processing will also be particularly strong, with 11 percent growth in units for MEMS microphones, increasingly for more sophisticated applications that use the devices in an always-listening capacity, continually sensing what is happening around in the home, in the car or in the factory. That means more processing power and software are needed to detect key sounds form the background noise, and even recognize what they mean.

Another coming change: MEMS micro speakers will soon finally hit the market. STMicroelectronics is currently making wafers for USound for qualification. "Micro speakers will happen next year," says Eloy, noting that this will enable a proliferation of small and diffuse audio applications, and will increase demand for more and more sophisticated audio ICs for processing, as audio increasingly becomes a more main used human-machine interface.

Smarter image sensing will also make its way into more applications, while various types of 3D imaging like ultrasonics, radar, and LIDAR are starting to get traction not only in automotive applications, but also in smartphones for autofocus and for facial recognition for security.

Adding intelligence at the edge

The next generation of sensor technology will also clearly integrate more intelligence. IoT applications are generating immense amounts of data, which needs to be intelligently processed into useful information for local action. However, sending all that data to the cloud and back for processing is often not practical. "Now that we have so much sensor data available—not just motion, but also sound, imaging, IR, UV, and other spectra—the next opportunity is to add artificial intelligence (AI) or machine learning at the edge, so the sensors report only the selective information required to signal problems that need action," says Pete



FIGURE 2. Growing opportunity for adding audio value based on MEMS means interest by a host of competing players. Source: Yole Développement.

Beckman, co-director, Northwestern/Argonne Institute for Science and Engineering, Argonne National Laboratory. Beckman will talk at SEMICON West (July 11-13) about his lab's open platform that allows researchers to experiment with adding machine learning to sensor nodes.

The Argonne Waggle platform includes a Linux-based single board computer to handle encrypted networking and data caching. It also pulls sensor data from customized boards or off-the-shelf sensor devices. The Waggle management (wagman) board controls power and diagnostics. The third key component is a single board computer focused completely on edge computing, supporting AI and machine learning. With eight CPU cores and a GPU, the edge processor can be trained to recognize sounds and images or other patterns, using open source software like UC Berkeley's Caffe deep learning software and the OpenCV computer vision package. "We isolated this part on a separate board to run the newest software available, and out on the leading edge of development, all of this AI software can still be a little buggy," Beckman notes.

The group is working with the city of Chicago on a network of these smart nodes to monitor things like traffic

incidents, air pollution, ice on roads, or potential flooding. Other researchers are the using the platform to measure pollen and particulates in air to predict asthma outbreaks, or monitor water flow patterns across a prairie site.

Adding intelligence to development

"If the MEMS industry is going to innovate more smartly, we can't keep doing things the same old way we always have, and the foundries have to do their part to do things differently as well," notes Tomas Bauer, Silex Microsystems' SVP Sales & Business Development, who will discuss Silex's efforts to use tailored IT systems to speed the development of MEMS devices. Since most innovative MEMS devices depend on developing a whole new wafer process, ramping to stable volume production has often taken years. So Silex has worked on developing information systems to track the wafers through development, with a cockpit view for easy access to all the statistics on the runs and the risk items, immediate notification of potential issues, and more sophisticated queuing and optimization of pathways of development batches to speed throughput in the high-mix fab, Silex's also uses optical inspection tools during processing so its engineers can roll back the images to see what went wrong. "Instead of trying to standardize the process, we need to find ways to speed the development of the custom process," Bauer suggests. ◆

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MEMS & Sensors Technical Congress 2017: Knowing your unknowns

As in life, knowing everything in MEMS and sensors is impossible. Often the best we can do is to "know the unknowns" because articulating what we do not yet understand allows us to seek answers so that we can stay competitive.

MEMS and sensors supply chain members need to know what is "state of the art" in terms of technology, what the competition is doing, and how to identify the best partners in order to increase revenue more quickly. Bridging alliances across the supply chain is truly the only way you'll get from here to there.

These concepts are integral to MEMS & Sensors Industry Group's (MSIG's) upcoming conference, MEMS & Sensors Technical Congress (MSTC), Working Together to Solve Technical Challenges and Increase Value across the MEMS and Sensors Supply Chain. What will you experience at MSTC? You will get to rub elbows with top technologists from both inside and adjacent to the MEMS and sensors industry as they share their expertise on how to address the most common technical challenges to growth. This year Stanford University's SystemX is hosting MSTC and they will offer a guided tour of their two nanofabs (one of which recently opened, so this is a special treat).

For this year's MSTC, we've lined up some impressive keynote speakers.

Chris Ré, assistant professor, Department of Computer Science, Stanford University, will present "Snorkel: Ameliorating the Labeling Bottleneck in Machine Learning." With machine learning an indispensable part of voice-recognition, image search, natural language processing and other applications, Chris will explore new techniques for circumventing the most common bottleneck in machine learning — creating training sets. I think everyone will welcome the opportunity to learn how to snorkel our way through a smarter planet.

Scott Borg, director and chief economist of U.S. Cyber Consequences Unit will present "Understanding Sensor and MEMS Security from an Economic Standpoint." Scott's keynote will address the value and opportunity cost of MEMS and sensors devices with respect to cyber attacks, focusing on the value as opposed to the cost. His premise is that "approaches that are purely technical are especially likely to waste resources." Intriguing, no?

MSTC 2017 will also include breakout sessions that will give attendees an opportunity to roll up their sleeves and tackle some of the most challenging technical issues still affecting both the front-end, middle and back-end of manufacturing. These "known unknown" topics include:

- 1. Technology Transfer for Dummies: How to Get to a Stable High-yielding Process – chaired by Mary Ann Maher, Ph.D., president and founder, softMEMS
- Back-end Challenges of MEMS and Sensors (Packaging, Testing, & Reliability) – chaired by Mike Mignardi, manager, technology development, Texas Instruments
- 3. Integration Opportunities (Technological & Business Considerations) – chaired by Peter Himes, general manager, SITRI Innovations and SITRI Ventures
- Emerging MEMS, Sensors, and Systems Incorporating Them – led by Nicole Kerness, vice president, Sensor Design and Technology, Kionix
- 5. Piezoelectric and other Emerging Materials for MEMS and Sensor Applications – chaired by Dave Horsley, PhD., Chirp Microsystems

MSTC 2017 has also compiled an impressive lineup of speakers who will address issues such as sensor integration and its benefits (STMicroelectronics Senior Manager, MEMS Product Marketing Jay Esfandyari,). Coventor Vice President of Engineering Stephen Breit, will discuss enabling "easy customization" of MEMS sensors for integrated, highvalue solutions. Silicon Microgravity Executive Chairman Paul Vickery will describe new technology that allows us to measure Earth's gravitational field to an astounding resolution of 1 ppb. Plasma-Therm Business Development Manager Yanick Pilloux will offer insights into the emerging process of plasma dicing technology.



KAREN LIGHTMAN, MEMS & Sensors Industry Group, SEMI



Many THANKS to the attendees, speakers and sponsors who made The ConFab 2017 a resounding success. We look forward to another great event in 2018!

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