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MARCH 2013

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Reliability  
Challenges P. 18

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## MEETING SYMPOSIA

## ENERGY

- A Film Silicon Science and Technology
- B Organic and Hybrid Photovoltaic Materials and Devices
- C Thin-Film Compound Semiconductor Photovoltaics
- D From Molecules to Materials—  
Pathways to Artificial Photosynthesis
- E Materials and Integration Challenges for Energy Generation  
and Storage in Mobile Electronic Devices
- F Materials for Vehicular and Grid Energy Storage
- G Electrochemical Interfaces for Energy Storage and Conversion—  
Fundamental Insights from Experiments and Computations
- H Nanoscale Thermoelectrics—  
Materials and Transport Phenomena II
- I Materials for Solid-State Refrigeration
- J *In-Situ* Characterization Methods in Energy Materials Research
- K Materials for Sustainable Development

## NANOMATERIALS

- L Nanoparticle Manufacturing, Functionalization, Assembly,  
and Integration
- M Solution Synthesis of Inorganic Functional Materials—  
Films, Nanoparticles, and Nanocomposites
- N Nanomaterials in the Subnanometer-Size Range
- O Beyond Graphene—2D Atomic Layers from Layered Materials
- P Graphene and Related Carbon Nanomaterials
- Q Surfaces of Nanoscale Semiconductors
- R Nanostructured Semiconductors and Nanotechnology
- S Nanostructured Metal Oxides for Advanced Applications
- T Electrical Contacts to Nanomaterials and Nanodevices
- U Measurements of Atomic Arrangements and Local Vibrations  
in Nanostructured Materials
- V Nanoscale Heat Transport—From Fundamentals to Devices
- W Piezoelectric Nanogenerators and Piezotronics
- Y Advances in Scanning Probe Microscopy  
for Imaging Functionality on the Nanoscale
- Z Nanotechnology and Sustainability

## ELECTRONICS/PHOTONICS

- AA Advanced Interconnects for Micro- and Nanoelectronics—  
Materials, Processes, and Reliability
- BB Evolutions in Planarization—  
Equipment, Materials, Techniques, and Applications
- CC Gate Stack Technology for End-of-Roadmap Devices  
in Logic, Power, and Memory
- DD Emerging Materials and Devices  
for Future Nonvolatile Memories
- EE Phase-Change Materials for Memory, Reconfigurable  
Electronics, and Cognitive Applications
- FF Compound Semiconductors for Generating, Emitting,  
and Manipulating Energy II
- GG Single-Dopant Semiconductor Optoelectronics
- HH Materials for High-Performance Photonics II
- II Resonant Optics in Metallic and Dielectric Structures—  
Fundamentals and Applications
- JJ Fundamental Processes in Organic Electronics
- KK Charge and Spin Transport  
in Organic Semiconductor Materials

## BIOMATERIALS

- LL Hybrid Inorganic-Biological Materials
- MM New Tools for Cancer Using Nanomaterials,  
Nanostructures, and Nanodevices
- NN Multifunctional Biomaterials
- OO Design of Cell-Instructive Materials
- PP Adaptive Soft Matter through Molecular Networks
- QQ Conjugated Polymers in Sensing and Biomedical Applications
- RR Lanthanide Nanomaterials for Imaging, Sensing,  
and Optoelectronics
- SS Bioelectronics—Materials, Interfaces, and Applications
- TT Materials and Processes for Electronic Skins

## GENERAL

- UU Plasma and Low-Energy Ion-Beam-assisted Processing  
and Synthesis of Energy-related Materials
- VV Materials Applications of Ionic Liquids
- WW Nuclear Radiation Detection Materials
- XX Oxide Thin Films and Heterostructures  
for Advanced Information and Energy Technologies
- YY Titanium Dioxide—Fundamentals and Applications
- ZZ Carbon Functional Interfaces II
- AAA Superconducting Materials—  
From Basic Science to Deployment
- BBB Size-Dependent and Coupled Properties of Materials
- CCC Novel Functionality by Reversible Phase Transformation
- DDD Extreme Environments—A Route to Novel Materials
- EEE Materials Education—Toward a Lab-to-Classroom Initiative

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Rachel Segalman University of California, Berkeley  
Lonnie D. Shea Northwestern University  
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## Don't miss these future MRS meetings!

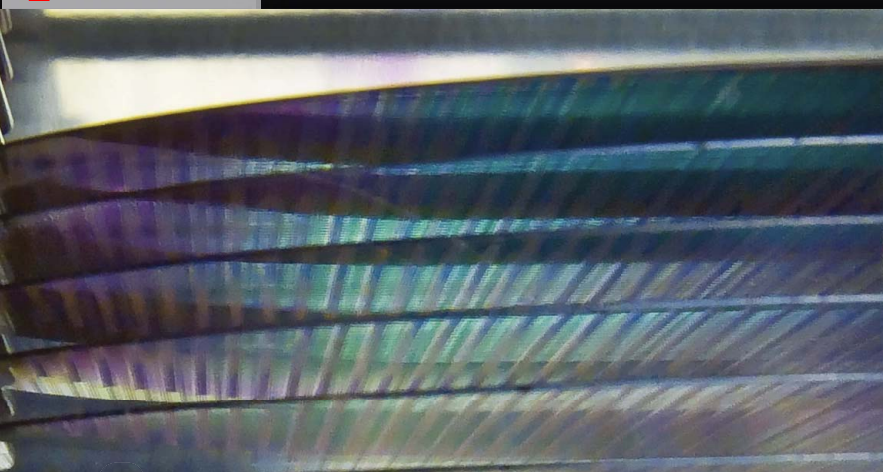
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MARCH 2013 VOL. 56 | NO. 2

Wafers await processing inside Silex's  
MEMS fab.

COVER

## FEATURES

13

**PACKAGING** | Vertical through-wafer insulation:  
Enabling integration and innovationThrough-wafer insulation has been used to develop technologies such as Sil-Via TSV and Zero-Crosstalk. *Peter Himes, Silex Microsystems AB, Järfälla SWEDEN*

18

**RELIABILITY** | Today's top reliability challengesBTS, BTI, soft errors, dielectric breakdown and other reliability challenges will be addressed at the upcoming International Reliability Physics Symposium. *Pete Singer, Editor-in-Chief*

21

**INSPECTION** | Exploring the dark sideA look at the impact of back side particles on front side defectivity. *Rebecca Howland, Ph.D. and Marc Filzen, KLA-Tencor, Milpitas, CA*

23

**CMP** | Automatic wafer inspection system  
replaces eyeballs with camerasA fully automated RDS inspection system to replace human inspectors is a game changer. *Christopher Eric Brannon, Texas Instruments, Inc., Dallas, TX*

25

**RELIABILITY** | Insights into low frequency  
noise in high-mobility transistorsThe impact of high-mobility channel materials and novel device architectures on the low-frequency noise behavior of 22nm and below CMOS transistors is reviewed. *Eddy Simoen, et al, imec, Leuven, Belgium*

## COLUMNS

- 3 Editorial** | Filling the fabs of the future, *Pete Singer, Editor-in-Chief*
- 11 LEDs** | Worldwide LED component market grows 9%, *Ella Shum, Strategies Unlimited*
- 13 Packaging** | 3D IC with TSV: Status and developments, *Jan Vardaman, TechSearch International*
- 33 Industry Forum** | Managing process variations, *Dr. Zhihong Liu, Executive Chairman, ProPlus Design Solutions*

## DEPARTMENTS

- 2** Web Exclusives
- 4** News
- 30** New Products
- 32** Ad Index

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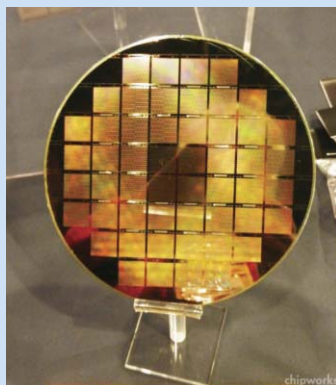
## Web Exclusives

### ISSCC 2013

Trends unveiled at the International Solid State Circuits Conference (ISSCC) are described by subcommittee chairs, focusing on high-performance digital, memory, analog, wireless, RF, energy-efficient digital, large-area displays, MEMS, medical and imagers. <http://bit.ly/1335ed9>

### Intel foundries MEMS for fuel cell start-up Nectar

Chipworks' Dick James reports on how Intel manufactured a fuel-cell based USB charging system on a 200mm wafer for a start-up called Nectar. The Nectar generator chip contains the fuel processor, fuel cell stack, and catalytic converter. The fuel processor cracks the butane into hydrogen and carbon monoxide by using a lean mixture of air and butane to give incomplete combustion; then  $O_2^-$  ions from the air feed on the other side of the SOFC stack migrate through the stack and combine to give water and carbon dioxide; then the exhaust gases exit through a catalytic converter. The fuel processor uses a mechanically suspended reaction zone formed in silicon, with a heat exchanger adjacent to the reaction zone. <http://bit.ly/Wlw0aD>



### Looking for an integrated post-tapeout flow

Dr. Steffen Schulze, the Product Management Director for the Mentor Graphics' Calibre Semiconductor Solutions, says the issue of platforms has been on his mind. He notes that a platform not only provides the integration and efficient operation at the work-flow level, but it also enables efficiency at the data-center level, considering the simultaneous and sequential execution of many different designs and computational tasks. <http://bit.ly/Y2DxQh>

## n&b news and blogs

### EUV source roadmaps: Physics vs Engineering

Dr. Vivek Bakshi tackles the question of when EUV sources will be ready to support high volume manufacturing. He notes that it is a difficult question to answer, partly because readiness metrics have been a moving target. <http://bit.ly/XgaKJO>

### MEMS: The first prototype

MEMS-developer David DiPaola blogs about MEMS new product development, including the importance of the first prototype. He notes that nothing shows proof of principle and sells a design like a working prototype. <http://bit.ly/12YNnbB>

### Insights from the Leading Edge



**Dr. Phil Garrou** reports on SEMI Europe's first European 3D

TSV Summit in Grenoble, held in late January with a theme of "On the Road towards TSV Manufacturing". ST showed wide IO bandwidth capability the same as LPDDR3 although the DDR memory takes a significant hit in power efficiency. <http://bit.ly/XINT5J>



## editorial

# Filling the fabs of the future

At press time, the sessions for The ConFab 2013 ([www.theconfab.com](http://www.theconfab.com)) are being finalized. The overall theme of the conference is "Filling the fabs of the future," with a focus on the types of products that will drive demand for semiconductors in the next decade, the technologies and processes that will be required to meet this demand, and the manufacturing and operational challenges that will arise as a result of this demand and how to meet them.

We'll kick things off on Tuesday morning with a keynote talk by Y.W. Lee, vice chairman of Samsung. Session 1 will focus on major economic trends, with talks from Jim Feldhan of Semico, Bill McClean of IC Insights, Mark Thirsk of Linx Consulting and Dan Hutcheson of VLSI Research.

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by registering now on our  
website, [www.theconfab.com](http://www.theconfab.com)"

Next, we'll look at the design/manufacturing/packaging/testing supply chain, including collaboration between fabless/product design companies and foundries. Mike Campbell of Qualcomm and Jae Cho of Xilinx will present in this session.

In the afternoon on Monday, we'll hear from a panel of experts on 3D integration, including Mike Ma of SiliconWare, Subu Iyer of IBM (who will also be keynoting on Tuesday morning), HoMing Tong of ASE, and Bob Patti of Terazzon. A special thanks to Phil Garrou and IEEE CPMT, the technical sponsor of this session and another session on Advanced Packaging.

Tuesday will begin with a keynote from Subu Iyer, followed by a panel session moderated by Scott Jones of Alix Partners. The session will focus on R&D Portfolio Management and Improving R&D Efficiency. Jones will share the results of a AlixPartners' study of the 72 largest semiconductor companies globally over the past six years that found that companies with a higher degree of R&D efficiency show greater profitability.

We'll then get into a status report on advanced packaging, with an excellent line-up of speakers, including: Devan Iyer from Texas Instruments, Bob Lanzone from Amkor, Steve Anderson from STATS ChipPAC, and Ted Tessier from FlipChip International.

In the afternoon on Tuesday, we'll hear from Sanjay Rajguru of ISMI and a panel of speakers assembled by ISMI, focusing on accelerating manufacturing productivity. I hope you can join us!

—Pete Singer, Editor-in-Chief

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# news

## worldnews

**WORLD | STMicroelectronics** and **Hyundai Autron** plan to jointly develop integrated products for next-generation vehicles.

**WORLD | Singapore-based A\*STAR's Institute of Microelectronics** and **Stanford University** will develop switch technology for efficiency in mobile devices.

**USA | Cabot Microelectronics Corp.** will collaborate with **SEMATECH** to develop advanced solutions for emerging CMP applications.

**EUROPE | Tronics** launched a new large-scale MEMS project to industrialize **CEA-Leti's** technology.

**USA | Araca** and **ISMI** are partnering to deliver CMP processing and productivity solutions.

**ASIA | Renesas** and **J-Devices** signed a MoU regarding the transfer of the semiconductor back-end production business of three facilities.

**ASIA | STATS ChipPAC** and **UMC** demonstrated aTSV-enabled 3D IC chip stacking technology developed under an open ecosystem collaboration.

**JAPAN | Mitsubishi Electric Corp.** developed a prototype multi-wire electrical discharge processing technology to cut SiC ingots.

**EUROPE | Imec** and **PVA Tepla** achieved void detection in through-silicon vias at wafer level.

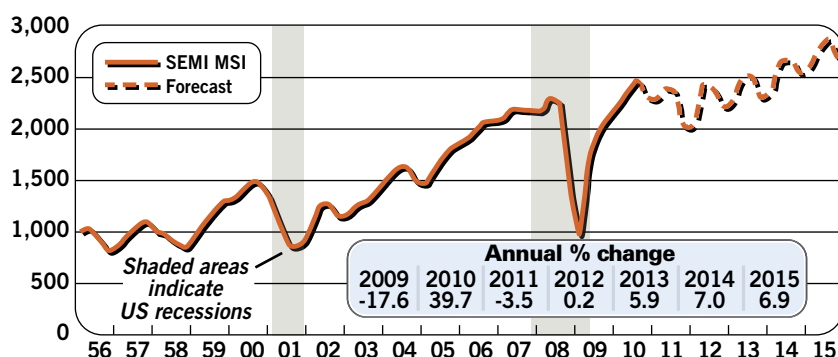
**USA | SRC** and **DARPA** dedicated \$194 million to six new university microelectronics research centers.

## Econometric Forecast: Semiconductor growth should recover by 2014

The weakness in economic growth spills into end products containing semiconductors in 2012 and early 2013, according to a new report from Linx Consulting. Their model relating final demands to

up at a modest pace that averages slightly less than 6% for the full year. By 2014, growth should recover to long-term potential growth for MSI of approximately 7%/year.

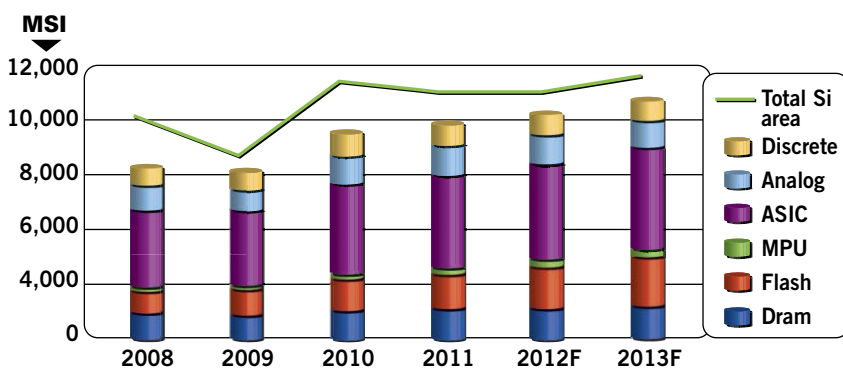
Key assumptions driving this



**Figure 1.** Aggregate semiconductor production from 1955 to present, with forecast to 2015.

aggregate semiconductor production (measured by SEMI's Million Square Inches of silicon processed, MSI) suggests weak demand was anticipated in 2012, and that by early 2013, enough improvement in end markets occurs to push growth

forecast include some solution to the fiscal cliff dilemma that permits US consumers and businesses to begin to return to more normal conditions. Removing uncertainty drives a modest expansion US spending on technology goods of



**Figure 2.** The difference between Segment Demand and Total Silicon Area (includes test and monitor wafers).



around 2.3%, up from the anemic 0.8% growth anticipated for 2012. Most of that growth will occur in the second half of 2013, as it will take some time for businesses to analyze the new policy environment and then implement investment plans. Inventory-shipment ratios for technology goods, which are spiking in the last half of 2012, are assumed to recede on a steady pace to more typical levels through 2013. If shipments in IT goods do not develop as expected, the quarterly pattern above would most likely show a steeper decline in 2012Q4 and a further decline in 2013Q1, followed by strong gains in Q2 or Q3.

The overall picture of MSI growth breaks down into the expected performance of device segments and technology nodes. Despite the shift to consumer electronics and mobile platforms, we expect growth to be concentrated in CMOS products with a continuing slowing of unit growth and analog and discrete devices. Strongest growth will remain with flash memories, and advanced foundry logic devices targeted at tablets and phones.

In contrast with advanced memory and logic processing, approximately 56% of the market continues to be produced at design dimensions in excess of 100 nm on wafer sizes at 200 mm or smaller. This market segment is extremely sensitive to economic volatility and has slowed significantly in the last four years. Manufacturers of these devices are often capital constrained and extremely cost sensitive, leading to little process innovation

and limited capacity expansion.

On a technology basis, despite tight capital budgets, the

introduction of devices at 28 and 22nm half pitches continues apace,

*Continued on page 8*

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## newscont.

## GaN use growing in power semiconductors

GaN has turned out to be the choice for most of the power semiconductor applications and is quickly replacing the existing silicon technology, according to a new report from Research and Markets. The various properties of GaN, such as wider bandgap, high break-down voltage, larger critical electric field,

and higher thermal conductivity, let the GaN devices operate at higher voltages, high switching frequencies, handle higher power density, and offer enhanced power efficiency than the pure Si devices. These properties allow the GaN discretes like Schottky diodes, MOSFETs, and the other advanced transistors

to operate at much higher voltage levels, which are difficult for the counterpart Si devices. GaN power semiconductors also help in reducing the conduction and switching losses. The major application segments are the inverters (and converters), RF devices, power supply modules, and motor drives. ◀

## 10 IC product segments to exceed total IC market growth in 2013

Ten product categories, led by tablet MPUs and cellphone application MPUs, are forecast to exceed the 6% growth rate forecast for the total IC market this year, according to IC Insights' 2013 McClean Report. This report identifies and segments the total IC market into 34 major IC product categories. Five categories are forecast to enjoy double-digit growth. The number of categories with positive growth is expected to more than double to 22 in 2013 from 10 in 2012.

Consumer-driven mobile media devices, particularly smartphones and tablet computers, are forecast to keep the tablet MPU (50%) and cellphone application MPU (28%) segments at the top of the growth list for the third consecutive year. Other IC categories that support mobile systems—including NAND flash (12%) and special-purpose logic devices—are expected to enjoy better-than-industry-average growth in 2013, as well.

Due to increasing demand for higher levels of precision in embedded-processing systems and the growth in connectivity using the Internet, the market for 32-bit MCUs is also forecast to outpace total IC market growth in 2013. Embedded applications in medical/health systems and smartcards have helped boost the 32-bit MCU market. In the automotive world, demand for

Product Category	2012 Growth	2013F Growth
Tablet MPUs	60%	50%
Cellphone App MPUs	41%	28%
Wired Telecom – Special Purpose Logic/MPR	17%	13%
NAND Flash	6%	12%
Wired Telecom – App-specific Analog	24%	11%
DRAM	-10%	9%
Wireless Telecom – Special Purpose Logic/MPR	9%	9%
Auto – Special Purpose Logic/MPR	2%	7%
Consumer – Special Purpose Logic/MPR	12%	7%
32-bit MCU	4%	7%
Total IC Market	-2%	6%

32-bit MCUs is being driven by “intelligent” car systems such as driver information systems and semi-autonomous driving features such as self-parking, advanced cruise controls, and collision-avoidance systems. In the next few years, complex 32-bit MCUs are expected to account for over 25% of the processing power in vehicles.

After back-to-back years of steep declines in 2011 and 2012, the DRAM market is forecast to increase 9% in 2013, three points more than the total IC market. DRAM unit growth is expected to increase only 2%, but the overall average selling price is forecast to jump 7% this year. In five of the past six years (2007-2012) the DRAM



market declined, which took its toll on weaker suppliers. Fewer suppliers in the marketplace mean fewer competitors trying to undercut each other's prices in order to gain marketshare and enhances the likelihood of a more stable pricing environment in the coming year.

Interestingly, in a world that is increasingly wireless, two IC categories of "wired" telecom ICs are forecast to grow faster than the total IC market. Wired telecom—special purpose logic/MPR and wired telecom—application-specific analog are forecast to grow by 13% and 11%, respectively.

Telecom companies and network operators have been upgrading their long-haul and metropolitan-wide communications systems, which require many high-speed transmission ICs and other circuits. New 100Gb/s technology has been ready for deployment since 2009 and is being deployed now. Next-generation transmission technology and ICs for 1 trillion bits per second ("Terabit") networks are in development.

Telecom and network operators say data traffic is increasing more than 50% per year due to growing use of the Internet and video transmissions. All wireless traffic eventually goes through high-speed cable transmission "backbone" networks—communications are routed over long distance via optical cable before getting to the cellular network on the other end. All the mobile Internet, data, and video traffic has to go through a cable network and that is driving up the market for wired telecom—special-purpose logic/

MPR and wired telecom—application-specific analog. To a lesser degree, the wired telecom segments are growing on account of developing country markets. ◀

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- ▶ LED fabrication

### FEATURES

- ▶ Liquid cooled
- ▶ Fan cooled
- ▶ Multi output
- ▶ Redundant systems



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## newscont.

## China's top 10 packaging and assembling facilities

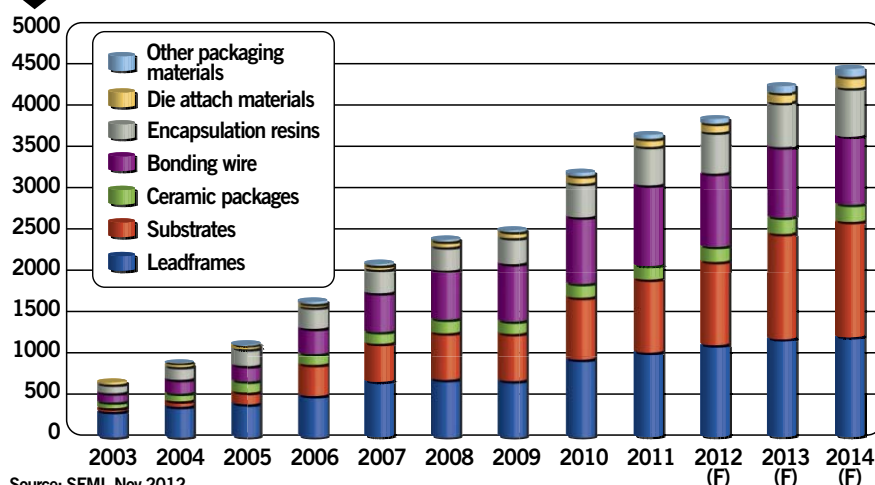
Packaging and assembly are key segments of the growing semiconductor supply chain in China. SEMI China reports that, based on their tracking of 139 companies, and considering numerous small companies not tracked in detail, there are over 200 companies competing in the packaging and assembly market in China. Although many are small companies manufacturing low-pin count devices, all of the world's "Top 10" OSAT, Outsourced Semiconductor Assembly and Test, players have one or more assembly and testing facilities in China. Eight of the world top 10 IDM companies have assembly and test manufacturing facilities in China, and most entered into China earlier than the OSAT players, in the mid-1990s.

## Top Ten OSAT Facilities in China

1. ASE
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3. SPIL
4. STATS ChipPAC
5. Powertech
6. UTAC
7. ChipMOS
8. JCET
9. KYEC
10. Unisem

**Forecast** Continued from page 5

and significant process challenges are driving increased complexity and resultant challenges in patterning, cleaning, CMP and deposition throughout the device

**China packaging material market (\$M)**

In addition to the international companies, domestic subcontractor companies are increasingly joining the global outsourcing market. The assembly of small-size optoelectronic chips like CMOS image sensors is the most mature 3D through-silicon via platform at the moment and China players occupy an important place through transferring authorized technology from overseas partners. Also, domestic semiconductor equipment suppliers that previously focused on front-end tool development are applying their products in wafer level package and TSV assembly.

With the growth of semiconductor packaging industry in China, domestic packaging material suppliers are emerging with the industry and are now starting to serve the worldwide leading packaging houses. Given the emphasis on low-cost manufacturing, packaging houses will continue to evaluate China-based suppliers to realize lower material cost. On the other hand, to enhance their competitive power, stabilize sales and marketing channels, and reduce operational risk, China-headquartered material suppliers are forming partnerships with leading packaging houses. ◀

manufacturing process. 2012 is forecast to have produced more silicon area at 32nm than any other node, and the introduction of low 20nm half pitches and flash has continued to grow startling rates.

In total devices manufactured at 65nm and below continued to show strong area growth in 2012 of 14%, with devices at 90nm and above largely offsetting declines from 2011 with 8% growth in 2012. ▶



## MEMS devices shape medical industry

MEMS devices are shaping the competitive landscape in the global medical device industry. According to a new report from Global Information, several factors are behind the increasing demand for and innovation in MEMS devices in the medical industry: growing number of MEMS applications in healthcare; innovations, revolution and growth in the personal healthcare market, including wireless implants; and rising awareness and affordability of healthcare.

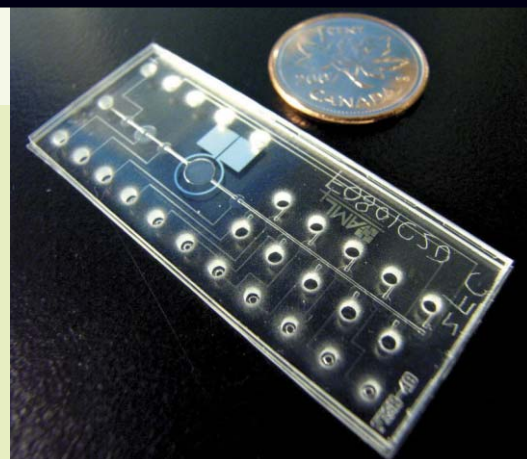
The use of MEMS devices by different stakeholders is driving market growth by adding to the demand of devices from different medical market segments as discussed above. This is also indirectly encouraging for medical sector market players (particularly big ones) that have diverse customer bases composed of different stakeholders and diverse product portfolios (such as diagnostics, research, and medical devices), as they can capitalize on the MEMS market by leveraging their existing resources to some extent. Moreover, a diverse set of devices catering to the needs of different stakeholders encourages new entrants into sectors of their choice to complement or suit their capabilities and potentials.

Integrated devices and advancements in inertial sensors, such as products for human motion analysis, are meeting the needs of the modernized healthcare delivery model,

especially for the elderly patient sector, by adding the element of prevention. An example of product innovation is microneedles for drug delivery, which is gaining popularity by offering a pain-free and enhanced, accurate method of drug delivery. Similarly, the diagnostic devices have significantly reduced the sample testing time from hours to a few minutes, thus significantly adding value to the healthcare delivery model from different perspectives such as time efficiency, convenience, patient satisfaction, and ease of operations.

Microfluidic/lab on chip (LOC) is considered a revolutionary technology for the life sciences and healthcare industry. This technology enables the integration of assay operations, such as sample pretreatment and sample preparation, on a single chip. This is radically changing the pharmaceutical and life-sciences research sector by changing the way procedures, such as DNA analysis and proteomics, are conducted.

The microfluidic/lab on chip (LOC) segment is expected to rise to 72% of the market share of MEMS devices by 2017. Major growth drivers of this sector are research tools, which are expected to achieve significant growth of CAGR 28.8% from 2012 to 2017. A surge from 2012 to 2017 in research applications, such as proteomics, genomics, and cellular analysis, is also expected to boost this sector.



In terms of applications, the macro segments of the market include pharmaceutical and life-sciences research, in vitro diagnostics, home healthcare, and medical devices. Among all of these applications, research is expected to grow at the highest CAGR of 28.3% from 2012 to 2017.

Expected to triple in size over the next five years, the bioMEMS market is expected to grow from \$1.9 billion in 2012 to \$6.6 billion in 2018. Microsystem devices have applications in four key healthcare markets: pharmaceutical, in-vitro diagnostics, medical devices and medical home care. Microsystem devices have become increasingly visible in the healthcare market by serving as solutions adapted to the requirements of various applications. The usefulness of these devices is two-fold: they improve medical device performance for the patient; and secondly, they offer competitive advantages to system manufacturers. For example, the introduction of accelerometers in pacemakers has revolutionized the treatment of cardiac diseases. ◀

## newscont.

## Silicon Innovation Forum to bridge funding gaps

SEMI, in collaboration with strategic investing groups throughout the global semiconductor industry, has announced the Silicon Innovation Forum, or SIF, to bridge funding gaps for new and early-stage companies with valuable semiconductor manufacturing and technology solutions. SIF will be held in conjunction with SEMICON West, on July 9, 2013 at the Moscone Center in San Francisco, Calif. The event will consist of a one-half day conference highlighted by investment presentations from new and emerging companies with innovative technology solutions targeted at next generation semiconductors. The Silicon Innovation Forum is being organized by leading strategic investment groups in the industry including Applied Ventures, Dow Chemical Company, Intel Capital, Micron Ventures, TEL Venture Capital, and Samsung Ventures.

"At a time when the need for new ideas and technologies has never been greater, venture capital and private funding sources for advanced semiconductor technology development has significantly declined over the past decade, threatening the future of Moore's Law and the economic engine of today's connected, electronic society," said Denny McGuirk, president and CEO of SEMI. "The Silicon Innovation Forum will address these funding gaps by providing a platform for new and emerging innovators, strategic investors, and venture capitalists to discuss the needs and requirements for next-generation technologies, and provide insights into technology, capital, partnership, and collaboration strategies necessary for mutual success."

This collaboration of leading strategic investor groups from throughout the world has formed to streamline and accelerate partnership opportunities for technology entrepreneurs to bridge the gap between R&D and product development funding. The Forum will provide short-term business opportunities for early / mid-stage companies, R&D entrepreneurs from larger companies, and other industry innovators — while addressing long-term structural changes to the industry necessary to foster a healthy innovation pipeline.

New and emerging companies can showcase their innovations through table top and/or poster displays for one-on-one meetings with qualified investors, plus showcase their ideas during short pitches during the SiF Conference. The SIF Conference will be free to all SEMICON West attendees, but the Innovation Showcase and Reception for one-on-one presentation and meeting opportunities will be restricted to qualified partnership and investor groups. ◀

## Tronics to produce submicron MEMS technology of CEA-LETI

Tronics launched a new large-scale MEMS project to industrialize CEA-Leti's breakthrough M&NEMS, or Micro and Nano Electro-Mechanical Systems, technology. This technology is based on piezoresistive nanowires rather than pure capacitive detection, which will advance device performance and chip size. This project sets the stage for a new generation of combo sensors for motion sensing applications.

Within two years, the team will develop 6 DOF, 9 DOF and higher DOF devices, where all sensing elements are using the same M&NEMS technology. The goal is to achieve both significant surface reduction and performance improvement of the multi-DOF sensors. Beyond the smaller die size and the ultra-low power consumption, M&NEMS technology allows manufacturing of all the sensor's axes with one unique technology platform. This high level of integration and commonality simplifies the associated control and readout electronic circuits, both in terms of design and operational efficiency.

In addition to investments by Tronics and its partners, a substantial portion of the project's cost is supported by a 6.5 million euros grant provided by the French Ministry of Industry within its Nanoelectronique Industrial Support program.

To generate the volumes required by consumer applications, Tronics plans to support the technology all the way to high volume eight inch production maturity. ▶



# Worldwide LED component market grows 9%

*LED component revenue for lighting applications reached \$3.11 billion in 2012, narrowly dethroning the large area display backlight segment at \$3.06 billion. The worldwide market for LED components was \$13.7 billion and is expected to grow to \$15 billion in 2017, for a CAGR of 1.8%.*

The total illumination market for 2012 is estimated at \$14.52 billion. LED lighting includes LED replacement lamps and luminaires is estimated at \$11.72 billion—an increase of 26% between 2011 and 2012—and it is forecast to grow at a CAGR of 12% over 2012-2017.

LEDs used in large display (TV and monitors) backlights also reached a new record at \$3.06 billion in 2012. This is chiefly due to the success in penetrating the CCFL stronghold of the 32-inch TV. “Chubby” TVs will spread from 32 inches in both directions in size. It is expected to reach TVs 42 to 50 inches size in 2013-2014. With drastic reduction in number of LEDs used and rapid price erosion, the large display market for LEDs is expected to decline to \$1.7 billion in 2017.

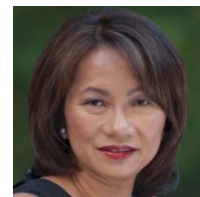
The total market for LEDs in the automotive segment was \$1.4 billion in 2012 and is projected to grow to \$2.1 billion in 2017. The number of cars with LED headlights nearly doubled in 2012. Revenue for 2012 was \$97 million and the five-year CAGR is projected to be 36%.

While LED revenue from tablets grew 54% to \$578 million, the overall mobile segment dropped 3%. The drop in notebook backlight demand, the OLED success in smart phone display, and the general

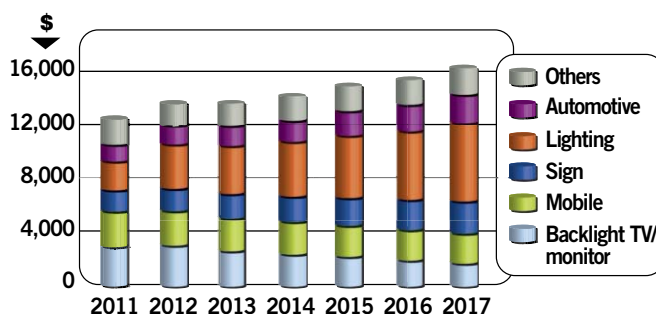
demand decline for other small and medium display will take the segment down to \$958 million in 2017, for a 5 year CAGR of -7%.

The signage segment is expected to grow to \$2.4 billion in 2017, for a CAGR of 7%. Use of LEDs in signage and channel letters grew 7% to \$1.7 billion in 2012. Full-color signs contributed more than 80% of the revenue.

On the supply side, 11 companies accounted for more than 72% of the LED market. We arrived at these figures after analyzing market demand as well as the supply-side activity of more than 54 LED component



**Ella Shum,**  
Strategies  
Unlimited



Worldwide market for LED components. Source: Strategies Unlimited.

suppliers. Their rank by revenue of packaged LED components, is:

1. Nichia
2. Samsung LED
3. Osram Opto Semiconductors
4. LG Innotek
5. Seoul Semiconductor\*
6. Philips Lumileds\*
7. Cree
8. TG
9. Sharp
10. Everlight\*
11. Lumens\*

(\*Companies have the same ranking when the difference in revenue is within the margin of error. Revenue includes sales of packaged LEDs of 30 lm/W or more.)

The LED packaging industry is expected to grow modestly at a CAGR of 1.8% in the next five years. 2013 should see less severe price drops as excess capacity is slowly absorbed by the rise of lighting applications. ♦

## LEDs



# 3D IC with TSV: Status and developments

*While the drivers for 3D ICs remain performance and form factor, the time line for its adoption keeps shifting out into the future. Several technical challenges and infrastructure issues such as are delaying high volume manufacturing of TSV technology for 3D ICs. Until these issues can be resolved, alternative packages will continue to be used.*

On the technical side while there has been a lot of progress in via formation and filling, there are still some process steps that impact yield and have low throughput such as the debonding step during wafer thinning. The problem is combo material and equipment problem. New materials are being introduced and show promise, but engineering requires time. Stacking memory would seem to be the first step, but has proved to be challenging. 3D IC solutions without a debond step have been introduced by Tezzaron using its architecture and a novel process to stack memory was introduced by Elpida before it went in bankruptcy.

Many companies show a silicon interposer or 2.5D solution on their packaging roadmaps where a logic device is mounted next to a stack of memory and the through silicon vias are in the substrate. The problem is that this assumes stacked memory with TSV is commercially available at a cost/performance ratio that matches the requirements. With the stacked memory unavailable this pushes out the adoption of even 2.5D. Some companies also indicate that the cost of the silicon interposer is too high

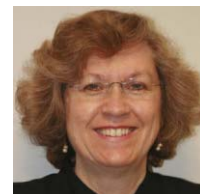
## Packaging



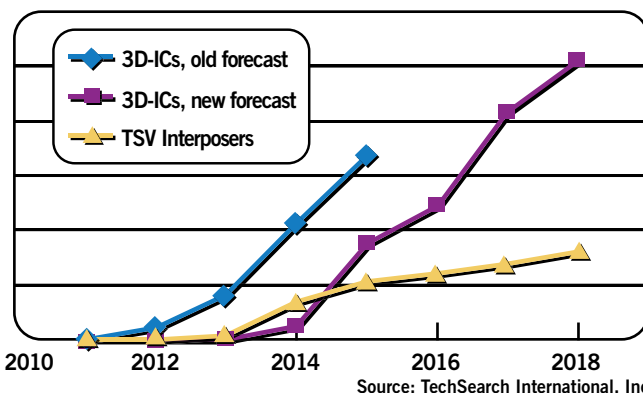
and they would like to consider a glass interposer or even a high-density organic substrate. At this time, glass interposers with TSVs are not commercially available and organic substrates with fine features are still in development.

For stacks of memory and logic the industry still needs thermally aware design tools and even new thermal solutions for stacks that contain logic and memory. Where there has been progress on test methodology development, additional work is still needed. Commercialization of EDA tools will benefit the industry greatly.

Once the 3D IC technical challenges are resolved and the technology becomes cost-effective, business challenges will remain until the industry settles on a model. According to ASE, the industry will use multiple models depending on the customer and the foundry.



**E. Jan Vardaman,**  
TechSearch  
International, Inc.



Effect of Interposers on 3D IC Forecast

Many approaches to 3D packages exist, including stacked die with wire bond or wire bond/flip chip, stacked packages, package-on-package (PoP), and chip-on-chip (CoC). Companies plan to continue the use of today's 3D packages with evolutionary improvements and adopt a 2.5D or interposer solution until 3D IC challenges can be met. It is important to remember that new package technology introduction takes time and the process and infrastructure have to be well developed: Xilinx spent 6 years to develop its now famous FPGA partitioned die on silicon interposer with TSV solution. ◀



## PACKAGING

# Vertical through-wafer insulation: Enabling integration and innovation

**PETER HIMES**, Silex Microsystems AB, Järfälla SWEDEN

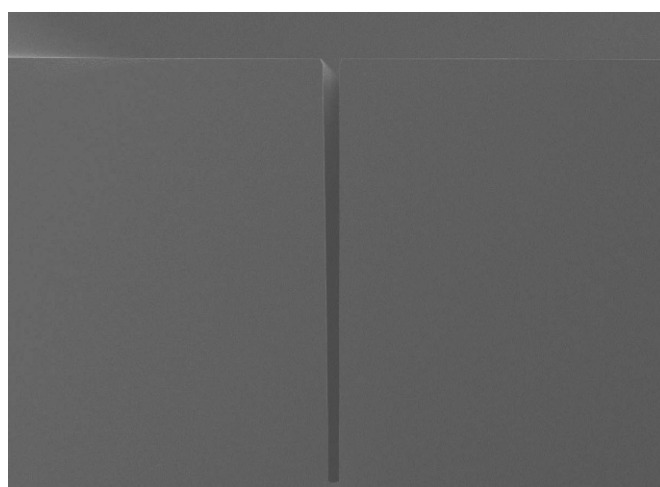
*Through-wafer insulation has been used to develop technologies such as Sil-Via TSV and Zero-Crosstalk.*

**T**SI, or through-silicon insulation, is the processing of silicon wafers by MEMS techniques to create dielectrically isolated areas of the silicon. By taking advantage of the high aspect ratio and vertical sidewall capabilities of deep reactive ion etching (DRIE), trenches can be formed in silicon which extend all the way through the silicon wafer (**FIGURE 1**).

The final wafer after TSI processing exhibits islands of single crystal silicon separated by high quality isolation. This structure is the basis of TSI, and forms the building block of many of Silex's offered technologies.

TSI has been compared to either a dielectric isolation (DI) or silicon-on-insulator (SOI) process, and the comparisons are fairly close. TSI has, in fact, been called a "vertical SOI" process because of its similarity to SOI in creating an insulator-based separation between sections of single-crystal silicon. Unlike SOI, of course, TSI goes vertically through the wafer to create islands of silicon joined by insulating bands. In this second way, it is similar to a DI process where dielectrically isolated islands are created on a SOI device layer, which are then used in device manufacture like diode arrays. Unlike DI, though, TSI extends completely through the wafer: the standard thickness for a TSI processed wafer is 430µm, thick enough to be processed through all MEMS or CMOS steps without the need for special carriers or handling. It is this mechanical strength which makes TSI so useful as a wafer level feature.

MEMS is, of course, a mechanical structure and



**FIGURE 1.** SEM image of TSI DRIE etch through silicon.

MEMS structures can use the entire bulk of the silicon as elements in its construction. This is unlike ICs which are primarily concerned with the surface 10 or 20µm of silicon area where the circuit elements are formed. And yet MEMS wafers undergo wafer processing which has all the requirements of IC processing (in terms of implants, diffusions, thermal or deposited films, thermal budgets, etc.) plus additional challenges of deep etching, forming complex 3D structures, wafer to wafer bonding, debonding, oxide or silicon release, and noble metal processing. Any TSI process, then, would have to hold up to the full range of processing challenges.

## Sil-Via TSV

TSI was developed in the 2003-4 timeframe when a working through-silicon via (TSV) approach was

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## PACKAGING

needed for a major customer. This customer needed a TSV solution which was via-first (the TSV patterned and formed prior to any other wafer processing), high density (small footprint of the device was critical), and high reliability (the end application was a smartphone.)

Traditional approaches to TSVs at the time were poly-fill (which didn't offer the low resistance or reliability that the customer needed) or metal-filled (which suffer from reliability concerns due to TCE mismatch with the silicon), but our engineers recognized that a new approach was needed. Their solution was to take a highly doped substrate, typically

phosphorous doped down to 1-3 m $\Omega$ -cm or less, and use the TSI approach to form a via out of the single crystal silicon (**FIGURES 2 and 3**).

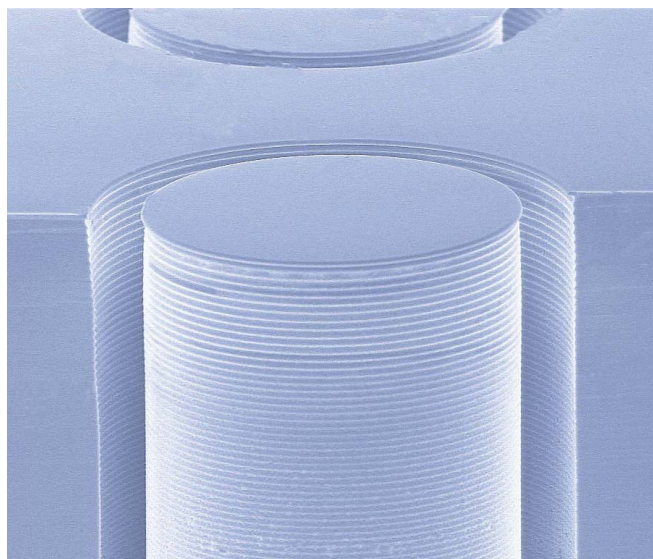
The resulting structure is a single crystal, full wafer thickness TSV exhibiting typical resistances of 0.5-1 $\Omega$  for a 100 $\mu$ m diameter x 430 $\mu$ m thick via. The single crystal construction (formed out of the native wafer material) is perfectly matched thermally to the wafer, eliminating any TCE concerns or reliability issues. The gap formed by the TSI etch is filled by a proprietary insulating material, and gives TeraOhm level DC isolation of the via post to the surrounding substrate.

The Sil-Via TSV went into production in 2005 and eventually ramped up to a peak of 2000 wafers per month. Since then, the Sil-Via has been in continuous production and implemented on over 50 different products on both 6" and 8" wafers. With over 50,000 wafers shipped across all products, we have seen zero field failures for the TSV making it one of the most widely recognized and reliable TSV technologies on the market.

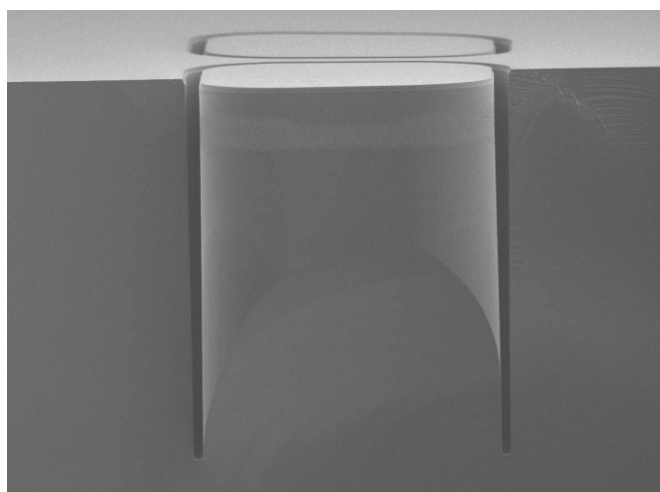
Sil-Via TSVs have been used in bulk MEMS applications, wafer capping, and advanced silicon interposers for 2.5D and 3D packaging, as will be discussed below. They can support via pitches down to 50 $\mu$ m and continuous via formation across the entire wafer. As we shall discuss later as well, Sil-Via provides an intriguing platform for higher functional integration, such as ESD protection diodes and functional interposer solutions.

### Met-Via TSV

While Sil-Via addressed the production, cost, and reliability needs of the market when it was released, TSI has been adapted to support metal through-silicon vias since then. Using the vertical isolation for sidewall protection of the TSV, Silix has brought to market an all-metal TSV that meets the low resistance and high frequency needs of our customers. Licensing the XiVia™ technology from ÅAC Microtec, another Swedish company creating packaging solutions for space-level reliability applications, the Met-Via utilizes two connected DRIE TSVs and double sided copper RDL plating with hermetically sealed vias to create a high reliability metal TSV. The XiVia approach creates a 'locking pin' which protects against thermal cycling concerns, and the hollow-plated TSV gives additional flexion for the TCE mismatch (**FIGURE 4**).



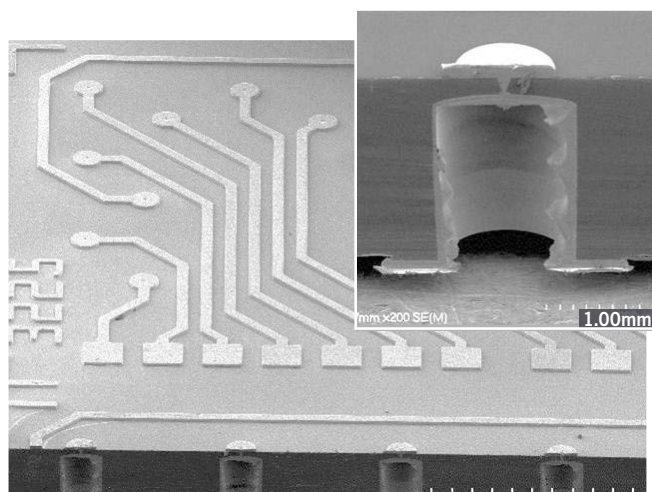
**FIGURE 2.** SEM of the TSI etch to form the Sil-Via TSV.



**FIGURE 3.** Example of two Sil-Via TSVs with oblong shape. Note the tight via pitch possible with TSI processing.



## PACKAGING

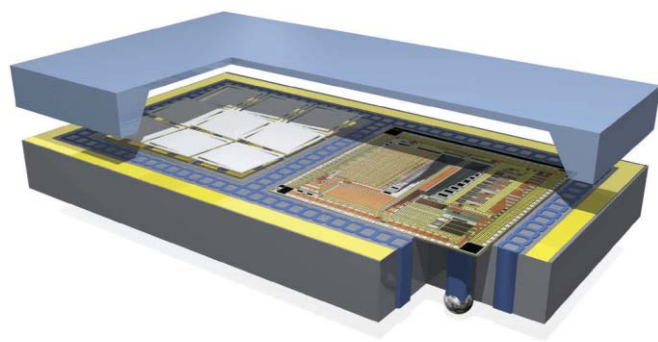


**FIGURE 4.** Microphotograph of Met-Via interposer test structure with close-up of Met-Via cross-section showing the XiVia feature. (some metal smearing evident due to wafer saw).

### Zero-Crosstalk substrate isolation

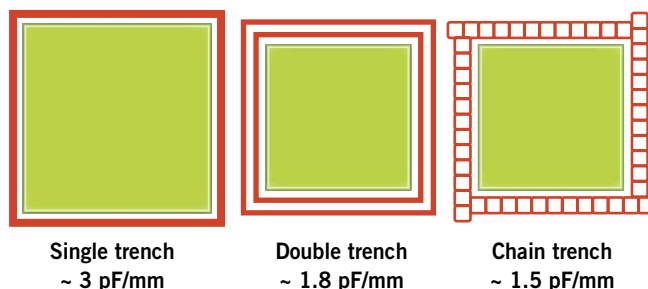
The Sil-Via TSV is in essence a round post through the silicon wafer, but the beauty of TSI's flexibility is that it doesn't have to be like that. TSI is patterned by lithography, so any geometry or shape can be formed as a TSI structure (There is a practical limit to this: first there are processing challenges relating to the percent of silicon being etched away across the entire wafer, and second the trench width has to be consistent in order to have a complete and reliable fill).

Taking a clue from the "Vertical SOI" image of TSI, Silex developed and also offers a substrate isolation platform called Zero-Crosstalk™. This uses either chains of Sil-Via type structures, or continuous trench rings to define the isolated areas of the silicon. Each silicon island then is completely DC isolated from its neighbors,



**FIGURE 5.** Zero-Crosstalk™ concept CAD drawing.

making them act as physically distinct pieces of silicon. A common application for Zero-Crosstalk is to create separate analog and digital grounds for mixed-signal applications (**FIGURES 5 and 6**).



**FIGURE 6.** Three different options for Zero-Crosstalk showing typical capacitance figures for a 20µm trench – 350µm wafer thickness implementation.

Zero-Crosstalk can be implemented on low resistivity or high resistivity substrates, making it a viable technology for IC substrate isolation as well (**FIGURE 7**).

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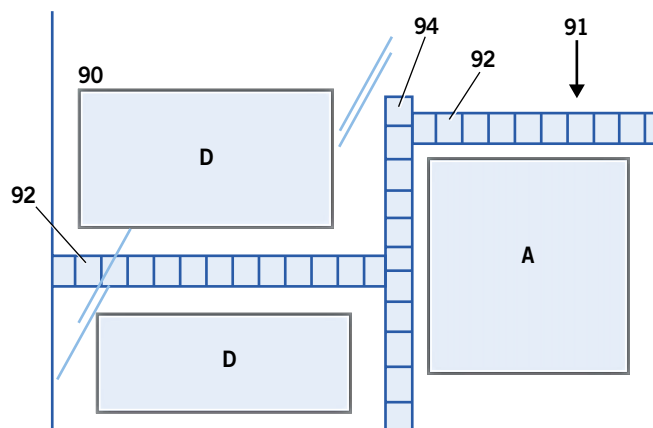
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## PACKAGING



**FIGURE 7.** CAD drawing showing separate analog/digital substrate areas defined by Zero-Crosstalk.

In the MEMS area, Zero-Crosstalk has among other applications been used for LED interposers to provide isolated substrates for diode arrays, X-Ray detectors to isolate individual detection elements, and in the following example.

In this product example of a microbattery array from mPhase Technologies, TSI is used to create electrically isolated microbattery cells which also act as electrical interconnects through the cell layers. This is an example of the flexibility of TSI, where arbitrary geometries can be defined which can act both as Zero-Crosstalk areas and Sil-Via TSVs (**FIGURES 8-10**):

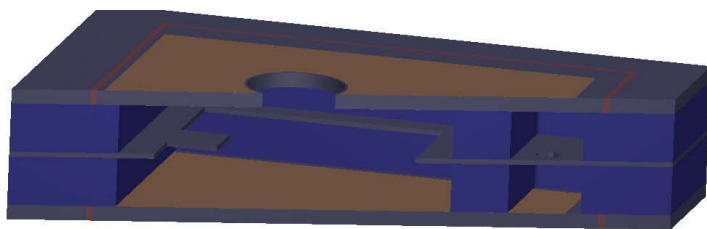
### The rigid interposer approach

The application which drove the development of TSI and the Sil-Via TSV was for a 2.5D interposer with Zero-Crosstalk for cellphone microphones, with the CMOS ASIC mounted side-by-side. MEMS has, in fact, always been involved with advanced packaging requirements because of the need to package the MEMS and IC in the same package.

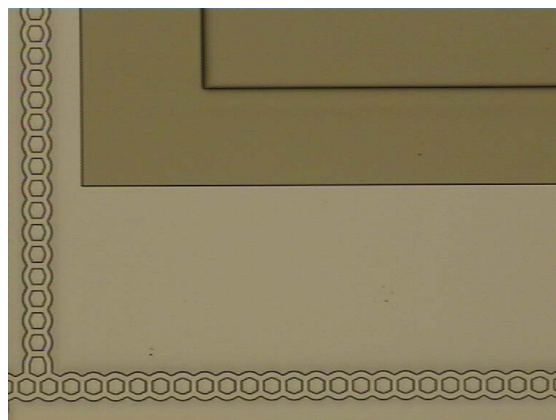
Interposers for package-level integration of multichip ICs is an emerging hot topic and an area that most major OSATs, one where packaging houses are looking to provide complete solutions. MEMS foundries like Silex have a critical role to play in this emerging supply chain, as the interposer foundry for either the IC company or the OSAT directly, as neither

entity nor the traditional IC foundry has the infrastructure or expertise to build these 3D structures reliably and in high volume. Yole Developpement refers to this emerging supply chain element as the “Mid-End Foundry,” and predicts it will service a \$1.7B market by 2017 as interposer packaging hits the mainstream.

And yet, despite all the press about 3D integration, the engineering challenges of 3D packaging have presented a substantial barrier to companies pursuing this packaging path. This is because each element of the package presents engineering challenges, and the current focus of the 3D industry (ultra thin wafers, specialty wafer handling, organic substrates, chip to chip signal routing, thermal and electrical optimi-

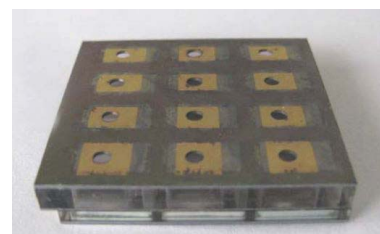


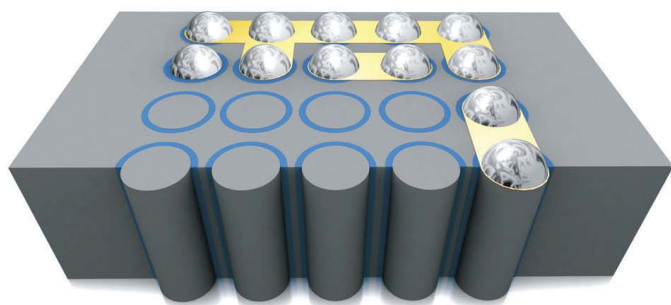
**FIGURE 8.** Cross section diagram of the 5-layer bonded mPhase microbattery structure.



**FIGURE 9.** Photomicrograph of the TSI chain structure defining the Zero-Crosstalk TSV structures for the mPhase microbattery.

**FIGURE 10.** Photomicrograph of the final mPhase microbattery (image courtesy mPhase Technologies, Inc.).





**FIGURE 11.** Graphic of a Sil-Via based interposer.

zation, and yield loss ownership by the supply chain) make the challenges to adoption more daunting. This focus is also concentrating on the very bleeding edge of technology (like the highest cost FPGAs), technologies which are overkill for the majority of ICs being produced in the market.

Our approach is to leverage our full wafer thickness TSI technology to provide rigid interposers to the marketplace, simplifying the engineering and supply chain challenges. “Rigid Interposers” means interposers from 300 to 430 $\mu$ m thick, with enough mechanical strength to support the microbump, mounting and molding steps of the assembly process. By eliminating the ultrathin wafer requirements and associated bonding, debonding, and carrier handling steps, not only is the assembly process simplified but the organic substrate used in the 2.5D package can be eliminated. What results is an all-silicon package which is reliable, mechanically strong, and thermally stable for advanced IC use (**FIGURE 11**).

2.5D packaging technologies offer integration and footprint reduction advantages to a wide range of IC uses, yet the extreme costs and engineering challenges of the mainstream approach effectively removes it from consideration for the majority of the market. We believe that rigid interposers not only simplifies the engineering challenges, but makes 2.5D a viable option for a much broader IC market.

### Future TSI-enabled markets

Even though it was created to solve a specific need, TSI remains a platform for innovation in bringing new customer-integratable features to the market. Among the technologies being worked on by Silex or with customers today are:

- Full DI substrates for IC processing – the application of Zero-Crosstalk for IC applications, taking the concept of full dielectric isolation all the way to the IC fab.
- CMOS TSVs – TSVs as interconnects which allow stackable components has long made technological and economical sense for MEMS components. Extending this to the IC world as a via-first or via-middle technology which can support full IC processing is the natural progression of this capability.
- Metal IC TSVs – Many ICs require the performance of an all-metal TSV, and foundries want to avoid the cost and expense of thin wafer handling. Integrating the Met-Via TSV as a via-middle process into the customer’s design and IC flow affords the advantages of all metal TSVs without the limitations of thin wafer handling (which are only available at the highest and most costly technology nodes)
- TSVs with Integrated Diodes – since Sil-Via is a doped substrate silicon TSV, the via can be constructed to incorporate blocking or steering diodes directly into the via, thereby giving active component capability integrated directly into the via.
- TSVs with ESD protection – a variant of the integrated diodes, especially for interposers where multiple chips can be interconnected and protected at the same time
- Through-silicon 3D inductors – making use of the copper TSV technology of Met-Via to create a true wound inductor, using the silicon wafer itself as the inductor spool. A mag core element can be integrated to boost Q value, as well.

### Summary

The TSI platform has proven to be a very reliable and production worthy technology. In continuous production for over six years, it has been integrated in one form or another in over two dozen different projects. Customers, working with Silex engineers, continue to find innovative ways to take what’s available in TSI and re-purpose it for another use. By providing higher value customer-integratable features, both Silex and the customers stay ahead in the MEMS and packaging games. TSI truly allows all true semiconductor integration options to be “more than Moore.” ◀



## RELIABILITY

# Today's top reliability challenges

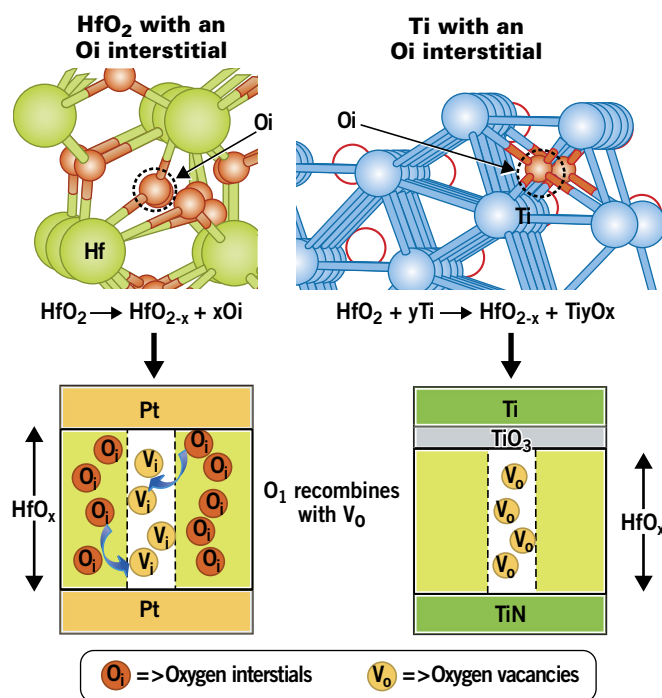
**PETE SINGER**, Editor-in-Chief.

*BTS, BTI, soft errors, dielectric breakdown and other reliability challenges will be addressed at the upcoming International Reliability Physics Symposium.*

A double challenge faces today's reliability engineers. They not only must understand the physics behind a complex set of mechanisms, such as bias temperature instability (BTI), but they must accurately simulate those mechanisms through modeling to predict device performance over time and estimated end-of-life.

These challenges will be front and center at the upcoming International Reliability Physics Symposium (IRPS), to be held April 14-18, 2013 at the Hyatt Regency Monterey Resort & Spa in Monterey, CA. The conference begins with tutorials on Sunday that run through Monday afternoon (40% of attendees are first time attendees). A plenary session on Monday afternoon after the tutorials is a "Year in Review" where experts highlight work published over the last year. Tuesday morning starts with a keynote by Berkeley's Chenming Hu who will talk about compact modeling as well as tri-gate scaled reliability challenges. Krishnan said that compact modeling is one of the main themes of this year's conference. "There has been a lot of work on how do we take reliability into the circuits and how do we model, not only at the SPICE level, but from a compact modeling perspective," he said. The Compact Modeling Council will have a meeting immediately following IRPS at the same location. Tuesday's keynote is followed by 19 sessions in three tracks, with a panel session, workshop and a combined poster session and buffet at Chateau Julien wine estate on Wednesday evening.

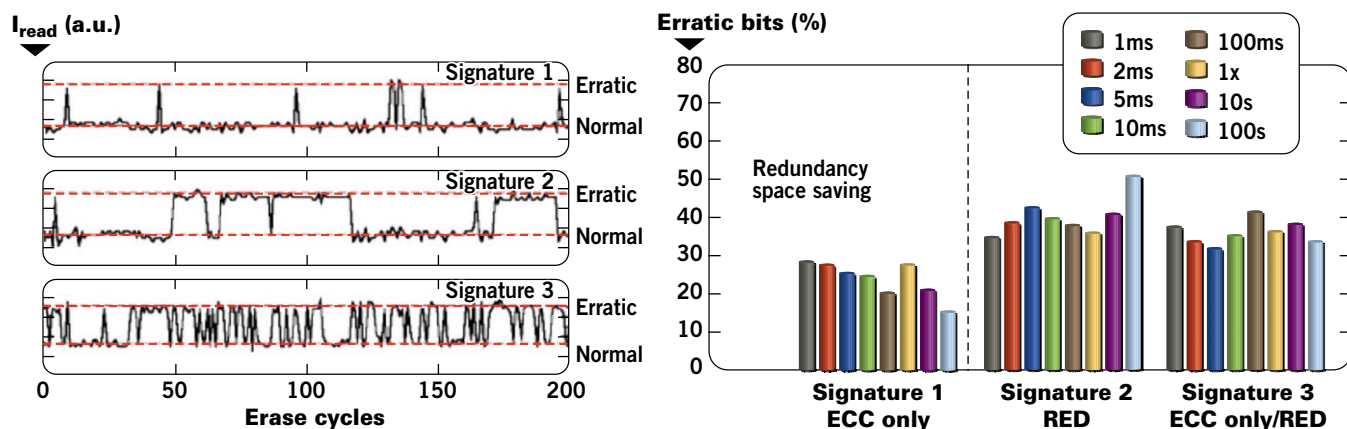
In terms of the overall reliability concerns now facing the industry, Krishnan said the number one thing people are worried about is the tri-gate finFET.



**FIGURE 1.** Atomistic structure of HfO<sub>2</sub> with an O<sub>i</sub> interstitials leading the the recombination of Oi+Vo in Pt/ Pt during reset (left). Atomistic structure of Ti awith an O<sub>i</sub> interstitial creating more V<sub>o</sub> in HfO<sub>2</sub> (right).

"Our devices have been planar but now all of the sudden you have three sides to it. How do you reject the heat from a finFET?" he asks. "The second concern is basically electromigration. How do we scale EM?" The third main challenge lies in gallium nitride and HEMT structures. "What is the reliability of these GaN FETs in the field when you have some of these trapping effects that go on?" Krishnan asks. "The switch is good on day one but it slowly degrades over time. That's why you're seeing a lot on GaN FETs."

A few examples that will be presented at this year's IRPS will serve to highlight the reliability issues facing the industry.



**FIGURE 2.** Examples of different erratic bit signatures (left). Normal and erract states are highlighted for clarity. Erratic bits percentage per signature classification in delay time cycling experiments are shown on the right.

### Reliability in memories

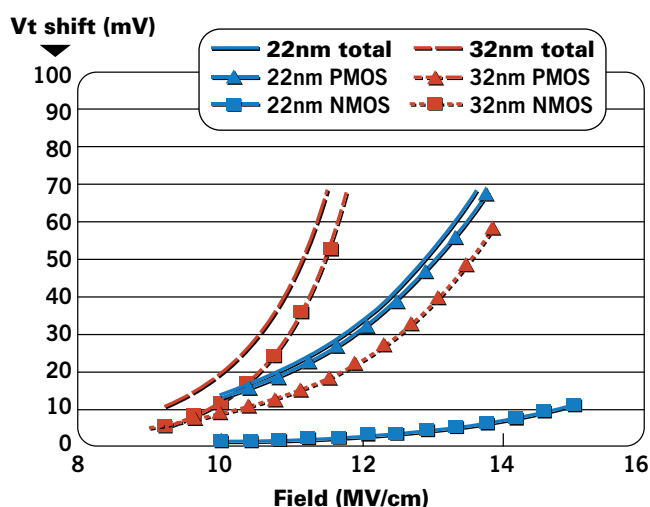
Researchers from Mila Polytechnic, Micron and Intel will present a paper titled “Resolving Discrete Emission Events: a New Perspective for Detrapping Investigation in NAND Flash Memories.” Charlie Slayman, IRPS Vice Technical Program Chair, said that researchers looked at the effects of individual discrete traps in the tunnel oxide for 30nm NAND flash. “Looking at the threshold voltage over time, you can actually see the threshold voltage change in discrete quantized steps. They’ve analyzed this and determined these are individual traps in the device that are trapping and detrapping. This will have an impact on future flash technologies where single electron and defects become increasingly important,” Slayman said.

In a second paper on resistive RAM, authors are from Minatec and coauthors from the Center for Semicon-

ductor Components at the University of Campinas Brazil and the department of electrical engineering at Stanford studied the retention time -- the ability of a resistive RAM device to maintain its resistance state. The RAM consists of two metal electrodes and a hafnium oxide between those, where the hafnium oxide acts as a variable resistor. The authors look at the use of different metal materials. In one case they use platinum for the electrode, and in a second example they use a TiN-Ti to sandwich the hafnium oxide. They showed that the Pt/Pt electrode device loses its on-state resistance sooner than the TiN/Ti device. “They attribute the phenomenon to oxygen interstitials in the  $\text{HfO}_2$ , and TiN-Ti’s ability to basically getter those interstitials and pin them at the surface,” Slayman said. This is illustrated in **FIGURE 1**.

A third paper on memory focuses on flash, specifically erratic bit classification in flash devices used in automotive applications. The authors studied error correction code and redundant addresses, both of which are widely used in flash as well as SRAM and DRAM memory. “What’s new with this paper is the authors have classified these erratic or bad bits,” Slayman said. **FIGURE 2** shows three different types of erratic bits and their behavior over time. “In the first case, they are looking at the read current of one type of erratic bit where it will periodically spike to a higher read current. Then there’s another type of erratic bit they observed where about half the time, it’s in a low read current state and the other half of the time it’s in a high read current state. Then they have a third class of erratic bits where it’s just going back and forth constantly between the high read state and the low read state,” Slaymain explained.

Typically, redundant address repair would be used



**FIGURE 3.** 22nm BTI is comparable to 32nm. NMOS is significantly improved due to gate optimization and WF scaling.

## RELIABILITY

when these bad bits are created, after so many read-write cycles, but that can be an expensive fix. "For a certain class of bad bits -- such as the erratic bits on the top of Fig. 3, that are most of the time good and only infrequently bad -- don't bother using redundant address, just use your error correction code and that's sufficient," Slayman said. "Save your redundant addresses for the really bad erratic bits." The authors demonstrated that they can save 35% of their redundancy space by using this classification scheme.

## FinFET concerns

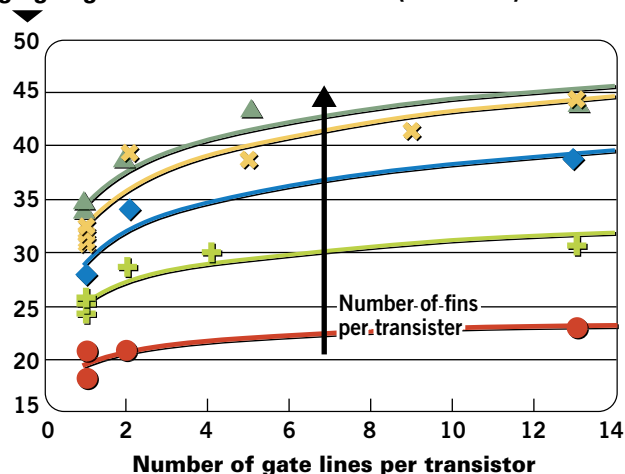
At the device level, Giuseppe Larosa, IRPS Technical Program Chair, said the focus is squarely on FinFETs. "For future nodes, 14nm and down to 10nm, FinFETs will be the device design of choice," he said.

Larosa said one of the key questions people ask is how BTI is actually scaling when we go to finFETs. "Key information is coming from Intel, suggesting that NBTI seems to be an issue because it's increasing with finFET scaling." At IRPS, Intel will present a comparison of 32nm planar technology to a 22nm finFET technology, as shown in **FIGURE 3** (32 in red and 22nm in blue). "You can see they can manage to really reduce the PBTI but the NBTI is actually getting worse with scaling," he said.

The second item on the list for finFETs is self-heating. "Self-heating is always there," said Larosa. "Anytime you drive current through a channel you produce some self-heating. But if you have a bulk technology, the self-heating will just move away down into the bulk. But in finFETs, because it's a three-dimensional structure, this self-heating is a bottleneck in scaling down."

Another Intel paper talks about the effect of self-heating in accelerating aging, not only at the level of the device in terms of finFETs, but also in terms of metal wires that are sitting on top of the finFET. "You may have some impact on electromigration in the metal wires. You can have enhanced electromigration simply because the self-heating of the finFET can locally increase the temperature in the metal wires above," Larosa explained. "A key issue here is how to calibrate the self-heating to make sure that you have a good understanding of the local temperature of the structure, and then how to take that into account in

Aging degradation with channel ON (arb. units)



**FIGURE 4.** Self-heat manifests as a sensitivity to the fin or gate count in switching aging degradation. Here, switching conditions are accelerated to enhance the sensitivity.

your models that predict end-of-life aging, specifically finFETs and metal lines," he said.

**FIGURE 4** shows how self-heating at the device level is affecting aging of a given FET: It's a function of the number of fins and the number of active lines per transistor. "It looks like through optimization of the gate stack with appropriate oxide scaling and metal gate work function tuning and so on, you can achieve reliability similar to previous nodes," Larosa said.

Another reliability concern to be discussed at IRPS: High-k dielectrics. "There are two aspects of high k dielectrics that people have to face," Larosa said. "BTI is again a concern with continued scaling. Contrary to nitride oxides, high-k bring a higher sensitivity to the NFET devices to PBTI. This is mostly due to the fact that the high-k material can be sensitive to electron trap activation or generation, producing PBTI effects that you will not see in standard nitride oxide technologies."

At IRPS, GLOBALFOUNDRIES will present the first large-scale stochastic BTI (particularly PBTI) study in metal gate/high-k technology confirming fundamental BTI area scaling trends derived from conventional SiO<sub>2</sub> technologies, and IBM will report on TDDDB in high-k, and how it will lead to more accurate models. "Without this model you cannot be confident in predicting end of life, and having this type of simulation can help in making a projection that will be relevant for product level of circuit level reliability," Larosa said. ◀



## INSPECTION

# Exploring the dark side

REBECCA HOWLAND, Ph.D. and MARC FILZEN, KLA-Tencor, Milpitas, CA.

*A look at the impact of back side particles on front side defectivity.*

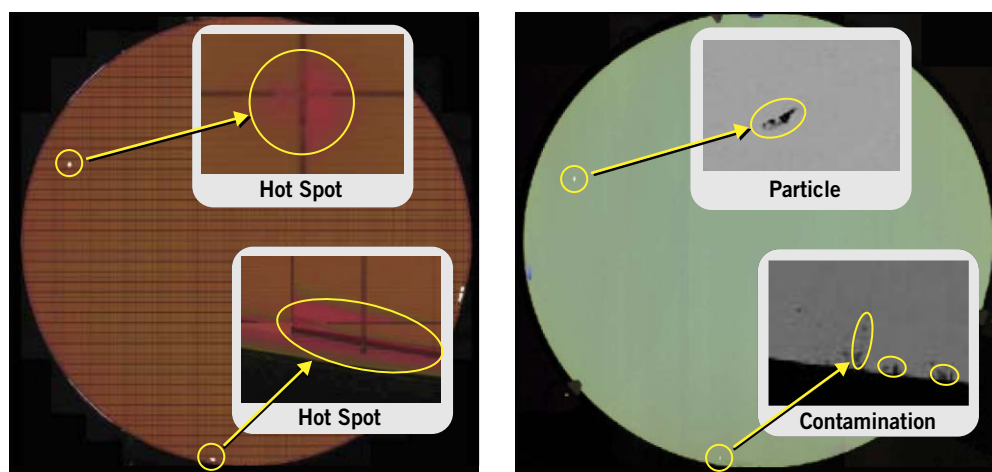
When a 300mm wafer is vacuum mounted onto the chuck of a scanner, it needs to be flat to within about 16nm over a typical exposure field, for wafers intended for 28nm node devices.[1] A particle as small as three microns in diameter, attached to the back side of the wafer—the dark side, if you will—can cause yield-limiting defects on the front side of the wafer during patterning of a critical layer. The impact of back side particles on front side defectivity becomes even more challenging as design rules decrease.

Studies have shown that a relatively incompressible particle three microns in diameter or an equivalent cluster of smaller particles, trapped between the chuck and the back surface of the wafer, can transmit a localized height change on the order of 50nm to the front side of the wafer.[2] With the scanner's depth-of-focus reduced to 50nm for the 28nm node, the same back side particle or cluster can move the top wafer surface outside the sweet spot for patterning. The CD of the features may broaden locally; the features may be misshapen. The result is often called a *defocus defect* or a *hotspot* (FIGURE 1). These defects are frequently yield-limiting because they will result in electrical shorts or

opens from the defective feature to its neighbors.

A particle on the back side of the wafer may remain attached to the wafer, affecting the yield of only that wafer, or it may be transferred to the scanner chuck, where it will create similar defects on the next wafer or wafers that pass through the scanner.

At larger design nodes, back side defects were not much of an issue. The scanner's depth of focus was sufficient to accommodate a few microns of localized change in the height of the top surface of the wafer. At



**FIGURE 1.** Caption: Correlation between front side (left) and back side (right) results is evident in the wafer defect maps and patch images

larger design nodes, then, inspection of the back side of the wafer was performed only after the lithography track and only if defects were found on successive wafers, indicating that the offending particle remained on the scanner chuck, poised to continue to create

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## INSPECTION

yield issues for future wafers. In this case corrective measures were undertaken on the track to remove any suspected contamination. The track was re-qualified by sending another set of wafers through it and looking for defectivity at the front side locus of the suspected back side particle. This reactive approach was economically feasible for most devices throughout volume production of 32nm devices.

At the 28nm node, however, lithography process window requirements are such that controlling back side particles requires a more proactive approach. Advanced fabs now tend to inspect the wafer back side before the wafer enters the scanner, heading off any potential yield loss. Scanner manufacturers are also encouraging extensive inspection of the back side of wafers before they enter the track. As we see what lithography techniques unfold for the 16nm, 10nm nodes and beyond, it's entirely possible that 100% wafer sampling will become the best-known method.

As with inspection of the front side of the wafer,

sensitivity to defects of interest (DOI) and the ability to discriminate between DOI and nuisance events are important. Even though particles need to be two to three microns in diameter before they have an impact on front side defectivity, the inspection system ought to be able to detect submicron defects, since small defects can agglomerate to form clusters of critical size. Submicron sensitivity is beneficial for identifying process tool issues based on the spatial signature of the defects—while high-resolution back side review enables imaging of localized defects, so that appropriate corrective actions can be taken to protect yield. Submicron sensitivity also serves to extend the tool's applicability for nodes beyond 28nm. ◀

### References

1. Assuming 193nm exposure wavelength, NA = 1.35 and K2 = 0.5, then depth of field = 50nm. Normally 30% of the DOF is budgeted for wafer flatness.
2. Internal studies at KLA-Tencor.



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## CMP

# Automatic wafer inspection system replaces eyeballs with cameras

**CHRISTOPHER ERIC BRANNON**, Texas Instruments, Inc., Dallas, TX

*A fully automated RDS inspection system that replaces human inspectors is a game changer.*

**T**he chemical-mechanical polishing (CMP) process in the fabrication of silicon wafers is exceedingly labor intense. As a result, automating a critical aspect of CMP – namely, the physical inspection of wafers for metal residue following CMP – cannot only improve CMP cycle times, but it also can be integrated into a quality control system that improves wafer yields and maintains those yields at a high level.

The typical method for inspecting wafers as they emerge from CMP has involved a technician visually examining one wafer at a time as it is raised on an H-bar wafer elevation tool (**FIGURE 1**). The inspector would try to detect metal residue left on the wafer following an incomplete polishing process. If undetected, this metal residue can damage the devices made from the silicon. In other words, undetected metal residue can cause wafer and chip yields to plummet.

Of course, manual inspection processes have inherent limitations. Technicians may not perform a thorough inspection of the entire wafer or miniscule remnants of residue may elude human vision. Microscopes are also difficult to employ at today's technology nodes. And, expanding wafer sizes, from



**FIGURE 1.** Manually inspecting a wafer on an H-bar tool.

200mm to 300mm, doubles the area that must be inspected, increasing the chances that residue somewhere on the wafer will elude the human eye.

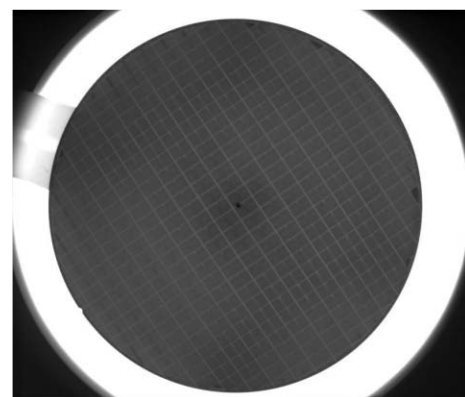
As a result of this situation, research was begun to develop a low-cost, single-step automated process that would inspect 100 percent of all wafers after the CMP polishing process. Improved yields would be achieved by detecting residue more effectively and by incorporating the results of the inspection into a closed-

loop feedback system that would control and dynamically fine tune the CMP process. At the heart of this automated residue detection system (RDS) would be a high-resolution imaging capture and compare process.

## Capturing the golden wafer

First the RDS's camera must scan a

**FIGURE 2.** A grayscale image of a wafer.



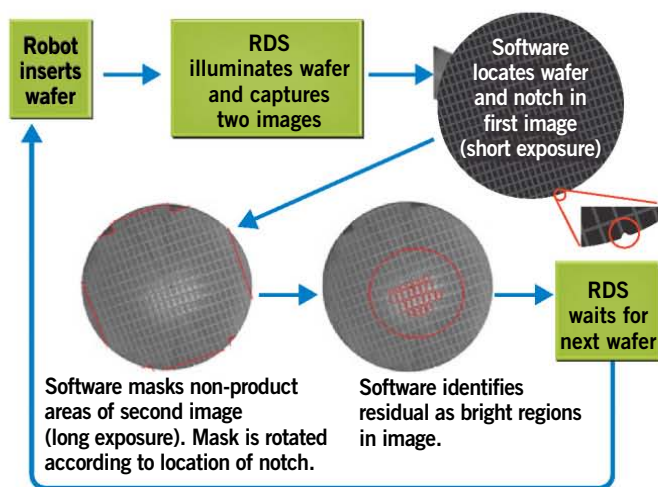
**CHRISTOPHER ERIC BRANNON**, is a DMOS5 Copper CMP Manufacturing Engineer Texas Instruments, Inc., Dallas, TX.



## CMP

fully polished and fully metalized wafer. This image will become the golden wafer or reference wafer for subsequent inspections. A grayscale map of the golden wafer is stored and reference values are associated with various characteristics of the wafer, such as the thickness variations in metals and dielectrics, the number and orientation of detectors, edge exclusions and the metals detected, usually tungsten or copper.

With the image of the golden wafer stored, the RDS can begin inspecting production wafers. Each production wafer is scanned and a grayscale image captured (**FIGURE 2**) which is compared to the golden wafer. The differences in the gray levels between the image of the production and that of the golden wafer will reveal any residual metal remaining on the production wafer (**FIGURE 3**).



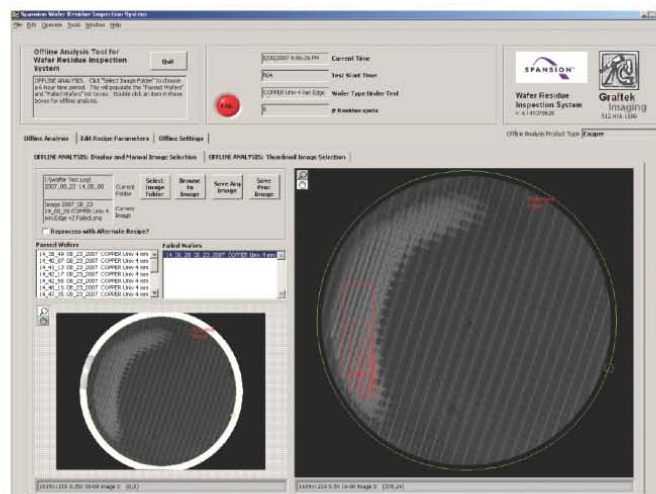
**FIGURE 3.** RDS system flow diagram.

As mentioned, the data gathered by the RDS following CMP polishing can be fed back into a control mechanism that can adjust the parameters of the CMP process itself and thereby improve its effectiveness. This is best illustrated by citing several brief case studies:

### Erroneous CMP recipe

A set of 25 wafers was inspected with the RDS tool and residual metal was detected on every wafer (**FIGURE 4**). Manual inspection with a microscope confirmed the presence of the metal residue.

The consistent location of the residue and the fact that it was present on each wafer indicated a systemic



**FIGURE 4.** The RDS detected residual metal on the wafer.

fault of some sort. This knowledge assisted in the troubleshooting exercise that ensued. Eventually, it was determined that the software controlling the CMP process had employed an incorrect polish recipe with shorter polish times and other erroneous process parameters.

### Flow problems

In another case, the polish used in the CMP process began to exhibit random or non-linear behavior result patterns. Specifically, some, but not all, of the wafers inspected by RDS had a considerable amount of residual metal at the center of the wafer (**FIGURE 5**). The erratic polishing patterns led to an examination of the CMP slurry flow on the polishing pad. It was concluded that the flow of slurry to the pad was interrupted intermittently; hence, the erratic behavior patterns of the polishing process.

### Operator error

Subsequent to the polishing of a batch of wafers, inspection by the RDS system revealed that five wafers were inexplicably left unpolished. Fortunately, the relatively fast cycle time of RDS allows for 100 percent inspection of all wafers. Eventually, the mysterious five unpolished wafers were attributed to operator error. Had RDS not been capable of inspecting every wafer, the five unpolished wafers might have been missed completely.

*Continued on page 32*

## RELIABILITY

# Insights into low frequency noise in high-mobility transistors

**EDDY SIMOEN**, imec, Leuven, Belgium

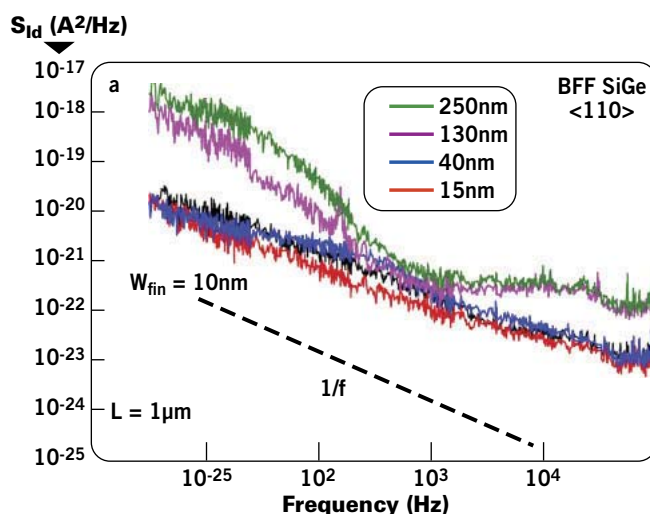
*The impact of high-mobility channel materials and novel device architectures on the low-frequency noise behavior of 22nm and below CMOS transistors is reviewed.*

The implementation of novel high-mobility channel materials (SiGe, Ge, III-V) and the use of advanced device architectures (thin films on UTBOX, FinFETs and nanowire transistors) in upcoming CMOS nodes strongly affect their low frequency (LF) noise performance [1,2]. Both  $1/f$  noise and gate-voltage dependent generation-recombination (GR) noise can be found in silicon bulk FinFETs[2]. The flicker noise mechanism can be governed both by number and mobility fluctuations in the same wafer, while the GR noise, normally ascribed to trapping in the gate dielectric, causes a significant variability of the power spectral density (PSD).

## Impact of high-mobility channels

It has been shown that the implementation of strained SiGe channels not only boosts the device performance [3,4] but at the same time, can result in a lower noise PSD, when the channel is off-set from the interface [5,6].

To study the impact on the noise, a comparison is made with planar implant-free quantum well (IFQW) pMOSFETs, exhibiting mainly  $1/f$  noise which is governed by mobility fluctuations, based on the behavior of the normalized current PSD versus the channel current in linear operation. Contrasting LF noise spectra (**FIGURE 1**) and PSD (**FIGURE 2**) are



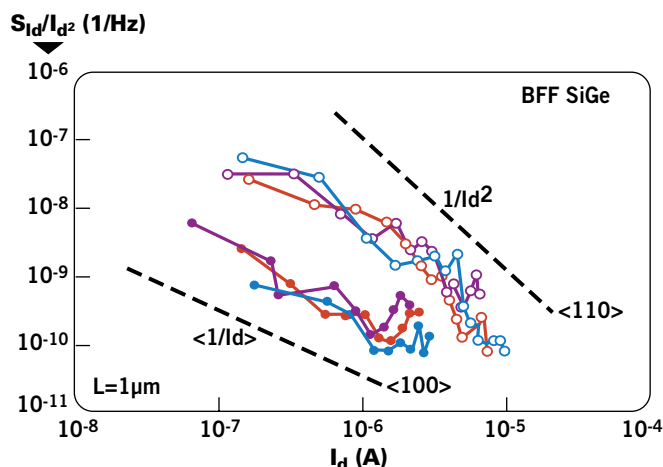
**FIGURE 1.** Current noise PSD versus frequency, corresponding with p-type SiGe-channel BFFs fabricated on a (110) Si substrate, respectively, with  $L=1\text{ }\mu\text{m}$  and different  $W_{fin}$ .

seen for (110) and (100) SiGe p-channel bulk FinFETs. While the (100) devices exhibit similar behavior as the planar references, the (110) structures suffer from excess GR noise, especially for larger widths. This is associated with the faceting of the SiGe QW, which introduces extended defects in the material.

The reduction of the  $1/f$  noise in SiGe buried channel pMOSFETs is well documented in the literature [5-8] and has recently also been demonstrated for SOI pFinFETs [9]. In case the PSD is related to number fluctuations, this

E. SIMOEN, T. ROMEO, L. PANTISANO, A. LUQUE RODRÍGUEZ<sup>1</sup>, J.A. JIMÉNEZ TEJADA<sup>1</sup>, M. AOULAICHE, A. VELOSO, M. JURCZAK, R. KROM, J. MITARD, CH. CAILLAT<sup>2</sup>, P. FAZAN<sup>2</sup>, F. CRUPI<sup>3</sup>, and C. CLAEYS<sup>4</sup>; Imec, Kapeldreef 75, B-3001 Leuven, Belgium. Tel.: +32-16-28 13 81, Fax: +32-16-28 17 06, Email: Eddy.Simoen@imec.be; <sup>1</sup>University of Granada, Spain, <sup>2</sup>Micron Technology Belgium, Leuven, <sup>3</sup>University of Calabria, Italy, <sup>4</sup>also at KU Leuven, Belgium. Originally presented at the 2013 International Electron Devices Meeting.

## RELIABILITY



**FIGURE 2.** Normalized noise spectral density versus drain current  $I_d$  for a number of p-type SiGe-channel BFFs fabricated on (100) and (110) Si substrates, at  $f=25\text{Hz}$ .

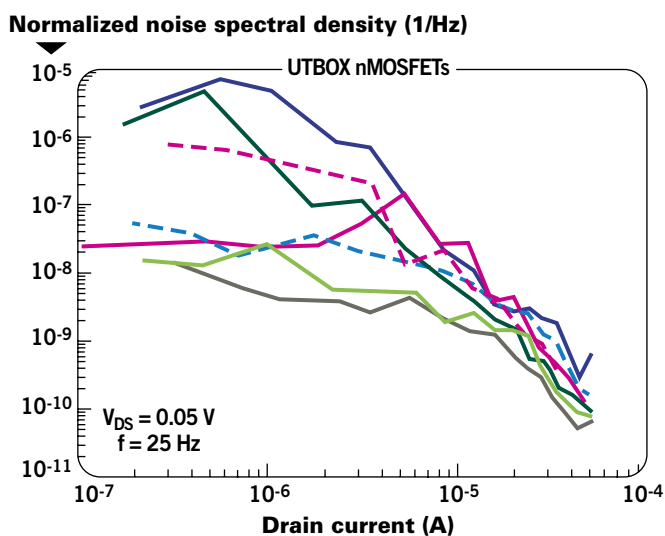
reduction can be ascribed to the larger tunneling distance and the valence band offset of the SiGe QW with respect to silicon, which reduces the number of accessible traps in the gate dielectric. At the same time, the presence of extended defects in (Si)Ge channel pMOSFETs can contribute excess GR noise [1], as in the case of the (110) channel devices reported here. These extended defects are related to the faceting of the epilayer. This also gives rise to a higher density of interface states, where both top and sidewalls are according to different (110) lattice planes.

In spite of this, the highest hole mobility is obtained for the (110) based SiGe-channel pMOSFETs, which can be ascribed to the favorable channel orientation compared with (100) silicon substrates.

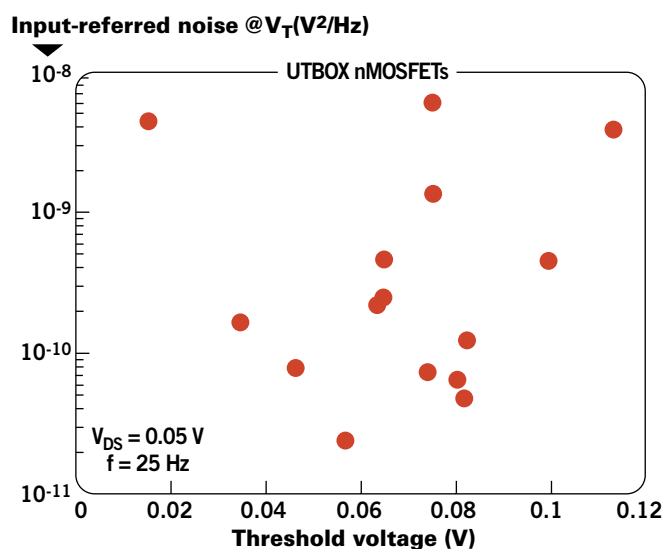
### LF noise variability

A general tendency for the noise of transistors with nanometric device dimensions is the large, orders-of-magnitude variability of the noise PSD, which is usually due to the presence of random telegraph noise (RTN), associated with traps in the gate oxide. A similar variability has been found in Si bulk FinFETs [2] or in SiGe channel bulk FinFETs. A detailed numerical simulations' analysis has recently been reported [10], investigating the role of the position of the RTN trap with respect to the channel on the induced relative current switching amplitude  $\Delta I_d/I_d$ .

However, it has also been noted that the responsible  $1/f$  noise mechanism for bulk FinFETs changes from number to mobility fluctuations *within the same wafer and from die to die* [2]. This implies other possible origins of the PSD variability. Therefore, a more systematic study of the LF noise variability has been undertaken in UTBOX SOI nMOSFETs, developed for 1-transistor (1T) Floating-Body RAM (FBRAM) memory applications, with a BOX thickness of 10 nm

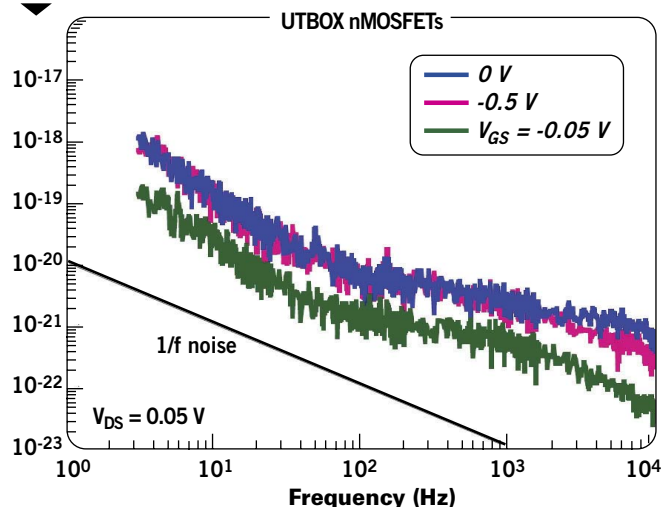


**FIGURE 3.** Normalized noise current spectral density versus drain current at  $f=25\text{Hz}$  and in linear operation for a set of  $1\text{mm} \times 0.105\text{mm}$  UTBOX SOI nMOSFETs, aligned across the vertical diameter in the center of the wafer.

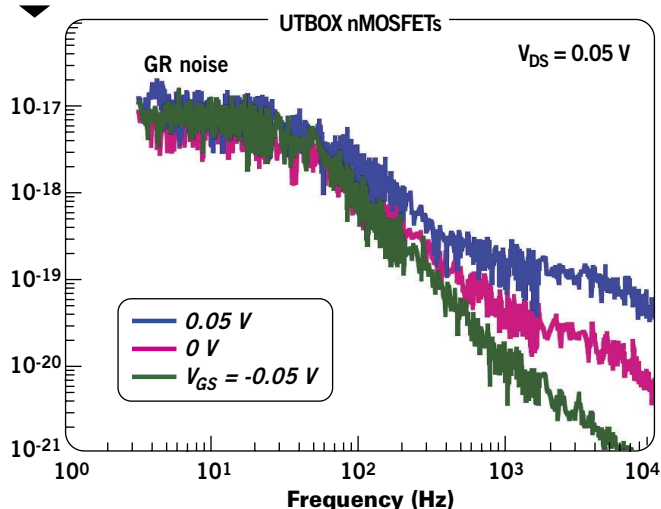


**FIGURE 4.** Correlation between the input-referred noise PSD  $S_{VG}@V_T$  at 25 Hz versus threshold voltage for  $1\text{mm} \times 0.105\text{mm}$  FD UTBOX SOI nMOSFETs on the same wafer in linear operation ( $V_{DS}=50\text{mV}$ ).



Current noise spectral density ( $A^2/Hz$ )

**FIGURE 5.** Low-frequency noise spectra around  $V_T$  for a 1 mm x 0.105mm FD UTBOX SOI nMOSFET exhibiting predominantly 1/f noise around 25 Hz.

Current noise spectral density ( $A^2/Hz$ )

**FIGURE 6.** Low-frequency noise spectra around  $V_T$  for a 1 mm x 0.105mm FD UTBOX SOI nMOSFET exhibiting two GR noise components, one showing gate voltage dependence while the other one does not.

and a film thickness of 10 or 20 nm. The impact of the presence of extensions has also been evaluated. An example is given in **FIGURE 3**, whereby no clear correlation has been found with the corresponding variability in the DC parameters, like the threshold voltage (**FIGURE 4**). From comparing **FIGURES 5 and 6**, it is derived that the higher LF noise PSD is due to excess GR noise, which in many cases exhibits gate-

voltage dependent parameters (corner frequency  $f_0$  and plateau amplitude  $SI(0)$ ).

### LF noise model for FD thin-film or narrow-fin devices

While gate-voltage-dependent Lorentzians are usually ascribed to traps in the gate oxide [11], we have shown that in the case of FD devices, GR centers in the Si film (or fin) can give rise to the same behavior. We have also shown that the SRH time constant can vary significantly with gate bias, as this modulates the electron quasi-Fermi level with respect to the trap level position  $ET$ .

Our model has some important implications. First, it provides a tool for GR defect spectroscopy in advanced FD or narrow-fin devices: from the VGS at maximum plateau amplitude, one can readily derive the trap activation energy, as  $ET$  coincides with the calculated  $EF_n$ . Combining with the calculated free carrier densities, one may derive the electron and in

Continued on page 28

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some cases also the hole capture cross section from Eq. (2). Finally, the trap concentration follows from  $SI(0)$ . This is equivalent to changing the temperature in PD or bulk devices [11], resulting in the construction of an Arrhenius plot. However, here the Fermi level is modulated by the gate voltage instead of the temperature. It has been verified that both analysis methods yield the same activation energy for the trap levels, responsible for the GR noise. In case of two independent gates, like for SOI devices with UTBOX, the back-gate voltage provides an additional degree of freedom to scan the band gap of the semiconductor.

A second important consequence is that the model provides an alternative explanation for the variability of the noise PSD in thin-film or narrow-fin structures: GR noise amplitude can be varied over more than a decade, depending on the position of the Fermi level with respect to the trap energy. It is the *energy level position in the band gap* which is responsible for the variability of the noise PSD induced by defects in the *FD silicon film or fin*. Additional GR noise variability can be induced by device-to-device variations in the threshold voltage, as this will equally modify the quasi-Fermi level with respect to the trap level for the same operation voltages.

A third consequence specific to 1T FBRAM devices

on UTBOX SOI substrates is that there is a correlation between the retention time and the PSD. [12]. The retention time is in this case defined by the degradation of the '0'-state by hole generation through defects in the silicon film or at the interface (Gate-Induced Drain Leakage) [13,14]. It indicates that LF noise is also a useful tool for the study of the hole generation centers responsible for the degradation of the 0-state in these 1-transistor memories. Finally, it is shown that the application of the model to bulk FinFET devices is straightforward. ◀

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[www.nandk.com](http://www.nandk.com)

VAT

**VAT REAL L-MOTION Valve for SEMI and LED**

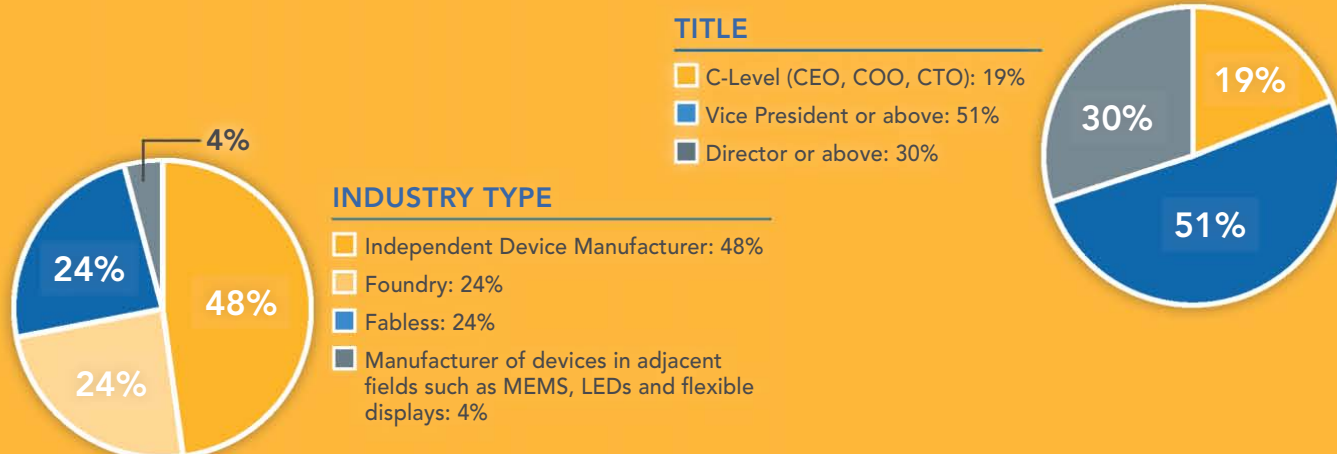
Designed to achieve uniform sealing compression and minimal particle generation, VAT's Real L-Motion valves meet the demands of SEMI applications handling 200mm, 300mm and 450mm wafers AND high brightness LED (HB-LED) applications.

[www.vatvalve.com](http://www.vatvalve.com)



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# New Products

## E-beam inspection system

KLA-Tencor Corp. announced the eS805, a new electron-beam inspection system capable of detecting very small defects, and defects that cause electrical problems



such as opens, shorts or reliability issues. The eS805 is also designed to provide supplementary information to the fab's optical inspection systems, with the goal of boosting the ability of the optical inspectors to preferentially capture defects that matter. **KLA-Tencor**, Milpitas, CA, [www.kla-tencor.com](http://www.kla-tencor.com).

## 1/f noise measurement system

ProPlus Design Solutions, Inc., announced it is shipping a new wafer-level, 1/f noise measurement system designed to measure low-frequency noise characteristics of on-wafer or packaged semiconductor devices, including MOSFETs, bipolar junction transistors (BJTs), junction field effect transistors (JFETs), diodes and diffusion resistors. In addition to frequency domain measurement, 9812D can measure device noise in the time domain and can be used to perform on-wafer auto measurement for flicker (1/f) noise and Radom Telegraph Signal (RTS) analyses. **ProPlus Design Solutions, Inc.**, San Jose, CA, [www.proplussolutions.com](http://www.proplussolutions.com).

## Deep UV excimer laser mirrors

Newport Corp. introduced long-lived deep ultraviolet (UV) excimer laser mirrors with projected lifetimes greater than 30 billion pulses when used in the proper photocontamination controlled environment. The advanced new mirrors feature all dielectric high reflector coatings to minimize absorption and maximize

reflected energy at 193nm.

The high energy laser mirrors are designed with excimer-grade UV-fused silica substrates which are polished to better than  $\lambda/10$  flatness to preserve wavefront quality and maintain excellent stability. All coating and testing are done in a special photocontamination controlled deep UV cleanroom that has been qualified to 193nm standards. The company says that the new laser mirrors offer exceptionally high laser damage resistance. Special Pet-G and metal foil packaging ensure that parts are delivered clean and protected from any environmental photocontamination. **Newport Corp.**, Irvine, CA, [www.newport.com](http://www.newport.com).



## Virtuoso Advanced Node EDA

Virtuoso Advanced Node is a new set of custom/analog capabilities designed for the advanced technology nodes of 20nm and below. Built on the Cadence Virtuoso custom/analog technology, Virtuoso Advanced Node features capabilities that prevent errors before they are created rather than detect them late in the design process. Working in concert with Cadence Encounter RTL-to-GDSII flow, QRC Extraction and Physical Verification System, Virtuoso Advanced Node enables the development of mixed-signal chips that power today's consumer electronics devices.

The new and advanced Virtuoso technologies address layout-dependent effects (LDEs), double patterning, color-aware layout and new routing layers. They integrate with the Cadence Integrated Physical Verification System (IPVS) to conduct on-the-fly checks that reduce layout iterations. **Cadence Design Systems, Inc.**, San Jose, CA, [www.cadence.com](http://www.cadence.com).

# What ideas will you COLLABORATE on?

Sessions at The ConFab 2013 will include:

- Market Outlook: Innovation, Specialization and Performance Drives Semiconductors
- Update on 450mm Wafer Transition from G450C
- 3D Integration and Advanced Packaging: Technical Sponsor IEEE CPMT
- CMOS and Beyond: The Next Transistor
- What's Making it Happen from the Inside (Teardowns to the Atomic Scale)
- The Fabless/Foundry Supply Chain
- Accelerating Manufacturing Productivity: In partnership with ISMI
- And more!

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"The ConFab 2013 will delve into the changing demand for semiconductor devices that will fill fabs in the near future. This demand increasingly depends on mobile devices, the fastest growing market segment. CEOs, fab managers and suppliers must plan now for devices that will go into production in the next few years. Foundries, in particular, face the challenge of confidently supplying specs for designs that will be produced at next-generation technology nodes." *—Pete Singer, Conference Chair*

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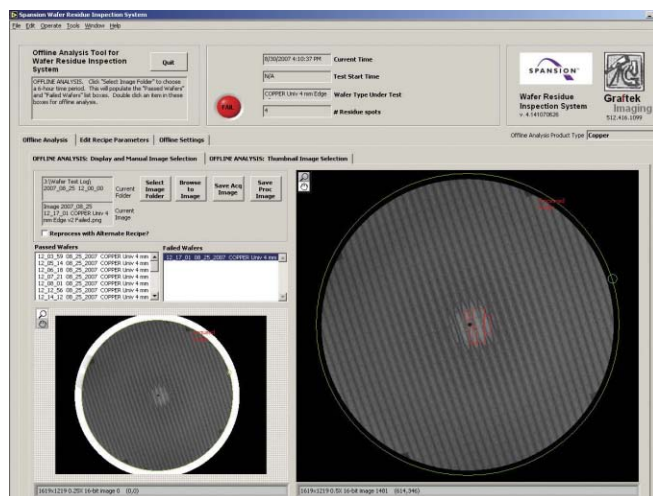
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## CMP

Continued from page 24



**FIGURE 5.** The RDS detected residual metal at the center of the wafer.

### Benefits all around

Improving manufacturing yields on silicon wafers and semiconductor devices is the foremost goal of every chip manufacturer. Improving yields will increase operating efficiencies and profitability. Although the CMP metal polishing process is only one segment of the entire fabrication process, it is particularly crucial in terms of cycle times and yields because it has been an intensely manual part of the overall process.

The development of a fully automated RDS inspection system to replace human inspectors who can be error prone and less than comprehensive is a game changer on several fronts. First, as a standalone inspection tool, it is fully automated. This means RDS has a robust and fast cycle time, which gives the system the ability to inspect every wafer as it emerges from the CMP polishing slurry. This 100 percent sampling rate is hugely beneficial to the manufacturer because a much higher percentage of residue is detected when compared to a manual inspection process which would likely involve a sampling rate that would be much less than 100 percent.

Second, because of the small footprint of the RDS system, it can be integrated into a CMP process tool and provide a means to continuously monitor the CMP process, providing an early detection scheme for residual metal left on wafers. The data output by RDS can allow for tight control of the CMP process within pre-defined reference limits and it can give insight into the development of more effective CMP processing procedures. ♦

## ad index

Advertiser	Pg
2013 IEEE 63rd ECTC .....	22
Coherent Inc. ....	5
Edwards .....	15
Lasertec Corporation .....	27
Materials Research Society .....	C2
N&K Technology Inc. ....	28
TDI Power .....	7
VAT Inc. ....	28

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## Managing process variations

Process variations are becoming one of the biggest challenges that both process development engineers and circuit designers must deal with in advanced process nodes. The increased random variations and layout-dependent effects inevitably and significantly impact the yield of a chip. Therefore, these process effects must be physically understood and accurately modeled up front in SPICE models that can be used later by the circuit designers during various circuit design stages, including simulation and verification.

To reduce risks for low-yield wafer manufacturing and design re-spins or even re-design, accurate yield prediction and realistic design optimization between performance and yield are urgently needed. The keys here are the accurate statistical models and useful design tools with high prediction accuracy and superior simulation performance.

Traditionally, engineers selectively run process, voltage and temperature (PVT) corner analysis and Monte Carlo analysis. Unfortunately, the process information given by the foundry models are sometimes either too conservative or too optimistic, and the foundry models may be used inappropriately or incorrectly on an application-specific basis.



**Dr. ZHIHONG LIU,**  
*Executive Chairman,  
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Compounding the problem are selective corner models and Monte Carlo analysis approaches often employed by circuit designers may give limited information, giving them low confidence on the yield prediction and design optimization. As a result, the overall design efforts may lead to loose conclusions. What's worse, the information and value given to circuit designers are, in fact, limited.

In another scenario, the variation model in the SPICE model library of a process design kit (PDK) is the only channel where designers can understand the complexity of variations and its relation to design. Its accuracy, completeness and quality can impact the final simulation and analysis results and confidence level. Having good model knowledge and properly using and applying it in the design flow offers increasing value, not to mention that improper usage of models may lead to deviated results.

Since the lack of integration can lead to a loose integration to simulators, one remedy would be to enhance the link between design and manufac-

The design community  
and foundries need to  
work more collaboratively

turing by integrating modeling, simulation and statistical analysis software tools. A set of elements for yield analysis can make the yield analysis more reliable and realistic.

There are three key components for handling process variations for circuit designs, i.e., accurate SPICE models considering process variations, a fast and reliable statistical simulation engine and hardware-validated sampling technologies. Performance can be improved and the license cost can be reduced immediately with an integrated SPICE engine instead of using an external engine. Having none of those components can lead to a loss in accuracy and degradation in simulation performance as well.

An integrated flow could enable designers to better use foundry corner models or help them re-generate corners, representative of the applications to improve efficiency and confidence levels for PVT analysis. Another analysis tool needed for yield prediction is Monte Carlo, which requires good statistical models. An integrated SPICE engine and hardware validated sampling technologies help designers here as well because they make the DFY more practical and faster, yet accurate because SPICE accuracy is preserved and sampling technologies are validated.

Managing process variations is something the semiconductor industry needs to pay more attention to, while the design community and foundries need to work more collaboratively to expand on the foundry-fabless model. The answer could come by more closely linking design and manufacturing with a rich software suite of SPICE modeling, circuit simulation and statistical analysis tools. ◀

# What new opportunities will you **CREATE** after The ConFab?

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