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Insights for Electronics Manufacturing

Reducing Polymer Defects in Metal

P. 12

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Solid State TECHNOLOGY

MARCH 2014 VOL. 57 NO. 2

On the bonnie banks: An aerial view of TI's Greenock, Scotland facility, the work home to the authors of this month's cover story.

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Web Exclusives

The need for high sigma yield

Dr. Bruce McGaughy, Chief Technology Officer and Senior Vice President of Engineering, ProPlus Design Solutions, Inc., says the move to state-of-the-art 28nm/20nm planar CMOS and 16nm FinFET technologies present greater challenges to yield than any previous generation.

http://bit.ly/1hjln7H

The most expensive SRAM in the world – 2.0

ISSCC 2014 illuminated the impeding problem – embedded SRAM scaling. Embedded SRAM scaling is broken and, with it, Moore's Law. Zvi Or-Bach, President and CEO of MonolithIC, and Ben Louie, Zeno Semiconductors share insights from ISSCC 2014.

http://bit.ly/1dSDmBH

Experts at the Table: Commercial potential and production challenges for 3D NAND memory technology

The last six months have seen several developments concerning 3D memory concepts moving into production, from companies such as Samsung, Micron, Toshiba and Sandisk. What follows are excerpts from a roundtable discussion with SemiMD, Samsung Electronics (SE) in South Korea, which has begun production of its proprietary 3D NAND technology, Bradley Howard, Vice President of Advanced Technology Group, Etch Business Unit, at Applied Materials and Jim Handy from Objective Analysis, which specializes in coverage of the memory industry. From SemiMD

http://bit.ly/J2FZUR

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http://bcove.me/fnppomc7

n&b news and blogs

Insights from the Leading Edge

Dr. Phil Garrou finishes up his look at the IEEE 3DIC meeting with a review of presentations by Tohoku University, Fujistu, ASE and RTI.

http://bit.ly/1k60iOG

If you fear change, ECO fill can help

Jeff Wilson of Mentor Graphics describes how an effective ECO fill strategy must be accurate and fast, concentrating only on the portion of the design affected by the ECO. By removing and replacing only the fill in that area, and re-verifying timing only in the affected area, we can reduce runtime, manage file size, and minimize timing impacts. By restricting the ECO fill operation to only the same locations where actual mask-making changes occur, we can limit the size of the region that must be evaluated for errors, edited, and refilled.

http://bit.ly/1ne56Dq

Is the chip industry as important as we think? Depends on whom you ask

Vivek Bakshi asks the question: "Are we as leading-edge industry making a difference in the world?"

http://bit.ly/1dtqBZH

Exploring the MEMS-enabled life

Munich, Germany is one of Karen Lightman's favorite cities in the world. If you agree or if you've never been there, she has the perfect opportunity for you to join her: MEMS Industry Group's (MIG's) MEMS Executive Congress Europe 2014 will be held at the beautiful Sofitel Hotel Bayerpost on March 10-11.

http://bit.ly/1ewpCs7

editorial

Mission accomplished. Now what?

In the late '80s and '90s, when our magazine staff gathered for dinner we often made a toast: "Here's to chip silicon!" I really believed (and still do) that making electronics more affordable would increase their use and make our lives better and the world a better place to be.

I haven't toasted to cheap silicon for a while. Why? Because that mission has been accomplished.

> I haven't toasted to cheap silicon for a while. Why? Because that mission has been accomplished.

At SEMI's ISS, Paul Farrar, manager of the G450C consortium put the industry progress over the last 40+ years in perspective. "1 Megabyte of memory in 1970 was $750,000. It was sold as an IBM add-on," he said. "The great technology was made of 57mm wafers, five masking levels, and one level of metal. Today, it's is less than a penny. That is a 100 million X improvement."

Of course, most people would like to see this trend continue, but it's highly unlikely that we'll see such dramatic progress. Scaling is getting too expensive. The transition to 450mm looks feasible from a technical standpoint (see my column on pg. 10) but it's not yet clear if it will be less expensive than 300mm, particularly when you factor in 450mm lithography.

So if the scaling mission is accomplished, what's next? There's exploding interest in the "Internet of Things" where almost everything is tagged and connected. That will require some big upgrades in the server/network infrastructure, but that can be done with existing technology. It will also require inexpensive sensors and wireless communication. By some estimates, the technology to achieve that is not ready. We need about a 10X improvement in price/performance. Ditto for wearable electronics and a whole host of applications in medical, automotive and the smart grid.

In the future, perhaps electronics will be printed like potato chip bags on roll-to-roll machines with ink-jet-like deposition of materials. Perhaps tiny MEMS with integrated sensors, thin-film batteries, energy harvesting, microprocessors and other functions will be produced for less than a penny. Perhaps everyone will have inexpensive body area networks embedded in their clothing that constantly monitor their health.

It's all possible, but it will take some innovation in processing equipment and materials.

—Pete Singer, Editor-in-Chief

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EUROPE | **GLOBALFOUNDRIES** and **Fraunhofer Institute for Integrated Circuits IIS** announced the extension of their long-term collaboration, focusing on 40nm and 28nm processes. **GLOBALFOUNDRIES** will also join the European Multi Product Wafer Program **EUROPRACTICE**.

USA | **MACOM** acquired Nitronex, LLC.

ASIA | **SPTS Technologies** announced the opening of a new office in Panyo, Korea.

USA | **Soraa** announced the world's most efficient LEDs, using third generation GaN-on-GaN LEDs.

ASIA | **International Rectifier** opened a new ultra-thin wafer processing facility in Singapore.

USA | **Epoxy Technology, Inc.** and **John P. Kummer Group**, a distributor of instruments and materials for the microelectronics and related industries, announce the formation of a new specialty adhesive packaging company, **Epoxy Technology Europe Ltd**.

EUROPE | **PLACYD**, an EU funded consortium of industrial and academic collaborators and led by **Arkema** will establish a dedicated material manufacturing facility that allows the production of block copolymers meeting the rigorous standards required for their use in industry as nanolithographic templates. Partners include: **CEA-Leti, STMicroelectronics, Intel IPLS, Mentor Graphics, ASML** and other leading EU companies and research organizations.

IBM continues to evolve: Semiconductor business up for sale; moving into the cloud

The Financial Times (FT) is reporting that IBM Corp is exploring the sale of its semiconductor business and has hired Goldman Sachs to find potential buyers. The FT report continues that another financial option may be to find a partner for a JV to jointly run its semiconductor business.

FT projects that the most likely buyers would be Global Foundries or TSMC since it is likely that these two foundry giants along with Samsung and Intel will be the only players left in advanced chip manufacturing as the cost of 20nm and lower fabs now exceeds $6B.

This should not come as a shock to readers of SST's IFTLE blog (Insights From the Leading Edge) which reported early rumors of such a sale back in the summer of 2010.

While the semiconductor business has become an increasingly less important part of IBM's operations in recent years as it has expanded in IT software and services, any sale or joint venture would surely have to ensure that IBM still had a guaranteed supply of the advanced chips required for its mainframe and high end server businesses.

GlobalFoundries is the most likely candidate for sale or JV since they are a member of the IBM common platform, have been working with IBM for over a decade and have placed their latest fab (Fab 8) in IBMs back yard in upstate NY.

This report comes two weeks after the announcement that, pending government approval, IBM will sell its low-end server business for $2.3 billion to Chinese PC maker Lenovo. Some may recall that a decade ago Lenovo bought IBM's ThinkPad PC business for $1.75B.

This low end server decision was likely driven by the trend for many major corporations to move their IT requirements to "the cloud" with companies such as Amazon web services. With customers having more choices for handling their IT, they will be reluctant to get locked into client-server service contracts with IBM.

In fact IBM has just announced [link] plans to commit over $1.2B to significantly expand its global cloud footprint. IBM plans to deliver cloud services from 40 data centers worldwide in 15 countries and five continents globally, including North America, South America, Europe, Asia and Australia. IBM will open 15 new centers worldwide adding to the existing global footprint of 13 global data centers from SoftLayer, which it acquired in July of 2013, and 12 from IBM. ◆

By Dr. Phil Garrou, Contributing Editor

Entegris to acquire ATMI

In a merger that will bring together two key suppliers in the semiconductor industry, Entegris, Inc. and ATMI today announced Entegris will acquire ATMI for approximately $1.15 billion, or approximately $850 million net of cash acquired, including the net cash proceeds from the sale of ATMI's LifeSciences business of $170 million. The companies anticipate closing the transaction in the second quarter of 2014.

"Upon closing, approximately 80 percent of our product sales will be unit-driven and focused on the most rapidly growing and critical areas of the semiconductor fab," said Bertrand Loy, President and CEO of Entegris. "We are excited about the opportunities ahead and look forward to quickly realizing the significant benefits of this transaction for our shareholders, customers and employees."

"Throughout this process, our goal has been to enter into a transaction that not only maximizes shareholder value, but also places our business with the right partner for our valued customers and employees," said Doug Neugold, President and CEO of ATMI. "We are pleased to merge our microelectronics business into Entegris. Entegris' global platform and complementary products represents a great opportunity for ATMI stakeholders, including our shareholders, who will receive an immediate premium for their investment."

ATMI shareholders will receive $34.00 in cash, without interest or dividends, for each share of ATMI common stock they hold at the time of closing. The price represents a premium of 26.3 percent to ATMI's closing price of $26.93 on February 3, 2014. Entegris expects to fund the all-cash transaction with a combination of existing cash balances and additional committed debt financing.

Goldman, Sachs & Co. is serving as the exclusive financial advisor, and Ropes & Gray LLP is serving as legal counsel to Entegris. Barclays Capital is serving as the financial advisor and Weil, Gotshal & Manges LLP is serving as legal counsel to ATMI. Goldman Sachs Bank USA has been appointed to act as the lead arranger and bookrunner for the committed financing that has been obtained by Entegris in connection with the merger and the related transactions.

North Carolina State University to lead research consortium on power electronics

The Obama Administration announced the selection of North Carolina State University to lead a public-private manufacturing innovation institute for next generation power electronics. Called the Next Generation Power Electronics Institute, the new consortium will provide shared facilities, equipment and testing to companies from the power electronics industry, focusing on small and medium-sized companies. The 18 companies already committed to the consortium include: ABB, APEI, Avogy, Cree, Delphi, Delta Products, DfR Solutions, Gridbridge, Hesse Mechantronics, II-VI, IQE, John Deere, Monolith Semiconductor, RF Micro Devices, Toshiba International, Transphorm, USCi and Vacon.

The institute, backed by a $70 million investment from the Department of Energy, will focus on power electronics using wide bandgap (WBG) semiconductors, bringing together over 25 companies, universities and state and federal organizations.

This $140 million manufacturing hub in Raleigh has the potential to fast-forward development of some products by at least a decade," said Greg Scheu, president and CEO of ABB Inc., a Raleigh-based power electronics manufacturer. "We expect that consumers will start to see some low-voltage products, like residential solar, coming out the quickest and within five years. The high-power products like industrial motors and drives and hog-voltage gear will take a few more years to come to market, mainly due to the rigorous reliability testing requirements of the electric utility industry."

Power electronics – such as inverters, transformers and transistors – help control and convert electricity and are playing a growing role in electricity generation, distribution and transmission. According to a study by the Oak Ridge National Laboratory, approximately 30 percent of all power generation today utilizes power electronics between the point of generation and its end use. By 2030, this is expected to jump to 80 percent of generated electricity – supporting greater renewable energy integration and increased grid reliability. WBG semiconductor-based power electronics will be able to better withstand the power loads and switching frequencies required by next generation utility technologies.

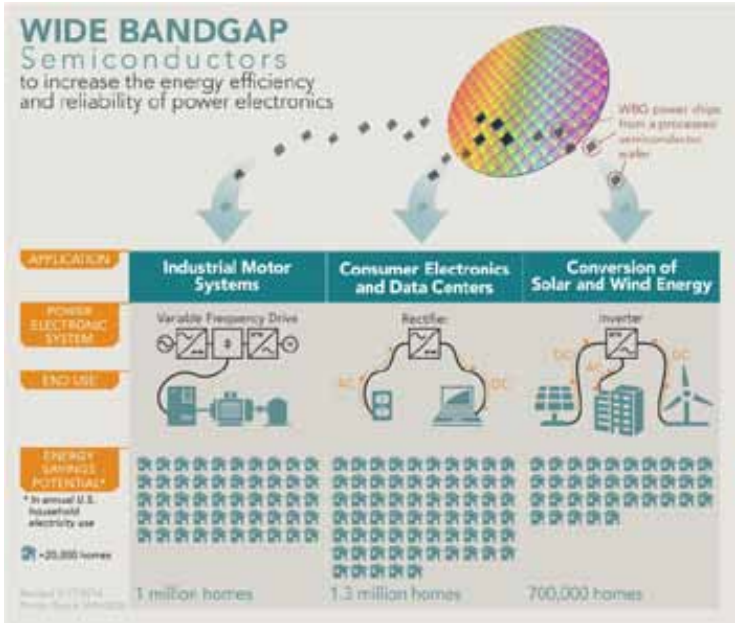
Power electronics that use WBG semiconductors will also be smaller, more efficient and cost less. A WBG semiconductor-based inverter, which switches electricity from direct current to alternating current, could be four times more powerful, half the cost and one-fourth the size and weight of a traditional inverter. At a larger-scale, WBG semiconductors could help reduce the size of an 8,000 lbs. substation to 100 lbs. and the size of a suitcase – ultimately helping to lower the cost of electricity and build a stronger, more reliable grid.

WBG semiconductors such as silicon carbide and gallium nitride can operate at higher temperatures and have greater durability and reliability at higher voltages and frequencies.

The state of North Carolina is expected to contribute at least $10 million to the new consortium, which is expected to help bolster employment in North Carolina, as well as to help focus on manufacturing as a potential source of economic growth.

According to the official statement from the Obama administration, The Next Generation Power Electronics Institute supports President Obama's vision for a full national network of up to 45 manufacturing innovation institutes that help make America a magnet for jobs and manufacturing and ensure that U.S. workers have the training they need to lead in the global economy.

"I see it this way," said Mr. Scheu, "the president asked the industry to work together and see where we can replace silicon with other semiconductor materials to reduce energy loss — meaning huge energy efficiency — for equipment that can handle higher voltages, higher temperatures and higher frequencies. To me, this is the goal. And this is where the imagination takes off."



SRC and MIT extend high-resolution lithography capabilities

MIT researchers sponsored by Semiconductor Research Corporation have introduced new directed self-assembly (DSA) techniques that promise to help semiconductor manufacturers develop more advanced and less expensive components.

The MIT study demonstrates that complex patterns of lines, bends and junctions with feature sizes below 20nm can be made by block copolymer self-assembly guided by a greatly simplified template. This study explained how to design the template to achieve a desired pattern.

Electron-beam lithography was used to produce the template serially, while the block copolymer filled in the rest of the pattern in a parallel process. This hybrid process can be five or more times faster than writing the entire pattern by electron beam lithography.

"We believe our research will help Moore's Law to be continued," said Caroline Ross, MIT professor of Materials Science and Engineering. "To increase the density of transistors in a given area, the pitch of the features in a transistor should be scaled down, but the increasing time and cost of manufacturing such fine and dense features becomes more problematic. Our research suggests a solution to this problem."

Leveraging block copolymer self-assembly to produce dense, high-resolution patterns was proposed and demonstrated several years ago, but there was no systematic way to design templates to achieve a complex block copolymer pattern. The MIT study developed a simple way to design a template to achieve a specific block copolymer pattern over a large area. Although the work used electron-beam lithography to define the template, other methods such as photolithography with trimming could be used to produce the templates.

Block copolymer lithography is already on the semiconductor industry roadmap as directed self-assembly, but the process is still in its infancy. Although DSA patterning has been demonstrated on 300mm wafers, these early trials used templates fabricated by photolithography with limited resolution and limited control of the feature geometry. The MIT process offers a path to far more complicated geometries using relatively simple templates. Next steps involve the research being shared with semiconductor companies for further studies.

"The demand for computing processors with higher bandwidth and memories of larger capacity continues to grow, but the manufacturing cost of these devices is also increasing as the transistor and associated interconnect dimensions shrink," said Bob Havemann, Director of Nanomanufacturing Sciences at SRC. "Lithography research such as the work completed by the MIT team is critically important as the required feature sizes in semiconductor manufacturing scale below what is achievable with conventional lithography techniques."

Silicon-germanium chip sets new speed record

A research collaboration consisting of IHP-Innovations for High Performance Microelectronics in Germany and the Georgia Institute of Technology has demonstrated the world's fastest silicon-based device to date. The investigators operated a silicon-germanium (SiGe) transistor at 798 gigahertz (GHz) fMAX, exceeding the previous speed record for silicon-germanium chips by about 200 GHz.

Although these operating speeds were achieved at extremely cold temperatures, the research suggests that record speeds at room temperature aren't far off, said professor John D. Cressler, who led the research for Georgia Tech. Information about the research was published in February of 2014, by IEEE Electron Device Letters.

"The transistor we tested was a conservative design, and the results indicate that there is significant potential to achieve similar speeds at room temperature – which would enable potentially world changing progress in high data rate wireless and wired communications, as well as signal processing, imaging, sensing and radar applications," said Cressler, who hold the Schlumberger Chair in electronics in the Georgia Tech School of Electrical and Computer Engineering. "Moreover, I believe that these results also indicate that the goal of breaking the so called 'terahertz barrier' – meaning, achieving terahertz speeds in a robust and manufacturable silicon-germanium transistor – is within reach."

Meanwhile, Cressler added, the tested transistor itself could be practical as is for certain cold-temperature applications. In particular, it could be used in its present form for demanding electronics applications in outer space, where temperatures can be extremely low.

IHP, a research center funded by the German government, designed and fabricated the device, a heterojunction bipolar transistor (HBT) made from a nanoscale SiGe alloy embedded within a silicon transistor. Cressler and his Georgia Tech team, including graduate students Partha S. Chakraborty, Adilson Cordoso and Brian R. Wier, performed the exacting work of analyzing, testing and evaluating the novel transistor. "The record low temperature results show the potential for further increasing the transistor speed toward terahertz (THz) at room temperature. This could help enable applications of Si-based technologies in areas in which compound semiconductor technologies are dominant today. At IHP, B. Heinemann, H. Rücker, and A. Fox supported by the whole technology team working to develop the next THz transistor generation," according to Bernd Tillack, who is leading the technology department at IHP in Frankfurt (Oder), Germany.

Silicon, a material used in the manufacture of most modern microchips, is not competitive with other materials when it comes to the extremely high performance levels needed for certain types of emerging wireless and wired communications, signal processing, radar and other applications. Certain highly specialized and costly materials – such as indium phosphide, gallium arsenide and gallium nitride – presently dominate these highly demanding application areas.

But silicon-germanium changes this situation. In SiGe technology, small amounts of germanium are introduced into silicon wafers at the atomic scale during the standard manufacturing process, boosting performance substantially.

The result is cutting-edge silicon germanium devices such as the IHP Microelectronics 800 GHz transistor. Such designs combine SiGe's extremely high performance with silicon's traditional advantages – low cost, high yield, smaller size and high levels of integration and manufacturability – making silicon with added germanium highly competitive with the other materials.

Cressler and his team demonstrated the 800 GHz transistor speed at 4.3 Kelvins (452 degrees below zero, Fahrenheit). This transistor has a breakdown voltage of 1.7 V, a value which is adequate for most intended applications.

The 800 GHz transistor was manufactured using IHP's 130-nanometer BiCMOS process, which has a cost advantage compared with today's highly-scaled CMOS technologies. This 130 nm SiGe BiCMOS process is offered by IHP in a multi-project wafer foundry service.

The Georgia Tech team used liquid helium to achieve the extremely low cryogenic temperatures of 4.3 Kelvins in achieving the observed 798 GHz speeds.

"When we tested the IHP 800 GHz transistor at room temperature during our evaluation, it operated at 417 GHz," Cressler said. "At that speed, it's already faster than 98 percent of all the transistors available right now." ◆

Global semiconductor industry posts highest-ever January sales

The Semiconductor Industry Association announced that worldwide sales of semiconductors reached $26.28 billion for the month of January 2014, an increase of 8.8 percent from January 2013 when

sales were $24.15 billion, marking the industry's highest-ever January sales total and the largest year-to-year increase in nearly three years. Global sales from January 2014 were 1.4 percent lower than the December 2013 total of $26.65 billion, reflecting normal seasonal trends. Regionally, sales in the Americas increased by 17.3 percent compared to last January. All monthly sales numbers are compiled by the World Semiconductor Trade Statistics (WSTS) organization and represent a three-month moving average.

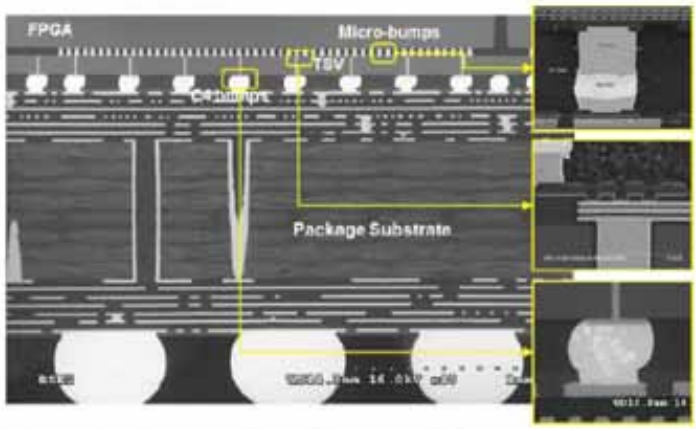
"The global semiconductor industry has built on its record revenues from 2013 with an impressive start to 2014, led largely by continued strength in the Americas market," said Brian Toohey, president and CEO, Semiconductor Industry Association. "Sales in January were up across most regions and nearly all product categories compared to last January, which bodes well for continued growth during the rest of 2014."

Regionally, year-over-year sales increased in the Americas (17.3 percent), Europe (11.3 percent), and Asia Pacific (8.3 percent), but decreased in Japan (-4.7 percent). Sales were flat in Europe compared to the previous month, but decreased slightly in Asia Pacific (-0.6 percent), Japan (-2.3 percent), and the Americas (-3.5 percent). January sales historically are lower than December sales due to seasonal trends.

IMAPS wrap-up

Dr. Phil Garrou,
Contributing Editor

Last summer, at The ConFab, Siliconware (SPIL) announced the instillation of a dual damascene line for fabrication of high density interposers. At the fall IMAPS meeting, Xilinx and SPIL shared results from their 2.5D 28nm FPGA program.



THE SPIL/XILINX 2.5D 28NM FPGA

The high performance FPGA die (manufactured by TSMC) is a 4 slice 28nm chip mounted on a 25 x 31mm 100µm thick Si interposer with 45um pitch microbumps. The interposer is assembled onto a 45 x 45mm organic BGA with 180µm C4 bumps. The figure above shows the structure in cross section. SPIL is manufacturing the interposer and doing the assembly.

SPIL is the first OSAT to propose an OSAT centric model where the interposer is fabricated by the OSAT who then assembles and tests modules made with chips from multiple sources. The impediment to this route in the past has been the lack of OSAT capability to fabricate the fine pitch interposers, which require dual damascene processing capability, which until now was only available in the foundries. SPIL has now announced the equipment for fine pitch interposer capability (>2 layers, 0.4-3µm metal line width and 0.5µm TSV) has been purchased and is in place.

Nanyang University and IME also presented at IMAPS. They reported how copper TSVs exert thermo-mechanical stress on silicon due to the CTE mismatch. This stress can result in variability of the device mobility and mechanical reliability issues. This can be alleviated by using an oxide liner that has a lower elastic modulus such as some of the "low-k" dielectric materials (e.g., Black Diamond). This would reduce the keep out zone and in addition such materials will lower the parasitic capacitance of the circuit.

These Singapore institutions looked at the use of low-k carbon doped oxides to serve as a more compliant layer TSV insulator layer due to its lower modulus (7.2 GPa vs plasma enhanced TEOS with modulus of 75GPa) . The FEA analysis shown below indicates that the low-K materials "should" lower the stress exerted by the Cu TSV on the silicon. Micro raman spectroscopy on samples verifies that the use of a low-k liner results in less compressive stress exerted by the Cu TSV on the silicon between the TSV.

As a side note, I saw no discussion of mechanical reliability comparisons. Since low-k is known for being very fragile, I wonder whether the TSV stress will fracture the low-k material which would show up as less stress on the silicon?

Also at IMAPS, Canon, normally associated with front end (FE) lithography addressed "Lithography Process Optimization for 3D and 2.5D Applications." Canon has developed the FPA-5510iV and FPA-5510iZ TSA steppers to support high density processes and to support implementation of 2.5 & 3D technology.

In a typical backside manufacturing process, patterned wafers are bonded face down to a support wafer before being ground and thinned. The bonding and thinning process causes shape distortion in the wafer. Downstream processes require lithography that produces patterns that can overlay such distortions with high accuracy. These systems also employ vacuum assist functions to compensate for large wafer warpage.

Packaging

No technical barriers seen for 450mm

Pete Singer,
Editor-in-Chief

Paul Farrar, general manager of the G450C consortium, said early work has demonstrated good results and that he sees no real barriers to implementing 450mm wafers from a technical standpoint. Speaking at the SEMI ISS meeting in January, Farrar showed impressive results from, etch, CVD, PVD, CMP, furnaces, electroplating, wet cleans and lithography processes and said the inspection/metrology tools were in place to measure results. "I don't believe we will find fundamental technology limiters," he said. "But we will have to keep working to find ways to maximize the efficiency." Gaining such efficiencies are critical in order to meet the cost-saving goals of the program. "In the end, if this isn't cheaper, no one is going to do it," he said.

G450C is a consortium based at the CNSE campus in Albany, NY. It is financed by Intel, TSMC, Samsung, IBM, GLOBALFOUNDRIES, and New York State (CNSE). "Our job is to make it as easy as possible to innovation and be collaborative between the semiconductor makers and our key friends in the industry who enable the 450 work to be done in an economic way," Farrar said.

At the end of 2013, G450C at 34 tools delivered to its 50,000ft2 fab in Albany, with another 7 tools in place at partner's facilities. "The FOUPS are going, the overhead transport is well underway and some of the cleanroom is actually starting to look like a cleanroom," Farrar said.

Farrar started with etch results, saying they were "starting to see some pretty good data – 3 sigma at about 2%. Yes, there's still some work to get to the very edge of the wafer but relatively good progress and good jobs on gas delivery, etc.

He showed good results with both oxide and silicon nitride CVD, with close to 1.5mm edge exclusion. "It's very representation data from early in the program," Farrar said, noting that they were starting to pattern some of the more complex oxides.

He said the goal for PVD was to demonstrate better than 5% uniformity. "We know we have step coverage challenges for both the 10 and 7nm nodes. There's tremendous work going on in the injection rings for gases, high density plasmas from multiple RF sources, but again some progress to me made but pretty good data for right out of the chute," he said.

CMP results demonstrated repeatability less than 4%. "Very good job done by our suppliers," Farrar said. Farrar described data from furnaces as reasonably good. "We still need to do more characterization at what I call the micro level," he said. "We see some hot spots on the edge, but we're starting to work on those." Also "pretty good data" from electrochemical plating (ECP) of copper. "Well done here," Farrar said. "The challenge is thermal and pattern loading effects, and gap fill."

More of the same with wet cleans. "We're starting to see some pretty good particle data. We're cleaning wafers relatively well. We are seeing a few things like what I would call micro-metallic contamination that can grow some things so we're still working on that. But from a particle removal standpoint, pretty good unit process work," Farrar said.

Farrar acknowledged that lithography remained as one of the biggest challenges in the 450mm transition, but showed good results from directed self assembly across a 450mm wafer, and said the consortium had a very strong partnership with Nikon. "We're working with them and we've seen some tremendous progress at their factory," he said. "I'm fully confident that we'll have capability by July to run patterned wafers. Immersion is going to be the workhorse. I think that's a key enabler to get to 450mm." He said the industry would have to see how the economics of EUV played out later in time. "I don't think it's going to be early in time," he said.

Semiconductors

Solutions for polymer defects at plasma metal etch

Equipment Engineers at Texas Instruments' GFAB facility in Greenock, Scotland have developed a method for polymer defect reduction in plasma metal etch systems that increases the preventive maintenance interval and correspondingly reduces associated PM costs.

ALLAN O'BRIEN *and* **ROBERT ADAMS**, *Texas Instruments, Greenock, Scotland*

The problem of polymer flaking on plasma metal etch systems in wafer fabs is a common long standing issue which impacts three key fab metrics: Fab Yield (PY), Tool Availability (Ao) and Cost of Ownership (CoO). With each occurrence of flaking, there is a risk of reduced PY losses due to short circuits caused by metal bridging. When defects are detected on product lots at post-process inspection at the tool, this induces unplanned maintenance interventions which have an associated Ao and CoO impact.

Our team focused on the equipment related causes for polymer flaking and monitored the performance of the equipment in running consistently between consecutive preventive maintenance (PM) events (sometimes known as PM hit rate) as a figure of merit. We took the view that there is a direct and proportional relationship between PM hit rate and PY, Ao and CoO. However, it is also worth noting that the extent of this problem is dependent not only on equipment-influencing factors but also on the processes for which the equipment is used. In this case a typical aluminum with titanium/tungsten barrier structure using a chlorinated chemistry for the aluminum etch and a fluorinated chemistry for the barrier etch. Some plasma metal etch equipment use periodic plasma cleaning in an attempt to minimize polymer flaking. However, this method needs to be tuned to a particular process regime and finding a "one size fits all" has in some cases been found limited in its success.

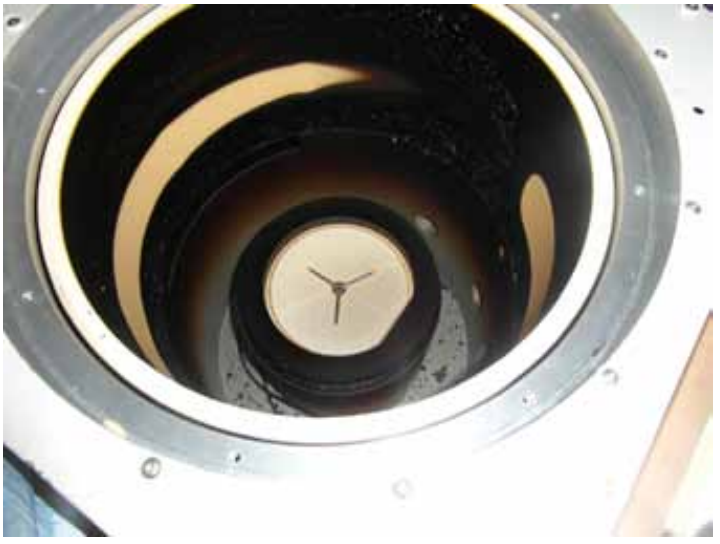


FIGURE 1. Typical chamber condition of a system which has failed for polymer defects detected on product post-processing.

FIGURE 1 shows the typical chamber condition of a system which has failed for polymer defects detected on product post-processing. The Ishikawa analysis (**FIGURE 2**) of possible equipment-related causes was generated to form an action plan to audit, correct and prevent these causes where applicable and possible.

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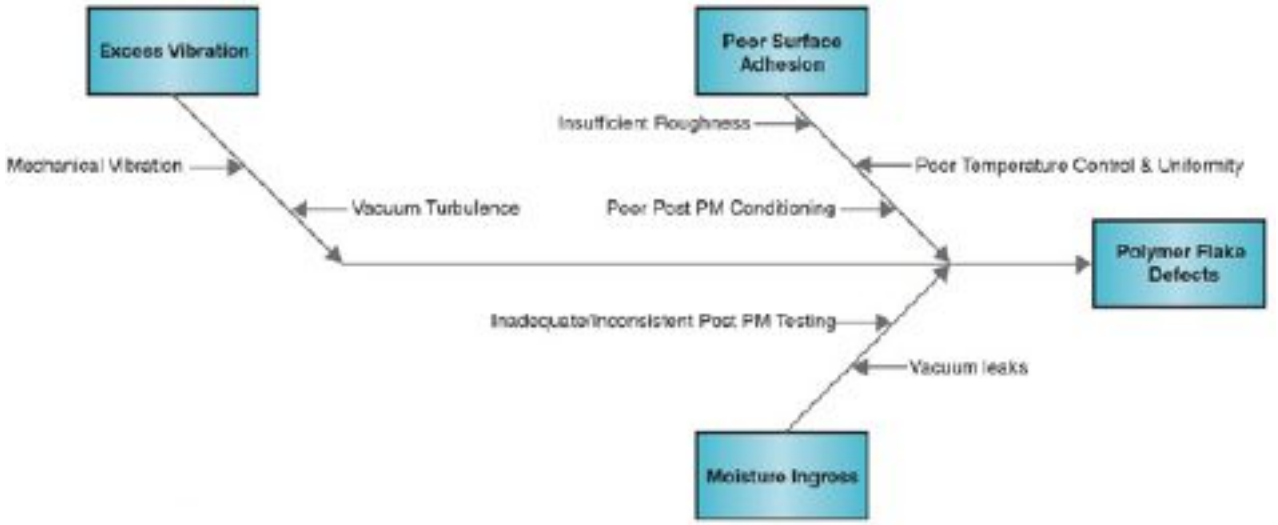

FIGURE 2. Ishikawa analysis.

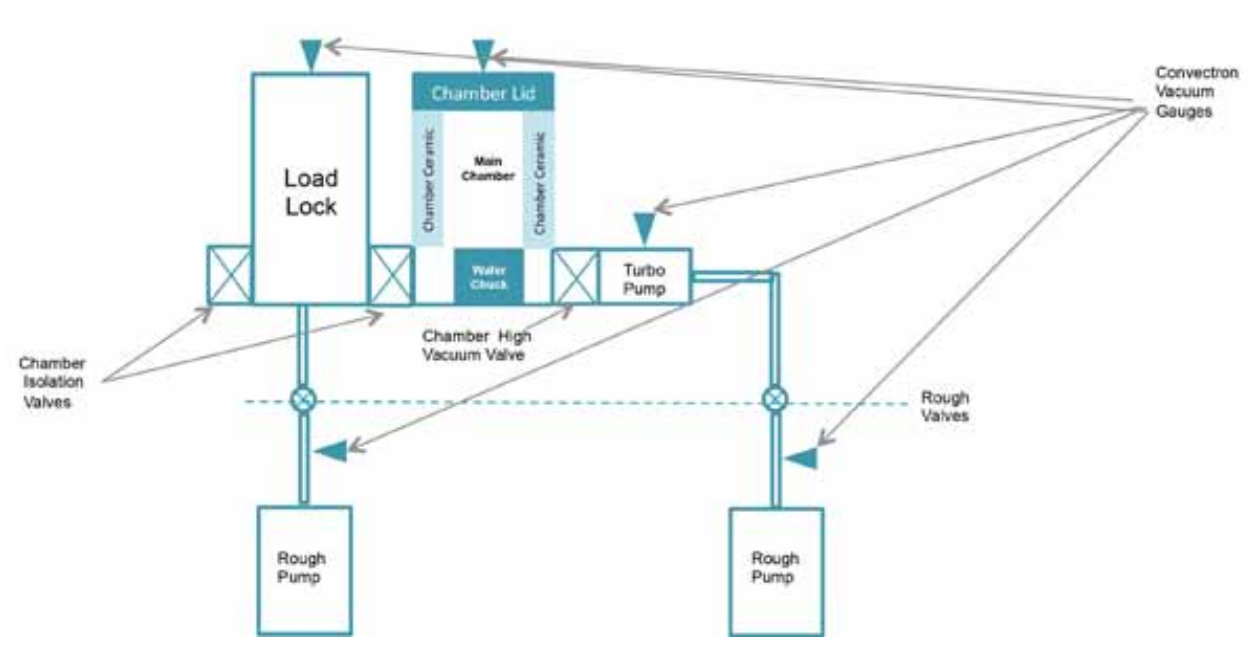

FIGURE 3. Vacuum schematic.

The analysis determined that there were three likely causes: poor surface adhesion, moisture ingress and excess vibration.

Poor surface adhesion

For poor surface adhesion, three sub-causes were considered, namely insufficient surface roughness (Ra), poor temperature control and poor post PM conditioning practices.

In the case of surface roughness, it was thought that insufficient surface roughness in the chamber surfaces, on which multiple films of process byproducts are deposited, would have a high likelihood of flaking. This is because the stress on these films, if developed across large areas, particularly when subjected to thermal cycles, would cause the films to crack and flake off. This is in contrast to a film whose stress is developed across multiple smaller areas and would have a lower likelihood of cracking and flaking. Chamber ceramics manufactured from aluminum oxide and the chamber lid manufactured from stainless steel were already being cleaned, baked and vacuum packaged by an external contractor. The Ra of these components was measured on the existing clean method and then an alumina bead blast was incorporated into the cleaning process to ascertain if this

Ra value could be improved. The results were encouraging in that the surface roughness of chamber parts could effectively be doubled. The chamber ceramic Ra improved from 1.5–2.5µm to 4-5µm and the chamber lid Ra improved from 3–4µm to 6-9µm.

On poor temperature control, plasma metal etch equipment systems typically maintain process chamber temperatures between 60 and 70°C using heater cartridges integrated into the chamber body. The emphasis in the study was to ensure the accuracy of this temperature control and more importantly the functionality of all heater cartridges to ensure the desired temperature is uniform across all chamber surfaces. This is to avoid temperature gradients which, when subjected to multiple temperature cycles, would expand and contract at different rates and possibly flake. The investigation uncovered one such open circuit chamber heater cartridge that could have been causing a cool spot.

Poor maintenance practices were also discovered. Specifically, when resist-coated conditioning wafers were ran by equipment technicians after the post-PM leak up rate test failed. This practice was flawed from the beginning, as in effect it trapped moisture between the chamber surfaces, resulting in poor polymer adhesion.

Moisture ingress

The three influencing factors supposed for moisture ingress were atmospheric exposure duration of the process chamber, vacuum leaks and inadequate/inconsistent post-PM testing.

In the case of atmospheric exposure duration, high variation was noted and was minimized by an update to PM specifications. This stipulates that process chambers should only be exposed to atmosphere when a dedicated technician is available to complete the PM and return the chamber under vacuum in the shortest possible time.

On vacuum leaks, historical assumptions that a leak up rate (or rise over base) check was an adequate measure of vacuum integrity. However, when a helium leakcheck was carried out, several small leaks were discovered on multiple tools. These were corrected and helium leak checking was incorporated into the specified PM procedure to prevent recurrence.

Furthermore, all tools run what is known as a post PM recipe that serves to pump down the chamber to a base pressure then backfill with nitrogen a fixed number of times (known as a pump/purge). This is followed by a leak up rate test. It was discovered that not all tools had the same recipe parameters. So a best known method (BKM) for these parameters was defined and specified.

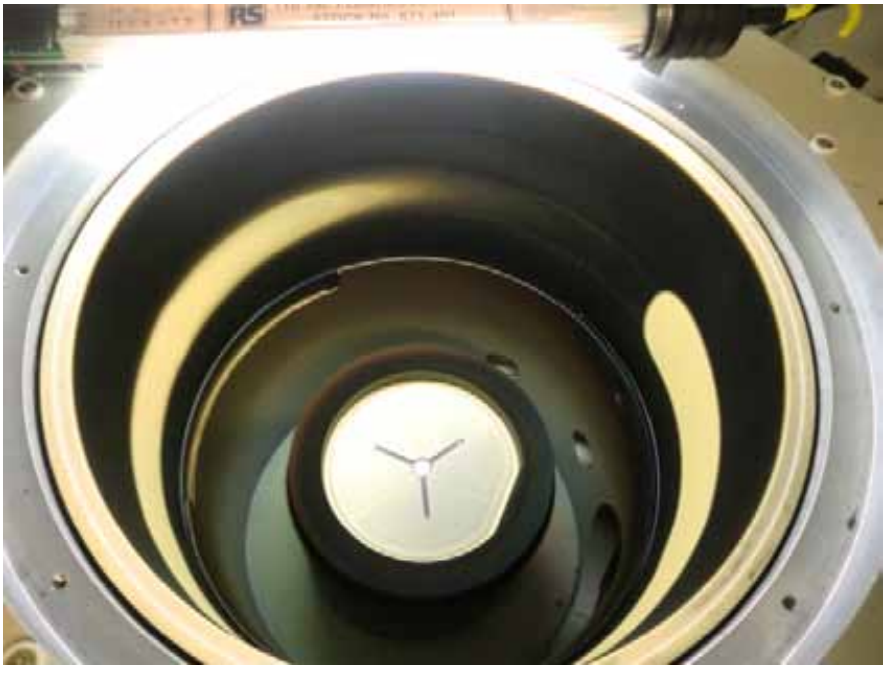

FIGURE 4. Beneficial results can be distinguished in chamber conditions where no discernable flaking is evident.

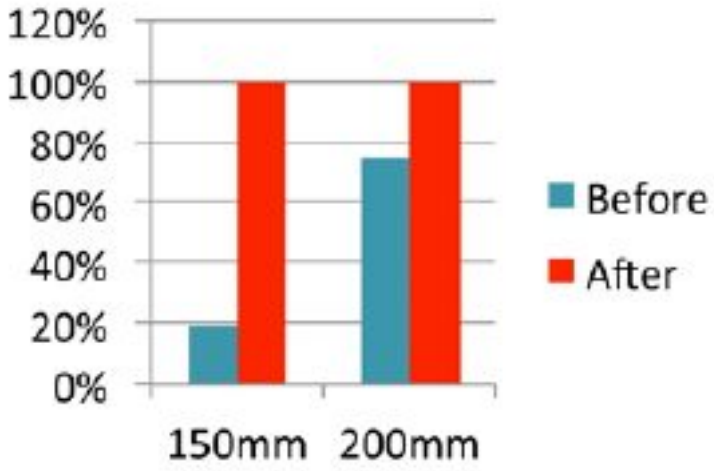

FIGURE 5. PM hit rate.

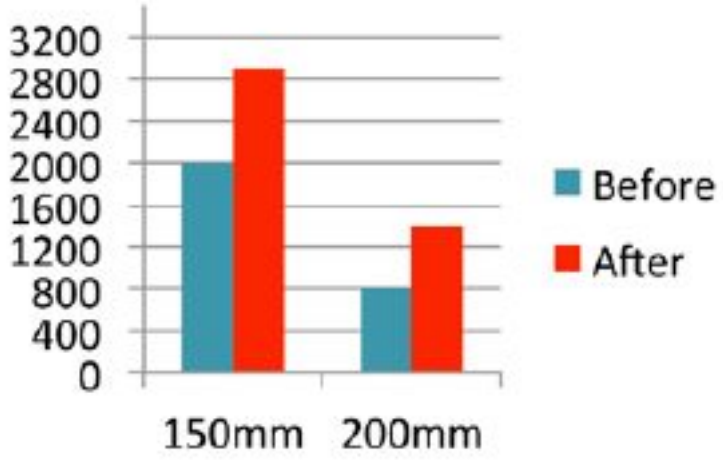

FIGURE 6. PM interval.

Excess vibration

Finally for excess vibration, the two root causes considered were mechanical vibration and vibration form vacuum turbulence.

The first root cause is mechanical vibration from assemblies within the tool that frequently actuate as part of normal operation. Upon further investigation, several tools were found to have high vacuum isolation valves (shown in **FIGURE 3**) with incorrectly adjusted or missing pneumatic dampers. This results in mechanical vibration which could dislodge polymer from the chamber surfaces.

Vacuum turbulence transpires when two isolated chambers are perceived by the tool to be at the same pressure but, in reality, are not. If the respective vacuum gauges (in this case convectron gauges again shown in Fig. 3) are not calibrated precisely, a degree of turbulence occurs when these chambers are exposed to each other until actual equilibrium is established. Similarly, when chambers are roughed down from atmosphere it is important to have a suitable low crossover pressure at which the chamber is exposed to a high vacuum pump. Typical crossover pressures range from 50mTorr to 200mTorr depending on the equipment in question.

Results and conclusion

As a result of responding to the aforementioned findings, the beneficial results can be distinguished firstly in the observed chamber conditions as shown in **FIGURE 4** where no discernable flaking was evident. In terms of key fab metrics, PM hit rate was sustained at 100 percent (**FIGURE 5)** which provided confidence to enable a PM interval increase by 45 percent on 150mm tools and 75 percent on 200mm tools (**FIGURE 6**). From a PY perspective, losses from polymer flake defects were eliminated, and with fab cost being a perennial challenge, resulted in a reduction in PM-related CoO by 19 percent. This was realized by eliminating unplanned PMs and increasing PM interval.

For so long, polymer flake defects have been considered and accepted somewhat as a trait associated with plasma metal etch. But we have found that these defects can in fact be significantly mitigated by a thorough approach to analyzing contributory factors in the equipment such as surface adhesion, moisture ingress and vibration. This can help a manufacturer deliver a high yielding process through equipment that is reliable, predictable and has low CoO. ◆

SiC power device advantages enhance power conversion systems

TAKU HAMAGUCHI, *ROHM Semiconductor, Santa Clara, CA.*

Compared to silicon, SiC has ten times the dielectric breakdown field strength, three times the bandgap and three times the thermal conductivity.

Three major factors are influencing the evolution and implementation of next-generation power semiconductor devices: regulatory requirements for ongoing improvements to efficiency in power conversion systems; market demands for lighter, smaller, more cost-effective systems with more integrated features and emerging new applications such as electric vehicles (EVs) and solid state transformers (SSTs). Up until recently, silicon has been the primary material used in power electronics, and although silicon technology continues to improve, it does have certain limitations that must be taken into consideration when designing for the growing list of essential power system requirements.

Device manufacturers have proven during the last ten years that wide bandgap (WBG) materials such as silicon carbide (SiC) and gallium nitride (GaN) provide multiple advantages in the development of next-generation power semiconductor devices. WBG-based devices offer dramatic improvements in performance, operating temperature, power handling efficiency and the ability to deliver new capabilities, which are not possible with silicon-based devices. For this reason, WBG power devices are now considered the future of power semiconductor devices.

The growing popularity of SiC devices can be traced to the availability of all components needed to build complete power systems, namely SiC diodes, switches and modules. This increased availability is the result of an expanded supply chain with a growing number of suppliers that can offer more economically viable pricing. GaN power devices have been available commercially for a much shorter period of time. Because of this varying state of maturity, SiC and GaN devices have evolved to support separate but complementary functions in different market segments.

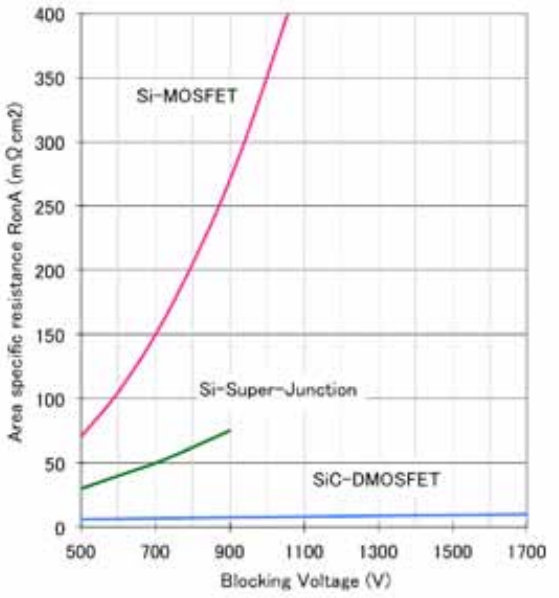

FIGURE 1. Comparison of specific on-resistance of Si-MOSFET and SiC-MOSFET.

SiC is being used for power systems because it has been proven to be more efficient than silicon. The primary advantage of SiC MOSFETs is their very

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Properties	Si	4H-SiC	GaAs	GaN
Crystal Structure	Diamond	Hexagonal	Zincblende	Hexagonal
Energy Gap : E_G (eV)	1.12	3.26	1.43	3.5
Electron Mobility : μ_n (cm^2/Vs)	1400	900	8500	1250
Hole Mobility : μ_p (cm^2/Vs)	600	100	400	200
Breakdown Field : E_B (V/cm) X10^6	0.3	3	0.4	3
Thermal Conductivity (W/cm°C)	1.5	4.9	0.5	1.3
Saturation Drift Velocity : v_s (cm/s) X10^7	1	2.7	2	2.7
Relative Dielectric Constamt : ε_S	11.8	9.7	12.8	9.5
p, n Control	○	○	○	△
Thermal Oxide	○	○	×	×

TABLE 1. Physical Characteristics of major wide bandgap materials.

low switching losses, which increase efficiency and enable higher-frequency operation.

Because the wide bandgap discussion can be a lengthy topic, this article will focus primarily on the advantages of SiC technology in power conversion systems.

SiC material advantages

The wide bandgap material properties shown in **TABLE 1** explain why SiC-based power devices can outperform silicon. SiC's breakdown field strength is ten times higher than that of silicon, plus SiC devices can be constructed to withstand the same breakdown with a much smaller drift region. In theory, SiC can reduce the resistance per unit area of the drift layer to 1/300 compared to silicon at the same silicon breakdown voltage.

Compared to silicon, SiC has ten times the dielectric breakdown field strength, three times the bandgap and three times the thermal conductivity. Both p-type and n-type regions, which are necessary to fashion device structures in semiconductor materials, can be formed in SiC. These devices can be produced with a much thinner drift layer and have very high breakdown voltage (600V and up), but provide very low resistance relative to silicon devices. Resistance of high-voltage devices is predominantly determined by the width of the drift region. Compared to silicon, the resistance per unit area of the drift layer can be reduced up to 1/300 at the same breakdown voltage with SiC materials. These properties make SiC an optimal power device material that can far exceed the performance of their silicon counterparts.

The first commercial SiC Schottky Barrier Diodes (SBDs) were introduced more than ten years ago and have been designed into many power systems, most notably into power factor correction (PFC) circuits of switch mode power supplies. Technology maturity, performance and dramatic cost reduction due to increasing volume and competition are the main reasons SiC MOSFETs have been adopted in more and more applications. SiC SBDs are currently available with breakdown voltage ratings of 600V-1700V and 1A-60A current ratings. Thus, SiC devices tend to compete with silicon MOSFETs in the 600V-900V range and with IGBTs in the 1kV+ range.

SiC MOSFETs are now experiencing greater demand with power designers for its normally-off operation and voltage controlled device advantages. Plus, SiC MOSFETs offer gate drive simplicity versus that of junction gate field-effect transistors (JFETs) and bipolar junction transistors (BJTs).

High temperature advantages

The high temperature capabilities of SiC power devices have not been fully exploited because of limitations in packaging technology and the associated lower operating temperatures of other components in systems. Currently available products are rated only at 150°C to 175°C, and SiC power modules that use special die bonding technology can operate at 250°C. R&D tests on SiC have shown operation up to 650°C is possible, whereas the upper limit of silicon semiconductors is 300°C.

Additionally, SiC's thermal conductivity is three times higher than that of silicon. These properties contribute to lower cooling needs, making it simpler

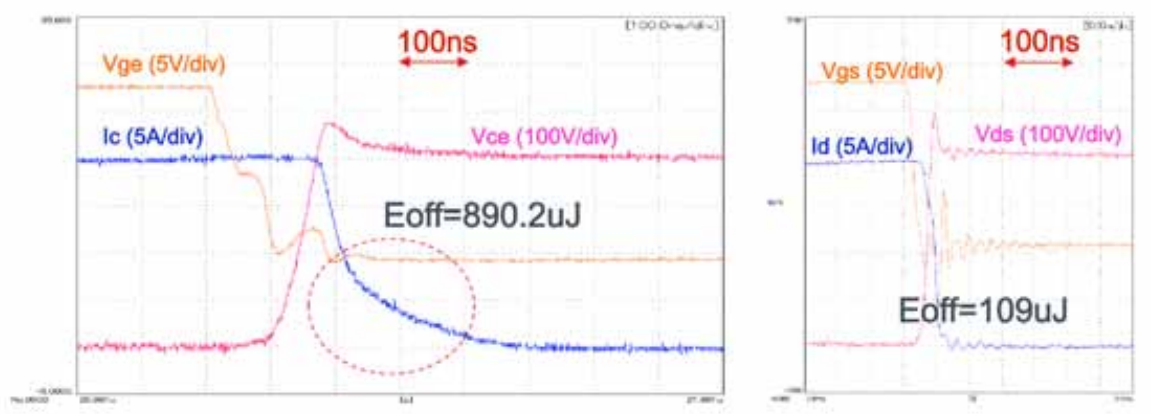


FIGURE 2. Shows 88% reduction of turn-off loss: SiC-MOSFET + SiC SBD v. Si IGBT + FRD.

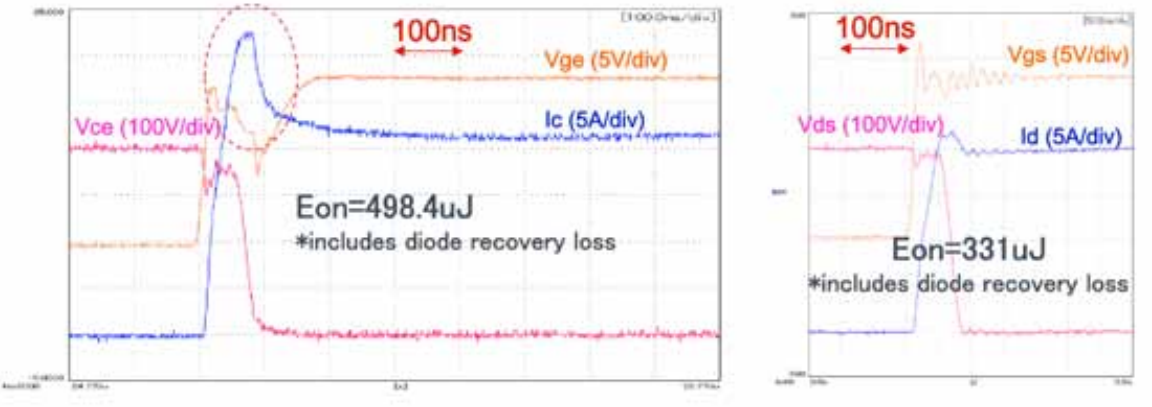


FIGURE 3. 4% reduction of turn-on loss: SiC-MOSFET + SiC SBD v. Si IGBT + FRD.

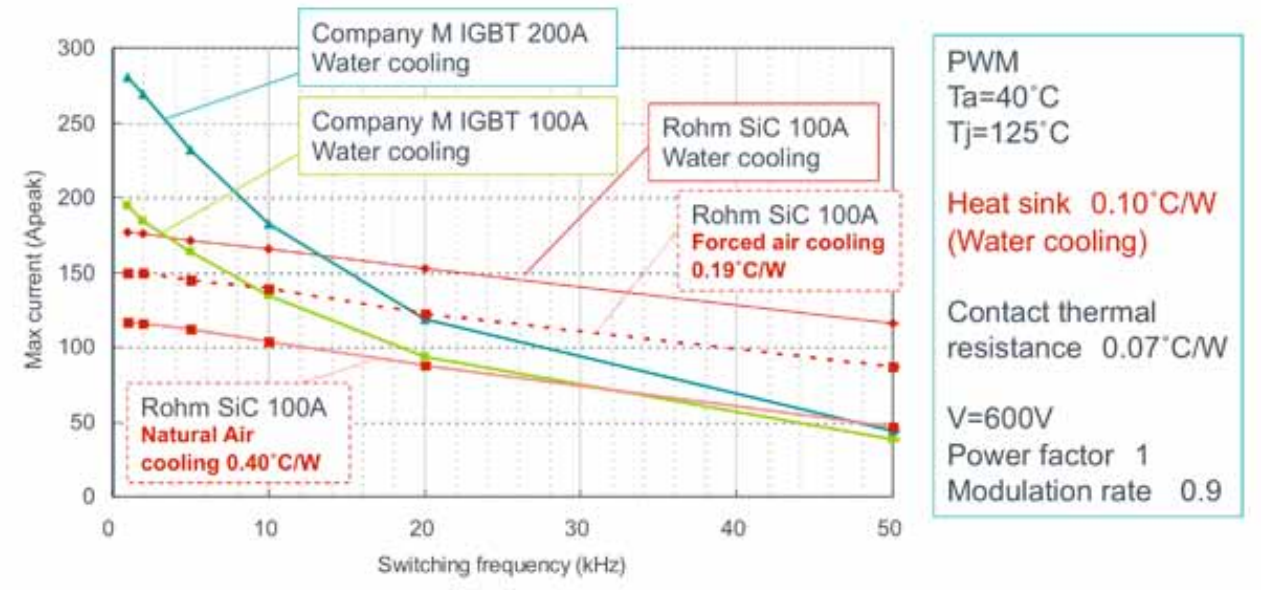
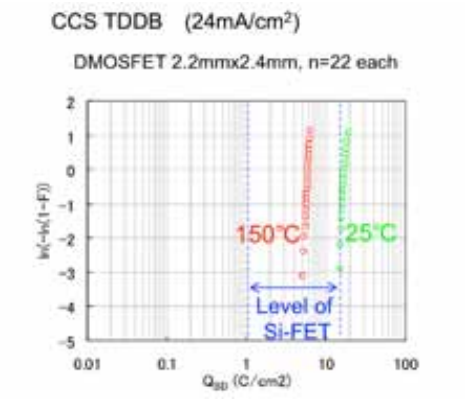
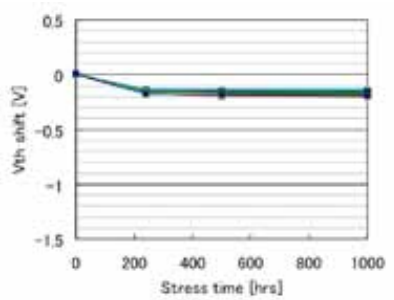


FIGURE 4. Lower switching losses allow 100A SiC module to replace 200A IGBT module.





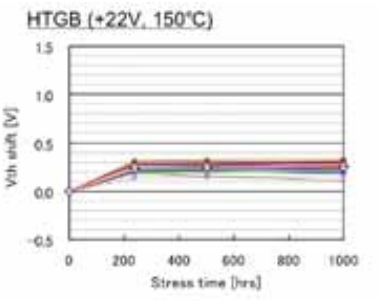


FIGURE 5. (L) Constant Current - Time Dependent Dielectric Breakdown Measurements
FIGURE 6. (C) Vth increases due to extended application of positive gate voltage.
FIGURE 7. (R) Vth decreases due to extended application of negative gate voltage.

to cool SiC components. This results in supporting thermal systems that can be smaller, lighter and lower cost.

Enablers of improved power switches

An ideal power switch is able to carry large current with zero voltage drop in the on-state, blocks high voltage with zero leakage in the off-state and incurs zero energy loss when switching from off- to on-state and vice versa. In silicon-based devices, it is difficult to combine these desirable but diametrically opposed characteristics, especially at high voltage and current. To address this problem, many designs have employed Insulated Gate Bipolar Transistor (IGBT) devices. With IGBTs, low resistance at high

breakdown voltage is achieved at the cost of switching performance using minority carriers injected into the drift region to reduce conduction (on-) resistance. Therefore, when the transistor is turned off, it takes time for these carriers to recombine and "dissipate" from the base region, thus increasing switching loss and time.

Contrary to IGBTs, MOSFETs are majority carrier devices so they have no "tail" current. SiC MOSFETs, therefore, can deliver all three requirements of power switch -- high breakdown voltage, low on-resistance and fast switching speed (**FIGURE 1**). For example, compared with silicon IGBTs and fast recovery diodes (FRDs), ROHM combines a SiC MOSFET and SiC SBD in one package, which provides 88 percent lower turn-off loss and 34 percent lower turn-on loss enabling switching frequency in hundreds of kHz range. The improvement in turn-off is due to absence of tail current in the MOSFET. The improvement in turn-on is due to the much lower recovery loss of the SiC diode.

Power systems designs can gain significant benefits through low switching losses:

- Less heat generated translates into simpler, cheaper, smaller, and/or lighter cooling systems and ultimately higher power density.
- Allows switching frequency to increase to reduce sizes of passive components (capacitors, inductors), reducing system cost, size, and weight.
- Enables lower operating temperatures so components do not have be derated as much, allowing smaller, less expensive components to be used. At the system level, this means a lower-rated SiC system can replace higher-rated silicon system.

The tests shown in **FIGURE 2** and **3** were conducted at Vdd = 400V, Icc = 20A, and 25°C, and diode recovery losses are included.

FIGURE 4 shows that at 20 kHz switching frequency, a 100-A SiC half bridge module that is forced-air cooled can replace a 200-A IGBT module that is water cooled.

SiC MOSFET reliability

Reliability is a one of the most important considerations in power electronics design. Therefore, one of the first questions from power system engineers is: "Is SiC as reliable as silicon?" The three most important aspects related to overall reliability are gate oxide reliability, stability of gate threshold voltage Vt, and the robustness of the body diode with reverse conduction.

Electrical overstressing of the gate oxide is a common failure mode of MOS devices. Gate oxide quality, consequently, directly affects SiC MOSFET's reliability. The good news is that manufacturers have solved the problem of developing high-quality oxide on SiC substrates to minimize defect density (interface and bulk traps) without compromising device life or electrical characteristics stability.

A standard test that measures the quality of gate oxide MOS is the Constant Current Stress Time-Dependent Dielectric Breakdown (CCS TDDB), shown in **FIGURE 5**. The accumulated charge QBD is a quality indicator of the gate oxide layer. The value of 15-20°C/cm2 is equivalent to that of silicon MOSFETs.

FIGURE 6 shows that when a positive voltage is applied to the gate for an extended period of time, crystal defects at the oxide-SiC interface trap electrons and cause Vth to increase.

In **FIGURE 7,** when a negative voltage is applied, trapped holes cause Vth to decrease -- the shift in Vth is 0.3V or less. These tests are performed on the ROHM Semiconductor SCT2080KE SiC MOSFET.

The results are comparable to that of a silicon MOSFET. However, the shift would be much smaller in practical usage since MOSFETs are alternately switched on and off. This allows trapped electrons and holes to "escape" between switching cycle. Thus, the accumulated trapped carriers, which cause shift in Vth, are much less.

A new era of power conversion systems

Even though there have been many significant technology advances in the last decade, and the supply chain continues to expand, the wide bandgap technology industry for SiC devices has a long way to go to reach its full potential. Making great strides is the next generation of SiC power devices, which are well-positioned to enable new era of high-volume power conversion applications such as EVs and solid state transformers. SiC can also be a positive catalyst for future technology development that enhances application capabilities while continuing to stimulate market demand.

Cashing in with chips: Improving efficiency in semiconductor R&D

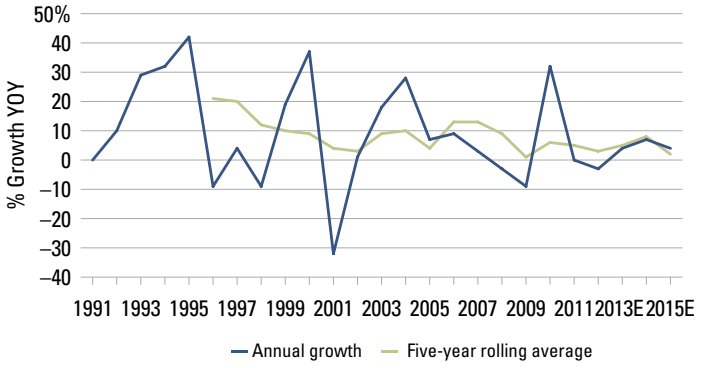
SCOTT JONES, *Alix Partners, San Francisco, CA*

Companies have achieved a 30% or greater increase in R&D efficiency—as measured by the return on invested R&D dollars—through the implementation of proper planning processes and the better allocation of resources.

The semiconductor industry showed a sign of recovery in 2013: revenue growth returned to positive territory, although it remained well below historical averages. Still, research and development (R&D) investment stayed at historically high levels for the industry, at nearly $50 billion [1]. That was largely because R&D investment is a crucial lever for maintaining high operating margins through cost improvements and for integrating new capabilities into silicon to support new applications in growing markets such as smartphones and tablets. The industry as a whole appears to be at a crucial turning point; the next two years could be make-or-break for several vital technologies that have been in development for a decade or more. The ways semiconductor companies react to those challenges may determine their own futures as well as the future of the industry as a whole. Individual companies need to achieve greater returns on their necessarily large R&D investments, and we see a need for greater R&D alignment across the industry.

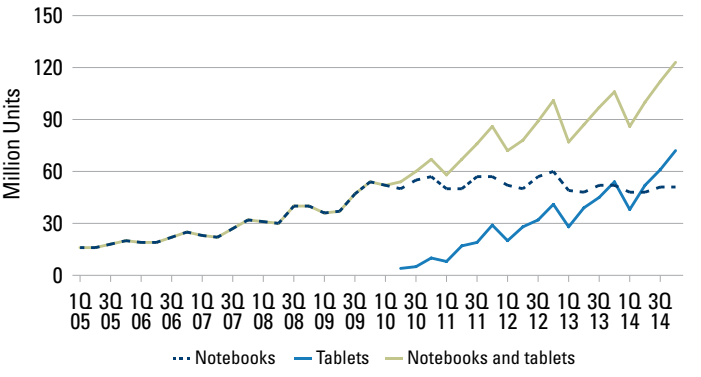
Revenue growth is back, just not as strong as before

In 2013, industry revenue was estimated to have grown by 5%. We expect revenue to grow by 6 to 7% in 2014 before 2015, when we expect it to return to levels well below the long-term average. Despite lower actual growth and due to the roll-off of 2009 data, we should observe in 2014 a spike in the five-year rolling average. When



Source: Semiconductor Industry Association and AlixPartners research

FIGURE 1. Semiconductor Revenue Growth



Source: Gartner and AlixPartners analysis

FIGURE 2. Notebook and Tablet Unit Growth

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the 2010 growth spike rolls off in 2015, the five-year rolling average will return to its previous range of 5% and below (**FIGURE 1**).

Since the sharp recovery in 2010, the industry saw zero to negative growth for two years and began only a mild recovery in 2013.

Shifting market demand

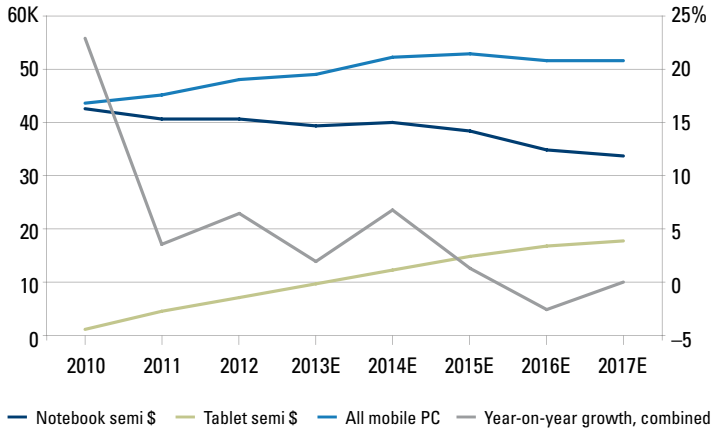
The shift from personal computers to tablets and smartphones is causing more demand for leading-edge foundry capacity as well as a temporary decrease in semiconductor content. We expect that trend to continue through 2017. The industry enjoyed a momentary boost from the introduction of tablets in 2010, but since then the growth of semiconductor content in the combined, notebook-plus-tablet market is up only marginally, even though unit demand continues to increase at historical rates (**FIGURE 2**). We expect growth in the industry to bottom out in 2017, after which the combined PC and tablet markets should return to more-traditional growth patterns of 8 to 10% per year as the transition from consumer notebooks to tablets stabilizes with converged platforms. We believe that at that point, the industry could begin to see increased growth from a multitude of end markets such as the Internet of Things and medical devices.

Further evidence that the growth engine for semiconductors is shifting from PCs to tablets and smartphones can be found in the list of the largest consumers of semiconductors. Apple's and Samsung's consumption of semiconductors has grown dramatically during the past five years, whereas the largest PC original equipment manufacturers have seen relatively little growth (**FIGURE 3**).

Leading-edge R&D spend rising rapidly

Revenue growth may be slowing, but the same cannot be said of the cost of R&D for leading-edge technologies. The cost of developing next-generation products and chip-manufacturing processes is increasing at higher rates with each generation.

Figures released by the Common Platform consortium have consistently shown that integrated device manufacturers (IDMs) and foundries are experiencing 35% cost increases from one process technology to the next and that fabless semiconductor companies are seeing even greater cost increases—of roughly



Source: Gartner and AlixPartners analysis

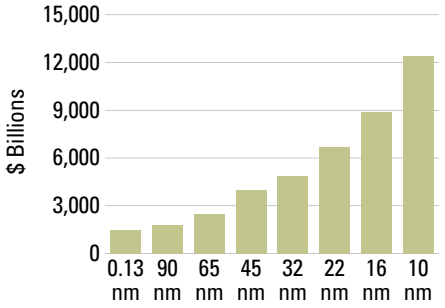
FIGURE 3. Notebook versus Tablet Semiconductor Content Growth (US$ millions)

60%—for designs and tape-outs of next-generation process technologies.

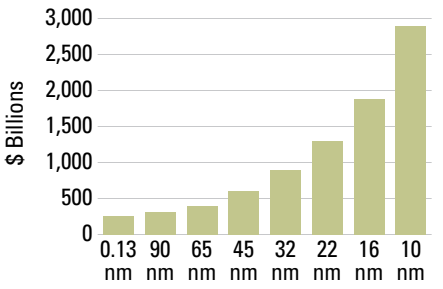
Leading-edge fabrication costs have increased at an average rate of roughly 30% per generation in the past decade, and we expect at least the same rate of increase at the 16nm generation or higher due to increased photolithography costs and the challenges of a new transistor technology necessary at 16nm and 14 nm (**FIGURE 4**). Currently, Intel is expected to be the first company to release products with 16nm technology in early to mid-2014.

Process technology development: higher costs, fewer customers

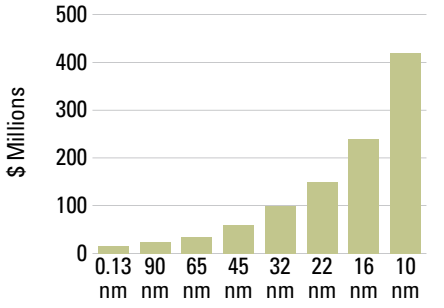
The R&D costs of development of a next-generation process manufacturing technology are increasing at nearly 40% per generation—a rate that has remained relatively steady for the past decade (**FIGURE 5**) and been caused mostly by the high cost of the test wafers and development tools necessary to deliver a new process technology. More-expensive test wafers and tools mean that foundries and IDMs cannot afford to invest in as many customer-specific or variant technologies. And that puts more pressure on foundries and IDMs to deliver a leading-edge technology platform that can address more of the market, which means placing large bets on industry trends and partnering with customers that will design into a particular manufacturing technology. If that foundry or IDM is unable to partner with customers that have significant volume demand on the leading edge, then the foundry or IDM



Source: Common Platform Technology Forum 2012 and AlixPartners analysis



Source: Common Platform Technology Forum 2012 and AlixPartners analysis



Source: Common Platform Technology Forum 2012 and AlixPartners analysis

FIGURE 4. (L) Fab Costs by Node (in US$ billions) **FIGURE 5.** (C) Process Technology Development Costs by Node (US$ billions) **FIGURE 6.** (R) Chip Design Costs by Node (US$ millions)

may never achieve a positive return on its substantial investment in the fab and design technology.

Risk is higher on investment in process technology largely because the cost of chip design for leading-edge products is rising rapidly. The cost of designing a chip for a leading-edge process has increased at nearly 60% per generation over the past decade (**FIGURE 6**), which is twice the level of the increase in the costs of leading-edge fabs and new process technologies. As a result, fabless semiconductor companies can afford fewer chip designs for the leading-edge processes, which makes it even more crucial that the leading development programs (1) have the features that end-market customers require and (2) target the market segments with the highest values. The upstream impact on the foundries is that fewer designs on the leading edge result in a higher concentration of volumes on a small number of products. That again highlights the importance of partnering with the right customer—one that can provide significant volumes on leading-edge process technologies. With fewer and fewer designs on each generation, bets on the winning technology trends will likely only get bigger.

R&D spending drivers and technology challenges

Regardless of whether we look at IDMs, foundries, or fabless semiconductor design companies, we observe a consistent increase in R&D costs across the industry. The slowed revenue growth of the past six years jeopardizes companies' ability to gain on the leading edge or even maintain current levels of financial return. That trend seems to put more pressure on semiconductor companies to seek higher returns on R&D investments so as to maintain the pace of innovation needed. For many companies, 2014 will be a pivotal year, as new technologies reach critical points in their applications to products and manufacturing. In the first half of 2014, Intel is expected to introduce its first product based on trigate transistors, which will be the company's first product based on nonplanar transistors. Other companies—such as Taiwan Semiconductor Manufacturing Company (TSMC), Samsung, and GlobalFoundries—are developing their own process technologies based on FinFET transistors [4]. The ability to ramp up those technologies at 16 nm and 14 nm will be crucial to the continued scaling necessary to drive the cost reductions consistent with Moore's law.

Beyond the technology issues that have to be faced at 16nm and 14nm are more-significant challenges, such as extreme ultraviolet lithography (EUVL) technology. Lithography is the most expensive and most crucial portion of the semiconductor manufacturing process, and the technology's current application is unable to continue in the same manner at 16nm and below. Currently, the approach for 16 nm does not use EUVL, instead calling for double patterning, which means that lithography costs will double on the current generation based on the need to go through the steps two times to get the same result as in previous generations. This will add roughly 10% to wafer costs beyond the normal cost increases from one generation to the next, as well as add increased quality concerns and yield concerns to the manufacturing process.

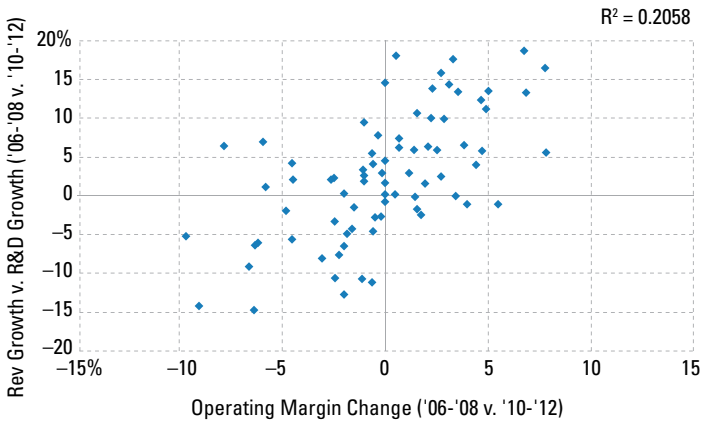
And the problem only worsens in the 12nm generation:

foundries and IDMs would have to use triple patterning if EUVL technology has not become an economically viable alternative by that time. Triple patterning would require roughly $2.5 billion additional capital spending to devise a typical fabrication capable of producing 600,000 wafers per year and would add more than $400 million to product costs per year for the fabrication [5]. If EUVL can be successfully introduced at adequate throughputs, it would be able to mitigate those additional costs and keep semiconductors scaling on the same path as during the past 30 years. For EUVL to be viable for high-volume manufacturing, the costs per wafer will have to be significantly lower than those involved in the double- and triple-patterning approaches. This would likely be necessary to drive adoption of a new technology, with significant R&D and capital investment required to integrate it into a manufacturing line.

Because the traditional advances in lithography have not achieved scaling, the industry has begun looking to other solutions. Many companies are considering different types of 3D integration -- such as multiple chips in a package or wafer-to-wafer bonding -- to achieve more flexibility in their supply chains and to improve performance without increasing the scaling on a single-chip design. But 3-D technology has not been able to gain traction with high-volume chip manufacturers because of its high costs and yield concerns, although many firms are still evaluating the options (3-D integration might help mitigate other challenges such as double and triple patterning on advanced process technologies). There is also a push to move the industry from 300mm wafers to 450mm wafers, which historically has improved the average cost per die by 30% based on the transitions to 200mm and 300mm wafer sizes. Currently, Intel seems to be the dominant force behind that push, but others such as Samsung, TSMC, and GlobalFoundries are also part of the consortium to explore the move to 450mm wafers [6].

Why R&D efficiency is crucial

Companies' major risk during periods of slower revenue growth is that pressured R&D budgets prevent the product development necessary to spur future revenue growth, thereby leading companies to miss major product cycles. This creates a so-called death spiral, whereby a company's inability or unwillingness to fund necessary R&D programs leads to further market share erosion



Sources: S&P Capital IQ and AlixPartners analysis

FIGURE 7. Change in Operating Margin versus Change in R&D as Percent of Revenue

and greater revenue declines. How does that downward spiral begin? When a company has missed market signals and its products are not aligned with end-market needs, the company is likely to lose key market share or become too heavily exposed to a shrinking market. That can lead to obvious negative impacts on revenue and earnings. A common reaction to such a scenario is to constrain R&D spending as part of overall retrenchment, but if such R&D cutbacks are not carried out in a careful and thoughtful way, the company risks accelerating its losses through continued market share declines that would result from lack of innovation.

One of the major effects of R&D efficiency is the ability to get products to market on time. For leading-edge products when power and performance count, time to market can mean the difference between success and failure. Not only must companies deliver individual programs on time, but also they must balance a portfolio of R&D resources and deliver multiple programs on time—and do it generation after generation. Having the proper balance of resources is crucial; one program that goes over budget could affect the development of the next generation of products by delaying the roll-off of resources onto that program. Sometimes organizations take on too many programs and stretch their resources too thin in an effort to capture every incremental opportunity, and that can jeopardize the delivery of programs serving the core business. Without proper discipline, chasing multiple incremental opportunities can delay key programs and can snowball into multiple generations of delayed programs. That may lead to market share loss and/

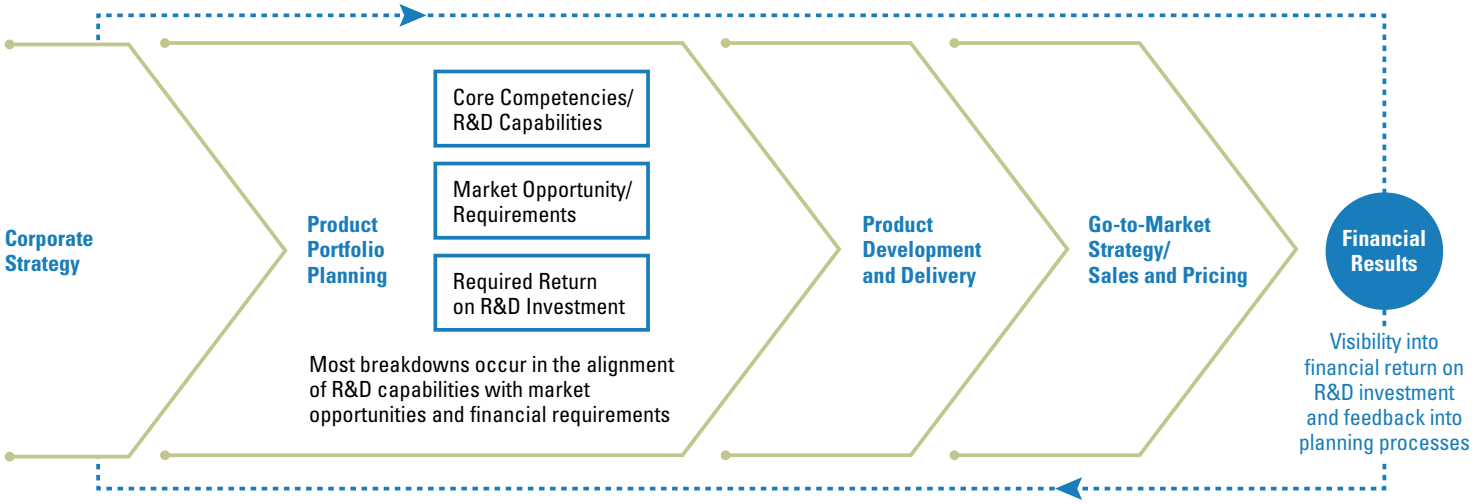


FIGURE 8. Developing a Road Map

or more-aggressive discounting and pricing, leaving fewer margin dollars to fund future R&D investment.

How spending affects profitability

Certainly, R&D is a crucial lever for maintaining competitive advantage, but simply increasing R&D spend does not necessarily lead to increased revenue growth and profitability. In fact, AlixPartners' study of the 86 largest semiconductor companies globally found no significant difference in operating margins among those companies that increased R&D spend and those that maintained or reduced spend.

What matters more, in terms of profitability, is the relationship between spending increases and revenue increases. We have consistently seen that those companies whose revenue growth exceeded their R&D spending growth outperformed their competitors by a wide margin. Such companies saw operating margins increase 85% of the time; their operating margin increases were three times higher than those of companies that had grown R&D spend more quickly than revenue (**FIGURE 7**).

Companies that achieve higher returns on their R&D investments, as demonstrated through higher revenue growth, are much more likely to achieve higher levels of profitability over time. And although there are many paths to improved profitability, we believe that improved R&D efficiency is one of the surest bets.

How do semiconductor firms improve R&D efficiency?

Companies have achieved a 30% or greater increase in R&D efficiency—as measured by the return on invested R&D dollars—through the implementation of proper planning processes and the better allocation of resources. In turn, those improvements can lead to top-line growth through market share gains in key segments and to lower R&D costs per program through faster time to market. Companies with poor R&D efficiency often suffer more from lack of proper planning than from inability to innovate. The areas of greatest importance are alignment of R&D investment with market needs, allocation of the right amount of resources, and stipulation of sufficient financial requirements for the programs to meet. Those areas require integrated planning processes, with inputs from sales and marketing, R&D, operations, and finance. Such processes should be able to capture market requirements in a specified time frame based on end-market customer feedback and be aligned with the R&D organization's ability to deliver based on its capabilities.

Aligning R&D capabilities with opportunities from the marketing organization can enable management to create a list of potential programs the company could pursue to meet market needs. After financial requirements and analysis have been provided, management can then rank the potential programs based on the company's strategic priorities and on the expected return on investment. Once program execution has begun, management should ensure that the highest-rated priority programs get fully resourced and brought to market on time, with all of the key features necessary to make the offering successful.

That approach, known as the zero-based-budget method, has been successful in the semiconductor industry as applied by such industry leaders as Texas Instruments and Intel [7]. Linkages among the marketing, R&D, and finance organizations are important in the

development of a road map that aligns company strategy with the company's go-to-market approach (**FIGURE 8**). The proper channels must be in place to ensure alignment of the different organizations at all key junctures of program development and execution; this enables the organization to course correct if market forces change and thereby affect the program's business case. Early identification of those changes can make the difference between achieving a profitable return on investment in a program and taking a substantial loss.

Several benefits result from proper program planning and proper resource allocation. For instance, delivering a predictable road map that has credibility with the customer base is essential to maintaining and growing market share in product market segments. And it makes available certain key resources for the next-generation programs necessary to keep semiconductor companies on the leading edge of the industry.

Other advantages, not always as apparent, are the effects on pricing, supply chain complexity, and R&D operational expenses. Often, when companies are late to market or misaligned with market needs, they deliver products without key features and are forced to cut their selling prices in order to maintain market share. Having a planning process in place that aligns market requirements with R&D activities enables companies to reduce the likelihood of having to discount their products heavily just to maintain market share nother potential benefit is the ability to avoid stock-keeping-unit proliferation. For instance, when it becomes apparent that a core technology investment will not generate the required financial returns, a company might produce variations of the platform technology to capture more revenue. But those additional investments and offerings add substantial complexity to the supply chain and the company's manufacturing operations. Although the incremental R&D investment for that opportunity might seem small, the impact on other organizations could be substantial because of the need to fully support a separate product offering across operations, manufacturing, and sales and marketing. Without a proper view of portfolio profitability, it is impossible to determine the impact of a program across the entire company. When a company has a well-developed planning process in place, the platform technology investment should capture sufficient market share to generate the required financial returns without having to chase incremental opportunities that have only marginal benefit and can put other investments at risk.

Where to start?

Tracking investments by program and monitoring the financial results to report their actual return on R&D investments by program can seem daunting at first. The best way to start is usually by developing a strong baseline understanding of (1) the areas in which the company is making or losing money in its current customer and product portfolios and (2) where it has targeted current R&D investments for future revenues. Such a baseline understanding facilitates the establishment of an analytics platform that can reveal the true potential of a company's investments and that can identify opportunities for improving the return on those investments. We believe that to ensure alignment with market needs, R&D capabilities, and financial returns, the establishment of the aforementioned processes and tools is central to starting a robust planning process with proper inputs from all of the key organizations.

Innovation is a major competitive differentiator for semiconductor companies. Getting to market on time and with the right products can make the difference between success and failure, especially because today's revenue growth remains low and the cost of R&D continues to rise. In that context, optimizing the efficiency of the R&D investment process is of paramount importance. Successful semiconductor companies likely avoid the so-called innovation death spiral and improve R&D returns through proper planning processes and better allocation of resources. In that way, companies can achieve top-line growth while lowering R&D costs per program, thereby paving the way to future successes.

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FinFET on SOI: Potential becomes reality

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By using SOI-based FinFET technology, the need for doping in the body has been effectively minimized, resulting in excellent matching characteristics in the undoped DRAM transfer device, and truly remarkable minimum operating voltage in the SRAM.

We report here empirical results demonstrating the electrical benefits of SOI-based FinFETs. There are benefits inherent in the elimination of dopant as the means to establish the effective device dimensions. However, significant compromise is unavoidable when using doping as a means of isolation, as in bulk-based FinFETs. Accordingly, we use SOI as the base on which to build the FinFET, which not only simplifies the process but enables full realization of the potential of the device.

Fully depleted transistor technologies – both planar and SOI-based FinFET – offer excellent circuit operation for SRAM and DRAM due to the unsurpassed threshold voltage matching associated with the near-absence of doping. Additionally, good low voltage and stacked-fet circuit operation is realized due to the superior electrostatics associated with thin-body devices. Hardware data specifically illustrating these features is described below.

Threshold voltage matching and distribution

A significant improvement in threshold voltage mismatch has been well documented, as well as the degradation associated with adding doping to a FinFET. Less well publicized, however, is the even larger relative benefit to be found in thick-dielectric transistors, such as are used for analog and IO devices, and also in DRAM.

Random dopant fluctuation is not the only mechanism contributing to local threshold voltage mismatch, but it has historically been the largest contributor. It has been an even larger contributor for thicker dielectrics, as its baleful influence scales directly with dielectric thickness, unlike work function variations for example. Therefore an even more dramatic improvement in matching is found in thick-dielectric devices, as shown in **FIGURE 1**.

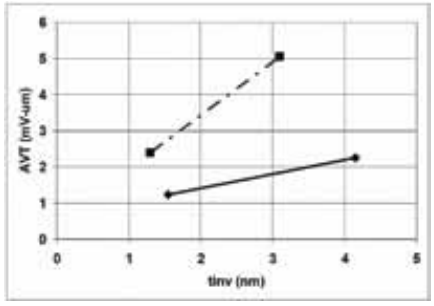

FIGURE 1. Mismatch data as a function of tinv for conventional doped (dotted line) and SOI FinFET (solid line). While the improvement in matching for 'thin-oxide' (1.2-1.5nm) is well known, less widely recognized is the even larger advantage obtained with 'thick-oxide' (>3nm) devices commonly used in IO and analog applications.

This improvement is important to IO and analog circuit operation and is vital to scaling the DRAM transfer device into the next generations.

In **FIGURE 2** are shown probability plots of the threshold voltage for two DRAM transfer gate transistors and the profound improvement is obvious. The FinFET version actually has a considerably thicker gate dielectric than the

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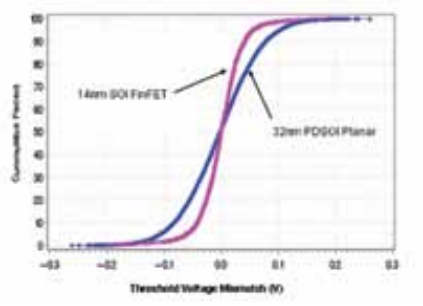

FIGURE 2. Threshold voltage matching for DRAM transfer devices. Blue: 32nm generation thick oxide doping-controlled device. Red: 14nm generation thick oxide FinFET device.

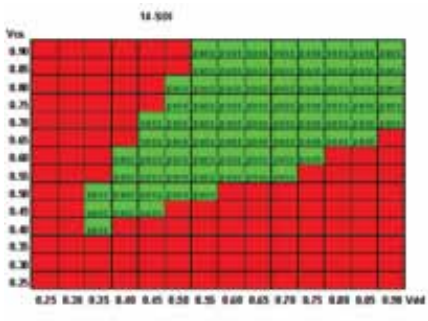

FIGURE 3. Shmoo plot of 14nm SOI FinFET SRAM array showing a minimum operating voltage of 400mV, with full read and write capability.

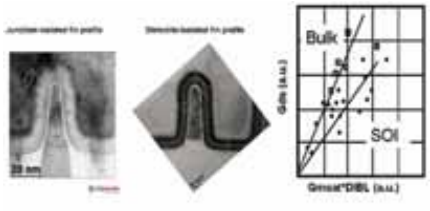

FIGURE 4. Representative bulk-based and SOI-based fin profiles, and corresponding empirical degradation in electrostatics. The tapered shape of the bulk fin shown results in nonuniform current flow and poorer low-voltage operation and self-gain than the more ideally shaped SOI FinFET.

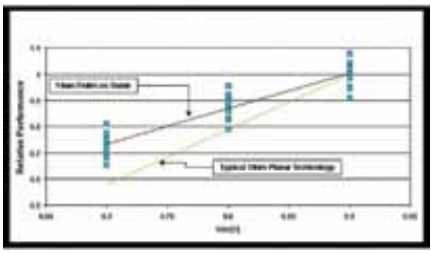

FIGURE 5. Normalized frequency reduction as a function of Vdd for a suite of circuits (NANDs, NORs, and inverters). Near-perfect correspondence of the SOI FinFET data with the compact model is shown. This flatter voltage dependence is highly superior to that typical of doping-controlled planar technology.

conventional doped device and a shorter gate yet much better matching. The absence of thickness-driven matching opens up the device design space and enables optimization of the overall design, as well as allowing for the fundamental area scaling needed to move to the next generation.

SRAM Vmin

One of the most important benefits of improved matching is the much-desired reduction in the minimum operating voltage of the classic 6T SRAM. While the transistor matching data clearly show an advantage, putting it all together into a quantized FinFET SRAM cell with correct beta and gamma ratios and device centering to actually achieve low Vmin is a larger challenge.

Additionally, there may be other factors present in the scaled-up SRAM array that may not be so evident in the classic Pelgrom analysis from which most matching data are derived, such as some perturbation to line-edge-roughness, or nfet/pfet interactions, or any number of other possibilities.

Our data demonstrate that these concerns are surmountable and that real SOI FinFET SRAMs can operate at very low voltages. **FIGURE 3** shows remarkable results on an SRAM array, with full read and write operation down to 400mV, without any assist circuitry. This is among the best results ever reported, even among those that utilize boost techniques and in-situ tuning of the devices.

Low voltage circuit operation

A considerable improvement in electrostatics associated with the FinFET over conventional doped devices not only enables the necessary gate-length scaling, but simultaneously improves the relative performance at reduced voltage and therefore reduces the power density at a given performance. While fully-depleted devices should in principle enjoy this advantage, the introduction of non-uniformity such as is involved with the tapered fin profile associated with bulk-based FinFET seriously compromises the output conductance and may obviate these expectations, as shown in **FIGURE 4**.

The fin profile obtainable in SOI-based FinFETs is very nearly ideal and our data show that the low voltage benefits are fully realized in hardware. The frequencies of a suite of ring oscillator circuits (inverter, NANDs, and NORs) were measured on 14nm SOI-based FinFET hardware as a function of voltage and compared to the modeled expectations.

FIGURE 5 shows excellent correspondence with expectation, and also shows how the data are far superior to the voltage dependence of conventional planar technology.

Ag plating in HBLED packaging improves reflectivity and lowers costs

JONATHAN HARRIS, *President, CMC Laboratories, Inc., Tempe, AZ*

Various types of Ag plating technology along with the advantages and limitations of each plating approach are discussed. Potential issues with Ag as a packaging metallization, and some of the steps that need to be taken to mitigate risks, are also reviewed.

HBLED packaging is becoming one of the new, high volume applications for Ag metallization. Traditionally used in power semiconductors, plated Ag is rapidly replacing Au in all levels of HBLED packaging, including first level ceramic packages and second level IMS materials. The replacement of Au is driven by two clear advantages of Ag for the HBLED application: much lower material cost and higher reflectivity in the visible spectrum. Other advantages of Ag include higher electrical conductivity, higher thermal conductivity and no tendency to work-harden under repeated mechanical stress. Table 1 shows a comparison between Au and Ag for a number of key properties.

But Ag also has some disadvantages that must be carefully considered. Ag plating often involves higher free cyanide concentration plating solutions that require more safety controls (and thus more cost). And autocatalytic electroless plating baths for Ag are much less mature, and have fewer vendors, than autocatalytic Au. Another area of concern for device reliability is Ag migration. If a thin film of water absorbs on the surface between two Ag pads at different voltage, Ag dendrites can rapidly form effectively shorting out the two pads. This is particularly a problem in the presence of halide contamination. Last is the well know phenomena of Ag sulfide formation which can greatly reduce reflectivity as well as solder wetting and wirebond ability of a Ag surface. Ag2S forms when Ag metal is exposed to sulfur containing gases such

Property	Ag	Au
Metal Cost (per tr. oz)	15	863
Electrical conductivity (S/m)	6.3 x 107	4.1 x 107
Thermal conductivity (w/m-K)	429	318
Density (g/cm3)	10.49	19.3
Reflectivity 500nm %	**>90**	**<40**

TABLE 1. Comparison of Ag and Au.

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Bath Type	Source of Oxidation/ Reduction Reaction	Key Deposit Characteristics
Immersion Silver	Oxidation/dissolution of the pad or circuit line metal surface	Very thin Ag layer. Deposits wherever metal is present. Requires pad material to be less noble than Ag (Cu, Ni)
Autocatalytic Silver	Oxidation and reduction of chemical species in the bath	Can be a thick deposit. Deposits wherever metal is present. Can deposit on more or less noble metals. Requires rigorous control over plating process. Bath lifetime a few metal turn-overs.
Electrolytic Silver	Plating is driven by an external electrical current with an applied voltage	Only deposits on pads connected to the external circuit. Can be very thick. Very mature plating technology for Ag. Many parameters to adjust deposit properties.

TABLE 2. Comparison of basic plating processes.

as H2S, a component in air pollution. Special precautions must be taken to protect Ag surfaces from H2S and other sulfur containing chemicals. Ag surfaces also passivate when exposed to chlorides, so limiting chloride exposure is also necessary to keep the Ag surface metallic.

The purpose of this article will be first to discuss the different types of Ag plating technology, and how each plating approach fits in the HBLED application. The second focus will be to discuss both the advantages and dis-advantages of Ag with respect to HBLED device performance as well as short and long term reliability.

Ag plating technology

There are two broad categories of plating technology: electrolytic and electroless plating. For electrolytic plating, the metal surface to be plated is biased as the cathode in an electrochemical cell which contains dissolved metal ions (Ag+). The plating solution acts as the (ion conducting) electrolyte and an external Ag electrode in the plating bath acts as the anode. When the substrate to be plated is cathodically biased, and electrical current is applied, Ag ions from solution will plate out on the cathode (reduction reaction), and Ag metal from the anode will dissolve into solution (oxidation reaction). The critical requirement for electrolytic plating is that all of the circuit features that need to be plated are electrically connected and can be easily contacted with an external connector (typically a pin in a plating rack).

There are a number of key advantages of electrolytic plating if this circuit continuity can be achieved:

- Plating is directly controlled by the applied electrical current. The higher the current, the faster the plating rate (within limits, if the rate is too fast other competing reactions can occur)
- There is no intrinsic limit to the thickness of the deposit
- There are many adjustable parameters including current density, metal ion concentration, voltage profile, temperature, and degree and type of agitation. These parameters can be used to adjust and optimize deposit ductility, thickness uniformity, density, roughness and pad adhesion.
- If properly maintained, the lifetime of the plating bath can be very long, on the scale of many months. In addition, electrolytic plating chemistry is significantly less expensive than electroless plating baths. Both of these factors lower plating costs.

For electroless plating, the oxidation and reduction occurs within the plating bath, not driven by an external

circuit. This allows plating to be accomplished on metal features that are electrically isolated from each other, which is a common feature of many types of circuits. There are two basic types of electroless plating technologies. One is "immersion plating" and the other is "autocatalytic plating."

Immersion plating is accomplished by depositing a "more noble" metal onto a pad of "less noble" metal. The reaction is very simple. The oxidation reaction is the dissolution of the "less noble" pad metal into the plating solution. The reduction reaction is deposition of "more noble" metal ions in solution onto the pad material. This is essentially a controlled galvanic corrosion process. In the case of Ag, deposition can occur on metals such as Cu or Ni which are less noble. The limitation of immersion plating is that the process stops or slows dramatically once the pad surface is covered with the depositing metal since corrosion of the underlying pad material can no longer occur (oxidation reaction is shut down). Consequently, immersion plated layers tend to be very thin.

Auto-catalytic electroless plating is much more complex. In this case, specific species are added to the plating bath which drive continuous oxidation and reduction reactions. Small levels of catalyst are first deposited on the surface to be plated to favor reduction reactions (plating) on the surface of the pad versus in the solution. Auto-catalytic plating baths require high levels of chemical sophistication to develop, because there is a very fine balance that must be achieved. If the oxidation/reduction reactions are too aggressive, plating will occur in solution or on surfaces that are not metal. If the oxidation/reduction reactions are too passive, then plating cannot be easily initiated on all metal surfaces. Because chemical reactions are very sensitive to impurities, chemical uniformity and temperature, the plating process must be very tightly controlled so that impurities do not build up in the bath, and temperature across the part being plated is extremely uniform. However, an advantage of auto-catalytic baths compared to immersion baths is that much thicker plated layers can be achieved. These basic plating processes are compared in **TABLE 2**.

For the HBLED application, there are a number of potential requirements for the Ag plated layer which impact which type of plating chemistry is utilized. Some of these various requirements are summarized in **TABLE 3**.

From a development standpoint, immersion Ag and high cyanide (CN) electrolytic Ag plating baths are well established technologies. Auto-catalytic Ag and lower free CN Ag electrolytic plating baths are newer technologies that are less established in high volume applications.

Ag Layer Function	Conditions	Comments	Candidate Baths
Solder Pad	SAC 305 Solder	Ag layer should be thin to limit Ag dissolution in the solder	Immersion Ag, autocatalytic Ag, electrolytic Ag
High reflectivity pad or conductor	Maintain reflectivity after heat exposure for die attach, wirebonding, silicone curing cycles	Underlying metals such as Ni or Cu diffuse in Ag during thermal cycles. On the Ag surface these metals form oxides and they can hurt die attach and wirebonding reliability as well as reducing Ag reflectivity. Thicker Ag layers reduce this effect.	Auto catalytic Ag, electrolytic Ag. If plating with a white solder mask or dry film present, then only low CN, lower pH electrolytic Ag is stable

TABLE 3. Summary of HBLED Ag layer requirements.

Critical issues for Ag plating

For most HBLED applications, electrolytic Ag plating is preferred if this can be accomplished with the circuit design. This allows use of a very mature plating technology and can be used to deposit thick Ag layers. If thick Ag is required to maintain high reflectivity, good wirebonding and die attach after thermal exposure, and electrolytic plating is not possible, then the less mature autocatalytic Ag is the only real option. In addition to being less proven in high volume manufacturing, this plating technology is also more expensive to implement due to higher plating bath costs and shorter bath lifetime (few metal-turn-overs or MTO) and the need for very tight control over the plating environment.

Ag migration

From an HBLED reliability point-of-view, the most significant issue for Ag metallization (no matter how it is deposited) is Ag migration. If Ag migration forms a short between the diode anode and cathode, of course the device will no longer function. There are a number of critical requirements which must be met for Ag migration to initiate:

1. There must be two electrodes separated by a dielectric at different electrical bias
2. The electrode with an anodic bias must have some amount of exposed Ag
3. Between the two electrodes the surface of the dielectric must have a hydrophilic surface chemistry
4. There must be a source of humidity. The humidity level does not have to be very high since electrochemical Ag migration can occur with a few monolayers of adsorbed water. RH above 30% have shown migration to occur in some cases.
5. There must be a source of ionic contamination, particularly chlorides. For chlorides the level should exceed 4 μgrams/in$_2$. [1]

Typically an organic residue such as a flux residue on the dielectric surface results in a hydrophilic surface chemistry on FR4. Most ceramic materials, such as Al_2O_3 also have hydrophilic surfaces which will attract a water layer.

Once these conditions are met, the electrical bias difference between the two pads results in the electrochemical dissolution of the Ag from the anode and deposition of this dissolved Ag onto the cathode. Because of the low concentration of Ag in solution, the structure of the deposit is dendritic. Dendrites will continue to grow until they form a short between the anode and the cathode. Under the right set of conditions, dendrites can grow in a matter of minutes. **FIGURE 1** shows a Ag dendrite grown on an Al_2O_3 surface between two Ag pads (pads are not shown). Typically the first few dendrites that connect will burn out like a fuse due to the high current density, but over time a more stable short will develop with many dendritic fingers.

Studies have shown that the presence of a solder mask between the two biased pads can help reduce the probability of dendrite formation, as long as the solder mask

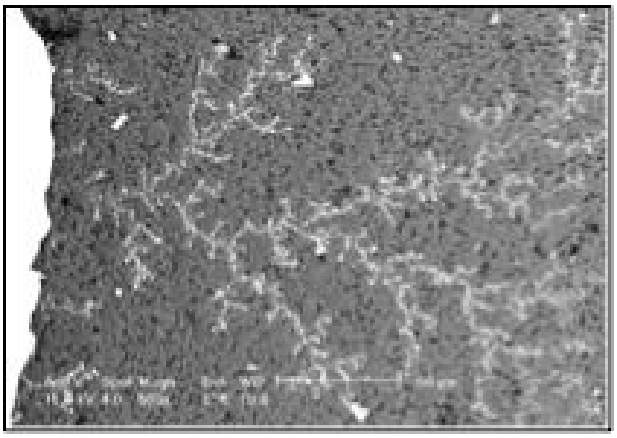

FIGURE 1. Dendrites growing across alumina dielectic. Ag electrodes on top and bottom (not shown).

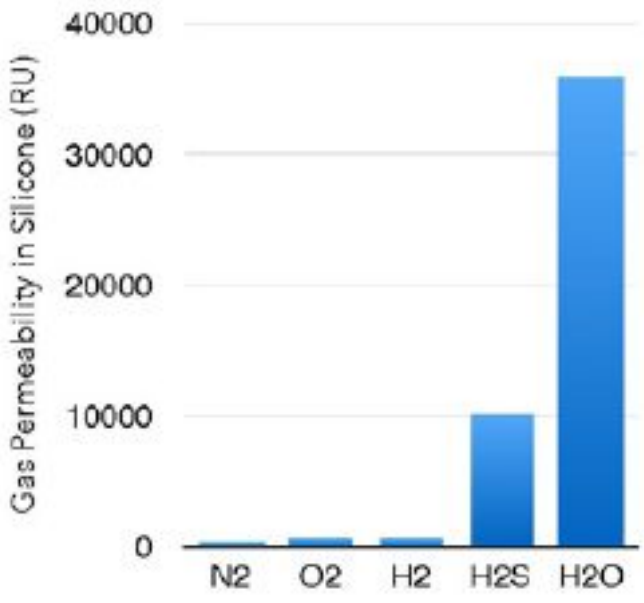

FIGURE 2. Gas permeation rates through silicone (relative).

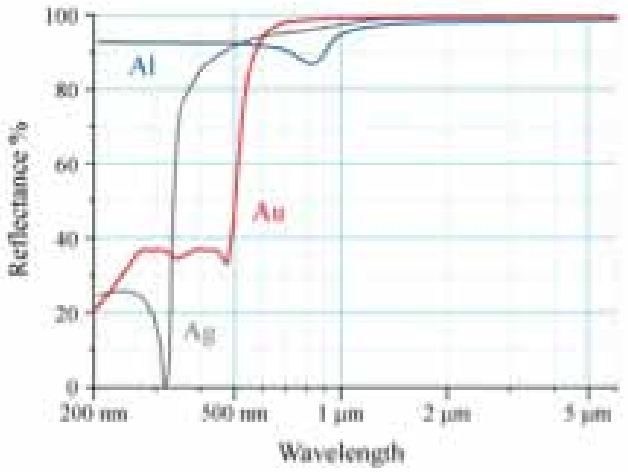

FIGURE 3. Reflectance % vs. wavelength through the visible for various metals.

is not a source of halide contamination. The presence of the mask makes it much more difficult for a continuous layer of water to form between the two pads. [2]

Ag sulfide formation

Ag does not readily form an oxide but will form a sulfide with exposure to sulfur containing gas species such as H2S. This is an issue for HBLED for two reasons. First, a moderate level of Ag_2S will decrease visible light reflectivity hurting HBLED light output. For more severe Ag sulfide formation, Ag conductor lines can be corroded.

There are two main areas of focus in controlling the impact of Ag_2S formation. The first focus area begins after plating is complete and ends once the device is packaged and assembled. Since thin layers of Ag_2S passivation will impact assembly operations such as wirebonding, rigorous efforts must be made to keep the Ag surface very clean until assembly is complete. One option is to control exposure to sulfur containing gases by keeping plated parts in a controlled environment. Another option is to apply a thin organic coating, the way OSP is used to protect plated Cu from oxidation in the PCB industry. Many plating bath vendors who sell Ag formulations also sell proprietary organic coating baths.

The second area of concern is silver sulfide formation in the finished package. This can impact reflectivity, as discussed above, as well as conductor integrity in more extreme cases of exposure. Encapsulates such as silicone are typically not good barriers to H_2S and thus offer limited protection. Relative rates of gas permeation in silicone is shown in **FIGURE 2**. [3]

FIGURE 4. Cross section showing plated Cu with bright Ni smoothing layer to decrease surface scattering.

Factors that influence Ag reflectivity

As shown in **FIGURE 3** [4], Ag intrinsically has very high reflectivity in the visible spectrum (wavelength from 350 to 750 nm). In addition, plating can be utilized to further enhance light reflection by decreasing surface roughness which can lead to surface scattering.

FIGURE 4 shows a cross section of a rough plated Cu surface that has been over-plated with an electrolytic bright Ni layer that has had organics added to the plating bath to promote leveling and smoothing of the surface. You can see from this cross section how dramatically smoother the surface texture is after the bright Ni layer. The peak-peak roughness factor, RP goes from 2.89 µm for the as-plated Cu, to 0.09 µm for the top of the bright Ni deposit. When this surface is then plated with Ag, a mirror finish results.

Assembly operations with Ag

Provided that there is no significant Ag_2S passivation, Ag is an excellent surface for both soldering and wirebonding. For wirebonding to Ag pads, typically Au wire is utilized. Because Au and Ag form a continuous solid solution, a diffusion bond is formed during wirebonding, very similar to a Au/Au wirebond.

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3D NAND: To 10nm and beyond

SARA VER-BRUGGEN *contributing editor*

The transition to 3D NAND is inevitable, but there is still plenty to be squeezed from 2D NAND technology. An Applied Materials-sponsored panel at IEDM discussed where the industry is today and where it's headed.

In launching the iPod music player, Apple bumped consumption of NAND flash – a type of non-volatile storage device – driving down cost and paving the way for the growth of the memory technology into what is now a multibillion dollar market, supplying cost-effective storage for smart phones, tablets and other consumer electronic gadgets that do not have high density requirements.

The current iteration of NAND flash technology, 2D – or planar – NAND, is reaching its limits. In August 2013, South Korean consumer electronics brand Samsung announced the launch of its 3D NAND storage technology, in the form of a 24-layer, 128 GB chip. In 2014, memory chipmakers Micron and also SK Hynix will follow suit, heralding the arrival of a much-anticipated and debated technology during various industry conferences in recent years. Other companies, including Sandisk, are all working on 3D NAND flash technology.

Like floors in a tower block, in 3D NAND devices memory cells are stacked on top of each other, as opposed to being spread out on a two-dimensional (2D), horizontal grid like bungalows. Over the last few decades as 2D NAND technology has scaled, the X and Y dimensions have shrunk in order to go to each chip generation. But scaling, as process nodes dip below 20nm and on the path towards 10nm, is proving challenging as physical constraints begin to impinge on the performance of the basic memory cell design. While 2D NAND has yet to hit a wall, it is a matter of time.

Transition to mass production

But despite the potential of 3D NAND and announcements by the leading players in the industry, transferring 3D NAND technology into mass production is very challenging to do. As Jim Handy, from Objective Analysis, points out: "The entire issue of 3D NAND is its phenomenal complexity, and that is why no one has yet shipped a 3D NAND chip yet." Mass production of Samsung's device will happen this year. With 3D NAND there is the potential for vertical scaling, going from 16-bit-tall strings to string heights of more than 128 bits.

But while 3D NAND does not require leading-edge lithography, eventually resulting in manufacturing costs that are lower than they would be for the extension of planar NAND, new deposition and etch technologies are required for high-aspect-ratio etch processes. This "staircase" etching requires very precise contact landing (**FIGURE 1**). In 3D NAND manufacturing depositing layers of uniform thickness across the entire wafer presents issues with pull-back etching for these "stair steps" that currently increase the lithography load more than was originally anticipated.

"Everything in 3D is a significant challenge. With vertical scaling the challenges include etching high aspect ratio holes, with the aspect ratio doubling with each doubling of layers. These holes must have absolutely parallel walls or scaling and device operation may be compromised. If the layers are thinned then the atomic-layer deposition (ALD) of the layers must be able to apply a constant thickness layer across the entire wafer, which is also true of the layers that are deposited on the walls of the hole," according to Handy.

Indeed, while the best combination of cost, power and performance will be found in 3D NAND archi-

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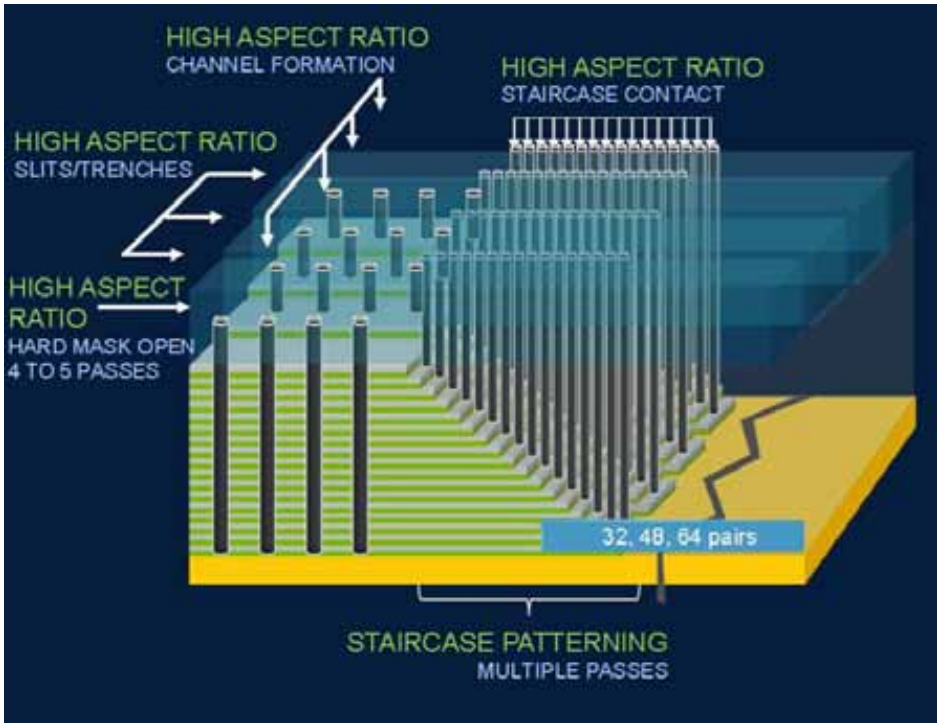

FIGURE 1. Staircase etching requires very precise contact landing.

tectures, there still remain issues concerning cost, especially. These issues, in the context of their respective memory technology roadmaps, were discussed by memory chipmakers, including Sandisk, SK Hynix and Micron, at a forum organized and sponsored by semiconductor industry equipment manufacturer Applied Materials in December 2013, while the equipment supplier provided some in-depth discussion on 3D NAND manufacturing considerations and challenges. The session was hosted by Gill Lee, Senior Director and Principal Member of Technical Staff Silicon Systems Group at Applied Materials.

Sandisk plays its 2D hand for as long as possible

Ritu Shrivastava, Vice President Technology Development, at Sandisk Corporation, set out the challenge. "Whenever you talk about technology, it has to be in relation to the objectives of your company. In our case we have a $38 billion total available market projected to 2016 and any technology choices that we make have to serve that market." Examples of products he was referring to include smart phones and tablets. "Our goal is to choose technologies that are most cost-effective and deliver in terms of performance."

Sandisk has a joint NAND fab investment with Toshiba and the two have had a 128 GB 2D NAND flash chip using 19 nm lithography in production for a while now. They have also previously announced plans to build a semiconductor fab for 16-17 nm flash memory.

"One of our goals is to extend the life of 2D NAND technologies as far as possible because it reflects the huge investment that we have made in fabs and the technology, over the number of years," said Shrivastava. "Of course, 3D NAND is extremely important and when it becomes cost-effective then it will move into production." Sandisk plans to start producing its 3D NAND chips in 2016.

"We are travelling in what we think is the lowest cost path in every technology generation, going from 19 nm to 1Y where we at the limit with lithography, and then we will scale to 1Z, which is our next-generation 2D NAND technology. We believe that this scaling path gives us the lowest cost structure in each of the nodes and in terms of cumulative investment," he added.

But it is not just achieving the smallest die size, it is the cost involved in scaling. Capital equipment investment is what determines success in the market, according to Shrivastava. "Even though we are saying that 3D NAND is a reality there are a couple of things that we need to keep in mind. It leverages existing infrastructure, which is good, but there are still a lot of challenges. 3D NAND devices use TFT as opposed to the floating gate devices commonly used in 2D NAND chips. New controller schemes and boards will be required also."

So while, according to Shrivastava, 3D NAND is looking very promising, there is a big 'but' for a company such as Sandisk, which produces some of the most cost-competitive flash memory devices on the market. "2D NAND still continues to be more cost-effective than 3D NAND and 3D NAND is not yet proven in volume manufacturing. Every new technology takes some time. Getting to mass manufacturing will take time. Our goal is to extend 2D NAND as long as possible, continue to work on 3D NAND and introduce it when it becomes cost-effective."

Shrivastava sees 2D and 3D NAND technologies co-existing for the rest of the decade. Beyond 3D NAND the company is developing a 3D resistive RAM (RRAM) as the future technology beyond 3D NAND.

From 3D DRAM to 3D NAND

Next Chuck Dennison, Senior Director Process Integration, from Micron, provided an overview of where the company is today in terms of its own NAND memory technology roadmap.

"Our current generation is 16nm NAND that is now in production and we're showing that it is getting to be a very competitive and very cost-effective technology," according to Dennison. Micron's new 16nm NAND process provides the greatest number of bits per sq mm at the lowest cost of any multilayer cell (MLC) device. Eight of these die can hold 128 GB of data. The 16nm storage technology will be released on next-generation solid state drives (SSDs) during 2014. SSDs consist of interconnected flash memory chips as opposed to platters with a magnetic coating used in conventional hard disk drives (HDDs). A Micron 16nm chip is shown in **FIGURE 2**.

"Our next node is a 256 GB class of the NAND memory. Technically it could be extended before taking the full step to 3D NAND," he said.

Today NAND is the lowest cost-per-bit memory technology and this continued cost-per-bit reduction is really driving the whole of the NAND industry, according to Dennison. It is why NAND replaced DRAM in terms of total dollars and has continued to proliferate across various applications, and is responsible for continued innovation in portable consumer electronics, such as tablets, where so much functionality enabling photography, video recording, storage of an entire music library, and so on, can be packed into one device.

Outlining Micron's technology scaling path, Dennison explained: "We went to high-K/metal gate to 20 nm and we used the same technology to extend us to 16nm. From there, the company is moving to a vertical channel 3D NAND for a 256 GB class.

"In terms of capital expenditure (CapEx) per wafer it all looks very cost-effective, with a little bit of transition going to 20 nm," explained Dennison, because of the high-K metal gate, but with minimal increase going to 16nm. "But when you go to 3D NAND it is expensive, per wafer. So if you are increasing your wafer costs by X amount you need a much higher amount of GB per cm sq, so the density we are choosing to go with is a 256 GB class. And when you start actively looking at 3D NAND there are a lot similarities between 3D NAND and DRAM," he explained, referring to the stacked capacitor of DRAM. "There is a lot planarization, you are etching very high aspect ratio contacts where you need to be very controlled, in terms of how you define your control and CD uniformity. Then there are a lot of additional modules requiring ALD deposition. So we think that there is a lot of opportunity to utilize our DRAM expertise."

He outlined an inflection point going from 16nm, again. "We're transitioning to go to the 256 GB density. We think that when we do this it will make financial sense and it will be a cost-effective solution despite the high Capex. And then from there we will continue. With the majority, or bulk, of the market we'll see vertical NAND continuing to scale with a couple of us scaling fast for that market."

Dennison also touched on longer term advances in classes of flash memory, in the form of 3D cross-point technology. These are memories stacked in cross-point arrays over CMOS logic to enable memory technology with speed features akin to DRAM but the density and cost effectiveness of NAND. The 3D stacked memory arrays in 3D cross-point technology would make these devices suitable, for future, in very high density computing and even biological systems.

"But, to conclude, NAND will not be replaced and will

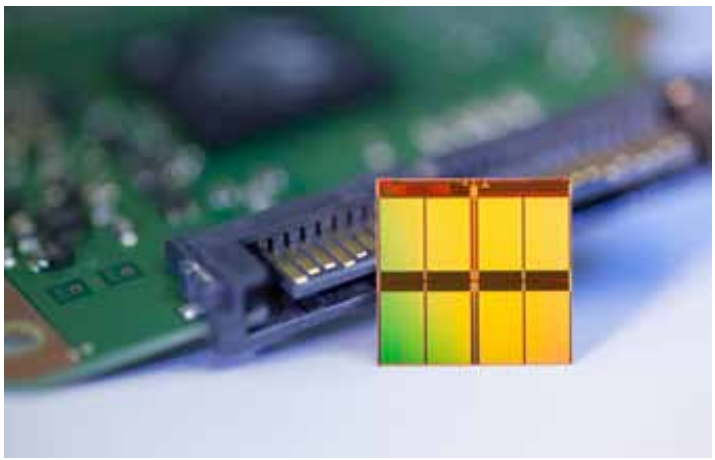

FIGURE 2. Micron 16nm NAND die.

continue to be the lowest cost, it's going to be the largest market in tablets, phones and so on. It's not the best memory technology – it has poor cycling endurance and it has a terrible latency – but it is very low cost at very high density so it is the most cost-effective solution. We think that 3D cross-point absolutely has a market in terms of displacing DRAM and will selectively displace some NAND in very high performance applications but we will stay with NAND and go to 3D NAND."

Soek-Kiu Lee, VP and Head of the Flash Device Technology Group, at SK Hynix brought the audience up to speed on his company's NAND technology. Every year SK Hynix has increased bit density per area by around 50%. The company's 16nm 64 GB MLC NAND flash, based on floating gate technology, has been in production since mid-2013 with SK Hynix now entering full scale mass production of 16nm chips. SK Hynix will start to ship samples of its 3D NAND chips this year with mass production happening later in 2014.

Like Shrivastava, Lee expects that 2D NAND and 3D NAND will co-exist and compete with each other in terms of reliability, performance and density, for some time and that the big challenges facing the transition to 3D NAND architectures include stabilization of multi-stack patterning to improve yields, better metrology and defect monitoring in the 3D structure itself.

Head for heights

Lastly, Applied Materials was able to provide some insight into manufacturing the more complex structures that moving to 3D NAND device architecture entails. Very simplistically, to make 3D NAND flash devices requires building extremely tall multilayer structures. Every layer in the device requires an insulating layer, so – for example – a 32-layer device is really a 64-layer device. As a result of this, aspect ratios of the structure being etched are getting to be very high and the challenge that this poses is nothing less than a game-changer for etch and deposition, according to Applied Materials' Vice President, Advanced Technology Group Etch Business Unit, Bradley Howard.

"Historically, if you look at how scaling has gone, it has been limited by lithography on getting to the next node down, now we getting to the point where scaling is being driven by deposition and etching because as the scaling is now going in a vertical direction you've eased out the design rules," he said. The reality is that lithography is still important, Howard said, listing off control, good uniformity and other factors. 'Everything that you had to have from lithography before still needs to be there but it just does not need to be the limiting factor for scaling."

High aspect ratios present lots of challenges. Standard photolithography will not hold up for the long etches required for etching such deep features so hard mask layers are needed. "Depositioning is transitioning from single layer depositions in typically thinner films to multilayer stacks where you go and deposit alternating stacks of films and then also very thick films for both device and the hard mask," said Howard.

Howard addressed the gates axis, an alternating stack of materials built up with alternating layers. "You need to have very precise control and very low defectivity. Historically, if you had a defect come in on a film it affected that bit, or that area. Now if you get a defect that gets deposited on your first layer down at the bottom it becomes a propagating defect that goes up the entire stack and it is going up in regions, which means that the defect density on deposition is becoming more important."

Howard then moved on to hard masks. "We are going to have thicker hard masks because the aspect ratios of what you are trying to etch are getting very extreme as well as the amount of depth you have to etch. Having a micron or a micron-and-a-half of hard mask is not unusual. In effect, the hard mask that you are forming is its own high aspect ratio feature and then it is forming a high aspect ratio feature below it. In addition, there are various challenges on the isolation on getting the gap filled between the features and also into these very complex three dimensional structures.

"On the etch side high aspect ratio is really the key. There are multiple features, contacts in the array, there are contacts coming out of the staircase, and 60: 1 aspect ratios are becoming the common target here.

"At the edge of the array access still has to be made at each one of the layers, so a staircase structure is made to enable different landing pads for contacts to come down. But some of the contacts – towards the top – are very shallow and the ones at the bottom are extremely deep.

"You might think it might be achieved by doing a litho step and an etch step and a litho step and an etch step

and doing that 32, 64, or whatever number of times, but what happens is that you are starting out with a feature and you etch down into the feature then you pull back the resist and then you etch again and then you pull back the resist and so you start to form your 'steps' that way and you do that as many times as you can get away with, depending on the amount of resist that you have. So, you can envision that you are trying to pull this resist back really fast. The problem is the resist is now determining the CD for the cell, so you need to have good control in place." Howard summarized the challenges as being about sequential processes for both deposition and etching, thick films – whether it be the alternating stack of films or the thick films that are done to separate out the different arrays – and, finally, defect densities – especially with deposition – which are becoming more critical than ever before because of the additive effect on the deposition.

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Trends shaping modern product delivery

Product delivery is critical to success and a competitive advantage for market leaders, and garners substantial executive attention, highlighting the strategic role that products hold in organizations. It's cross-functional, spanning executive management, sales, marketing, service, support and operations in addition to the traditional product management, development, QA and release management functions.

Companies have spread product development across various sites and teams, often in individual technology silos, factors that lead to inefficiencies relating to time management, duplication of effort and communications across teams and groups, which all extend the product development cycle.

In a survey conducted by Forrester Research on behalf of Jama, five main factors contributed to product delays:

1. Product teams often lack a clear understanding of customer needs. Unclear/changing requirements plague product delivery. Not being able to get timely feedback on possible solutions results in delays and wasted time, effort, and money.

2. Conflicting priorities caused by stakeholder disagreements put product delivery teams in an unfortunate bind. Lack of clarity about objectives, assumptions, and possible solutions leads to a lack of focus.

3. Effective collaboration spans roles, teams, and geographies. Modern products are complex, requiring a wide variety of expertise to deliver successfully. The reality of the global marketplace means that co-located development is rare; globally distributed teams are increasingly commonplace.

4. Unnecessary handoffs and delayed decisions reduce speed and impair quality. Rapid delivery is increasingly a competitive differentiator. Any delay in making decisions or obtaining feedback needlessly hampers product delivery.

5. Delivering winning products requires unprecedented collaboration across diverse roles, spanning the organization from executives to operations and from marketing to quality assurance.

To remain relevant we need to change the way we work, to be faster, manage complexity and innovate to better understand customers. There are several broad areas that can evolve product delivery within the semiconductor space:

1. **Define** - The core of development — define / build / test — needs to be solid. In addition to defining all the features and functions, take time to understand, define and share the 'why.' Why customers need this feature, what problem does it solve for them? Most importantly, define the business outcomes that we are hoping to achieve.

2. **Focus on Core Business Value** - For every initiative, find and hold true to the core business value - the absolute, essential set of deliverables that is necessary to fully realize the idea and no more. Enter into development with a strong viewpoint of what success looks like based on customer interviews, value testing, design reviews.

3. **Traceability** - Generally refers to engineering activities such as change impact analysis, compliance verification or traceback of code, regression testing and validation. But traceability also needs to link all these activities back to the business rationale and the customer need.

4. **Collaboration** - This is the layer that brings everything together – people and data. The key to enterprise collaboration is keeping it connected to the work. Structured collaboration ties the conversations and communication directly with the specific requirement or use case in question.

5. **Reuse** - Different versions of a Product often share 80-95% of the same IP. Reusing your assets will directly help you tackle product complexity. Organizations that centralize all their requirements can boost efficiency by 50% or more.

6. **Review Early and Often** - It's important to move away from long meetings going over requirements line by line. Switching that to lightweight, iterative reviews early and often to engage your team and stakeholders. Draw people in early on, then transition to value testing, then design reviews, then more formal requirements reviews.

7. **Rethink Change** - Change was a completely different beast 25 years ago. Back then we built products the same way we built buildings, following a traditional methodology. Today, there is no change, just a constant, never-ending flow of new information into product teams. Modern tools take advantage of this constant flow, and adopting tools that are inherently social eases the sharing and discussion of new information in the context of their work and in real time. ◆

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