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3D 'Pop-up' Silicon Structures P. 6

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On the cover: 3D microstructures of device-grade silicon formed using concepts similar to those in children's 'pop-up' books. Source: University of Illinois.

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The ConFab 2015

I'm delighted to announce the keynotes and other key speakers for The ConFab 2015, to be held May 19-22 at The Encore at The Wynn in Las Vegas.

Our first keynote, on Wednesday, will be Ali Sebt, President and CEO of Renesas America, who will provide his insight on monetizing the Internet of Things. He'll discuss how intelligent and connected platforms will enable new value chains based on a platform play, or an associated ecosystem play.

"What are some of the enabling technologies necessary to make IoT a reality? Come to The ConFab 2015 and find out!"

Our second keynote, on Thursday, will be Paolo Gargini, Chairman of the ITRS. The newly "re-framed" ITRS roadmap process has been extended with studies of key requirements from a system-level perspective that includes heterogeneous integration, new revolutionary devices and new ways of physical and wireless connectivity. Paolo will describe what is known as the ITRS 2.0.

Also slated to speak is Subramani Kengeri, Vice President, Global Design Solutions at GLOBALFOUNDRIES, who will talk about how the design eco-system is a critical enabler for semiconductor growth. Subi says that the rapid evolution of applications in the consumer and mobile space coupled with the emergence of the IoT are driving innovations that push the limits of power, performance, cost, and time-to-volume. At the same time, next generation SoCs are demanding stronger design and technology co-optimization solutions—some of which are optimal in main-stream technologies—to support complex design integration functions.

Lode Lauwers, Vice President Business Development, at imec will continue the IoT theme, focusing on how it is driving technology trends on system scaling and semiconductor manufacturing effectiveness. Lode says to realize the promises of an augmented, connected sustainable world, promised by the IoT, the IC industry faces significant challenges both at a distributed level, with the development of ultralow power sensor and radio technologies, as well as in the cloud, with huge computational requirements to store and process data.

Jim Feldhan, president of Semico, will present the outlook for key components of the IoT market. Wearables, electronic health care, smart home, cities and cars all promise to be high volume semiconductor markets. What will these markets look like? What are some the enabling technologies necessary to make IoT a reality? Come to The ConFab 2015 and find out! See www.theconfab.com for more info.

—Pete Singer, Editor-in-Chief

Solid State TECHNOLOGY®

Pete Singer, Editor-in-Chief
Ph: 978.470.1806,
psinger@extensionmedia.com

Shannon Davis, Editor, Digital Media
Ph: 603.547.5309
sdavis@extensionmedia.com

Ed Korczynski, Senior Technical Editor,
edk@extensionmedia.com

Jeff Dorsch, Contributing Editor

Phil Garrou, Contributing Editor

Dick James, Contributing Editor

Vivek Bakshi, Contributing Editor

Sara Ver-Bruggen, Contributing Editor,
Semiconductor Manufacturing & Design

CREATIVE/PRODUCTION/ONLINE

Spryte Heithecker, Production Manager

Yishian Yao, Media Coordinator

Nicky Jacobson, Senior Graphic Designer

Caldin Seides, Graphic Designer

Slava Dotsenko, Senior Web Developer

MARKETING/CIRCULATION

Jenna Johnson,
jjohnson@extensionmedia.com

CORPORATE OFFICERS

Extension Media, LLC
Vince Ridley, President and Publisher
vridley@extensionmedia.com

Clair Bright, Vice President and Publisher
Embedded Electronics Media Group
cbright@extensionmedia.com

Melissa Sterling, Vice President,
Business Development
msterling@extensionmedia.com

For subscription inquiries:
Tel: 847.559.7500; Fax: 847.291.4816;
Customer Service e-mail: sst@omeda.com;
Subscribe: www.sst-subscribe.com

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Web Exclusives

Applied's merger with TEL: Still a work in progress

Applied Materials reported that its proposed merger with Tokyo Electron Ltd. (TEL) is still under way, without giving a deadline or expected date of conclusion. President and CEO Gary Dickerson said the company is "making progress with regulators" and plans to "complete the merger as soon as possible." He declined to elaborate on that point, on advice of its attorneys.

http://bit.ly/1LkbMdp

SEMICON show highlights chip manufacturing in South Korea

The SEMICON Korea conference and exhibition was held in Seoul for a three-day run. The show highlighted the importance of semiconductor manufacturing in South Korea, home to two of the biggest memory chip makers in the world, Samsung Electronics and SK Hynix. (From SemiMD)

http://bit.ly/1DBsWUE

5nm node needs EUV for economics

At IEDM 2014 last month in San Francisco, Applied Materials sponsored an evening panel discussion on the theme of "How do we continue past 7nm?" Given that leading fabs are now ramping 14nm node processes, and exploring manufacturing options for the 10nm node, "past 7nm" means 5nm node processing. There are many device options possible, but cost-effective manufacturing at this scale will require Extreme Ultra-Violet (EUV) lithography to avoid the costs of quadruple-patterning. (From SemiMD)

http://bit.ly/1tFK2NA

Directed Self Assembly Hot Topic at SPIE

Jeff Dorsch reports from the SPIE Advanced Lithography Symposium in San Jose, Calif. The hottest three-letter acronym is less EUV and more DSA, as in directed self-assembly.

http://bit.ly/1K913r3

n&b news and blogs

EUVL – Remaining challenges and preview of topics for the 2015 SPIE EUVL Conference

With the 2015 SPIE Advanced Lithography (AL) conference around the corner, some people have asked me what remaining EUVL challenges need to be addressed to ensure it will be ready for mass production later this year or next. Here are Vivek Bakshi's thoughts on this topic and what he expected to hear at the conference.

http://bit.ly/1vIVPl0

Insights from the Leading Edge: Semi Industry Strategy Symposium 2015

The SEMI ISS (Industry Strategy Symposium) brings together industry leaders to share their opinions on where our industry is going. The US meeting is held each January in Half Moon Bay, CA. The new darling of the microelectronics industry is obviously the Internet of Things (IoT). Many of the speakers focused on this topic though there was far more predicting than there was hard data.

http://bit.ly/1AUyXeN

Oscar for DMD Inventor Hornbeck

Hornbeck has been awarded an Academy Award of Merit (Oscar statuette) for his contribution to revolutionizing how motion pictures are created, distributed, and viewed using DMD technology (branded as the DLP chip for DLP Cinema display technology from TI). (From SemiMD)

http://bit.ly/1w6iylM

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T Strength and Failure at the Micro- and Nanoscale—From Fundamentals to Applications
U Microstructure Evolution and Mechanical Properties in Interface-Dominated Metallic Materials
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DD Diamond Electronics, Sensors and Biotechnology—Fundamentals to Applications
EE Beyond Graphene—2D Materials and Their Applications
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WW Modeling and Theory-Driven Design of Soft Materials
XX Architected Materials—Synthesis, Characterization, Modeling and Optimal Design
YY Advanced Atomistic Algorithms in Materials Science
ZZ Material Design and Discovery via Multiscale Computational Material Science
AAA Big Data and Data Analytics for Materials Science
BBB Liquids and Glassy Soft Matter—Theoretical and Neutron Scattering Studies
CCC Integrating Experiments, Simulations and Machine Learning to Accelerate Materials Innovation
DDD Lighting the Path towards Non-Equilibrium Structure-Property Relationships in Complex Materials

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news

worldnews

EUROPE | **imec** reported a breakthrough results in directed self-assembly (DSA) process development.

USA | **GLOBALFOUNDRIES** announced a partnership with imec for joint research on future radio architectures and designs for highly integrated mobile devices and IoT applications.

ASIA | **Gigaphoton Inc.** announced that it has successfully achieved continuous operation of 140W EUV light source at 50 percent duty cycle on its prototype laser-produced plasma light sources for EUV lithography scanners.

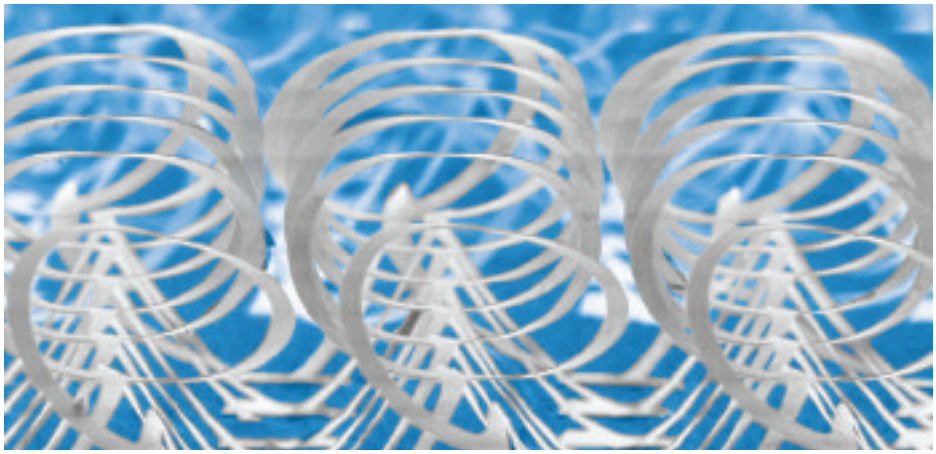
USA | **Amkor Technology, Inc.** announced that Susan Y. Kim has been appointed as a new member of the Company's Board of Directors.

EUROPE | Scientists from **Ghent University** and **imec** announced that they demonstrated interaction between light and sound in a nanoscale area. Their findings elucidate the physics of light-matter coupling at these scales – and pave the way for enhanced signal processing on mass-producible silicon photonic chips.

USA | **Micron** appointed Robert Peglar as Vice President of Advanced Storage Solutions.

ASIA | **Qualcomm Incorporated** announced that it has reached a resolution with China's National Development and Reform Commission regarding the NDRC's investigation of Qualcomm under China's Anti-Monopoly Law. Qualcomm has agreed to implement a rectification plan that modifies certain of its business practices in China and that fully satisfies the requirements of the NDRC's order.

3D 'Pop-up' silicon structures



Researchers at the University of Illinois at Urbana-Champaign have developed a unique process for geometrically transforming two dimensional (2D) micro/nanostructures into extended 3D layouts by exploiting mechanics principles similar to those found in children's 'pop-up' books.

3D microstructures of device-grade silicon formed using concepts similar to those in children's 'pop-up' books. The image shown is a colorized scanning electron micrograph. The silicon has a thickness of 2 microns.

Complex, 3D micro/nanostructures are ubiquitous in biology, where they provide essential functions in even the most basic forms of life. Similar design strategies have great potential for use in a wide variety of man-made systems, from biomedical devices to microelectromechanical components, photonics and optoelectronics, metamaterials, electronics, energy storage, and more.

Continued on page 8

Global semiconductor industry posts record sales in 2014

The Semiconductor Industry Association (SIA) announced that the global semiconductor industry posted record sales totaling $335.8 billion in 2014, an increase of 9.9 percent from the 2013 total of $305.6 billion. Global sales for the month of December 2014 reached $29.1 billion, marking the strongest December on record, while December 2014 sales in the Americas increased 16 percent compared to December 2013. Fourth quarter global sales of $87.4 billion were 9.3 percent higher than the total of $79.9 billion from the fourth quarter of 2013. Total sales for the year exceeded projections from the World Semiconductor Trade Statistics (WSTS) organization's industry forecast. All monthly sales numbers are compiled by WSTS and represent a three-month moving average.

Continued on page 10

Smartphone display manufacturers facing pressure to further reduce prices in 2015

Even as smartphone panel resolution continues to rise, and as display sizes continue to grow, panel manufacturers are facing pressure to reduce prices. According to the Quarterly Mobile Phone Display Shipment and Forecast Report from IHS, a global source of critical information and insight, total mobile phone display shipments are estimated to reach a new record high of 2 billion units in 2014. Average smartphone display prices declined nearly 14 percent year-over-year (YoY) from $22 per module in 2013 to $19 in 2014. IHS Technology forecasts another double-digit fall for smartphone display prices in 2015, resulting in a blended ASP of about $17.

Continued on page 11

KLA-Tencor extends its 5D patterning control solution with new metrology systems

KLA- Tencor Corporation introduced two advanced metrology systems that support the development and production of 16nm and below IC devices: Archer 500LCM and SpectraFilm LD10. The Archer 500LCM overlay metrology system provides accurate overlay error feedback through all stages of the yield ramp, helping chipmakers resolve overlay issues associated with innovative patterning techniques, such as multi-patterning and spacer pitch splitting. Through reliable, precise measurement of film thickness and stress, the SpectraFilm LD10 films metrology system enables qualification and

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Researchers noted that existing methods for forming 3D structures are either highly constrained in the classes of materials that can be used, or in the types of geometries that can be achieved.

"Conventional 3D printing technologies are fantastic, but none offers the ability to build microstructures that embed high performance semiconductors, such as silicon," explained John Rogers, a Swanlund Chair and professor of materials science and engineering at Illinois. "We have presented a remarkably simple route to 3D that starts with planar precursor structures formed in nearly any type of material, including the most advanced ones used in photonics and electronics. A stretched, soft substrate imparts forces at precisely defined locations across such a structure to initiate controlled buckling processes that induce rapid, large-area extension into the third dimension. The result transforms these planar materials into well-defined, 3D frameworks with broad geometric diversity."

Potential applications range from battery anodes, to solar cells, to 3D electronic circuits and biomedical devices.

"The 3D transformation process involves a balance between the forces of adhesion to the substrate and the strain energies of the bent, twisted elements that make up the planar precursors," explained Sheng Xu, a postdoctoral fellow and co-author of the research paper. "Basically, we print 2D structures onto a pre-strained elastomer substrate with selected bonding points. Releasing the substrate to its original shape induces buckling processes that lift the weakly bonded regions of the 2D structure out of contact with the surface. The resulting spatially dependent deformations occur in an ordered sequence to complete the 3D assembly."

These motions follow precisely the predictions of 3D computational models of the mechanics. These models, in turn, serve as rapid, inverse design tools for realizing a wide range of desired shapes.

Compatibility with the most advanced materials (e.g. monocrystalline inorganics), fabrication methods (e.g. photolithography) and processing techniques (e.g. etching, deposition) from the semiconductor and photonics industries suggest many possibilities for achieving sophisticated classes of 3D electronic, optoelectronic, and electromagnetic devices.

"With this scheme, diverse feature sizes and wide-ranging geometries can be realized in many different classes of materials," stated postdoctoral fellow and co-author Zheng Yan. "Our initial demonstrations include experimental and theoretical studies of more than forty representative geometries, from single and multiple helices, toroids and conical spirals, to structures that resemble spherical baskets, cuboid cages, starbursts, flowers, scaffolds, fences and frameworks, each with single and/or multiple level configurations, constructed in various materials, including semiconductors, conductors and dielectrics."

"This work establishes the concepts and a framework of understanding. We're now exploiting these ideas in the construction of high performance electronic scaffolds for actively guiding and monitoring growth of tissue cultures, and networks for 3D electronic systems that can bend and shape themselves to the organs of the human body. We're very enthusiastic about the possibilities." Rogers added.

Rogers is the director of the Frederick Seitz Materials Research Laboratory and an affiliate of the Beckman Institute for Advanced Science and Technology at Illinois. He also holds affiliate appointments in the departments of bioengineering, chemistry, electrical and computer engineering, and mechanical science and engineering. With his research teams, Rogers has pioneered flexible, stretchable electronics, creating pliable products such as cameras with curved retinas, medical monitors in the form of temporary tattoos, a soft sock that can wrap an arrhythmic heart in electronic sensors, and LED strips thin enough to be implanted directly into the brain to illuminate neural pathways. His work in photovoltaics serves as the basis for commercial modules that hold the current world record in conversion efficiency. This research was supported by the U.S. Department of Energy Office of Science.

Rick Kubetz, Engineering Communications Office, University of Illinois ◆

news cont.

Continued from page 6

"The global semiconductor industry posted its highest-ever sales in 2014, topping $335 billion for the first time thanks to broad and sustained growth across nearly all regions and product categories," said John Neuffer, president and CEO, Semiconductor Industry Association. "The industry now has achieved record sales in two consecutive years and is well-positioned for continued growth in 2015 and beyond."

Several semiconductor product segments stood out in 2014. Logic was the largest semiconductor category by sales, reaching $91.6 billion in 2014, a 6.6 percent increase compared to 2013. Memory ($79.2 billion) and micro-ICs ($62.1 billion) – a category that includes microprocessors – rounded out the top three segments in terms of sales revenue. Memory was the fastest growing segment, increasing 18.2 percent in 2014. Within memory, DRAM performed particularly well, increasing by 34.7 percent year-over-year. Other fast-growing product segments included power transistors, which reached $11.9 billion in sales for a 16.1 percent annual increase, discretes ($20.2 billion/10.8 percent increase), and analog ($44.4 billion/10.6 percent increase).

Annual sales increased in all four regional markets for the first time since 2010. The Americas market showed particular strength, with sales increasing by 12.7 percent in 2014. Sales were also up in Asia Pacific (11.4 percent), Europe (7.4 percent), and Japan (0.1 percent), marking the first time annual sales in Japan increased since 2010.

"The U.S. market demonstrated particular strength in 2014, posting double-digit growth to lead all regions," continued Neuffer. "With the new Congress now underway, we urge policymakers to help foster continued growth by enacting policies that promote U.S. innovation and global competitiveness." ◆

Continued from page 7

monitoring of the films and film stacks used in fabrication of FinFETs, 3D NAND and other leading-edge devices. The new systems are key products in KLA-Tencor's unique 5D patterning control solution, which drives optimal patterning results through the characterization and monitoring of fab-wide processes.

"As the industry leader in non-destructive optical metrology, we have closely collaborated with our customers to understand their challenges in optimizing pattern overlay, critical dimensions and films quality," stated Ahmad Khan, group vice president of KLA-Tencor's Parametric Solutions Group. "Across foundry, logic and memory, our customers require production-capable metrology systems that produce the data necessary to decipher complex process issues. Full-featured metrology systems, such as our new Archer 500LCM and SpectraFilm LD10 platforms, implement multiple innovations that facilitate measurement flexibility across a broad range of applications, helping our customers drive current-node yield and investigate next-node technologies."

With both imaging and unique laser-based scatterometry measurement technologies, the Archer 500LCM overlay metrology system offers a wide range of measurement options and supports a diverse range of overlay measurement target designs, such as in-die, small pitch and multi-layer targets. This flexibility enables cost-effective generation of accurate overlay error data that can be used for scanner corrections or for identification of inline excursions, helping engineers determine when to re-work wafers or adjust processes to meet strict patterning requirements. Multiple Archer 500LCM systems are in use at foundry, logic and memory manufacturers worldwide where they provide an independent assessment of overlay performance for advanced development and high volume production.

The SpectraFilm LD10 introduces a laser-driven plasma light source, producing reliable, high-precision film measurements for a broad range of film layers, including the thin, multilayer film stacks used in forming complex device structures such as FinFETs. Characterization of the thick, multilayer film stacks found in 3D NAND flash devices is enabled with a new infrared-based subsystem. With a significant increase in throughput compared to the previous-generation Aleris® platform, the SpectraFilm LD10 maintains high productivity while qualifying and monitoring the increased number of film layers associated with multi-patterning and other leading-edge fabrication techniques. Multiple SpectraFilm LD10 orders have been placed for use in advanced IC development and production. ◆

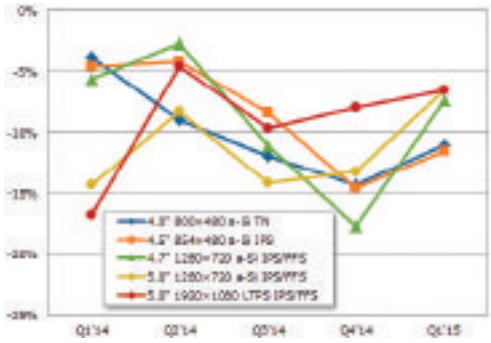
Continued from page 7

"While smartphone display resolution and sizes reach new milestones, panel makers are still being challenged to reduce display module prices," said Terry Yu, analyst for small and medium displays and display technologies for IHS Technology, formerly with DisplaySearch. "Shipment and manufacturing of panels using various display technologies like a-Si, Oxide, LTPS and AMOLED continues to rise, while pricing continues to decline. The sharpest smartphone average panel price declines occurred in 2014, and this trend of double-digit declines is expected to continue in 2015."

Panel makers (like Tianma, BOE, InfoVision, and Japan Display Inc. (JDI) via their subsidiary TDI) are all promoting their products to Chinese smartphone makers with aggressive pricing strategies. Chinese smartphone makers are agile enough to use economies of scale and their strong market position to better negotiate display prices. On the supply side, LTPS LCD manufacturing capacity is increasing in all regions. Taiwanese panel suppliers are aggressively shifting production of smartphone panels to Gen 5 fabs, as well. These factors are adding pressure to reduce prices.

According to the Monthly Smartphone and Tablet PC FPD Pricing Report, 5-inch LTPS TFT LCD FHD (1920×1080) smartphone panels with IPS/FFS LCD technology, experienced a decline of 30 percent YoY, from $30 in December 2013 to $21 in December 2014.

"Smartphone ASPs will continue to drop substantially in the first quarter of 2015, which is a traditionally slow season for smartphone display panel purchasing," Yu said.



The 5-inch 720 HD (1280×720 pixels) module is the most popular smartphone display size in China, helping the format to gain over 40 percent market share in the market global 5.x-inch space during 2014.

"Most brands are promoting low-priced, high-specification models with these displays, especially on e-commerce platforms," Yu said. "China is the major battlefield for 5-inch smartphone displays. Demand for these displays is very strong, but they face strong competitive price pressure in the set market."

In China's open market, prices for 5-inch 720HD panels declined significantly to just under $12 in December 2014. Business agreements aside, market pricing for low-specification 5.x-inch panels is expected to decline to about $11 by March 2015. Prices of some low-grade specifications panels (lower brightness requirement) could decline to below $10 by the same period.

Due to the booming demand for LTPS LCD in China, panel makers are expected to continue expanding their LTPS manufacturing capacities & shipment.

"By the end of 2016, new fab investments by AUO, BOE, China Star, Tianma, and Foxconn will result in at least five Gen 6 LTPS fabs running in China and Taiwan, which may induce more pressure to reduce smartphone ASPs in the future," Yu said.

Another price-reduction pressure in the smartphone display market comes from aggressive smartphone end-market pricing by Chinese smartphone brands. According to the Monthly Smartphone and Tablet PC FPD Pricing Report, after the introduction of the iPhone 6 Plus with its 5.5-inch FHD display, more Android-based premium models are expected to come equipped with wide-quad high-definition (WQHD) (2560×1440) displays driving FHD models down into the mid-range segment with lower pricing.

On December 23, 2014, Meizu, a rising brand in China, introduced its new "No Blue Note" smartphone, which was equipped with a 5.5-inch FHD display from Taiwan, which sells for just CNY 999 ($161). This model and pricing has been cited by many in the industry as a warning for upcoming price competition in 2015.

"Facing ASP pressures, display cost reduction will be the top priority for the panel makers, especially through more effective production yield rate management and improvements in component performance," Yu said.

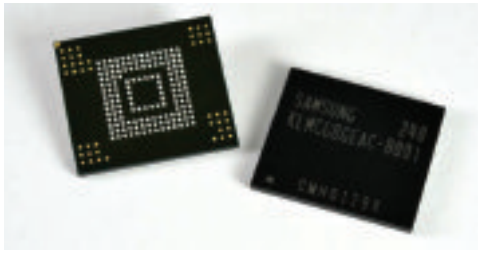
Battling over Apple

Dr. Phil Garrou,
Contributing Editor

Not since the Garden of Eden have we seen so much activity generated by an apple?

Recall, Apple signed up TSMC back in 2013 to produce its future A series processor chips while undergoing legal battles with Samsung their current provider. However, Apple has not been unable to completely disengage from Samsung. Both TSMC and Samsung produced the 22nm A8 processors for the iPhone 6, though TSMC had the majority of the order.

Now, according to South Korea's Maeil Business Newspaper, Apple has turned back to Samsung to manufacture its A9 chip. Reports are that Samsung will get 75% of the chip production for the next iPhone.



Samsung reportedly began production of Apple's A9 in their Austin TX plant using the 14nm FinFET technology. Samsung has 14nm FinFET production capability in both Austin, and Giheung, Korea, but will produce A9 only in Austin initially. I guess that this "technically" makes the chips "made in the USA."

Samsung also is putting significant pressure on Qualcomm with the pervasive rumors that Samsung will use its own microprocessors in the next version of the Galaxy S smartphone. Both Qualcomm and Samsung have declined comment.

Citing "people with direct knowledge of the matter," Bloomberg has reported that that Samsung, "… tested the new version of Qualcomm's Snapdragon chip, known as the 810, and decided not to use it". Qualcomm's Snapdragon processors, combined with its cellular baseband chips, have dominated the market for smartphones in recent years.

Qualcomm has faced rumors in recent months about potential overheating in the 810. While it is believed that Qualcomm has solved the 810's overheating problems, the issue has put Snapdragon 810 production a few months behind schedule.

Qualcomm has publically confirmed that it will no longer supply chips for a "large customer's flagship device". While the company did not confirm that this was Samsung, the firm in question is big enough for Qualcomm to lower its 2015 outlook in its first quarter fiscal financial results.

It remains possible that Qualcomm will convince Samsung that they have fixed the overheating problem and be reinserted into the Samsung phone.

Samsung mass producing high-density ePoP memory

Samsung has announced that the company will be mass producing the extremely thin ePoP (embedded package on package) memory, a single memory package consisting of 3GB LPDDR3 DRAM, 32GB eMMC and a controller for use in high-end smartphones (see photo).

The 3GB LPDDR3 mobile DRAM inside the ePoP operates at an I/O data transfer rate of 1,866Mb/s, with a 64-bit I/O bandwidth.

Because of its "thinness and special heat-resistant properties," Samsung claims that the smartphone ePoP does not need any space beyond the 225 square millimeters (15 x 15mm x 1.4mm high) taken up by the mobile application processor. A conventional PoP (also 15 x 15mm), consisting of the mobile processor and DRAM, along with a separate eMMC (11.5mm by 13mm multimedia card) package, takes up 374.5 square millimeters. Replacing that set-up with a Samsung ePoP reportedly decreases the total area used by approx. 40%.

Samsung is basically stacking all the memory, both RAM and NAND, on a single ePoP module that's then positioned on top of the processor, rather than beside it.

The use of such ePoP chips seems to be a likely choice for the upcoming Galaxy S6. It is intended to be used in mobile devices packing 64-bit processors and 3GB of RAM which is what's rumored to be spec'ed in the Galaxy S6 and other top mobile devices later this year. ◆

Packaging

Proponents of EUV, immersion lithography face off at SPIE

Jeff Dorsch,
Contributing Editor

The two main camps in optical lithography are arrayed for battle at the SPIE Advanced Lithography Symposium in San Jose, Calif.

Extreme-ultraviolet lithography, on one side, is represented by ASML Holding, its Cymer subsidiary, and ASML's EUV customers, notably Intel, Samsung Electronics, and Taiwan Semiconductor Manufacturing.

On the other side is 193i immersion lithography, represented by Nikon and its customers, which also include Intel and other leading chipmakers.

There are other lithography technologies being discussed at the conference, of course. They are bit players in the drama, so to speak, although there is a lot of discussion and buzz about directed self-assembly technology this week.

ASML broke big news on Tuesday morning, reporting that Taiwan Semiconductor Manufacturing was able to expose more than 1,000 wafers in one day this year with ASML's NXE:3300B EUV system. "During a recent test run on an NXE:3300B EUV system we exposed 1,022 wafers in 24 hours with sustained power of over 90 watts," Anthony Yen, TSMC's director of research and development, said at SPIE.

While ASML was obviously and justifiably proud of this milestone, after achieving its 2014 goal of producing 500 wafers per day, it cautioned that more development remains for EUV technology.

"The test run at TSMC demonstrates the capability of the NXE:3300B scanner, and moves us closer to our stated target of sustained output of 1,000 wafers per day in 2015," ASML's Hans Meiling, vice president service and product marketing EUV, said in a statement. "We must continue to increase source power, improve system availability, and show this result at multiple customers over multiple days."

The day before, Cymer announced the first shipment of its XLR 700ix light source, which is said to improver scanner throughput and process stability for manufacturing chips with 14-nanometer features. The company also debuted DynaPulse as an upgrade option for its OnPulse customers. The XLR 700ix and DynaPulse together are said to offer better on-wafer critical dimension uniformity and provide stable on-wafer performance.

Another revelation at SPIE is that SK Hynix has been working with the NXE:3300, too, and is pleased with the system's capabilities. According to Chang-Moon Lim, who spoke Monday morning, SK Hynix was recently able to expose 1,670 wafers over three days, with uptime of 86.3 percent over that period.

"Progress has been significant on various aspects, which should not be overshadowed by the delay of [light] sources," he said of ASML's EUV systems.

The Korean chipmaker is exploring how it could work without pellicles on the EUV reticle, Lim noted. ASML has been developing a pellicle, made with polycrystalline silicon, in cooperation with Intel and others.

Nikon Precision and other Nikon subsidiaries didn't issue any press releases at SPIE. The companies presented much information at Sunday's LithoVision 2015 event, held at the City National Civic auditorium, across the street from the San Jose Convention Center, where SPIE Advanced Lithography is staged.

On offer at the Nikon conference was the claimed superiority of 193i immersion lithography equipment to EUV systems for the 14nm, 7nm and future process nodes. Donis Flagello, Nikon Research Corp. of America's president, CEO, and chief operating officer, emphasized that message on Tuesday morning with an invited paper on "Evolving optical lithography without EUV."

Nikon's champion machine is the NSR-S630D immersion scanner, which was touted throughout the LithoVision event. The system is capable of exposing 250 wafers per hour, according to Nikon's Yuichi Shibazaki.

Semiconductors

Changes and challenges abound in multi-patterning lithography

JEFF DORSCH, *contributing editor*

Multi-patterning lithography is a fact of life for many chipmakers. Experts in the fields of electronic design automation and lithography address the issues associated with the technology. Providing responses are David Abercrombie, Design for Manufacturing Program Manager, Mentor Graphics; Gary Zhang, Vice President Marketing, ASML Brion; and Dr. Donis Flagello of Nikon Research Corporation of America.

1. What are the significant considerations in semiconductor manufacturing and design with multi-patterning lithography?

David Abercrombie: Like most process/design trade-offs moving from one node to another it comes down to cost vs area and performance. Without multi-patterning or EUV you will struggle do design at 20nm or below limiting the opportunity to take advantage of design area and performance scaling. Essentially, Moore's Law slows to a crawl without it. Multi-patterning affects almost all aspects of design and manufacturing. For physical design it adds additional design rule constraints and constrains cell placement and routing depending on cell architecture. For electrical design it adds additional parasitic variability to consider in timing analysis. For DFM it adds additional requirements for fill and lithographic checking. In manufacturing it adds additional masks, process steps and increases stepper utilization. All of these increase complexity and have an associated cost. It ultimately has to make business sense. Because of this you are seeing fewer companies moving to these advanced nodes as quickly as before, as they must have the volume and profit margins to justify the increased cost. Fortunately, there are products that do need the newest and most advanced process nodes, and because of those needs we continue to move forward into these new technology nodes on a regular schedule.

Gary Zhang: Multiple patterning (MPT) using immersion lithography is required for the semiconductor industry to continue device scaling until extreme ultraviolet (EUV) comes into full production (EUV is expected for a mid-node insertion in the 10nm logic node, and for 7nm node development and production in the 2015-2017 time frame). Multiple-patterning lithography brings the following new challenges from design to manufacturing. ASML has been collaborating with the chipmakers in a holistic lithography framework to tackle these challenges with innovative hardware and software solutions, including scanner systems, computational lithography, metrology and process control.

Integrated circuit designs have to be multiple patterning compatible. Industry has been developing methods to enable MPT-compatible designs via layout decomposition (coloring) and conflict resolution using multiple patterning rules as constraints. This applies to standard-cell libraries, cell boundaries,

JEFF DORSCH *is a contributing editor for Solid State Technology.*

and placement and route to ensure full chip layouts meet all manufacturing requirements and can be decomposed into separate masks without any post-coloring MPT conflicts. Structured layouts with highly restricted design rules seem to be a key enabler for MPT-compliant designs.

The rule-based approach to MPT compatible designs tends to run the risk of pattern defects from design hot spots, especially when design rules are pushed aggressively for competitive die size. The lithography process window of these design hot spots can be enlarged using source-mask optimization (SMO). Brion's Tachyon SMO has been routinely used to co-optimize scanner optics such as illumination source and projection lens wavefront and mask enhancements including sub-resolution assist features (SRAF) and optical proximity correction (OPC) for any given designs. Take triple patterning of a 10nm node metal layer as an example. Tachyon SMO enables a 23% larger process window for the selected SRAM and logic designs (**FIGURE 1**). By evaluating a range of design variations, SMO can help optimize design rules and MPT coloring rules to eliminate design hot spots in the technology development stage. For production mask data preparation, Brion's multiple patterning OPC and LMC (Lithography Manufacturability Check) are widely used by the leading chipmakers to deliver the best full chip process window in wafer manufacturing. A combination of SMO, OPC and LMC makes up ASML's process window enhancement solutions to the design hot spot problem.

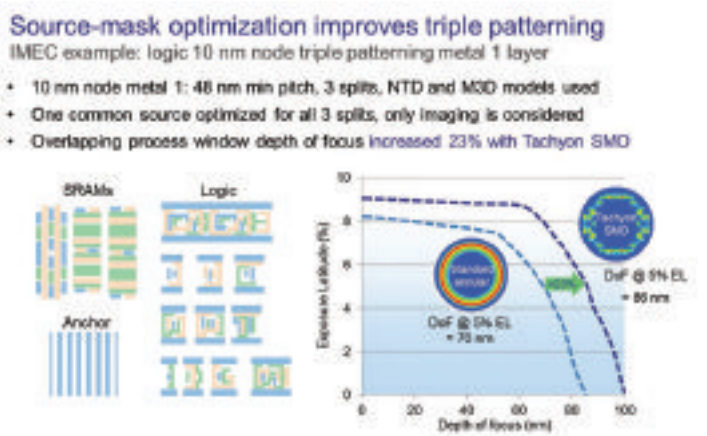


FIGURE 1. Source-mask optimization (SMO) of a 10 nm node metal layer in triple patterning lithography. Overlapping process window of all three splits (masks) is improved by 23% for selected SRAM and logic patterns imaged with the same illumination setup. Source: ASML.

Multiple patterning drives tighter CD, focus and overlay requirements to account for more process variations from the additional processing steps. Overlay is used here as an example to show the increasing complexity in multiple patterning process control from single exposure at 28nm node, to double patterning at 14nm node, to triple patterning at 10nm node (**FIGURE 2**). Tighter overlay specification has to be met for the exponentially increasing number of critical masks and metrology steps at 14nm and 10nm nodes. To deliver the required overlay control on product wafers, scanner matching and process control have to include high order corrections (**FIGURE 3**). ASML's latest generation of immersion scanners have a large number of flexible actuators and are capable of sub-3 nm matched-machine overlay, dynamic lens heating and reticle heating corrections, and high-order interfield and intrafield corrections for imaging, focus and overlay.

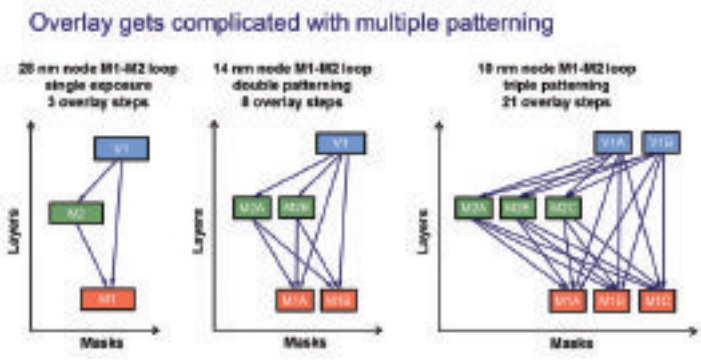


FIGURE 2. A comparison of overlay metrology and control for single exposure at 28 nm node, double patterning at 14 nm node and triple patterning at 10 nm node, using the Metal 1 (M1) to Metal 2 (<2) process loop as an example. Source: ASML.

With the introduction of multiple patterning below 28 nm node, the increasing number of masks and metrology steps translates to lower wafer throughput per scanner and longer wafer cycle time from start to finish. This then leads to cost per wafer significantly higher than the historical cost scaling trend from the previous technology nodes. ASML has been continuously driving the scanner innovation to increase the throughput and improve productivity in terms of wafer output per day. ASML's YieldStar integrated metrology is another innovative solution to reduce wafer cycle time and improve

on-product performance for effective productivity gain and overall cost benefit.

In summary, a full suite of design and manufacturing solutions are required to address the new challenges in multiple-patterning lithography. ASML has taken a holistic approach and worked in close collaboration with the chipmakers to optimize design, scanner, mask and process control altogether for the best manufacturability and yield. **FIGURE 4** gives an example on how holistic lithography enables focus roadmap down to 1x nm node. In the design phase, process window enhancement solutions such as SMO, OPC and LMC are used to eliminate the design hot spots and maximize the full chip process window. In the wafer manufacturing phase, process window control solutions such as scanner matching and high order corrections are implemented to optimize CD, overlay and focus control dynamically from tool to tool, field to field, wafer to wafer and lot to lot. A combination of the largest process window and the tightest process control delivers the most robust manufacturability and yield in volume production.

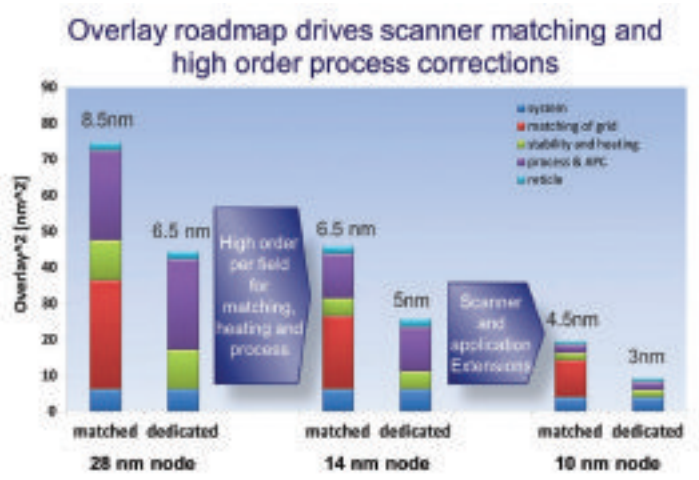


FIGURE 3. On-product overlay roadmap showing the ever tighter specification from 28 nm node to 14 and 10 nm nodes and the requirement of advanced scanner correction capabilities (such as dynamic and high-order).Two different production scenarios are considered, namely scanner/chuck dedication and mix and match of different scanners. Source: ASML.

Donis Flagello: Multiple patterning brings a host of issues due to the added complexity associated with imaging and processing multiple patterns within the same design layer. From the exposure tool point of view, we need to ensure that the overall cost of ownership is maintained and the tool can enable further scaling. We are concentrating on many aspects of the technology. One of the most critical is overlay. This must be as low as possible such that the ensemble overlay of all the exposures within a layer is equal or better than a single exposure. Simultaneously, we need to increase the throughput of the tools to ensure that cost per wafer per hour is also continuously improved. Both of these aspects drive a huge amount of innovation and technology development.

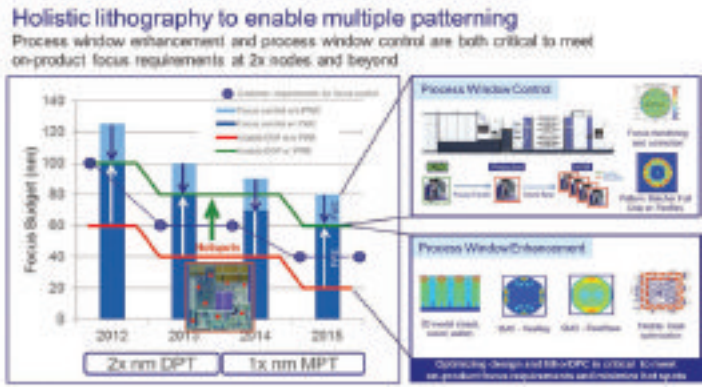


FIGURE 4. An example of how holistic lithography enables focus roadmap down to 1x nm node (DPT: double patterning; MPT: multiple patterning). A combination of process window enhancement and process window control solutions delivers robust manufacturability and yield in volume production. Source: ASML.

2. How do you deal with color assignment?

Abercrombie: The answer to that depends on the foundry and layer being discussed. Colorless, partial coloring and full coloring flows exist. In colorless flows the designer does not assign colors. There are specialized checks (like odd cycle checks in double patterning) that make sure the layout can be decomposed into multiple masks later once the design is taped-out to the foundry. In a partial coloring flow most of the layout follows the colorless flow, but the designer can manually assigns some parts of the layout to a particular color to manage subtle variation concerns. For instance, making sure matched circuitry also has matched coloring. In a fully colored flow the designer is responsible for producing the final mask assignments for all polygons in the layer. A GDS layer is

dedicated to each mask. To assign a polygon to a given mask a copy of it is placed on the appropriate mask color layer. EDA companies provide various automation capabilities to assist with color assignment in custom, P&R and batch full chip applications.

It is best to use an EDA solution like Calibre that not only can address all different coloring flows but also provides the same checks/algorithms for all phases a design goes through from initial IP blocks to final full chip signoff.

Zhang: Layout decomposition or coloring has to deliver split patterns on separate masks which are free of any process rule violations and can then be patterned in single exposure with sufficient process window. A double patterning (DPT) using a litho-etch-litho-etch process is shown as an example (**FIGURE 5**). In the DPT coloring step, any non-native color conflicts are resolved in a layer aware implementation with stitches that are properly located away from the overlap region between layers (such as a metal line contacting a via) and have the least impact on the device performance and manufacturing yield. Process robust stitching must have sufficient overlap margin to tolerate misalignment between the exposures of the split masks. This is the concept of overlay aware stitching.

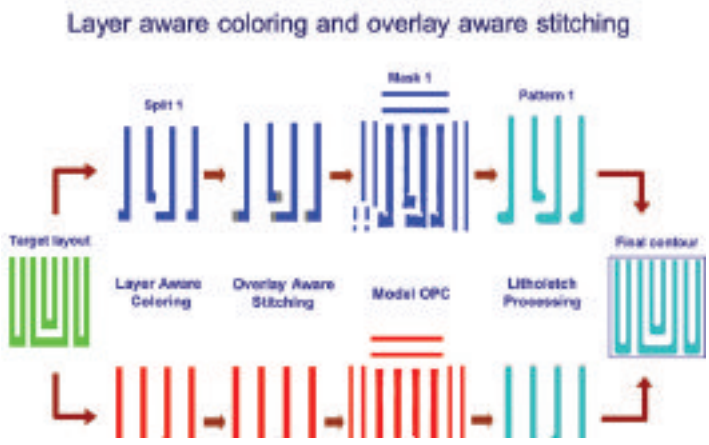


FIGURE 5. An example of design to manufacturing work flow for a litho-etch-litho-etch double patterning (DPT) process, from layer aware coloring to overlay aware stitching, to model based OPC, to the final contour after litho and etch processes. Source: ASML.

Color balancing is another critical care-about in layout decomposition. MPT coloring not only needs to deliver split layouts free of MPT conflicts but also has to ensure the pattern density is balanced between the split masks. Color balancing is beneficial for litho and etch process control so that robust and uniform patterning qualities can be achieved.

Coloring can also be optimized for best process window using a model based approach, as described above in the "Design hot spots" section. Model-based coloring is not suitable for full chip application. It can be either used in source-mask optimization for MPT rule development or applied in local hot spot fix during the mask data preparation.

3. How does design rule check change? How is it the same?

Abercrombie: In a fully colored flow the design rules change slightly. First for every traditional spacing check there are essentially two checks for double patterning (DP): a minimum spacing for different colored polygons, and a larger minimum spacing for same colored polygons. In addition, there are usually additional density checks making sure the ratio between the colors is reasonably equal. In colorless flows specialized new checks have been developed to verify if a valid coloring exists for a given layout construct. In double patterning these specialized checks include odd cycle checks. For triple patterning (TP) and quadruple patterning (QP) new types of checks are required.

Zhang: Triple patterning (TPT) coloring is a lot more difficult and complex than DPT coloring. It is extremely hard to determine if a layout is TPT compatible, known as NP-complete problem in graph theory. There is no efficient way to find a solution on the full chip level. There are no existing methods for determining the number of conflicts and their locations.

Stitches are color-dependent in TPT and candidate stitch locations can be determined only after or during coloring.

Therefore it is important to ensure TPT compliance by design construct.

4. What are the complexities and issues in transitioning from double-patterning to triple-patterning?

Abercrombie: Although checking and decomposing a layout for two colors is complex, the algorithmic processing scales reasonably by design size. However, the generalized solution for triple and quadruple patterning has exponentially increasing run time as the number of polygons processed increases. This is, of course, is not a practical solution. So the problem must be constrained such that reasonable heuristic algorithmic approaches can be applied that provide reasonably scalable run times. So the complete set of design rules and design methodology need to be properly tuned to constrain the graph-complexity of the layouts produced so these checking and decomposition heuristic tools can be utilized. In addition, specialized checks may be needed so that layout constructs that do not meet the complexity constraints can be diverted from processing (to keep run time from exploding) and flagged to the user for modification until they can be properly processed.

The other challenge in moving from DP to TP and QP is colorless error visualization. If you are doing a colorless flow and need to check if the design can legally be colored, you need a way to highlight constructs for which no valid coloring solution exists in a way that the designer can understand so he/she can make changes in the layout to fix it. For DP this was odd cycle error visualization. An even-numbered cycle of interacting polygons can be colored and an odd numbered cycle of interacting polygons cannot. For TP and QP this is not the case. Any simple even or odd cycle can be colored. The constructs which cannot be colored are much more complex than in DP. In addition, narrowing down the implicated constructs to the "root" of the problem is more difficult. To address these issues Mentor Calibre is developing a new array of error visualization layers to help inform and guide the user to appropriate and productive fixes.

Flagello: Years ago many industry observers did not believe that double patterning was viable. Today double and triple patterning is being done. However, there are some key differences between the two. Depending on the technology used, double exposure from a tool perspective is more or less straightforward. Mask alignment is usually based on the previous layer mark. However, moving to triple exposure often results in much more of an optimization problem to determine the best alignment strategy. Sometimes, the previous layer alignment mark may have a poor signal depending on the number of films involved in the multiple-patterning schemes. While increasing the number of patterning steps increases some of the complexity, the solutions become more of an optimization and controls challenge.

5. What issues in IC design and verification emerge with multi-patterning?

Abercrombie: The designer should expect to see new design rules, more parasitic variation, more complexity in design and methodology constraints, increased wafer cost, and the need for new EDA tools and additional CPU hardware to process their designs. This is really not new as this increased complexity and cost has existed between every node transition. The difference is that the delta may be more than between previous nodes. It is important that design teams educate themselves early on the impacts of moving to multi-patterned process nodes. That includes getting information from the foundry and EDA partners as well as reading available material on the subject.

Zhang: In addition to the power, performance and area metrics, designers now have to ensure their IC designs are MPT compliant and free of design hot spots so that they can be manufactured cost effectively with the best yield using multiple-patterning lithography. From lithography point of view, design hot spots are the major yield detractor. Device performance such as RC timing delay, cross talk, leakage (such as IDDQ), breakdown voltage and final yield is heavily influenced by MPT process variations. Brion's LMC has been used to evaluate the impact of realistic dose, focus, mask and overlay variations on MPT hot spots both intra-layer and interlayer. Identification of such MPT hot spots helps drive design and OPC improvements so that they can be eliminated in wafer manufacturing. ◆

Supplier Hub answers the needs of a changing semiconductor industry

LUC VAN DEN HOVE, *imec, Leuven, Belgium*

Supplier Hub answers the needs of a changing semiconductor industry

Our semiconductor industry is a cyclical business, with regular ups and downs. But we have always successfully rebounded, with new technologies that have brought on the next generation of electronic products. Now however, the industry stands at an inflection point. Some of the challenges to introduce next generation technologies are larger than ever before. Overcoming this point will require, in our opinion, a tighter collaboration than ever. To accommodate that collaboration, we have set up a new Supplier Hub, a neutral platform where researchers, IC producers, and suppliers work on solutions for technical challenges. This collaboration will allow the industry to overcome the inflection point and to move on to the next cycle of success, driven by the many exciting application domains that appear on the horizon.

Call for a new collaboration model

The formulas for the industry's success have changed. Device structures are pushing the limits of physics, making it challenging to continue progressing according to Moore's Law. Intricate manufacturing requirements make process control ever more difficult. Also chip design is more complex than ever before, requiring more scrutiny, analysis and testing before manufacturing can even begin. And the cost of manufacturing equipment and setting up a fab has risen exponentially, shutting out many smaller companies and forcing equipment and material suppliers to merge.

In that context, more and more innovation is coming from the supplier community, both from equipment and material suppliers. But as processes are approaching some fundamental limits, such as material limits, chemical, physical limits, it is also for suppliers becoming more difficult to operate and develop next-generation process steps in an isolated way. An earlier and stronger interaction among suppliers is needed.

All this makes a central and neutral platform more important than ever. That insight and the requests we got from partners set imec on the path to organizing a supplier hub. A hub that is structured as a neutral, open innovation R&D platform, a platform for which we make a substantial part of our 300mm cleanroom floor space available, even extending our facilities. It is a platform where suppliers and manufacturers collaborate side-to-side with the researchers developing next-generation technology nodes.

Organizing the supplier hub is a logical evolution in the way we have always set up collaborations with and between companies that are involved in semiconductor manufacturing. Collaborations that have proven very successful in the previous decade and that have resulted in a number of key innovations.

Supplier Hub off to a promising start

Today, both in logic and in memory, we are developing solutions to enable 7nm and 5nm technology

LUC VAN DEN HOVE *is president and CEO of imec, Leuven, Belgium*

nodes. These will involve new materials, new transistor architectures, and ever shrinking dimensions of structures and layers. At imec, the bulk of scaling efforts like these used to be done in collaborative programs involving IDMs and foundries, but also the fabless and fablite companies. All of these programs were strongly supported by our partnerships with the supplier community.

But today, to work out the various innovations in process steps needed for future nodes, we simply need this stronger and more strategic engagement from the supplier community, involving experimenting on the latest tools, even if they are still under development. And vice-versa, the tool and material suppliers can no longer only develop tools based on specs documents. To fabricate their products successfully and on time, they need to develop and test in a real process flow, and be involved in the development of new device concepts, to be able to fabricate tools and design process steps that match the requirements of the new devices.

A case in point: it is no longer possible now to develop and asses the latest generation of advanced litho without matching materials and etch processes. And reversely, the other tool suppliers need the result of the latest litho developments. So today, all process steps have to be optimized concurrently with other process steps, integrating material innovations at the same time. And this is absolutely necessary for success.

So that's where the Supplier Hub enters.

In 2013, imec announced an extended collaboration with ASML, involving the set up an advanced patterning center, which will grow to 100 engineers. In 2014, the new center was started as the cornerstone of the supplier hub. Mid 2014, Lam Research agreed to partake in the hub. And since then a growing number of suppliers has been joining, among them the big names in the industry. Some of more recent collaborations that we announced e.g. were Hitachi (CD-SEM metrology equipment) and SCREEN Semiconductor Solutions (cleaning and surface preparation tools).

End of 2014, ASML started installing its latest EUV-tool, the NXE:3300. In the meantime, we have initiated building a new cleanroom next to our existing 300mm infrastructure. The extra floor space will be needed to accommodate all the additional equipment that will come in in the frame of the tighter collaboration among suppliers. Finally, during our October 2014 Internal Partner Conference, we organized a first Supplier Collaboration Forum where the suppliers discussed and evaluated their projects with all partners, representing a large share of the semiconductor community.

We have also been expanding the supplier hub concept through a deeper involvement of material suppliers. These will prove a cornerstone of the hub, as many advances we need for scaling to the next nodes will be based on material innovations.

Enabling the Internet-Of-Everything

I hold great optimism for the industry. The last years, the success of mobile devices has fueled the demand for semiconductor-based products. These mobile applications will continue to stimulate data consumption, going from 4G to 5G as consumers clamor for greater data availability, immediacy, and access. Beyond the traditional computing and communications applications loom new markets, collectively called the 'Internet of Everything.'

In addition, nanoelectronics will enable disruptive innovations in healthcare to monitor, measure, analyze, predict and prevent illnesses. Wearable devices have already proven themselves in encouraging healthier lifestyles. The industry's challenge is now to ensure that the data delivered via personal devices meet medical quality standards. In that frame, our R&D efforts will continue to focus on ultra-low-power multi-sensor platforms.

While there are many facets to the inflection point puzzle, the answers of the industry begin to take shape. The cost of finding new solutions will keep on rising. Individual companies carry ever larger risks if their choices prove wrong. But through closer collaboration, companies can share that risk while developing solutions, exploring and creating new technologies, shorten times to market, and be ready to bring a new generation of products to a waiting world. The industry may indeed stand at an inflection point, but the future is bright. Innovation cannot be stifled. And collaboration remains the consensus of an industry focused on the next new thing. Today, IC does not just stand for Integrated Circuit, it indeed calls for Innovation and Collaboration.

Advanced analytics for yield improvement and zero defect in semiconductors

ANIL GANDHI, PH. D. *and* **JOY GANDHI**, *Qualicent Analytics, Inc., Santa Clara, CA*

Machine learning based advanced analytics for anomaly detection offers powerful techniques that can be used to achieve breakthroughs in yield and field defect rates.

In the last few decades, the volume of data collected in semiconductor manufacturing has grown steadily. Today, with the rapid rise in the number of sensors in the fab, the industry is facing a huge torrent of data that presents major challenges for analysis. Data by itself isn't useful; for it to be useful it must be converted into actionable information to drive improvements in factory performance and product quality. At the same time, product and process complexities have grown exponentially requiring new ways to analyze huge datasets with thousands of variables to discover patterns that are otherwise undetected by conventional means.

In other industries such as retail, finance, telecom and healthcare where big data analytics is becoming routine, there is widespread evidence of huge dollar savings from application of these techniques. These advanced analytics techniques have evolved through computer science to provide more powerful computing that complements conventional statistics. These techniques are revolutionizing the way we solve process and product problems in the semiconductor supply chain and throughout the product lifecycle. In this paper, we provide an overview of the application of these advanced analytics techniques towards solving yield issues and preventing field failures in semiconductors and electronics.

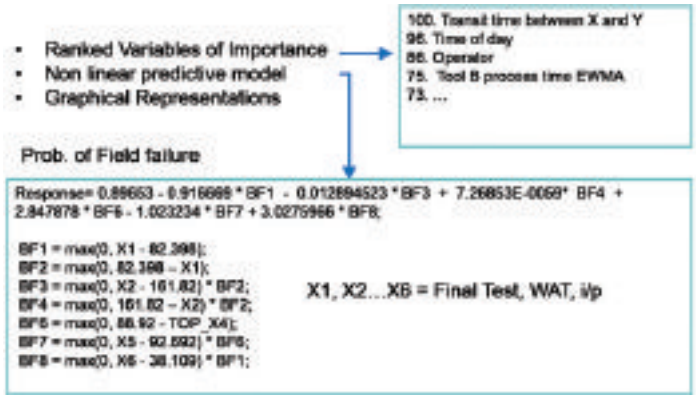


FIGURE 1. Predictive model example.

Advanced data analytics boosts prior methods in achieving breakthrough yields, zero defect and optimizing product and process performance. The techniques can be used as early as product development and all the way through high volume manufacturing. It provides a cost effective observational supplement to expensive DOEs. The techniques include machine learning algorithms that can handle hundreds to thousands of variables in big or small datasets. This capability is indispensable at advanced nodes with complex fab process

ANIL GANDHI, PH. D. *is President and Data Scientist and* **JOY GANDHI** *is chief marketing officer at Qualicent Analytics, Inc., Santa Clara, CA.*

technologies and product functionalities where defects become intractable.

Modeling target parameters

Machine learning based models provide a predictive model of targets such as yield and field defect rates as functions of process, PCM, sort or final test variables as predictors. In the development phase, the challenge is to eliminate major systematic defect mechanisms and optimize new processes or products to ensure high yields during production ramp. Machine learning algorithms reduce the number of variables from hundreds to thousands to the few key variables of importance; this reduction is just sufficient to allow nonlinear models to be built without over fitting. Using the model, a set of rules involving these key variables are derived. These rules provide the best operating conditions to achieve the target yield or defect rate. **FIGURE 1** shows an example non-linear predictive model.

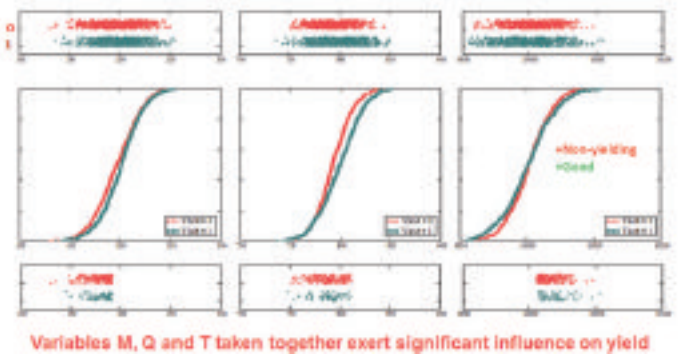


FIGURE 2. Individual parameters M, Q and T do not exert influence while collectively they create conditions that destroy yield. Machine learning methods help discover these conditions.

FIGURE 2 is another example of rules extracted from a model, showing that when all conditions of the rule are valid across the three predictors simultaneously, then this results in lower yield. Discovering this signal with standard regression techniques failed because of the influence of a large number of manufacturing variables. Each of these large number of variables has a small and negligible influence individually, however they all combine to create noise and thus masking the signal. Standard regression techniques, available in commercial software, therefore are unable to detect the signal in these instances and therefore are not of practical use for process control. So how do we discover the rules such as the ones shown in Fig. 2?

Rules discovery

Conventionally, a parametric hypothesis is made based on prior knowledge (process domain knowledge) and then the hypothesis is tested. For example to improve an etest metric such as threshold voltage one could start with a hypothesis that connects this backend parameter with RF power on an etch process in the frontend. However many times it is impossible to make a hypothesis based on domain knowledge because of the complexity of the processes and the variety of possible interactions, especially across several steps. So alternatively, a generalized model with cross terms is proposed and then significant coefficients are picked and the rest are discarded. This works if the number of variables is small but fails with large number of variables. With 1100 variables (a very conservative number for fabs) there are 221 million possible 3-way interactions, and 60 million 2-way cross terms on top of the linear coefficients!

Fitting these coefficients would require a number of samples or records that are clearly not available in the fab. Recognizing that most of the variables and interactions have no bearing on yield, we must then reduce the feature set size (i.e. number of predictors) within a healthy manageable limit (< 15) before we apply any model to it; several machine learning techniques based on derivatives of decision trees are available for feature reduction. Once the feature set is reduced then exact models are developed using a palette of techniques such as those based on advanced variants of piece-wise regression.

In essence, what we have described above is discovery of the hypothesis, while more traditionally one starts with a hypothesis...to be tested. The example in Fig. 2 had 1100 variables most of which had no influence, six of them have measurable influence (three of them are shown), all of these were hard to detect because of dimensional noise.

The above type of technique is part of a group of methods classified as supervised learning. In

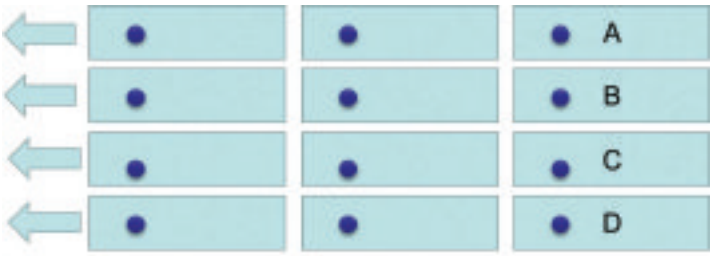


FIGURE 3. Solar manufacturing line conveyor, sampled at four points for colorimetry.

this type of machine learning, one defines the predictors and target variables and the technique finds the complex relationships or rules governing how the predictors influence the target. In the next example we include the use of unsupervised learning which allows us to discover clusters that reveal patterns and relationships between predictors which can then be connected to the target variables.

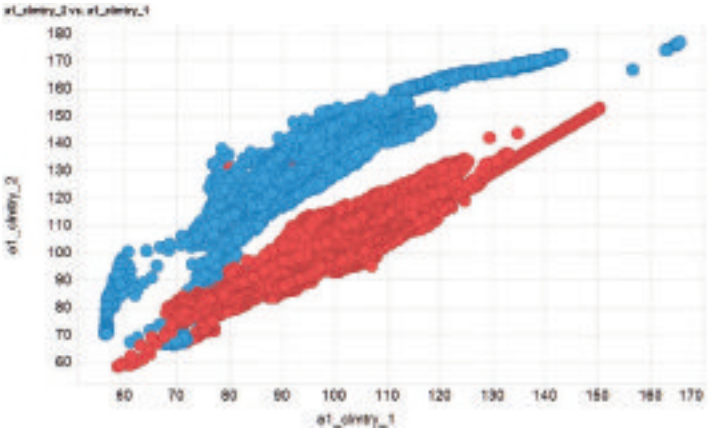


FIGURE 4. The ratios between 1, 2, 3 and 4 colorimetry were found to have clusters and the clusters corresponded to date separation.

FIGURE 3 shows a solar manufacturing line with four panels moving on a conveyor. The end measure of interest that needed improvement was cell efficiency. Measurements are made at the anneal step for each panel as shown at locations 1, 2, 3, 4 in **FIGURE 4**. The ratio between measurement sites with respect to a key metric called Colorimetry, was discovered to important; the way this was discovered was by employing clustering algorithms, which are part unsupervised learning. This ratio was found in subsequent supervised model to influence PV solar efficiency as part of a 3-way interaction.

In this case, without the use of unsupervised machine learning methods, it would have been impossible to identify the ratio between two predictors as an important variable affecting the target because this relationship was not known and therefore no hypothesis could be made for testing it among the large number of metrics and associated statistics that were gathered. Further investigation led to DATE as the determining variable for the clusters.

Ultimately the goal was to create a model for cell efficiency. Feature reduction described earlier is performed followed by advanced piecewise regression and the resulting model based on 10 fold cross validation (build model on 80% of data and test against rest 20% and do this 10 times with a different random sample each time) results in a complex non-linear model with key element that includes a 3 way interaction as shown in **FIGURE 5**, where the dark green area represents the condition that drops the median efficiency by 30% from best case levels. This condition Colorimetry < 81, Date > X and N2 < 23.5 creates the exclusion zone that should be avoided to improve cell efficiency.

Advanced anomaly detection for zero defect

Throughout the production phase, process control and maverick part elimination are key to preventing failures in the field at early life and the rest of the device operating life. This is particularly crucial for automotive, medical device and aerospace applications where field failures can result in loss of life or injury and associated liability costs.

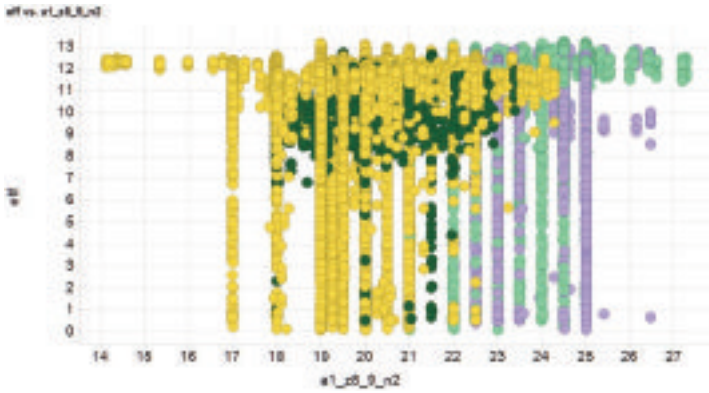


FIGURE 5. N2 (x-axis) < 23.5, colorimetry < 81 and Date > X represent the "bad" condition (dark green) where the median cell efficiency drops by 30% from best case levels.

The challenge in screening potential field failures is that these are typically marginal parts that pass individual parameter specifications. With increased complexity and hundreds to thousands of variables, monitoring a handful of parameters individually is clearly insufficient. We present a novel machine learning-based approach that uses a composite parameter that includes the key variables of importance.

Conventional single parameter maverick part elimination relies on robust statistics for single parameter distributions. Each parameter control chart detects and eliminates the outliers but may eliminate good parts as well. Single parameter control charts are found to have high false alarm rates resulting in significant scrap rates of good material.

In this novel machine learning based method, the composite parameter uses a distance measure from the centroid in multidimensional space. Just as in single parameter SPC charts, data points that are farthest from the distribution that cross the limits are maverick and are eliminated. In that sense the implementation of this method is very similar to the conventional SPC charts, while the algorithm complexity is hidden from the user.

		predicted		
		pass	fail	
actual	pass	18,413	20	18,433
	fail	6	1	7
		18,419	21	18,440

TABLE 1. Top Parameter

		predicted		
		pass	fail	
actual	pass	18,429	4	18,433
	fail	1	6	7
		18,430	10	18,440

TABLE 2. Composite Parameter

See **FIGURE 6** for a comparison of the single parameter control chart of the top variable of importance versus the composite distance chart. **TABLES 1** and **2** show the confusion matrix for these charts. With the single parameter approach, the topmost contributing parameter is able to detect 1 out of 7 field failures. We call this accuracy. However only one out of 21 declared fails is actually a fail – we call this purity of the fail class. Potentially more failures can be detected by lowering the limit somewhat, in the top chart however in that case the purity of the fail class which was already bad now balloons rapidly to unacceptable levels.

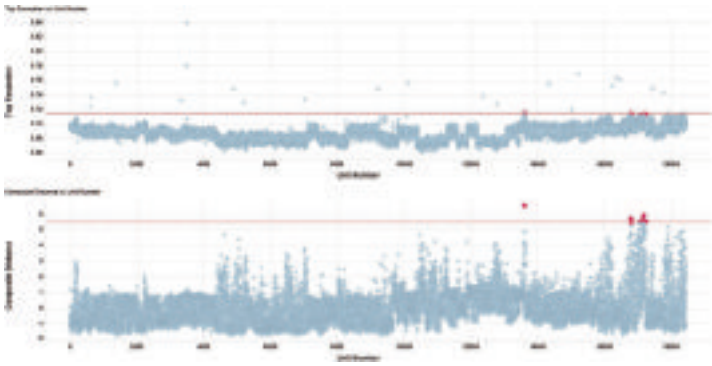


FIGURE 6. Comparison of single parameter control chart for the top parameter in the model and Composite Distance Control Chart. The composite distance method detected almost all field failures without sacrificing good parts whereas the top parameter alone is grossly insufficient.

In the composite distance method, on the other hand 6 out of 7 fails are detected – good accuracy. The cost of this detection is also low (high purity) because 6 of 10 declared fails are actually field failures – which is a lot better than 1 out of 21 in the incumbent case and significantly better if the limit in the single top parameter chart was lowered even a little.

We emphasize 2 key advantages of this novel anomaly detection technique. First, the multi-variate nature enables detection of marginal parts that not only pass the specification limits for individual parameters but also are within distribution for all of the parameters taken individually. The composite distance successfully identifies marginal parts that fail in the field. Second, this method significantly reduces the false alarm risk compared to single parameter techniques. This leads to reduction of the cost associated with the "producer's risk" or beta risk of rejecting good units. In short, better detection of maverick material at lower cost.

Summary and conclusion

Machine learning based advanced analytics for

anomaly detection offers powerful techniques that can be used to achieve breakthroughs in yield and field defect rates. These techniques are able to crunch large data sets and hundreds to thousands of variables, overcoming a major limitation with conventional techniques. The two key methods that were explored in this paper key are as follows:

Discovery – This set of techniques provides a predictive model that contains the key variables of importance affecting target metrics such as yield or field defect levels. Rules discovery (a supervised learning technique) among many other methods that we employ, discovers rules that provide the best operating or process conditions to achieve the targets. Or alternatively it identifies exclusion zones that should be avoided to prevent loss of yield and performance. Discovery techniques can be used during early production phase when there is greatest need to eliminate major yield or defect mechanisms to protect the high volume ramp. And of course the techniques are equally applicable in high volume production.

Anomaly Detection – This method based on the unsupervised learning class of techniques, is an effective tool for maverick part elimination. The composite distance process control based on Qualicent's proprietary distance analysis method provides a cost effective way for preventing field failures. At leading semiconductor and electronics manufacturers, the method has predicted actual automotive field failures that occurred in top carmakers. ◆

Imaging tomorrow's components, acoustically

TOM ADAMS, SONOSCAN, INC., *Elk Grove Village, IL*

Packages are changing. Acoustic methods provide a way to image and analyze them.

By the year 2020, the design, dimensions and materials of various electronic component packages will have changed in varying degrees from their current forms. PEMs (plastic-encapsulated microcircuits) will still be in production, but likely with shrinking sizes and better (or less expensive) encapsulants. Stacking of die connected by non-wire methods such as through-silicon vias (TSVs) will be in production. These and other package types, along with components such as ceramic chip capacitors, will need to be inspected for internal anomalies, typically by non-destructive acoustic micro imaging. This article takes a forward look at some of the challenges and changes that may take place in various packages and the possible advances in acoustic methods for imaging and analyzing them.

In electronic components, the business of acoustic micro imaging is to make visible and and analyze internal structural features. Acoustic micro imaging tools such as Sonoscan's C-SAM® series are used to image anomalies and defects, or to verify their absence. The defects are typically gaps - delaminations, voids, cracks, non-bonds and the like - but an acoustic micro imaging tool will also reveal surprises such as the out-of-place or missing die sometimes noted in counterfeit components.

New acoustic imaging methods

Today, the prevalent imaging mode for acoustic micro imaging tools is what is commonly called the Time Domain Amplitude Mode. The scanning transducer sends a pulse of VHF (5 to 100 MHz) or UHF (above 100 MHz) ultrasound into an x-y location. A few microseconds later, the transducer receives a number of echoes from the depth of interest. The amplitude of the highest-amplitude echo within a gate (time window) is used to assign a pixel value to that x-y location. The other echoes are ignored.

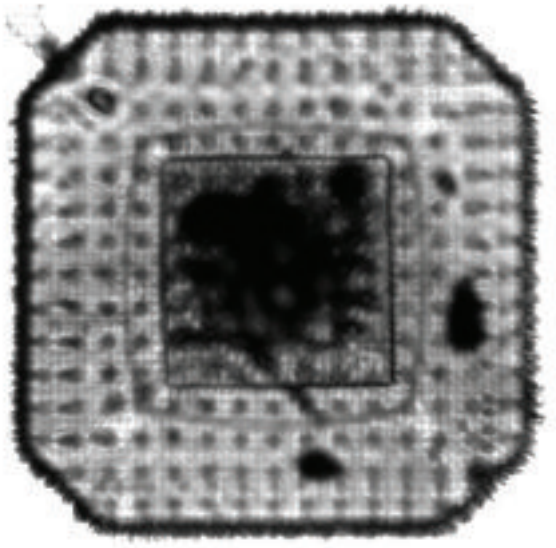


FIGURE 1. Thru-Scan image shows acoustic shadows of anomalies in a BGA package, but gives no depth information.

At the moment, there are about a dozen other imaging modes which collect data in different ways and which yield different information and images about a sample.

TOM ADAMS *is a consultant to Sonoscan, Inc., Elk Grove Village IL USA*

One example: it is important in imaging IGBT modules to measure and map the thickness of the solder bonding the heat sink to the ceramic raft above. Irregular solder thickness often means that the raft is tilted or warped (and thus may restrict heat dissipation). The Time Difference™ mode will map the interface. This mode ignores echo amplitude altogether and uses the arrival time of the echoes to measure and map the thickness of the solder. Irregular solder thickness means that the raft is tilted or warped (and thus may restrict heat dissipation). Other acoustic imaging modes use other techniques to detect thickness variations.

The Frequency Domain mode produces multiple images of the target depth in a sample. Each image is made using echoes within a very narrow frequency range (e.g., 102.0-103.5 MHz). This mode is useful in samples having subtle anomalies or defects that may be hard to discern with, say, Amplitude Mode.

A new mode is typically developed when the user of an acoustic micro imaging tool expresses the need to push acoustic imaging beyond its current capabilities in order to solve a specific inspection problem. In some instances an existing mode that was previously developed for research purposes is found to be useful for emerging sample types. It is very likely that new acoustic imaging modes will developed as electronic components and assemblies continue to evolve.

A recently developed mode is the Echo Integral Mode. It gives a view similar to, but more informative than, the Amplitude Mode. While Amplitude Mode picks the highest single amplitude to assign a pixel value, The Echo Integral Mode uses the sum of the amplitude of all the echoes at a given x-y coordinate to determine the pixel color for that coordinate. This approach makes it easier to see subtle local differences in, say, the quality of a bond between two materials.

FIGURE 1 is the Thru-Scan mode image of a plastic BGA package. Thru-Scan pulses ultrasound into the top of the package and uses a sensor beneath the package to read the amplitude of the arriving ultrasound at each x-y location. Gap-type defects block ultrasound and thus appear in a Thru-Scan image as black acoustic shadows.

In Figure 1, the black features within the die at center are surely significant anomalies, but an engineer cannot tell from this Thru-Scan image what depth they lie at: are they in the die attach material or in the substrate below?

At left in **FIGURE 2** is the Amplitude Mode image of the die area. This image is gated on (reads echoes only from) the die attach depth, and ignores echoes from other depths. The black dots are not features in the gated depth, but are the acoustic shadows of voids in the mold compound above the die. The die area itself is rather uniformly pale gray, with no features of note.

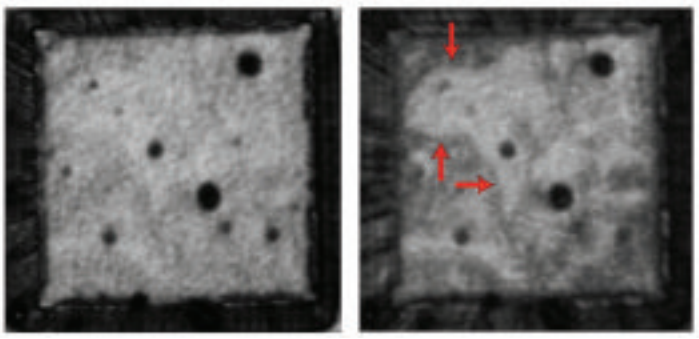


FIGURE 2. Amplitude mode (left) shows no defects, but Echo Integral Mode (right) shows locations of defects in the die attach.

The image at right used the Echo Integral Mode, also gated on the die attach material. Using the average amplitude of all the echoes at of millions of x-y coordinates gave a different result: there are significant differences in brightness. The large bright area marked by arrows is a gap-type defect in the die attach, and there are other, smaller defects of the same type. The defects imaged as black shadows by Thru-Scan are imaged here as near-white defects by the Echo Integral Mode. They are clearly in the die attach, and not in the substrate. The roughly spherical feature in the upper right of the Thru-Scan image, however, is the shadow of the void in the mold compound above the die.

Components will continue to shrink

Sonoscan's laboratories have for some time been imaging PEMs that are only 200 microns thick and 3mm x 3mm in area. The die is typically less than 100 microns thick. In some ways, the small dimensions are an advantage in acoustic imaging: the plastic encapsulant scatters and absorbs ultrasound, so the less encapsulant the pulse and the resulting echo need to

travel through, the better the resolution in the acoustic image. Such a component may be imaged with the very high frequency of 230 MHz, rather than the 15 MHz to 100 MHz of larger plastic packages. Higher frequency means better spatial resolution in the acoustic image.

One of the most commonly imaged non-PEM components is the ceramic chip capacitor, where the goal is to image delaminations and cracks that can lead to leakage between electrode layers. The very smallest ceramic chip capacitors currently being manufactured measure 0.010 inch by 0.005 inch. They can be imaged acoustically, but extremely small dimensions make imaging time-consuming.

Mid-end components

So named because they involve both front-end and back-end processes, mid-end components are typically assembled by mounting flip chips onto a wafer and then encapsulating the flip chips with plastic before dicing the wafer. They have been described as non-wired QFNs.

What has evolved is that some mid-end components can be imaged well enough to see details of the solder bump bonds, while others cannot. Sonoscan has developed transducers having an acoustic frequency that is low enough to get through the plastic encapsulant, and high enough to give good details about the bump bonds.

But many mid-end components have an encapsulant that is only partly transparent to ultrasound. Gross features and defects will be visible, but not the details of the bump bonds, which will probably become even smaller in the future. The alternative is to use the Thru-Scan™ imaging mode. Any gap in between, such as a break in a solder bump, will block the arriving ultrasound and be visible as a black feature. These acoustic shadows contain no information about the depth of a feature, but the relatively simple design along with experience with a given mid-end component are helpful.

The evolution of package design may in time alleviate the encapsulant problem. The trend is toward more chip-on-wafer type designs, and toward ever-smaller dimensions. The encapsulants may perhaps become unnecessary; their departure would enhance acoustic inspection.

Stacked die

Individual components typically have industry standards that can be used to judge the risk posed by a void in the die attach material or a delamination along a lead finger. Stacked die have no industry standards; presumably each maker of stacked die uses their own guidelines to reduce field failures.

Die stacks can be imaged acoustically before encapsulation, and in the future some may be imaged after encapsulation, particularly if ultrasound-friendly encapsulants are used. In both situations, the same problem occurs: each pulse encountering a material interface is partly reflected and partly transmitted across the interface. Unencapsulated stacks are typically imaged during development in order to refine assembly processes. Even a four-die stack (that has at least eight interfaces) can generate so many echoes that it becomes very difficult to identify the echo being sent by the delamination of the adhesive on the top of die #3.

For unencapsulated stacks, this problem has largely been solved by software developed jointly by Sonoscan and the Technical University of Dresden. The software uses material properties and dimensions to create a virtual stack as much like the physical stack as possible, and works out the imaging techniques, which are then further refined on the physical stack. The goal is to identify the echoes that were returned from specific depths of interest - e.g., the interface between the bottom surface of die #6 and the adhesive beneath it. By repeatedly moving between the virtual sample and the physical sample, the imaging parameters are defined that will show the echoes at this depth.

Nearly all memory devices are stacked, and the die are wire-bonded to each other. But there are stacks have many different configurations; one common configuration puts a small memory chip on top of a larger processing chip.

It's hard to tell where the architecture of die stacks may go from here. In some stacks, through-silicon vias (TSVs) will replace wires. Defects such as delaminations will be visible acoustically, but whether the TSVs will be visible acoustically is difficult to judge at this point. What manufacturers want to see is that each TSV is filled. Their diameters are already extremely

small. Whether acoustic methods will be devised to make them nondestructively visible is not known yet.

A long-standing problem in imaging typical PEMs is that a delamination on the back side of the die paddle cannot be imaged when scanning the top side of the PEM. Before the PEM is surface-mounted, it can simply be flipped over and imaged from the back side. After mounting, only the top surface is available for scanning. The problem is that there are too many interfaces: the pulsed ultrasound must cross the top surface of the plastic, the plastic-to-die interface, the die-to-die attach interface, and the die attach-to-die paddle interface. This is essentially the same problem encountered in the imaging of stacked die. In theory, a delamination between the die paddle and the plastic below it can be located and imaged by the software developed for die stacks.

Package-on-package

Package-on-package assemblies, such as a package containing one or more memory die on top of a package containing one or more logic die, are beginning to appear in Sonoscan's testing laboratories. These package designs have some advantages over the stacking of die; for example, if one of the two packages is found to be defective before assembly, it can be replaced, while the logic package is retained. It seems likely that the popularity of these assemblies will increase in the next few years.

After the two packages are bonded together, the chief structural reliability concern is the adhesive between the two packages. This is where gap-type defects, primarily voids, may be found. If present, voids put stress on the solder joints for the BGA balls.

How acoustic imaging is performed depends on the structure of the assembly. Normal reflection-mode pulse-echo imaging can sometimes be used, but the assembly is likely to have numerous material interfaces that could limit the effectiveness of this method. Because internal structural defects in this assembly are largely limited to voids at a specific known depth, it often makes more sense to use the Thru-Scan mode to reveal the voids.

Interposers

The term "interposer" is used rather loosely to describe a redistribution layer between a top die and a lower die or printed circuit board. chip and the solder balls that make connection with a substrate. In terms of acoustic imaging, interposers behave much like flip chips, in that the depth of interest is between two structures.

The common defects are delaminations, significant because they are capable of attracting contaminants (and thus causing corrosion) and of expanding through thermal cycling. The growth of chips having advanced processing capabilities will likely make the acoustic imaging of interposers more frequent.

Summary

The advantage of acoustic micro imaging tools is their ability to image nondestructively gap-type anomalies and certain other anomalies (tilting, warping) in electronic materials. In recent years, the original Amplitude Mode has been joined by roughly a dozen other modes that push imaging capabilities into new areas.

It can be expected that electronic components will continue to add their own capabilities and to reduce their physical dimensions. Some components will become more difficult to image; others, particularly those that become thinner or that use acoustically friendly materials, may permit the use of higher frequencies to image smaller features. Since there is no good non-destructive substitute for acoustic modes, engineers who demand reliability may want to apply acoustic micro imaging to new device configurations and keep track of new acoustic imaging modes. ◆

Consider packaging requirements at the beginning, not the end, of the design cycle

JOHN T. MACKAY, *Semi-Pac, Inc., Sunnyvale, CA*

Consider these eight issues where the packaging team should be closely involved with the circuit design team.

Today's integrated circuit designs are driven by size, performance, cost, reliability, and time-to-market. In order to optimize these design drivers, the requirements of the entire system should be considered at the beginning of the design cycle—from the end system product down to the chips and their packages. Failure to include packaging in this holistic view can result in missing market windows or getting to market with a product that is more costly and problematic to build than an optimized product.

Chip design

As a starting consideration, chip packaging strategies should be developed prior to chip design completion. System timing budgets, power management, and thermal behavior can be defined at the beginning of the design cycle, eliminating the sometimes impossible constraints that are given to the package engineering team at the end of the design. In many instances chip designs end up being unnecessarily difficult to manufacture, have higher than necessary assembly costs and have reduced manufacturing yields because the chip design team used minimum design rules when looser rules could have been used.

Examples of these are using minimum pad-to-pad spacing when the pads could have been spread out or using unnecessary minimum metal to pad clearance (**FIGURE 1**). These hard taught lessons are well understood by the large chip manufacturers, yet often resurface with newer companies and design teams that have not experienced these lessons. Using design rule minimums puts unnecessary pressure on the manufacturing process resulting in lower overall manufacturing yields.

Packaging

Semiconductor packaging has often been seen as a necessary evil, with most chip designers relying on existing packages rather than package customization for optimal performance. Wafer level and chipscale packaging methods have further perpetuated the belief that the package is less important and can be eliminated, saving cost and improving performance. The real fact is that the semiconductor package provides six essential functions: power in, heat out, signal I/O, environmental protection, fan-out/compatibility to surface mounting (SMD), and managing reliability. These functions do not disappear with the implementation of chipscale packaging, they only transfer over to the printed circuit board (PCB) designer. Passing the buck does not solve the problem since the PCB designers and their tools are not usually expected to provide

JOHN T. MACKAY *is President and CEO of Semi-Pac, Sunnyvale, CA. www.semipac.com*

FIGURE 1. In this image, the bonding pads are grouped in tight clusters rather than evenly distributed across the edge of the chip. This makes it harder to bond to the pads and requires more-precise equipment to do the bonding, thus unnecessarily increasing the assembly cost and potentially impacting device reliability.

optimal consideration to the essential semiconductor die requirements.

Packages

Packaging technology has considerably evolved over the past 40 years. The evolution has kept pace with Moore's Law increasing density while at the same time reducing cost and size. Hermetic pin grid arrays (PGAs) and side-brazed packages have mostly been replaced by the lead-frame-based plastic quad flat packs (QFP). Following those developments, laminate based ball grid arrays (BGA), quad flat pack no leads (QFN), chip scale and flip-chip direct attach became the dominate choice for packages.

The next generation of packages will employ through-silicon vias to allow 3D packaging with chip-on-chip or chip-on-interposer stacking. Such approaches promise to solve many of the packaging problems and usher in a new era. The reality is that each package type has its benefits and drawbacks and no package type ever seems to be completely extinct. The designer needs to have an in-depth understand of all of the packaging options to determine how each die design might benefit or suffer drawbacks from the use of any particular package type. If the designer does not have this expertise, it is wise to call in a packaging team that possesses this expertise.

Miniaturization

The push to put more and more electronics into a smaller space can inadvertently lead to unnecessary packaging complications. The ever increasing push to produce thinner packages is a compromise against reliability and manufacturability. Putting unpackaged die on the board definitely saves space and can produce thinner assemblies such as smart card applications. This chip-on-board (COB) approach often has problems since the die are difficult to bond because of their tight proximity to other components or have unnecessarily long bond wires or wires at acute angles that can cause shorts as PCB designers attempt to accommodate both board manufacturing line and space realities with wire bond requirements.

Additionally, the use of minimum PCB design rules can complicate the assembly process since the PCB etch-process variations must be accommodated. Picking the right PCB manufacturer is important too as laminate substrate manufacturers and standard PCB shops are most often seen as equals by many users. Often, designers will use material selections and metal systems that were designed for surface mounting but turn out to be difficult to wire bond. Picking a supplier that makes the right metallization tradeoffs and process disciplines is important in order to maximize manufacturing yields

Power

Power distribution, including decoupling capacitance and copper ground and power planes have been mostly a job for the PCB designer. This is a wonder to most users as to why decoupling is rarely embedded into the package as a complete unit. Cost or package size limitations are typically the reasons cited as to why this isn't done. The reality is that semiconductor component suppliers usually don't know the system requirements, power fluctuation tolerance and switching noise mitigation in any particular installation. Therefore power management is left to the system designer at the board level.

Thermal Management

Miniaturization results in less volume and heat spreading to dissipate heat. Often, there is no room or project funds available for heat sinks. Managing junction temperature has always been the job of the packaging engineer who must balance operating and ambient temperatures and packaging heat flow.

Once again, it is important to develop a thermal strategy early in the design cycle that includes die specifics, die attachment material specification, heat spreading die attachment pad, thermal balls on BGA and direct thermal pad attachment during surface mount.

Signal input/output

Managing signal integrity has always been the primary concern of the packaging engineer. Minimizing parasitics, crosstalk, impedance mismatch, transmission line effects and signal attenuation are all challenges that must be addressed. The package must handle the input/output signal requirements at the desired operating frequencies without a significant decrease in signal integrity. All packages have signal characteristics specific to the materials and package designs.

Performance

There are a number of factors that impact performance including: on-chip drivers, impedance matching, crosstalk, power supply shielding, noise and PCB materials to name a few. The performance goals must be defined at the beginning of the design cycle and tradeoffs made throughout the design process.

Environmental protection

The designer must also be aware that packaging choices have an impact on protecting the die from environmental contamination and/or damage. Next-generation chip-scale packaging (CSP) and flip chip technologies can expose the die to contamination. While the fab, packaging and manufacturing engineers are responsible for coming up with solutions that protect the die, the design engineer needs to understand the impact that these packaging technologies have on manufacturing yields and long-term reliability.

Involve your packaging team

Hopefully, these points have provided some insights on how packaging impacts many aspects of design and should not be relegated to just picking the right package at the end of the chip design. It is important that your packaging team be involved in the design process from initial specification through the final design review.

In today's fast moving markets, market windows are shrinking so time to market is often the important differentiator between success and failure. Not involving your packaging team early in the design cycle can result in costly rework cycles at the end of the project, having manufacturing issues that delay the product introduction or, even worse, having impossible problems to solve that could have been eliminated had packaging been considered at the beginning of the design cycle.

System design incorporates many different design disciplines. Most designers are proficient in their domain specialty and not all domains. An important byproduct of these cross-functional teams is the spreading of design knowledge throughout the teams, resulting in more robust and cost effective designs.

Techniques for Simplifying Pulsed Measurements: Part 2

DAVID WYBAN, *Keithley Instruments, a Tektronix Company, Solon, Ohio*

Common pulsed measurement challenges are defined.

For SMU and PMU users, an issue that sometimes arises when making transient pulse measurements is the presence of "humps" (**FIGURE 1**) in the captured current waveform at the rising and falling edges of the voltage pulse. These humps are caused by capacitances in the system originating from the cabling, the test fixture, the instrument, and even the device itself. When the voltage being output is changed, the stray capacitances in the system must be either charged or discharged and the charge current for this either flows out of or back into the instrument. SMUs and PMUs measure current at the instrument, not at the DUT, so the instrument measures these current flows while a scope probe at the device does not.

This phenomenon is seen most often when the change in voltage is large or happens rapidly and the current through the device itself is low. The higher the voltage of the pulse or the faster the rising and falling edges, the larger the current humps will be. For SMUs with rise times in the tens of microseconds, these humps are usually only seen when the voltages are hundreds or even thousands of volts and the current through the device is only tens of microamps or less. However, for PMUs where the rise times are often less than 1µs, these humps can become noticeable on pulses of only a couple of volts, even when the current through the device is as high as several milliamps.

Although these humps in the current waveform may seem like a big problem, they are easy to eliminate. The humps are the result of the current being measured at the high side of the device where the voltage is changing. Adding a second SMU or PMU at the low side of the device to measure current will make these humps go away because at the low side of the device the voltage does not change so there's no charge or discharge currents flowing and the current measured at the instrument will match the current at the device. If this isn't an option, this problem can be minimized by reducing the stray capacitance in the system by reducing the length of the cables. Shorter cables equal less stray capacitance, which reduces the size of the humps in the current waveform.

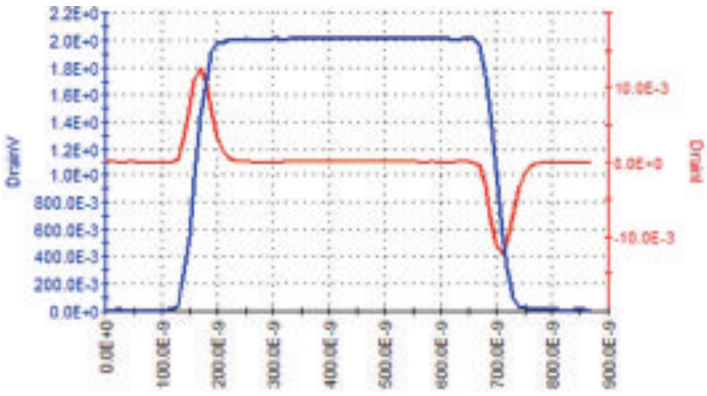


FIGURE 1. Humps in the captured current (red) waveform at the rising and falling edges of the voltage pulse.

The next common pulse measurement issue is test lead resistance. As test currents get higher, the

DAVID WYBAN *is an applications engineer at Keithley Instruments, a Tektronix Company, Solon, Ohio.*

impact of this resistance becomes increasingly significant. **FIGURE 2** shows an SMU that is performing a pulse I-V measurement at 2V across a 50mΩ load. Based on Ohm's Law, one might expect to measure a current through the device of 40A, but when the test is actually performed, the level of current measured is only 20A.

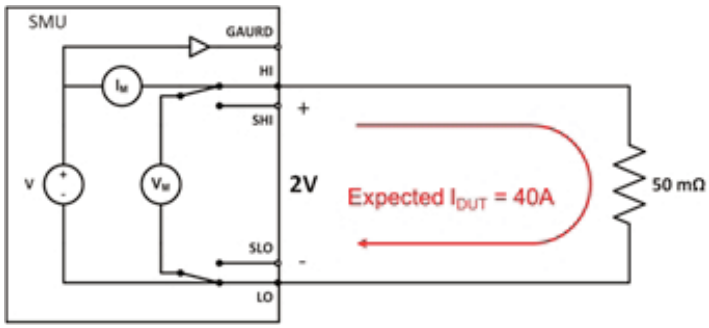


FIGURE 2. Impact of test lead resistance.

That "missing" 20A is the result of test lead resistance. In fact, we were not pulsing 2V into 50mΩ but into 100mΩ instead, with 25mΩper test lead. With 50mΩ of lead resistance, half of the output voltage sourced was dropped in the test leads and only half of it ever reached the device.

To characterize the device correctly, it's essential to know not only the current through the device but the actual voltage at the device. On SMUs this is done by using remote voltage sensing. Using a second set of test leads allows the instrument to sense the voltage directly at the device; because almost no current flows through these leads, the voltage fed back to the instrument will match the voltage at the device. Also, because these leads feed the voltage at the device directly back into the SMU's feedback loop, the SMU can compensate for the voltage drop across the test leads by outputting a higher voltage at its output terminals.

Although SMUs can use remote sensing to compensate for voltage drops in the test leads, there is a limit to how much drop it can compensate for. For most SMUs, this maximum drop is about 3V/lead. If the voltage drop per lead reaches or exceeds this limit, strange things can start happening. The first thing is that the rise and fall times of the voltage pulse slow down, significantly increasing the time required to make a settled measurement. Given enough time for the pulse to settle, the voltage measurements may come back as the expected value, but the measured current will be lower than expected because the SMU is actually sourcing a lower voltage at the DUT than the level that it is programmed to source.

If you exceed the source-sense lead drop while sourcing current, a slightly different set of strange behaviors may occur. The current measurement will come back as the expected value and will be correct because current is measured internally and this measurement is not affected by lead drop, but the voltage reading will be higher than expected. In transient pulse measurements, you may even see the point at which the source-sense lead drop limit was exceeded as the measured voltage suddenly starts increasing again after it appeared to be settling.

These strange behaviors can be difficult to detect in the measured data if you do not know what voltage to expect from your device. Therefore, inspecting your pulse waveforms fully when validating your test system is essential.

Minimizing test lead resistance is essential to ensuring quality pulse measurements. There are two ways to do this:

- ***Minimize the length of the test leads.*** Wire resistance increases at a rate that's directly proportional to the length of the wire. Doubling the wire's length doubles the resistance. Keeping leads lengths no greater than 3 meters is highly recommended for high current pulse applications.
- ***Use wire of the appropriate diameter or gauge for the current being delivered.*** The resistance of a wire is also directly proportional to the cross sectional area of the wire. Increasing the diameter, or reducing the gauge, of the wire increases this area and reduces the resistance. For pulse applications up to 50A, a wire gauge of no greater than 12 AWG is recommended; for applications up to 100A, it's best to use no greater than 10 gauge.

Excessive test lead inductance is another common issue. In DC measurements, test lead inductance is rarely considered because it has

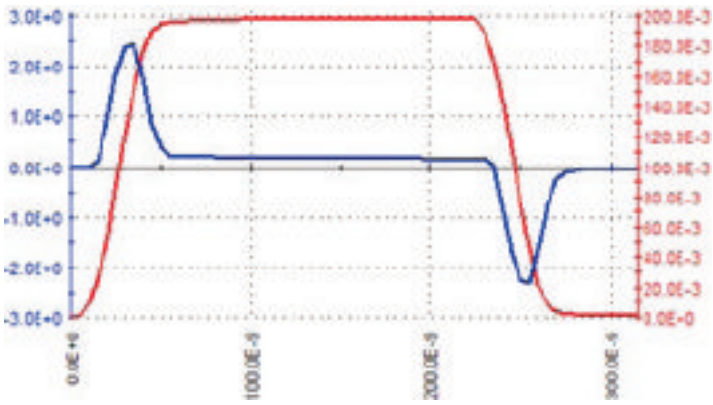


FIGURE 3. Humps in the voltage waveform of transient pulse measurements due to test system inductance.

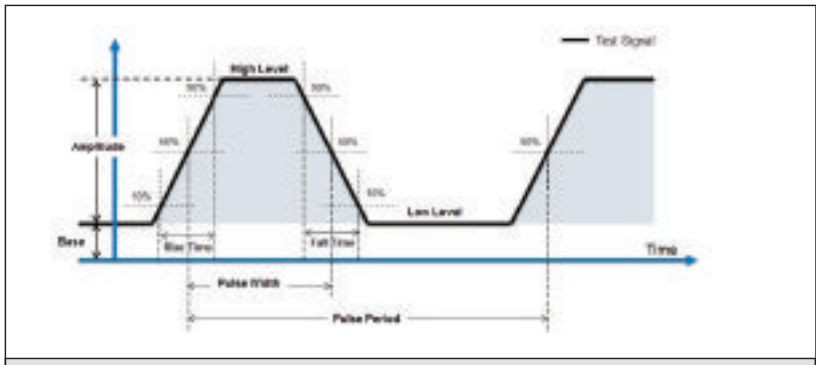
little effect on the measurements. However, in pulse measurements, lead inductance has a huge effect and can play havoc with a system's ability to take quality measurements.

Humps in the voltage waveform of transient pulse measurements (**FIGURE 3**) are a common problem when generating current pulses. Just as with humps in the current waveforms, these humps can be seen in the data from the instrument but are nowhere to be seen when measured at the device with an oscilloscope. These humps are the result of the additional voltage seen at the instrument due to inductance in the cabling between the instrument and the device under test.

$$V = L \times \frac{di}{dt}$$

EQUATION 1.

Equation 1 describes the relation between inductance and voltage. With this equation, we can see that for a given change in current over change in time (di over dt), the larger the inductance L is, the larger the resulting voltage will be. This equation also tells us that for a fixed inductance L, the larger the change in current or the smaller the change in time, the larger the resulting voltage will be. This means that the larger the pulse and or the faster the rise and falls times, the bigger the voltage humps will be.



The Anatomy of a Pulse

The amplitude and base describe the height of the pulse in the pulse waveform. Base describes the DC offset of the waveform from 0. This is the level the waveform will be both before and after the pulse. Amplitude is the level of the waveform relative to the base level and has an absolute value that is equal to the base plus amplitude. For example, a pulse waveform with a base of 1Vand an amplitude of 2V would have a low level of 1V and a high level of 3V.

Pulse width is the time that the pulse signal is applied. It is commonly defined as the width in time of the pulse at half maximum also known as Full Width at Half Maximum (FWHM). This industry standard definition means the pulse width is measured where the pulse height is 50% of the amplitude.

Pulse period is the length in time of the entire pulse waveform before it is repeated and can easily be measured by measuring the time from the start of one pulse to the next.

The ratio of pulse width over pulse period is the duty cycle of the pulse waveform.

A pulse's rise time and fall time are the times it takes for the waveform to transition from the low level to the high level and from the high level back down to the low level. The industry standard way to measure the rise time is to measure the time it takes the pulse waveform to go from 10% amplitude to 90% amplitude on the rising edge. Fall time is defined as the time it takes for the waveform to go from 90% amplitude to 10% amplitude on the falling edge.

measure around this lead inductance and measure the voltage directly at the device. However, as with excessive lead resistance, excessive lead inductance can also cause a problem for SMUs. If the inductance is large enough and causes the source-sense lead drop to exceed the SMU's limit, transient pulse measurement data will have voltage measurement errors on the rising and falling edges similar to the ones seen when lead resistance is too large. Pulse I-V measurements are generally unaffected by lead inductance because the measurements are taken during the flat portion of the pulse where the current is not changing. However, excessive lead inductance will slow the rising and falling edges of voltage pulses and may cause ringing on current pulses, thereby requiring larger pulse widths to make a good settled pulse I-V measurement.

Although SMUs are able to compensate for some lead inductance, PMUs have no compensation features, so the effects of inductance must be dealt with directly, such as by:

- Reducing the size of the change in current by reducing the magnitude of the pulse.
- Increasing the length of the transition times by increasing the rise and fall times.
- Reducing the inductance in the test leads.

Depending on the application or even the instrument, the first two measures are usually infeasible, which leaves reducing the inductance in the test leads. The amount of inductance in a set of test leads is proportionate to the loop area between the HI and LO leads. So, in order to reduce the inductance in the leads and therefore reduce the size of the humps, we must reduce the loop area, which is easily done by simply twisting the leads together to create a twisted pair or by using coaxial cable. Loop area can be reduced further by simply reducing the length of the cable. ◆

Web tension control in roll-to-roll web processing

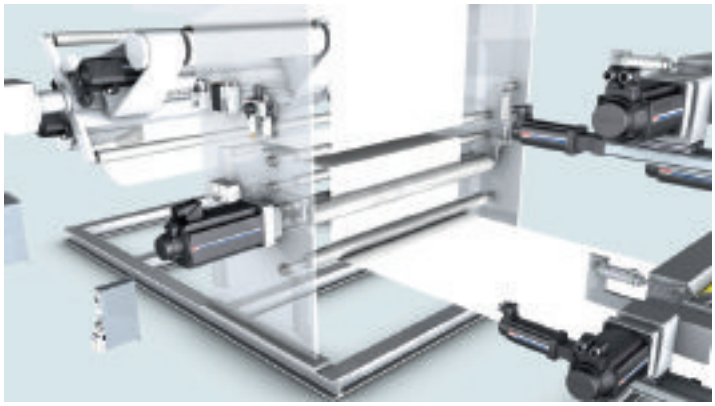
BIPIN SEN, *Bosch Rexroth, Hoffman Estates, IL*

Achieving precise registration accuracy is a factor of two related variables: web tension and transport velocity.

One of the brightest developments in electronics is Organic Light Emitting Diode (OLED) TVs, which are attracting consumers with their eye-popping colors and super-thin designs. Unlike the components found in traditional flat-screen display technology, OLEDs use thin, flexible sheets of material that emit their own light and are produced using a technique similar to inkjet or sheet-feed printing.

Introduced to the consumer market only a few years ago, OLEDs are still relatively costly to manufacture in large sizes due to limitations in both shadow-mask deposition methods, and in newer laser annealing and inkjet printing techniques. To scale up large area display production economically, printed electronics manufacturers are seeing the benefits of another production method — namely, digital roll-to-roll web processing.

Like an inkjet printer deposits ink on sheets of paper, a digital roll-to-roll press patterns thin-film transistors and other devices directly onto large organic, flexible substrates. But unlike slower sheet-fed digital printing, the substrate in a roll-to-roll press is supplied from an infeed reel through the printing section onto an outfeed reel in one continuous inline web. An array of piezo-electric printheads deposit the ink — comprised of a conductive organic solution — on the substrate at precise locations. In roll-to-roll web processing,



electroluminescent materials or other microcrystalline layers are deposited on substrate at slower speeds, on the order of 10 to 100 feet (3 to 30 meters) per minute.

The speed of the roll-to-roll process reduces the cost of fabrication dramatically—but several challenges must be overcome to make it pay off.

Fast speeds create big challenges

Similar to how Sunday newspaper comics require precise color registration to keep images from blurring, printed electronics require far tighter registration. Tolerances for applications such as Thin-Film Transistors (TFTs) or OLEDs require registration smaller than 10 microns. High-speed, high-resolution cameras measure registration accuracy and provide input to the control system. To ensure that degree of accuracy, precise web tension control is required.

BIPIN SEN *is a Senior Business Development Engineer at Bosch Rexroth, Hoffman Estates, IL. Email: Bipin.Sen@boschrexroth-us.com*

Achieving precise registration accuracy is a factor of two related variables: web tension and transport velocity.

Web transport control ensures proper uniform tension on the substrate web as it travels through the process. Because the substrate changes properties in response to force loading, changes in tension affect the stability of deposited materials. Substrate expansion causes cracks, broken traces, short circuiting and layer delamination. Changes in web velocity in the print zone affect registration, thickness and resolution of fine lines.

As the web travels downstream, constant tension must be maintained in each tension zone, which is defined as an isolated area in a machine where constant tension must be maintained appropriate to the process being performed in that area. A roll-to-roll press has several tension zones. Problems occur when a change is made in one tension zone and no change is needed in other areas. When tension control is coupled between all zones, a change in one creates a cascade of changes in others, impacting the stability of the entire web.

FIGURE 1 shows how instability affects a web traveling at five meters per second with two successive tension controllers for two tension zones. A command for a step change tension reduction is sent to the green zone controllers. No change is required in the upstream blue zone. But because the web is continuous, the tension disturbance is carried back to the blue zone, which causes the blue controller to compensate. In turn, this change affects the downstream green zone, sending jitter back to the blue zone. This back and forth jitter takes about 85 seconds to settle down. The web tension finally stabilizes in about 90 seconds. During that time, the machine is yielding waste product.

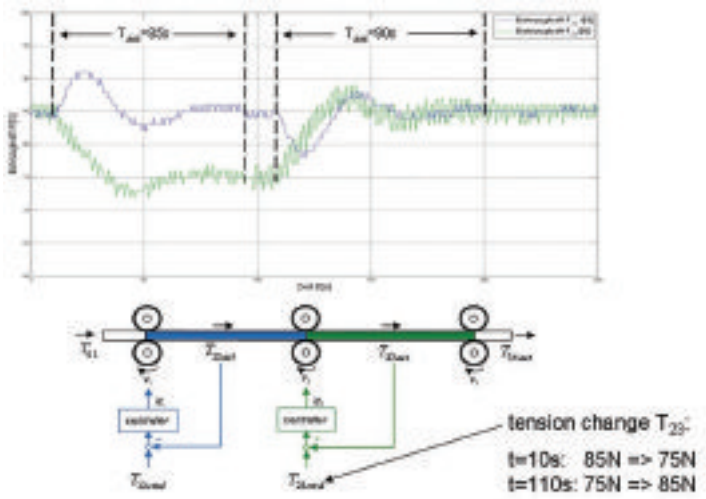


FIGURE 1. Tension instability.

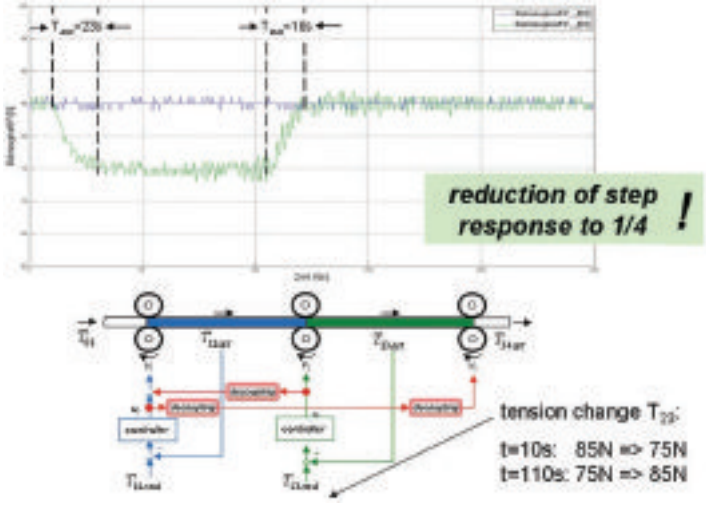


FIGURE 2. Improved tension control.

The challenge of tension adjustment

In an ideal world, web instability would never occur because tension adjustment would never be needed. But tension adjustment is necessary due to several mechanical factors:

- Oscillations caused by mechanical misalignments
- Differing inertial response (lag) of mechanical elements during web acceleration
- Out-of-round unwind and tension rolls
- Slipping through nip rolls
- Over aggressive web-guide correction

Several technical process and control issues also affect tension: tension set point changes, phase offset on driven rolls, tension bleed from one zone to another, and, of course, thermal effect (contraction/expansion) as the substrate passes through various processes.

The factors requiring tension adjustment cannot all be eliminated. Variance in any one factor in a zone necessitates changes in tension control and web speed. Consequently, with coupled tension zone control, jitter is inevitable in a continuous web where the controllers cause a feedback loop.

The benefits of decoupled controllers

There is a solution: Decouple each tension zone, allowing each controller to operate independently.

This has been accomplished in digital printing applications using Bosch Rexroth controllers incorporating a unique tension decoupling function block. As the name implies, the function block allows tension control for each zone to operate independently. As a result, tension changes can be isolated in one zone without affecting tension change in other areas.

The result can be seen in **FIGURE 2**. In this example, the press uses two successive controllers. But now the step change signaled by the green section controller doesn't create a cascade effect upstream. Along with decoupling to prevent feedback, the Rexroth controller initiates a response to step reduction in tension control in one-fourth the time compared to typical controllers.

With the Rexroth solution, tension can be controlled for up to eight axes. One or multiple points can be selected to be left uncontrolled. At the selected axis, line speed is held constant. At a standstill, web tension can be maintained. In fact, Rexroth multi-axis tension control increases standstill web tension accuracy by a factor of two to four. Achieving the desired standstill web tension is also much faster. Without decoupling, a setpoint can be achieved in 13-14 seconds; with decoupling, it takes three to four seconds.

During acceleration, tension control decoupling ensures the web is stable as soon as full production speed is reached, compared to a delay of five seconds or longer with coupled control. And when tension setpoint changes occur during runtime, the transient response with decoupling takes about one second, compared to about four seconds with coupled control.

Not unlike digital printing, the adoption of roll-to-roll web printing will accelerate as the technology demonstrates its ability to provide high accuracy at high speeds.

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EXECUTIVE OFFICES

Extension Media 1786 18th Street, San Francisco, CA 94107-2343.

ADVERTISING

Sales Manager
Kerry Hoffman
1786 18th St.
San Francisco,CA 94107-2343
Tel: 978.580.4205;
e-mail: khoffman@extensionmedia.com

North America
Kerry Hoffman
Tel: 978.580.4205
khoffman@extensionmedia.com

Germany, Austria, E. Switzerland & E. Europe
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Tel: +49.0.8801.9153791
holgerg@pennwell.com

China, Hong Kong
Adonis Mak
Tel:+852.90182962
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Taiwan
Diana Wei
Tel: +886.2.23965128 ext: 270
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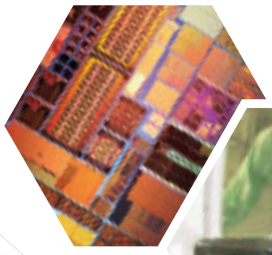


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Flexible facilities for 450mm wafer fabs

When the commercial semiconductor manufacturing industry decides to move to the next wafer size of 450mm, it will be time to re-consider equipment and facilities strategies. Arguably, there is reason to implement new strategies for any new fab to be built regardless of the substrate size. In the case of 450mm, if we merely scale up today's 300mm layouts and operating modes, the costs of construction would more than double. Our models show that up to 25% of the cost of new fab construction could be saved through modular design and point-of-use (POU) facilities, and an additional 5-10% could be saved by designing for "lean" manufacturing.

In addition to cost-savings, these approaches will likely be needed to meet the requirements for much greater flexibility in fab process capabilities. New materials will be processed to form new devices, and changes in needed process-flows and OEM tools will have to be accommodated by facilities. In fact, tighter physical and data integration between OEM tools and the fab may result in substantially reduced time to first silicon, ongoing operating costs and overall site footprint.

POU utilities with controls close to the process chambers, rather than in the sub-fab, have been modeled as providing a 25-30% savings on instrumentation and control systems throughout the fab. Also, with OEM process chamber specifications for vacuum-control and fluid-purity levels expected to increase, POU utilities provide a flexible way to meet future requirements.

JOE CESTARI, *Total Facility Solutions, Plano, Texas*

Reduction of fluid purity specifications on central supply systems in harmony with increases in localized purification systems for OEM tools can also help control costs, improve flexibility, and enhance operating reliability. There are two main reasons why our future fabs will need much greater flexibility and intelligence in facilities: high-mix production, and 1-12 wafer lots.

High-mix production

Though microprocessors and memory chips will continue to increase in value and manufacturing volumes, major portions of future demand for ICs will be SoCs for mobile applications. The recently announced "ITRS 2.0"—the next roadmap for the semiconductor fab industry after the "2013" edition published early in 2014—will be based on applications solutions and less on simple shrinks of technology. Quoting Gartner Dataquest"s assessment:

"System-on-chip (SoC) is the most important trend to hit the semiconductor industry since the invention of microprocessors. SoC is the key technology driving smaller, faster, cheaper electronic systems, and is highly valued by users of semiconductors as they strive to add value to their products."

1-12 Wafer Lots

The 24-wafer lot may remain the most cost-effective batch size for low-mix fabs, but for high-mix lines 12-wafer lots are now anticipated even for 300mm wafers. For 450mm wafers, the industry needs to re-consider "the wafer is the batch" as a manufacturing strategy. The 2013 ITRS chapter on Factory mentions in Table 5 that by the year 2019 "Single Wafer Lot Manufacturing System as an option" will likely be needed by some fabs. Perhaps a 1-5 wafer carrier and interface would be a way for an Automated Material Handling System (AMHS) to link discrete OEM tools as an evolution of current 300mm FOUP designs.

However, a true single-wafer fab line would be the realization of a revolution started over twenty years ago when the MMST Program was a $100M+ 5-year R&D effort funded by DARPA, the U.S. Air Force, and Texas Instruments, which developed a 0.35µm double-level-metal CMOS fab technology (with a three-day cycle time). In the last decade BlueShift Technologies was started and stopped to provide such revolutionary technology for vacuum-robot-lines to connect single-wafer chambers all with a common physical interface.

Lean manufacturing approaches should work well with high-mix product fabs, in addition to providing more efficient consumption of consumables in general. In specific, when lean manufacturing is combined with small batch sizes—minimally the single wafer—there is tremendous improvement in cycle-time.

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