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Solid State TECHNOLOGY®

MARCH 2016 VOL. 59 NO. 2

The element neon (Ne) gives a distinct reddish-orange glow when used in either low-voltage neon glow lamps or in high-voltage discharge tubes or neon advertising signs.

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China's semiconductor strategy

China has become the largest and the fastest growing market in the world. 40% of the worldwide semiconductor shipments go to China and that's expected to increase to almost 42% in 2019.

The "National Semiconductor Industry Development Guidelines" and "Made in China 2025" were published by China's State Council in June 2014 and May 2015, respectively. Both policies have already led to a major push in the development of the local IC industry, with investments in semiconductor memories, design, foundries, OSATS, and equipment and materials.

Based on the "National Semiconductor Industry Development Guidelines," a US$19 billion national industry investment fund has been set up to help local foundries finance the build-up of advanced manufacturing processes, and also to assist local IC firms to form mergers and/or make acquisitions internationally. Dieter Ernst, a Senior Fellow at the East West Center In Hawaii says with this plan, China seeks to move from the catching up stage to a full-scale forging ahead.

With the "Made in China 2025" initiative, China is aiming to improve the self-sufficiency rate for ICs in the nation to 40% in 2020, and boost the rate further to 70% in 2025.

What will be key is how Chinese companies can gain access to 16/14nm, 10nm, and 7nm technologies as well as DRAM and 3D NAND technologies.

According to Handel Jones of IBS, who spoke at SEMI's Industry Strategy Symposium earlier this year, China is also strongly positioned in 5G. "China will be the global leader in 5G," he said. Based on an analysis of Huawei, Ericsson, Nokia and others, Jones said Huawei – which is investing about $1 billion/year -- is ahead. "That's going to have a fairly disruptive effect on the supply chain," he said. He expects early development in 2017/2018 and then fairly extensive deployment in 2020.

In a recent report, "From Catching Up to Forging Ahead: China's Policies for Semiconductors," Ernst points out that while the opportunities for China are real, they all involve considerable uncertainty. "Basic parameters that determine how China will fare may change at short notice and in unpredictable ways," he said. To succeed, China needs to move toward a bottom-up, market-led approach.

—Pete Singer, Editor-in-Chief

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Web Exclusives

What's happening in the China market?

The application that world's largest contract chipmaker TSMC submitted to set up a 12-inch wafer plant in China will likely be green-lighted before Chinese New Year's rolls around on February 8, according to the China Post on January 26.

http://bit.ly/1osDMa1

Familiar phrase returns to the fray at EV Group conference

At the EV Group Technology Day conference on Wednesday in Fremont, Calif., a familiar phrase that hasn't been often heard in recent years was used: Step-and-repeat. (From SemiMD.com)

http://bit.ly/1RTk3fB

Cadence debuts product for reducing test time, costs

Cadence Design Systems is introducing the Modus Test Solution, a product that it touts as capable of reducing IC testing time and test costs, while improving profit margins for chips. (From SemiMD.com)

http://bit.ly/1Ww33va

Optimism reigns at SPIE lithography conference, despite challenges

The changes required in lithography and related technologies to continue IC scaling promise to be painful and costly. Mitigating the pain and the cost is a common theme at the SPIE conference. Jeff Dorsch, Contributing Editor, reports.

http://bit.ly/1R4FTli

ASML details advances in DUV, Metrology, EUV

ASML Holding is glad to talk about its continuing progress in extreme-ultraviolet lithography technology. But first, the company has some information about its deep-ultraviolet scanners, as well.

http://bit.ly/21k0dQC

n&b news and blogs

Does consolidation put innovation at risk?

Consolidation in the semiconductor industry continues apace, with more than $100 billion in mergers and acquisitions announced in 2015, and more to come in 2016. "With our industry growth rates being so low, it's a lot cheaper to acquire market share than it is to invest and beat your competitor over the head," said analyst Bill McClean, speaking at SEMI's Industry Strategy Symposium (ISS) in January.

http://bit.ly/1QoQofe

Insights from the Leading Edge: 3D ASIP and On the Passing of Moore's Law

Continuing our look at the 2015 3D ASIP conference, one of the themes of this year's conference was the coming of age of 3D stacked memory which now comes in several flavors from several vendors.

http://bit.ly/1Qqm25E

3D XPoint uses PCM material in ReRAM device

IM Flash pre-announced "3D XPoint" memory for release later this year, and lack of details has led to widespread confusion regarding what it is. (From SemiMD.com)

http://bit.ly/1Qqm6m8

Cautious expectations amid a slow-growth economy

The health of the IC industry is increasingly tied to the health of the worldwide economy. Rarely can there be strong IC market growth without at least a "good" worldwide economy to support it. Consequently, IC Insights expects annual global IC market growth rates to closely track the performance of worldwide GDP growth

http://bit.ly/1VsbPdy

Another record year for silicon wafer shipment volumes in 2015

Worldwide silicon wafer area shipments increased 3 percent in 2015 when compared to 2014 area shipments according to the SEMI Silicon Manufacturers Group (SMG) in its year-end analysis of the silicon wafer industry. However, worldwide silicon revenues decreased by 6 percent in 2015 compared to 2014.

http://bit.ly/1Ww1uNO

worldnews

ASIA - **TSMC** announced that the earthquake of 6.4 magnitude which struck southern Taiwan on February 6 did not cause any serious personnel injuries nor any structural or facility damage to the Company's Fab 14 and Fab 6 manufacturing sites in the Tainan Science Park.

EUROPE - **Soitec** began mass production of 300mm RF-SOI substrates for mobile communications.

USA - **WIKA** Group adopted the **HERCULES** lithography track system from EV Group.

EUROPE - **EV Group** announced its participation in the 3D integration consortium of IRT Nanoelec, which is headed by **CEA-Leti**.

ASIA – **SEMI** announced that **SEMICON Southeast Asia 2016** will be returning to Penang, Malaysia.

USA - **Teradyne, Inc**. has appointed Gregory Smith as president of the Teradyne semiconductor test division, replacing Mark Jagiela who has been acting division president since 2014.

EUROPE - **Dialog Semiconductor** has determined not to revise its proposal to acquire US-based microcontroller and touch solutions specialist **Atmel Corp**.

USA – **Microchip Technology** appointed Ganesh Moorthy as President and Chief Operating Officer.

ASIA – **Presto Engineering** announced the opening of two manufacturing hubs and a worldwide logistics center in Asia.

USA – **TowerJazz** completed its acquisition of **Maxim Integrated Product Inc.'s** San Antonio facility.

Fairchild rejects proposal from China Resources, Hua Capital

Fairchild Semiconductor International, Inc. announced this month that its board of directors, after consultation with its legal and financial advisors, has determined that the unsolicited proposal received on December 28, 2015, from China Resources Microelectronics Ltd and Hua Capital Management Co., Ltd. to acquire Fairchild does not constitute a "Superior Proposal" as defined in the Company's Agreement and Plan of Merger with ON Semiconductor Corporation.

On January 5, 2016, Fairchild announced that the Board determined that the Acquisition Proposal would reasonably be expected to result in a Superior Proposal. The Fairchild management team, along with Fairchild's legal and financial advisors, engaged in extensive discussions with China Resources and Hua Capital. After conducting a thorough review, and after consultation with Fairchild's legal and financial advisors, the Board concluded that the Acquisition Proposal is not superior to Fairchild's existing agreement with ON Semiconductor.

As previously announced on November 18, 2015, Fairchild entered into an Agreement and Plan of Merger with ON Semiconductor, under which a wholly owned subsidiary of ON Semiconductor agreed to acquire all of the outstanding shares of Fairchild common stock for $20.00 per share in cash.

Fairchild remains subject to the Agreement and Plan of Merger with ON Semiconductor, and the Board has not changed its recommendation in support of that agreement.

Goldman, Sachs & Co. is acting as financial advisor to Fairchild, and Wachtell, Lipton, Rosen & Katz is serving as its legal counsel.

Silicon chip with integrated laser: Light from a nanowire

Ever smaller, ever faster, ever cheaper – since the start of the computer age the performance of processors has doubled on average every 18 months. 50 years ago already, Intel co-founder Gordon E. Moore prognosticated this astonishing growth in performance. And Moore's law seems to hold true to this day.

But the miniaturization of electronics is now reaching its physical limits. "Today already, transistors are merely a few nanometers in size. Further reductions are horrendously expensive," says Professor Jonathan Finley, Director of the Walter Schottky Institute at TUM. "Improving performance is achievable only by replacing electrons with photons, i.e. particles of light."

Photonics – the silver bullet of miniaturization

Data transmission and processing with light has the potential of breaking the barriers of current electronics. In fact, the first silicon-based photonics chips already exist. However, the sources of light for the transmission of data must be attached to the silicon in complicated and elaborate manufacturing processes. Researchers around the world are thus searching for alternative approaches.

Scientists at the TU Munich have now succeeded in this endeavor: Dr. Gregor Koblmüller at the Department of Semiconductor Quantum-Nanosystems has, in collaboration with Jonathan Finley, developed a process to deposit nanolasers directly onto silicon chips. A patent for the technology is pending.

Growing a III-V semiconductor onto silicon requires tenacious experimentation. "The two materials have different lattice parameters

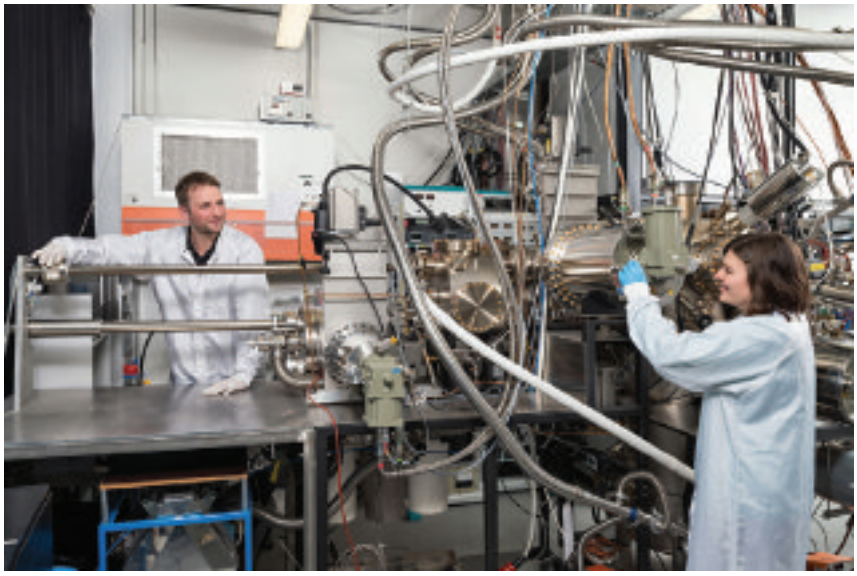

Figure 1: The candidate Benedikt Mayer and Masters student Lisa Janker in an experiment at the molecular beam epitaxy in the Walter Schottky Institute of the Technische Universitaet Muenchen am teaching Suhl for semiconductor nanostructures and quantum devices, with Prof. Dr. Jonathan Finley; persons depicted (from left): Benedikt Mayer, Lisa Janker; Location: Walter Schottky Institute, Am Coulombwall 4, 85748 Garching, Germany; Date: 02/10/2016; CREDIT: Uli Benz / TU Muenchen

and different coefficients of thermal expansion. This leads to strain," explains Koblmüller. "For example, conventional planar growth of gallium arsenide onto a silicon surface results therefore in a large number of defects."

The TUM team solved this problem in an ingenious way: By depositing nanowires that are freestanding on silicon their footprints are merely a few square nanometers. The scientists could thus preclude the emerging of defects in the GaAs material.

Atom by atom to a nanowire

But how do you turn a nanowire into a vertical-cavity laser? To generate coherent light, photons must be reflected at the top and bottom ends of the wire, thereby amplifying the light until it reaches the desired threshold for lasing.

To fulfil these conditions, the researchers had to develop a simple, yet sophisticated solution: "The interface between gallium arsenide and silicon does not reflect light sufficiently. We thus built in an additional mirror – a 200 nanometer thick silicon oxide layer that we evaporated onto the silicon," explains Benedikt Mayer, doctoral candidate in the team led by Koblmüller and Finley. "Tiny holes can then be etched into the mirror layer. Using epitaxy, the semiconductor nanowires can then be grown atom for atom out of these holes."

Only once the wires protrude beyond the mirror surface they may grow laterally – until the semiconductor is thick enough to allow photons to jet back and forth to allow stimulated emission and lasing. "This process is very elegant because it allows us to position the nanowire lasers directly also onto waveguides in the silicon chip," says Koblmüller.

Basic research on the path to applications

Currently, the new gallium arsenide nanowire lasers produce infrared light at a predefined wavelength and under pulsed excitation. "In the future we want to modify the emission wavelength and other laser parameters to better control temperature stability and light propagation under continuous excitation within the silicon chips," adds Finley.

The team has just published its first successes in this direction. And they have set their sights firmly on their next goal: "We want to create an electric interface so that we can operate

Continued on page 6

***Silicon chip**, Continued from page 5*

the nanowires under electrical injection instead of relying on external lasers," explains Koblmüller.

"The work is an important prerequisite for the development of high-performance optical components in future computers," sums up Finley. "We were able to demonstrate that manufacturing silicon chips with integrated nanowire lasers is possible."

The research was funded by the German Research Foundation (DFG) through the TUM Institute for Advanced Study, the Excellence Cluster Nanosystems Initiative Munich (NIM) and the International Graduate School of Science and Engineering (IGSSE) of the TUM, as well as by IBM through an international postgraduate program.

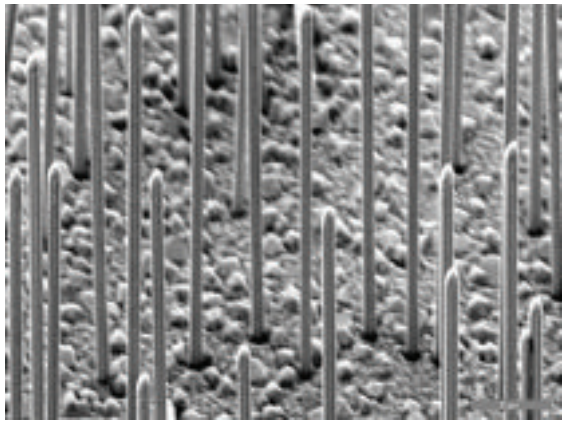

Figure 2: GaAs nanowires on a silicon surface – CREDIT: Thomas Stettner / Philipp Zimmermann / TUM

Neon shortage coming

The current Neon demand is growing in "stealth mode" – hidden from the layman's view because of significant factors only analysts fully versed in lithography, OLED/FPD and semiconductor device trends would catch. The traditional method of using historical data to predict future Neon demand will grossly underestimate future usage.

"Those who are basing their thinking on projections of historical Neon growth are in for a big surprise," said TECHCET's President/CEO, Lita Shon-Roy. "Even with the recovery of the Neon supply chain, Neon conservation actions, and new sources in China, we predict that Neon demand will grow faster than Neon supply," she added.

The largest and most rapidly growing Neon demand drivers are Lasik, OLED/FPD (displays) and DUV lithography. However, Neon gas consumed by DUV excimer laser gases is growing at a faster pace and represents more than 90% of world's Neon consumption.

Semiconductor lithographic use of Neon is increasing more rapidly than expected for several reasons including the delay of EUVL while demand for finer line width patterning is increasing.

In addition, new consumer related markets drive increased usage of legacy device processing. Each increase in the number of lithographic steps increases the need for more DUV lithography tools, and drives up the volume demand for Neon. This is true for V-NAND process flows, as well as DRAM and Logic devices dependent on multi-patterning.

Currently, the installed base of DUV lithography tools is ~ 4,400. In contrast, there have only been a dozen or so EUVL tools shipped through the end of 2015.

"The continued growth of DUV tools will push up demand for NEON beyond which supply can support," cautioned Shon-Roy.

More details can be found from TECHCET's latest Critical Materials Report on NEON Supply & Demand. Information will also be presented at the CMC Conference, scheduled for May 5-6, in Hillsboro, Oregon – this is the open forum portion of the Critical Materials Council meetings.

SUNY Poly, GLOBALFOUNDRIES announce new $500M R&D program

SUNY Polytechnic Institute (SUNY Poly) and GLOBALFOUNDRIES today announced the establishment of a new Advanced Patterning and Productivity Center (APPC), which will be located at the Colleges of Nanoscale Science and Engineering (CNSE) in Albany, N.Y.

The $500 million, 5-year program will accelerate the introduction of Extreme Ultraviolet (EUV) lithography technologies into manufacturing. The center is anchored by a network of international chipmakers and material and equipment suppliers, including IBM and Tokyo Electron, and will generate 100 jobs.

"This advanced new partnership between SUNY Poly and GLOBALFOUNDRIES demonstrates how Governor Cuomo's strategic investments in SUNY are bolstering the system's research capacity, leveraging private dollars, and creating exciting new opportunities at our campuses for students and faculty," said SUNY Chancellor Nancy L. Zimpher. "SUNY Poly's nanotechnology expertise coupled with the governor's innovative public-private partnership model has positioned New York as a global leader in computer chip research, development, and manufacturing. SUNY System Administration strongly applauds Dr. Kaloyeros for his leadership in bringing the Advanced Patterning and Productivity Center to Albany."

"Today's announcement is a direct result of Governor Cuomo's innovation driven economic development model. His strategic investments supporting the state's world class nanotechnology infrastructure and workforce have made us uniquely suited to host the new APPC, which will enable the continuation of Moore's Law and unlock new capabilities and opportunities for the entire semiconductor industry," said Dr. Alain Kaloyeros, President and CEO of SUNY Polytechnic Institute. "In partnership with GLOBALFOUNDRIES, IBM and Tokyo Electron, we will leverage our combined expertise and technological capabilities to meet the critical needs of the industry and advance the introduction of this complex technology."

"GLOBALFOUNDRIES is committed to an aggressive research roadmap that continually pushes the limits of semiconductor technology. With the recent acquisition of IBM Microelectronics, GLOBALFOUNDRIES has gained direct access to IBM's continued investment in world-class semiconductor research and has significantly enhanced its ability to develop leading-edge technologies," said Dr. Gary Patton, CTO and Senior Vice President of R&D at GLOBALFOUNDRIES. "Together with SUNY Poly, the new center will improve our capabilities and position us to advance our process geometries at 7nm and beyond."

EUV lithography is a next-generation semiconductor manufacturing technique that produces short wavelengths (14-nanometers and below) of light to create minuscule patterns on integrated circuits. The technology is critical to achieve the cost, performance, and power improvements needed to meet the industry's anticipated demands in cloud computing, Big Data, mobile devices, and other emerging technologies.

Introducing Novel NMT Technology for Ultra-Thin Film Measurement

RONI PERETZ, BENNY DONNER, COLIN SMITH *and* **MICHAEL GEFFIN**, *XwinSys, Israel*

In the semiconductor industry, 3D stacking leads the race to miniaturizing devices at a competitive cost. Thin films are becoming ultra-thin and more localized, and feature wider material variations and smaller scales interactions with less tolerance to aberrations.

NMT: a new generation of XRF technology

XwinSys has identified the semiconductors recent market trends and has developed a novel XRF technology accordingly, named NMT: Noise-reduced Multilayer Thin-film measurement. This innovative approach can be used for in-line inspection and metrology features, to accurately and precisely analyze single and multi-layered elements in ultra-thin films, down to 1Å.

FIGURE 1: XwinSys Onyx System

Overcoming EDXRF weaknesses

The NMT concept significantly improves the S/N ratio, resulting in low background noise by using a set of unique Silicon Drifted Detectors (SDD), replacing the air atmosphere with helium, implementing a-spot vertical incident X-ray beam and applying unique background removal algorithms.

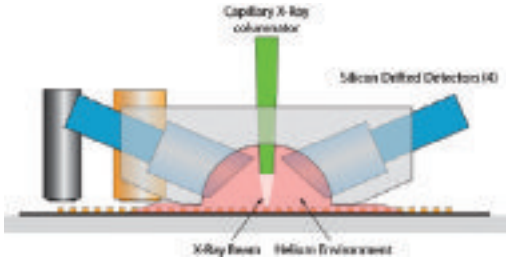

FIGURE 2: XwinSys XRF Module

Free from optical constants

When using common optical techniques to analyze layer's thickness below 50Å, calculation constants (D, N, K) are necessary but also highly unpredictable; In a multi-layer stack the values of these constants are even more challenging to analyze. X-ray is not sensitive to these constants, hence direct results of ultra-thin layers (both opaque and transparent materials) can be accurately valued by the NMT.

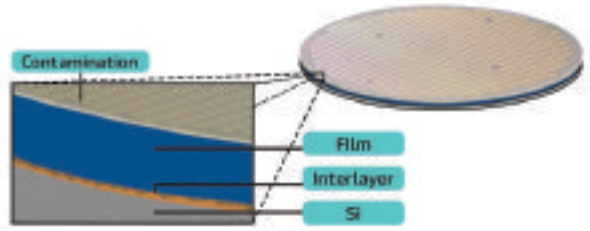

FIGURE 3: Layers Structure of Ultra-Thin Film

NMT novel technology can be utilized for in-line applications ranging from localized ultra-thin film stacks to the inspection of 3D localized features to the analysis of defects involving geometries, voids and material elements.

XwinSys Technology Development Ltd.
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XwinSys is dedicated to the design, manufacture and marketing of novel solutions based on improved X-ray technology combined with automated optical 3D & 2D microscopes, for the Semiconductor and related industries.

A comeback for WLP in IoT

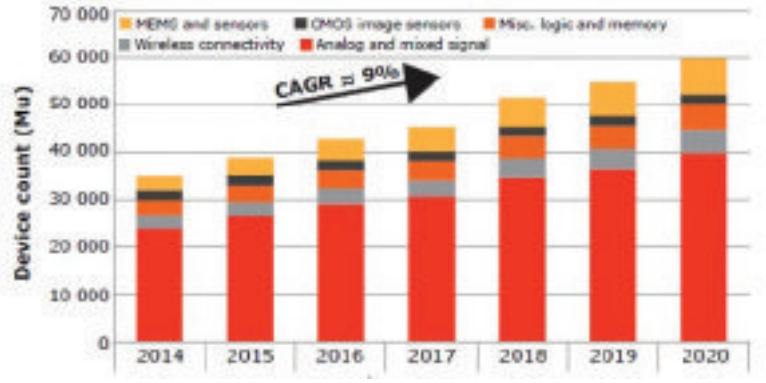
PHIL GARROU,
Contributing Editor

I want to start our look at the 48th International Symposium on Microelectronics (IMAPS 2015) with the presentation by the new Yole Developpement packaging team on the technology and market trends for WLP. You may wonder why I focus on this technology which was leading edge literally 20 years ago. Certainly it is near and dear to my heart since many of my most exciting days in technology were shared with the WLP pioneering groups at Flip Chip Technologies (FCT) and Microelectronics Center of NC/Unitive as this initial wafer level technology was being conceived and developed with my team developing BCB. These two small startup companies certainly were underdogs, and they were using my new dielectric, also an underdog, but within two years we were in nearly every cell phone made in the world.

Since its inception by Rajen Chanchani at the Boston IMAPS conference in 1994 to the commercialization of the UltraCSP by Pete Elenius of FCT in 1998, what was at first one of many chip sized package solutions evolved into wafer level chip scale packaging and then more simply into wafer level packaging or WLP.

By the early 2000's it became obvious that WLP had unmatched advantages in both form factor and cost and the technology was quickly licensed by all the key OSATS and OEMs worldwide and adopted in nearly all mobile phone products.

Yole points out that although WLP has been seemingly out of the spotlight with the advent of higher density packaging solutions such as copper pillar bump, 2.5 & 3DIC and fan out and embedded packaging , WLP remains a highly important and constant presence. The mobile market continues to be the main driver for WLP with over 90% of all fan in packages being found in handsets and tablets.



Fan-in WLP unit forecast.

Since the WLP eliminates the need for WB, substrates, FC bumps and in most cases mold compound, it still results in the shortest interconnects, lowest parasitics, and best electrical performance in terms of speed and frequency. Bump pitch of 0.35mm are currently in high volume production with 0.3 and 0.25mm under consideration. Most fan-in die are below 7 x 7mm and below 200 I/O. In general warpage and board level reliability for larger dies remains a concern. If your die is relatively small and your I/O demands relatively low this is the best packaging solution.

Fan-in WPL units hit 35B in 2014 with a 9% CAGR. BT + WiFi + FM combos, CMOS image sensors and Rf transceivers account for ~ 50% of all WLP applications.

Yole has identified more than 70 high volume fabless and IDM companies implementing their designs in fan-in WLP along with over 20 fan-in manufacturing companies.

In the future IoT (internet of things) will eventually succeed mobile phones as the microelectronic driver...the big dog. However, there have been many unjustified presentations over the last few years detailing, without any support data, how IoT will drive leading edge, high end technologies like 3DIC. IFTLE does not agree with that conclusion but rather contends that IoT will be low I/O and will demand two things – small form factor and low, low cost. As such IoT will generate a huge potential market for fan-in WLP.

Back in the mid 1990's WL-CSP was an underdog who proved itself and became an integral part of cell phone manufacturing and, now after being somewhat overshadowed by newer leading edge technologies for a while, is about to make a comeback due to the inherent strengths of this technology.

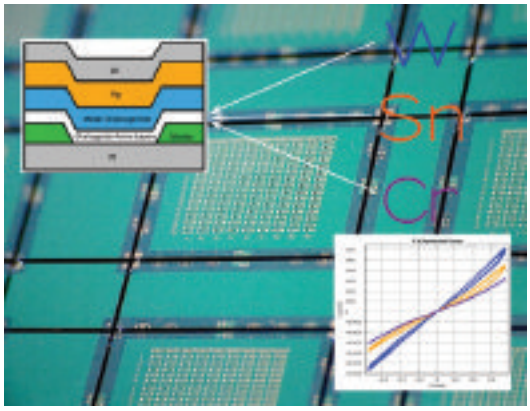
Packaging

Memristor variants and models from Knowm

ED KORCZYNSKI,
Sr. Technical Editor

Knowm Inc. (www.knowm.org), a start-up pioneering next-generation advanced computing architectures and technology, recently announced the availability of two new variations of memristors targeting different neuromorphic applications. The company also announced raw device data available for purchase to help researchers develop and improve memristor models. These new Knowm offerings enable the next step in the R&D of radically new chips for pattern-recognition, machine-learning, and artificial intelligence (AI) in general.

There is general consensus between industry and academia and government that future improvements in computing are now severely limited by the amount of energy it takes to use Von Neumann architectures. Consequently, the US Whitehouse has issued a grand challenge with the Energy-Efficient Computing: from Devices to Architectures (E2CDA) program.



Schematic cross-section of Knowm's memristor devices using Tin (Sn) or Chromium (Cr) or tungsten (W) metal layers, along with the device I/V curves for each. (Source: Knowm)

The **Figure** shows a schematic cross-section of Knowm's memristor devices—with Tin (Sn) and Chromium (Cr) metal layers as the new options to tungsten (W)—along with the device I/V curves for each. "They differ in their activation threshold," explained Knowm CEO and co-founder Alex Nugent in an exclusive interview with Solid State Technology. "As the activation thresholds become smaller you get reduced data retention, but higher cycle endurance. As that threshold increases you have to dissipate more energy per event, and the more energy you dissipate the faster it will burn-out." Knowm's two new memristors, as well as the company's previously announced device, are now available as unpackaged raw dice with masks designed for research probe stations.

Knowm is working on the simultaneous co-optimization of the entire "stack" from memristors to circuit architectures to application-specific algorithms. "The potential of memristors is so huge that we are seeing exponential growth in the literature, a sort of gold rush as engineers race to design new circuits and re-envision old circuits," commented Knowm CEO and co-founder Alex Nugent. "The problem is that in the race to publish, circuit designers are adopting models that do not adequately describe real devices." Knowm's raw data includes AC, DC, pulse response, and retention for different memristors.

"In the future what I image is a single chip with multiple memristors on it. Some will be volatile and very fast, while others will be slow," continued Nugent. "Just like analog design today uses different capacitors, future neuromophic chips would likely use memristors optimized for different changes in adaptation threshhold."

The applications spaces for these devices have intrinsically different requirements for speed and retention. For example, to exploit these devices for pattern recognition and/or anomaly detection (keeping track of confidence in making temporal predictions) it seems best to choose relatively high activation thresholds because the number of operations is unlikely to burn-out devices. Conversely, for circuits that constantly solve optimization problems the best memristors would require low burn-out and thus low activation thresholds. However, analog applications are generally problematic because the existing memristors leak current, such that stored values degrade over time.

Knowm is shipping devices today, mostly to university researchers, and has tested thousands of devices itself. The Knowm memristors can be fabricated at <500°C using industry-standard unit-process steps, allowing for eventual integration with silicon CMOS "back-end" metallization layers. While still in early R&D, this technology could provide much of the foundation for post-Moore's-Law silicon ICs. ◆

Impact of triboelectric charging from DI water on transistor gate damage

STEPHEN SWAN, JOSEPH WILLIAMS, ANN CONCANNON, JIM OHANNES *and* **ERIC EVANGELOU**, *Texas Instruments, Dallas, TX*

Optimized settings for DI water pressure at CMP and careful analysis of interconnect layout are used to improve quality on a complex analog design.

Triboelectricity is defined as a charge of (static) electricity generated by friction. The concept was first applied in the 1940s for electrostatic painting and is now widely used in photocopy machines. This phenomenon becomes a concern in wafer manufacturing processes since water is a polar molecule and deionized water (~18MOhm) is a good insulator [1, 2].

Our investigation into circuit damage was initiated by a finding of high leakage from a single transistor within a complex analog design. Electrical and physical analysis of a failing site revealed a halo image on a TEM micrograph, suggesting that the area of highest electric field under the poly gate had been damaged (**FIGURE 1**).

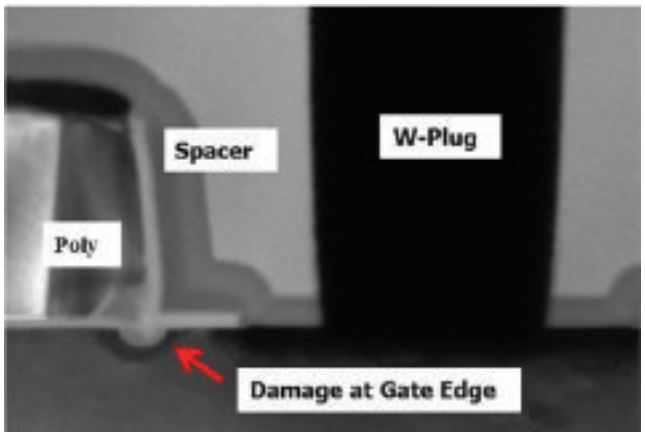


FIGURE 1. TEM showing damaged gate.

Wafer signature – fab root cause

After insuring there was no quality risk (with HTOL and ELFR reliability testing), focus was placed on identifying the physical root cause, understanding why the failures were only occurring on a single transistor, and developing a design rule to reduce the risk on future products. Examination of wafer yield maps revealed fallout of less than 500 parts per million (ppm) in a distinctive geometric pattern with failing die at unique radius from the wafer center. Discussions with fab process experts within TI revealed that the geometric pattern aligned with positions of DI water jets on a single wafer oxide chemical mechanical planarization (CMP) tool and that the problem correlated to use of high DI water pressure (60psi) during wafer transfer operation.

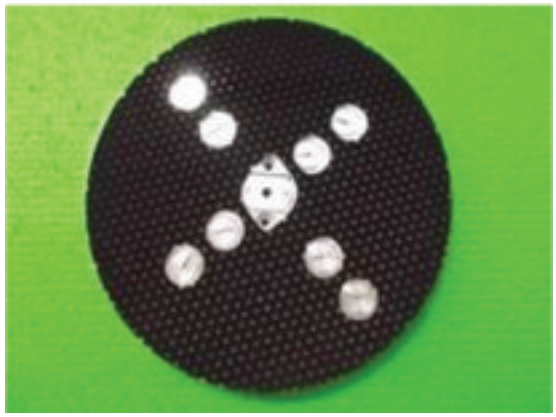


FIGURE 2. Load chuck from CMP tool showing location of DI water jets.

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FIGURE 3. Load chuck from CMP tool showing DI water spray.

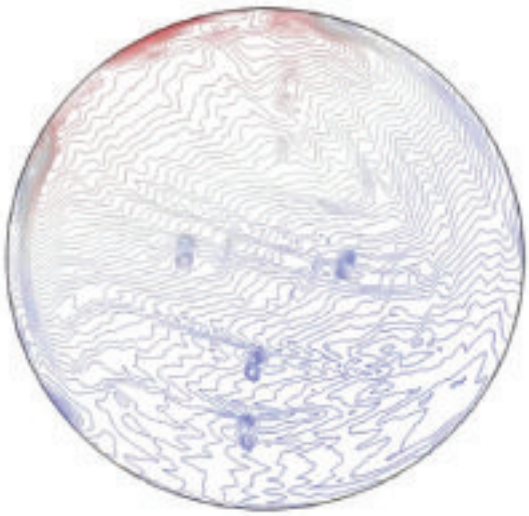

FIGURE 4. Charge map showing 3x higher oxide surface charge in areas impacted by DI water jets.

Subsequent experiments proved that transistor damage was occurring when DI water was used to elevate the (inverted) wafer from the load chuck to the polish head with jets of water causing static discharge in distinct locations (**FIGURES 2, 3**). Interim corrective action was taken to match the DI water pressure to the recommended setting of 20psi, with verification provided by both passive data and experimental results [3].

Since static electricity in triboelectric charging is caused by friction, we can apply the Bernoulli principle to estimate the relative change in static charge when dropping water pressure from 60psi to 20psi (**Equation 1**). This principle states that the sum of energy (kinetic and potential) in a fluid under steady flow must be equal at all points along the stream. In the case of water being ejected from a fixed nozzle, this would require that a drop in pressure (potential energy) results in a drop in velocity (kinetic energy) thereby reducing friction and static charge.

Equation 1: Bernoulli principle

$$\frac{v^2}{2} + gz + \frac{p}{\rho} = \text{constant}$$

Where:

v is the fluid flow (m/s)

g is the value of acceleration due to gravity (9.81m/s2)

z is the orifice size

p is the pressure (pascals)

ρ is the density of water (1000 kg/m3)

Solving for relative difference, we find that velocity is a function of pressure, such that reducing pressure from 60psi to 20psi will decrease the velocity by about 40 percent. Thus, we can predict a corresponding drop in static charge due to friction by the same amount. The relative difference in charge was validated by using a surface photovoltage (SPV) tool, which is a method of monitoring the potential of a semiconductor surface [4], **FIGURE 4**.

Tool 'fingerprint' analysis

Now that a physical explanation for how excess static charge was being applied to the face of product wafers had been defined, the next step was to understand why the resulting damage to the product circuit was always observed in a specific transistor (as opposed to being randomly distributed throughout the circuit). Through yield map signature analysis of the diagonal clusters of product die with a revised test screen, it was noted that while the clusters of failing die appeared at distinct radius dimensions from wafer center, their orientations were not fixed and, at first pass, seemingly random. However, upon closer inspection of the load chucks (**FIGURES 2, 3**), it was found that the water jets (appearing as a 'slit' style nozzle) had fixed orientations that were different from tool to tool.

This information led to an effort of correlating the nozzle position on each CMP tool to the orientation of diagonal clusters in the stacked yield wafer maps. This comparison made it possible to map yield loss sites from individual wafers to specific tools, and to identify that the damage was taking place at a specific layer for the product (second dielectric CMP, after metal-1).

Capacitive coupling

With the knowledge that the source of the physical damage was coming from triboelectric charging at one oxide CMP step , a working theory was created to show how the electric charge could find a path to ground from the front side (DI water jet) to the backside (grounded wafer chuck) of the wafer (**FIGURE 5**).

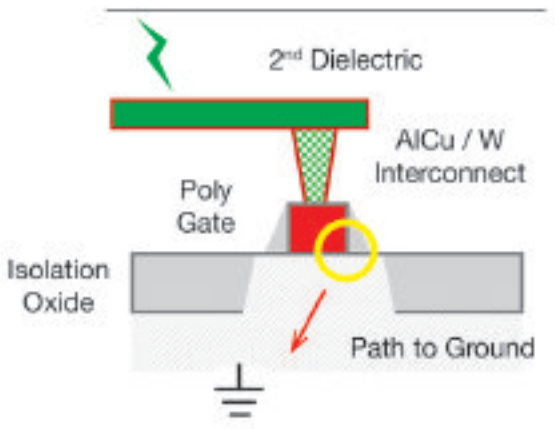

FIGURE 5. Path for charge transfer from oxide surface to grounded substrate.

Design considerations

In a design of more than 180 thousand transistors, it was significant that all failures mapped to a single NMOS transistor. This device was one of six identical structures, a two finger minimum sized 5V NMOS and the device was isolated from any external connections so charge coupling from an external pin was eliminated as a potential cause. Also, a review of metal-to-gate antenna design rules confirmed that there were no violations within the failing array and metal to gate ratios were well within the specification, with 10X margin. Since it was unlikely that a traditional antenna was the cause of the gate damage, additional aspects of the layout needed investigation [5].

Two areas of concern at the metal-1 layer under second dielectric were minimum metal spacing and adjacent metal routes for parallel lines. Investigation of the layout and design rules at this layer showed that minimum spacing of parallel lines was smaller than that of other metal layers, which would make the capacitance coupling between metal lines at this layer more significant.

Further analysis of the adjacent metal showed that this one transistor had a considerable amount of floating metal (prior to subsequent metal routing) adjacent to its gate metal compared to the five adjacent transistors. A model of capacitance between the floating metal and gate metal of the six structures showed that the LED5 transistor had a ratio more than 10:1 compared with ratios less than 1:1 for each of the other five transistors.

Our conclusion from these combined efforts was that failure of the single transistor in question was due to the unique layout of tight metal spacing and a high ratio of floating metal-to-gate metal, when under the influence of triboelectric charging from the fab CMP process.

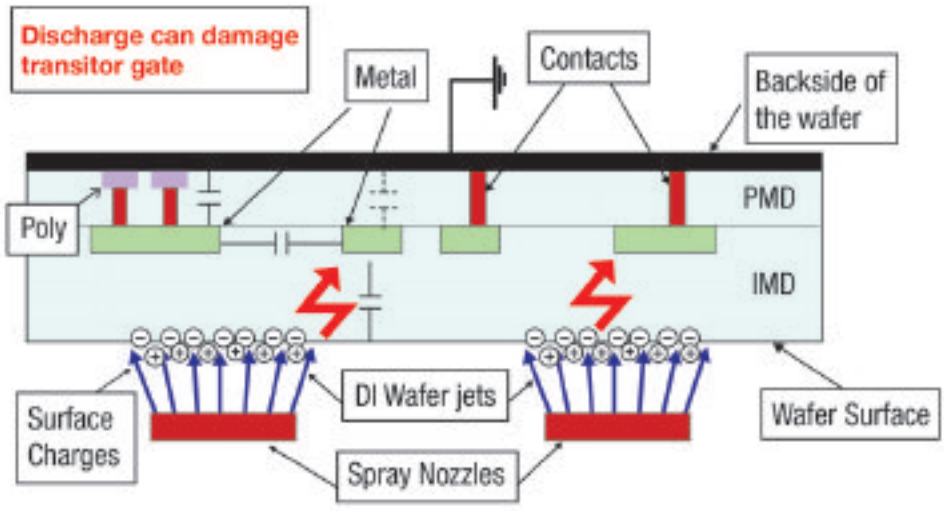

FIGURE 6. Discharge path from front side of wafer to ground.

An updated graphic (**FIGURE 6**) is used to show that charge is induced on the wafer (oxide) surface and coupled to the floating metal and finally, to the gate metal. The floating metal increases the effective gate metal capacitance such that it is now large enough to accumulate adequate charge to damage its gate oxide.

To prevent this effect from impacting future designs, an electronic design automation (EDA) approach was used to define conditions which would flag combinations of metal:gate antenna ratios and proximity of gate to floating metal.

Summary

Root cause of high leakage from a single transistor within a complex analog design was proven to be due to an interaction between triboelectric charging in the wafer CMP process and the unique layout of this structure. Process modifications were performed to reduce DI water pressure during the wafer handling sequence at CMP, a test screen was developed to yield off any future failures and ELFR / HTOL reliability verification was performed to insure no quality risk on finished goods. EDA design checks have been developed to flag structures with high ratios of spacing for floating metal to gate metal for sites with significant metal antenna ratios.

Acknowledgments

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System-level MEMS design – An evolutionary path to standardization

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For IC design, it took decades of academia and industrial endeavors for models, SPICE simulators, and foundry PDKs to emerge, mature, and converge into well-adopted industry standards. The MEMS modeling and simulation counterparts need to go through the same evolutionary path.

Successful design of highly-integrated IoT systems (**FIGURE 1**) requires simulating MEMS components together with the peripheral circuitry. However, MEMS devices are traditionally designed using CAD tools that are completely different from IC design tools. In the past two decades, both academia and industry have been seeking new methodologies and have chosen to implement multi-disciplinary MEMS design within the IC design environment. Performing MEMS-IC co-simulation in IC design environment allows designers to take advantage of advanced analog circuit solvers and the system verification capabilities that IC tools offer.

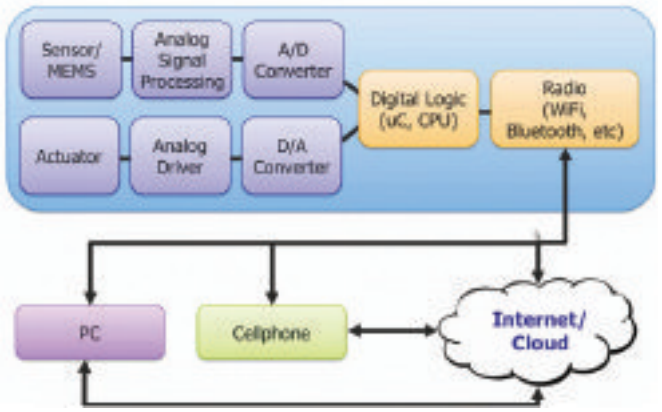

FIGURE 1. Typical IoT design.

A good system-level design methodology should facilitate MEMS device models and structure representations that are compatible with the IC design flow, and provide simulation accuracy and speed that are comparable or superior to typical analysis tools in the appropriate physical domains. It should also provide broad coverage of physical effects, and be able to support large systems. The three methodologies in use today for system-level MEMS modeling and simulation are:

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- Lumped-element modeling with equivalent circuits
- Hierarchical abstraction of MEMS and analytical behavioral modeling
- MEMS behavioral modeling based on Finite Element Analysis (FEA) and Boundary Element Analysis (BEA)

Lumped-element modeling with equivalent circuits

To implement SPICE-compatible modeling and simulation for MEMS, the most straightforward method is to create equivalent circuits for MEMS based on lumped-element modeling. For example, **Figure 2(a)** shows a spring-mass-damper system. A formal analogy can be derived between the mechanical and electrical elements, leading to an equivalent circuit "in series" topology as **Figure 2(b)** shows. Similarly, an "in parallel" circuit analogy can be derived as **Figure 2(c)** shows.

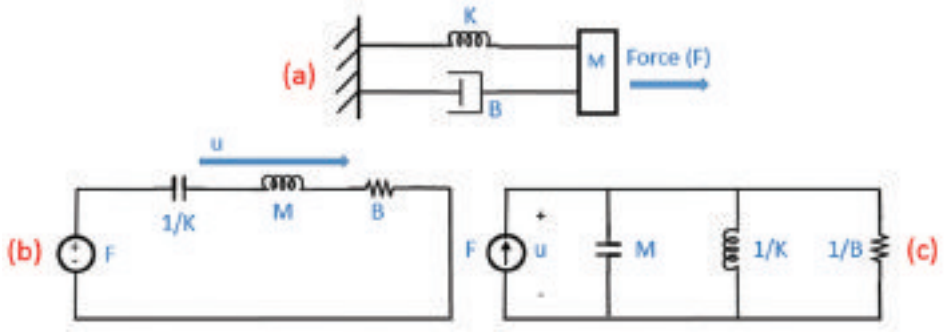

FIGURE 2. (a) A spring-mass-damper system (b) Equivalent "in series" circuit topology (c) Equivalent "in parallel" circuit topology.

Although the equivalent-circuit methods appear straightforward, designers must be aware of their viability and limitations. First, analogies shown in **Figure 2** are based on the assumption that MEMS structure can be significantly simplified into a spring-mass-damper system and that the effective mass, stiffness, and damping factor can be derived. This is only suitable for simple MEMS devices. For complex devices, the derivation could be too complicated and thus impractical to perform.

Secondly, the equivalent circuits are not easy to extend. Designers have to re-derive new models in order to account for additional physical effects or to adapt to changes in geometry, topology, or boundary conditions of the design.

Therefore, it is not uncommon for designers to determine that equivalent-circuit methods are too difficult or impossible to implement. More advanced methodologies are needed.

Hierarchical abstraction of MEMS and analytical behavioral modeling

In IC design, complex systems are built up hierarchically using building blocks at different abstraction levels. Hierarchical schematics are created to represent systems as structural networks comprising instances of these building blocks, connected together based on design topologies. Similar ideas have been explored and applied to MEMS design.

Figure 3 provides an example of the hierarchical abstraction of a folded-flexure resonator that contains a MEMS transducer and an electrical interface circuit. The MEMS transducer is an electrostatic device that is hierarchically built using a set of functional-level elements, each of which are further decomposed into atomic-level elements.

Behavioral models for MEMS elements can be written in analog hardware description languages such as Verilog-A, Verilog-AMS, and VHDL-AMS. Resulting models are compatible with SPICE simulators, thus serve well for co-simulation purposes. Analytical behavioral models for MEMS contain the following:

- Definition of terminals, with the associated physical disciplines specified.
- Definition of model parameters, including material and process properties as well as geometric sizing and layout orientation parameters.

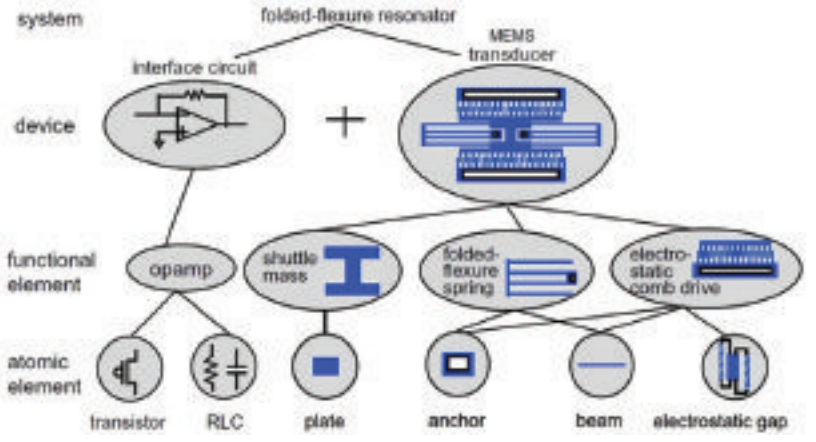

FIGURE 3. Hierarchical abstraction of a folded-flexure resonator.

Description of model behavior using a series of Differential Algebraic Equations (DAEs) that govern the relationship between, across and through variables of the terminals, with coefficients formed by parameters and internal variables.

It's crucial to obtain precise values of the material and process parameters in order for the models to match silicon. For standardized MEMS designs, foundries have started to develop and offer MEMS PDKs. For novel MEMS designs, designers have to fabricate test structures first then extract the parameters from lab measurement results.

After models are ready, they form model libraries that can be used for many designs in the appropriate design space. For example, atomic-level elements shown in **Figure 3** not only serve as the foundation for folded-flexure resonators, but also work for many other typical suspended MEMS designs, such as accelerometers, gyroscopes, resonator filters, micro mirrors, and RF switches. Model libraries make it possible for people unfamiliar with MEMS to use the models for system integration, and help protect MEMS IP.

Due to the large variety of MEMS designs in underlying physics, fabrication processes and design styles, no model library can be a universal solution that fits all. If the device employs unique, irregular geometries, or if the device involves physics mechanisms that are not well-understood, a new model has to be developed from scratch.

MEMS behavioral modeling based on FEA/BEA

Because geometry shapes supported by analytical models are discrete and limited, MEMS designers sometimes resort to Finite Element Analysis (FEA) and Boundary Element Analysis (BEA) tools. FEA/BEA tools use conventional numerical analysis methods for simulations in mechanical, electrostatic, magnetic, and thermal domains. They often rely on auto-meshers to partition a continuum structure into a mesh comprised of low-order finite elements. The tools then construct system matrices based on the meshing and solve the matrices within boundary conditions.

Efficient simulation of coupled physical domains is often a challenge to FEA/BEA-based tools. For example, to model the interaction between mechanical and electrostatic domains, some FEA/BEA tools must perform analyses for each domain separately and iteratively until a converged solution is found. Superior tools can simulate coupled domains all-together, but the simulation is computationally expensive and may result in unacceptable run times.

To alleviate limitations of FEA/BEA-based methods, while still utilizing their strength, Reduced Order Modeling (ROM) has been deployed, effectively bridging the gap between traditional FEA/BEA tools and electrical circuit simulators. ROM is a numerical methodology that attempts to reduce the degrees of freedom within system matrices to create macro models for MEMS devices. The resulting models can be constructed in languages like Verilog-A, then exported into SPICE simulators for co-simulation.

Up-to-date ROMs can be built not only from FEA/BEA results, but also from user-defined analytical equations and experimental data. Parameters in the reduced models can be preserved, so that design variations can be evaluated without going through the FEA and model order reduction process again. This enhances the coverage and efficiency of model libraries based on FEA/BEA and ROM.

Like all modeling methodologies, FEA/BEA-based methods cannot fully cover the entire MEMS design space either. Physical effects, as well as design and process imperfections, must be pre-defined in the original FEM/BEM model in order to be captured. In addition, creation of accurate models not only requires solid understanding of the underlying physics of MEMS devices, but also knowledge in both FEA/BEA tools and the model order reduction process.

Conclusion

To meet the need for MEMS-IC co-simulation, multiple modeling and simulation methodologies have been proposed, explored, and developed over the past two decades. Equivalent-circuit methods, structural analytical behavioral modeling, and reduced-order modeling based on FEA/BEA, are all effective methods and each has its own advantages and limitations. Knowing when to use which type of modeling method is important:

- When the design is small and simple, equivalent-circuit methods are the most straightforward.
- When the design is decomposable and the geometry, process, and dominant physical effects are close to what was used in the creation of primitive model libraries, hierarchical analytical modeling and structural system composition are the best choice.
- For unique designs using complex geometries, ROM methods based on FEA/BEA are more flexible and powerful.

For IC design, it took decades of academia and industrial endeavors for models, SPICE simulators, and foundry PDKs to emerge, mature, and converge into well-adopted industry standards. The MEMS modeling and simulation counterparts need to go through the same evolutionary path. This path has even more challenges than IC design, due to the much broader multi-physics coverage of MEMS and the diversity of MEMS manufacturing processes, applications, and design styles. Joint effort from design companies, foundries, and EDA tool vendors is required to enable this evolution.

Chipmakers seek solution to neon gas supply shortage

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Finding a short term solution to the neon gas shortage problem will be challenging.

When many people think of neon, they think of brightly lighted signs used in restaurants and other retail environments. The element neon (Ne) gives a distinct reddish-orange glow when used in either low-voltage neon glow lamps or in high-voltage discharge tubes or neon advertising signs. The red emission line from neon is also responsible for the well known red light of helium–neon lasers. Neon is commercially extracted by the fractional distillation of liquid air. It is considerably more expensive than helium, since air is its only source.

What those outside the chip industry likely don't know is that neon has been employed for semiconductor manufacturing for more than a decade, since deep ultraviolet (DUV) lithography came into widespread use starting with 248nm exposure systems. Why is neon important in lithography? Excimer lasers use gases like krypton fluoride (KrF) and argon fluoride (ArF) to generate light, and those gases are regularly changed out during use. However, a charge of excimer laser gas is actually about 98 percent neon, making this carrier gas essential to the laser's operation. Three main steps are involved in producing gas suitable for excimer laser use: (1) bulk neon production, (2) purification, and (3) final mix.

Today, the semiconductor industry is experiencing severe neon shortages, leading to price increases that are impacting end-users' bottom line. As a result, fab owners are rushing to secure enough neon to keep their facilities in operation, including buying the critical gas on the cash market and then having it purified and mixed to allow them to put it into use as quickly as possible.

Neon is a byproduct of steel production, but because it is a rare component of the waste gases, it must be recovered at very large steel plants. The former Soviet Union manufactured all of its oxygen plants for steel mills with neon, krypton and xenon capabilities and formerly worked on high-powered lasers as weapons, giving rise to significant neon capacity. Ukraine and Russia still operate the old-style massive manufacturing plants that have long since disappeared from Western countries, and have thus historically enabled the gas to be in over-supply.

From 1990 to 2012, many of these eastern European plants simply sent the crude neon into the atmosphere as no one would buy it. This over-supply began to tighten in 2014, as many old oxygen plants in Eastern Europe were either replaced by newer units without neon capability or shutdown altogether, especially with the contraction of the steel industry.

Why the shortage?

The neon crisis was triggered in part by conflict in the Ukraine, resulting in slowed production and escalating costs on the part of gas suppliers. Because neon is used for the majority of lithography light sources, the shortage caused many chip factories to face potential slowdown or even shutdown. In addition to gas prices increasing as much as 10 times over previous rates, chipmakers

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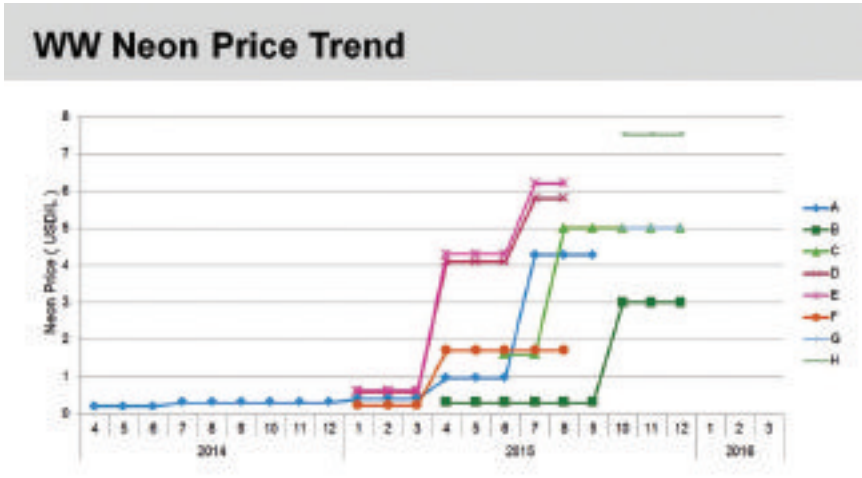

FIGURE 1. Neon gas pricing in USD for global chipmakers, compiled by Gigaphoton.

faced the prospect of a 15-percent or greater reduction in available supply of neon gas.

In China, old oxygen plants are being privatized or de-activated, or are being replaced by newer plants that lack the additional rare gas recovery investment. Even though there is a strong market for rare gases, the new plants are being put in without the rare gas capability due to a minimal ROI impact. Thus, while China has increased its market share in neon gas, the country's purification facilities are few and far between, so the country currently lacks production capacity for high-grade purification of neon gas. Regional specialty gas suppliers have also reported diminished supplies, all of which has had severe implications for the future of lithography and global chip manufacturing.

Between 2012 and 2014, the net effect of the neon supply shortage was around 125 million liters of lost annual production. In 2015, neon production, at 400 million liters, was falling short of demand by roughly 75 million liters.

A deeper look at the problem

Semiconductor-related lithography accounts for about 70 percent of worldwide neon demand. As mentioned earlier, an excimer laser uses a multi-gas mixture. The term "excimer" refers to the rare gas / halide molecule. Each fill is dedicated to the generation of a single wavelength. Four wavelengths can be generated from fluorine laser gas mixtures: 157 nm (F2), 193 nm (ArF), 248 nm (KrF) and 351 nm (XeF).

According to some reports, the price of neon gas skyrocketed in 2014, from roughly $1,000 for a 6,000-liter bottle of the gas, to approximately $6,000 for the same quantity as of late 2015. This is evident as seen in **FIGURE 1**, where the different colors represent the various global chipmakers. Neon gas, minerals, and the industry workhorse—silicon —are among the critical materials vital to semiconductor industry operations. The industry has had to deal with shortages in helium and rare earths in recent years, but was able to find at least temporary solutions.

Neon gas, on the other hand, appears to be a shortage for which finding a solution in the short term will be far more challenging. This problem is expected to continue for several years until a) sufficient new capacity comes on line, b) recycling can be implemented, or c) reprogramming of lasers can be accomplished, in order to allow for more efficient usage. In all likelihood, it will be a combination of all three of these factors that will alleviate the industry's neon supply challenges, although getting prices back down to a more affordable level is likely to take longer.

Neon conservation

In the meantime, the industry is looking at ways to conserve neon gas to help stretch its usage until such as time as the larger issues begin to be addressed in a more long-term fashion. Important developments in neon conservation include recent excimer laser gas usage optimization efforts that have been put in place by lithographic tool and laser equipment vendors to help end-customers reduce consumption. Optimization can be achieved via software updates for current systems and may result in up to 40 percent more efficient neon usage. In addition, recovery and recycling of neon may be relatively straightforward with few technical challenges, so several suppliers are proposing recycling and recovery plans.

With that said, the potential impact of these conservation efforts should be carefully considered, as some have the potential to put on hold, or even cancel, capital investment plans to produce more neon. This could mean the neon shortage would become exacerbated or prolonged beyond its current, already critical level.

To combat this crisis, Gigaphoton developed its unique Neon Gas Rescue Program, which expands on its previously announced program offering its eTGM technology for all new and existing GT series ArF immersion lasers.

The new program provides a more comprehensive package that includes the following:

1. A program for rapid qualification of new gas suppliers requested by customers. Previously, testing and qualification of a new gas supplier required anywhere from six to 12 months, but the new program will enable customers to begin using new gas suppliers much more quickly – cutting the qualification time down to as little as one month.

2. A limited, free-of-charge offer of the company's eTGM technology will also be extended to the G41K series KrF lasers and GT40A series ArF lasers. This extended offer will commence in November 2015. By introducing eTGM, customers can reduce the laser's neon usage by 25 percent on KrF and ArF lasers, and up to 50 percent on ArF immersion lasers.

3. The accelerated introduction of Gigaphoton's newest gas recycling technology, hTGM, which can be applied to all types of lasers. hTGM is expected to begin roll-out later this year. By implementing the hTGM technology, customers will be able to recycle up to 50 percent of their gas consumption.

Conclusion

While the semiconductor industry is facing a unique challenge with the current neon gas supply shortage, it has history on its side in terms of innovative solutions. The lithography sector, in particular, has repeatedly found ways to extend and revitalize technology applications.

How finFETs ended the service contract of silicide process

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A look into how the silicide process has evolved over the years, trying to cope with the progress in scaling technology and why it could no longer be of service to finFET devices.

Samsung and TSMC introduced their finFET devices in 2015 and joined Intel as the semiconductor industry's three major manufacturers possessing the most advanced technology. Intel's 14nm finFET 5Y70 processor was commercialized in 2014 and within six months Samsung mass produced their 14nm finFET Exynos 7 7420 SoC. Later that same year, TSMC started supplying their 16nm finFET based devices to Apple. Today Samsung and TSMC both supply their finFET based processors to Apple, which are being used for the iPhone6's A9 processor.

Since the release of the iPhone6 several blogs and articles have been written about the cost of fabrication, the performance of tri-gates, the type of work-function materials used by the manufacturers, the dominant supplier for Apple and speculation about the future of finFET devices. TechInsights has performed detailed structural analyses of these three devices and has also tried to understand some of these questions. While comparing these structural reports on finFET devices, one small detail stands out is that a major pillar of semiconductor processing is missing. The silicide process is not being used. Intel stopped using the silicide process in their 22nm finFET "Ivy Bridge" Processor. Samsung and TSMC at 20nm used the existing planar structure and employed NiSi on top of their source and drain regions. But as soon as these two device makers adopted finFET structure in 14 and 16nm nodes they abandoned the thirty year old silicide process. It is interesting to look into how the silicide process has evolved over the years, trying to cope with the progress in scaling technology and finally also why it could not anymore be of service to finFET devices.

The silicide process has been an integral part of semiconductor manufacturing since the early 1980s. The first patents were filed by Motorola, Fairchild and IBM. This process is used as an interface between semiconductor material and metals to reduce the contact resistance between tungsten contacts and the source-drain regions or the gate electrode. This parasitic resistance should be minimized to enable higher drive currents in transistors. Silicides have metal-like properties and are made by reacting Si to refractory or near-noble metals. A large number of metals in the periodic table can form silicides. The most common silicides in the semiconductor industry are titanium silicide, tungsten silicide, cobalt silicide, nickel silicide and nickel-platinum silicide. Platinium was used to stabilize the NiSi phase at a specific temperature. These compositions can exist in various phases and have unique phase diagrams. One particular integration process of silicides, known as self-aligned silicides (also termed 'salicide'), has played a significant role in bipolar devices, passives and in CMOS devices. In this scheme, no additional mask is needed; the silicide is grown on exposed silicon or polysilicon surfaces and not at all on neighboring dielectric surfaces.

The main steps of growing the silicide are depositing a refractory metal or a near-noble metal on the exposed Si and then annealing in a non-oxidizing atmosphere at a suitable temperature to react the metal with Si. The duration of the thermal cycle should be long enough to convert the majority of the metal to a silicide composition. Several stages of annealing may be completed to stabilize the phase. Thereafter the unreacted metal is removed

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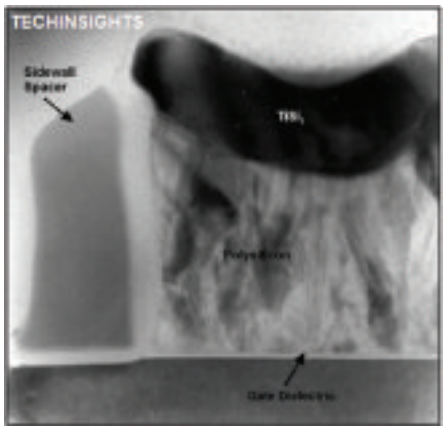

FIGURE 1. TEM cross-section of transistor structure of Intel A80502166 166 MHz Pentium Microprocessor (0.35 µm technology node) (source: A Structural Analysis of the Intel A80502166 166MHZ Pentium Microprocessor).

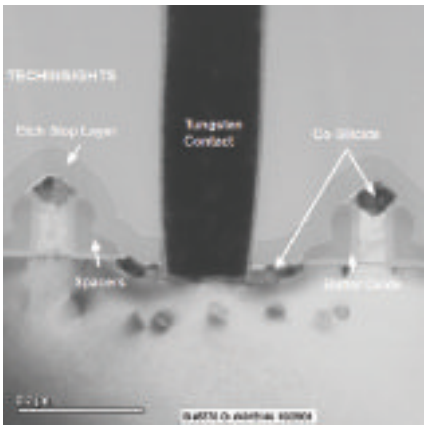

FIGURE 2. TEM cross-section of transistor structure of Intel Pentium-III 'Tualatin' Microprocessor (0.13 µm technology node) (source: A Structural Analysis of the Intel BX80530C1266512SL5LW Pentium III "Tualatin" Microprocessor using Copper Interconnect).

by wet-etching. For a detailed understanding of silicide process please refer to the book "Silicide technology for integrated circuits" by L.J. Chen or to the lecture notes from Professor Sarsawat from Stanford University [1].

The earliest image of the silicide process in TechInsights' database is from Intel's 166 Mhz Pentium microprocessor A80502166 based on a 0.35 µm CMOS process. The die markings of this device suggest that it was made in 1992-93. **FIGURE 1** shows a TEM cross-section of a gate employing titanium silicide. The transistors in this device have 0.40 µm thick titanium silicide on top of the gates and silicided diffusions formed using a salicide process.

The industry realized very quickly that $TiSi_2$ was not easily scalable. It has two phases C49-$TiSi_2$ and C54-$TiSi_2$. The first is formed at temperatures between 350 to 700° C and has a resistivity of 60-80 µΩcm; while the other is formed around 750° C and has a resistivity lower than C49-$TiSi_2$ (~20 µΩcm). As devices scaled down it became necessary to reduce the thermal budget which had the consequence of forming C49-$TiSi_2$ instead of C54-$TiSi_2$, which resulted in higher contact resistance. Since this was counter-productive, it was time to switch to a new silicide. Intel's Pentium III "Tualatin" used Co-silicide in a 0.13 µm CMOS process (**FIGURE 2**).

The next major milestone for silicide processes came at the 90nm node when Intel introduced the concept of raised source and drain for the PMOS transistor in their "Prescott" processor. The raised source and drain regions were formed by etching out portions of the Si substrate at the source and drain regions and then depositing epitaxial layers of Si1-xGex, where x is between 0 and 1. The etching out used both dry and wet chemistry. This concept was an innovative use of the growth rate variability on the bottom surface and on the side walls of the cavity due to the different crystal plane orientations of the silicon substrate.

SiGe has a lattice constant that is slightly larger than that of silicon so this epitaxial film induces a large uniaxial compressive strain in the PMOS channel region, resulting in significant hole mobility improvement. But SiGe surfaces were not very suitable for Co-Silicide. Most silicides have much lower free energy than germanides so when the silicide is formed on a Si-Ge alloy the Ge is expelled. This expelled Ge undergoes agglomeration and increases the contact resistance thus negating the effect of the enhanced mobility. The use of Ni instead of Co was especially beneficial for salicidation of both Si and SiGe source drain regions because Ni provides a more uniform contact resistance. Moreover, NiSi has the same resistivity as $CoSi_2$ but has smaller Si consumption. **FIGURE 3** shows Intel's 90nm "Prescott" transistor along with NiSi on top of SiGe regions.

NiSi was the mainstream process for two process nodes (90nm and 65nm) and was employed on top of polysilicon gate as well as on top of the source-drain regions. Around

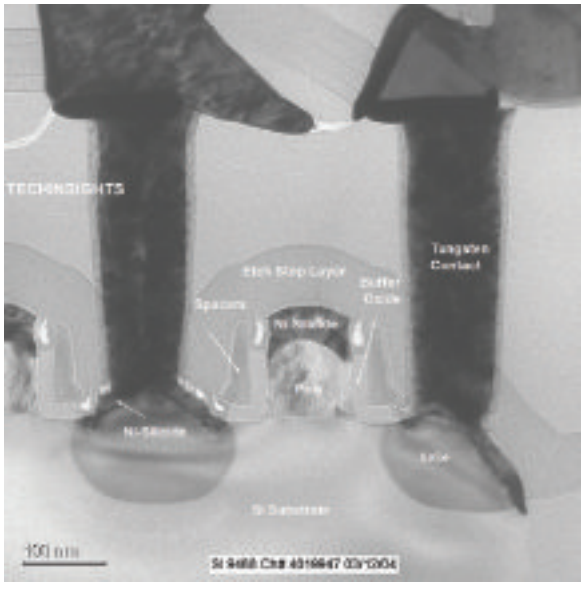

FIGURE 3. TEM cross-section of the transistor structure of Intel's 90nm "Prescott" processor with a gate length of 50nm and having raised source-drain regions of SiGe capped with NiSi (source: Detailed Structural Analysis I of the Intel Pentium 3.0E GHz Processor "Prescott").

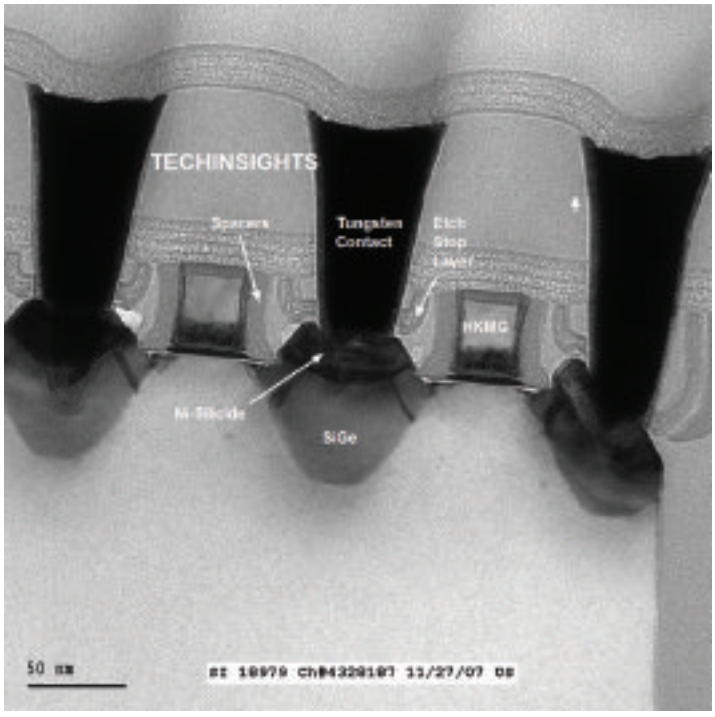

FIGURE 4. TEM cross-section of the transistor structure of Intel's 45nm "Penryn" processor with a high-k-metal gate (HKMG) having NiSi only in source-drain regions (source: Logic Detailed Structural Analysis including Process Flow on the Intel 45nm QX9650 Penryn Processor).

the year 2000, there were even discussions about a fully silicided (FuSi) gate. Then in 2008 Intel introduced the high-k dielectric and metal gate-last (HKMG) process at the 45nm node in their "Penryn" processor. This device did not require any more silicide on top of the gate but only at the source-drain regions. **FIGURE 4** shows a TEM cross-section of Intel's 45nm "Penryn" processor. In these devices, silicide is formed only on top of source and drain regions. The silicide is self-aligned to the sidewall spacer. The surface of the SiGe source-drain regions that is in contact with the silicide has enriched Si concentration to facilitate the silicide process. The nickel silicide depth from the silicon surface is about 65nm.

Finally, in 2012 Intel commercialized the first finFET device at 22nm in their "Ivy Bridge" (Intel core i5-3550) processor, in this device the silicide process was abandoned. To understand why the silicide process was not employed, it is important to grasp the differences between a tri-gate device and a planar device. Tri-gate brought in several advantages. For example, the effective gate width is proportional to the fin height and can be increased without increasing the device footprint. Additionally, because the gate wraps around the fin, there is better control of the channel. Another benefit is that the walls of the fin offer a different crystallographic plane than the top of the fin. Here, in this integration scheme the PMOS transistors benefit from higher mobility along the fin sidewalls.

The tri-gate integration scheme also brought in several process challenges. Epitaxial SiGe for PMOS and epitaxial Si islands for NMOS must be grown in a recess in a narrow Si fin rather than in the Si substrate. One constraint is due to double patterning, which requires that all the fins be of the same width and pitch; so if a larger gate width is required then multiple fins have to be employed. That means that the gate width is dependent on integer units of fins. This concept of integer units of fins is well illustrated in **FIGURE 5**, where the I/O transistor of TSMC finFET is shown having several fins connected in parallel.

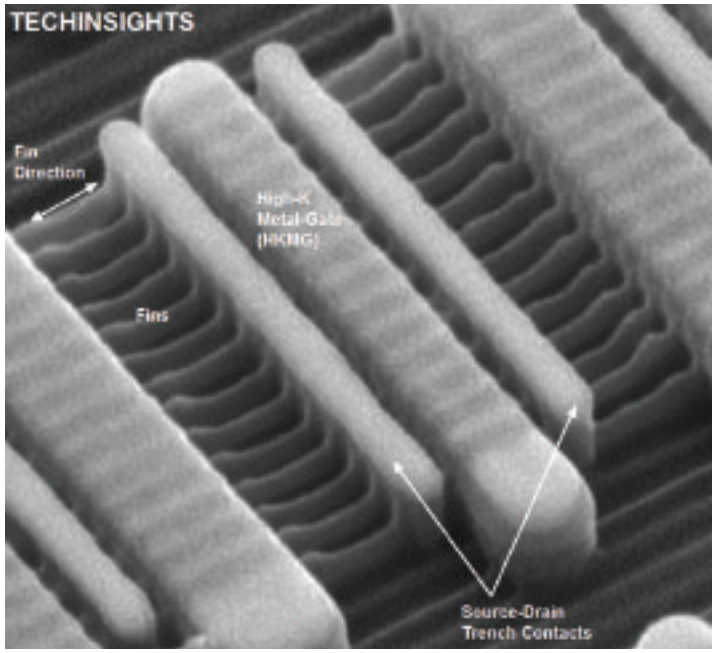

FIGURE 5. Tilted SEM cross-section of the I/O transistor structure of TSMC 16nm finFET device, showing 14 fins are connected in parallel by the same gate and by the same trench contacts (source: TSMC 16nm finFET Process in Apple A9 Processor - Logic Detailed Structural Analysis).

Multiple fins connected in parallel imply that the contact to the source-drain regions must have exactly the same contact resistance on multiple fins and this was indeed difficult to guarantee with the silicide process due to the vagaries of the diffusion process. In the Ni silicide process, it is believed that Ni atoms are the dominant diffusing species in Ni monosilicide formation; this property can lead to excessive silicidation on narrow lines. Ni-silicide is sensitive to temperature and often at low temperature a $NiSi_2$ is formed. This phase is usually seen on strained PMOS structures and can create an increase of contact resistance. Non uniform distribution of silicide process was the biggest show-stopper for this old process.

In addition to the silicide process there was also the problem of dopants in the source and drain regions. The thermal process causes undesirable dopant diffusion and leads to the loss of the junction abruptness. Also, thermal processes create thermal budget issues in the integration's process flow. There could be also other reasons for avoiding the silicide process in finFET devices, like leakage and stress because it is well known that the silicide process has an impact on device properties. Luckily, the technology of in-situ doping was already mature and used for DRAM devices as these volatile memories do not require a silicide process due to leakage concerns. Intel in its 22 nm process flow, most likely used in-situ doping of epitaxial regions along with trench contacts to eliminate the silicide process. This does not mean that other doping techniques like implants and thin film doping were not employed; they were probably used during different parts of the process flow. Intel did mention at IEDM 2014 that thin film doping method was used for 14nm finFET devices.

The introduction of trench contact, which ensure equal and low contact resistance to multiple fins was the ultimate reason not to use the silicide process in FinFETs. The integration flow is described in **FIGURE 6**. First, multiple parallel fins are formed. Each fin is separated from its neighbors by the STI-oxide. On these fins a sacrificial poly-silicon gate structure is made that runs perpendicular to the fins. On portions of the fin not covered by the gate, cavities are etched by using a line mask or a self-aligned process. Recesses in the fins are made by selectively etching the silicon. In-situ doped epitaxial layers are then grown to form source-drain regions. These epitaxial layers extend beyond the fin width and may even merge to form a continuous layer. The epitaxial layers do not extend above the surface of the fin. Subsequently, the poly-silicon gate is removed and the high-k-metal-gate (HKMG) formed in its place. A dielectric layer is deposited on top of the gates and the fins. The dielectric layer is patterned to form trenches running parallel to the gate. The integration scheme further includes etching a trench in the epitaxial layers and then filling the trench with tungsten to form trench contacts.

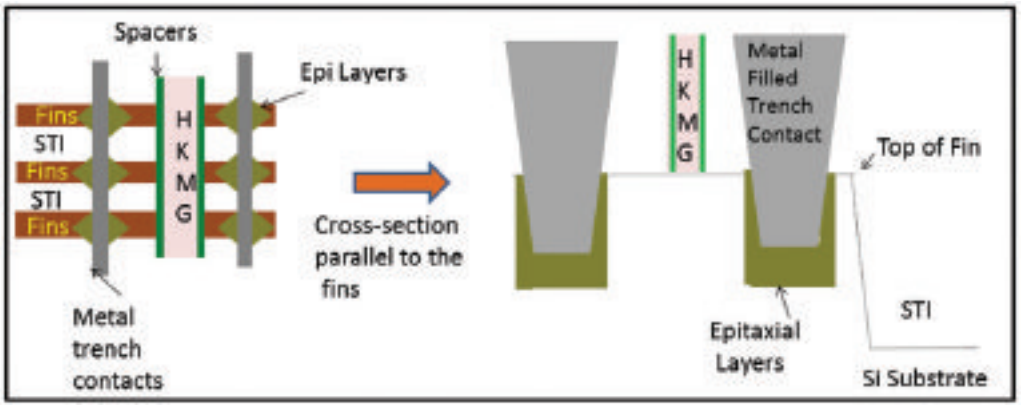

FIGURE 7. Schematics of how the trench contacts are embedded in the epitaxial layers.

FIGURE 7 shows the cross-sectional schematic diagram of how the trench contacts are embedded or well anchored in the epitaxial layers.

Cross-sectional images parallel to the fins of the three 1x node finFETs from Intel, Samsung and TSMC are collected in **FIGURES 8a, 8b and 8c**, respectively. The cross-section is made along one of the fins. The important point to note is that the trench contact at the surface of the source and drain regions is surrounded on three sides. It is more pronounced in the case of Samsung's device. The tungsten metal lines that run parallel to the gate, form the contacts for source-drain regions and are well anchored in the epitaxial layers. This increases the surface area of the contact and reduces the contact resistance.

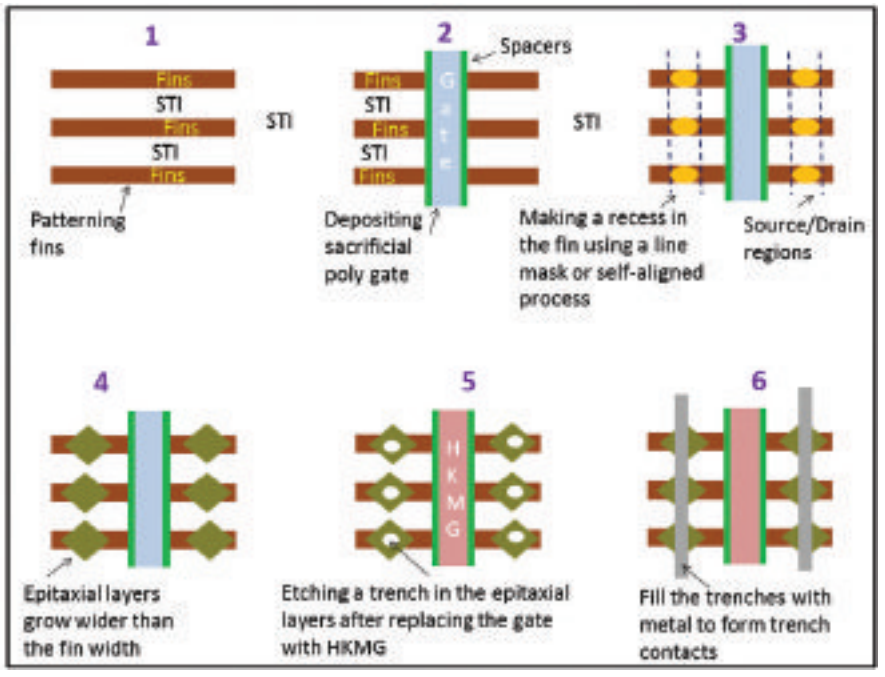

FIGURE 6. Schematics of forming the trench contacts in finFET devices.

FIGURE 8A. TEM cross-section 14nm node finFET devices from Intel. Cross-section is made parallel to the fins, showing the centre portion of the fin. (source: Logic Detailed Structural Analysis of the Intel 14nm 5Y70 Processor).

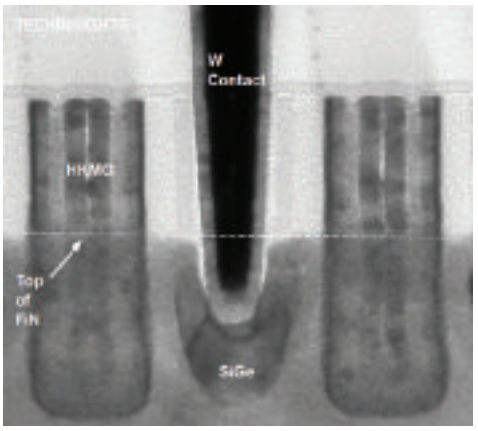

FIGURE 8B. TEM cross-section 14nm node finFET devices from Samsung. Cross-section is made parallel to the fins, showing the centre portion of the fin. (Source: Samsung 14nm Exynos 7 7420 Logic Detailed Structural Analysis).

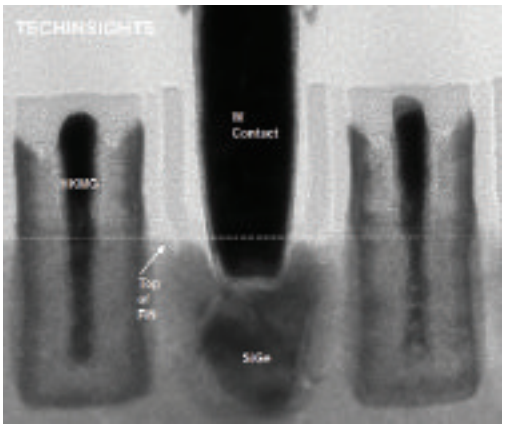

FIGURE 8C. TEM cross-section 16nm node finFET devices from TSMC. Cross-section is made parallel to the fins, showing the centre portion of the fin. (source: TSMC 16nm finFET Process in Apple A9 Processor - Logic Detailed Structural Analysis). Samsung 14nm Exynos 7 7420 Logic Detailed Structural Analysis).

FIGURE 9 shows the cross-section of the 16nm finFETs from TSMC in the direction perpendicular to the fins. In this direction the epitaxial regions could be designed to merge or extend beyond the fin width and thus increase the contact region with the metal contact. This increased contact region reduces the contact resistance.

The silicide process has a long history in the semiconductor industry; it has evolved through many phases from tungsten silicide to titanium silicide to cobalt-silicide to nickel silicide. But it could not be used for finFET devices. As for these devices, multiple fins may be used to form a single transistor, which implies that the contacts to all these fins have the exact same contact resistance. This is difficult to control in a process that is purely based on diffusion like the silicide process. So after 30 or more years of service it is time that the silicide process takes retirement and leaves the future to trench contacts and in-situ doping; however, there is always a possibility its use may be prolonged especially if the silicidation can be localized only inside the trench contact and not over the entire surface of the source-drain regions. Trench contacts will most likely be used in the next 10nm node but sub 10nm node, if new concepts like nanowire or new materials are introduced, the semiconductor industry is likely to innovate some other designs.

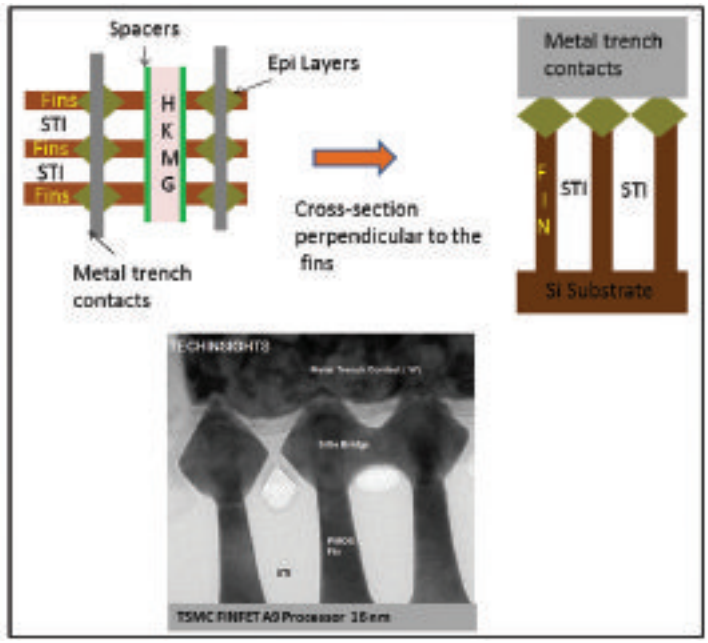

FIGURE 9. TEM cross-section 16nm finFET from TSMC. Cross-section is made along a trench contact and perpendicular to the fins. (source: TSMC 16nm finFET Process in Apple A9 Processor - Logic Detailed Structural Analysis).

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Managing hazardous process exhausts in high volume manufacturing

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Integrated sub-fab systems allow HVM fab operators to safely and efficiently implement new processes containing hazardous process chemicals.

The relentless scaling of structures and reduction in thermal process budgets that characterize state-of-the-art integrated circuit (IC) production have resulted in the incorporation of many complex and hazardous materials into high-volume manufacturing (HVM) processes. In order to meet the need to deposit these materials at ever-lower temperatures, many of the new process chemicals have low vapor pressures, are highly reactive and present serious hazards to personnel and equipment. Many new CVD precursors and their associated reaction by-products are flammable, pyrophoric, toxic (harmful-to-health), corrosive or otherwise hazardous to personnel or destructive to equipment, and have a tendency to condense in pipe-work, including process exhausts.

In this article we will review the risks associated with these materials and describe methods for mitigating process exhaust pipe hazards in high-volume manufacturing. In particular, we will describe an approach based on the integrating vacuum pumps and point-of-use abatement systems with essential safety devices and monitoring systems into a complete sub-fab vacuum and abatement solution. Such modular integrated sub-fab systems ensure safe system operation, including mitigation of process exhaust hazards, and reduce exposure of service staff to hazardous materials.

Process gas and reaction product hazards

Clearly, exposure of staff and equipment to hazardous chemicals leaking from process exhausts is a serious concern and careful attention to the design, control, safety qualification and maintenance of process exhaust systems is essential in configuring a safe and reliable sub fab operations.

The properties of process chemicals may be altered significantly as they pass through a process tool, and reaction products found in process tool exhausts may differ markedly from the original process precursors. For example, while high flows of tetraethylorthosilicate (TEOS) are widely used in CVD processes for deposition of silicon oxide films, the concentration of residual unreacted TEOS in a CVD process tool exhaust is minimal [1]. Instead, the TEOS is decomposed in the process chamber to form a greater volume of mixed hydrocarbon gases (ethene and ethanol, for example [2]), which are then pumped out of the process chamber into the process exhaust. When the safety of process exhausts is evaluated in the design of protective measures, interactions and transformations of process gases such as this must be considered carefully.

Deposition of hazardous materials in exhausts

In some cases, the process by-products which pass into the exhaust pipe are condensable. Frequently encoun-

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tered condensable by-products include aluminum chloride (AlCl3) in metal etch, ammonium chloride (NH4Cl) in LPCVD nitride, and ammonium hexafluorosilicate ((NH4)2(SiF6)) in PECVD nitride. Several of these condensates have also been found to incorporate partly-reacted hazardous materials. For example, partly-reacted silicon-containing compounds which condense in exhaust pipes during a PECVD process may react violently with fluorine gas which flows through the exhaust pipe during a subsequent chamber cleaning process. This has caused exhaust pipe fires and serious equipment damage in a number of cases (**FIGURE 1**).

In addition to the reactivity hazard posed by these materials, accumulation of condensed material during processing can block exhaust pipes, causing process tool downtime and possibly loss of production. Furthermore, the reaction of condensed fluorine- or chlorine-containing materials with atmospheric water vapor during removal and cleaning of exhaust pipes can release HF or HCl gas or other hazardous substances, posing a serious risk to service staff and requiring preventive measures.

A particularly serious example of harmful deposited materials in exhaust pipes is the condensation of extremely reactive polysiloxane materials in Si epi or Si-Ge epi exhausts [3]. These materials are particularly hazardous since they can react unpredictably and violently (explosively) on exposure to water vapor or air, or if they suffer a mechanical shock when the exhaust pipes are removed for cleaning.

The consequences of process gases escaping through leaks in exhaust pipes and the tendency of materials to condense in process exhaust pipes should be carefully considered when a process exhaust system is designed. Indeed, the exhaust pipe should be considered as an important functional element of the whole sub-fab process tool support system, otherwise there may be increased risks of staff injury and process tool downtime.

Leak integrity of process exhausts

Escape of process gases or reaction products from leaking process exhaust pipes presents serious risks to fab operations. For example:

- Flammable gas escaping from exhaust pipes may mix with air in closed spaces to create a fire risk
- Toxic gases leaking out of non-enclosed exhaust pipes present an injury risk to fab personnel
- Corrosive gases leaking out of non-enclosed process exhausts can harm personnel and cause severe damage to fab equipment
- Process gas odors may cause complaints from fab staff or local residents

Typically, area gas detectors are deployed in fabs to warn of process gas leaks. These are very effective in detecting escaping process gas, but when they are activated process

FIGURE 1. Consequences of byproduct condensation in process exhausts; left: solid ammonium chloride blocks an LPCVD silicon nitride process exhaust; middle: flexible stainless steel bellows perforated by corrosive by-product condensate; right: flexible stainless steel bellows ruptured by detonation of reactive solid condensate.

operations are interrupted and fab output affected. Furthermore, gas detectors cannot detect inward leaks into reduced pressure pump exhausts, such as air entering exhaust pipes where it could mix with flammable process gases to form flammable mixtures. In the worst case, a flammable process gas / air mixture could be ignited by a local ignition source, such as a dry-pump or point-of-use abatement system, and cause an exhaust pipe fire.

Configuring the vacuum/abatement/exhaust components as a single coherent system can increase staff safety and manufacturing efficiency by reducing the risk of hazardous process gas escape and ensuring appropriate action if a leak is detected In particular, integrated sub fab systems enable the use of extracted secondary enclosures around vacuum pumps, point-of-use abatement systems, fuel gas delivery systems and all interconnecting pipework to contain escaping gas, while ownership, maintenance and integrity of the process exhaust pipes becomes the responsibility of the system supplier, rather than remaining undefined.

Exhaust dilution

A standard safety precaution widely used to avoid the possibility of fires in process exhausts is the dilution of flammable gases below their Lower Flammable Limit (LFL). However, there are risks with this strategy. Considering the previously cited example, if the required dilution flow is calculated based only on the volume of TEOS gas in the exhaust pipe, it will be insufficient to dilute the larger volume of hydrocarbon decomposition products below their LFL. A related risk is formation of a flammable mixture in the exhaust if there is an air leak into the exhaust pipe coincident with the TEOS being decomposed by the process chamber. As noted above, the process dry-pump and point-of-use abatement system are both ignition sources that could ignite the hydrocarbon / air mixture and cause an exhaust pipe fire.

To operate process exhausts containing flammable gases safely using this strategy, not only must the dilution flow be calculated appropriately, but the vacuum and abatement system controller must include a capability to shut off the flammable gas flow from the process tool if the dilution flow should drop below some critical level, or if a fire occurs in the exhaust pipe, as required by semiconductor industry safety standards such as SEMI S18 [4].

In recent times, the risks associated with flammable and pyrophoric gases have become more severe as highly reactive compounds such as disilane and trimethyl aluminum have become more widely used in CVD processes. Some of these materials have extremely low LFLs – for example, disilane has a published LFL of 0.2% [5], and trimethyl aluminum is known to be extremely flammable though specific LFL data appears not to be widely available [6]. This characteristic makes their dilution to safe levels costly and inefficient from an operational efficiency perspective. For example, the low LFL of disilane requires a very large volume of nitrogen required to dilute it to a safe level, increasing the direct cost of the nitrogen and putting additional load on the fab facilities. The resulting high gas flow in the process exhaust increases the total cost of abatement by requiring larger, more expensive equipment, more sub-fab floor space, and a higher utility consumption. Finally, the abatement efficiency of highly-diluted process gases may be degraded, creating an environmental concern if emissions of process gas that exceed permitted levels.

Temperature control of process exhaust pipes

The risks posed by the condensation of process by-products in exhaust pipes can be mitigated by controlling the temperature of the exhaust pipes at a suitably high value (**FIGURE 2**). Commercial products are widely available to perform this function, but when selecting a suitable system, its capability to maintain a uniform temperature throughout the exhaust system

FIGURE 2. Heating elements and thermal insulation (red) enclose pump exhaust lines leading to the abatement system to maintain exhaust gases at a temperature high enough to prevent condensation.

should be considered carefully – in particular, cold spots caused by inadequate thermal insulation or lack of adequate real-time temperature control can cause localized by-product condensation and pipe blockage. At the other extreme, if exhaust pipes are heated to an excessively high temperature, unused CVD precursors may react, depositing solid materials in the exhaust pipe. Ideally, temperature will be actively and precisely controlled within a specified range.

Integrated sub-fab systems

Integration of the process exhaust pipe assemblies together with dry-pumps and point-of-use abatement into a complete sub-fab system by the equipment manufacturer permits an optimization of safety, performance, efficiency and cost that cannot be achieved in the installation of discrete units by individual suppliers.

FIGURE 3. Complete integration of vacuum pumps and abatement systems can lead to significant reductions in required abatement capacity, capital equipment investment, utilities consumption and total operating costs in a high volume manufacturing environment. Note in particular the reduced number of utility connections required to support four process pumps and a point-of-use abatement system in this specific example of an integrated system.

A typical integrated sub-fab system is designed to incorporate dry-pumps, point-of-use abatement systems, exhaust pipe assemblies, temperature management systems (TMS), together with all necessary safety devices, into a single entity which also includes a supervisory control system and all process tool and fab interfaces. Since all individual functional elements are integrated into a single unit, typically only one connection for each fab utility is required – not only does this reduce the overall installation cost of the sub-fab equipment, it also occupies less valuable sub-fab space. Each such integrated system is typically used to support a single process tool, and is usually designed to fit conveniently within the "shadow" of the process tool in the sub-fab.

This close integration of the individual sub-fab functional elements into a unified system enables a reduction in risks associated with exhaust pipe leaks by continuously monitoring the leak status of the exhaust pipes, by monitoring the air extraction rate in secondary enclosures, and by monitoring the temperature and pressure in the process exhaust pipes. In the event of an excursion by any of these parameters into a critical condition, an integrated system can be designed to initiate shut-down of the process gas through its interfaces to the process tool, and alert the fab MES through its interface to a central monitoring system (CMS). Furthermore, real-time collection and processing of data from all the functional elements in the integrated system allows events leading up to previous alerts to be analyzed. Predictive algorithms can then be developed that can enable the CMS to anticipate or predict future failure events.

Provided the safety features of an integrated sub-fab system are properly designed, including those which specifically monitor the condition of the exhaust pipes, it becomes practical to reduce dilution rates of flammable gases safely, leading to significant reductions in required abatement capacity, capital equipment investment, utilities consumption and total operating costs in a high volume manufacturing environment (**FIGURE 3**).

Implementation of Best Known Methods (BKMs)

Integrated sub-fab systems are typically built, installed and serviced by a single supplier, who takes responsibility for the complete system design, including all necessary safety functions and external interfaces. Safe sub-fab system operation is normally assured by a comprehensive safety assessment of the integrated system design and by compliance with global semiconductor industry safety standards such as SEMI S2 [7].

However, to ensure the most efficient operation it is also necessary to set-up the sub-fab system according to a Best Known Method (BKM) for each process tool. Application of process BKMs ensures that each integrated sub-fab system is fit-for-purpose to meet the specific requirements of its allocated process tool, and shortens the time required to qualify the tool for process. Typically, sub-fab equipment suppliers use know-how based on experience of similar processes in other HVM facilities to define their own BKMs and set-up equipment properly.

FIGURE 4. An example of continuous improvement and application of best known methods in a point-of-use abatement system: in a TEOS CVD process the standard inward-fired burner (left, after 9k wafers) was replaced with a shortened version (right, after 26k wafers). The resulting increase in surface firing rate greatly reduced unwanted deposition, improving the mean time between service (MTBS) from 10K wafers to 42K wafers.

Once an integrated system is operational, service support, applications support and continuous improvement programs (CIP) are all available from a single source which ensures that all critical safety systems are properly maintained and comply with the latest BKMs (**FIGURE 4**).

Summary

The concept of integrated sub-fab systems is a valuable tool that allows HVM fab operators to safely and efficiently implement new processes containing hazardous process chemicals. The integrated functionality and comprehensive safety systems guard against hazardous process gas escape, leakage of air into exhausts containing flammable gas, and condensation of a wide range of hazardous materials in exhaust pipes. Collectively these attributes enable the safest and most efficient sub-fab operation for HVM.

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A new class of MFCs with embedded flow diagnostics

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Recent trends in multi-sensor measurements within a mass flow controller are reviewed, with a focus on controller self-diagnostics.

Sub 20nm nodes and complex 3D architecture are driving new process control challenges. In regards to gas delivery, these complex and highly sensitive processes require mass flow controllers (MFCs) to provide better accuracy, repeatability, long term stability and consistent dynamic response. In addition, foundries are driving a need for greater process and equipment flexibility which means the MFC must meet demanding process requirements across a wider control range.

While the quality, reliability, accuracy, response and range of MFCs continues to improve year after year, the process is still at risk because meaningful real-time in situ data is limited or nonexistent. Consequently, an error in delivered flow that is substantial enough to cause yield and scrap issues would go undetected until the next off-line flow check.

In situ data traditionally has been limited to detecting obvious hard failures such as an MFC that is not communicating; the flow output doesn't meet the set point; or the MFC output at a zero set point is offset (not zero). A zero offset will cause a change in flow accuracy if it is due to an active change in the zero reference of the flow meter. However, zero offsets recorded during a process can also be caused by an MFC valve leak or even an isolation valve leak. A few fault detection and clarification (FDC) systems attempt to trend valve voltage but hysteresis of up to 40 percent of a reading means that only obvious failures can be detected.

In lieu of in situ flow data, flow tests are performed off-line using a technique such as chamber rate of rise (ROR). The ROR technique is simply to evacuate a known volume, flow gas into it and measure pressure change. With chamber ROR, the known volume is the processing chamber. The chamber is taken off-line (not running a process) and the MFC is given a flow set point. As gas flows into the constant volume chamber, the chamber pressure rises at a constant rate. Flow can be calculated using the gas law as shown in **FIGURE 1**. Off-line testing reduces tool availability and can only detect flow errors after the fact, placing wafer lots at risk. Chamber ROR accuracy is +/- 3 percent of reading to +/- 5 percent of reading, depending on flow rate, gas properties, temperature gradients, manometer accuracy and chamber outgassing. Even if a better flow standard is available, flow tests are time-consuming. Chamber ROR testing every MFC at only one set point on a four-chamber etch tool can take 12 hours and is typically performed weekly.

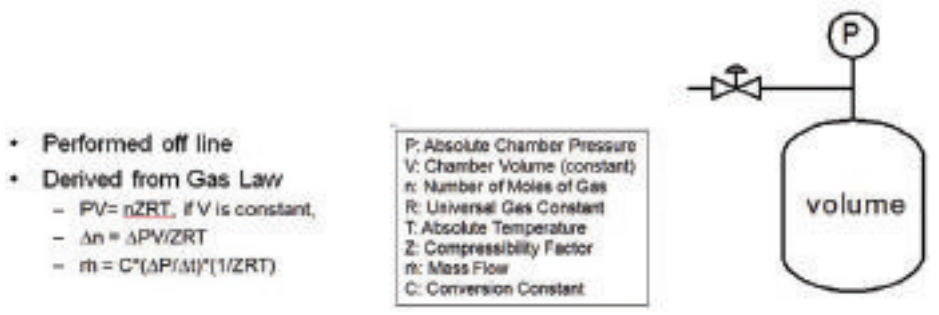

FIGURE 1. Rate of Rise (ROR) measurement technique.

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Process engineers are seeking an in situ flow verification process to ensure process repeatability enabling real-time FDC to alarm on conditions that could lead to wafer scrap. In situ flow data could also be used to intelligently determine when to take a tool down for flow verification tests instead of running time-consuming weekly flow maintenance checks on all MFCs.

The evolution of the MFC

In 2004, MFC manufacturers developed pressure transient insensitive (PTI) MFCs. Pressure sensors were added to measure fluctuations in pressure and advanced control concepts were introduced to compensate for pressure fluctuations in real time.

Recently, several manufacturers have experimented with using pressure and temperature signals available in PTI MFCs to determine if the controller accuracy is degrading. (The authors have used the phrase "multi-sensor diagnostics" to describe this new class of advanced MFCs). Every multi-sensor diagnostic technique involves some form of pressure rate of decay (ROD). ROD is similar to chamber ROR except instead of flowing into a constant volume and measuring the pressure rise, flow is released from a constant volume and the rate of pressure decay is measured. The concept has been around for 30 years and involves shutting off an upstream valve to create a constant volume and measuring the pressure drop within the volume. The technique wasn't practical until digital processors with enough computational power were available to perform the technique.

Multi-sensor diagnostic instrumentation can be broken into two groups. The first group (idle self-diagnostic) can only perform self-diagnostics while the tool is idle or in between process steps. Pressure decay in the volume is measured but there is no attempt to control flow. The signature of the pressure drop is compared to a previous measurement and analyzed to look for changes. While considered an improvement, this technique does not provide true in situ data and a dynamic event during a process could easily go undetected. The second group (active self-diagnostic) actively controls process steps while the pressure decay is measured. Although more challenging to implement, this technique enables true in situ flow verification (**FIGURE 2**).

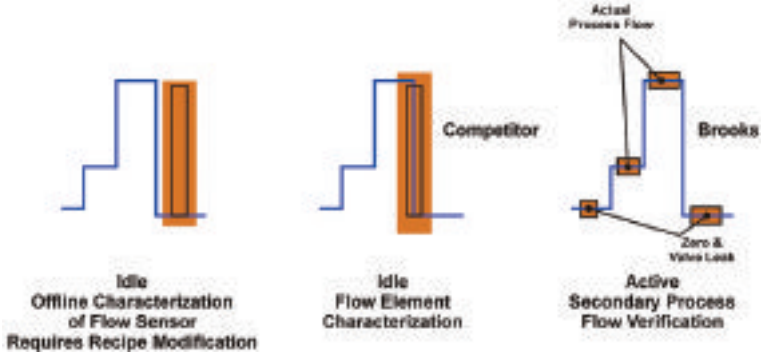

FIGURE 2. Comparison of idle and active self-diagnostic during wafer processing.

Examples of idle self-diagnostics

Example 1 - thermal MFC: The upstream isolation valve is closed and the position of the flow control valve is frozen. The MFC then records pressure decay. The characteristics of the pressure decay curve are compared to a baseline curve. Changes in the curve are trended to determine if a flow sensor is degrading (**FIGURE 3**). Special maintenance checks would have to be programed into the tool controller to take advantage of this technique as it cannot be triggered during a normal process run.

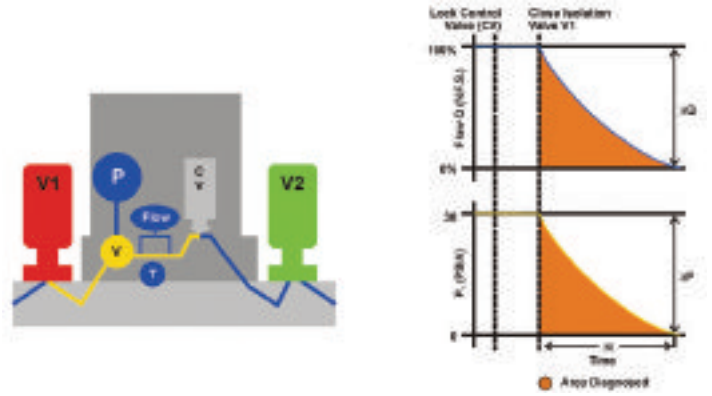

FIGURE 3. *Thermal MFC idle self-diagnostics.*

Example 2 - pressure-based MFC: Traditional pressure-based MFCs measure pressure drop across a laminar flow element (LFE) (**FIGURE 4**). The valve must be placed upstream for two reasons. First, the pressure measurement is more accurate and stable if P2 is vacuum;

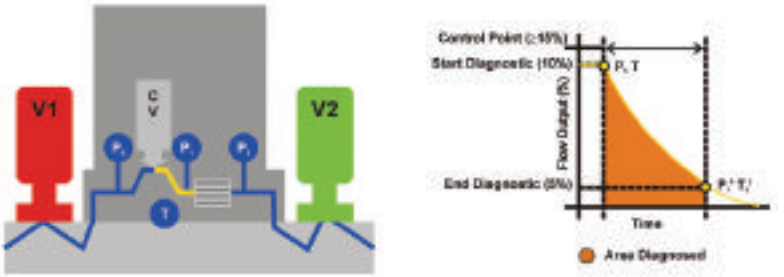

FIGURE 4. Pressure-based MFC idle self-diagnostics.

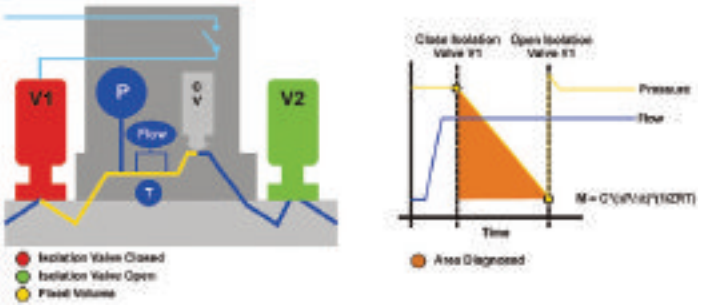

FIGURE 5. Thermal MFC active self-diagnostics.

second, this method requires a stable inlet pressure, P1. The downside to placing the valve upstream is slow turn off. The gas must bleed through the laminar flow element after the gas is turned off. The bleed downtime is a function of gas properties, the laminar flow element volume upstream of the LFE, and pressure in the upstream volume. For multi-sensor diagnostics, the manufacturer takes advantage of the bleed-down and characterizes the pressure decay every time the MFC is given a command to shut off. Any deviation from baseline signifies a change in either the LFE flow path or pressure sensors, and would trigger the user to perform a maintenance check.

Active self-diagnostics

Unlike idle self-diagnostics, where MFC characterization is performed when the MFC is not running a process, the latest development in multi-sensor self-diagnostics enables true in situ flow verification. This means flow anomalies can be captured in real-time during a process and assessed before several wafers are affected.

FIGURE 5 shows the cross-section of a multi-sensor self-diagnostic MFC mounted on a traditional surface mount gas stick. In this example, the MFC contains a pilot valve that enables the MFC to control the state of the upstream isolation valve. Other implementations integrate the isolation valve into the body of the MFC.

The MFC closes the upstream isolation valve when it is ready to take a secondary flow measurement. This creates a fixed volume between the isolation valve and the MFC control valve. While pressure decays in the volume, the MFC control system continues to maintain flow while recording pressure, temperature and time. A secondary flow measurement is computed based on the pressure decay (ROD) and compared to baseline data recorded during the installation of the MFC on the tool. Once this measurement is complete, the MFC re-opens the isolation valve. PTI technology is used to compensate for the initial pressure spike, ensuring continued stable flow. The same measurement technique can be used to monitor zero drift and valve leak when the MFC is given a zero set point.

Case study on etch process tool at leading IDM

Two multi-sensor MFCs capable of active self-diagnostics were installed on an etch chamber at a major integrated device manufacturer. The MFCs were configured to store accuracy, zero drift and valve leak self-diagnostic data in flash memory located within the MFC. Performance transparency tests were run with self-diagnostics activated to ensure the technology did not change the process. The process engineers continued to perform regular off-line flow verification tests at a set point of 30 percent. No accuracy issues were detected by the traditional maintenance tests and no adjustments such as re-zeroing or re-calibration were performed. Data was collected for 24 months.

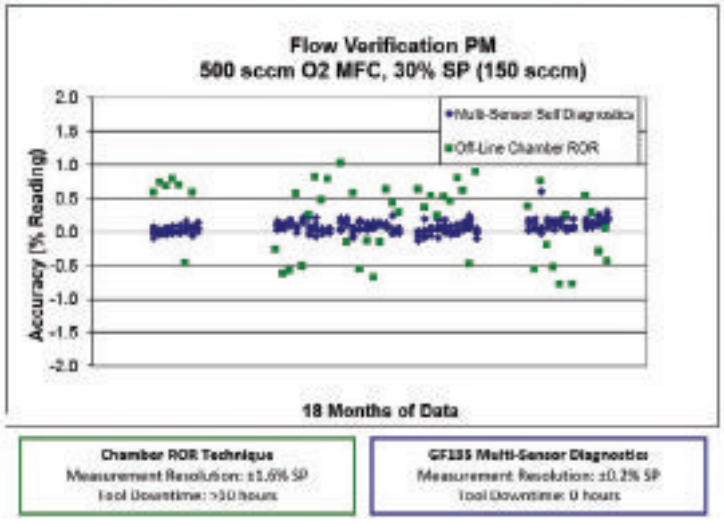

FIGURE 6. Chamber ROR flow verification vs. multi-sensor self-diagnostics.

Active multi-sensor diagnostics vs. off-line chamber ROR: Self-diagnostic data was collected during the regular off-line flow verification tests. **FIGURE 6** shows that repeatability of self-diagnostics was 8X better than the time-consuming off-line flow verification tests.

Active flow accuracy: The etch process utilized MFC set points of 4 percent, 12 percent, 24 percent and 40 percent (**FIGURE 7**). In situ active self-diagnostic data was automatically collected at each set point every three seconds during wafer processing. The MFC flow accuracy was very repeatable over the two-year test period at

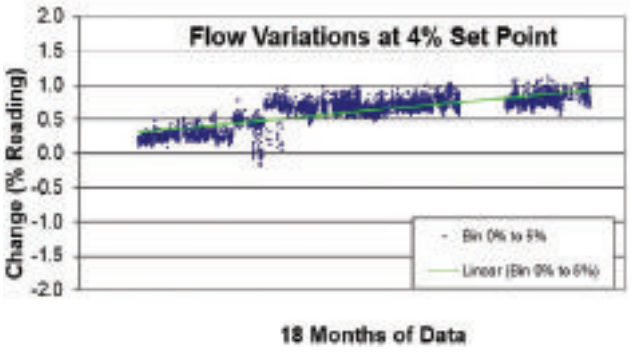

FIGURE 7A. In situ flow accuracy results.

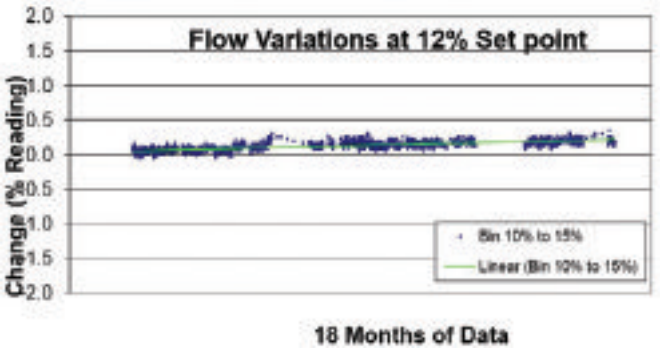

FIGURE 7B. In situ flow accuracy results.

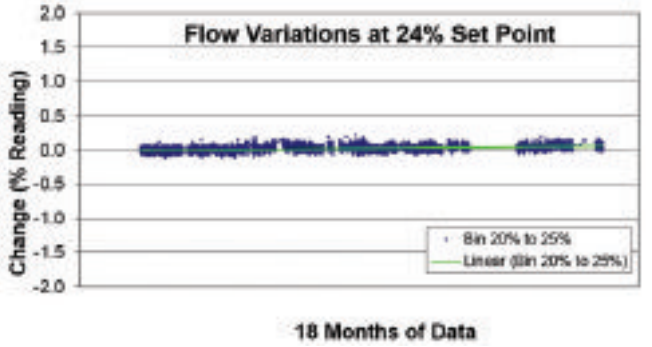

FIGURE 7C. In situ flow accuracy results.

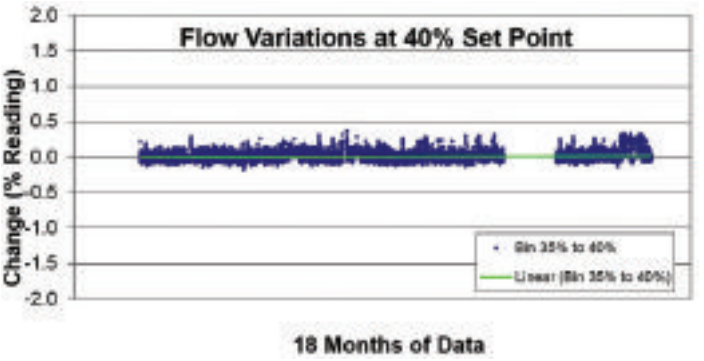

FIGURE 7D. In situ flow accuracy results.

set points of 24 percent and 40 percent. However, flow accuracy at 4 percent shows an increase in flow of 1 percent over the two-year evaluation period. Note that off-line flow verification tests were only performed at a set point of 30 percent where the MFC is stable. Traditional off-line chamber ROR flow tests proved not only to be costly, but also ineffective in detecting flow changes in this case.

In situ zero drift trending: Increasing flow errors at low set points usually indicate a change in the zero of the flow meter. The output of a flow meter should be zero at no flow. However, all measurement instruments will eventually drift resulting in some level of zero offset. A small zero offset in the flow meter is a negligible part of the flow signal at a high flow rate. However, small zero offsets can become significant when the MFC is operated at low set point such as 4 percent shown in this tool data. Consequently, the self-diagnostic zero reading was analyzed to see if the accuracy error at a 4 percent set point correlated with zero drift.

The MFC zero drift rate was < 0.027 percent full scale (FS) per year. This is exceptionally stable and 20X less than the spec limit (**FIGURE 8**). No maintenance test performed today on-tool would identify this low level of zero drift. This data highlights recent

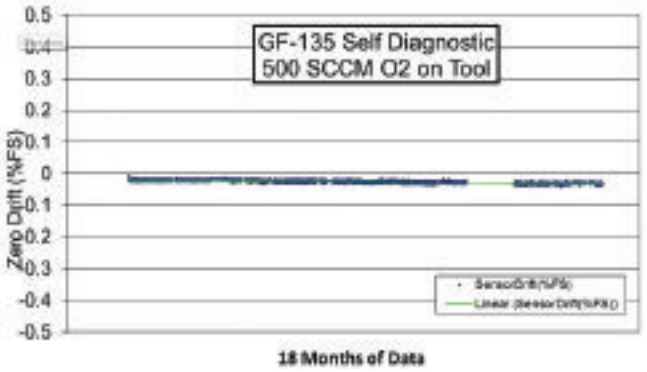

FIGURE 8A. In situ zero trending results.

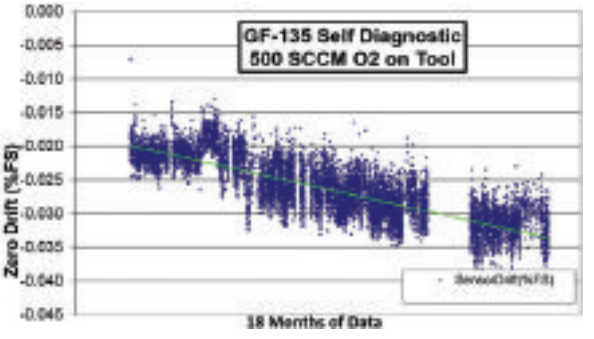

FIGURE 8B. In situ zero trending results (20X magnification).

improvements in the stability of thermal MFCs. However, expanding the zero drift axis does reveal a slight trend in zero of 0.045 percent FS. This offset is exactly equal to the 1.1 percent of reading flow error identified during process runs at the 4 percent set point.

Valve leak: Valve leak is linked to first wafer effects and can indicate contamination in the gas delivery line. Excessive valve leak can cause loss of control at low set points. Self-diagnostic valve leak was trended during this study. The MFC valve leak was extremely low and stable throughout the study (**FIGURE 9**). Process engineers typically get concerned when valve leak reaches 0.5 percent FS to 1.0 percent FS. The data reveals excellent resolution of the valve measurement and demonstrates how easy it would be to detect changes in valve leak well before it could affect process yield.

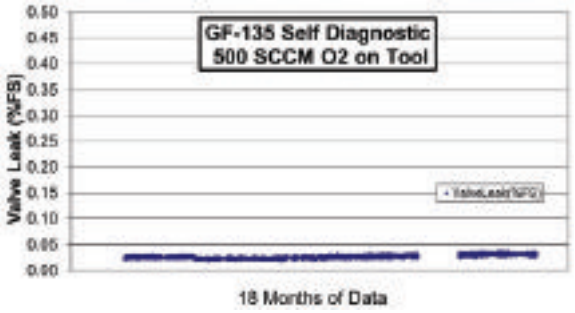

FIGURE 9. In situ valve leak results.

TABLE 1 compares data and resolution available in situ from a traditional MFC; a tool in idle mode; a tool off-line; and the active multi-sensor self-diagnostic data captured in this study. The process knowledge gained from this technology enables the process engineer to be proactive instead of reactive. In addition, an intelligent FDC system could use this data to identify more subtle MFC issues such as excessive sensitivity to changes in pressure or temperature, and even leaks in the gas stick isolation valves.

Conclusions

This data highlights how current best known methods for MFC on-tool monitoring and off-line maintenance are unable to capture changes in process and ensure repeatability.

The on-tool study demonstrated multi-sensor self-diagnostic MFC technology is a process-transparent upgrade with the capability to:

- Track flow changes in situ with 10X better resolution than currently available for off-line flow verification processes
- Enable advanced fault detection and classification where MFC performance is tracked while running process, and logic trees can be set up to determine root causes of process degradation
- Increase tool up-time, where determining the root cause before taking the tool off-line will minimize downtime; reduce or eliminate scheduled flow-verification tests; reduce troubleshooting; and reduce tool maintenance
- Eliminate MFC-induced wafer scrap, using an alarm to alert for conditions that may lead to wafer scrap before producing product.

	Flow-Related Process Data Available to FDC System			
Data Type	Traditional MFC In Situ Data	Tool Off-line	MFC w/ Idle Self-Diagnostics	MFC w/ Active Self-Diagnostics
MFC Output	+/- 0.05 % SP		+/- 0.05 %	+/- 0.05 %
Temperature	+/- 1 °C		+/- 1 °C	+/- 1 °C
Inlet Pressure	+/- 0.1 PSI		+/- 0.1 PSI	+/- 0.1 PSI
Valve Voltage	Varies +/- 20%		Varies +/- 20%	Varies +/- 20%
MFC Zero		+/- 0.05 %F		+/- 0.02 %F
MFC Valve Leak		0.05 %FS		0.02 %FS
Changes in Flow Accuracy		+/- 1 %SP	TBD	+/- 0.3 %SP
Detects Flow Deviations During Wafer Process				Yes

TABLE 1.

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Trace metal contamination: Choosing elastomer materials for critical operations

KNUT BEEKMANN, *Precision Polymer Engineering (PPE), part of the IDEX Sealing Solutions Group, Blackburn, England*

An exploration of where trace metals come from, the impact they have on the industry and what can be done to reduce the risks.

Triboelectricity is defined as a charge of (static) electricity generated by friction. The concept was first applied in the 1940s for electrostatic painting and is now widely used in photocopy machines. This phenomenon becomes a concern in wafer manufacturing processes since water is a polar molecule and deionized water (~18MOhm) is a good insulator [1, 2].

When working at the nanoscale of microchip production, even low levels of contamination have the capacity to alter the electrical characteristics of the device and affect the reliability of the end product. Operational hygiene has always been an issue due to the sensitivity of semiconductors to contaminants, but the threat of trace metal contamination specifically is significant. This is mainly true for front end processing but, due to the high mobility of many of these contaminants, it remains a threat at all stages of the manufacturing process flow.

Trace metal constituents of elastomer seals can be released as byproducts during erosion of the seal in aggressive plasma or chemical environments that are part of routine process tool operation. Contamination of semiconductor devices by trace metals adversely affects device performance and as linewidths decrease, the allowable levels of metal contamination reduce. This article explores where trace metals come from, the impact they have on the industry and what can be done to reduce the risks.

Background

Semiconductor microchips, which provide inexpensive, fast computing power for electronic devices, are made from millions or even billions of transistors. The transistor is fundamentally an electronic switch that contains no moving parts but uses an applied low voltage to the gate which in turn allows electrons to move from the source to the drain.

The overall chip making process involves many repeating steps to form the transistor at the front end, and subsequent formation of the back end interconnect including multiple metal and dielectric levels and several etch steps in between. In the process of building these layers, many transistors are created and interconnected. When completed, a single wafer will contain hundreds of identical chips that must pass rigorous testing. The chip is then mounted onto a metal or plastic package that undergoes final testing, ready to be assembled into final products [1,2].

During routine operation, many components within the process tools and ancillary equipment will be subject to wear and abrasion, particularly those components within the process module that are directly exposed to harsh physical and chemical environments. The most critical locations are those where components are exposed to such environments and in proximity to the substrate being processed.

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Equipment consumable items that can sometimes be overlooked are elastomer seals or O-rings. These materials have a certain lifetime proportional to the mechanical and chemical properties of the operating environment and the physical constraints of the groove and location. While an elastomer in a critical location may not actually determine the maintenance cycle of the process tool, byproducts and elastomer constituents will be released into the process environment during active operation. Therefore, whatever constitutes the elastomer can contaminate the wafer and this applies equally to the trace metals.

Trace metal contaminants fall broadly into two categories. Alkali metals which include elements such as sodium (Na), potassium (K) and lithium (Li) and heavy metals which include elements such as copper (Cu), iron (Fe), zinc (Zn), titanium (Ti) and chromium (Cr). The effects on the device of such contaminants vary depending on the type of the element. Sodium for example, can readily lose its outer electron to form an ion with charge +1. It can then readily diffuse through the oxide under the influence of an electric field even at room temperature, however; it cannot penetrate the silicon crystal lattice which means that a charge can accumulate at the silicon/silicon dioxide interface. This in turn leads to unpredictable voltage threshold shifts and correspondingly random digital outputs from logic circuits.

Additional failure mechanisms include current leakage through the dielectric and reduced dielectric breakdown voltage, degradation of time dependent dielectric breakdown (TDDB), or complete breakdown of the gate [3]. Gettering layers are also no guarantee of eliminating the issue. Phosphosilicate glass (PSG) and borophosphosilicate glass (BPSG) layers are often used to getter sodium ions, however, the presence of moisture either through integral process steps or atmospheric absorption can facilitate the release of trapped mobile ions in the getter [4]. Rather than accumulate at the semiconductor interface, heavy metals tend to diffuse through the semiconductor, where they effectively create energy states in the bandgap of the semiconductor causing changes in carrier lifetime or the diffusion length [5].

Consumer demands for faster, more powerful and portable technology with greater functionality is a key factor driving the semiconductor manufacturing industry. Although the part of Moore's law that refers to shrinking technology remains largely intact, the pressure on cost reduction is rising throughout the whole value chain [6]. Reduced device dimensions and gate thickness leads to devices that become more sensitive to a number of factors including trace metal contamination.

It is clear that such contamination leads to unstable device performance, yield loss, device degradation with increased risk of reliability failures, potentially costing the fab in lost time, loss of revenue and wafer production capacity.

Purity in elastomers

When choosing elastomer materials or seals for critical applications, device manufacturers must ensure that they select appropriate materials with ultra-low levels of trace metals, in order to avoid contamination and device degradation. Manufacturers must also decide on the material in accordance with the location in the tool and the chemistry involved. Critical locations where the elastomer is in contact with the chemistry or process media, where degradation takes place, and where the byproducts of this degradation can be transported to the wafer, require the highest quality seal material in order to avoid contaminating the device. The sealing product must precisely fit the characteristics of the operating equipment.

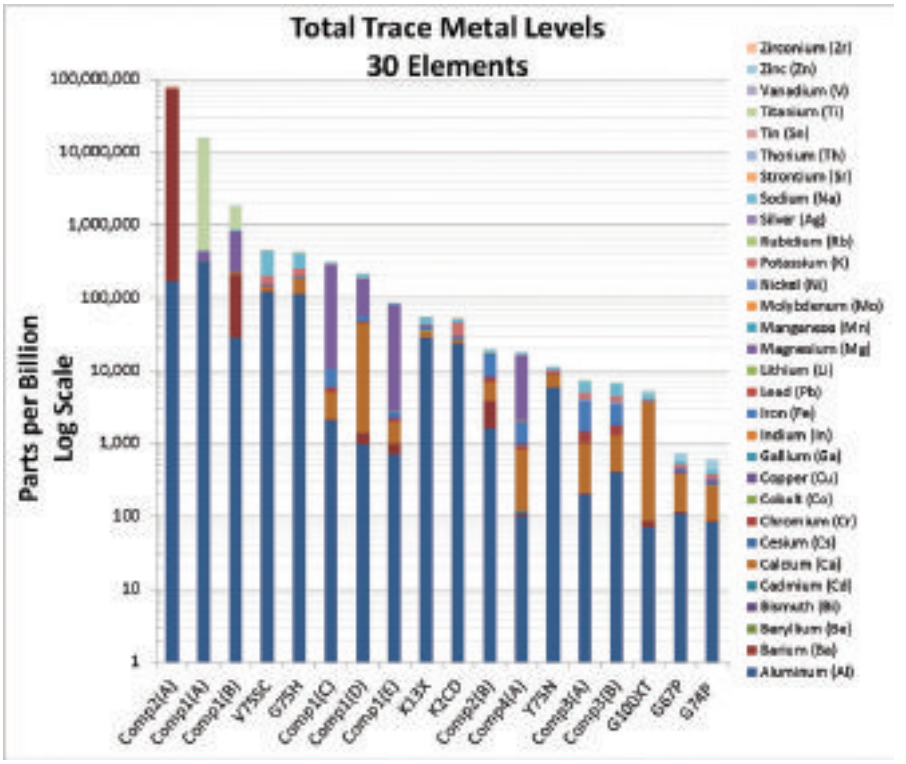

FIGURE 1. Comparative VPD ICPMS testing of elastomer materials.

There is often a large choice of products for any one particular application and 'semiconductor compatibility' is often taken for granted especially in critical applications. However, not all elastomer materials are equal when it comes to the level of undesirable contaminants. For many device applications, it is no longer adequate to measure contamination at the parts per million (PPM) level. When analyzing trace metal levels in elastomer materials, vapor phase decomposition (VPD) combined with inductively coupled plasma mass spectrometry (ICPMS) yields data down to parts per billion [7]. A number of different elastomer materials have been analyzed by an independent test laboratory in order to quantitatively determine the amount of trace metal within each sample. The materials analyzed include the leading elastomer brands and the results are graphically represented in **FIGURE 1**. It should be particularly noted that In order to accommodate all the samples tested, a log scale was used.

The results show that the elastomers that achieved the lowest trace metal content of all materials tested were entirely organic perfluoroelastomers, or FFKMs. The cleanest fluoroelastomer or FKM material was found to be Nanofluor Y75N, again a fully organic highly fluorinated elastomer. **FIGURES 2, 3 and 4** below illustrate the individual levels for several of the key contaminants that should be avoided for three of the cleanest materials tested.

FIGURE 2. G74P trace metal content.

FIGURE 3. G67P trace metal content.

FIGURE 4. G100XT trace metal content.

Conclusion

It is clear that the seal lifetime is not the only factor that should be considered when making elastomer choices for specific applications. Elastomer or seal wear in key tool locations during normal operation exposes the wafer to the degradation byproducts of the elastomer material, and therefore also the impurities contained within the elastomer, such as trace metals. FFKM elastomers are particularly suited to the most critical applications, and the harsh environments presented by higher temperatures, aggressive wet chemical and plasma processes. The more aggressive the environment and the more sensitive the device, the greater is the need to consider the contaminating degradation byproducts of the system components.

Contamination ultimately results in loss of yield, increased cost, or loss of reputation. The use of high purity components becomes a preventative measure, guarding against costly transistor damage or increased risk of poor reliability. Elastomer materials that contain only ultra-low levels of metallic contaminants are ideal for manufacturers of devices at advanced technology nodes and all fabs wishing to minimize the risk of random changes to electrical characteristics and reliability failures.

For further information about how to integrate high performance elastomer seals into your production equipment, and to understand the benefits of customized sealing solutions please contact the author at kbeekmann@idexcorp.com.

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Overlooked semiconductor technology plays a key role in secure IoT

Over the past 40 years, the semiconductor industry has worked hard to miniaturize ICs, and has stayed very much in line with Moore's eponymous prediction. In fact, the latest frenzy into the sub-20nm node and beyond has been primarily driven by smart phone applications, an industry that is constantly looking for new points of differentiation as the market rapidly matures and manufacturers are challenged to find new novel features to entice consumers with. The latest application processors for Apple and Qualcomm, which are running on 14nm and 16nm foundry nodes, are perfect examples. In this stampede to be at the leading edge, the industry has inadvertently deserted a many technology and capacity capabilities of the semiconductor manufacturing process.

The industry's single-minded focus on advanced technology has left mature modular process nodes between 180nm and 90nm, on 8- or 12-inch wafer size, to be set to the side. Yet there is a wealth of process technologies and ready libraries in this process range for engineers to build perfectly marketable ICs, such as ASIC's and SoCs, that optimize designs traditionally found in conventional PCB-based sub-assembly or module applications.

When you add the advancement of sensor technologies like MEMS, radiofrequency, optical circuits, all the ingredients are there to create some very interesting products for markets where size is just a little less preoccupying than it is in smart phones and tablets.

The up and coming IoT market, which is expected to double in size in the next four years, is the perfect match for these technologies. While combining sensors, analog to digital conversion, local processing, storage, secure element hardware, and communications in a single application is not new to the industry, rethinking of these IoT applications in industry, home, cities, health, and transportation with a view to taking advantage of semiconductor integration is new. And thanks to mature/mainstream semiconductor technologies, it is both possible and economically viable. Designing a chip on older fab nodes can often be accomplished within a $5 million US dollar budget!

With the advent of independent service suppliers at different stages of the semiconductor manufacturing process, fabless companies do not need to be a major players in the industry to make their own ICs. Market forecasters, like Gartner and McKinnsey, have predicted that the IoT will generate thousands of new applications for electronics and semiconductor consumption. I expect that this new demand will make its way into custom IC's, because the required infrastructure is already there and using it is easier and less expensive to do than it was only a few years ago.

I see a paradigm shift on the horizon. Integrating and miniaturizing multifunction systems using older process technologies may be a bit less glamourous than the long running chase to minimize devices and process geometries, but it will be an important transition for the industry.

Editor's note:

Presto Engineering recently expanded its turnkey capabilities with the opening of two new manufacturing hubs and a world-wide logistics center in Asia.

As an outcome of its partnership with Inside Secure, announced April 2015, Presto Engineering is taking on the facilities in Asia, adding footprint; significant expertise; and a new, enhanced suite of services for Presto's customers. Presto Engineering now offers a complete and comprehensive turn-key product engineering and production management solution for integrated circuits (IC), from GDSII hand-off (design output) to finished ICs shipped directly to end customers, targeted at the latest in high-speed communication, Internet of Things (IoT) and secured elements markets.

The new operations are located in Bangkok, Thailand; Kaohsiung, Taiwan; and Hong-Kong, SAR. To Presto's existing capacity in the US and Europe, they add 20+ probe test cells, advanced die prep capabilities, and payment module manufacturing in secured (EAL5+/EAL6) floors, ready to support large projects with unit volumes of 10 million or more. ◆

CÉDRIC MAYOR, *Chief Technical Officer, Presto Engineering, Inc., Caen, France*

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