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MARCH 2017 VOL. 60 NO. 2

Haptics are increasingly being paired with VR technology to further enhance the gaming user experience.

COVER

FEATURES

COLUMNS

DEPARTMENTS

editorial

New approaches to scaling needed

Applied Materials hosted a panel session in December in San Francisco during the International Electron Devices Meeting, titled: "Rethinking Scaling: New Paragdigms, New Approaches."

My main takeaway was that scaling has we have come to know it over the last 30 years was driven by lithographic shrinks, and that's come to an end. "Scaling has stopped. It's clear, said Rama Divakaruni, technical executive, advanced process technology, research and systems interaction, IBM Research.

That's the bad news. The good news is that if we redefine scaling to include new approaches such as 3D structures and packaging, there are many ways for scaling to continue to evolve. "Whatever technology we need to achieve the power, performance, cost and area scale performance required is what is called scaling," said Raman Achutharaman, Corporate VP, etch business unit at Applied Materials, who was the panel moderator.

"We are going away from scaling just thinking of it as single dimension. Now scaling is getting into multiple dimensions as the end market drivers are evolving," Achutharaman said. New applications, whether it's mobility, cloud computing, big data, autonomous cars, robotics, health care, and others are driving a need to look at new paradigms, he added. "We are in a cusp where on one hand people think the industry is becoming very challenging but on the other hand actually it's pretty exciting because there are a lot more new applications coming up," he said.

PR (Chidi) Chidambaram, VP of engineering, QCT Process Technology, Qualcomm, rightfully pointed out that the semiconductor industry is behind on meeting new consumer demands. "In a cell phone today, the digital has become less relevant simply because we effectively scaled the power and area but not really offered to solve any of the user experience demands," he said. In the process, display and RF has started becoming bigger consumers of power, he said.

Chidambraram said the next big opportunities are in integration, including what he called "silicon in package" integration. "We are trying to look at putting together many of the pieces and integrating the system, but the truth is if you just took off the shelf any of our chips and stack them and there is really no power advantage that we can get right now as is. There has to be a lot more innovation that has to happen to to realize the benefit from this. That's really the challenge," he said.

Divakaruni said the "magic of scaling" the semiconductor enjoyed in the past increased performance (faster!), increased density (smaller!) and decreased cost per transistor (cheaper!). But in the FinFET era, he said scaling slowed. While performance increased (faster!), he gave only half credit to increase chip-level density (sorta smaller) and to decrease in transistor cost (sorta cheaper!). Quoting Meatlof lyrics from 1977, Divakruni said, "Now don't be sad. 'Casue two out of three ain't bad."

—Pete Singer, Editor-in-Chief

Solid State TECHNOLOGY

Pete Singer, Editor-in-Chief
Ph: 978.470.1806,
psinger@extensionmedia.com

Shannon Davis, Editor, Digital Media
Ph: 603.547.5309
sdavis@extensionmedia.com

Ed Korczynski, Senior Technical Editor,
edk@extensionmedia.com

Dave Lammers, Contributing Editor

Phil Garrou, Contributing Editor

Dick James, Contributing Editor

Vivek Bakshi, Contributing Editor

CREATIVE/PRODUCTION/ONLINE

LS Jerrett, Production Traffic Coordinator

Nicky Jacobson, Senior Graphic Designer

Simone Bradley, Graphic Designer

Slava Dotsenko, Senior Web Developer

MARKETING/CIRCULATION
Jenna Johnson,
jjohnson@extensionmedia.com

CORPORATE OFFICERS

Extension Media, LLC
Vince Ridley, President and Publisher
vridley@extensionmedia.com

Clair Bright, Vice President and Publisher
Embedded Electronics Media Group
cbright@extensionmedia.com

Melissa Sterling, Vice President,
Business Development
msterling@extensionmedia.com

For subscription inquiries:
Tel: 847.559.7500; Fax: 847.291.4816;
Customer Service e-mail: sst@omeda.com;
Subscribe: www.sst-subscribe.com

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Web Exclusives

Edge placement error control in multi-patterning

SPIE Advanced Lithography remains the technical conference where the leading edge of minimum resolution patterning is explored, even though photolithography is now only part of the story. Leading OEMs continue to impress the industry with more productive ArFi steppers, but the photoresist suppliers and the purveyors of vacuum deposition and etch tools now provide most of the new value-add. Tri-layer-resist (TLR) stacks, specialty hard-masks and anti-reflective coatings (ARC), and complex thin-film depositions and etches all combine to create application-specific lithography solutions tuned to each critical mask. (From SemiMD.com)

http://bit.ly/2miYPid

Intel EMIB implementation in the Stratix MX

At the recent IEEE ISSCC in SF, Intel discussed the implementation of their EMIB technology [Embedded Multi-die Interconnect Bridge] technology in the Altera Stratix 10 FPGA family designed to meet the needs of developing high end communications systems. Dr. Phil Garrou, Contributing Editor, reports.

http://bit.ly/2meJzmn

Taiwan maintains largest share of global IC wafer fab capacity

IC Insights recently released its new Global Wafer Capacity 2017-2021 report that provides in-depth detail, analyses, and forecasts for IC industry capacity by wafer size, by process geometry, by region, and by product type through 2021. Taiwan led all regions/countries in wafer capacity with 21.3% share, a slight decrease from 21.7% in 2015 when the country first became the global wafer capacity leader. Taiwan was only slightly ahead of South Korea, which was in second place.

http://bit.ly/2meGP8A

n&b news and blogs

Insights from the Leading Edge: SEMI ISS 2017: A period of uncertainty?

SEMI's annual Industry Strategy Symposium was held at its usual site, Half Moon Bay, CA a few weeks ago, and it seemed like this year's overall message was one of an industry searching.

http://bit.ly/2lk1U0v

Huge growth in cloud memory changes semiconductor supply chain

The explosive growth in demand for internet bandwidth and cloud computing capacity brings a new set of technology challenges and opportunities for the semiconductor supply chain.

http://bit.ly/2m5n5oz

SEMI 2020: "There are far better things ahead than any we leave behind"

Denny McGuirk, SEMI president and CEO, writes about where the industry is going and how SEMI is changing to keep up with it.

http://bit.ly/2ls90hG

AMOLED production equipment purchases to reach record high in 2017

The flat-panel display (FPD) industry is in the midst of a historic wave of building new factories to manufacture active matrix organic light emitting diode (AMOLED) displays. This will drive $9.5 billion worth of AMOLED-specific production equipment purchases in 2017, according to IHS Markit.

http://bit.ly/2lDAJ0S

Is a stretchable smart tablet in our future?

Engineering researchers at Michigan State University have developed the first stretchable integrated circuit that is made entirely using an inkjet printer, raising the possibility of inexpensive mass production of smart fabric.

http://bit.ly/2kWG6Vj

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news

worldnews

USA - **Brooks Instrument** named Mohamed Saleem as new Chief Technology Officer.

EUROPE – The Flemish government announced an increase of financial support of **imec.**

ASIA - **Seoul Semiconductor** started mass production of its patented filament LEDs.

USA - **Veeco** entered into agreement to acquire **Ultratech**.

ASIA - **GE Ventures and Samsung Electro-Mechanics (SEMCO)** announced a global microelectronics packaging patent agreement.

ASIA - **GlobalFoundries** 12-inch wafer production line in Chengdu commenced operation.

USA - **Applied Materials** CTO Dr. Om Nalamasu was elected to the National Academy of Engineering.

ASIA - **Toshiba** started construction of Fab 6 and memory R&D center at Yokkaichi, Japan.

USA - **NXP Semiconductors N.V.** announced that Marcel Pelgrom is the recipient of the 2017 Gustav Robert Kirchhoff Award from the **IEEE**.

ASIA - **Qualcomm** and **TDK Corporation** announced the launch of a joint venture under the name RF360 Holdings Singapore PTE. Ltd.

Intel announces $7B investment in next-gen semiconductor fab in Arizona

Intel Corporation announced plans in February to invest more than $7 billion to complete Fab 42, a project Intel had previously started and then left vacant. The high-volume factory is in Chandler, Ariz., and is targeted to use the 7 nanometer (nm) manufacturing process. The announcement was made by U.S. President Donald Trump and Intel CEO Brian Krzanich at the White House.

According to Intel's official press release, the completion of Fab 42 in 3 to 4 years will directly create approximately 3,000 high-tech, high-wage Intel jobs for process engineers, equipment technicians, and facilities-support engineers and technicians who will work at the site. Combined with the indirect impact on businesses that will help support the factory's operations, Fab 42 is expected to create more than 10,000 total long-term jobs in Arizona.

Context for the investment was outlined in an e-mail from Intel's CEO to employees.

Intel plans to invest more than $7 billion to complete Fab 42. On completion, Fab 42 in Chandler, Ariz., is expected to be the most advanced semiconductor factory in the world. (Credit: Intel Corporation)

"Intel's business continues to grow and investment in manufacturing capacity and R&D ensures that the pace of Moore's law continues

Continued on page 6

GlobalFoundries reveals expansion plans

GLOBALFOUNDRIES announced plans in February to expand its global manufacturing footprint in response to growing customer demand for its comprehensive and differentiated technology portfolio. The company is investing in its existing leading-edge fabs in the United States and Germany, expanding its footprint in China with a fab in Chengdu, and adding capacity for mainstream technologies in Singapore.

"We continue to invest in capacity and technology to meet the needs of our worldwide customer base," said GF CEO Sanjay Jha. "We are seeing strong demand for both our mainstream and advanced technologies, from our world-class RF-SOI platform for connected devices to our FD-SOI and FinFET roadmap at the leading edge. These new investments will allow us to expand our existing fabs while growing our presence in China through a partnership in Chengdu."

In the United States, GF plans to expand 14nm FinFET capacity by an additional 20 percent at its Fab 8 facility in New York, with the new production capabilities to come online in the beginning of 2018. This expansion builds on the approximately $13 billion invested in the United States over the last eight years, with an associated 9,000 direct jobs across four locations and 15,000 jobs within the regional ecosystem. New York will continue to be the center of leading-edge technology development for 7nm and extreme ultraviolet (EUV) lithography, with 7nm production planned for Q2 2018.

In Germany, GF plans to build up 22FDX 22nm FD-SOI capacity at is Fab 1 facility in Dresden to meet demand for the Internet of Things (IoT), smartphone processors, automotive electronics, and other battery-powered wirelessly connected applications, growing the overall fab capacity by 40 percent by 2020. Dresden will continue to be

Continued on page 7

Intel continues to drive semiconductor industry R&D spending

Intel continued to top all other chip companies in R&D expenditures in 2016 with spending that reached $12.7 billion and represented 22.4% of its semiconductor sales last year. Intel accounted for 36% of the top-10 R&D spending and about 23% of the $56.5 billion total worldwide semiconductor R&D expenditures in 2016, according to the 20th anniversary 2017 edition of The McClean Report that was released in early 2017. **Figure 1** shows IC Insights' ranking of the top semiconductor R&D spenders based on semiconductor manufacturers and fabless suppliers with $1 billion or more spent on R&D in 2016.

Intel's R&D spending is lofty and exceeded the combined R&D spending of the next three companies on the list. However, the company's R&D expenditures increased 5% in 2016, below its 9% average increase in spending per year since 2011 and less than its 8% annual growth rate since 2001, according to the new report.

Underscoring the growing cost of developing new IC technologies, Intel's R&D-to-sales ratio has climbed significantly over the past 20 years. In 2010, Intel's R&D spending as a percent of sales was 16.4%, compared to 22.4% in 2016. Intel's R&D-to-sales ratios were 14.5% in 2005, 16.0% in 2000, and just 9.3% in 1995.

Among other top-10 R&D spenders, Qualcomm—the industry's largest fabless IC supplier—remained the second-largest R&D spender, a position it first achieved in 2012. Qualcomm's semiconductor-related R&D spending was down 7% in 2016 compared to an adjusted total in 2015 that included expenditures by U.K.-based CSR and Ikanos Communications in Silicon Valley, which were acquired in 2015. Broadcom Limited—which is the new name of Avago Technologies after it completed its $37 billion acquisition of U.S-based Broadcom Corporation in early 2016—was third in the R&D ranking. Excluding Broadcom's expenditures in 2015, Avago by itself was ranked 13th in R&D spending that year (at nearly $1.1 billion).

Memory IC leader Samsung was ranked fourth in R&D spending in 2016 with expenditures increasing 11% from 2015. Among the $1 billion-plus "R&D club," the South Korean company had the lowest investment-intensity level with 6.5% of its total semiconductor revenues going to chip-related research and development in 2016, which was up from just 6.2% in 2015.

Toshiba in Japan moved up two positions to fifth as it aimed its R&D spending at 3D NAND flash memories. Foundry giant

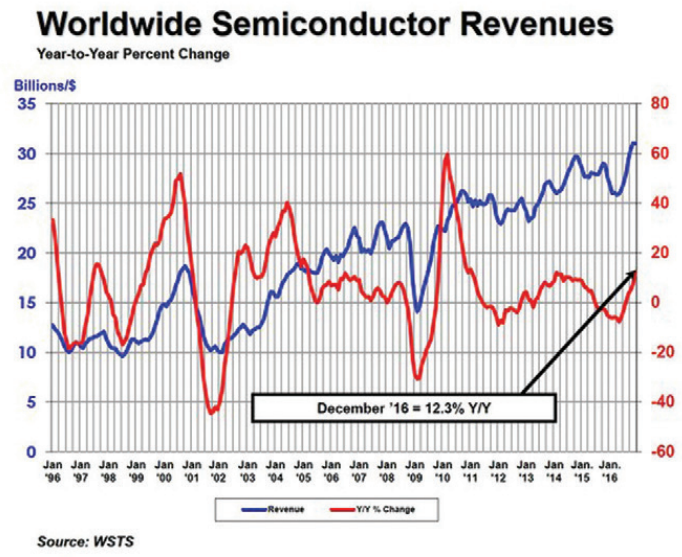
Continued on page 7

Global semiconductor sales reach $339B in 2016

The Semiconductor Industry Association (SIA) announced the global semiconductor industry posted sales totaling $338.9 billion in 2016, the industry's highest-ever annual sales and a modest increase of 1.1 percent compared to the 2015 total. Global sales for the month of December 2016 reached $31.0 billion, equaling the previous month's total and bettering sales from December 2015 by 12.3 percent. Fourth quarter sales of $93.0 billion were 12.3 percent higher than the total from the fourth quarter of 2015 and 5.4 percent more than the third quarter of 2016. All monthly sales numbers are compiled by the World Semiconductor Trade Statistics (WSTS) organization and represent a three-month moving average.

"Following a slow start to the year, the global semiconductor market picked up steam mid-year and never looked back, reaching nearly $340 billion in sales in 2016, the industry's highest-ever annual total," said John Neuffer, president and CEO, Semiconductor Industry Association. "Market growth was driven by macroeconomic factors, industry trends, and the ever-increasing amount of semiconductor technology in devices the world depends on for working, communicating, manufacturing, treating illness, and countless other applications. We expect modest growth to continue in 2017 and beyond."

Several semiconductor product segments stood out in 2016. Logic was the largest semiconductor category by sales with $91.5 billion in 2016, or 27.0 percent of the total semiconductor market. Memory ($76.8 billion) and micro-ICs ($60.6 billion) – a category that includes microprocessors – rounded out the top three segments in terms of total sales. Sensors and actuators



was the fastest growing segment, increasing 22.7 percent in 2016. Other product segments that posted increased sales in 2016 include NAND flash memory, which reached $32.0 billion in sales for a 11.0 percent annual increase, digital signal processors ($2.9 billion/12.5 percent increase), diodes ($2.5 billion/8.7 percent increase), small signal transistors ($1.9 billion/7.3 percent), and analog ($47.8 billion/5.8 percent increase).

Regionally, annual sales increased 9.2 percent in China, leading all regional markets, and in Japan (3.8 percent). All other regional markets – Asia Pacific/All Other (-1.7 percent), Europe (-4.5 percent), and the Americas (-4.7 percent) – saw decreased sales compared to 2015. ◆

GlobalFoundries, Continued from page 4

the center for FDX technology development. GF engineers in Dresden are already developing the company's next-generation 12FDX technology, with customer product tape-outs expected to begin in the middle of 2018.

In China, GF and the Chengdu municipality have formed a partnership to build a fab in Chengdu. The partners plan to establish a 300mm fab to support the growth of the Chinese semiconductor market and to meet accelerating global customer demand for 22FDX. The fab will begin production of mainstream process technologies in 2018 and then focus on manufacturing GF's commercially available 22FDX process technology, with volume production expected to start in 2019.

In Singapore, GF will increase 40nm capacity at its 300mm fab by 35 percent, while also enabling more 180nm production on its 200mm manufacturing lines. The company will also add new capabilities to produce its industry-leading RF-SOI technology.

"GF has had a strong foundry relationship with Qualcomm Technologies for many years across a wide range of process nodes," said Roawen Chen, senior vice president, QCT global operations, Qualcomm Technologies, Inc. "We are excited to see GF making these new investments in differentiated technology and expanding global capacity to support Qualcomm Technologies in delivering the next wave of innovation across a range of integrated circuits that support our business." ◆

Intel announces, Continued from page 4

to march on, fueling technology innovations the world loves and depends on," said Krzanich. "This factory will help the U.S. maintain its position as the global leader in the semiconductor industry."

"Intel is a global manufacturing and technology company, yet we think of ourselves as a leading American innovation enterprise," Krzanich added. "America has a unique combination of talent, a vibrant business environment and access to global markets, which has enabled U.S. companies like Intel to foster economic growth and innovation. Our factories support jobs — high-wage, high-tech manufacturing jobs that are the economic engines of the states where they are located." ◆

Intel continues, Continued from page 5

Taiwan Semiconductor Manufacturing Co. (TSMC) was sixth with a 7% increase in 2016 R&D spending, followed by fabless IC supplier MediaTek in Taiwan, which moved up one position to seventh with 13% growth in R&D expenditures. U.S.-based memory supplier Micron Technology advanced from ninth to eighth in the ranking with its research and development spending rising 5% in 2016.

Rounding out the top 10, NXP in Europe was ninth in 2016, slipping from sixth in 2015 and SK Hynix grew its R&D spending 9% to complete the list. Fabless Nvidia just missed the cut with a 10% increase in expenditures for research and development.

Semiconductor consolidation played a factor in industry R&D spending rising just 1% in 2016 to a record-high $56.5 billion after a 1% increase in 2015 to $56.2 billion. The slowdown in industry-wide R&D spending growth also corresponded with weakness in worldwide semiconductor sales, which declined 1% in 2015 and then recovered with a low single-digit increase in 2016. ◆

Top Semiconductor R&D Spenders
(Companies with ≥$1.0B in Spending)

2016 Rank	Company	R&D Exp ($M)	R&D/Sales %	16/15 % Chg in R&D
1	Intel	12,740	22.4%	5%
2	Qualcomm	5,109	33.1%	-7%
3	Broadcomm Ltd.	3,188	20.5%	-4%
4	Samsung	2,881	6.5%	11%
5	Toshiba	2,777	27.6%	-5%
6	TSMC	2,215	7.5%	7%
7	MediaTek	1,730	20.2%	13%
8	Micron	1,681	11.1%	5%
9	NXP	1,560	16.4%	-6%
10	SK Hynix	1,514	10.2%	9%
	Top 10 Total	**35,395**		
11	Nvidia	1,463	22.0%	10%
12	TI	1,370	11.0%	7%
13	ST	1,336	19.3%	-6%

Source: Company reports, IC Insights' *Strategic Reviews* database

The New DARPA Program "CHIPS"

PHIL GARROU,
Contributing Editor

The research wing of the Defense Department, otherwise known as DARPA, put out a broad agency announcement in Sept 2016 for a program called "Common Heterogeneous Integration and IP Reuse Strategies with the same acronym, CHIPS [BAA-16-62] with an anticipated funding level of ~ $70MM. Multiple award are expected. Final proposal due date was Dec 16th and the estimated start date was reported to be ~ 4 months after proposal submission. The program is being run by Dr. Dan Green in MTO (Microsystems Technology Office).

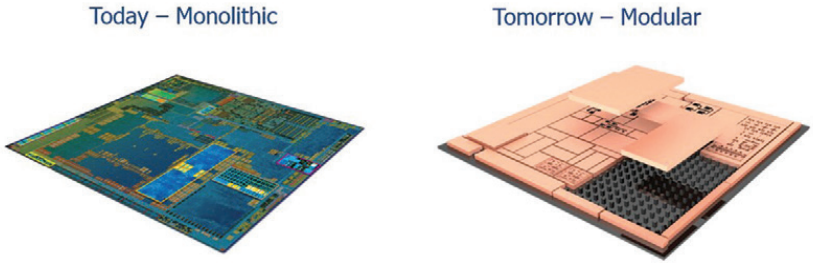


FIGURE 1. DARPA's CHIPS program has the possibility of creating a paradigm shift in how electronics are done today.

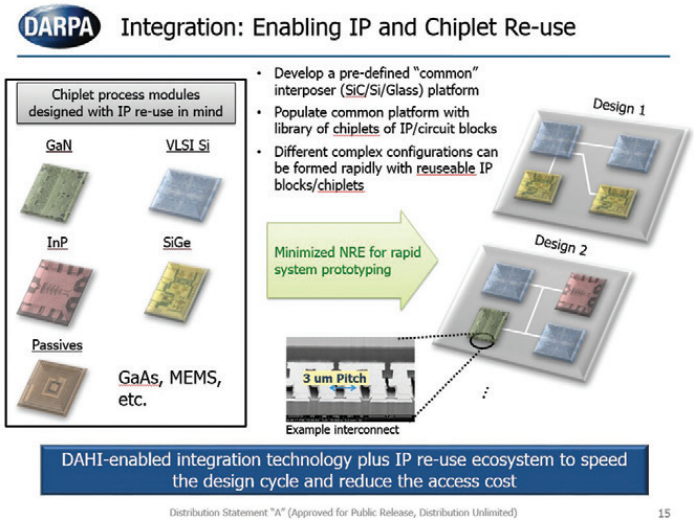


FIGURE 2. A key feature of CHIPS is the establishment of standard interfaces to promote the reusability and interchangeability of modular circuit functional blocks or chiplets.

Pay attention to this program because it has the possibility of creating a paradigm shift in how electronics are done today. The goal is to lower cost and decrease turnaround time for military electronics, but design flows that will be created could have major impact on the industry as a whole. As I've said recently, with the end of Moore's Law, we are searching for high impact alternatives and this just may be it.

As the BAA describes it, DARPA expects participants to "…leverage existing designs that would benefit from translation to a modular framework (**FIGURE 1**) in order to enable reuse of captive IP, include commercial IP, or allow faster redesign and update cycles." A key feature of CHIPS is the establishment of standard interfaces to promote the reusability and interchangeability of modular circuit functional blocks or chiplets (**FIGURE 2**). In the first phase of the program the community will "converge on a limited number of interface standards that are broadly useful"

CHIPS consists of 3 technical areas (TA1) focused on modular digital designs; (TA2) focused on modular analog design and (TA3) focused on supporting technologies.

SoC (system on chip) technology has been driving the industry for several decades as further functions were implemented on chip. We are now looking at a reversal of this process. DARPA called it "dis-aggregation." I prefer to call it "disintegration". Once in place it will allow you to replace only functions that need to be upgraded and not have to redesign and remanufacture the whole SoC chip. Whatever you want to call it, it looks like exciting times are ahead. ◆

Packaging

Picosun and Hitachi MECRALD process

ED KORCZYNSKI,
Sr. Technical Editor

A new microwave electron cyclotron resonance (MECR) atomic layer deposition (ALD) process technology has been co-developed by Hitachi High-Technologies Corporation and Picosun Oy to provide commercial semiconductor IC fabs with the ability to form dielectric films at lower temperatures. Silicon oxide and silicon nitride, aluminum oxide and aluminum nitride films have been deposited in the temperature range of 150-200 degrees C in the new 300-mm single-wafer plasma-enhanced ALD (PEALD) processing chamber.

With the device features within both logic and memory chips having been scaled to atomic dimensions, ALD technology has been increasingly enabling cost-effective high volume manufacturing (HVM) of the most advanced ICs. While the deposition rate will always be an important process parameter for HVM, the quality of the material deposited is far more important in ALD. The MECR plasma source provides a means of tunable energy to alter the reactivity of ALD precursors, thereby allowing for new degrees of freedom in controlling final film properties.

The Figure shows the MECRALD chamber— Hitachi High-Tech's ECR plasma generator is integrated with Picosun's digitally controlled ALD system—from an online video (https://youtu.be/SBmZxph-EE0) describing the process sequence:

1. first precursor gas/vapor flows from a circumferential ring near the wafer chuck,

2. first vacuum purge,

3. second precursor gas/vapor is ionized as it flows down through the ECR zone above the circumferential ring, and

4. second vacuum purge to complete one ALD cycle (which may be repeated).

The development team claims that MECRALD films are superior to other PEALD films in terms of higher density, lower contamination of carbon and oxygen (in non-oxides), and also show excellent step-coverage as would be expected from a surface-driven ALD process. The relatively density of these films has been confirmed by lower wet etch rates. The single-wafer process non-uniformity on 300mm wafers is claimed at ~1% (1 sigma). The team is now exploring processes and precursors to be able to deposit additional films such as titanium nitride (TiN), tantalum nitride (TaN), and hafnium oxide (HfO). In an interview with Solid State Technology, a spokesperson from Hitachi High-Technologies explained that, "We are now at the development stage, and the final specifications mainly depend on future achievements."

The MECR source has been used in Hitachi High-Tech's plasma chamber for IC conductor etch for many years, and is able to generate a stable high-density plasma at very low pressure (< 0.1 Pa). MECR plasmas provide wide process windows through accurate plasma parameter management, such as plasma distribution or plasma position control. The same plasma technology is also used to control ions and radicals in the company's dry cleaning chambers.

FIGURE. Cross-sectional schematic of a new Microwave Electron Cyclotron Resonance (MECR) plasma source from Hitachi High-Technologies connected to a single-wafer Atomic Layer Deposition (ALD) processing chamber from Picosun. (Source: Picosun)

"I'm really impressed by the continuous development of ALD technology, after more than 40 years since the invention," commented Dr. Tuomo Suntola,, and the famous inventor and patentor of the Atomic Layer Deposition method in Finland in 1974, and member of the Picosun board of directors. "Now combining Hitachi and Picosun technologies means (there is) again a major breakthrough in advanced semiconductor manufacturing."

MECRALD chambers can be clustered on a Picosun platform that features a Brooks robot handler. This technology is still under development, so it's too soon to discuss manufacturing parameters such as tool cost and wafer throughput. ◆

Semiconductors

Please, touch the display

SRI PERUVEMBA, *Board Director & Head of Marketing, Society for Information Display*

The possibilities for integrating haptics with displays are nearly limitless.

Haptics are increasingly being paired with VR technology to further enhance the gaming user experience.

A technology trend you may be hearing about more frequently is haptics. The term refers, quite literally, to the science of touch – it is tactile-feedback technology that applies force, motion or vibration to the user to create the sense of touch. In many cases, an actuator is used to convert electrical, hydraulic or pneumatic energy into vibrations that are controlled and managed by special software (**FIGURE 1**). First integrated into motors, haptics can now be encountered nearly anywhere, enhancing the user's sense of realism and attracting attention in unique ways. For example, new car models employ haptics in the seat, steering wheel and other areas in conjunction with such technologies as lane departure and forward collision warning alarms.

Haptics are particularly useful when combined with actual touch technologies. Most of us are familiar with touch displays, given their ubiquity in smartphones, tablets and newer automotive displays. But they do have drawbacks. Touch screens can be difficult to use in wet or sandy environments, as well as those involving extremes of temperature. Now, consider the notion of haptic touch – essentially, a screen that touches you back. Haptic touch screens can provide tactile feedback to your finger as you swipe or scroll over the screen. Ultra-low electrical currents that create sensation on the skin can allow you to feel buttons, textures and other visually flat surface features, resulting in a more immersive experience.

Automotive applications

Haptics are turning up in the design of today's cars for a range of applications, helping improve the driving experience and making it safer. As mentioned earlier, car makers are including vibration alerts that warn drivers of potential impact with another vehicle, and sensors integrated with haptics can provide warnings that help drivers parallel park safely. The union of haptics and displays can ideally help improve the interface between people and vehicles. Some automobile brands employ a system similar to a tablet. Located in the center console, it enables the driver to use fingertip touch to control the vehicle. Other carmakers are incorporating haptic feedback in the dashboard and console to enhance driver control and maintain safety.

Mobile devices and gaming

As makers of mobile devices began to adopt haptic technology, the vibrate function on mobile phones became a standard feature. The basic vibrations first incorporated into mobile phones, which allowed users to get notifications without having to turn on the ringer, have now become fully customizable. Utilizing this haptic "language," users can know generally what's happening without having to stop right away and look at their device, increasing safety and convenience while driving, biking, running and other activities. The Apple Watch allows the wearer to hear and feel communication, utilizing the company's patented "taptic engine" to deliver a physical tap. It also allows the wearer to literally send another person a tap – the recipient will feel a similar sensation when tapping his or her watch, and will know who is looking to get in touch. The next generation of haptic technologies will take it further, allowing a dozen or more uniquely different sensations to be created using new polymer materials driven by customized waveforms.

In the gaming space, early haptics comprised vibrations sent through a handheld controller. As more companies entered

SRI PERUVEMBA is Board Director & Head of Marketing, Society for Information Display.

FIGURE 1. Novasentis (Burlingame, Calif.) is integrating its electro-mechanical polymer (EMP) actuator technology into wearable devices to enable real-time haptic feedback. (Photo courtesy Novasentis)

the space and launched their own systems, every console featured some type of haptics. Over the last 20 years, haptics have moved beyond the controller, to steering wheels and gaming chairs, among other tactile gaming accessories. Today, the gaming market is approaching $100 billion, and the combination of haptics with large, high-resolution screens is making gaming a fully interactive experience. Even familiar video games like Pong or those using dice or cards take on a new dimension of reality when haptics are integrated. The newest trends include integration of as many as 10 haptic actuators into the handheld gaming controller. Each of these actuators can provide unique feedback, in both intensity and pattern, driven by software/waveforms.

AR/VR

The fastest-growing application for haptic displays is virtual reality and augmented reality (VR/AR). Companies such as Intel, Microsoft and Facebook and large startups such as Magic Leap are investing a great deal in this space, while smaller entrants are expanding the landscape, creating many new opportunities. Virtual reality now looks and sounds so lifelike that you feel as though you're physically in the virtual space, so you want to touch things and to feel things touching you. But without haptics, this isn't possible. Early versions of AR/VR devices offered visual and auditory experiences with rudimentary haptic feedback. The next generation of devices will allow even more varied virtual experiences – e.g., realtors can 'walk' buyers through a new home, while travel promoters can allow clients to 'experience' new vacation destinations. In addition, AR/VR with high-resolution displays and haptics will bring tremendous gains to the medical and entertainment industries. All of these advances will be possible with haptic technologies that let you distinguish textures, feel rain on your palm, and be able to differentiate between hard pebbles and soft sand.

Haptics in medicine

Today, if you undergo medical or dental surgery, there's a good chance the surgeon used technology involving haptics to practice and hone his or her skills. Integrating medical devices with haptics provides a new level of intuitive performance for medical practitioners. While technology developments have yielded new medical devices that let doctors perform procedures with minimal disturbance to the patient, the all-important personal connection between them has lessened. What haptic technology enables is a return to the importance of touch in strengthening this personal connection between doctors and patients. The result is a multi-disciplinary approach to developing medical devices.

Laparoscopic surgery has already become a boon to surgeons, enabling them to obtain clear internal information on a patient with minimal invasion, recovery time and scarring. Integrating laparoscopes with haptics takes this invaluable technique one giant step further, giving doctors the ability to obtain a similar sensation to what they could receive using their hands and other tools while still minimizing patient discomfort. Dental training simulators also become more effective and realistic when integrated with haptics, and using haptic technology in student practice can help eliminate professional errors.

Looking ahead

The possibilities for integrating haptics with displays are nearly limitless. Imagine being able to "travel" to remote areas and experience what it's like to visit the rainforest, Antarctica, or virtually any other place on earth. Not only tourism, but the real estate market could benefit from this type of application – people who need to relocate or invest in property far away from their current location could use haptics to allow the full virtual open house experience. Think of the convenience and savings in travel time. In the retail space, before you visited a big department store, such as Harrods of London, you could go through the store with a VR set outfitted with haptics for a fully tactile pre-shopping experience. And then there's entertainment. Hollywood is finding new ways to allow you be part of a movie – e.g., 3D films shown in a theater equipped with motion simulator seats – while Disney Research has a major project in the works called Surround Haptics.

If you'd like to know what the industry's brightest minds are dreaming up in the haptics space, plan to visit Display Week 2017, being held May 21-26 in Los Angeles. Display Week is the premier event for previewing display technologies that will be on the market in the next two to five years. This year, AR and VR will be well represented, along with many haptics-related demos. Come join us for a sneak preview, and feel. ◆

Architecture innovation in the DRAM industry: How it affects firms' sustainable competence

HEISEUNG KIM *and* **HEESANG LEE**, *Management of Technology Department at Sungkyunkwan University, Suwon, South Korea*

The technology leader in the DRAM industry has a greater advantage in terms of market share and profit.

This paper presents an empirical study that links between firms' technological leadership and the firms' sustainability. While extant studies focused on the effect of incremental or radical innovation on the firm, a few researches have been carried out on the other types of innovation. In this study, architecture innovation in the DRAM industry is used to analyze how the continuous architecture innovation of scaling affects firms' performance. We compared the historical technology roadmap of each firm with their market share and profit data and concluded that continuous architecture innovation would positively affects the performance of a firm as well as its chance of survival. This study suggests that continuous architecture innovations are required in order to stay competitive in DRAM industry.

Introduction

Invented by Robert Dennard at IBM in 1966, Dynamic Random Access Memory (DRAM) is one of the major types of semiconductor products. Since then, the DRAM market has grown significantly, accounting for $45.1 billion in sales in 2015 [1]. The DRAM industry has three main and crucial industry characteristics: product life cycle is short, it is technology driven, and it requires a huge investment [2]. The average DRAM product life cycle is about two to three years and the capacity ranges increased from 4K DRAM in 1974 to 2G DRAM in 2010. The implication of the short product life cycle is that the DRAM manufacturer with technology leadership will be able to recover their initial investment and gain more profit; therefore, the DRAM industry is highly driven by technology [3]. The technology leader can earn premium profit at the initial stage of a new product and benefit from additional profit by sustainability in the grown market. However, technology followers can suffer from price reduction when they launch a new product due to the mature state of a product life cycle, and it might thus be difficult to recover their initial investment [4]. The production of DRAM requires numerous steps with very expensive equipment; the cost of a new semiconductor fab is billions of dollars; a proper analysis and suitable strategy is therefore needed in order to compete with other comparative companies in the industry. In 1991, there were more than dozen DRAM production firms. However, by 2012, only four major companies survived: Samsung, SK Hynix, Elpida, and Micron [1].

The well-known scaling law of semiconductors, known as Moore's Law, was used to review the technology development process in the semiconductor industry [5]. Recently, many researchers, including Mack and Kim, have argued that, even though Moore's Law provided considerable insight into the semiconductor industry, it is no longer valid; they added that the physical and technical limitation will slow down the innovation and breakthrough technologies are necessary in the semiconductor industry [3-4,6]. Therefore, many companies and researchers are focusing on developing new memory devices, such as Magnetic RAM (MRAM) and Phase-change RAM (PRAM), to replace current DRAM memory. However, it is not clear how and when are the right time to replace the current DRAM memory with new memory devices and how it might affects the firms' business performance [5,7-8]. In this paper, we will discuss how continuous architecture innovation affects the performance of DRAM companies in terms of market share and profit.

Innovation types

In the long run, technological innovation capabilities are the major source of competitive advantage and many companies are pursuing extensive research activities in order to stay competitive in the market [9]. The ability

to develop and introduce new products or processes in shorter time periods is inevitable and has become the major competence for firms [10].

Henderson and his colleagues defined the types of innovation as four categories: incremental, architecture, modular, and radical innovation [11], defined as follows:

- Incremental innovation: innovation with no change in architecture and concept.
- Architecture innovation: innovation with new architecture but without change in concept.
- Modular innovation: fundamental change of technological concept without change in architecture.
- Radical innovation: new architecture and new concept.

By using Henderson's definition, the types of innovation in the DRAM industry can be defined as shown in **TABLE 1**. In this paper, we will focus on the architecture innovation which is the major innovation in DRAM industry [3,5].

Types	Activities
Incremental Innovation	- Cost down, - Change material - Changing design and layout
Architecture Innovation	- Scaling (shrinkage of DRAM device to the next node) - Changing the structure of capacitor, transistor etc. - Change from planar to vertical structure
Modular Innovation	- Development of MRAM, PRAM
Radical Innovation	- Development of non-MOS(Metal Oxide Semiconductor) based memory

TABLE 1. Innovation activities in DRAM industry

Market leadership and profit relationship

Many firms attempt to improve their performance through innovation and according to recent study by Bowen and his colleagues the relationship between innovation and the future performance of the firm is positive [12]. For many firms, including DRAM

Samsung	2006	2007	2008	2009	2010	2011	2012
Technology Ranking							
Market Share Ranking							
Profit Ranking							

TABLE 2. Samsung data (Blue = 1st ranking, Red = 2nd ranking)

manufactures, maintaining a leadership position in the industry is a major goal because the duration of the stay at the top of the market reflects the length of time they might be able to enjoy the benefits as a market leader [13]. Therefore, a study is needed on the relationship between the market leader and the followers in terms of profits. In the case of the DRAM industry, the forces of competition are high and there are no room for slow followers to stay profitable; winner takes it all.

Continuous development

Van Valen introduced a theory known as the Red Queen Effect which states that competition will eliminate less fit organizations and stimulate organizational learning [14]. Therefore, continuous innovation is needed in order to maintain fitness relative to the system [15]. This theory explains the continuation of the never ending arms race which is due to the initial innovation of a firm which not only increases its competitiveness, but also decreases the competitiveness of its rivals. The rivals are threatened by an increased competitive pressure, and will respond to a competitor's innovation with their own innovation, which then increases the competitive pressures in the market, creating a continual cycle of competitiveness [16]. The same theory is valid when assessing competitiveness in the DRAM industry. In 2007, the production by firms in the DRAM industry greatly increased, initiating a price war between the companies, known as the Chicken Game. After 2007, the price of DRAM dropped and DRAM manufacturers underwent a severe decrease in profits [1]. Those who prepared for this race were able to endure the race. However, those who were not prepared and decided to cut production could not withstand the massive supply of DRAM; such companies included Elpida, which lost its position as a leader in the more advanced technology. Their economies of scale reduced and due to the severe deficit, they lost their business and merged with Micron in 2013.

Methodology and data

For the DRAM industry, the market share of the top four companies is about 95% of the total industry's market share therefore the force of competitions and innovation-performance relationship are well represented by these four companies. The market share and OPM data of the top four companies, Samsung, SK Hynix, Elpida, and Micron, were used in this study and the market share data was refined to represent only these four companies [1]. The data from third quarter of 2006 to 2012 is used because chicken game started at 2007 and Elpida was merged to Micron at 2013. For the companies' historical product roadmap, development histories of different nodes were obtained from each company's press releases. For the statistical data of the market share and the operating profit margin (OPM) was obtained from market research firm, IHS isuppli.

Results and discussions

FIGURE 1 shows the trend of the market share change in terms of companies' historical roadmaps in the DRAM industry. The same numbers of color, 6x, 5x, 4x, 3x 2x nm, indicates the same device generations of architecture innovation and showing the technology gap among firms. For example, Samsung's 68nm node is competing with SK Hynix's 66nm and SK Hynix is one quarter behind than Samsung. As expected, the market share of the technology leader, Samsung, is the highest. Samsung has the highest market share of

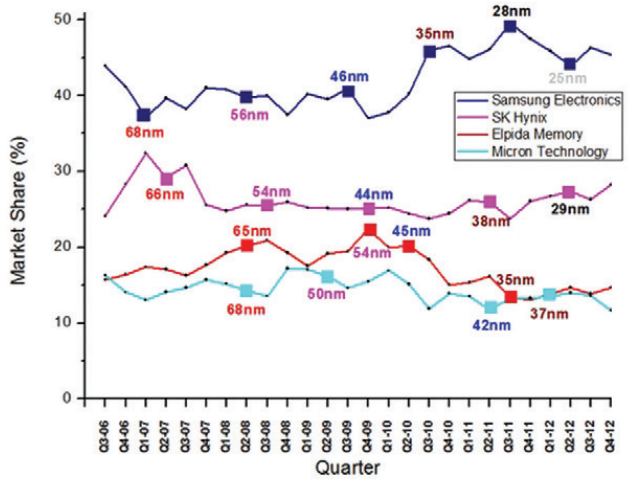


FIGURE 1. Market share vs. companies' historical roadmaps in DRAM industry.

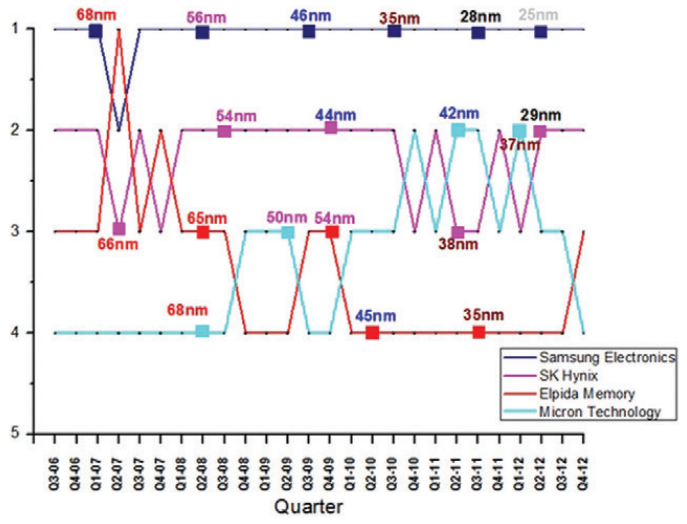


FIGURE 2. Profit Ranking (OPM) vs. companies' historical roadmaps in DRAM industry.

slightly above 40% and SK Hynix has about 25%. Elpida and Micron both have a market share of about 15%. Also, the market share of the technology leader increased as Samsung managed to develop next node product faster than competitors. Technology ranking exactly matches the market share ranking and Samsung was able to maintain their technology and market leadership.

FIGURE 2 shows the profit ranking among the DRAM manufactures in terms of device generations. Profit might be more important factor than market share for the firms' sustainability since it is directly connected to the firms' survival as seen during the chicken game. Samsung, the market and technology leader, shows the highest Operating Profit Margin (OPM). The profit ranking changed once for Samsung in the second quarter of 2007, during the chicken game. After the second quarter of 2007, Samsung retained the title of the most profitable firm in the DRAM industry. However, there were many fluctuations for the firms that ranked second and less. During 2007 to 2012, Samsung had a negative profit quarter five times [1]. This is very low compared to the 12 times shown by the second leader, SK Hynix, 16 times by Elpida, and 17 times by Micron.

A previous study by Weber and Yang suggested that in semiconductor industry while leading edge manufacturers make large profits, but their ROI (Return On Investment) might be lower than the slow followers [17]. This might be true for logic semiconductor devices, since the logic firms produce much specified products and, most of the time, the competitiveness of such firms does not derive from the most advanced scaling node or continuous architectural innovation; rather it derives from optimization, design, and customer value. However, for the DRAM industry, the effect of logic's competitiveness is limited since the price of DRAM, as a commodity, is determined by the market and the main competitiveness is how many bits that firms can produce in a restricted area of 300nm wafers. Therefore, slow follower probably not able to compete in the market in terms of price.

TABLE 2 shows the ranking data of Samsung from third quarter of 2006 to 2012. Samsung, the market and technology leader was able to manage to stand at the top in terms of technology and market share. In terms of profit, Samsung ranked 2nd only for one quarter in 2007 and managed to return 1st rank due to technological advantage. This result suggests that Samsung was able to maintain its position even during the chicken game and was able to stay fit in the market and make profit compared to the other companies. In the case of the DRAM industry, continuous architecture innovation means that the number of chips per wafer would increase as innovation succeeded. The delayed

development of the next generation device would lead to SK Hynix, Elpida, and Micron producing fewer DRAM chips per wafer than Samsung, which led to the increase of the DRAM manufacturing cost. Staying competitive in the market by continuous architecture innovation is most important for DRAM manufacturers' as it enables more profit to be made than the competitors; Elpida could not stand the large amount of deficit and merged to Micron.

Conclusions

In this study, the benefits of being the technology leader of architecture innovation in the DRAM industry are clearly shown, where the technology leader has a greater advantage in terms of market share and profit than the competitors. Also, the technology leader has more resilience when the industry is undergoing a difficult time, and would be able to perform better than other firms. The firms that do not continue to innovate will not survive. In 2002, 11 DRAM manufacturers were competing intensely in the market; however currently, only 3 major DRAM manufacturers had survived. Many large firms such as Qimonda and Elpida failed to survive. The critical factor which determines the ability to dominate in the DRAM industry is continuous architecture innovation. For example, EUV lithography is necessary for continuous architectural innovation since the next scaling node will require smaller patterning with multi-patterning of ArF, which needs many additional steps and processes than EUV process. However, the application of a 450mm sized wafer is not considered as an architectural innovation since the 450nm wafer does not improve the structure of the device. Therefore, it is considered an incremental innovation for the DRAM industry; the 450nm sized wafer is not urgent and not yet required. This study provides understanding for firms to suggest which technology that they need to focus on in order to stay competitive in the market in the future.

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SiPs simplify wireless IoT design

By **DAVID LAMMERS**, *Contributing Editor*

System-in-package solutions, running a proven software stack, are easing wireless design for Internet of Things end node applications

It takes a range of skills to create a successful business in the Internet of Things space, where chips sell for a few dollars and competition is intense. Circuit design and software support for multiple wireless standards must combine with manufacturing capabilities.

Daniel Cooley, senior vice president and general manager of IoT products at Silicon Labs (Austin, Tx.), said three trends are impacting the manufacture of IoT end-node devices, which usually combine an MCU, an RF transceiver, and embedded flash memory. "There is an explosion in the amount of memory on embedded SoCs, both RAM and non-volatile memory," said Cooley. Today's multi-protocol wireless software stacks, graphics processing, and security requirements routinely double or quadruple the memory sizes of the past.

Secondly, while IoT edge devices continue to use trailing-edge technologies, nonetheless they also are moving to more advanced nodes. However, that movement is partially gated by the availability of embedded flash.

Thirdly, pre-certified system-in-package (SiP) solutions, running a proven software stack, "are becoming much more important," Cooley said. These SiPs typically encapsulate an MCU, an integrated antenna and shielding, power management, crystal oscillators, and inductors and capacitors. While Silicon Labs has been shipping multi-chip modules for many years, SiPs are gaining favor in part because they can be quickly deployed by engineers with relatively little expertise in wireless development, he said.

"Personally, I believe that very advanced SIPs increasingly will be standard products, not anything exotic. They are a complete solution, like a PCB module, but encased with a molding compound. The SiP manufacturers are becoming very sophisticated, and we are ready to take that technology and apply it more broadly," he said.

For example, Silicon Labs recently introduced a Bluetooth SiP module measuring 6.5 by 6.5 mm, designed for use in sports and fitness wearables, smartwatches, personal medical devices, wireless sensor nodes, and other space-constrained connected devices (**FIGURE 1**).

"We have built multi-chip packages – those go back to the first products of the company – but we haven't done a fully certified module with a built-in antenna until now. A SiP module simplifies the go-to-market process. Customers can just put it down on a PCB and connect power and ground. Of course, they can attach other chips with the built-in interfaces, but they don't need anything else to make the Bluetooth system work," Cooley said.

Designing with a certified SiP module supports better data throughput, and improves reliability as well. The SiP approach is especially beneficial for end-node customers which "haven't gone through the process of launching a wireless product in in the market," Cooley said.

FIGURE 1. System-in-package (SiP) solutions ease the design cycle for engineers using Bluetooth and low low-energy wireless networks. (Source: Silicon Laboratories).

Control by voice

The BGM12x Blue Gecko SiP (**FIGURE 2**) is aimed at Bluetooth-enabled applications, a genre that is rapidly expanding as ecosystems like the Amazon Echo, Apple HomeKit, and Google Home proliferate.

Matt Maupin is Silicon Labs' product marketing manager for mesh networking products, which includes SoCs and modules for low-power Zigbee and Thread wireless connectivity. Asked how a home lighting system, for example, might be connected to one of the home "ecosystems" now being sold by Amazon, Apple, Google, Nest, and others, Maupin said the major lighting suppliers, such as OSRAM, Philips, and others, often use Zigbee for lighting, rather than Bluetooth, because of Zigbee's mesh networking capability. (Some manufactures use Bluetooth low energy (BLE) for point-to-point control from a phone.) "The ability for a device to connect directly relies on the same protocols being used. Google and Amazon products do not support Zigbee or Thread connectivity at this time," Maupin explained.

Normally, these lighting devices are connected to a hub. For example, Amazon's Echo and Google's Home "both control the Philips lights through the Philips hub. Communication happens over the Ethernet network (wireless or wired depending on the hub). The Philips hub also supports HomeKit so that will work as well," he said.

Maupin's home configuration is set up so the Philips lights connect via Zigbee to the Philips hub, which connects to an Ethernet network. An Amazon Echo is connected to the Ethernet Network by WiFi.

"I have the Philips devices at home configured via their app. For example, I have lights in my bedroom configured differently for me and my wife. With voice commands, I can control these lamps with different commands such as 'Alexa, turn off Matt's lamp,' or 'Alexa, turn off the bedroom lamps.'"

Alexa communicates wirelessly to the Ethernet Network, which then goes to the Philips hub (which is sold under the brand name Philips Hue Bridge) via Ethernet, where the Philips hub then converts that to Zigbee to control that actual lamps. While that sounds complicated, Maupin said, "to consumers, it is just magic."

A divided IoT market

IoT systems can be divided into the high-performance number crunchers which deal with massive amounts of data, and the "end-node" products which drive a much different set of requirements. Sandeep Kumar, senior vice president of worldwide operations at Silicon Labs, said RF, ultra-low-power processes and embedded NVM are essential for many end-node applications, and it can take several years for foundries to develop them beyond the base technology becoming available.

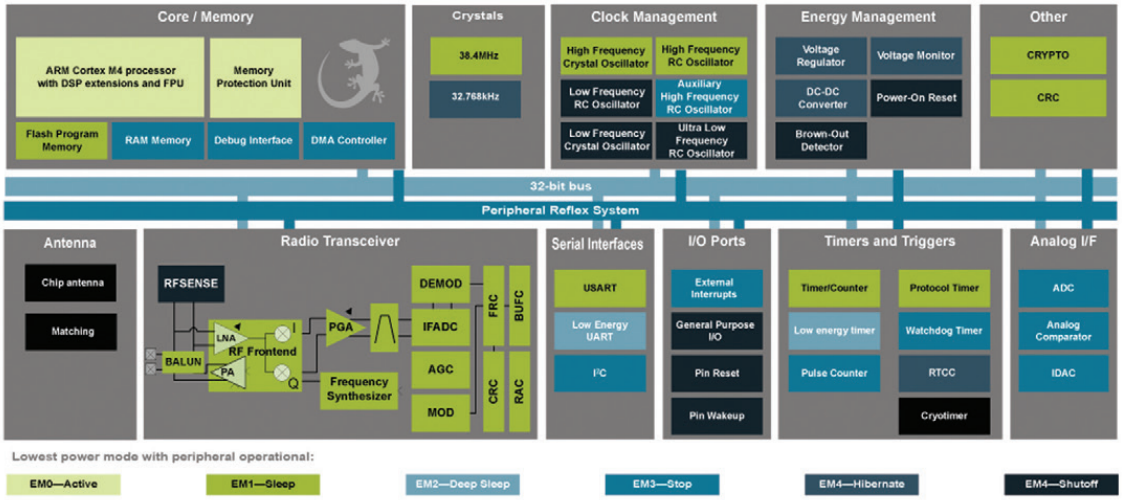

FIGURE 2. The BGM12x Blue Gecko SiP is aimed at Bluetooth-enabled applications.

"40nm is an old technology node for the big digital companies. For IoT end nodes where we need a cost-effective RF process with ultra-low leakage and embedded

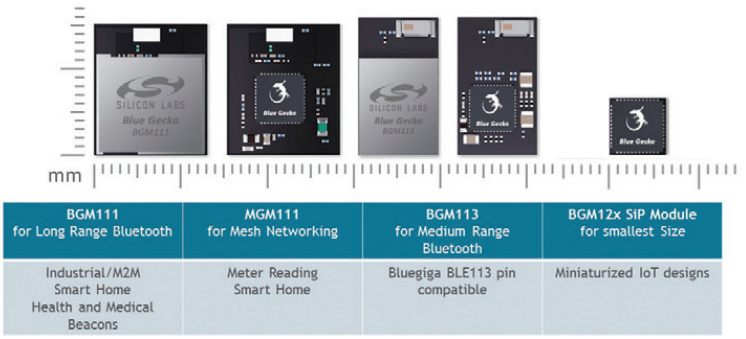

FIGURE 3. The SiP packages a wireless SoC with an antenna and multiple other components in a small footprint.

NVM, the state of the art is 55nm; 40 nm is just getting ready," Kumar said.

Embedded flash or any NVM takes as long as it does because, most often, it is developed not by the foundries themselves but by independent companies, such as Silicon Storage Technology. The foundry will implement this IP after the foundry has developed the base process. (SST has been part of Microchip Technology since 2010.) Typically, the eFlash capability lags by a few years for high-volume uses, and Kumar notes that "the 40nm eFlash is still not in high-volume production for end-node devices."

Similarly, the ultra-low-leakage versions of a technology node take time and equipment investments, as well as cooperation from IP partners. Foundry customers and the fabless design houses must requalify for the low-leakage processes. "All the models change and simulations have to be redone," Kumar said.

"We need low-leakage for the end applications that run on a button cell (battery), so that a security door or motion sensor, for example, can run for five to seven years. After the base technology is developed, it typically takes at least three years. If 40nm was available several years ago, the ultra-low-leakage process is just becoming available now. "And some foundries may decide not to do ultra-low-leakage on certain technology nodes. It is a big capital and R&D investment to do ultra-low-leakage. Foundries have to make choices, and we have to manage that," Kumar said.

The majority of Silicon Labs' IoT product volume is in 180nm, while other non-IoT products use a 55nm process. The line of Blue Gecko wireless SoCs (**FIGURE 3**) currently is on 90nm, made in 300mm fabs, while new designs are headed toward more advanced process nodes.

Because 180nm fabs are being used for MEMS, sensors and other analog-intensive, high-volume products, there is still "somewhat of a shortage" of 180nm wafers, Kumar said, though the situation is improving. "It has gotten better because TSMC and other foundries have added capacity, having heard from several customers that the 180nm node is where they are going to stay, or at least stay longer than they expected. While the foundries have added equipment and capital, it is still quite tight. I am sure the big MEMS and sensor companies are perfectly happy with 180nm," Kumar said.

A testing advantage

IoT is a broad-based market with thousands of customers and a lot of small volume customizations. Over the past decade Silicon Labs has deployed a proprietary ultra-low-cost tester, developed in-house and used in internal back-end operations in Austin and Singapore at assembly and test subcontractors and at a few outside module makers as well. The Silicon Labs tester is much more cost effective than commercially available testers, an important cost advantage in a market where a wireless MCU can sell in small volumes to a large number of customers for just a few dollars. "Testing adds costs, and it is a critical part of our strategy. We use our internally developed tester for our broad-based products, and it is effective at managing costs," Kumar said.

Vital control in fab materials supply chains

ED KORCZYNSKI, *Sr. Technical Editor*

Expert panel discussion at critical materials council (CMC) conference

The inaugural Critical Materials Council (CMC) Conference was held May 5-6 in Hillsboro, Oregon. Held just after the yearly private CMC meeting, the public CMC Conference provides a forum for the pre-competitive exchange of information to control the supply-chain of critical materials needed to run high-volume manufacturing (HVM) in IC fabs. The next CMC Conference will happen May 11-12 in Dallas, Texas.

2016 CMC Conference expert panelists (from left to right) John Smyth, Jonas Sundqvist, Jeff Hemphill, and Jean-Marc Girard.

At the end of the 2016 conference, a panel discussion moderated by Ed Korczynski was recorded and transcribed. The following is an edited excerpt of the conversation between the following industry experts:

- Jean-Marc Girard, CTO and Director of R&D, Air Liquide Advanced Materials,
- Jeff Hemphill, Staff Materials R&D Engineer, Intel Corporation
- Jonas Sundqvist, Sr. Scientist, Fraunhofer IKTS; and co-chair of ALD Conference, and
- John Smythe, Distinguished Member of Technical Staff, Micron Technology.

KORCZYNSKI: Let's start with specifications: over-specifying, and under-specifying. Do we have the right methodologies to be able to estimate the approximate 'ball-park' range that the impurities need to be in?

Jean-Marc Girard, Distinguished Member of Technical Staff of Micron Technology, provided the supplier perspective.

GIRARD: For determining the specifications, to some extent it doesn't matter because we are out of the world of specs, where what matters is the control-limits. To Tim Hendry's point in the Keynote yesterday *[EDITOR'S NOTE: Tim G. Hendry, vice president of the Technology and Manufacturing Group and director of Fab Materials at Intel Corporation provided a conference keynote address on "Process Control Methods for Advanced Materials"]*, what was really interesting is instead of the common belief that we should start by supplying the product with the lowest possible variability, instead we should try to explore the window in which the product is working. So getting 10 containers from the same batch and introducing deliberate variability so that you know the process space in which you can play. That is the most important information to be able to reach the most reasonable and data-driven numbers to specify control limits. A lot of specs in the past were primarily determined by marketing decisions instead of data.

ED KORCZYNSKI is co-chair of the CMC Conference, and Marketing Director of TECHCET CA the advisory services firm that administers the Critical Materials Council (CMC).]

Jonas Sundqvist, Sr. Scientist of Fraunhofer IKTS, discusses collaboration with industry on application-specific ALD R&D.

SUNDQVIST: Like the first introduction of what were called "super-clean" ALD precursors for the original MIS DRAM capacitors, Samsung used about 10nm of hafnium-aluminate and it would not matter if there was slight contamination in the precursors because you were not trying to control for a specific high-k phase. Whereas now you are doping very precisely and you have already scaled thinness so over time the specification for high-k precursors has become more important.

John Smythe, Distinguished Member of Technical Staff of Micron Technology, explains approaches to controlling materials all the way to point-of-use.

SMYTHE: I think it comes down to the premise that when you are doing vapor transport through a bubbler that some would argue that that's like a distillation column. So it's a matter of thinking about what is transporting and what isn't. In some cases the contaminant you're concerned about is in the ampule but it never makes it to the process chamber, or the act of oxidizing destroys it as a volatile byproduct. So I think the bigger issue is change-management not necessarily the exact specification. You must know what you have, and agree that a single adjustment to improve the productivity of chemical synthesis requires that 'fingerprinting' must be done to show the same results. The argument is that you do not accept "less-than" as part of a specification, you only accept what it is.

AUDIENCE QUESTION: The systems in which these precursors are used also have 'memory' based on the prior reactions in the chamber and byproducts that get absorbed on walls. When these byproducts come out in subsequent processing they can alter conditions so that you're actually running in CVD-mode instead of ALD-mode. Chamber effects can wash-out a lot of value of having really pure chemicals moving through a delivery system into a chamber and picking up contaminants that you spent a whole lot of money taking out at the point of delivery. What do you think about that?

GIRARD: Well, this is a 'crisis!' When something like this starts to happen in a fab or even during the development cycles, you can't prioritize resources and approaches you just have to do everything. Sometimes it's the tool, sometimes it's the chemical, sometimes it's the interaction of the two, sometimes it's back-streaming from the vacuum sub-system…there are so many ways that things can go wrong. Certainly you have to clear up the chemistry part as early as possible.

SUNDQVIST: We work with zirconium precursors for ALD, and you can develop a precursor that gives you a very pure ALD process that really works like an ALD process should. However, you can still use the TEMA-Zr precursor, that in processing has a CVD component which you can use that to gain throughput. So you can have a really good ALD precursor that gives low particle-counts and good process stability and ideal thermal processing range, but the growth rate goes down by 20% so you're not very popular in the fab. Many things change when you make an 'improved' molecule to perfect the process, and sometime you want to use an imperfect part of the process.

SMYTHE: What we're doing a lot more these days is doing chamber finger-printing, where we're putting a quad-filtered mass-spec on each chamber—not a cheap little RGA, but real analytical-grade—and it's been enlightening. If you look at your chemistry moving through a delivery line using something like the Schrødenger software, it's not a big deal to see that you can use the mass spec to see some synthesis happening in the line. We joke and call it 'point of use synthesis' but it's not very funny. We are used to having spare delivery lines built-in so we can install tools to try to gain insights to prevent what we've been talking about.

KORCZYNSKI: John, since Micron has fabs in Lehi and fabs in Singapore and other places, while they do run different product loads, do you have to worry about how long it takes things to travel on a slow boat to Singapore? Do you have to stockpile things more strategically these days, and does that effect your receiving department?

SMYTHE: What we really need are a few good ocean-going hydrofoil ships! The most complete answer is we first identify which things need 'batch-qual' so if we do a batch-qual in Virginia and know that material is going to Taiwan that we have confidence it will pass batch-qual in Taiwan. There are certain materials that we require information on which synthesis batch, which production batch, and sometimes which bottling batch. Sometimes you take a yield hit because you didn't have the right vision, and then you institute batch qual.

I think most of you are familiar with the concept of 'ship-to-stock,' when you have enough good statistical history and a good change management process with the supplier then you can do ship-to-stock and that reduces the batch-qual overhead. On a case by case basis you have to figure out how difficult that is. A small story I can tell is that with Block Co-Polymer (BCP) self-assembly we found one particular element that in concentration above 5 ppm prevented the poly-styrene from self-assembling in the same way, whereas other metal trace contaminants could be a hundred times higher and have no effect on the process. So this gets back to some of our earlier discussion that it's not enough to know that your trace elements are below some level. Tell me the exact atoms and the exact counts and then we'll talk about using them. The BCP R&D taught us that in some situations just changing from one batch to the next could increase defects a thousands times. So we will see a bigger push to counting atoms.

KORCZYNSKI: We heard from David Thompson *[EDITOR'S NOTE: Director of Process Chemistry, Applied Materials presented on "Agony in New Material Introductions - Minimizing and Correlating Variabilities"]* today on what we must control, and he gave an example of a so-called trace-contaminant that was essential for the process performance of a precursor, where the trace compound helped prevent particles from flaking off chamber walls. Do we need to specify our contaminants?

GIRARD: Yes. To David's point this morning, every molecule is different. Some are very tolerant due to the molecular process associated with it, and some are not. I'll give you an example of a cobalt material that's been talked about, where it can be run in production at perhaps 95% in terms of assay, provided that one specific contaminant is less than a couple of parts-per-million. So it's a combination of both, it's not assay OR a specification of impurities. It's a matter of specifying the trace components that really matter when you reach the point that the data you gather gives you that understanding, and obviously an assay within control limits.

HEMPHILL: Talking about whether we're over-specifying or not, the emphasis is not about putting the right number on known parameters like assay that are obvious to measure, the emphasis is on identifying and understanding what makes up the rest of it and in a sense trying over-specify that. You identify through mass-spectrometry and other techniques that some fraction of a percent is primarily say five different species, it's finding out how to individually monitor and track and control those as separate parameters. So from a specification point of view what we want is not necessarily the lowest possible numbers, but it's expanding how many things we're looking at so that we're capturing everything that's there.

KORCZYNSKI: Is that something that you're starting to push out to your suppliers?

HEMPHILL: Yes. It depends on the application we're talking about, but we go into it with the assumption that just assay will not be enough. Whether a single molecule or a blend of things is supposed to be there, we know that just having those be controlled by specification will not be sufficient. We go under the assumption that we are going to identify what makes up the remaining part of the profile, and those components are going to need to be controlled as well.

KORCZYNSKI: Is that something that has changed by node? Back when things were simpler say at 45nm and larger, were these aspects of processing that we could safely ignore as 'noise' but are now important 'signals'?

HEMPHILL: Yes, we certainly didn't pay as close attention just a couple of generations ago.

KORCZYNSKI: That seems to lead us to questions about single-sources versus dual-sourcing. There are many good reasons to do both, but not simultaneously. However, it seems that because of all of the challenges we're heard about over the last day-and-a-half of this conference it creates greater burden on the suppliers, and for critical materials the fabs are moving toward more single-sourcing over time.

SMYTHE: I think that it comes down to more of a concern over geographic risk. I'll buy from one entity if that entity has more than one geographic location for the supply, so that I'm not exposed to a single 'Act of God' or a 'random statistical occurrence of global warming.' So for example I need to ask if a supplier has a place in the US and a place in France that makes the same thing, so that if something bad happens in one location it can still be sourced? Or do you have an alternate-supply agreement that if you can't supply it you have an agreement with Company-X to supply it so that you still have control? You can't come to a Micron and say we want to make sure that we get at minimum 25% no matter what, because what typically happens with second-sourcing is Company-A gets 75% of the business while Company-B gets 25%. There are a lot of reasons that that doesn't work so well, so people may have an impression that there's a movement toward single-source but it's 'single flexible-source.'

HEMPHILL: There are a lot of benefits of dual- or multiple-sourcing. The commercial benefits of competition can be positive and we're for it when it works. The risk is that as things are progressing and we're getting more sensitive to differences in materials it's getting harder to maintain that. We have seen situations where historically we were successful with dual-sourcing a raw material coming from two different suppliers or even a single supplier using two different manufacturing lines and everything was fine and qualified and we could alternate sources invisibly. However, as our sensitivity has grown over time we can start to detect differences.

So the concept of being 'copy-exactly' that we use in our factories, we really need production lines to do that, and if we're talking about two different companies producing the same material then we're not going to get them to be copy-exactly. When that results in enough of a variation in the material that we can detect it in the factory then we cannot rely upon two sources. Our preference would be one company that maintains multiple production sites that are designed to be exactly the same, then we have a high degree of confidence that they will be able to produce the same material.

GIRARD: I can give you a supplier perspective on that. We are seeing very different policies from different customers, to the point that we're seeing an increase in the number of customers doing single-sourcing with us, provided we can show the ability to maintain business continuity in case of a problem. I think that the industry became mature after the tragic earthquake and tsunami in Japan in 2011 with greater understanding of what business continuity means. We have the same discussions with our own suppliers, who may say that they have a dedicated reactor for a certain product with another backup reactor with a certain capacity on the same site, and we ask what happens if the plant goes on strike or there's a fire there?

A situation where you might think the supply was stable involved silane in the United States. There are two large silane plants in the United States that are very far apart from each other and many Asian manufacturers dependent upon them. When the U.S. harbors went on strike for a long time there was no way that material could ship out of the U.S. customers. So, yes there were two plants but in such an event you wouldn't have global supply. So there is no one way to manage our supply lines and we need to have conversations with our customers to discuss the risks. How much time would it take to rebuild a supply-chain source with someone else? If you can get that sort of constructive discussion going then customers are usually open to single-sourcing. One regional aspect is that Asian customers tend to favor dual-sourcing more, but that can lead to IP problems.

Solid State TECHNOLOGY

EXECUTIVE OFFICES

Extension Media 1786 18th Street, San Francisco, CA 94107-2343.

ADVERTISING

Director of Sales
Kerry Hoffman
1786 18th St.
San Francisco, CA 94107-2343
Tel: 978.580.4205
khoffman@extensionmedia.com

North America
Kerry Hoffman
Tel: 978.580.4205
khoffman@extensionmedia.com

Germany, Austria, E. Switzerland & E. Europe
Holger Gerisch
Tel: +49.0.8856.8020228
holgerg@pennwell.com

Rest of World
Kerry Hoffman
Tel: 978.580.4205
khoffman@extensionmedia.com

Webcasts
Jenna Johnson
Tel: 612.598.3446
jjohnson@extensionmedia.com

The ConFab
Kerry Hoffman
Tel: 978.580.4205
khoffman@extensionmedia.com

Will I see you at The ConFab?

The ConFab — an executive conference now in its 13th year — brings together influential executives from all parts of the semiconductor supply chain for three days of thought-provoking talks and panel discussions, networking events and select, pre-arranged breakout business meetings.

Why the time is now: Electronics are an essential part of everyday life the world over. Smartphones, the Internet of Things, cloud computing, digital television, autonomous cars, advances in healthcare and so much more are possible only because of the advances in semiconductor technology over the last 50 years.

Although some say the industry is maturing, but the reality is that the industry will see explosive growth from a variety of applications, including the IoT, 5G telecommunication, autonomous driving, virtual and augmented reality, and artificial intelligence/deep learning. IoT alone is expected to drive not only a huge demand for sensors, but a far more sophisticated cloud computing infrastructure that will employ the most advanced logic and memory chips available, including 7 and 5nm logic devices and 3D NAND.

These new and varied applications, including healthcare, are creating new demands for semiconductor technology. Devices will require more innovative packaging solutions, including heterogeneous integration of diverse components. New advances in MEMS and sensors, will be required as well as new wireless capabilities, thin film batteries and energy harvesting devices, flexible electronics, power electronics, analog, and silicon photonics.

What can you expect in 2017? The ConFab 2017 conference program is designed to identify new opportunities in these fast-growing markets, showcase critical technology trends and discuss what challenges still need to be overcome. On Monday, we'll hear where mainstream semiconductor technology is today through the keynote talk and the morning session. We will soon be announcing who these speakers will be, but past speakers include Brian Krzanich of Intel, Tom Caulfield of GlobalFoundries, Yoon Woon Lee of Samsung, Bill Chen of Nvidia, Roawen Chen of Qualcomm, Ali Sebt of Renesas and Wally Rhines of Mentor Graphics. Also on Monday, we'll have a sure-to-be interesting panel session focused on heterogeneous integration and advanced packaging, starting with a talk from Jan Vardaman of TechSearch. Siemen's Sia Langrudi is also slated to speak on Smart Manufacturing in the semiconductor industry, which will encompass the Industry 4.0 initiative, also known as the Industrial Internet of Things (IIoT).

On Tuesday, we'll kick things off with a look at the growth opportunities in the automotive market, particularly the autonomous, self-driving car. We'll follow that up with talks on MEMS and sensors by Kevin Shaw of Algorithmic Intuition and J.C. Eloy of Yole Developpement, and then a panel session that looks at the coming opportunities and changes in a range of diverse markets, including MEMS & Sensors, power electronics, biomedical, LEDs, displays and more. Panelists will include Laura Rothman Mauer of Veeco, David Butler of SPTS and Mike Rosa of Applied Materials.

On Wednesday, we'll hear from Alissa Fitzgerald (A.M. Fitzgerald & Associates), followed by a talk on flexible electronics by Jason March, the director of technology at NextFlex. We'll conclude with a market overview from Bill McClean of IC Insights, who is sure to give us an idea of what coming years will bring, the impact of industry consolidation and new growth opportunities.

The ConFab also includes well-attended evening receptions plus breakfasts, lunches and refreshment breaks. These offer exceptional networking opportunities for people to meet in a relaxed environment conducive to making lasting connections.

What is clear is that the need for real collaboration has never been greater. That's why The ConFab 2017 is invaluable. In 2017, we are extending personal invitations to even more VIPs, and we expect heightened interest and involvement as industry leaders gather to tackle tough questions, take a look at the new growth opportunities and challenges, network in a unique environment and collaborate on the future. Check out our website at www.theconfab.com to see how you can participate. ◆

Pete Singer, Editor-in-Chief

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