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Insights for Electronics Manufacturing

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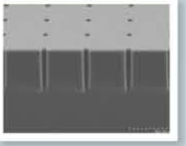
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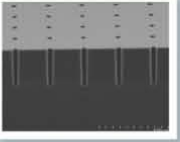
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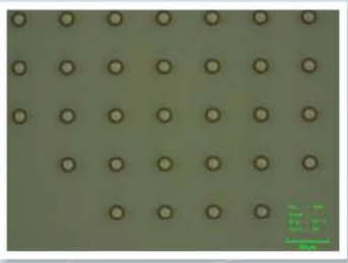
Si ETCH TO REVEAL Cu TSV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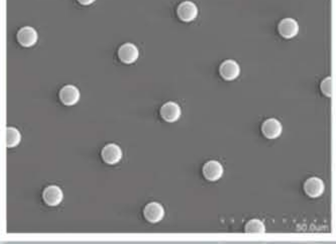
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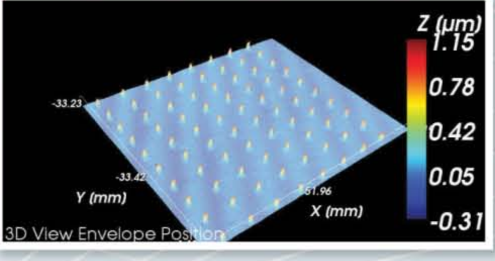

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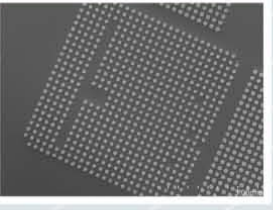

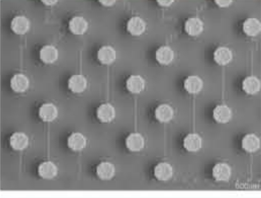

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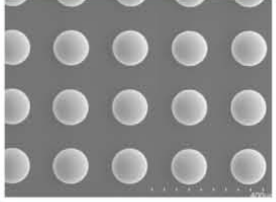

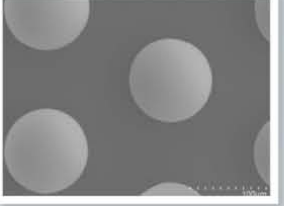

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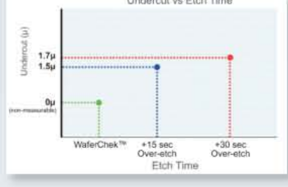
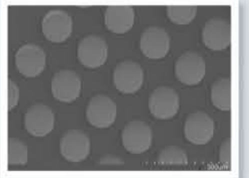
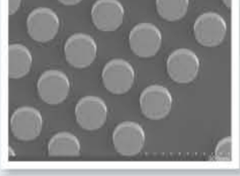



UBM Post Etch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APRIL 2012 VOL. 55 | NO. 3

Cryogenic aerosol cleaning is well-equipped to deliver 99% or better removal of the larger, probe-related defects associated with in-line electrical testing. Source: FSI International.

COVER

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The high particle removal efficiency of cryogenic aerosol cleans can provide yield advantages in the BEOL after in-line testing, without altering substrate properties. *Jeffery W. Butterbaugh, FSI International, Chaska, MN*

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New constraints and challenges associated with FinFET manufacturing are reviewed from the etch point of view. *Keren J. Kanarik, Gowri Kamarthy, and Richard A. Gottscho, Lam Research Corp., Fremont, CA.*

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The effect of pumping methods on the etching of PE-TEOS wafers was investigated. *Jung-Soo Lim, R. Prasanna Venkatesh, and Jin-Goo Park, Dept. of Materials Engineering, Hanyang University, Ansan, 426-791, Korea*

22 **LED PACKAGING** | Low cost AlN substrate technology for HBLED and power semiconductors
A technology has been developed that allows AlN to be sintered at lower temperatures. This allows the material to be sintered and flat fired in a continuous furnace very similar to furnaces used for alumina. *Jonathan Harris, CMC Laboratories, Tempe, AZ.*

27 **450mm** | The move to 450mm: Europe's perspective
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Web Exclusives

2012 capex up on stronger 28nm demand

Semiconductor foundries are already considering raising their 2012 capital expenditure budgets, says Terence Whalen, Semiconductor Equipment analyst for North America at Citi. The wafer foundry ramp up shows no signs of ending, with TSMC and Samsung likely to raise capex in 2012 to accommodate 28nm demand. Coupled with improving gross domestic product (GDP) and Purchasing Managers Index (PMI) that could increase overall IC demand in 2H, wafer fab equipment orders could grow 5-10% in 2012. **http://bit.ly/GAWeTP**

ISSCC: a memory analyst's view

The International Solid State Circuits Conference (ISSCC) took place in San Francisco the week of February 20. From a memory perspective, this show contained some highly interesting presentations. Jim Handy, an analyst at Objective Analysis, reports that both Toshiba and SanDisk presented papers on the two companies' 128Gb NAND chip that uses three-bit cells and a 19nm process to achieve the smallest die size (170.6 mm^2) for a chip of this density. This device uses some exotic techniques, like air gaps to lower the bitline RC time constant, and an internal temperature sensor, both of which help to keep the speed similar to devices processed on less aggressive geometries. **http://bit.ly/z57xr7**

High volume 200 mm fab reduces costs

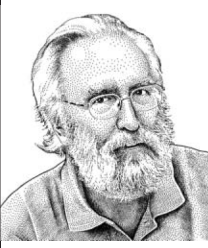
In this case study, a fab implemented a wafer-like, wireless airborne particle sensor as an alternative wafer monitoring methodology. Compared to the fab's previous monitoring method, the wireless airborne particle sensor more quickly measured combinations of potential particle source elements to determine the presence of particle sources and counts. **http://bit.ly/GJFr17**

n&b news and blogs

GloFo's FinFETS are better than Intel's!

This confident statement came from Subramani (Subi) Kengeri of GLOBALFOUNDRIES (GloFo) during the panel session in the GloFo/IBM/Samsung Common Platform Technology Forum (CPTF), held on March 14th in the Santa Clara Convention Center, reports blogger Dick James of Chipworks.

Towards the end of the panel discussions, the host, Jaga Jagannathan of IBM, asked Subi "How do you stack up against Intel, especially in the SoC/smartphone space?" This clearly took Subi by surprise, but after some preamble, he focused on FinFET development, which AMD, then GloFo, have been working on for the last ten years. In conjunction with customer input, they have been focusing their finFET efforts to optimize the 14 nm) process for mobile SoCs. He said that this was what would differentiate them from Intel, and in that space. "We believe we have a much better finFET that is optimized for mobile SoCs," he said. **http://bit.ly/GzUJHM**



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The internet of things

The future of electronics is increasingly being shaped by two major trends: mobile computing and the "internet of things." The pervasiveness of mobile is fairly obvious, with 1.2 billion units expected to ship in 2014. The internet of things is less obvious, but slowly becoming a reality. The idea is that all objects in our environment will be equipped with sensors and identifying devices and connected to the internet. And I'm talking about everything, from buildings to freeways to food containers to medicine.

"Dedicated hardware is the best way of saving power."

With the internet of things, companies would not run out of stock, as involved parties would know which products are required and consumed. Mislaid and stolen items would be easily tracked and located, as would the people who use them.

At the recent Common Platform Technology Forum -- produced by Global Foundries, Samsung and IBM -- Simon Segars, executive vice president and general manager of the physical IP division at ARM, spoke about the impact on the way electronics are designed. "Microcontrollers and sensors are getting embedded into pretty much everything we interact with," he said. "You're going to need very small and very power-efficient technology, and a power-efficient wireless network to pull it all together. "

Segars said changes in computing requirements will create a demand for smaller, dedicated technologies. "It's the case in pretty much any form of electronics, if you know what you're doing, dedicated hardware is the best way of saving power. This is why you have a video engine and a graphics engine in your phone -- because it's very expensive to do it on a general purpose computer. The same holds true for servers," he said.

Rather than get "fixated" by the apps processor, Segars said it's important to pay attention to the other chips required, such as smaller control chips used to manage battery power or the touch screen. "These aren't necessarily manufactured on the most leading edge digital process," he said. "These are using older, more mature processes which can drive higher voltages. There's a need for continual evolution on that kind of process technology, because it's going to be required for a long time." The big boys will have their $7.5 billion fabs, but let's not forget about the importance in investing in the rest of the supply chain.

—**Pete Singer,** Editor-in-Chief

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WORLD | Worldwide semiconductor revenue is projected to total $316 billion in 2012, a 4% increase from 2011, according to **Gartner Inc.** This outlook is up from Gartner's previous forecast, made in Q4 2011, for 2.2% growth.

WORLD | Semiconductor fab equipment spending will remain flat in 2012, shows SEMI's World Fab Forecast report. But look for a record spend from semiconductor makers in 2013, jumping from $38.85 billion spent in 2012 to $45 billion in 2013.

ASIA | **AMEC** installed a second-generation dielectric etch tool, the Primo AD-RIE, at Chinese foundry SMIC. It is the first time AMEC has installed the Primo AD-RIE in China.

ASIA | The formal announcement of China's light emitting diode (LED) subsidy program may drive tool utilization expansions for LED chip makers.

EUROPE | **Novaled AG** filed a registration statement with the US SEC for a proposed initial public offering. Novaled makes technologies and materials for organic electronics, particularly OLEDs.

WORLD | **Tokyo Electron Ltd.** (TEL) will join research organization CEA-Leti's IMAGINE open, collaborative industrial program on advanced lithography for semiconductor manufacturing.

USA | **Tabula** is implementing a family of 3PLD products manufactured by Intel using its advanced 22nm 3D trigate process and co-optimized packaging technology.

Common Technology Platform Forum looks to the future

The 2012 Common Platform Technology Forum took place March 14 at the Santa Clara Convention Center, with registration topping 1200 attendees by noon. The Common Platform is a Samsung /IBM/ GlobalFoundries foundry services entity created to provide a common design space with an assured production capability.

The meeting kicked off with Ana Hunter, Samsung's foundry business VP. The Common Platform had its roots in 65nm, and is presently working with 20nm gate-last and 14nm FinFET. Pre-revenue investment in the 20nm to 14nm range approaches $10B, with $1-2B in process development, $250M in IP & design libraries, $100M in chip design and $7B in fab construction.

Gary Patton, VP of SRDC at IBM, gave the first keynote with prognostication on the kind of technology development that is in the pipeline beyond traditional CMOS scaling. We are presently in the 3D decade, both in terms of 3D transistor design and 3D packaging integration. Next will be the decade of nanotechnology materials, in which the critical device dimensions do not depend on photolithography.

Long-term R&D for this coming decade is already underway, as an extremely long lead time is required for commercialization to manufacturing. In 2011 IBM broke its own US patent record with 6,000 filings, a position it has held for 19 straight years. He hopes EUV will be ready for 10nm, "but we have a dual path." At 10nm, EUV will provide a bump in k1 factor from 0.15 to 0.55, better that we enjoyed at 90nm. The scanner still needs a 10x improvement in light power, but additional work is needed in photoresist materials and mask fabrication and inspection technology. A new EUV Center of Excellence at Albany CNSE is expected to be operational later this year.

Below 80nm, resist development is focusing on directed self-assembly (DSA) of block copolymers. Presently, the 22/20nm work is being done in East Fishkill; 14/10nm at Albany; and 7nm & beyond at Yorktown Research. Fully depleted device structures are the recurring theme going forward. CNT devices provide advantages over FinFETs in terms an order of magnitude reduction in power consumption at the same operating frequency, or an order of magnitude increase in frequency at the same power. With these innovations in design constructs and materials, Patton

Continued on page 8

Inside Apple's new iPad display technology

The new Apple iPad, generation 3, uses a 2048 × 1536, 264 ppi retina display, quadrupling the pixels of the previous generation. However, Apple may be losing its cutting-edge status when it comes to gesture recognition beyond touchscreens.

Apple's higher-resolution iPad display relies on super high aperture (SHA) pixel designs — a method of increasing aperture ratio by applying approximately a 3µm thick photo-definable acrylic resin layer to planarize the device and increase the vertical gap between the indium tin oxide (ITO) pixel electrodes and signal lines. This reduces unwanted capacitive coupling and enables the electrode to be extended over the gate and data lines without causing cross talk or affecting image quality, explains NPD DisplaySearch. More than 25% of LCDs adopt SHA technology and that is likely to continue to grow in the future.

Overcoat process	Normal	UHA/SHA
Stucture	ITO	ITO Organic film
Advantage	• Easy process (normal)	• High aperture ratio
Application	• Conventional	• High brightness (light efficiency) • High resolution • Transflective/reflective modes

Conventional to SHA Pixel Design Comparison. Source: DisplaySearch TFT LCD Process Roadmap Report. Note: Image refers to VA type SHA pixel.

The iSuppli Displays Materials & Systems Service believes Apple likely has qualified three sources for the display in the new iPad: Samsung, LG Display (LGD), and Sharp, with volume shipments likely only from Samsung in the near term. Although they are currently shipping displays in small quantities, LGD and Sharp are expected to ramp up volume production of new iPad displays in April. SHA technology was pioneered by Sharp and JSR many years ago, NPD DisplaySearch notes. IHS predicts that Apple is likely to begin shipping new iPads with displays from these suppliers in Q2 2012.

Sharp is working with a new indium gallium zinc oxide (IGZO) technology that enables higher resolutions. The company now is working to ramp up the production of IGZO thin-film transistor (TFT) panels at its Gen 8 fab in Kameyama, Japan, but manufacturing problems could affect both the availability of displays for a full rollout of the new iPad,

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news cont.

Continued fromn page 6

noted that the transistors are still much more amenable to scaling than interconnects, in which RC performance and structural reliability in both the conductors and the insulators doth protest mightily with scaling. Photonic interconnects on chip continues to be an area of intense development, moving now from fundamental unit performance demonstrations to system integration. The packaging concepts that he reviewed, while challenging, were consistent with advanced packaging concepts that have been progressing over the past five years. TSV is currently in volume manufacturing for power system chips. For stacking large DRAM chips on top of high performance MPU, he expects TSV to be in production within 2 years.

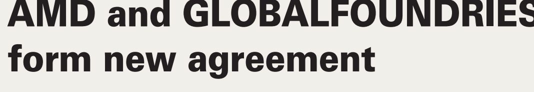
Subi Kengeri, head of the advanced architecture development group, filled in for GlobalFoundries CTO Gregg Bartlett to discuss the convergence of consumer mobility applications enabled by semiconductor technology advances. Foundries are a 300mm leading edge business growing at 15% CAGR. Since 90nm, the time between design start and tape out has been extending as design complexity increases. Design cost has been increasing at a 25% CAGR, whereas fab cost has been increasing at 18%, albeit a much larger number. Smart mobile computing is starting to move into the design driver seat that has up to now been occupied by MPU and GPU functions. Gate last HkMG at 20nm has been selected to meet these needs for 3rd generation HkMG FinFET mobile devices. At 14nm FinFET, you need 100 WPH (wafers per hour) throughput with EUV to break even with 193i with multiple patterning; 180 WPH provides a compelling advantage for EUV.

Jong Shik Yoon, Senior VP Semiconductor R&D at Samsung, spoke on opportunities and challenges in 3D device integration. SOI FinFETs were pioneered by IBM, while Samsung & Intel led the development of bulk FinFETs; the Common Platform supports bulk FinFET. SOI FinFET is used by IBM for server and specialty mobile applications. CNT FET work has been going on at Samsung as well.

Simon Segars, EVP & GM of the ARM Physical IP Division, wrapped up the morning with the fabless design and manufacturing implementation perspective. Industry drivers today are mobile computing, servers and the "internet of things." Lower cost entry level smart phones represent another billion unit market globally. Mobile networks require about 1 server for every 600 phones, which puts the server demand into perspective, particularly as servers alone become a more significant percentage of world power consumption (still single digits for now). Global internet mobile traffic for 2015 will be about 966 exabytes. Simon is confident that the collaboration infrastructure that has gotten them to 20nm is extendable to 14nm.

The Common Platform Technology Forum panel session.

A panel discussion featuring R&D leaders from the 3 Common Platform partners, ARM and CNSE on the R&D pipeline for future semiconductor technology innovation followed lunch. Michael Liehr, VP Research at CNSE pointed out several ways in which the fab there operates like an industrial site, with professors leading engineering teams that function as much like an IDM process development group as a graduate student research group. GlobalFoundries in Malta, NY is currently running 32nm production and 20nm full flow qualification. Work on DSA for photolithography started at IBM in 2000 and is still not ready for prime time. Similarly, copper interconnect development work started at IBM in 1984 and didn't go into production until 1997, and even then came as a surprise to many outsiders. This is indeed a very long development pipeline. **—M.F.**



AMD and GLOBALFOUNDRIES form new agreement

AMD amended its wafer supply agreement with GLOBALFOUNDRIES Inc., with a negotiated wafer price mechanism for 2012. AMD will also transfer its remaining ownership interest in GLOBALFOUNDRIES to GLOBALFOUNDRIES, eliminating its equity stake in the foundry company. AMD relinquishes its board seat at the foundry.

GLOBALFOUNDRIES, celebrating its 3-year anniversary of operation, will now be wholly owned by the Advanced Technology Investment Company (ATIC), the company announced. **—M.C.**

Continued fromn page 7

as well as the cost of the iPad displays. LGD has been pioneering the use of advanced in-plane switching (IPS) display technology, particularly in media tablet displays.

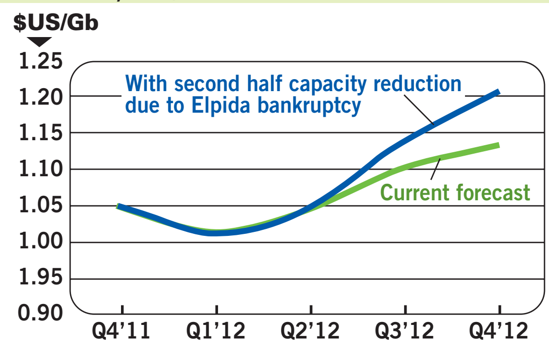
IMS Research believes Apple will need to embrace embedded vision-based technologies in its next product releases, not incremental technology upgrades as seen in the gen-3 iPad.

Apple is largely credited with bringing touchscreen interaction to the masses thanks to the iPhone. Now, other user interface technologies — particularly gesture recognition, voice commands — are complementing touch interfaces. Competitors such as Samsung and Microsoft have steadily begun integrating these technologies. Yearly worldwide shipments of devices with next-generation user interface technologies will grow to nearly 3.8 billion units in 2015, says IMS Research.

Apple's competitors are more aggressively deploying camera-based gesture recognition applications, as well as voice control (Apple's Siri did not get a spot on the new iPad). Microsoft uses gesture control with the Xbox 360 and upcoming Windows 8 laptops and tablets, along with gesture-friendly common interfaces across devices. Microsoft deploys standard or enhanced front-facing cameras for the new gesture-control applications. Android-based smartphones and tablets incorporating gesture control will debut in volume in late 2012. **—M.C.**

Elpida files for bankruptcy

Elpida Memory Inc. resolved to file a petition for the commencement of corporate reorganization proceedings at today's meeting of the board of directors, and filed the same with the Tokyo District Court. Elpida's consolidated subsidiary, Akita Elpida Memory Inc., also saw the commencement of corporate reorganization proceedings, and there is a possibility that claims against the said company may not be collected. Nikkei called the bankruptcy protection filing "the largest corporate failure among Japan's manufacturers since the end of World War II."



If more than 25% of Elpida's manufacturing capacity is taken offline, the global average selling price (ASP) for all DRAM shipments is projected to rise to $1.21 by the end of 2012, up 15.5% from $1.05 at the end of H1. The figure shows global ASP for all DRAM shipments (global DRAM revenue divided by gigabit shipments). SOURCE: IHS iSuppli Research.

Elpida cites sluggish DRAM growth in personal computers, as well as an increase of the capacity of DRAM per unit, for its overcapacity after 2006-2007 capital expenditures on wafer fabs and equipment. "At the beginning of 2007, the price of DRAM started falling sharply and, combined by a significant decrease of demand for the products due to the global economic downturn begun in the fall 2008, such price further declined.

DRAM chip prices may rise in the near term after Elpida filed for bankruptcy protection, Taiwanese memory chip vendors said. The remaining players in the DRAM market will benefit from reduced supply with a boost in pricing and revenue in H2 2012, according to the IHS iSuppli Memory & Storage Service. IHS conservatively estimates that 2012 DRAM revenue will exceed $30 billion, compared to the previous forecast of $24 billion.**—M.C.**

Driving down HB-LED package costs

HB-LED packaging accounts for 40% to 60% of finished LED cost. This makes packaging the #1 target for cost reduction.

Griff Resor,
Resor Associates, Maynard, MA USA

By convention, LED package costs do not include the cost of converting a finished LED to a lighting product — the "Luminaire". Mark McClear of Cree has repeatedly said an integrated approach is needed to deliver an attractive value for consumers. I'll come back to his point at the end.

A few years ago HB-LED packages were assembled from many discrete parts. These included a metal lead frame, a molded pocket for the LED, a zener diode, a mirror coating for the pocket, a heat sink for the LED, wire bonds for electrical connections, a sprayed on phosphor coating, an encapsulant to protect the assembled parts, and an attached lens.

Today LED packaging is using an integrated thin film approach. A single AlN "panel" about 100 mm square is used. Top side patterns provide a LED heat sink, area for wire bond connections, and electrical traces to vias that connect to the bottom side. Bottom side patterns provide for heat transfer and surface mount connections. Significant savings are realized by doing "panel" scale assembly. For example, lenses are molded 500 at a time on one AlN panel.

Philips-Lumileds has changed their LED structure, to enable flip-chip mounting of the LED on the AlN panel. This eliminates the wire bond cost, and eliminates the area needed for wire bonding. This enables a smaller, lower cost LED package. Expect more flip-chip LED designs.

LEDs

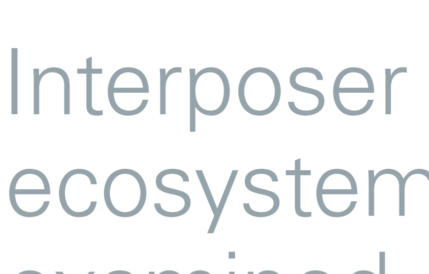
An analysis of packaged LEDs used for LCD-TV backlighting shows that much of the HB-LED package is a "frame" around the LED. This area does not increase significantly as LED area increases. The real goal is to reduce the cost/lumen, not just the package cost. By increasing lumens emitted from a package, one can reduce the packaging cost per lumen.

This tactic is already being employed in HB-LED packages — several small LED chips are being mounted inside one package. This provides an added benefit. The LEDs can be wired in series to increase the operating voltage. Higher voltage reduces the power conversion costs in the Luminaire. Which leads back to Mark McClear's point — consider the Luminare cost.

The Resor Associates' COO model was designed to study the tradeoff between package costs, LED area and LED yield. It is clear that larger LED chips significantly improve the cost/lumen for finished LED's. As yield improves, the optimum tradeoff shifts to larger LEs. So add improved LED yield to the roadmap for LED package cost reduction!

From the life cycle of ICs and FPDs it is clear that LED makers will use some of their cost savings to elaborate the product in ways that reduce the finished Luminaire cost. The most promising idea that I've seen is "integrated" LEDs. For example, one could form two strings of 40 LEDs each. These could operate directly at a line voltage of 120volts, eliminating the power conversion parts in the Luminaire. Why don't we see integrated LED products today? Defects/cm^2 are too high in LED fabs — a significant reduction in defect levels is needed first.

Bottom line, there are many ways to reduce the packaging cost in LEDs. But to realize some of these one has to look beyond the traditional LED package to the Luminaire and to the LED chip. ◆



Interposer ecosystem examined

At the recent IMAPS Device Packaging Conference in Ft. McDowell, AZ, Solid State Technology's Insights from the Leading Edge (IFTLE) brought together a panel of manufacturers, users and market specialists to discuss the evolving 2.5D / 3D Infrastructure.

Dr. Phil Garrou, Contributing Editor

I was joined by Douglas Yu, Sr. Director of front end and back end technology development for TSMC; Jonathon Greenwood, Director of Packaging R&D at GlobalFoundries; Remi Yu, Deputy Division Director of UMC; Nick Kim, VP of electronic packaging technologies at Hynix; Rich Rice, Sr. VP of sales for ASE ; Ron Huemoeller, VP of Advanced 3D interconnect at Amkor; Matt Nowak, Sr. Director of Engineering at Qualcomm and Jan Vardaman, President of TechSearch Inc.

The panelists were unanimous in their descriptions of mainstream 3D packaging being represented by 5-8µm copper through-silicon-via (TSV) middle on 50µm-thick silicon from integrated design manufacturers (IDMs) or foundries and interposers as 10µm Cu TSV in 100µm-thick silicon. Vardaman points out that some larger "TSV-last" from the backside are, of course, also being used in image sensors, and other TSV variations are being seen in MEMS applications.

When discussing interposer sourcing, Amkor's Huemoeller indicated that only 3 players were close to being ready to deliver interposers of any kind: TSMC, UMC, and GlobalFoundries. While some in the audience were resolute in their conviction that only panel-size formats (i.e., flat panel glass or laminates) could deliver the economics necessary to make 2.5/3D packaging mainstream, the assembled experts agreed that while glass panels and even possibly advanced laminates presented interesting possibilities for low-cost future products, they currently cannot meet requirements and are in the earliest stages of R&D.

If we assume interposers will be divided into the categories of "coarse" and "fine," the infrastructure question becomes "Where will these interposers be coming from?" Fine interposers by definition (1µm l/s) will require front-end semiconductor manufacturing tools and thus will be restricted to today's IDM and foundries that have such capability in place.

While all the outsourced semiconductor assembly and test (OSAT) providers have redistribution layer (RDL) technology capable of fabricating "coarse" interposers, so far none of the major players — ASE, Amkor, SCP, SPIL — have announced that they are entering the interposer business. TSMC, UMC, and GlobalFoundries all indicated that they will be commercializing fine-featured interposers, although, as of yet, only TSMC and IBM have initiated small-volume product production.

Nowak indicated that interposers would add substantial cost and as such probably would not be a broadly accepted solution for low cost mobile products. In response, TSMC's Yu responded that the addition of an interposer added cost to the overall component, but that "...this [2.5D] solution also offers cost savings by reuse of IP and separating digital and analog circuitry and allowing partitioning of costly SoC," and that this could make it the lowest-cost solution.

Based on the positions of these experts, one can conclude that initial interposer supply will be so-called "fine featured" high-end product, which will be provided today by foundries/3D-active IDMs. While we can anticipate that there will be future products designed to take advantage of "coarse" interposers, and some of the initial fine interposers might be able to migrate to coarse interposers as they become available, we will, initially at least, be limited by the availability and cost of foundry-supplied interposers. ◆

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Defect removal using dry cryogenic aerosols

JEFFERY W. BUTTERBAUGH, *FSI International, Chaska, MN*

The high particle removal efficiency of cryogenic aerosol cleans can provide yield advantages in the BEOL after in-line testing, without altering substrate properties.

Measuring the electrical performance of transistors formed in FEOL processes has traditionally forced device manufacturers to choose between the lesser of two yield-reducing evils, either testing at first metal (in-line) and causing higher defectivity on tested wafers, or waiting to test only finished devices with the potential of filling the manufacturing line with out-of-spec product.

The in-line testing method creates particulate defects at the M1 layer and M2 layers that can significantly reduce die yield. During this process, the physical contact between the test probe tip and the contact pads of the circuit – usually a test structure located in the scribe lines between the die – creates a scrub mark and sheds contact pad material. Particles that migrate to the active circuitry can produce a short between metal lines or between subsequent metal layers. The defects generated can cause an entire wafer to be scrapped. As a result, a fab with 25,000 wafer starts per month will potentially sacrifice one wafer per lot, or 1,000 wafers per month, based on typical in-line sampling strategies.

Meanwhile, manufacturers that choose to delay electrical testing until after wafer processing completion, potentially put at risk 100 percent of work-in-progress (WIP) processed from M1 to final metal.

Because of the high WIP values driven by increasingly elaborate BEOL processing, manufacturers typically judge yield loss from in-line test to be more economically acceptable – even in the face of test-induced revenue losses that can reach hundreds of thousands of dollars per month.

These in-line test related losses, however, can be drastically reduced by integrating a dry cryogenic aerosol cleaning process after first or second metal in-line testing. This article discusses yield advantages gained by leveraging the high particle removal efficiency (PRE) of cryogenic aerosol inserted in the BEOL after in-line testing, without altering substrate properties [1-4].

High PRE and safety with exposed materials, fragile structures

IC manufacturers have successfully inserted cryogenic aerosol cleaning into the process flow at many nodes as a viable technique to safely remove particles from surfaces -- particularly as a replacement of conventional wet techniques. Unlike wet technology, dry cryogenic aerosol technology cleans substrates without concern for film etching, material changes, watermarks or electrical charging. Today, those yield-protecting characteristics, including the ability to collect valuable parametric data without sacrificing yield, [5] have helped establish post in-line test cleaning as the most frequently used application of cryogenic aerosol

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cleaning technology.

Maintaining product integrity throughout the manufacturing process is critical. BEOL features that contain copper, along with porous low k dielectrics easily altered by chemicals and water absorption, increase the difficulty in maintaining the integrity of substrate materials during cleaning, especially as feature sizes and low k values decrease.

Conventional water or chemical scrub processes are not compatible with many advanced materials and cannot be used to safely remove in-line testing debris. Wet chemical cleans can damage device performance through copper corrosion, low-*k* dielectric degradation from moisture absorption, insufficient drying in high aspect ratio features, and drying marks caused by mixed surface hydrophobicity.

All-dry, chemical-free cryogenic aerosol, by comparison, is well established as a yield-increasing cleaning methodology that can achieve high particle removal efficiency (PRE) without concern for structure damage, film etching, material changes, watermarks or electrical charging. The aerosol is safe to apply on any metal or dielectric exposed at the test level. By avoiding corrosion, etching, and altering surface charge properties, manufacturers can recover nearly all of the final yield loss associated with in-line testing. In addition, successfully eliminating yield penalties encourages early, expanded testing feedback that leads to improved data collection and tighter process control.

The cryogenic aerosol process: detach, diffuse and demove

The cryogenic aerosol is formed from inert argon and/or nitrogen gas that is cooled and partially liquefied as it passes through a liquid nitrogen dewar. The resulting liquid-and-gas mixture is delivered to the process chamber, which is held at reduced pressure. As the cryogenic gas/liquid mixture flows from a linear array nozzle positioned above the substrate, rapid expansion creates sub-micron droplets that freeze to form solid aerosol clusters.

The solid clusters impact the substrate, colliding with and dislodging particles through momentum transfer. Thermophoresis also assists in moving detached particles away from the surface. A high laminar flow of nitrogen across the surface sweeps particles (and aerosol clusters) away from the wafer. Defects entrained in the gas flow are removed from the chamber by a vacuum pump.

The aggressiveness of the cryogenic aerosol is controlled to optimize the cleaning process and balance particle removal efficiency with potential pattern damage. The intensity of the aerosol's energy and size is managed by varying the argon-to-nitrogen gas ratio, process chamber pressure, and the pressure (temperature) of the liquid nitrogen heat exchanger. As an example, lower chamber pressure results in smaller, higher velocity cryogenic aerosols. Smaller, faster cryogenic aerosols increase PRE, especially for particles down to 45nm in size.

Non-damaging particle removal protects yields

A study to evaluate cryogenic aerosol defect removal, across multiple BEOL processing steps, used 300mm bare Si wafers in a 65nm logic production line [1]. For all particle sizes measured, PRE with cryogenic aerosol cleaning was 99% or greater, with no material loss or substrate modification.

The PRE values on a blanket test wafer are a critical metric and serve as a guide to estimate the final defect count on a device wafer after processing. Using these PRE values, the average remaining defect count is expected to be less than two for particles larger than 0.12μm. **Figure 1** shows typical clean efficiency data for particles greater than 45nm collected in FSI test lab. Fab installations deploying post-probe cleaning to remove fall-on defects created by in-line testing may use conventional scrubber techniques to remove particles from the backside of the wafer.

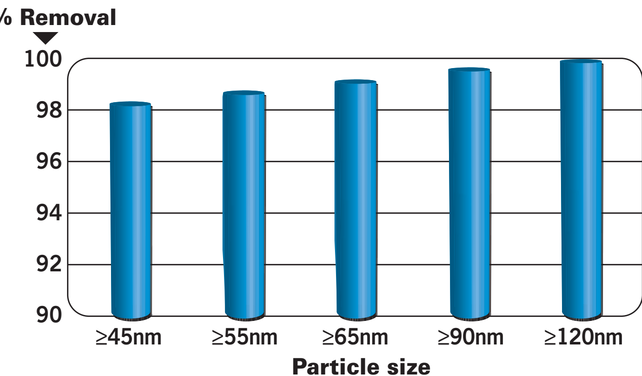

FIGURE 1. Typical clean efficiency data collected in FSI test lab. Cryogenic aerosol process proves effective for large & small particles.

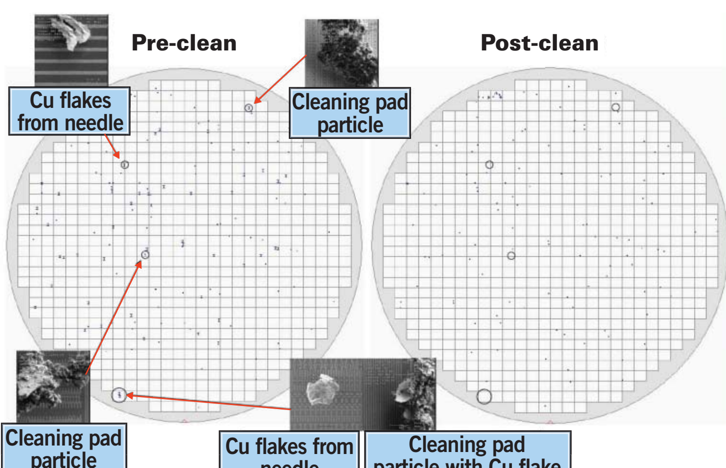

FIGURE 2. Defect maps before cryogenic aerosol treatment indicating the types of defects that are easily removed.

However, in many fabs wet treatment is minimized on the device side of the wafer following Cu CMP. In a 40nm production line example, replacing a scrub-clean sequence with cryogenic aerosol cleaning resulted in nearly a 60% improvement in defectivity, with no material loss or substrate modification.

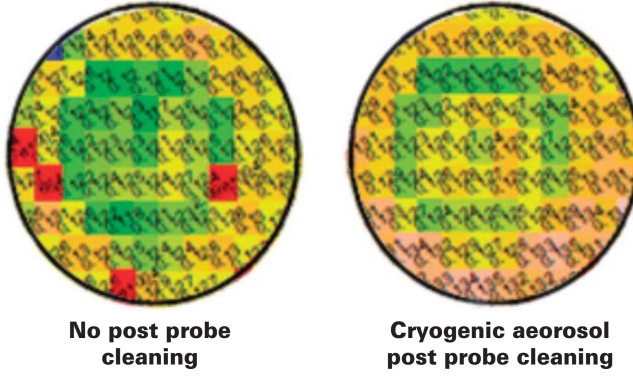

FIGURE 3. Wafer maps show that the cryogenic process virtually eliminates probe yield loss. Wafers with no clean have more defects.(Red indicates failed die).

Fourier Transform Infrared (FTIR) analysis detected no change in the porous low k dielectric film before or after exposure to cryogenic aerosol. This confirms the absence of moisture absorption that would degrade the dielectric constant. In addition, cryogenic cleaning reduced cost-of-ownership (CoO) by 30% compared to the process-of-record (POR).

An additional manufacturer study [2] looked specifically at in-line testing at the first metal layer in a copper process. Debris-related defects were detected by electrical testing at the next metal layer.

Fig. 2 shows a wafer map of defects before and after cleaning. **Fig. 3** shows electrical test maps of wafers in the test lot. Red squares mark electrical defects on uncleaned wafers. **Fig. 4** charts the functional yield improvements of approximately 19% that the manufacturer attributed to the cleaning process on two different lots that received 100% testing for reticle qualification.

Conclusion

The non-damaging, high particle removal efficiency of cryogenic aerosol cleaning is well-established across various IC process nodes as a critical factor in manufacturing yield recovery, especially as an alternative to water and chemical scrub technologies, which are incompatible with new materials. With a PRE performance validated against defects as small as 45nm, cryogenic aerosol cleaning is well-equipped to deliver 99% or better removal of the larger, probe-related defects associated with in-line electrical testing. In addition, by enabling engineers to return wafer yield previously sacrificed to gain valuable parametric data, cryogenic aerosol cleaning dramatically alters the cost-benefit calculation in favor of increased in-line testing. ◆

Increasing yield
Cryogenic clean
POR

FIGURE 4. Final yield of wafers that were 100% probed for reticle qual. Final yield improved by 19% for wafers that received the cryogenic aerosol treatment.

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ETCH

Plasma etch challenges for FinFET transistors

KEREN J. KANARIK, GOWRI KAMARTHY, AND RICHARD A. GOTTSCHO, *Lam Research Corp., Fremont, CA.*

New constraints and challenges associated with FinFET manufacturing are reviewed from the etch point of view.

As the industry moves to 3D tri-gate FinFET architectures to overcome transistor scaling issues [1], additional etch challenges have appeared that may require new approaches to plasma etching. Compared with planar transistors, the performance of FinFET devices will depend more on etch because the multiple gates and vertical fin structures are created by the etch process. Not only are there more etch steps required to form these structures, there are also more surfaces of a FinFET transistor exposed to the plasma, resulting in the need for high-precision etching with minimal — ideally no — structural damage.

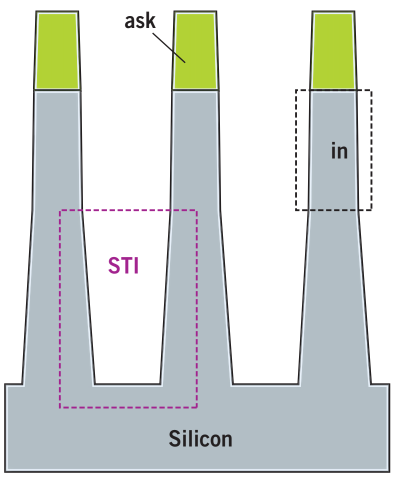

FIGURE 1. The fin/STI etch requires creating both tapered isolation trenches and vertical fins, which will form the transistor channels.

Fin/STI formation

Shallow trench isolation (STI) etch processes for conventional planar devices have increased in aspect ratio with each successive technology node. In the case of FinFET structures, there is increased complexity because the fin is formed directly from the Si substrate, and therefore the STI structure and fin are etched simultaneously. Different feature profiles must be created during the same etch process because STI requires a tapered sidewall, while the silicon fin requires a vertical sidewall, as shown in **Fig. 1**. With FinFET devices, for the first time, the etch process creates the actual channel (the fin), so producing a precisely vertical fin with low surface state density is critical. Any unintentional variation in the shape of the fin (width, height, profile) or excessive surface state density caused by plasma etch-induced damage would alter the transistor channel.

Gate formation

After the fins are formed, the FinFET gate must be etched so as to wrap around the fin (**Fig. 2**). As with the fin/STI etch, the sidewalls of the gate must be etched vertically to reduce variability of the device parameters. To accommodate the 3D topography, the etch needs to stop on top of the fin while etching further down to the silicon substrate. Once the etch reaches the base of the structure, complete removal of residue from the 3D corner requires ~70-100% over-etch time, compared with ~30% for conventional planar gates. Throughout the entire exposure time, the process must avoid etching or damaging the exposed fin, which would adversely affect device performance [2].

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Spacer formation

The spacer forms the mask for source/drain implantation, as well as encapsulates and protects the sidewalls of the gate. Like gate etch, spacer etch requires a directional process to prevent lateral consumption of the spacer material (CD loss), without damaging the exposed Si fin. In a planar transistor, integration schemes have typically included a liner film as a stop-layer to prevent Si loss during the etch process. In a FinFET device (and in many advanced-node planar devices), this liner film is omitted due to tight geometries, leaving the device fully exposed during the spacer etch. This is particularly problematic because a significantly longer over-etch is needed to fully clear residue at the bottom of the fin compared with planar transistors (~200-400% vs. ~30%). Consequently, the spacer etch is today considered the most challenging of the FinFET etch processes.

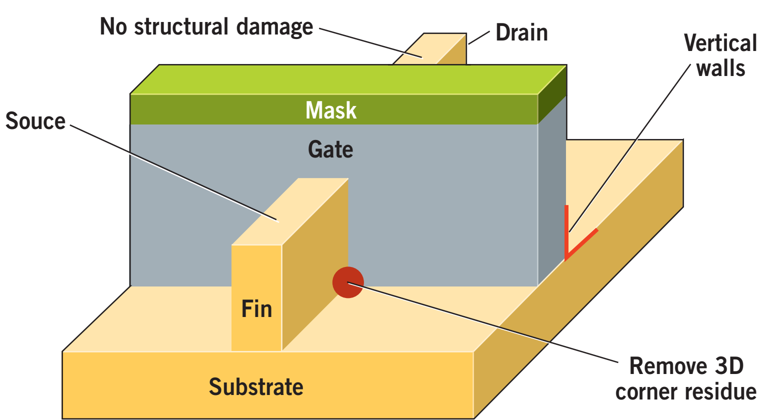

FIGURE 2. FinFET gate etch needs to simultaneously maintain vertical walls and remove corner residue, while protecting the exposed fin from structural damage.

Challenge of atomic-precision etching

As described above, one of the biggest challenges in enabling FinFET formation is to directionally etch the transistor features without damaging them — etching with atomic precision. The requirement of directionality is essential because ions are one of the fundamental root causes of plasma-induced structural damage. At the molecular level, energetic ions (~10-1,000eV) cause the exposed film surface to "blur" due to a collision cascade that can spread and penetrate many monolayers deep. This produces a damaged region (the selvage layer) of mixed contaminants, dangling bonds, and voids that are beneficial for fast etch rates, but compromise precision.

Here we define the parameter "Etch Precision", P_E, as the inverse of the number of damaged atomic layers that result from ion-enhanced etching. This can be expressed using measurable etch parameters:

Etch Precision,

$$P_E = \frac{1}{\#\text{damaged layers}} \propto \left(\frac{1}{ER_i} - \frac{1}{S \cdot J_R}\right) \cdot J_i \cdot \left(\varepsilon_i^{1/2} - \varepsilon_{th}^{1/2}\right) \varepsilon_i < \varepsilon_{sputter},$$

where ER_i = ion-enhanced etch rate (ignoring spontaneous chemical- or photon-induced etching), S = sticking parameter, J_R = reactant flux, J_i = ion flux, ε_i = ion energy, ε_{th} = threshold energy, and $\varepsilon_{sputter}$ = sputter threshold energy.

Ion-enhanced processes will have $P_E > 0$, and values for current etch processes typically range from approximately 0.01 to 0.1, where higher values indicate that fewer layers of film have been damaged by the ions (**Fig. 3**). Results approaching $P_E \sim 1$ have been realized under laboratory conditions with atomic layer etching (ALE), which uses alternating processes to remove one monolayer at a time [3]. Unfortunately, today's ALE techniques produce etch

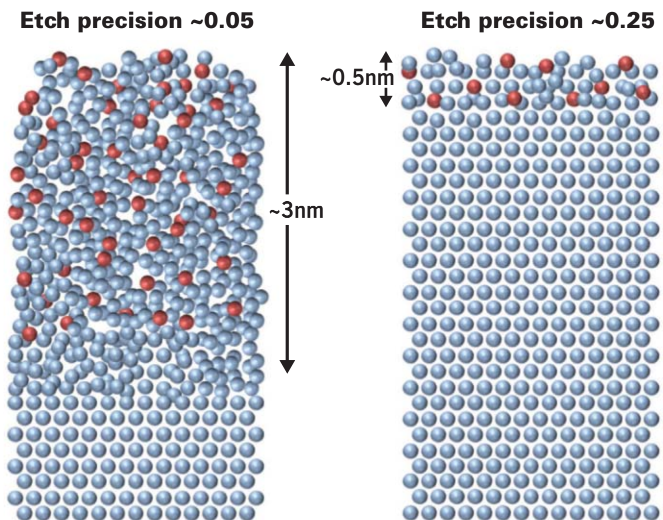

FIGURE 3. Higher Etch Precision (PE) indicates a more "pristine" or intact surface. Precision values for current etch processes typically range from ~0.01 to 0.1.

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rates that are too slow to be economically viable for manufacturing.

For practical purposes, the equation points to two conditions that improve P_E for a given ER_i. The first is to saturate the surface with reactants (increase $S \cdot J_R$). The second is to provide sufficiently energetic ions and surface-localized bombardment (increase $J_i \cdot (\varepsilon_i^{½} - \varepsilon_{th}^{½})$, $\varepsilon_{th} < \varepsilon_{sputter}$). The difficulty is in satisfying both conditions concurrently for the duration of the etch process, for example, because the ions compete with reactant stickiness. This is particularly challenging for the plasma methods currently used for etching planar transistors.

Approaches to improve etch precision

One approach for improving P_E is to lower electron temperature [4], which reduces the plasma potential and therefore lowers the ion energy to levels below those typically used for etch processes. Access to $\varepsilon_i < 15eV$ is possible with inductively coupled plasma reactors and other plasma sources and offers the benefit of a reactant-rich environment (saturates $S \cdot J_R$). However, the broader ion angle distributions at low energy will reduce directionality, causing CD loss **(Fig. 4a vs. 4b)**. Moreover, the low-energy ions are unlikely to overcome $\varepsilon_{th} > \sim 50eV$ for FinFET film stacks. Therefore, etching with low ion energy is not considered a desirable approach for critical FinFET etches.

Another approach is time modulation of plasma parameters. For example, "sync pulsing" is one technique where source and bias powers are turned on and off in ~100µs cycles. When the powers are shut off, there is less dissociation and shallower ion penetration, which some claim results in higher P_E [5]. However, less dissociation can result in insufficient reactant flux for surface saturation ($S \cdot J_R$), which can lead to Si loss during FinFET etching (**Fig. 4c**). A promising alternative is "bias pulsing" in which the bias power is turned on and off, while the source power remains

Continued on page 26

ETCHING

The effect of pumping methods on wet etching processes

JUNG-SOO LIM, R. PRASANNA VENKATESH, and **JIN-GOO PARK**, *Dept. of Materials Engineering, Hanyang University, Ansan, 426-791, Korea*

The effect of pumping methods on the etching of PE-TEOS wafers was investigated. The experiments were conducted in conventional wet bath and single wafer process tools, measuring etch rate, etch rate uniformity, and wafer-to-wafer uniformity, for various pumping methods.

Etching is one of the most important processes in semiconductor manufacturing industries. One such example is B-doped poly etchback process where silicon dioxide, PE-TEOS on wafers are etched, with the target etch depth of 500Å using BOE (Buffered Oxide Etchant, mixture of HF and NH_4F) as etchant. This process requires pumping to circulate and supply the etchant to the wafer's surface.

However, no studies have been reported in the literature regarding the influence of pumps on the performance of etching processes of wafers. In this present study, the performance of a magnetic levitation centrifugal pump (MLC-BPS 600, Levitronix) is evaluated and compared with the traditional diaphragm pumps (D1 and D2) for an etching process. The D1 has low pulsation intensity and high frequency of pressure oscillations compared to that of D2.

The etching tests were conducted using 8" PE-TEOS wafers and dilute hydrofluoric acid (DHF) as an etchant. In the conventional wet bath tool, the following conditions were employed: the concentration of DHF was 0.5 wt% and the process time was 10 min. The conditions were chosen to simulate semiconductor etching conditions. In general, etch rate normally changes with the position of the wafer in the bath. Thus, in the present study, five wafers including two dummy wafers were placed simultaneously in the etching bath for each test run and the wafer position in the etching bath was labeled as left, center and right. In the single wafer tool, the following conditions were employed: the concentration of DHF was 1 wt% and the process time was 3 min. The feed was injected at the wafer center for the three pumps. However, the spreading of chemicals on the wafer depends on the pumping method. As seen in **Fig. 1**, the chemicals are spreading over a fairly larger area of wafer in the case of diaphragm pumps, especially for D2 due to the higher pulsation intensity (30±6 psi) when compared to that of MLC pump (30 psi) and D1 pump (30±3 psi). Thus for the MLC pump, the experiments were conducted in an additional mode

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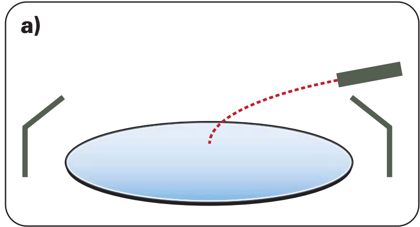

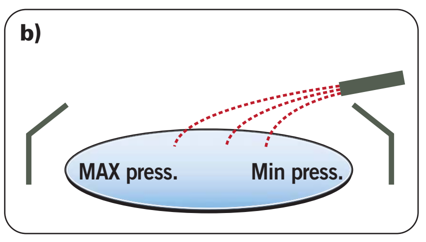

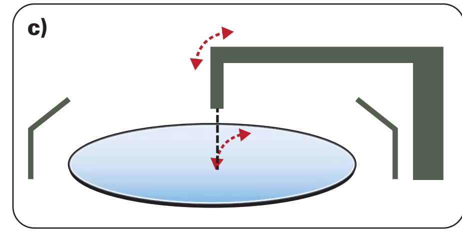

FIGURE 1. Schematics showing the spreading of chemicals over the wafer area for (a) MLC pump (b) diaphragm pumps and (c) MLC pump in swing mode. Note: The injection point is center for MLC pump, -10 to 50 mm (center is taken as zero) for D1 pump and -10 to 80 mm for D2 and MLC pump in swing mode.

called swing mode where the chemicals are supplied using a movable arm in such a way that the chemicals are spread over the same area as with D2.

The etch rate is calculated by measuring the thickness of PE-TEOS before and after the etching test. The thickness is measured by an inspection tool (K-Mac reflectometer, ST 4000, Korea) which is based on the principle of spectral reflectance. The thickness is measured at 33 specified locations on the wafer and the average etch rate and uniformity are calculated from these values.

Etching test in conventional wet bath tool

The etch rate of PE-TEOS oxide in 0.5 wt% DHF by the three different pumping methods is shown in **Fig. 2**. The average etch rate is 90 ± 5 Å/min for the MLC pump, 85 ± 5 Å/min for D1 and 95 ± 6 Å/min for D2, respectively (i.e., the etch rate is higher for D2 pump followed by MLC and D1 pumps, which show the lowest values). The high etch rate in the D2 pump may be attributed to its higher pulsation intensity. However, in the D1 pump, although the pulsation intensity is higher than MLC pump, the frequency of pump pulsations is higher which makes the etch rate more non-uniform

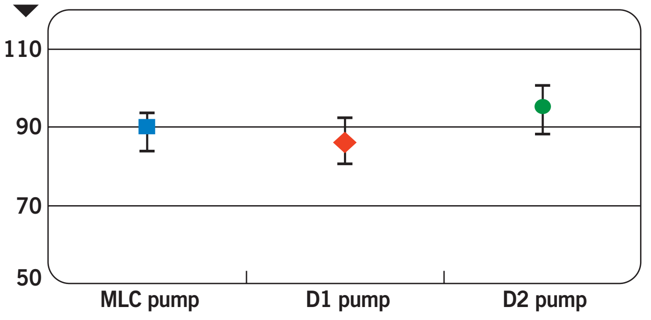

FIGURE 2. PE-TEOS etch rate in 0.5 wt% DHF for various pumps.

and hence the average etch rate observed is lower.

The within-wafer etch uniformity is lower for the MLC pump when compared to D1 and D2 pumps as shown in **Fig. 3.** In addition, the value of standard deviation is also relatively lower for the MLC pump when compared to the other two diaphragm pumps. This clearly says that flow behavior has a strong influence on etch uniformity. Since the flow

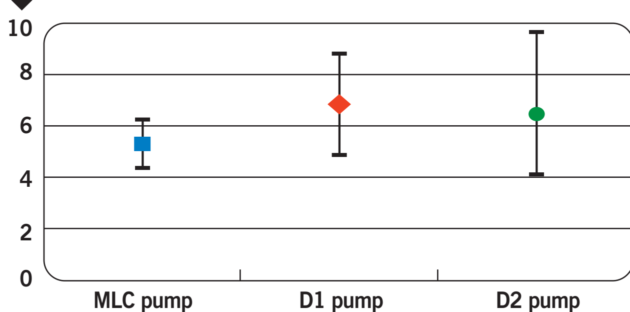

FIGURE 3. Etch rate uniformity for various pumps.

is continuous and smooth in the MLC pump, the spreading of etchant on the wafers is more uniform which results in a lower within-wafer uniformity. This suggests that the MLC pump is more suitable for wet etching processes in semiconductor industries. Among the diaphragms, the etch rate uniformity is higher for D1 pump because of its high frequency of pressure pulsations as previously mentioned.

In general, the etch uniformity strongly depends on position of the wafers in the etching bath. Hence, the change in the etch rate as a function of position of wafers in the bath for the three pumping methods is observed as shown in **Fig. 4.** For both MLC and D2 pumps, the etch rate is higher for the wafer positioned in the left side of the bath when compared to that of wafers in centre and right side. Since the feed is injected at left side of the bath

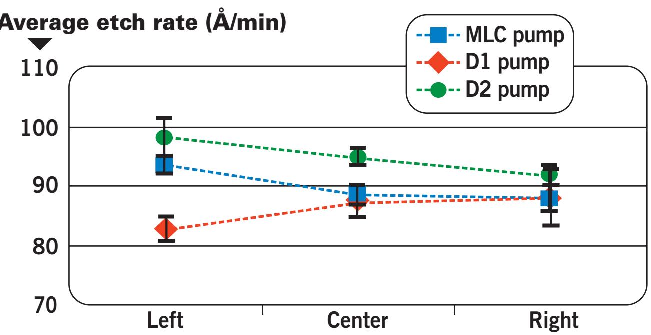

FIGURE 4. Etch rate for various pumps at bath position.

and the flow is from left to right side, the pressure would be higher at left side which may result in higher etch rate at left side of the bath. However in the D1 pump, the trend is opposite and the reason for this is not clear.

Wafer-to-wafer uniformity was also calculated and shown in **Fig. 5**. The value observed for MLC pump is 14% which is relatively low compared to that of 26% for D1 and 22.5% for D2 pumps. Thus, wafer-to-wafer uniformity is also strongly influenced by pressure variations in the pump. Since the pressure is constant with time due to the smooth flow, this does not affect the wafer-to-wafer uniformity. While in the case of other two pumps, the values are slightly higher as both the pumps exhibited larger pressure pulsations.

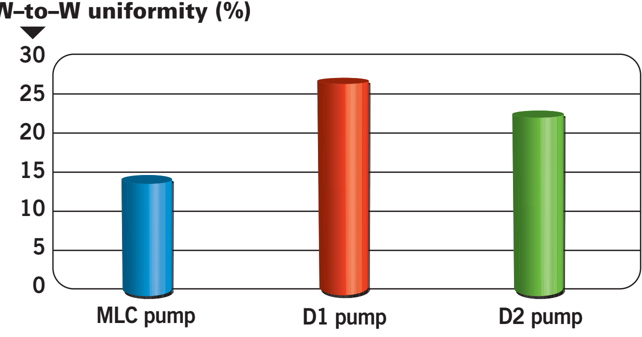

FIGURE 5. Wafer to wafer uniformity for various pumps.

Very low wafer to wafer uniformity values (<3-5% in conventional wet bath system) could be achieved in the semiconductor fab tool by ensuring laminar flow on each point of every wafer and by eliminating any eddies or dead zones using uniform flow control system and with careful tool design. However, within the limitations of our tool model, lower uniformity values could not be achieved.

Etching test in single wafer tool

The etch rate of PE-TEOS wafer in DHF solution for various pumping methods is shown in **Fig. 6**. The etch rate is 210 Å/min for the diaphragm pumps and, 215 Å/min and 212 Å/min for MLC pump when operated in normal mode and swing mode respectively. So the etch rate in single wafer tool is higher for the MLC pump unlike in conventional wet bath tool.

The etch rate uniformity is lower for the D2 pump among the three pumps when they were operated in normal mode, as shown in **Fig. 7**. This might be

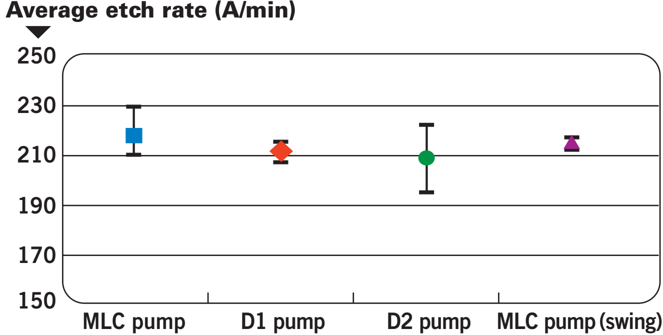

FIGURE 6. PE-TEOS etch rate in 1 wt% DHF for various pumps

because, in the D2 pump, the chemicals are spreading over a relatively large area of the wafer due to the high pulsation intensity (30±6 psi) compared to that of MLC (30 psi) and D1 pump (30±3 psi). In order to confirm

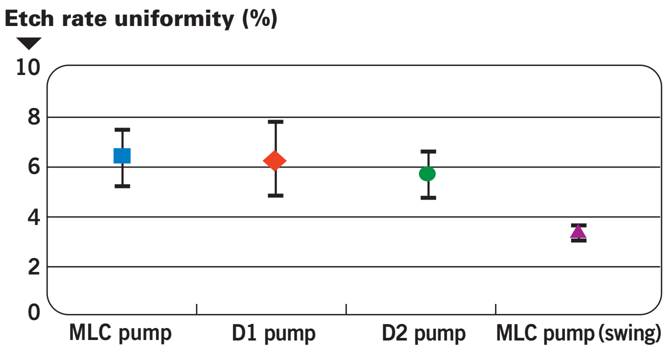

FIGURE 7. Etch rate uniformity for various pumps.

this, we operated the MLC pump in swing mode such that the chemicals were spread on same area of the wafer as in the D2 pump. As expected, MLC pump operated in a swing mode shows a much lower value because of the additional impact from non-fluctuating (non-pulsative) flow.

Fig. 8 shows the wafer-to-wafer uniformity for all

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LED PACKAGING

Low cost AlN substrate technology for HBLED and power semiconductors

JONATHAN HARRIS, *CMC Laboratories, Tempe, AZ*

A technology has been developed that allows AlN to be sintered at lower temperatures. This allows the material to be sintered and flat fired in a continuous furnace very similar to furnaces used for alumina.

Packaging requirements for high brightness LED (HBLED) technology is pushing the current material envelop for both low cost and high thermal performance. The desire to shrink package size is driving LED substrate requirements toward higher and higher heat dissipation. And the commercial imperative to decrease the $/Watt figure of merit for light output is putting cost pressure on the LED packaging technology to utilize lower cost substrate alternatives.

HBLED devices are bonded to a ceramic "tile" that consists of a ceramic substrate that has been metallized with thick-plated copper. Connection between the top surface with the active device and the backside, which is surface-mounted to a high thermal conductivity metal core printed circuit board, is accomplished with Cu-filled vias. Thus heat conduction from the active device occurs through both the Cu vias and the ceramic. The ceramic material provides electrical isolation between the different polarity inputs that drive the LED.

Traditionally, 96% Al_2O_3 has been used as the ceramic substrate in HBLED applications because of its low cost and good mechanical stability. However, with a thermal conductivity of only 20 W/m-K, alumina does not contribute significantly to heat transport in the tiles. This brings in the opportunity for using other ceramic materials with higher thermal performance such as AlN or Si_3N_4.

The downfall for both of these alternatives has been much higher cost than alumina.

Aluminum Nitride

Aluminum Nitride (AlN) is a polycrystalline, high melting temperature (refractory), ceramic material with an advantageous set of properties for die level packaging of high brightness LEDs and power semiconductors. These critical properties include:

- Good electrical insulation
- High thermal conductivity
- High flexural strength
- Stable up to very high temperature
- Able to be laser drilled, metallized, plated and brazed

A more detailed list of properties is shown in **Table 1** below.

TABLE 1.

Properties	Value	Comments
Thermal Conductivity	170 W/m-K	Laser Flash
Flexural Strength	325 MPa	Four Point Bend Test
Volume Resistivity	10^{14} Ohm-cm	Four Point Probe
Metallization Systems	Thin Film, DBC	

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As power densities of semiconductor devices increase, the need for packaging to remove generated heat increases, particularly for devices such as LEDs, which are sensitive to increasing temperature. AlN, which has a thermal conductivity that is 8-9 times higher than competitive materials such as Al_2O_3, becomes an excellent technical solution to increasing thermal demands on first level packaging materials.

Applications with high and increasing thermal demand include: RF power components for cellular infrastructure, HBLED, power semiconductors for motor control, packaging for highly concentrated photo-voltaic installations, and packaging for semiconductor lasers used in telecommunications.

AlN ceramic substrates are typically 15 to 60 mils thick, and up to 4.5" square (larger for some specialized applications). These substrates are fabricated using conventional ceramic processing technology. A typical fabrication sequence is given in **Table 2** below.

atmosphere. This means that binder removal, which is typically done through oxidation, must be done in a separate furnacing step (at a temperature well below the sintering temperature). A thick film continuous furnace can be used. For alumina, binder removal can be accomplished in the sintering furnace in one furnace step.

3. AlN is sintered in a batch furnace with much lower throughput than continuous furnaces used for alumina. In addition, these batch furnaces are constructed using Mo and W metal heat shields and heating elements because of the extremely high sintering temperatures (>1800°C), so the overall furnace cost is very high.
4. AlN can also be sintered in graphite batch furnaces. Though lower capital cost than W furnaces, the sintering fixtures for this type of furnace are very high cost and the throughput is still low due to batch processing. Also, the interaction of AlN with the

TABLE 2.

Fabrication Step	Processing Method	Equipment and Comments
Form a slurry with ceramic powder, sintering aids and organic binders	Slurry mixing and milling	Non-aqueous Solvents
Form a thin sheet	Tape casting	Non-aqueous tape caster
Cut out non-fired substrates	Blanking	Press that cuts tape
Press to a controlled density	Iso static lamination	Produces uniform density
Burn out the binder	Binder removal furnace	Continuous thick film furnace in air. Removes binder so only ceramic powder and sintering aids are left in sheet.
High temperature densification	Sinter at temperatures above 1800°C to full density	High Temperature, high cost, Tungsten or graphite batch furnace
Flatten dense substrates	Fire in stack with weight at high temperature (near 1800°C)	High Temperature, high cost, Tungsten or graphite batch furnace

As evident from the brief discussion above, AlN has a range of very beneficial properties for high thermal demand applications. However, there is one very key drawback of AlN which has limited its utilization. The key issue is the cost of AlN substrates relative to lower performance materials such as alumina. Typically, AlN costs 5-7 times more than alumina on a cost/square inch basis.

Below is a list of the key contributors to this higher cost structure:

1. Currently available AlN powder is approximately 20 times more expensive than alumina powder of comparable quality (purity, particle size).
2. AlN tape must be fired in a non-oxidizing

carbon containing atmosphere is a graphite furnace must be limited to produce high quality product.

5. The considerations of furnace cost and low throughput for sintering are also a factor for flat fire, so there is essentially a "double hit" for using batch processing.
6. Alumina can be processed in an aqueous environment. This makes the tape fabrication less expensive than the AlN process which must utilize non-aqueous solvents. This is a significant factor for tape casting.

The focus of this article will be to discuss a new technology that has been developed at CMC Laboratories, Inc. which addresses items 3, 4 and 5 in the list

above. This new technology allows AlN to be sintered at lower temperatures which allows the material to be sintered and flat fired in a continuous furnace very similar to furnaces used for alumina.

HBLED grade AlN

Table 3 below compares key properties for the low temperature sintered, lower cost "HBLED Grade" AlN compared to the standard, high temperature sintered, higher cost material that is currently commercially available.

It is clear from this graph that all of the properties are very similar, except that the thermal conductivity

TABLE 3.

Properties	Current AlN	HBLED Grade
Thermal Conductivity	170-190 W/m-K	110-130 W/m-K
Flexural Strength	325 MPa	300 - 325 MPa
Volume Resistivity	10^{14} Ohm-cm	10^{14} Ohm-cm
Metallization Systems	Thin Film, DBC	Thin Film, DBC

of the HBLED grade material is about 24% lower, but is still 6+ times higher than alumina. This makes the HBLED grade material suitable for all but the highest thermal demand applications for AlN.

HBLED grade AlN is made with the same basic processing steps outlined in Table 2 that are used for the high temperature material. The key difference is the sintering additives which allow the material to densify at 1675-1690°C as compared to the conventional 1820-1835°C. Tape binder formulations, tape casting conditions and the binder burn out process are also the same as, or very similar, to conventional material.

Fig. 1 shows a picture of a 4.5" x 4.5" x 20 mils substrate made from HBLED grade material that was fired at 1690°C in a nitrogen gas atmosphere with a hold time at sintering temperature of 3 hours.

Sintering aids for AlN ceramics perform two key functions: (1) they form a liquid phase at the sintering temperature which increases the rate of densification ("Liquid Phase Sintering" process); and (2) they getter oxygen from the AlN grains during sintering. Since the oxygen content of the AlN grains controls AlN's thermal conductivity, effective oxygen gettering is key to achieving the highest possible thermal performance.

The sintering temperature must be high for two reasons for the. First, the temperature must be high enough to melt the additive phase to form a liquid which enhances the rate of sintering by orders or magnitude. Second, the temperature must be high enough so that oxygen can diffuse out of the AlN grains during sintering to enhance the thermal conductivity of the AlN ceramic.

There is a third critical requirement for the additive phase during AlN sintering. While a liquid, the Y-Al-O phase will completely surround each AlN grain. If we define a wetting angle between the AlN and Y-Al-O measured at the 3 grain junctions, the microstructure has a very low wetting angle that is less than 60°. This type of microstructure is shown in the SEM micrograph in **Fig. 2a**. The dark grains in this figure, which are about 10 microns large, are the AlN. The bright phase is the Y-Al-O.

There are two critical performance issues with a wetted microstructure. First, because AlN fracture is inter-granular, the presence of a Y-Al-O phase between the grains lowers the tensile strength of the ceramic by a large factor. The second problem is that a wetted microstructure results in Y-Al-O covering large portions of the surface of the substrate. This reduces the consistency of AlN metallization processes.

So a key requirement for the oxide second phase during AlN sintering is that the oxide phase de-wet the ceramic

FIGURE 1. Low temperature sintered AlN substrate.

grains during the later stages of the sintering process so that the final microstructure will have a de-wetted Y-Al-O phase as shown in the micrograph in **Fig. 2b.**

- These same basic considerations for sintering of high temperature, conventional AlN are relevant to designing a low temperature sintering process:
- The sintering additive must melt at the sintering temperature to facilitate liquid phase sintering kinetics.
- The temperature must be high enough for oxygen to diffuse out of the AlN grains during sintering. This consideration puts somewhat of a lower limit on how low AlN can be sintered to produce high thermal conductivity.
- The liquid phase must de-wet from the AlN grains after densification to form a de-wetted microstructure and thus high flexural strength.
- This de-wetting is also required to produce ceramic with high electrical resistivity

Fig. 3 shows the microstructure of a low temperature formulation that was fired at 1675C. This has a modified sintering additive package which will melt at much lower temperature than the conventional Y-Al-O additives, but still has a strong chemical driving force to getter oxygen from the AlN grains.

As in the previous micrographs, the dark grey areas are the AlN ceramic grains, about 3-5 microns in size, and the bright areas are the oxide sintering additive phase.

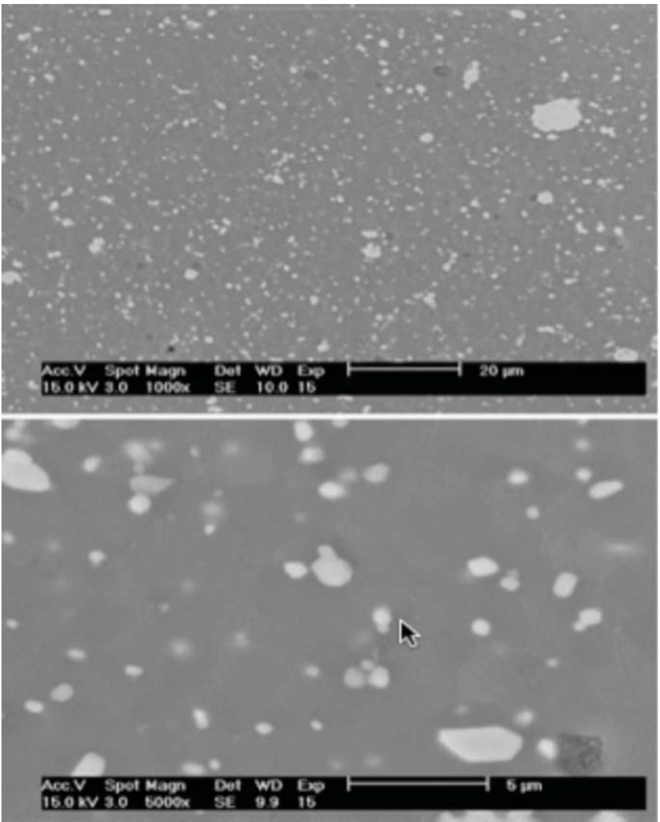
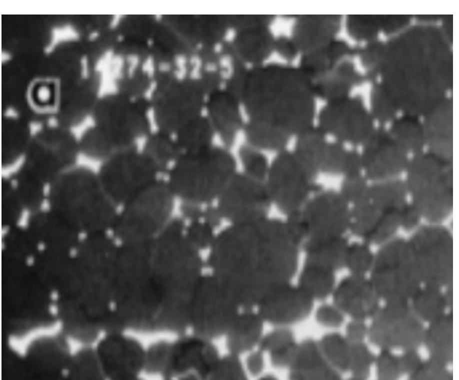


FIGURE 3. Microstructure of AlN, sintered at 1675°C.

Furnacing considerations

The motivation for developing an AlN formulation that sinters below 1700°C is the new furnace options that this lower temperature opens up. At 1700°C or below, a continuous tunnel kiln can be utilized. This furnace runs in a N_2 atmosphere with a small amount of H_2 present to protect the heating elements from oxidation. The heat shields are constructed of alumina and the heaters are made from Mo. The substrates are stacked on alumina plates which are continuously pushed through the furnace. The rate of travel depends on the length of the hot zone and, the required time at sintering temperature (about 3-5 hours). Thus the longer the hot zone, the faster the speed through the furnace and the higher the sinter through-put. Since a continuous furnace runs in steady state, there is no time required for the furnace to heat up and cool down. The heat up and cool down cycles are the key rate limitations in a batch furnace.



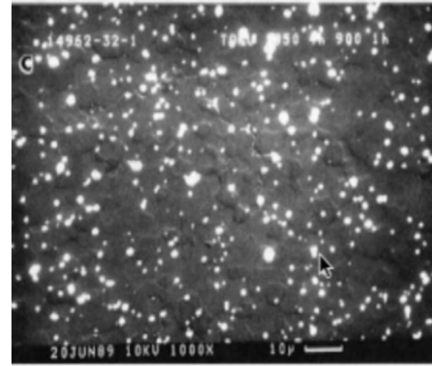


FIGURE 2A. Wetted microstructure- high temperature AlN
FIGURE 2B. De-wetted microstructure- high temperature AlN

Conclusion

The five major cost factors for AlN substrates (compared to Al_2O_3) were discussed: (1) higher cost powder; (2) separate BBO cycle; (3) batch sintering cycle; (4) batch flat fire cycle and (5) non-aqueous processing. By adopting a low temperature sintering configuration, cost factors 4 and 5 are addressed bringing the sintering and flat-firing operations in line with the process for alumina.

Of course, this process will only be appropriate for applications where a thermal conductivity of 130 W/m-K is acceptable. This thermal conductivity should be acceptable for most HBLED, RF and power semiconductor applications. For laser diode telecommunications applications, 130 W/m-K will most likely be too low and conventional higher cost AlN will continue to be utilized.

The availability of a low temperature, continuous sintering process also provides strong motivation for the next phase of cost reduction for AlN, utilization of lower cost, lower performance AlN powder. Again, with a focus on HBLED and power semiconductor applications, sensitivity to impurities such as Fe and Si, which drive up AlN powder costs, may not be anywhere as stringent as applications such as RF and microwave (where dielectric properties at high frequencies are important). The combination of lower cost powder and a continuous sintering process would move AlN substrate pricing much more in line with alumina. ◆

ETCH

Continued fromn page 17

on. During the "on" phase, sufficiently high ion energy is provided to achieve directional etching in bursts that are less likely to cause damage. During the "bias-off" phase, the source power produces reactants that re-saturate the surface (increase $S \bullet J_R$). In this way, bias pulsing rapidly alternates between directional etching and surface saturation to deliver high-precision etching **(Fig. 4d)**.

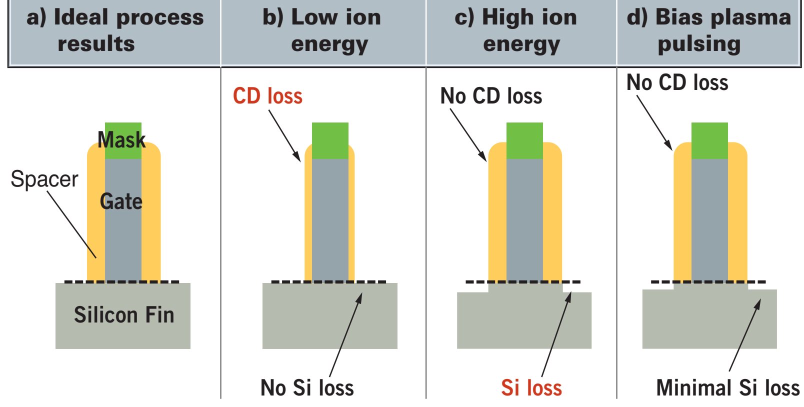


FIGURE 4. Comparison of different approaches for FinFET spacer etch. Bias plasma pulsing offers a viable approach for minimizing Si loss while maintaining directionality to prevent CD loss.

Conclusion

High-precision etching is more important than ever, and new etch techniques may be needed to achieve the requirements of 3D transistor architectures. While there is still work to be done, bias pulsing offers a viable approach to achieve directional etching with minimal structural damage that will be needed for manufacturing FinFET devices. ◆

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Acknowledgments:

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The move to 450mm: Europe's perspective

The European Equipment and Materials 450mm Initiative (EEMI450) provides Europe's perspective on the transition to 450mm wafers

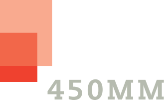
In 2009 the European Semiconductor Equipment and Materials industry decided to form a 450mm dedicated initiative, called EEMI450, to bring the interested parties together, to promote common 450mm efforts and to induce common 450mm European projects. Currently, this Initiative has more than 45 members, and to date, four 450mm European research projects have been labeled through the European ENIAC and CATRENE funding instruments.

The EEMI450 Initiative has written a white paper which defines the goals of the EEMI450 Initiative and in which the economical motivation concerning the 450mmm wafer transition for the semiconductor industry is explained. The white paper emphasizes the importance of early engagement in 450mm research and development activities for the European semiconductor related equipment and materials industry, which plays a significant role in the global semiconductor marketplace. In February, the white paper was delivered to Neelie Kroes, Vice-President of the European Commission and Commissioner for the Digital Agenda. The following is an excerpt from that white paper. The entire white paper can be found online at www.eemi450.net/White_paper_EEMI450_Final.

From left to right: Bernie Capraro, EU Research Programme Manager, Intel Ireland (co-author of the EEMI450 White Paper); Neelie Kroes, Commissioner for the Digital Agenda and Vice-President of the European Commission; Rob Hartman, Director Strategic Technology Program, ASML (member of the EEMI450 initiative); Bas van Nooten, Director European Cooperative Programs, ASM International (chairman of the EEMI450 initiative); and Heinz Kundert, President, SEMI Europe.

The semiconductor manufacturing industry has undergone dramatic growth during the second half of the last century, and throughout the first decade of the new millennium. A primary driver of that growth is the realization of "Moore's Law", whereby the number of transistors in an integrated circuit doubles approximately every 2 years with an associated increase in circuit functionality, reduction in operational power, and a reduction in unit cost. This, in turn, leads to an increased market demand for consumer products containing silicon integrated circuits, such as personal computers, mobile phones, and other electronic devices.

As an economic consequence, the silicon wafers used in the manufacturing processes to produce the silicon chips have undergone a diameter increase approximately every 10 years to improve throughput and reduce manufacturing costs. Silicon wafers that have been used in high volume manufacturing



processes range from 1-inch diameter, to the current state-of-the-art diameter of 300mm (11.8- inch, usually referred to as 12-inch). During this wafer size evolution, the ever increasing complexity of the supply chain of semiconductors has, and continues to demand, an increasing involvement from materials suppliers and equipment manufacturers.

Tier 1 initiatives

The next silicon wafer size is destined to be 450mm (18-inch), and activities are currently underway amongst the Tier 1 Semiconductor Manufacturing Companies, Intel, Samsung, TSMC and others, to prepare for manufacturing using this next wafer size in the second half of the current decade. In order for this to happen, a plethora of technological breakthroughs are required from the Equipment and Materials organizations, beyond a simple scale-up and extension of current technologies. This represents a global challenge as these organizations operate in all regions of the World. The European Equipment and Materials organizations therefore have a key role to play in this activity. By taking this initiative to be involved in this next wafer size transition, they will have the opportunity to establish share of the 450mm equipment and materials market.

Why the transition to the next generation wafer size? There is one fundamental and compelling question to be answered at each of the semiconductor manufacturing industry's wafer transitions; from the very early 2-inch diameter and less generations of the 1950's and 60's, through the 3-inch and 4-inch of the 1970's, the 5-inch and 6-inch of the 80's, the 200mm (8-inch) of the 90's, the 300mm (12-inch) of the 2000's, and now the 450mm (18-inch) generation expected in the second half of this decade and second century of semiconductor manufacturing. That question is: Why is a 50%-diameter increase in semiconductor processing platform needed about every decade?

As with the previous wafer size transitions, the move to 450mm is largely driven by the productivity, environmental, and economic challenges of the semiconductor industry as it continues to evolve. In particular:

- The number of semiconductor manufacturing fabrication facility ("fab") construction projects must be sustainable based on both its manufacturing complexity and environmental impact;
- The productivity and thus the economic feasibility of semiconductor manufacturing costs must be preserved [normalized for analysis purposes as cost per square centimeter ($cost/cm^2$)] in the face of continuous and exponentially increasing manufacturing facilities, equipment and materials costs. These costs are driven by the technology investments required to meet customer expectations for the doubling of functionality and performance approximately every 2 years, as defined by Moore's Law.

If we look at the data governing the volume of silicon shipped during the history of the semiconductor industry (based upon the SEMI® silicon shipment history), we can see that, historically, the baseline demand compound annual growth rate (CAGR) is a constant 7.6% since 1993, and prior to that was 15%, with periodic cycles around 2inch, 4inch, 6inch and 8inch silicon wafers used in semiconductor manufacturing processes these core rates. These major business cycles have occurred with a 7 to 8-year periodicity, with a minor "slowing" cycle in between the major cycle trough and peak.

Another factor affecting the growth rate of the industry is the overall downward trend of the Average Selling Prices (ASPs), which in effect has turned what used to be luxury electronic devices into commodity goods for the general public.

At a CAGR of 7.6%, the amount of silicon shipped for all types of electronic products such as memory, microprocessors, and other specific logic devices would double in less than 10 years. This would therefore require new factory capacity to sustain such growth. In previous wafer size generations, this has led to the adoption of the next-generation wafer size in order to reduce the number of factories to be built and sustained. Therefore, at some point in the future along this demand curve, despite any future possible industry consolidation, it will become more economical for chip makers to build one 450mm factory rather than two 300mm factories.

When the cycle-based demand growth is applied to the ISMI Industry Economic Model in a scenario without the 450mm wafer generation, the number of 300mm equivalent 35K wafer starts per month (wspm)

fab capacity increments rises to above 500 fabs, for all wafer generations, by the middle of this decade, and to above 600 fabs into the next decade. Based on this model, the level of fab capacity in any one wafer generation would rise to a level unprecedented in history, and create untenable challenges for companies required to meet the anticipated customer demand associated with many different products. With further potential industry consolidation, and therefore new factory builds resting with fewer companies, these challenges become even more critical.

Even if the size of an individual company's actual site (versus normalized 35K wspm equivalent increments) grows to take advantage of scale, the pressures upon the company resources for personnel, training, and facility infrastructure will be challenging even under the 300mm-only scenario. In addition, the environmental impact of water usage, sewage effluent, and efficient materials and energy usage will be far greater on a per square centimeter basis, as demonstrated by the 300mm wafer generation's own history during the 200mm to 300mm transition from 2001 -2010.

Another consideration in the absence of 450mm manufacturing would be the number of incremental new 300mm fab additions required to support the growing semiconductor market. This would be greater than the number of 450mm facility builds required, and hence could increase the number of annual build projects above the historic steady and sustainable level.

A 450mm roadmap

Looking from a cost perspective, historically, the cumulative cost per transistor benefit, weighted across all product types (with memory functionality most heavily weighted) resulted in a compound reduction of cost per function of -29% per year. This reduction was a combination of doubling the functionality in a square centimeter every two years (as per "Moore's Law") and keeping the cost of manufacturing for that square centimeter approximately flat. The benefit of a new wafer size generation's productivity has been estimated in the past by "resetting" by a 30% cost reduction every 10 years the ~3-4% /year exponentially increasing costs due to technology cycle upgrades and insertions, e.g., copper interconnects replacing aluminum.

Although not necessarily desired, the ITRS has been anticipating a slowdown in the rate of the technology cycle from 2 years, to 3 years, resulting in a slowing of the functional density in a square centimeter. In the absence of a 450mm productivity solution, the net slowdown effect upon the combination of the slower density and the higher cost per square centimeter results in only a -27% average cost/transistor reduction rate. This may appear to be a minor effect, but over the 2006 – 2024 timeframe, the slower rate produces a cumulative ~1 trillion dollar productivity difference impact without the 450mm wafer generation productivity gain. (In order to arrive at this statement, an in depth analysis should be performed per product type, taking in to account certain industry specific details e.g. EUV introduction, initial high cost of 450mm silicon and Flash cost growth due to 3D layer implementation.

The ability to extend Moore's Law into the future is dependent upon the development and production of new semiconductor manufacturing equipment. The operating costs associated with the silicon IC manufacturing Industry are heavily dominated by the cost of the equipment depreciation and maintenance. Therefore, by providing a new generation of processing equipment for 450mm silicon wafers, IDM, Foundry and OEM organizations are set to benefit in the future, and enable the sustained growth of the Industry.

There exists an outstanding benefit for European Equipment and Materials manufacturers to pool their efforts, to get support by Public Authorities at European and National level on their first steps into this required research and development. Thus, not only the 450mm technology will become a success story, but also the next generation of 300mm equipment and the More-Than-Moore fabs will have strong benefits, resulting presumably in safeguarded employment and in several thousands of new, high quality jobs across Europe. Perhaps to reduce risk, innovations on 300mm equipments and then scale up to 450mm may be a sometimes preferred route for both OEMs and IDMs, and subsequent process technology development on 300mm wafers, then scale up, a cheaper approach for IDMs to follow. The presence of an appropriate supply chain, and of customers of 450mm processed wafers, could be an invaluable attraction to maintain semiconductor production in Europe and to consider Europe for additional 450mm fabs. ◆

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NewProducts

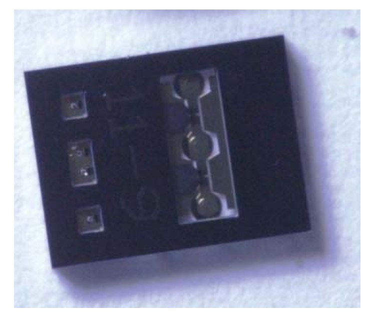
PECVD for displays

Applied Materials, Inc. announced new PECVD film technology to produce higher-performance, high-resolution displays for next-generation tablet computers and TVs. Available on the company's AKT-PECVD system, these advanced insulating films enable the use

of metal oxide-based transistors that produce smaller, faster-switching pixels to create higher resolution screens preferred by consumers. Applied's new PECVD films provide a dielectric-layer interface for metal oxide transistors that minimizes hydrogen impurities to improve transistor stability and deliver optimized screen performance. These high-quality silicon oxide (SiO_2) films can be deposited by the AKT-PECVD system with precise uniformity on sheets of glass up to $9m^2$ in size - a capability that is critical to achieving high production yields and low manufacturing costs. In addition to its new PECVD films, Applied is currently developing advanced PVD solutions, including IGZO deposition, for metal oxide manufacturing. **Applied Materials**, Santa Clara, CA, www.appliedmaterials.com.

MEMS relays for test

Advantest Corporation began producing micro electro mechanical system (MEMS) relays, designed for use in semiconductor testing equipment, high-speed communications devices, high-frequency wave measurement equipment and their components.



Mass production will begin in January 2013. Advantest manufactures the MEMS with its proprietary deposition technology, creating 1µm-thick piezoelectric film. This enables a smaller form factor and lower actuation voltage (12V) compared to high-frequency wave relays using electromagnetic or electrostatic actuation. The MEMS device is available in 5.4 x 4.2 x 0.9mm or 2.9 x 3.4 x 0.9mm form factors. The MEMS are not easily affected by ambient static electricity, like electrostatic relays. **Advantest**, Tokyo, Japan, www.advantest.com.

Wafering tool

Wafering tool supplier Silicon Genesis (SiGen) developed its second-generation production system for fabricating thin-silicon solar wafers, as well as high-brightness light-emitting diode (HB-LED), and 3D semiconductor packaging wafers. The system tailored for silicon, GaAs, germanium, SiC, GaN and sapphire materials. The new GenII PolyMax system targets high volumes, aiming to replace wire wafer saws with a kerf-free wafering tool. The system creates thinner wafers than are possible with wire-based slicing. The proton beam-induced wafering design was created over 6 years with numerous equipment and solar cell partners. **Silicon Genesis**, San Jose, CA, www.sigen.com.

Resist coat and develop platforms

SUSS MicroTec launched the RCD8 manual resist coat and develop platform for R&D and low-volume use in micro electro mechanical system (MEMS), semiconductor packaging, light-emitting diode (LED) and other applications. The RCD8 can convert from a spin coater, with the proprietary GYRSET closed cover coating technology, to

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a spray developer. The convertion takes minutes. Install options range from basic manual operation to semi-automated to puddle & spray developer. Processes developed on the manual RCD8 are easily transitioned to a SUSS MicroTec production tool. The RCD8 combines SUSS' multiple dedicated Delta Series tools that served specific applications in MEMS, advanced packaging, and LED fab or the R&D market. All necessary coating and developing processes for these applications are incorporated. **SUSS MicroTec**, Garching, Germany, www.suss.com.

High voltage system SourceMeter

The Model 2657A is optimized for high voltage applications such as testing power semiconductor devices, including diodes, FETs, and IGBTs, as well as characterizing newer materials such as gallium nitride (GaN), silicon carbide (SiC), and other compound semiconductor materials and devices. It is also useful for characterizing high speed transients and performing breakdown and leakage tests on a variety of electronic devices at up to 3,000V.

Like the rest of the Series 2600A family, the Model 2657A offers a highly flexible, four-quadrant voltage and current source/load coupled with precision voltage and current meters. **Keithley Instruments**, Cleveland, OH, www.keithley.com.

Gas and ancillary asset management system

The Lasso System is a customer centric supply chain and inventory management system capable of monitoring the location and operating status of gas products and other highly valued assets in real time. The system combines RFID and pressure monitoring technology designed for monitoring the inventory, movement and operating pressure of compressed gas cylinders. The Lasso operating software is optimized for reporting critical parameters of interest to users of compressed gases and has intelligence for generating gas cost and usage analytics to facilitate gas management decisions aimed at reducing aggregate gas costs. **Matheson**, Montgomeryville, PA, www.mathesongas.com.

Parametric test system upgrade

Supported by the latest version of Keithley Test Environment software (KTE V5.4), the S530 can now be configured for 48-pin full Kelvin switching and with new integrated options for pulse generation, frequency measurements, and low voltage measurements. These new capabilities allow S530 systems to address an even broader range of production parametric test applications with one high speed, cost-effective test solution. A new high speed, high resolution oscilloscope option supports ring oscillator testing over a broad frequency measurement range. **Keithley Instruments**, Cleveland, OH, www.keithley.com.

Test tools suit ASSP, RF test

ATE provider LTX-Credence Corporation released the Diamondx test platform for application-specific standard products (ASSP) and the DragonRF for radio frequency (RF) devices. In addition, LTX-Credence launched a SerDes test instrument and new testing software. The Diamondx tool increases tester throughput, offers better multi-site test capability, and has lower capital expenditure and operations costs than comprable tools, according to LTXC. The tool boasts a small footprint with an energy-efficient, air-cooled design. **LTX-Credence**, Norwood, MA, www.ltxc.com.

the three pumps. Like etch rate uniformity, the wafer-to-wafer uniformity is also higher for the D1 pump owing to the high frequency of pump pulsations. There is no significant difference between the D2 and MLC pumps. In short, the MLC pump operated in swing mode is preferred for single wafer etching process as it shows high etch rate with lower etch rate uniformity.

Conclusion

Etching experiments using three different pumps (a MLC pump and two diaphragm pumps, D1 and D2) were conducted. In a batch type bath, the etch rate is higher for the D2 pump, and lower for D1. For MLC pumps, the value is in-between. However within-wafer uniformity is higher for D1 pump followed by D2 and MLC pumps owing to the high frequency of pump pulsations. Both within wafer uniformity and wafer-to-wafer to uniformity are lower for MLC pump when compared to the other two pumps. This is mainly because of continuous and smooth flow exhibited by the MLC pump. In a single wafer tool, the etch rate is higher for MLC pumps when compared to diaphragm pumps. Also, the etch rate uniformity is lower for MLC pumps when operated in a swing mode. Thus, the lower etch rate uniformity could be achieved with MLC pump both in conventional wet bath and single wafer tool without affecting the etch rate. ◆

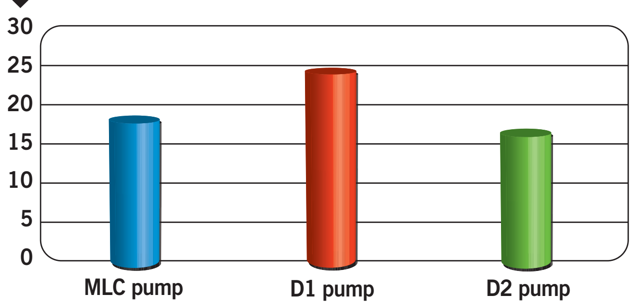

FIGURE 8. Wafer to wafer uniformity for various pumps.

Suggested additional reading

1. F.C. Chang, S. Tanawade and Rajiv Singh, Effects of stress-induced particle agglomeration on defectivity during CMP of low-K dielectrics, Journal of The Electrochemical Society, 156 (1), H39-H42, 2009.
2. R. P. Venkatesh, J-S. Lim and J-G. Park, Random yield loss during wafer cleaning, Solid State Technology, 54(4), 16-18 &23, 2011.

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Advanced packaging in the new decade

In the last decade, advanced packaging has emerged as an enabler of today's electronic products. The impact of packaging, assembly, and test is increasingly felt in the semiconductor industry and package selection is important to the success of the end product. The industry has seen a package evolution in the past 10 years and the road ahead may require a package revolution. Issues for future packaging include handling and assembly of devices with low-k and ultra low-k dielectrics, especially with Pb-free bumps and fine pitch bumps such as copper pillar. When the first low-k wafers were shipped from the foundry to assembly houses, the same assembly processes and materials were used. No one realized that stresses in the assembly process would cause delamination within the IC structure that would result in reliability problems causing devices to fail. Because no one gave much thought to the assembly process, companies missed revenue shipments. Assembly and packaging houses scrambled to study the problem and eventually made process changes and adopted new formulations of materials such as underfill and mold compounds.

Fast forward to today. There is a power struggle emerging between some foundry players and the IC package contract and assembly test houses on who will do the assembly of die on silicon interposers. The discussion focuses on who will bear responsibility for certifying reliability if the foundry builds the interposer and assembly of that interposer is done at the packaging house. This will be more interesting to watch than a Japanese Noh play, but maybe the moves won't be so subtle.

Not only is the assembly process important, but materials also play an increasingly critical role. Packaging and assembly of low-k and ultra low-k wafers has been an important topic of discussion at many recent conferences held by organizations such as IEEE CPMT and IMAPS. Presentations have discussed methods to minimize the potential for extreme low-k (ELK) delamination in flip chip packages with work focused on the design of the UBM structure, stress buffer layer materials, and types of substrates. Wire bond packages can also be impacted by the used of ELK materials in device fabrication and many companies are studying assembly and material requirements to solve potential issues.

> "The industry has seen a package evolution in the past 10 years and the road ahead may require a package revolution."

Assembly of integrated circuits fabricated at the next silicon technology nodes will require changes in materials or new formulations of materials to handle the stresses of the future devices. Trends in 3D packaging indicate that new developments in materials and processes are likely to be required. Reliability concerns may change the type of bumps used, the underfill materials, substrate materials and construction.

The semiconductor packaging materials business also counts for an increasing amount of the revenue associated with the industry. The recent *Global Semiconductor Packaging Materials Outlook* published by SEMI and TechSearch International indicates that the market for semiconductor packaging materials was more than $22 billion in 2011 and is expected to grow to almost $26 billion by 2015. This includes organic substrates, leadframes, bonding wire, mold compounds, underfill materials, liquid encapsulants, die attach materials, solder balls, wafer level package dielectrics, and thermal interface materials.

Many IC makers have noticed that the cost of packaging devices is increasing rapidly, impacting margin and revenue. Choice of packaging solutions in the next decade will require careful cost/benefit analysis. Co-design of IC and package will no longer be a cute phase mentioned in PowerPoint slides, but a topic of serious discussion at any IC maker that plans to be successful in the next decade. ◆

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