EQUIPMENT • MATERIALS
PACKAGING • TEST
SEMICONDUCTORS • LED
PV • EMERGING MARKETS

The Power of [X]

New Programs for 2013

- Silicon Innovation Forum—Top strategic investors review an exciting line-up of new and emerging companies
- A conversation on semiconductor R&D with leaders from imec, SEMATECH and CEA-Leti
- 450 mm Wafer Processing: Opportunities and Prospects
- The latest requirements on nonplanar architectures, stacked 3D ICs, the two paths for lithography, nano defect detection, silicon photonics, printed/flexible electronics, MEMS, LEDs
- Keynote address: Ajit Manocha, CEO, GLOBALFOUNDRIES

Wafer Processing
Packaging
Test

[SEMICON West]

Photovoltaic
Silicon Photonics
MEMS—LEDs

REGISTER NOW and get ready to be a part of the biggest event in microelectronics manufacturing—SEMICON® West 2013!

- Access more than 50 hours of technical programs focused on the critical issues in microelectronics manufacturing
- 450 mm, 3D IC, next-generation lithography, test, contemporary packaging, advanced materials, and more
- Discover technologies, materials, and manufacturing solutions for LEDs, MEMS, plastic electronics, and other emerging and adjacent markets
- Connect with technical experts and find solutions that move your ideas from the lab to the fab

Connect to the Power of [X]—
Connect to the Power of SEMICON West

SEMICON® West2013

July 9–11

Moscone Center
San Francisco, California
www.semiconwest.org

SEMICON West is brought to you by:

ADVANTEST® APPLIED MATERIALS® KLA-Tencor Accelerating Yield semi™

SEMICONDUCTORS • PACKAGING • MEMS • LEDS • DISPLAYS

MAY 2013

Solid State TECHNOLOGY®

Insights for Electronics Manufacturing

Manufacturing Flexible Displays P. 13

www.solid-state.com

PennWell®

Welcome to the
Digital Edition of

Solid State TECHNOLOGY®

Insights for Electronics Manufacturing

Easily **NAVIGATE** through the issue.

SEARCH for specific articles or content.

View the table of **CONTENTS** and easily navigate directly to an article.

Click **PAGES** to view thumbnails of each page and browse through the entire issue.

Easily browse all **BACK ISSUES**.

SHARE an article or page via social media.

A quick start guide to MAXIMIZING our interactive features.

SHARE an article via email.

PRINT any or all pages.

Click directly on the page to **ZOOM** in or out. Fit the issue to your screen.

DOWNLOAD the issue to your desktop.

lid State
CHNOLOGY®
or Electronics Manufacturing

The ConFab®

Conference & Networking Event

June 23-26, 2013 | Encore at the Wynn, Las Vegas

REGISTER AT WWW.THECONFAB.COM/REGISTER BY MAY 17, 2013 & SAVE $300!
Enter code AD13

Presented by: Solid State TECHNOLOGY Insights for Electronics Manufacturing

The ConFab's 2013 conference "Filling Fabs of the Future," takes an executive-level look at significant challenges to sustained growth, including:

- Improving R&D Efficiency
- Why 2.5D and 3D Semiconductors are Changing Everything
- CMOS Scaling Beyond 10nm
- Inside Today's Chips: What Teardowns Reveal
- 3D Integration's Killer App
- Innovation, Specialization and Performance Drive Semiconductors
- The "New" IC Industry Cycle Model
- Embedded Die Packaging: The Next Step in 3D System-in-Package Miniaturization
- A Review of the Cost and Technology Needed to Implement Next Generation Device Technology
- And more!

KEYNOTE SPEAKERS

MONDAY, JUNE 24, 2013

Technologies and Business Strategies of the Future IT Industry

Mr. Yoon-Woo Lee
Executive Advisor
Samsung Electronics Co., Ltd.

TUESDAY, JUNE 25, 2013

Orthogonal Scaling to Fill Today's Fabs in the Future

Mr. Subu Iyer
IBM Fellow
IBM Systems & Technology Group

For a preview of the outstanding line-up of sessions and speakers at The ConFab 2013, please visit **http://www.theconfab.com/conference.**

REGISTER BY MAY 17TH AND SAVE $300! ENTER CODE AD13

CONNECT. COLLABORATE. CREATE.

Owned & Produced by: PennWell®

www.theconfab.com

Solid State TECHNOLOGY®

MAY 2013 VOL. 56 | NO. 3

FlexUP, developed at Taiwan's ITRI research center, can be applied to fabricate conformal AMOLED, AMEPD, OLED light, flexible touch, and sensor applications.

COVER

FEATURES

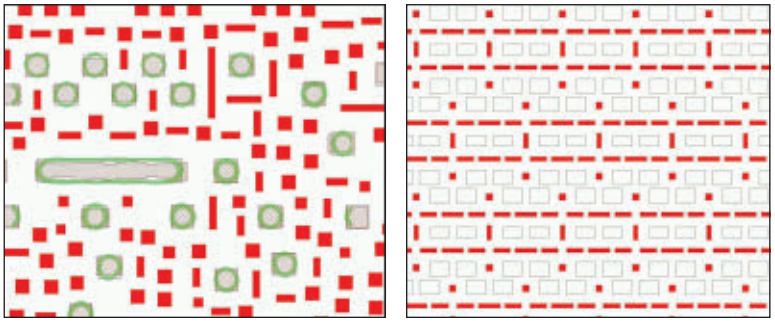
COLUMNS

DEPARTMENTS

Web Exclusives

The secrets of 14nm lithography

How is it possible to use 193nm wavelength light at 14nm? How can we provide the process window to pattern such tight pitches? Gandharv Bhatara, Mentor Graphics, shares how.
http://bit.ly/YGivJK



Random logic SRAM

MEMS New Product Development:

Critical design and process steps for successful prototypes

David DiPaola, managing director for DiPaola Consulting, reviews tolerance stacks, DFMEA, manufacturing assessment and process mapping. **http://bit.ly/10Lw76o**

How Samsung is climbing the charts

It's no secret that Samsung is up against Apple in many ways, in products, sales and innovation. However, even in the face of Apple's patent infringement lawsuits, Samsung is still climbing the charts. **http://bit.ly/13UAkto**

Dimensional scaling and the SRAM bit-cell

Zvi Or-Bach, President & CEO of MonolithIC 3D Inc. and Benjamin S. Louie of Zeno Semiconductor discuss dimensional scaling as it relates to EUV and future per transistor device cost.
http://bit.ly/162Mv4L

n&b news and blogs

Foundry Intel: Altera is the beginning... Is Apple next?

Altera and Intel entered into an agreement for the future manufacture of Altera FPGAs on Intel's 14nm tri-gate transistor technology. Dr. Phil Garrou believes this could signal the start of more intense competition between Intel and TSMC, who had previously been Altera's sole foundry.
http://bit.ly/ZtVcQ6

MEMS Executive Congress Europe in review

Karen Lightman, MEMS Industry Group, reflects on discussions and presentations from MEMS Executive Congress, held this year in Amsterdam.
http://bit.ly/XCelzf

EUVL Focus Blog

Bring me the rhinoceros

Dr. Vivek Bakshi shares technical highlights, new solutions and his favorite moments from 2013 SPIE Advanced Lithography EUVL Conference.
http://bit.ly/Z9V7ke

450mm in 2017: It's coming

The switch to 450mm will likely be the largest, most expensive retooling the semiconductor industry has ever experienced. 450mm fabs, which will give an unbeatable competitive advantage to the largest semiconductor manufacturers, are likely to cost $10 billion and come on-line in 2017, with production ramp in 2018.

Unprecedented technical challenges still need to be overcome, but work is well underway at an R&D center in upstate New York, at the Global 450mm Consortium, G450C. Paul Farrar Jr., the G450C General Manager, recently spoke on the current status of activities, key milestones and schedules during a webcast produced by Solid State Technology.

> For the next six or seven years, the industry will be developing and bringing capability to both 300mm and 450mm

"At this point, we have contracts with 12 major suppliers, and we have tools that are being delivered to the consortium starting in April and continuing through 2015," Farrar said.

The G450C team now has over 60 engineers and assignees from the member companies. The goal is to have more than 150 engineers by 2014, with approximately 60 supplier engineers on site. "2013 and early 2014 will be about getting tools installed and up and running. Then the integration and unit process scientists will continue from there," Farrar said.

Farrar said G450C has commitments for 112 process levels. For 45 processes, two suppliers are developing products (which equates to 90 process levels). A few have three suppliers, and about 10 process steps have one supplier. Farrar said that he sees 300mm and 450mm development continuing simultaneously. "We certainly know that for the next six or seven years, the industry will be developing and bringing capability to both 300mm and 450mm. A key goal here is to make sure that we do not slow down the scaling required for Moore's Law to go from say 20nm to 15 to 12 to 10, etc. versus the cost reduction you get from going to a larger wafer size. We need to both of these things simultaneously as an industry," he said. "A rough target is to get to 10nm, and then in 2016 we want to be ready for IC makers to make their decisions on when they will ramp to 450mm."

—Pete Singer, Editor-in-Chief

Solid State TECHNOLOGY®

Susan Smith, Group Publisher
Ph: 603-891-9447, susans@pennwell.com

Pete Singer, Editor-in-Chief
Ph: 603-891-9217, psinger@pennwell.com

Shannon Davis, Editor, Digital Media
Ph: 603-891-9145, shannond@pennwell.com

Robert C. Haavind, Editor-at-Large
Ph: 603-891-9453, bobh@pennwell.com

Phil Garrou, Contributing Editor

Michael Fury, Contributing Editor

Justine Beauregard, Marketing Manager

Cindy Chamberlin, Editorial Graphic Designer

Sheila Ward, Production Manager

Dan Rodd, Illustrator

Debbie Bouley, Audience Development

Marcella Hanson, Ad Traffic Manager

EDITORIAL OFFICES

PennWell Corporation,
Solid State Technology
98 Spit Brook Road LL-1,
Nashua, NH 03062-5737;
Tel: 603-891-0123; Fax: 603-891-0597;
www.ElectroIQ.com

PennWell

CORPORATE OFFICERS

1421 South Sheridan Rd., Tulsa, Ok 74112
Tel: 918-835-3161
Frank T. Lauinger, Chairman
Robert F. Biolchini, President and CEO
Mark Wilmoth, Chief Financial Officer

TECHNOLOGY GROUP

Christine A. Shaw, Senior Vice President and Publishing Director

For subscription inquiries:
Tel: (847) 559-7500; Fax: (847) 291-4816;
Customer Service e-mail: sst@omeda.com;
Subscribe: www.sst-subscribe.com

worldnews

EUROPE | **STMicroelectronics** began working with research partners to develop a pilot line for next-generation MEMS devices.

US | At its Fab 8 campus in Saratoga County, N.Y., **GLOBALFOUNDRIES** demonstrated its first functional 20nm silicon wafers with integrated Through-Silicon Vias (TSVs).

ASIA | **Gigaphoton, Inc.**, a lithography light source manufacturer, announced that as of April 2013, it has started business operations at the Gigaphoton Singapore Branch, its newly established branch in that country.

EUROPE | **Plessey** announced that samples of its Gallium Nitride (GaN) on silicon LED products, the world's first LEDs manufactured on 6-inch GaN on silicon substrates, are now available.

US | The **University of Central Florida** announced a new Bachelor of Science degree program in photonics science and engineering.

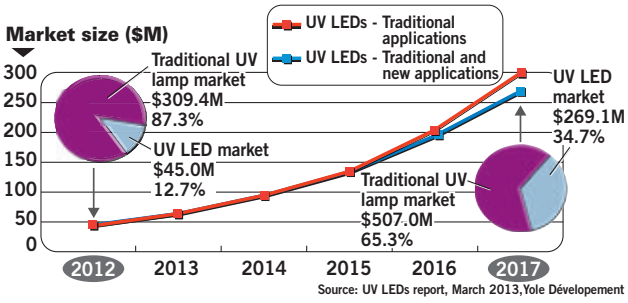
CANADA| **OneChip Photonics** revealed outsourcing plans, with announcements of newly-established relationships with semiconductor foundry **GCS** and wafer supplier **IQE**.

EUROPE | **AIXTRON SE** announced that it is participating as a key partner in the recently announced European Union Future Emerging Technology flagship project, "Graphene."

US | **Cadence Design Systems, Inc.** announced plans to aquire **Tensilica, Inc.** for approximately $380 million in cash.

The UV LED market is booming

Yole Développement announced its new report "UV LEDs: Technology & Application Trends" which presents UV LED new applications and associated market metrics for the period 2012-2020, and a deep analysis of UV LED technology and UV LED lighting industry.



Thanks to UV curing, UV LEDs should become a $270M business by 2017, and could hit $300M if new applications boom

Thanks to its compactness, low cost of ownership and environmentally-friendly composition, UV LED continues to replace incumbent technologies like mercury. Hence, the UV LED business is expected to grow from $45M in 2012 to nearly $270M by 2017, at a CAGR of 43% -- whereas the traditional UV lamps market will grow at a CAGR of 10% during the same time period.

In 2012, UVA/UVB applications represented 89% of the overall UV LED market. Amongst these applications, UV curing is the most dynamic and most important market, due to significant advantages offered over traditional technologies (lower cost of ownership, system miniaturization, etc.). This trend is reinforced by the whole supply chain, which is pushing for the technology's adoption: from UV LED module and system manufacturers to ink formulators and (of course) the associations created to promote the technology. And with Heraeus Noblelight's recent acquisition of Fusion UV (Jan. 2013), all major UV curing system manufacturers are now involved in the UV LED technology transition.

Concerning UVC applications, they are still in their infancy and their sales are mainly for R&D purposes and analytic instruments like spectrophotometers. But given some newly published results (increase of EQE over 10%, etc.) and the recent commercialization of the world's first UVC LED-based disinfection system (2012), the market should kick into gear within the next two years.

In addition to traditional applications (UV lamps replacement), and due to their unique properties (compactness, higher lifetime, robustness, etc.), UV LEDs are also creating new applications that aren't accessible to traditional

UV lamps, i.e. apps that are miniaturized and portable.

"In 2012, several new UV LED based products were launched, including cell phone disinfection systems, nail gel curing systems and miniaturized counterfeit money detectors - and this is likely to continue!" explains announced Pars Mukish, Technology & Market Analyst, LED, at Yole Développement. "We estimate that if new UV LED applications continue emerging, the associated business could represent nearly $30M by 2017, which would increase the overall UV LED market size to nearly $300M," he adds.

Supply chain battle to intensify

The booming UVA/UVB market (mostly UV curing) has attracted several new players from different backgrounds over the past few years: traditional UV lamp suppliers, traditional UV system suppliers, pure UV LED system suppliers, and others. Each player employs a different strategy for capturing the maximum value created by this disruptive technology: horizontal integration (from UV lamp to UV LED), vertical integration (from UV LED device to UV LED system and vice-versa) or both (from UV lamp to UV LED system). We should point out that traditional UV lamp manufacturers are under the most pressure since they have to compensate for the waning lamp replacement market by diversifying their activities in higher supply chain levels.

In the end, every UV LED device/system manufacturer faces the same technical issues when it comes to integrating UV LEDs into a system (thermal management, optics, etc.), but experience is gained with each passing year. Once UVC LEDs achieve sufficient performance, there's no way a manufacturer will allow the opportunity to pass them by. ◆

A single European semiconductor strategy is on its way

At the International Semiconductor Strategy Symposium (ISS Europe), the European semiconductor industry affirmed its ability to innovate. More than 170 top industry representatives agreed on a number of joint steps and strategic measures to strengthen their competitiveness and sustainability. The controversial question whether the best way to attack future challenges will be "More Moore" or "More than Moore," ended in an expected compromise, namely that the industry should pursuit both strategies concurrently, the participants of a panel expressed. While the More than Moore sector is traditionally strong in Europe, going on with More Moore is important for two to three device makers in Europe and in particular for the European equipment suppliers which export 80% of their products.

In a global scale, the semiconductor industry is approaching the move to 450mm wafer processing technology – a step that promises to greatly boost the productivity of semiconductor manufacturers. However, since the investment to build a 450mm fab easily exceeds the $10 billion mark, this move is regarded as risky and, for this reason, reserved to only the very largest enterprises. In the past, this perspective divided the European industry into two camps - the "More Moore" group that advocates taking on the 450mm challenge, and the "More than Moore" group which shunned this risky investment and preferred to rely on application-oriented differentiation instead.

At the event SEMI Europe, an industry association embracing enterprises that represent the entire value chain and organizer of the ISS Europe, set up a high-ranking panel discussion on options and choices of a single European semiconductor strategy. The panel proved that entrepreneurial spirit is well alive among Europe's chipmakers, technology suppliers and researchers.

The panel participants recognized that the European semiconductor industry possesses the necessary expertise. So far, the willingness to jointly face these challenges has been affected adversely by the macroeconomic environment and the Euro crisis, which discouraged far-reaching strategic decisions. The members of the European Commission that recently signalized understanding the needs of the semiconductor industry's vital role for the high-tech location Europe, certainly contributed to the optimism in the industry.

"We have all the knowledge, the materials and the equipment," said Rob Hartman, Director Strategic Program for leading equipment manufacturer ASML, during the panel. "Let's do it in the EU."

European Commissioner Neelie Kroes' idea of creating an "Airbus for chips," a European initiative for the semiconductor industry comparable to the initiative that once led to the launch of the Airbus in the aviation industry, was strongly hailed by the panel.

"An Airbus for chips could be a very powerful tool," Van der hove said. "It does not need to be a single company, it also can be a framework of companies," added Laurent Malier, CEO of French research centre CEA-LETI.

The main concern of the industry is the slow decision process of the European institutions due to a complex political approval process inside of the European Union, the participants agreed. This industry is moving fast and so the decisions have to be taken fast, too. The strong Euro and the lack of qualified labor are further regarded as potential stumbling blocks for the technological progress and the business competitiveness.

Intel leads unexpectedly large decline in semiconductor market inventory

After reaching a worrisome high in the third quarter of 2012, global semiconductor inventories held by chip suppliers fell at a surprisingly fast rate in the fourth quarter, led by dramatic reductions for market leader Intel Corp.

Days of Inventory (DOI) for semiconductor suppliers in the fourth quarter declined by 5% compared to the third quarter—higher than the 1.5% initially forecast, according to an IHS iSuppli Supply Chain Inventory Market Brief from information and analytics provider IHS. Meanwhile, inventory value in dollar terms fell almost 5%—larger than the originally projected 3%.

"Semiconductor companies reduced their inventories at a faster-than-expected rate in the fourth quarter as they moved to adjust to weakening demand," said Sharon Stiefel, analyst for semiconductor market intelligence at IHS. "Many chip suppliers demonstrated great agility in their reactions to the drop in demand. No. 1 semiconductor supplier Intel Corp. was the most aggressive, cutting its stockpiles by more than half a billion dollars—the largest decrease on a dollar basis of any chipmaker."

Cutting inventories down to size

Among semiconductor suppliers that reduced their inventory levels between the third and fourth quarters last year, the percentage of decrease ranged from 5% to 25%, resulting in chip stockpile value of $60 million to nearly $600 million being shaved off in the companies affected. And while inventory climbed in some companies during the same period, the spread was smaller, with the value of the increase worth slightly north of $40 million to approximately $250 million.

Memory suppliers were excluded from DOI and inventory value calculations because they report results much later than any other group in the semiconductor supply chain.

The rest of the companies covered effectively straddle the breadth of the semiconductor chain, including those engaged in the wireless, automotive, data processing and industrial segments.

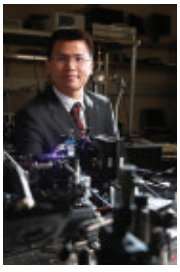
Intel leads inventory liquidation

The largest decrease in inventory value during the fourth quarter belonged to Intel, down $585 million from the third quarter, representing an 11% reduction. The company made aggressive moves to cut stockpiles. It also reduced production as it migrated to a new process technology: 14-nanometer lithography.

AMD and STMicroelectronics also experienced large inventory declines of $182 million and $131 million, respectively, or 25% and 9%.

Continued on page 9

Student develops brighter, smarter and more efficient LEDs



Rensselaer Polytechnic Institute student Ming Ma has developed a new method to manufacture light-emitting diodes (LEDs) that are brighter, more energy efficient, and have superior technical properties than those on the market today. His patent-pending invention holds the promise of hastening the global adoption of LEDs and reducing the overall cost and environmental impact of illuminating our homes and businesses.

For this innovation, Ma, a doctoral student in the Department of Materials Science and Engineering, has been named the winner of the prestigious 2013 $30,000 Lemelson-Rensselaer Student Prize. He is among the three 2013 $30,000 Lemelson-MIT Collegiate Student Prize winners announced today.

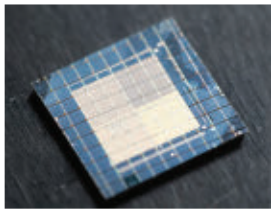
"For more than 175 years, Rensselaer has produced some of the world's most successful engineers and scientists, explorers and scholars, innovators and entrepreneurs. Doctoral student Ming Ma, with his groundbreaking invention of GRIN LEDs, honors and continues this tradition of excellence," said David Rosowsky, dean of the School of Engineering at Rensselaer. "Rensselaer and the School of Engineering offer a hearty congratulations to Ming for his achievement. We also applaud all of the winners, finalists, and entrants of the Lemelson-MIT Collegiate Student Prize for using their talent and passion to engineer a better world and a better tomorrow."

Ma is the seventh recipient of the Lemelson-Rensselaer Student Prize. First given in 2007, the prize is awarded annually to a Rensselaer senior or graduate student who has created or improved a product or process, applied a technology in a new way, redesigned a system, or demonstrated remarkable inventiveness in other ways.

"Invention is critical to the U.S. economy. It is imperative we instill a passion for invention in today's youth, while rewarding those who are inspiring role models," said Joshua Schuler, executive director of the Lemelson-MIT Program. "This year's Lemelson-MIT Collegiate Student Prize winners and finalists from the Massachusetts Institute of Technology, Rensselaer Polytechnic Institute, and the University of Illinois at Urbana-Champaign prove that inventions and inventive ideas have the power to impact countless individuals and entire industries for the better."

Seeking Brighter, Smarter LEDs

Conventional incandescent and fluorescent light sources are increasingly being replaced by more energy-efficient, longer-lived, and environmentally friendlier LEDs, but LEDs still suffer from challenges related to brightness, efficiency, and performance With his project, "Graded-refractive-index (GRIN) Structures for Brighter and Smarter Light-Emitting Diodes," Ma faced these problems head-on and tackled a fundamental, well-known technical shortcoming of LED materials.



LEDs are hampered by low light-extraction efficiency—or the percentage of produced light that actually escapes from the LED chip. Currently, most unprocessed LEDs have a light-extraction efficiency of only 25%, which means 75% of light produced gets trapped within the device itself.

One solution that has emerged is to roughen the surface of LEDs, in order to create nanoscale gaps and valleys that enable more light to escape. While surface roughening leads to brighter and more efficient light emission, the roughening process creates random features on the LED's surface that do not allow for a complete control over other critical device properties such as surface structure and refractive index.

Freeing Trapped Light with GRIN LEDs

Ma's solution to this problem was to create an LED with well-structured features on the surface

Intel *Continued from page 7*

In the case of AMD, inventory shrank for its microprocessors as a result of an amended wafer supply agreement with GLOBALFOUNDRIES for reduced stockpiles. For its part, STMicroelectronics cut utilization rates after exiting its money-losing joint venture with Ericsson.

Two other chip suppliers had notable inventory drawdowns: Texas Instruments, down $91 million or 5%, due to weak end-market demand for its chips; and ON Semiconductor, down $63 million or 10%, as it burned bridge inventory and coped with reduced revenue.

Among inventory gainers, most faulted low seasonality and an uncertain global economy for a rise in chip stockpiles. Companies in this group included MediaTek, up $58 million or 14%; NXP Semiconductors, up $44 million or 7%; and Infineon Technologies, up $43 million or 6%.

Qualcomm bucks the trend

The one exception among gainers that could boast of a strong performance that was linked to an increase in chip inventory levels was Qualcomm, up $247 million or 24%. Given the strong market acceptance of its wireless chips in products like the Apple iPhone and iPad, Qualcomm is ramping up production and inventories in order to meet demand.

Semiconductor suppliers will be positioning their inventories in the first quarter this year to prepare for anticipated demand. Inventories are expected to rise in response to slightly positive global economic indicators as well as favorable semiconductor and end-equipment forecasts—unless major swings occur once more from the larger suppliers that could then end up skewing the industry.

Student *Continued from page 8*

to minimize the amount of light that gets reflected back into the device, and thus boost the amount of light emitted. He invented a process for creating LEDs with many tiny star-shaped pillars on the surface. Each pillar is made up of five nanolayers specifically engineered to help "carry" the light out of the LED material and into the surrounding air.

Ma's patent-pending technology, called GRIN (graded-refractive-index) LEDs, has demonstrated a light-extraction efficiency of 70%, meaning 70% of light escaped and only 30% was left trapped inside the device—a huge improvement over the 25% light-extraction efficiency of most of today's unprocessed LEDs. In addition, GRIN LEDs also have controllable emission patterns, and enable a more uniform illumination than today's LEDs.

Overall, Ma's innovation could lead to entirely new methods for manufacturing LEDs with increased light output, greater efficiency, and more controllable properties than both surface-roughened LEDs and the LEDs currently available in the marketplace.

New MFCs mean higher yield

In what might be a case of the cobbler's children finally getting new shoes, new algorithms and control technology – powered by advanced semiconductors, of course — are enabling "intelligent" real-time flow error detection in mass flow controllers (MFCs).

Pete Singer,
Editor-in-Chief

The accuracy and repeatability of MFCs — which control the amount of process gas flowing into etch and deposition chambers, for example — can have a very direct impact on yield: "A simple 1% increase in yield on an etch system can equate to up to $60,000 a day savings," notes Shaun Pewsey, Director of Microelectronics Strategic Accounts at Brooks Instrument. "Process gas stability has been identified by virtually every IDM as critical to meeting yield enhancement goals and initiatives. MFC accuracy is critical in maintaining the level of control required," he said (the remarks were made during a recent webcast produced by Solid State Technology).

Pewsey said the challenges are only getting more severe as the industry moves to ever more challenging devices, larger die sizes, and greater die complexity. Compounding the problem is the push for a higher mix of products in the fabs, particularly foundries. "We're seeing tools that are being run with multiple recipe types, in some cases pushing the tool beyond its original design requirements," Pewsey said.

Semiconductors

The end result of this is a stronger focus on basic MFC performance attributes. Today, 1% accuracy is required for challenging applications and Pewsey believes we will soon see a requirement for 0.5% accuracy. Tighter flow repeatability is also required for chamber matching.

It's well known that the accuracy of MFCs can drift over time, in part due to the build-up of particles from process gas. The common practice for checking the accuracy of MFCs is to take the gas panel off-line and perform a flow check. This can easily take half a day, says Pewsey. And, of course, until this check is done, the drifting MFCs could have impacted hundreds of wafers.

To address this common problem, engineers at Brooks Instrument have developed the smarter MFC. The latest version, the GF135, uses Brooks' real-time rate-of-decay flow error detection technology to continually test for changes in the device's performance. Data can be used to improve accuracy at critical low-flow set points, set up alarm limits for critical performance parameters and monitor trends for predictive maintenance.

How does the new smart MFC work? In operation – while process gas is flowing into the chamber – Brooks figured out a way to momentarily close the valve in order to run a diagnostic test. "As the valve closes, we continue to deliver the required amount of gas to the process chamber as the internal pressure starts to decrease. As that happens, our control valve opens up, continuing to deliver the exact amount of flow required for the process," Pewsey explained.

After completing the measurement, the valve is reopened and the pressure transient compensation algorithm compensates for the initial pressure spike. A proprietary algorithm computes the flow based on the rate of pressure change and time and compares this against the baseline.

In short, the new technology identifies and corrects issues before they happen, preventing wasted time and wasted wafers, increasing uptime and yield. ◆

Rapid Defect Identification with Layout-Aware Diagnosis

MARTIN KEIM, *Technical Marketing Engineer, Mentor Graphics*

Scan logic diagnosis is a powerful tool to help failure analysis engineers determine the root cause of a failing die. Product and yield engineers, on the other hand, are interested in using diagnosis result to identify the defects that best represent systematic yield limiters. To be of value for both engineers, a diagnosis tool needs to be

- Accurate,
- With high resolution and
- Meaningful defect classifications

Significant improvements have been made in scan logic diagnosis algorithms. Through layout-aware diagnosis Tessent® Diagnosis improvements all three items, becoming a powerful tool in the hands of the failure analysis and yield engineer. Layout information enables Tessent Diagnosis to improve accuracy and resolution by 70% to 85% depending on the defect type and allows layout-validated defect types. More meaningful reporting for example on the polygon level prepares the diagnosis results for direct use by engineers.

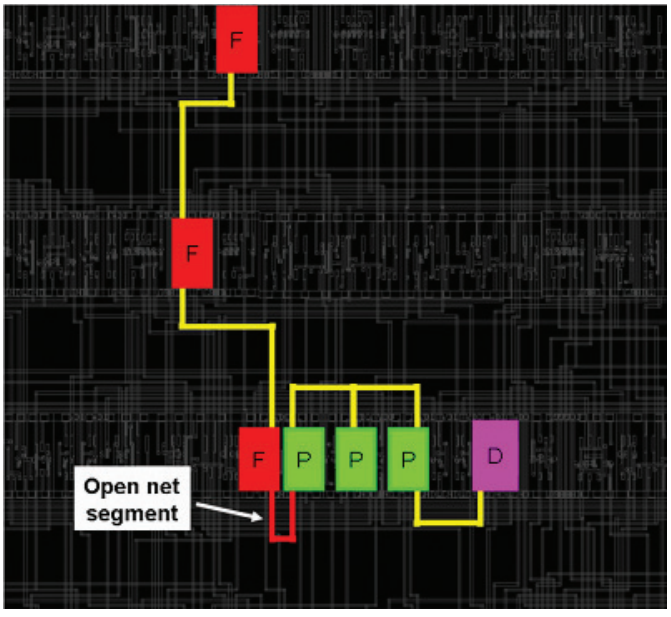


FIGURE 1: Net identified in diagnosis

Mentor Graphics,
Silicon Test and Yield Analysis
www.mentor.com/products/silicon-yield/
1-800-547-3000

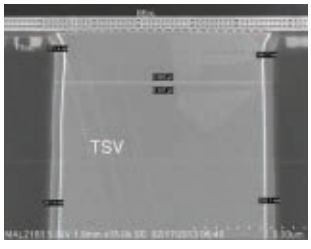
DOWNLOAD THE COMPLETE TECHNICAL PAPER NOW!

GlobalFoundries 2.5 / 3D at 20nm

Dr. Phil Garrou, contributing editor

A year ago, GlobalFoundries (GF) CTO Bartlett announced the installation of TSV production tools for the company's 20nm technology platform and announced that "the first full flow silicon with TSVs was expected to start running at Fab 8 (Saratoga, NY) in Q3 2012 with mass production expected in 2014 and the 2.5D line (their 65 nm Fab 7 line in Singapore) had a similar time schedule as the 3D line in the United States."

In early April, GlobalFoundries announced its first functional 20nm silicon wafers with integrated through-silicon vias (TSVs). At its Fab 8 facility in N.Y., the silicon foundry vendor manufactured TSV test wafers using their 20nm-LPM process technology, and at Fab 7 in Singapore, the company demonstrated a 65nm 32mm x 26mm interposer test vehicle for 2.5D chips. Both 2.5D and 3D are set for a 20nm introduction, full qualification by next year and non-early adopter production in 2015.



GLOBALFOUNDRIES utilizes a "via-middle" approach to TSV integration, inserting the TSVs into the silicon after the wafers have completed the Front End of the Line (FEOL) flow and prior to starting the Back End of the Line (BEOL) process. This approach avoids the high temperatures of the FEOL manufacturing process, allowing the use of copper as the TSV fill material.

They are using a 6 x 60 µm vias middle, copper TSV as shown in the figure below. Interposer size is limited by reticle size (i.e., 25-30 mm).

Dave McCann, VP of packaging technology at GlobalFoundries, reports that GF is taping out a 3D design for an undisclosed customer and is working with two others on 2.5D. "2.5D is already here," he added. Several 2.5D test structures were shown that were collaborations with Amkor.

While foundries TSMC and Samsung are both offering turnkey solutions, GlobalFoundries and UMC are supporting a partnering ecosystem where they will handle the traditional front-end steps and the "via creation" process and then will hand off the traditional backend steps such as temporary bonding/debonding, grinding, assembly and test to traditional packaging houses such as ASE, Amkor SCP and SPIL.

A year ago, GF announced hopes of shipping 28 and 20nm 3D chip stacks in 2014. Now, GF states only the 20nm chips will be used in stacks and they may not ship in volume till 2015.

Hybrid Memory Cube Consortium

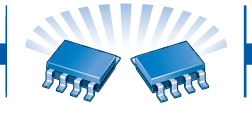
In related news, consider the current status of the Hybrid Memory Cube (HMC). ARM, HP, and SK Hynix joined former members including Micron, Samsung, Altera, IBM, Microsoft, AMD, Fujitsu, ST Micro, Marvell and Xilinx in June 2012.

The group has recently issued version 1.0 of its specification for a vertical memory stack with a defined logic-layer interface. The group is reportedly changing focus to higher-speed variations of a DRAM stacked using TSV technology. They want to increase data rate across modules from the current 10 - 15 Gb/sec up to 28 Gb/sec.

Micron said it will deliver engineering samples of 2 and 4 Gb versions of the stack by this summer with commercial production scheduled for late 2013 or early 2014.

High-speed networking vendors will probably be the first to commercialize with HPC-centric applications next in line. Initial HMC implementations will be DRAM, but multi-memory stacks that employ NAND flash and DRAM are expected to follow.

Packaging



Manufacturing flexible displays: The challenges of handling plastic

NICK COLANERI, *Flexible Display Center, Arizona State University, Phoenix, AZ*

The first flexible high-resolution displays will be produced using materials handling techniques that have been developed to allow the use of existing thin transistor fabrication facilities.

After more than a decade of development, the release of the first commercial products containing flexible displays is expected later this year. The companies that have made product release announcements have been relatively quiet about technical details, but it is likely that the mechanical flexibility of these products will be limited. Most of the effort to date has been focused on issues related to producing flexible display panels, with relatively less attention given to the mechanical vulnerability of interconnects and the other components of the systems incorporating these displays. Still, the arrival of the first products will be an important milestone along the path to truly flexible electronics.

The fabrication of flexible displays presents two key challenges. First, a glass substrate underlies all flat panel displays, and conventional display glass is both rigid and frangible. A number of flexible alternatives have now been investigated. Second, all high-resolution displays use an array of thin film transistor circuits to supply voltages or currents to modulate the appearance of the individual pixels. These thin film devices are produced using vacuum deposition and photolithographic patterning techniques that exploit the flatness and high-temperature tolerance of the glass substrate. To shorten development time it is desirable to use this existing infrastructure, so alternative substrates should closely mimic these features of glass.

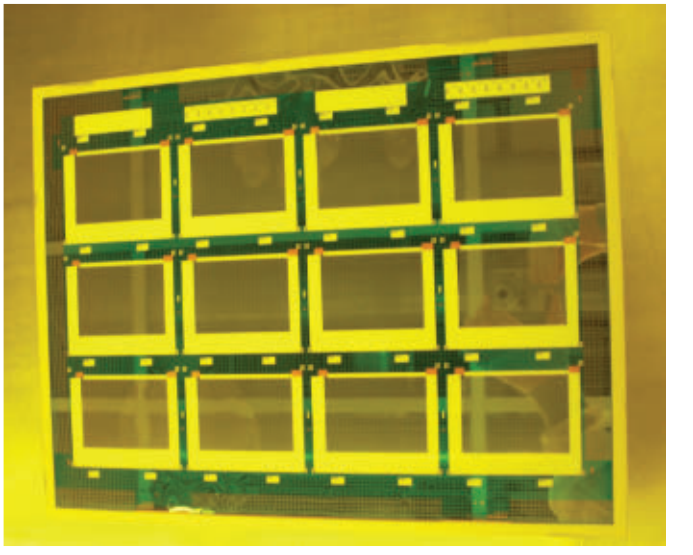


FIGURE 1. 370mmx470mm carrier panel with bonded PEN substrate, following fabrication of twelve 320x240 thin film transistor circuits using IGZO as the active semiconductor.

The principal substrate alternatives investigated over the last decade have been metal foils and polymer films. Recently, Corning and other glass manufacturers have also developed flexible glasses that are suitable for use in displays. In the last year, many companies have established the capability to produce these materials in rolls resembling polymer film, but this is a recent development. The most advanced prototypes shown at recent trade shows, such as FPD International in Yokohama or the Consumer Electronics Show in Las

NICK COLANERI *is the director of the Flexible Display Center, Arizona State University, Phoenix, AZ*

Vegas, have all relied on polymer substrates.

In order to process polymer films through conventional thin film transistor lines, it is necessary to develop methods for handling them. It is also necessary to modify certain process steps to avoid exceeding their temperature limits. Thus far, two different approaches have been developed for handling the films. Both essentially bond the material to a rigid carrier panel and then release the film after transistor fabrication. More exotic approaches involving "roll-to-roll" handling of the substrate are also frequently discussed, but layer-to-layer registration with a conventional deposition and patterning process remains a formidable challenge when the film is handled in this way.

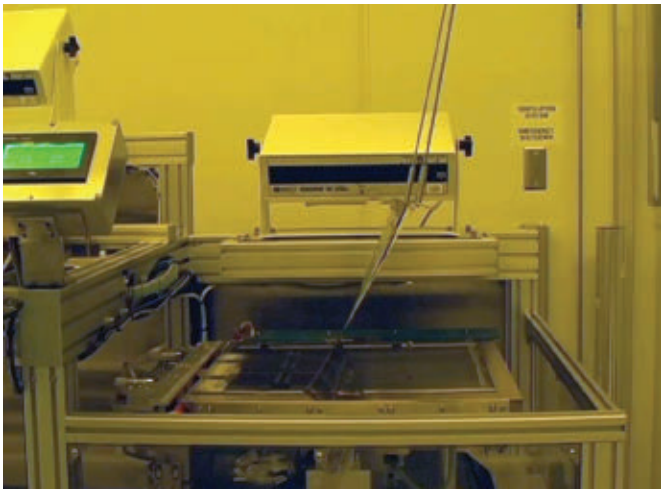


FIGURE 2. Experimental tool debonding a PEN substrate from a carrier panel after fabrication of thin film transistor circuits. The tool is applying between 0.1 and 0.2N of force.

The first approach to immobilizing a polymer film, pioneered at Philips Electronics over a decade ago, involves the coating of a thin layer of the polymer onto a rigid carrier from a solvent. Most of the groups practicing this technique are using a polyimide. The polyimide layer is sufficiently thin (typically only a few tens of microns) so that it will mechanically mimic the properties of the carrier, which is usually ordinary display glass. The thermal expansion or contraction of the thin polymer layer is constrained by the carrier, so the only limitation on process temperatures is the degradation that will begin to occur somewhat above 250°C (depending on the specific chemical composition of the polyimide). After transistor arrays have been fabricated on the free surface of the polymer, it is released by rastering a laser across the back side through the carrier. The laser, which generates a wavelength corresponding to a strong absorption band of the polymer, ablates a very thin layer where it is in contact with carrier, thereby releasing it.

The laser release process is intrinsically slow and generates debris that must be managed, but this process has been successfully employed by a number of groups. Other challenges are associated with the mechanical stresses that accumulate in the stack of materials comprising the transistor array during the fabrication process. This can lead to delamination of the transistors, either during the release or when the display is subjected to a mechanical shock. In addition, because the polymer substrate is so thin, it is not self-supporting. If it is simply released from the carrier, the stresses in the transistor layers will cause it to curl up into a tube with a curvature radius of several millimeters. The post-process must therefore be carefully designed to accommodate this fact.

Despite these challenges, a number of groups have sufficiently mitigated them to produce impressive prototypes using this handling process. E-Ink holdings, for example, have shown 9 in. diagonal electrophoretic display prototypes with a resolution of about 150dpi that are made on a pilot production line which uses this process. The electrophoretic laminate is stiff enough to overcome the tendency of the backplane substrate to curl, and the entire structure is about as flexible as a credit card.

The Flexible Display Center at Arizona State University has developed a second approach to flexible substrate handling in which a polymer film is bonded to a rigid carrier using an engineered adhesive. As in the technique discussed above, this composite substrate is then processed in conventional thin film transistor fabrication tools, after which the polymer film is released using a simple mechanical process. In the remainder of this article some of the details of this process will be described.

The substrate handling process has been done with a wide variety of flexible materials, including stainless steel foil, polyimides, and thin glass. The most extensive experience, however, is with Teonex® PEN

film from Dupont-Teijin Films, a heat-stabilized high-temperature polyester. It has been expressly designed for optical applications, and exhibits excellent transparency and dimensional stability during processing. The film used has 125µm thickness, although other thicknesses are available. The details of the transistor fabrication process must be varied depending on this thickness, as it has an impact on the evolution of film stresses during the process.

The PEN (or other) film is bonded to a carrier made of a high temperature ceramic which is stiffer than display glass and has a coefficient of thermal expansion much closer to that of the polymer. Panels are routinely processed with this material which are provided at Gen II size, i.e. 370mmx470mm (**FIGURE 1**). The carriers are fired after use to clean them and are then re-used.

The temporary adhesive has to meet a number of requirements. It must not induce unacceptable variation in the thickness of the composite substrate comprising the carrier, adhesive, and flexible substrate. It also must not out-gas any volatile organic compounds (VOCs). It must endure temperature transitions up to the limits of the deposition, and maintain bond integrity during exposure to high vacuum as well as wet and dry etch environments. Most importantly, once the transistors are fabricated, it must release without adversely impacting transistor performance. An experimental tool debonding a PEN substrate from a carrier panel is shown in **FIGURE 2.** An IGZO thin film transistor array fabricated using the bond-debond substrate handling protocol is shown in **FIGURE 3**.

After screening hundreds of adhesives across a broad range of chemistries, the experts at Flexible Display Center turned to a team now at Henkel Electronic Materials to engineer a solution. Their proprietary high molecular weight adhesive meets all of the requirements outlined above. It also has the additional advantage that it adheres preferentially to the carrier plate rather than the polymer film during the release process. This eliminates the need for a post-fabrication clean step.

The composite system consisting of the carrier plate together with the adhesive layer and bonded polymer film exhibits complex dimensional changes during the process of transistor array fabrication. Temperature ramp rates and deposition rates must be carefully managed to control stress accumulation and minimize

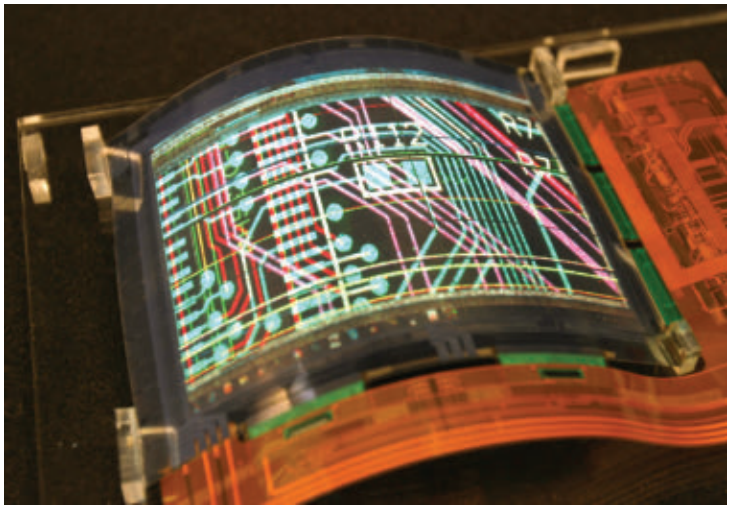


FIGURE 3. Full color active-matrix OLED display fabricated on an IGZO thin film transistor array fabricated using the bond-debond substrate handling protocol.

film distortion during these steps. To monitor these changes, a suite of metrology tools has been developed. An Azores Gen II photolithographic stepper fitted with distortion compensation software in its optical system enables the identification of pattern mismatches arising from dimensional change during a given process step. It is also important to measure out of plane "bowing" due to stress mismatches between the polymer film and the carrier plate. If this exceeds tolerances it will cause photolithography errors and produce handling errors by the robots in the process equipment.

This substrate handling protocol has been used to produce Gen II panels with multiple display transistor circuit arrays employing either amorphous silicon or indium-gallium-zinc-oxide (IGZO) as the active semiconductor. In both cases the highest nominal process temperature is about 180 °C. Despite the lower process temperatures, the amorphous silicon transistors exhibit operating characteristics that are indistinguishable from those in conventional glass-based displays, apart from the well-known drift in threshold voltage when they are used in current-drive mode. These have proven completely adequate for use in displays employing voltage-driven electro-optic effects, such as electrophoretic displays. The IGZO transistors are more suitable for current-driven displays such as OLEDs. Devices made with the low-temperature process exhibit about a 25-fold

Continued on page 32

Analysis of TSV proximity effects in planar MOSFETs and FinFETs

RICARDO BORGES, VICTOR MOROZ *and* **XIAOPENG XU,** *Synopsys, Mountain View, CA.*

The impact of TSV-induced stresses on transistor performance are simulated, and a "keep-out-zone" is identified.

Over the last several years, the semiconductor industry has made significant strides in demonstrating the technical feasibility of 3D-IC integration in several different configurations, each with its own challenges and potential benefits. For example, memory cubes comprised of stacks of NAND FLASH or DRAM memory die, connected internally with through-silicon vias (TSVs), have already been manufactured by several companies. Memory cubes reduce the form factor of the memory product and improve performance because of shorter electrical interconnections. In another configuration, silicon interposer technology, also known as 2.5D-IC, mitigates a number of challenges that arise in die-stacked 3D-IC, while offering the advantage of shorter inter-die connections relative to traditional 2D packaging. The silicon interposer approach is expected to evolve into more complex and higher value implementations by moving the I/Os and the global power and ground mesh onto the interposer. However, silicon interposer technology does not offer the full benefits of form factor reduction and electrical performance advantages envisaged with die-stacked 3D-ICs, which provides the motivation for the industry to continue the research and development needed to overcome the technical and commercial barriers toward the commercialization of die-stacked 3D-ICs.

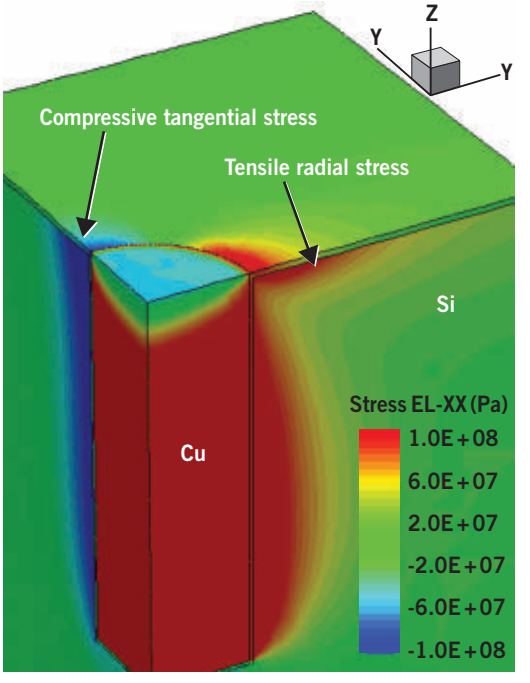


FIGURE 1. Stress map for the Sxx stress component around the copper TSV.

From the point of view of process development and transistor performance, the fabrication and integration of the TSVs within a 3D-IC system presents a number of challenges. These challenges, though manageable, need to be taken into account. Copper is the material of choice for the via conductor, due to its excellent electrical conductivity and pervasiveness in modern interconnect stacks. However, copper and silicon have very different coefficients of thermal expansion. Since the TSV fabrication steps involve thermal operations, the thermal mismatch of these materials induces stresses in the silicon surrounding the TSV. These stresses in turn alter the carrier mobility and on-current of the transistors fabricated in the

RICARDO BORGES *is senior Product Marketing Manager, TCAD group at Synopsys;* **XIAOPENG XU** *is R&D Manager, Silicon Engineering Group at Synopsys; and* **VICTOR MOROZ** *is a Synopsys Scientist. www.synopsys.com.*

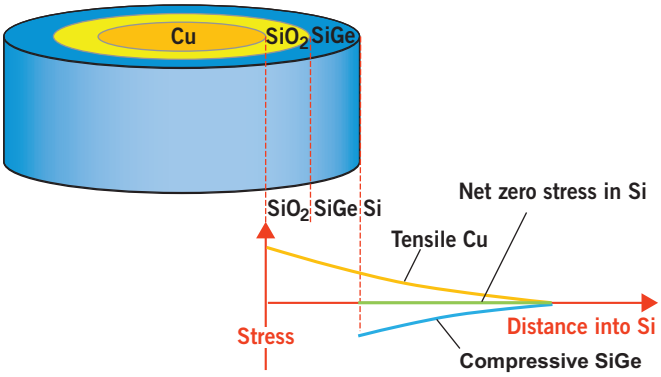


FIGURE 2. Canceling tensile TSV stress by a thin epitaxial compressive SiGe layer.

proximity of the TSV, through the same piezoelectric effect in silicon which is responsible for boosting the transistor performance in strained-silicon technologies. This so-called TSV stress proximity effect has a range of several microns and can either produce enhancement or degradation of the current. In addition to the TSVs, the micro bumps used for inter-die connections and the solder bumps, used to attach the die stack to the bumps, also induce stresses in their proximity. Besides their impact on transistor performance, these induced stresses lead to structural reliability concerns such as cracking and delamination.

The impact of the TSV-induced stress on transistor performance is amenable to simulation with Technology CAD (TCAD) tools such as Synopsys' Sentaurus Interconnect. The data generated from Sentaurus Interconnect can then be used to identify the keep-out-zone (KOZ) surrounding the TSV. Typically the KOZ for an analog function is larger than the KOZ for a digital, with the distinction being a function of the variation tolerance for the transistor performance [1].

FIGURE 1 illustrates propagation of the TSV-induced stress into the surrounding wafer. Due to the large size of the TSV, 5μm in diameter and 20μm in depth, the stress propagates into silicon for distances of about 20μm. Considering linear drive current (Idlin) variability tolerance of 5% for digital circuits, the TSV-induced KOZ is 8μm.

Such a large KOZ means that a large part of the chip area is wasted, as it can not contain any transistors. For analog circuits, where the Idlin variation tolerance reduces to 0.5%, the KOZ is about 20μm, which further increases the wasted chip area.

One way to dramatically reduce the KOZ is to cancel tensile copper stress with a similarly sized compressive stress source. Taking into consideration that a thin epitaxial layer of SiGe can generate a sizable compressive stress and the maturity of SiGe epitaxy in the industry, a thin epitaxial SiGe layer that is grown

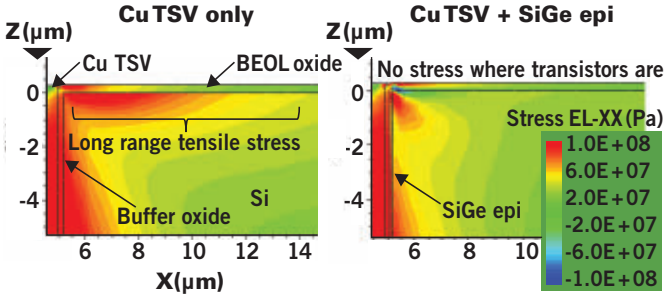


FIGURE 3. Comparing tensile TSV-induced stress in a conventional TSV (left) with the structure that contains compressive SiGe epi layer (right).

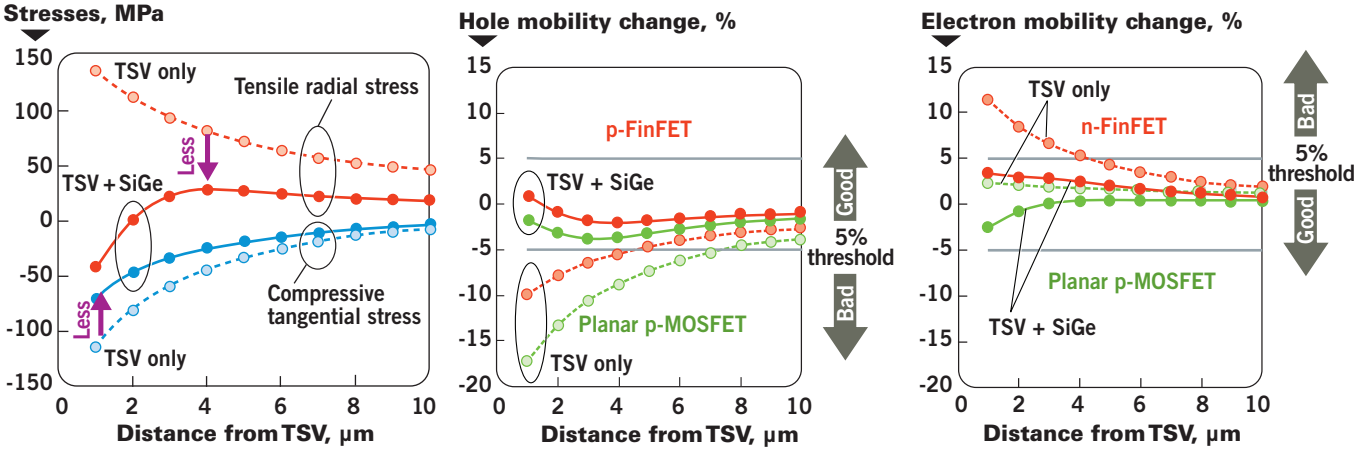


FIGURE 4. Distribution of the radial and tangential stress components along the Si surface vs distance from TSV. **FIGURE 5.** TSV-induced hole mobility change versus distance to TSV for the planar p-MOSFET (green) and for the p-FinFET (purple). TSV-only case is shown by the dashed lines, and the TSV+SiGe case is shown by solid lines. **FIGURE 6.** TSV-induced electron mobility change vs distance to TSV for the planar n-MOSFET (green) and for the n-FinFET (purple). TSV-only case is shown by the dashed lines, and the TSV+SiGe case is shown by solid lines.

inside the TSV hole before depositing the buffer oxide and the copper TSV, can provide the desirable large stress source with a small layout footprint. **FIGURE 2** illustrates this idea.

Introduction of the SiGe layer dramatically reduces stress on the surface of Si wafer as can be seen on **FIGURE 3**.

Quantitatively, the tensile radial and the compressive tangential stress components along the Si surface for the two TSV process options are compared on **Figure 4**. The tangential stress is reduced to some extent, and the radial stress is reduced significantly.

The stresses are converted into the TSV-induced mobility change, which is the dominant factor for the stress-induced Idlin variation. The conversion is performed using a sophisticated sub-band model rather than a simple linear piezo model. **Figure 5** depicts hole mobility distributions for the planar p-MOSFET and p-FinFET.

For the TSV-only case, the KOZ is 8µm for the p-MOSFET, reducing to 5µm for the p-FinFET. In contrast, for the TSV+SiGe case, the KOZ is zero for both the planar p-MOSFET and the p-FinFET.

Similarly, **FIGURE 6** shows what happens to the n-channel transistors. The planar n-MOSFET has zero KOZ, whereas the n-FinFET has 5µm KOZ.

Therefore, for the planar technology only the p-type transistor has a relatively large KOZ of 8µm. For the FinFET technology both transistor types have similar KOZs of 5µm. Similarly to the p-type transistor behavior, introduction of the SiGe epi layer eliminates the KOZ for both transistor types.

The impact of the TSV-induced stress on structural reliability can also be analyzed with Sentaurus Interconnect. The data from such analysis is used to evaluate material and structure design options. The results shown in **FIGURE** 7 identify interfacial shear stress as the crack driving force. The crack energy release rate is evaluated using a method known as J integral. The crack energy release rate is compared in **FIGURE 8** with the safety factor, which measures the difference between the material cohesive strength and the calculated J-integral. Although interface cracks between metal and oxide insulator show ~30%

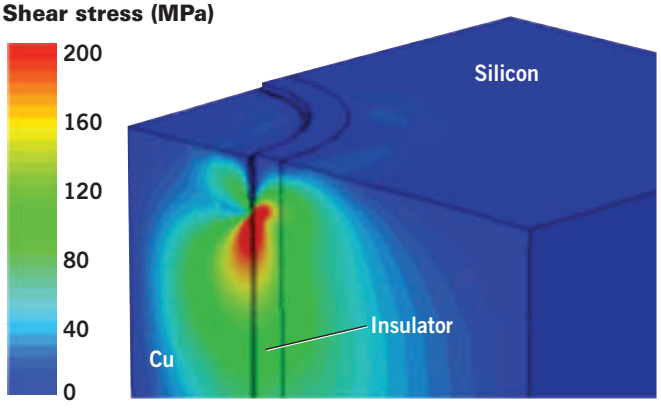


FIGURE 7. Shear stress evolution with TSV process steps.

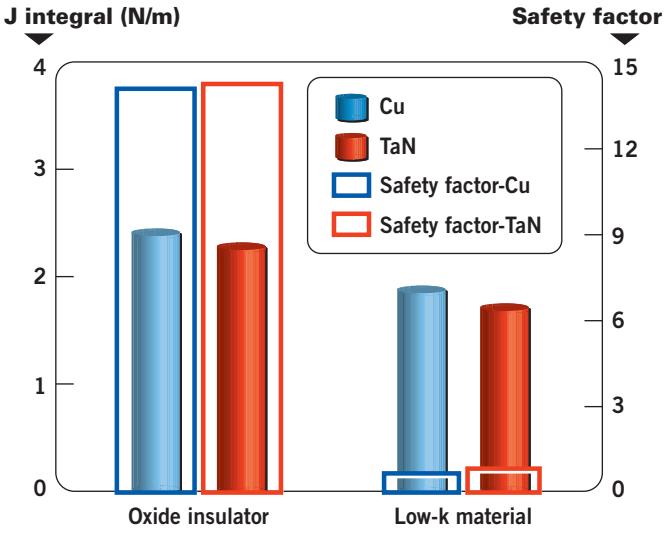


FIGURE 8. J-integral and safety factor for the crack with different insulators/barrier layers.

higher J-integral, the interfaces with oxide insulator possess larger safety factors than the interface with low-k insulator. The larger safety factor corresponds to stronger interfacial adhesion and strength. This analysis illustrates the greater adhesion and better reliability for metal/oxide interface as compared to the metal/low-k interface. For both insulation materials, TaN metal barrier shows slightly reduced J-integral as compared to a barrier with Cu-like material properties, thus improved interfacial reliability. These simulation findings are consistent with recent measurements [2].

The above stress data is obtained using process simulation techniques which capture the stress evolution during TSV fabrication. **FIGURE 9** illustrates the evolution of the normal stress component

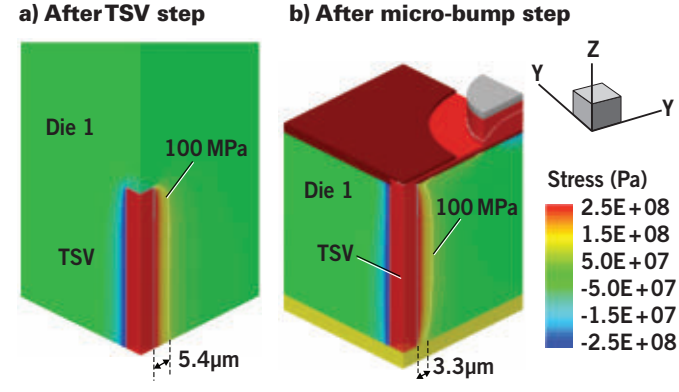


FIGURE 9. Stress evolution with TSV process steps.

Sxx between two process steps. After the TSV formation step, the region with Sxx greater than 100 MPa extends to 5.4 micron away from TSV. After the micro-bump formation step, the region only extends to 3.3µm [3].

The simulations shown here are a good illustration of the value Sentaurus Interconnect offers in the process development and optimization of TSVs and other 3D-IC structures. ◆

References

1. A. Mercha et al ,"Comprehensive Analysis of the Impact of Single and Arrays of Through Silicon Vias Induced Stress on High-k / Metal Gate CMOS Performance," Proceedings of International Electron Devices Meeting, 2010.
2. A. Karmarkar et al., "Material, Process and Geometry Effects on Through-Silicon Via Reliability and Isolation," MRS Proceedings, vol. 1249, 2010.
3. A. Karmarkar et al., "Copper Anisotropy Effects in Three-Dimensional Integrated Circuits Using Through-Silicon Vias," IEEE Trans. on Device and Materials Reliability, vol. 12, 2012.

Current and future defectivity issues for equipment components and materials

VIBHU JINDAL, *SEMATECH, Albany, NY*

The Nanodefect Center is tackling the big challenges in particle detection, characterization and mitigation for critical supply chain components and materials.

Changes in the semiconductor equipment and material ecosystem such as scaling of nodes below 20nm, new materials and process integration for sub-20nm node manufacturing, next generation lithography requirements, and progression to the 450mm wafer size require stringent performance specifications be met in a timely manner. The ecosystem is currently facing huge investment gaps where R&D costs are exponentially increasing due to the costly infrastructure necessary to deliver the solutions. This puts tremendous pressure on the component-level supply chain due to continuously changing technology requirements and slow adoption cycles which in turn result in sluggish recovery of high non-recurrent engineering costs.

Industry requirements for some processes, such as EUV lithography, require zero defects above 50nm in size, since these are considered killer defects, and only a few defects can be tolerated between 20nm and 50nm. The defect requirements for other applications are less stringent, though the trends are driving towards less than 10 particles at continuously smaller sizes. The reduction of particles at such small sizes is producing extreme challenges for original equipment manufacturers (OEMs) as they must tightly control the performance of every component within the equipment, in addition to reducing process defects. The component suppliers face additional challenges as they not only have to meet the stringent performance specifications but also must improve performance based on continuously changing process latitudes and chemistries of end users.

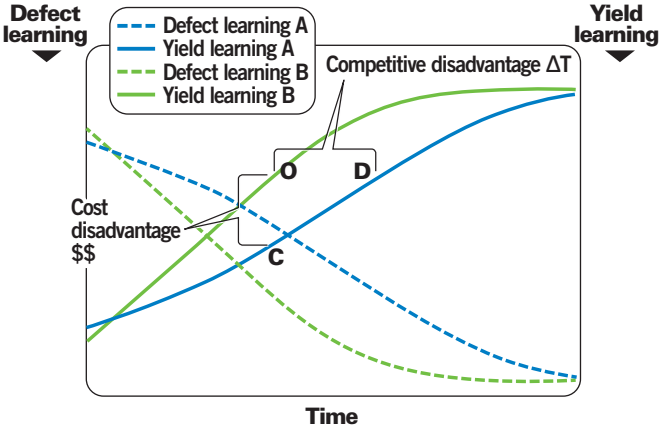


FIGURE 1. The comparison of faster and slower defect learning on yield ramps and curves describing cost advantage and competitive advantage.

VIBHU JINDAL *is managing projects at SEMATECH's Nanodefect Center on reducing defects in components and equipment. Previously, he was a Group Leader in SEMATECH's EUV Mask Blank Defect Reduction Program.*

One of the biggest challenges with such small defects is inspection and metrology. State-of-the-art inspection tools can find defects down to 25nm on wafers and masks. Inspection tools capable of detecting smaller sizes are not available. Inspection and failure analysis tools that are capable of detecting defect sources below 50nm are enormously costly, which causes a large infrastructure gap for suppliers working in component and material development. Lacking that infrastructure, it is very difficult for many OEMs and subsystem, component and material suppliers to reduce defect sources and improve defect performance.

Additionally, as defect reduction requirements go down to such small sizes, interdisciplinary knowledge is required to understand the defect generation process and later devise removal or mitigation techniques. Therefore, research and learning at such small defect sizes can take longer which increases development time of components and materials. This delay, in turn, affects yield ramps. Such challenges and slow development will put huge pressure on yield learning for end users in a production environment. A possible delay in yield ramp and learning is shown in **FIGURE 1**, for two cases (A and B) of defect learning and defect reduction in a manufacturing environment. Slower defect learning in the manufacturing environment not only translates to a higher cost of the manufactured chip but also results in the loss of competitive advantage as the chip products cannot be delivered in time. The difference OC in Figure 1 shows the cost disadvantage due to the yield loss while OD represents the competitive disadvantage due to delay in yield and time-to-market (TTM).

> SEMATECH is taking the initiative to aid the supply chain ecosystem by providing the required infrastructure and expertise through the Nanodefect Center (NDC).

SEMATECH has accelerated efforts to identify areas where particle performance can significantly affect yield learning in current and future manufacturing. By conducting multiple workshops with more than 70 companies (including major IDMS, foundries, OEMs, component and material suppliers), SEMATECH has identified major concerns and key focus areas. The defect performance of application-specific seals and valves, organic and molecular contamination, insufficient material and chemical filtration, defectivity and damage due to e-chuck, pump issues, and cleaning and packaging of components were some of the critical areas identified.

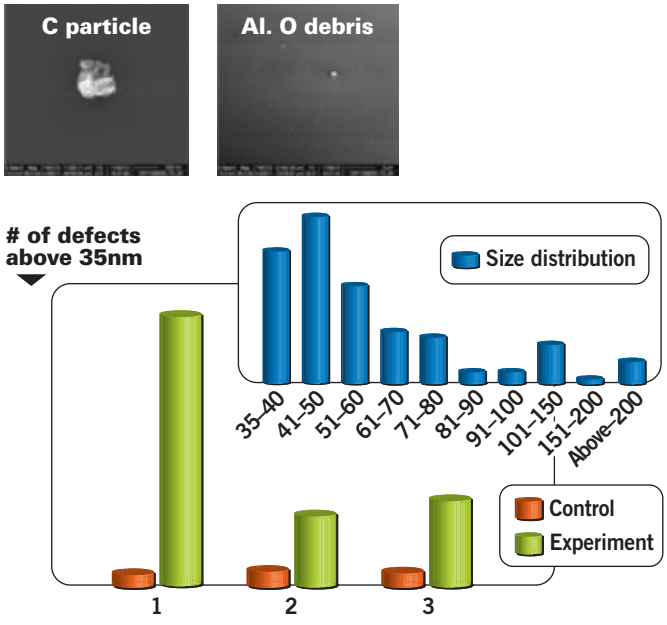


FIGURE 2. Defect performance of a valve evaluated by cycling 5000 times each in three different experiments. The size distribution test of the particle shows higher number of particles below 80 nm of composition like Al and C.

An example issue evaluated by using specialized test stands is shown in **FIGURE 2**. A valve and seal component was cycled 5,000 times per experiment. The initial cycles (Experiment 1) show a very high number of particles generated due to new component issues such as cleaning and packaging. Later, (in Experiment 2 and 3) the defect numbers per cycle were stabilized. The inspection map shows a signature of defects generated where the blade of the valve closes. It should be noted that the performance of this component was acceptable for particles above 100nm size specification while the defect performance will fail if critical defect size scales down to 50nm.

In a similar example, the defect performance of substrate transfer in a deposition system is studied for three different cases: adder defects with electrostatic

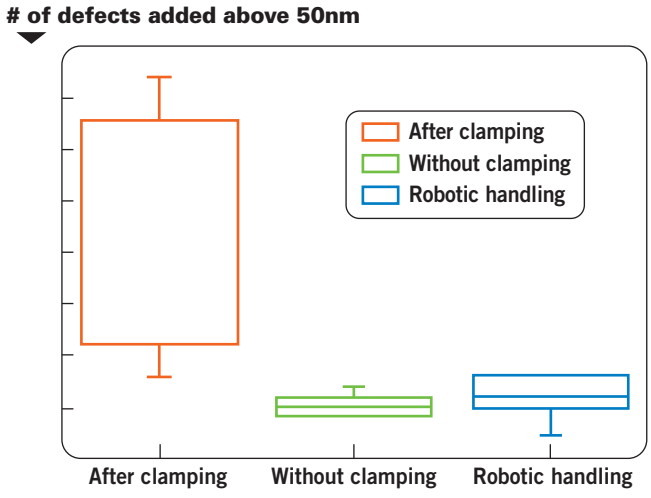


FIGURE 3. The defect performance of substrate transfer in a deposition system compared for robotic handling and substrate clamping.

chuck clamp, without clamping and repeated handling by robotics (**FIGURE 3**). A very high number of defects at a lower size distribution were found for substrates after clamping while the difference in defect performance at larger size distribution was comparable for three cases.

During the workshops, many industry representatives, from both OEMs and component suppliers, highlighted that insufficient progress in fundamental research in defect generation and transport, and lack of infrastructure to test or evaluate particle performance, may lead to a scenario where the industry is ill-equipped to meet the defectivity specifications. SEMATECH is taking the initiative to aid the supply chain ecosystem by providing the required infrastructure and expertise through the Nanodefect Center (NDC). The NDC has built on more than a decade of expertise and infrastructure developed by SEMATECH to tackle the big challenges in particle detection, characterization and mitigation for critical supply chain components and materials. An example of such unique capabilities at SEMATECH is shown in **FIGURE 4** where a sub-20nm particle on substrate buried beneath deposition layers was detected, characterized for compositional analysis and later traced back to determine the defect source.

The NDC offers the opportunity for different sectors of industry to conduct R&D using a common facility equipped with critical and expensive infrastructure to drive to the defect performance needed for components and materials. Sharing test facilities reduces the R&D costs and facilitates a closer supplier collaboration which is essential for the lateral and vertical integration needed in today's semiconductor industry. The center, in conjunction with SEMATECH's membership of chip manufacturers, will also develop roadmaps and key performance metrics for defectivity of critical components.

The NDC has already started to engage the supply chain in these key areas a) component development for defectivity performance for vacuum, plasma, and deposition applications, b) Evaluation and particle reduction for wet applications such as DI water, chemicals, resists, liquid filtration and surfaces after cleaning and c) sources and mitigation of molecular contamination and filtration. Multiple companies have engaged with the Nanodefect Center because they share SEMATECH's strategic vision that the roadmaps, key performance metrics and testing environments are critical to the future of the component and materials industry.

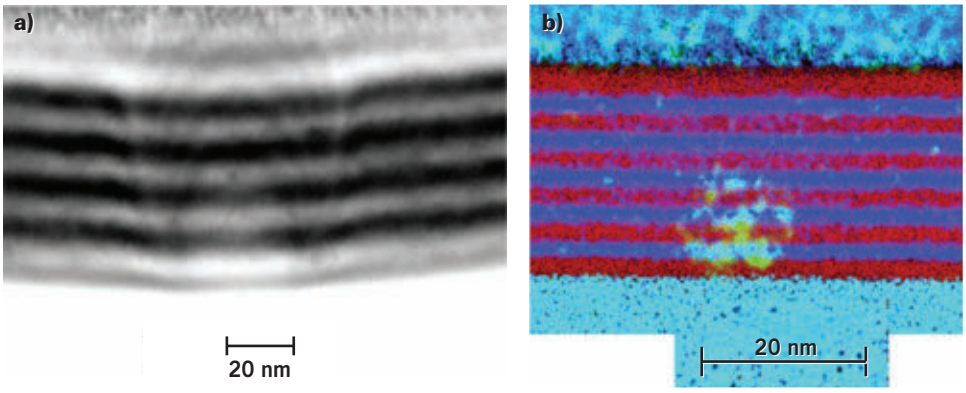


FIGURE 4. The inspection, detection and failure analysis of sub 20 nm defect of substrate buried beneath deposition layers. (a) TEM micrograph of defect on substrate buried beneath deposition layers. (b) EDS in TEM determining compositional analysis.

First 2.5D acoustic imaging

TOM ADAMS, *Sonoscan, Inc., Elk Grove Village, IL*

Acoustic micro imaging enables quick, non-destructive evaluation and can detect whether materials are bonded or not.

Silicon interposers that fit the "2.5D" definition will, within a year or two, move into volume production and provide high performance in a small, relatively inexpensive package having multiple functions. Right now, though, the 2.5 D interposers are going through the rigors of design and development - which explains why so many wind up at Sonoscan for advanced acoustic micro imaging.

Typically 2.5D configurations have one or more flip chips on top, connected by microbumps to the interposer itself. Through-silicon vias in the interposer serve as a complex redistribution layer, and are connected to the substrate below by larger solder bumps. The microbumps are typically 20 to 30µm in diameter, while the solder bumps are typically 100µm in diameter.

As one would expect during a period of active development, there are numerous variations among the many 2.5D samples that have come to Sonoscan. The makers of the packages are interested in seeing acoustic images that reveal the integrity and bonding of the tiny microbumps and the larger solder bumps, as well as the integrity of the two layers of underfill. Acoustic micro imaging is the best choice for quick, non-destructive evaluation because it can detect whether materials are bonded or not. X-ray can detect materials, but not bonding or the lack of bonding. Acoustic micro imaging can also bypass physical sectioning, which might well cut through the configuration at the wrong location, and which has the potential to produce artifacts that might be mistaken for defects.

The frequencies employed in acoustic micro imaging systems fall into two arbitrarily defined groups: Very High Frequency (from 5 MHz to 75 MHz), and Ultra High Frequency (from 100 MHz to 400 MHz). Silicon interposers require high resolution and therefore are typically imaged with UHF transducers; the same is true of less expensive glass interposers. Understandably, all 2.5D samples are currently highly confidential, so no acoustic images accompany the text of this article.

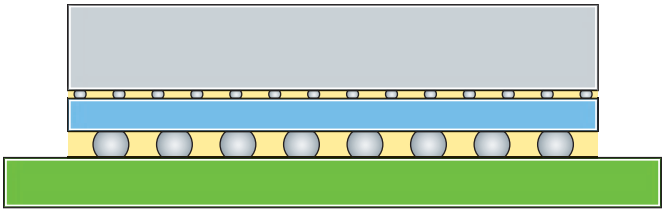


FIGURE 1. Diagrammatic side view of silicon interposer assembly.

All of the silicon interposer samples that have been sent to Sonoscan so far have been underfilled between the flip chip (or chips) and the interposer, and between the interposer and the substrate, as shown in **FIGURE 1**, which is not to scale. None of the samples was overmolded. There is considerable variation in the thickness of the chips. The flip chip may be as thick as 500µm, but is usually somewhat less. The silicon interposer is thinner, sometimes as thin as the 100µm solder bumps on which it rests. The top member of the assembly may be a single large flip chip, or multiple side-by-side smaller flip chips, which sometimes appear optically to be a single flip chip. Overall, imaging a 2.5D sample is somewhat similar to imaging a flip chip, but the number of internal interfaces is larger, making the imaging process somewhat more challenging.

All of the silicon interposer samples submitted have been imaged successfully. The firms submitting the samples want to see acoustic images of the 20µm

TOM ADAMS *is a consultant with Sonoscan, Inc., Elk Grove Village IL USA, Phone: 847 437-6400 E-mail: info@sonoscan.com Website: www.sonoscan.com*

and 100µm solder bumps to determine that they are present, intact and well bonded at their top and bottom surfaces. Even if its vertical extent is as little as 0.01µm, the gap that exists where a bump is not bonded reflects virtually all of the ultrasound. It thus creates a bright feature in the acoustic image or, in some cases, may simply appear as a missing bump in the pattern.

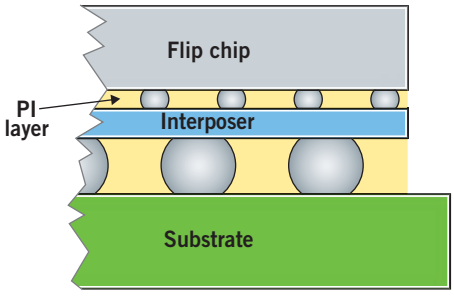


FIGURE 2. Key features, and depth imaged by each transducer.

Firms submitting 2.5D samples are also interested in the presence of voids or other anomalies in the underfill material. Voids have been imaged in the underfill beneath the flip chip and in the underfill beneath the silicon interposer. Voids are significant, especially when adjacent to a solder bump, because the local absence of underfill can permit leaded solder in particular to migrate into the void until the bump deforms and loses its electrical connection. A second mechanism is the fracturing of a bump that is adjacent to a void; this type of failure is far more common in the lead-free solder typically used in silicon interposer assemblies.

Also of interest are cold solder joints and bumps that are delaminated from the underbump metallization. On occasion other types of defects may be found. To date, aggregations of filler particles within the underfill have not been observed to be an issue.

The acoustic frequency used to image the flip chip bumps and interface bumps can be limited by structural features in the assembly. For example, some flip chips have a low-k dielectric layer made of any of several porous materials that attenuate ultrasound. There may also be a polyimide (PI) layer that coats the active surface of the flip chip. Since it is a polymer, the PI layer could also cause signal loss at high frequencies.

To date all silicon interposer samples have been imaged by standard Sonoscan transducers, but it is already evident that there may be advantages to imaging silicon interposers with customized transducers fine-tuned to the silicon interposers' geometries and materials.

In some samples better data and images about each solder bump layer can be used by employing software that allows the operator to divide the depth of interest into a number of individually gated depths, for each of which an acoustic image will be made during a single transducer scan.

The maximum number of gates is 200. In silicon interposer samples the two depths of interest are the two underfill layers, the solder interconnects in these layers, and the interfaces with layers above and below the underfill. These two depths are respectively about 25µm microns and about 100µm in vertical extent. Any desired number of gates can be set to image one of these depths. Each gate generates a single acoustic image, so a sequence of images moving downward through a layer creates what amounts to a slide show. If there is an anomaly in the solder bumps or the underfill, these images may provide detail.

The gates are normally set up to be adjacent to each other, but they can also be overlapped. Overlapping the gates increases the number of images and can provide even more information. The value of the method is limited, though, if the flip chip is warped. Part of each image will represent depths outside of the desired gate, and the images will therefore appear distorted.

The imaging of details in the interposer-to-substrate bumps can be challenging because of the number of interfaces ultrasound must travel through. Often these details can be enhanced by switching from the normal time domain imaging to a Frequency Domain Imaging (FDI) method. FDI decomposes the return echoes from a given depth range into individual frequencies. The depth range is often the vertical extent of the solder balls and underfill. From the decomposed echoes an acoustic image is made for each frequency; thus in one scan a single transducer might create 20 to 30 images, all from the same depth range, and all with the same transducer focus.

Examining these images, the microscope operator will notice significant differences in the imaging of features from one frequency to the next. A small or elusive anomaly such as bump damage or a void that would escape notice in a time domain image is very likely to be visible in one or more of the FDI images.

When the chips are down

SCOTT JONES, *Alix Partners, San Francisco, CA*

There's a need for greater R&D efficiency in the semiconductor industry.

It's well known in the semiconductor industry that R&D is the lifeblood of the business. In 2012, R&D spending in the $300 billion chip industry neared $50 billion annually—roughly 16% of revenues. These high levels of investment are necessary to keep pace with the demands of Moore's Law. With long development cycles, these companies must place huge bets on technology trends years before the products they enable enter the marketplace. In this industry more than any other, the ability to align ones' R&D capabilities with market opportunities and deliver these programs to the market on time is crucial to the financial success of semi companies. In the industry study AlixPartners recently released, we show how powerful the lever of increasing R&D efficiency can be to increasing profitability.

Currently, the ability to fund the necessary R&D to fuel industry growth is under pressure from a combination of slower revenue and growth and rapidly rising costs for leading edge development. Our study shows revenue growth is slowing across the industry, pressuring R&D teams to maintain the same level of innovation with fewer resources. At the same time, R&D costs are increasingly dramatically—by as much as 60% for fabless chip designers for development on the leading edge. As a result, companies face a significant risk that the combined pressures of reduced R&D budgets and higher R&D costs will drive an innovation death spiral, in which an inability to fund R&D programs causes companies to continuously miss product cycles, leading to further revenue declines and market share erosion. In this environment, getting more out of your investment through improved R&D efficiency is critical.

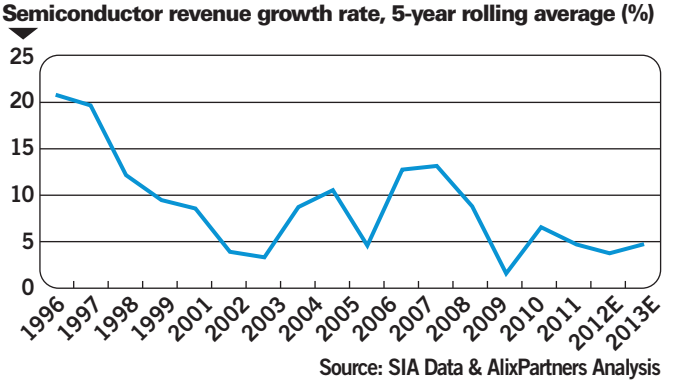


FIGURE 1. The rate of revenue growth in the semiconductor industry is near a 20-year low.

Slow revenue growth threatens R&D investment

The rate of revenue growth in the semiconductor industry is near a 20 year low (**FIGURE 1**). Even as the industry rebounds from the trough in 2009, the recovery has not yielded sustained annual growth near the historical levels of 8 to 10%. The five-year rolling average has been in a range of 1 to 6% for the past four years and is expected to improve only slightly in 2013. While we expect a slight recovery in the market in the second half of 2013, growth is unlikely to reach levels that exceed 5%, well below historical averages. The industry average revenue growth rate has slowed to 3% since 2006, after averaging 12% growth from 1991 to 2006. As companies attempt to maintain R&D spending as a percentage of revenue, the slower top-line growth pressures R&D teams to innovate with lower R&D budget growth.

One of the dynamics that is influencing the market growth is the convergence of the PC market with mobile handsets through the growth of smart phones and tablets. Since the introduction of the iPad in 2010, the tablet market has grown rapidly and is cannibal-

SCOTT JONES *is a Vice President at Alix Partners. Previously, he was an equity analyst with JPMorgan covering the semiconductor sector and spent seven years with Intel Corp. in finance and operations.*

izing demand for the traditional notebook PC market; while some of the demand for tablets has been incremental to the overall market, most tablet sales have come at the expense of the notebook PC market. The growth of the combined notebook and tablet market is marked by both a flattening of the growth trend for notebooks and an explosion in tablet growth since 2010. In 2011, tablet sales grew by more than 250% year over year while notebook sales grew by only 2%. In 2012, tablet sales are estimated to have grown at a 67% rate; notebook sales growth remained at a 2% rate.

Leading-edge R&D spending rising rapidly

Revenue growth may be slowing, but the same cannot be said for the need for and cost of R&D. The cost of developing leading edge products and chip manufacturing processes is increasing at higher rates each generation. A recent presentation at the Common Platform Technology Forum stated that integrated device manufacturers (IDMs) and foundries are experiencing 35% cost increases from one process technology to the next while fabless semiconductor companies are seeing even greater cost increases—of roughly 60%—for designs and tapeouts on next generation process technologies (**FIGURE 2**).

Leading-edge fab costs have increased at an average rate of roughly 30% per generation over the past decade and we expect at least the same sort of increase at 14nm, if not greater due to the complexities of moving to new transistor technologies necessary at geometries beyond 20nm.

The R&D costs necessary to develop a next-generation process manufacturing technology are increasing at a similar rate; at nearly 30% per generation, a rate that has remained relatively steady for the past decade. This is mostly due to the high cost of the test wafers and development tools necessary to deliver a new process technology. More expensive test wafers and tools mean that foundries and IDMs cannot afford to invest in as many customer specific or variant technologies. This puts more pressure on foundries to deliver a leading-edge technology platform that can address a sufficient segment of the market to allow for a positive return on their leading edge investment.

Chip design for leading-edge products is seeing the most rapid rise in costs. The cost to design a chip for a leading-edge process has increased at nearly 60% per generation over the past decade. This is twice the level of the increase in costs for leading-edge fabs and new process technologies. As a result, fabless semiconductor companies can afford fewer chip designs on the leading-edge processes. This makes it even more critical that the leading edge development programs have the features that end market customers require and are targeted at the market segments with the highest value. The upstream impact on the foundries is that fewer designs on the leading edge lead to a higher concentration of volumes on a small number of products.

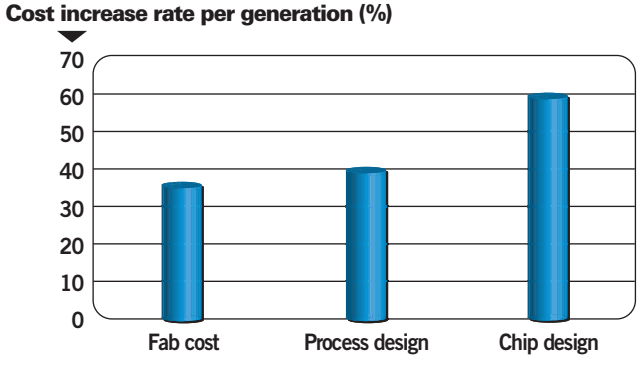


FIGURE 2. IDMs and foundries are experiencing 35% cost increases from one process technology to the next while fabless semiconductor companies are seeing even greater cost increases—of roughly 60%—for designs and tapeouts on next generation process technologies.

Importance of R&D efficiency and time to market

The major risk for companies during periods of slower revenue growth is that pressure on R&D budgets will prevent the product development necessary to spur future revenue growth, leading companies to miss major product cycles. This creates a potential innovation death spiral for companies, in which an inability or unwillingness to fund necessary R&D programs leads to further market share erosion and greater revenue declines.

How does this spiral downward begin? When a company has missed market signals and its products are not aligned with end market needs, it is likely to lose key market share or to become too heavily exposed to a shrinking market (for example, notebook PCs). This can lead to obvious negative impacts on revenue and earnings. A common reaction to this

scenario is to constrain R&D spending as part of overall retrenchment, but if this is not done in a careful and thoughtful way, the company risks accelerating its losses through continued market share declines resulting from a lack of innovation through insufficient R&D investment.

One of the biggest impacts of R&D efficiency is the ability to get products to market on time. For leading-edge products where power and performance count most, time to market likely means the difference between success and failure. The challenge for companies is not only to deliver individual programs on time but also to balance a portfolio of R&D resources and deliver multiple programs on time to the market—and to do it generation over generation. Often, organizations take on too many programs to gain market share on the current generation and starve resources for the subsequent generation, leading to an inability consistently deliver to market needs. The result of this R&D over-commitment is often that the effort to capture incremental opportunities puts the delivery of programs serving the core business at risk.

Efficient R&D leads to greater profitability

In a recent AlixPartners' study of the 72 largest publicly traded semiconductor companies globally finds that companies that are able to grow their revenues at a rate greater than R&D spending increases achieve increased profitability. As shown in **FIGURE 3**, thirty-four out of 41 companies—or 82%—that grew R&D spending as a percent of revenue more quickly than they grew revenue saw a decline in operating margins. But among those companies that grew R&D spending at a lower rate than revenue growth, 24 companies out of 31—or 77%—saw an increase in operating margins.

This does not mean that companies should reduce their R&D budgets to lower levels to reflect their revenue growth. It does, however, indicate that companies that achieve higher returns on their R&D investment, as demonstrated through higher revenue growth, are much more likely to demonstrate higher levels of profitability over time.

Companies with poor R&D efficiency often suffer from a lack of proper planning more than an inability to innovate. The areas of highest importance are: aligning R&D investment to the market needs, allocating the proper amount of resources, and setting sufficient financial requirements for the programs to meet. Aligning R&D capabilities with opportunities prioritized from the marketing organization can enable management to create a list of programs that the organization is capable of delivering. After financial requirements and analysis have been provided, management should be able to rank the potential programs based on the strategic priorities of the company and on expected ROI. Once the execution of the programs begins, the key is to ensure that the highest rated priority programs are fully resourced and brought to market on time with all of the key features necessary to make the offering successful.

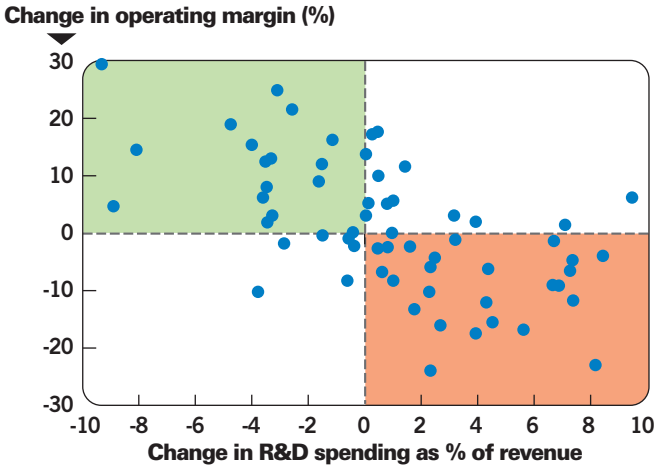


FIGURE 3. Companies that grew R&D spending at a lower rate than revenue growth saw an increase in operating margins.

Conclusion

Innovation is a key competitive differentiator for semiconductor companies. Getting to market on time with the right products can make all the difference between success and failure. As revenue growth remains low and the cost of R&D continues to rise, the amount of money companies can profitably spend on R&D is pressured. In this context, optimizing the efficiency of the R&D investment process is of paramount importance. Successful semiconductor companies must improve R&D ROI through proper planning processes and better allocation of resources. In this way, companies can achieve top-line growth while lowering R&D costs per program, paving the way for future successes.

Meeting the challenge of film frame handling automation

BOB FUNG *and* **JACK YAO**, *Owens Design, Fremont, CA*

Semiconductor and LED manufacturers are interested in automating the film frame handling process as a means to increase throughput and yield in their BEOL processes.

Until recently, the loading and unloading of film frames into process tools in both the semiconductor and LED industries has primarily been a manual operation. Both industries, however, are experiencing an increasing need to automate this process due to the large quantity of dies on wafer and scaling of production throughput.

Film frames are typically used in back-end-of-line (BEOL) operations in the LED and semiconductor industries to contain substrates that will eventually be diced or scribed and then split apart. The frame holds a sticky film that keeps the separated dice or LEDs in a manageable array after they have been separated into individual components. This can be particularly critical in LED manufacturing, where several thousands of LEDs are produced from a 2, 4, or even 6 in. wafer. For the same reason, film frame automation will be even more critical once LED industry migrates into 8 in. wafers.

In semiconductor applications, the film frame can be used to stretch the film to make it easier to pick up individual dice for BEOL test and binning applications, for example. In LED processes, stretching the film frame can be used to separate the individual LEDs after the wafer has been scribed.

Film frames are also particularly useful when processing fragile or thin substrates. In LED manufacturing, for example, the residual LED device wafers are more difficult to handle with standard wafer handling equipment after removal of the base sapphire substrate. Using film frames in such circumstances, will improve production yield by minimized the potential of device damage via improper handling of fragile wafers.

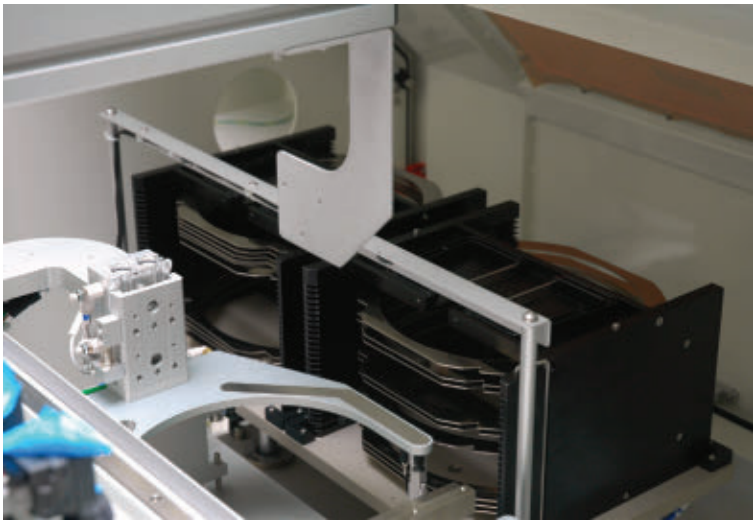


FIGURE 1. Film frame handler configured for side-by-side cassettes.

The need for automation

For the semiconductor industry the drive toward film-frame-handling automation is powered by the need to address the timing requirements of BEOL inspection

BOB FUNG *is Vice President of Engineering for Owens Design. He has a 30 year career in the disk drive, semiconductor and PV equipment development.* **JACK YAO** *is Director of Business Development at Owens Design. Prior to joining Owens Design, Jack spent twelve years in the semiconductor equipment industry working for Aviza Technology, ASML, Silicon Valley Group and Watkins Johnson. www.owensdesign.com.*

and test applications, where throughput with high yield is critical. The increasing size, weight and value of semiconductor wafers has added ergonomic and risk mitigation concerns that have further fueled the need to automate the process.

The LED industry has been expanding into a wide variety of applications, including aviation and automotive lighting, household appliances, remote controls for electronic systems, television backlighting, traffic systems and even household lighting. As a result, LED manufacturers have found it necessary to increasingly automate their manufacturing processes to enable the greater production volumes required to support this growing demand for their products across an expanding variety of markets.

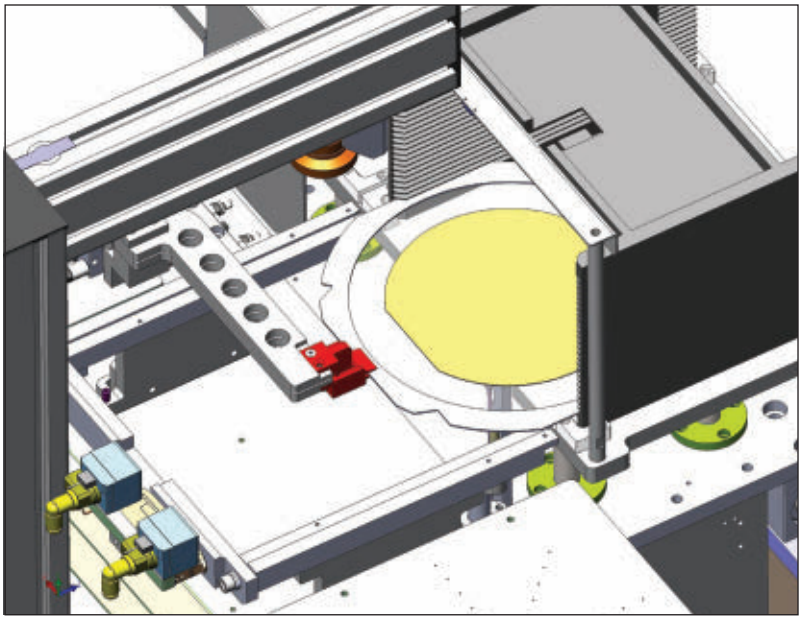


FIGURE 2. Film frame being removed from cassette and placed under an alignment camera.

At the same time, however, both industries are extremely cost sensitive. The semiconductor industry, for example, is driven by the imperative of Moore's Law that has governed number of transistors on integrated circuits doubles approximately every two years, has helped to influence reduction of IC pricing as technology advances. For the LED industry, lowering LED prices has been a key factor in its expansion into many markets and is critical if LEDs are to replace more power-hungry incandescent light bulbs in the home-lighting market.

While LED lighting offers consumers a more environmentally friendly alternative to the incandescent light-bulb, cost-per-watt parity at a minimum will be required to overcome consumer reluctance to adopt a new lighting technology in place of the familiar incandescent light bulb that has been in use for decades. This was amply demonstrated by the recent furor over Congress' attempt to mandate alternatives to the incandescent bulb. For the LED industry, the best route to ensuring widespread adoption of LED lighting in the home is to offer consumers a product that is more environmentally friendly, but which most importantly, costs less and lasts longer.

Challenges to automation

Traditionally, film frame has been handled manually by tool operators. Even today, many film frame applications remain manual. As a result there has been no effort to develop any kind of film frame handling standards in either the semiconductor or LED industries.

Due to this lack of industry-wide backend standards, the semiconductor and LED manufacturers either adopted or developed their own customized solutions that suited their manufacturing needs. In both industries there has been a widespread proliferation of varying film frame form factors, which make it extremely difficult for process tool manufacturers to develop cost effective automation solutions that can meet the needs of a wide range of manufacturers.

While there is discussion within the semiconductor industry of developing film frame handling standards for emerging 450mm processes, this does not address the automation needs of 200 and 300mm manufacturing lines. It also provides no automation relief for the LED industry which is mostly comprised of 50 and 100mm wafers.

This situation is exacerbated by the cost-sensitivity of the BEOL processes that use film frame handlers in both the LED and semiconductor markets. While manufacturers in both industries are eager to increase

throughput in their BEOL process to enhance volume production and yield, they are reluctant to do so if automation significantly increases their manufacturing costs. At the same time, process tool OEMs struggle to deliver automation solutions that will deliver an acceptable return on investment (ROI) due to the need to highly customize each system design In addition to the lack of industry standards and added hardware cost, attempts to automate film frame handling also face technical challenges relating to the management and alignment of film frames in and out of cassettes.

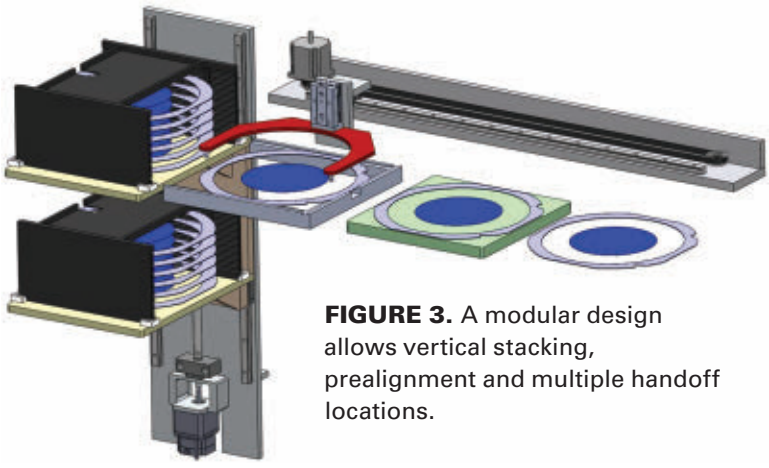


FIGURE 3. A modular design allows vertical stacking, prealignment and multiple handoff locations.

Traditionally, most equipment companies have leveraged the use of "off the shelf" robots as a key component in wafer automation. Unfortunately, using a typical robot and robotic end-effector to remove a film frame from a cassette via an insert, lift and pull motion path is frequently not feasible due to the limited slot pitch of the cassette.

Alternatively, removing film frames from cassettes by dragging the frames out by their leading edges could be a problem in some applications due to particle generation. Obviously, an automation solution that increases throughput, but decreases yields is not going to be seen as an optimal solution.

A final technical challenge involves proper alignment of the film frame relative to the target substrate. Proper alignment is often complicated by the fact that the substrate's mechanical features used for alignment are not accessible due to the supporting structure of the film frame. Misaligning the substrate or wafer prior to dicing or scribing would be disastrous in terms of lost product.

Meeting the automation challenges

What is needed, then, is an automation solution that can address these technical automation challenges, while offering a cost-effective solution that can be easily customizable to meet differing film frame configurations.

Such a system, such as that shown in **FIGURE 1**, would require easily customizable mechanisms and grippers to remove film frames from cassettes with tight slot pitches. These specialized film frame grippers need to grip the front edge of the film frame to extract it from the cassette. Since this approach does run the risk of particle contamination, the front edge of the film frame must be gripped in such a way that the frame can be slightly lifted vertically so that there is no rubbing between the frame and the cassette when the frame is extracted from or replaced into the cassette.

The issue of aligning the substrate with the film frame can be resolved using a combination of mechanical and vision technology to ensure fame and substrate alignment. Coarse alignment can be easily achieved by biasing two edges of the frame against two reference planes (**FIGURE 2**). Once this is done, fine alignment can be achieved with a vision system that is able to locate known features on the substrate. Using this information, the film frame handling system can accurately make position corrections as needed.

Most importantly, the film frame handling system requires cassette loadports that can be easily and cost-effectively tailored to meet the requirements for each unique frame and individual application (**FIGURE 3**). This requires that the overall architecture of the automation be very flexible and adaptable. However, the automation approach must be optimized in terms of functional flexibility and cost.

Conclusion

Film frames are used to handle wafers to be separated into individual devices in BEOL inspection, test and packaging applications in the semiconductor and

Continued on page 32

ADVERTISEMENT

Pixelligent Launches PixClear™ Nanocrystals

Introducing PixClear™, Zirconia nanocrystals for electronics and semiconductor applications. PixClear™ delivers a refractive index >1.85 with perfectly clear dispersions compatible with many polymers for seamless product integration. Order PixClear™ at www.pixelligent.com/ssapril.

pixelligent
THE CLEAR SOLUTION™

www.pixelligent.com/ssapril

OCD/Thin Film Metrology Tool for EUV Photomasks

The n&k Gemini furnishes:

(1) Accurate characterization of complex materials from multilayer film stacks; (2) Unlimited number of layers for models; (3) Accurate modeling of complex 2D and 3D OCD Structures for a wide range of pitch, CD and depth values, with no lower limit on structure size. (4) Excellent repeatability and reproducibility.

n&k Technology, Inc.

www.nandk.com

See What You've Been Missing!

Compare and see the MEGAPLUS advantage!

With decades of experience at engineering low-noise electronics and proprietary digital camera technologies, **MEGAPLUS** cameras define the industry by delivering superior image performance, reliability and value.

For a consultation email:
MEGAPLUS@princetoninstruments.com

MEGAPLUS®
Imaging Precision

www.princetoninstruments.com/MEGAPLUS

IC Package Inspection: 3D/2D HVM In-Tray

- Up to 120,000 UPH
- Unconstrained true bump height/coplanarity/warpage measurements
- In-tray measurements – minimal handling
- Supports all types of IC package inspections: BGA, QFN, QFP, LGA, SGA, PGA, PoP, and derivatives

zygo

www.zygo.com

Solid State Technology

For over 50 years, Solid State Technology has been the leading independent media resource, covering:

- Semiconductors
- Advanced Packaging
- MEMS
- Displays
- LEDs

Request a **FREE** subscription to our magazine and e-Newsletters today at
www.solid-state.com/subscribe

www.solid-state.com

Clean Environments for Electronics Mfg.

From Simplex — Use SIS 212 framing and AirBlock softwall curtains for modular, portable clean rooms and enclosures. Reduce contamination, increase product yields. Easy assembly. Anti-static curtain materials available. Move anywhere.

SIMPLEX™
ISOLATION SYSTEMS

www.simplexstripdoors.com/sis212.htm

LED industries. Handling film frames has traditionally been a manual process, which has led to a lack of industry-wide standards and a proliferation of varying film factors. Today, both semiconductor and LED manufacturers are interested in automating the film frame handling process as a means to increase throughput and yield in their BEOL processes. Since these manufacturing processes are extremely cost sensitive, the lack of standards has created a challenge in developing effective automation solutions. This cost and risk challenge has been exacerbated by various technical challenges involving removal of film frames from cassettes, substrate alignment and particle contamination . Fortunately, these technical challenges, as well as the development of customizable cost-effective solutions are possible.

FLEXIBLE DISPLAYS

Continued from page 15

increase in carrier mobility and about a 10-fold increase in threshold voltage stability.

An important question for mobile display applications concerns the display resolution that can be achieved with these carrier handling techniques. A number of flexible OLED display prototypes have been shown, presumably made on polyimide substrates coated onto a glass carrier and released using a laser. These displays have resolutions of order 200 dpi (full color), although very little information has been made publicly available regarding their long-term electrical performance. Flexible Display Center has not yet investigated the resolution limits that can be achieved using their adhesive bonding technique, although the data on dimensional distortion throughout their unique process suggests that resolutions of 200 dpi and higher ought to be achievable.

In summary, the appearance of the first flexible high-resolution displays in the market is imminent. They will be produced using materials handling techniques that have been developed to allow the use of existing thin transistor fabrication facilities. These techniques are still under intensive development, including the evaluation of the relative merits of different design trade-offs.

ad index

Solid State TECHNOLOGY

EXECUTIVE OFFICES

PennWell, 98 Spit Brook Rd, Nashua, NH 03062-5737
Tel: 603/891-0123

ADVERTISING

Marcella Hanson—
Ad Traffic Manager

Justine Beauregard—
Marketing Communications Manager

ADVERTISING SALES OFFICES

Group Publisher
Susan Smith
98 Spit Brook Rd,
Nashua, NH 03062-5737;
Tel: 603/891-9447;
Fax: 603/891-9328;
e-mail: susans@pennwell.com

Sales Manager
Kerry Hoffman
98 Spit Brook Rd.
Nashua, NH 03062-5737
Tel: 603/891-9118;
Fax: 603/891-9328;
e-mail: kerryh@pennwell.com

The ConFab
Sabrina Straub
98 Spit Brook Rd.
Nashua, NH 03062-5737
Tel: 603/891-9118;
Fax: 603/891-9328;
e-mail: sabrinas@pennwell.com

Europe
Holger Gerisch
Hauptstrasse 16,
D-82402 Seeshaupt, Germany;
Tel: 49/(0)8856-802022;
Fax: 493(0)8856-8020231;
e-mail: holgerg@pennwell.com

United Kingdom & Scandinavia
Kerry Hoffman
98 Spit Brook Rd.
Nashua, NH 03062-5737
Tel: 603/891-9118;
Fax: 603/891-9328;
e-mail: kerryh@pennwell.com

Israel
Dan Aronovic
Allstar Media Inc.,
3/1 Hatavas St.,
Kadima, 60920, Israel
Tel / Fax: 972/9-899-5813
e-mail: aronovic@actcom.co.il

Japan
Masaki Mori
ICS Convention Design, Inc.,
Chiyoda Bldg.,
Sarugaku-cho 1-5-18,
Chiyoda-ku, Tokyo
101-8449, Japan
Tel: 3-3219-3641;
Fax: 3-3219-3628;
e-mail: mori-masaki@ics-inc.co.jp

Taiwan
Diana Wei
Arco InfoComm, 4F-1,
#5 Sec. 1 Pa-Te Rd. Taipei,
Taiwan R.O.C. 100
Tel: 866/2-2396-5128
Ext. 270
e-mail: diana@arco.com.tw

China, Hong Kong
Adonis Mak
ACT International, Unit B, 13/F,
Por Yen Building, 478 Castle Peak Road,
Cheung Sha Wan,
Kowloon, Hong Kong
Tel: 852/2-838-6298;
Fax: 852/2-838-2766;
e-mail: adonism@actintl.com.hk

List Rental
Kelli Berry
1421 South Sheridan Rd.,
Tulsa, OK 74112;
Tel: 918/831-9782;
Fax: 918/831-9758;
e-mail: kellib@pennwell.com

May 2013, Volume 56, Number 3 • ***Solid State Technology*** ©2013 (ISSN 0038-111X) **Subscriptions:** Domestic: one year: $258.00, two years: $413.00; one year Canada/Mexico: $360.00, two years: $573.00; one-year international airmail: $434.00, two years: $691.00; Single copy price: $15.00 in the US, and $20.00 elsewhere. Digital distribution: $130.00. You will continue to receive your subscription free of charge. This fee is only for air mail delivery. Address correspondence regarding subscriptions (including change of address) to: *Solid State Technology*,, PO Box 3425, Northbrook, IL 60065-9595, sst@omeda.com, ph 847-559-7500 (8 am – 5 pm, CST).

Ensuring RoHS 2 success with agility

RoHS 2 is the second phase of the European Union's (EU) Restriction on Hazardous Substances (RoHS). After having a decade to understand and implement the requirements of RoHS, manufacturers must now comply with RoHS 2, which primarily extends the product classes, restrictions, and traceability requirements of the original directive. RoHS 2 extensions pertain to product classes (a subset of medical electronics, and industrial monitoring and control instruments), declarations of conformity, technical documents and archiving, Conformité Européenne (CE) mandatory product marking, product identification, traceability, and compliance demonstration through testing or assessment, as well as the phase-out of exemptions from the original RoHS legislation.

With these extensions to RoHS, more companies along the semiconductor and electronics supply chain that supply products to the EU must meet the RoHS 2 requirements. Furthermore, because of the requirement for the CE marking, there are additional responsibilities for manufacturers, importers, distributors, and authorized representatives to ensure and verify conformity to RoHS 2 by maintaining records for products, components, and sub-components, and – in the event that conformity to RoHS 2 is not met – it is the responsibility of the party with that information to report the incident.

LISA ANN *Cairns, Ph.D. , Senior Market Analyst, Smith & Associates*

Traceability and testing by certified partners

Given the explicit and detailed requirements of RoHS 2, agile and knowledgeable distributors are the in-demand partners. When looking for such a leading partner, it is important to ensure that they are industry accredited and certified to provide the quality management (QM), component and material testing laboratory facilities, and full traceability and flow-down reporting necessary to meet RoHS and CE requirements.

Among the internationally-recognized industry standards for accrediting testing laboratories is the ISO/IEC 17025 quality standard. The ISO/IEC 17025 accreditation is both a management and a technical facility quality standard. Labs certified to this standard are those whose testing is performed by industry-recognized professionals and whose facility itself meets various equipment, facility management, and testing methods for the products that are handled.

> If conformity to RoHS 2 is not met, it is the responsibility of the party with that information to report the incident.

Facilities and businesses who have received ISO/IEC 17025 accreditation, as well as ISO 9001, Quality Management Systems, are those that have and are continuously able to demonstrate that both their operations and procedures (O&P) and their QM processes meet rigorous requirements and are adopted and well-established throughout their organization. This type of detailed O&P is the cornerstone to ensuring proper CE and RoHS 2 compliance.

Quality at the core

Certainly RoHS 2 has increased the requirements and QM O&P for many businesses, but, in the global semiconductor supply chain, quality is all the more essential to general corporate strategies. RoHS 2 has increased the detailed list of what we are to recognize as and how we are to understand industry standards, at least for the EU presently, but this is certain to widen in geographical scope. Industry standards inform our understanding of recognized guidelines for processes and procedures, technical knowledge, and laboratory capabilities. While we continue to smooth the learning curve to ensure complete RoHS 2 compliance, understanding how to evaluate partners who can facilitate these transitions and remove any questions or burdens associated with compliance is truly a value add to business strategies today.

EQUIPMENT • MATERIALS
PACKAGING • TEST
SEMICONDUCTORS • LED
PV • EMERGING MARKETS

The Power of [X]

New Programs for 2013

- Silicon Innovation Forum—Top strategic investors review an exciting line-up of new and emerging companies
- A conversation on semiconductor R&D with leaders from imec, SEMATECH and CEA-Leti
- 450 mm Wafer Processing: Opportunities and Prospects
- The latest requirements on nonplanar architectures, stacked 3D ICs, the two paths for lithography, nano defect detection, silicon photonics, printed/flexible electronics, MEMS, LEDs
- Keynote address: Ajit Manocha, CEO, GLOBALFOUNDRIES

Wafer Processing
Packaging
Test

[SEMICON West]

Photovoltaic
Silicon Photonics
MEMS—LEDs

REGISTER NOW and get ready to be a part of the biggest event in microelectronics manufacturing—SEMICON® West 2013!

- Access more than 50 hours of technical programs focused on the critical issues in microelectronics manufacturing
- 450 mm, 3D IC, next-generation lithography, test, contemporary packaging, advanced materials, and more
- Discover technologies, materials, and manufacturing solutions for LEDs, MEMS, plastic electronics, and other emerging and adjacent markets
- Connect with technical experts and find solutions that move your ideas from the lab to the fab

Connect to the Power of [X]—
Connect to the Power of SEMICON West

SEMICON® West2013

July 9–11

Moscone Center
San Francisco, California
www.semiconwest.org

SEMICON West is brought to you by:

ADVANTEST® APPLIED MATERIALS® KLA-Tencor Accelerating Yield semi™