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MAY 2014

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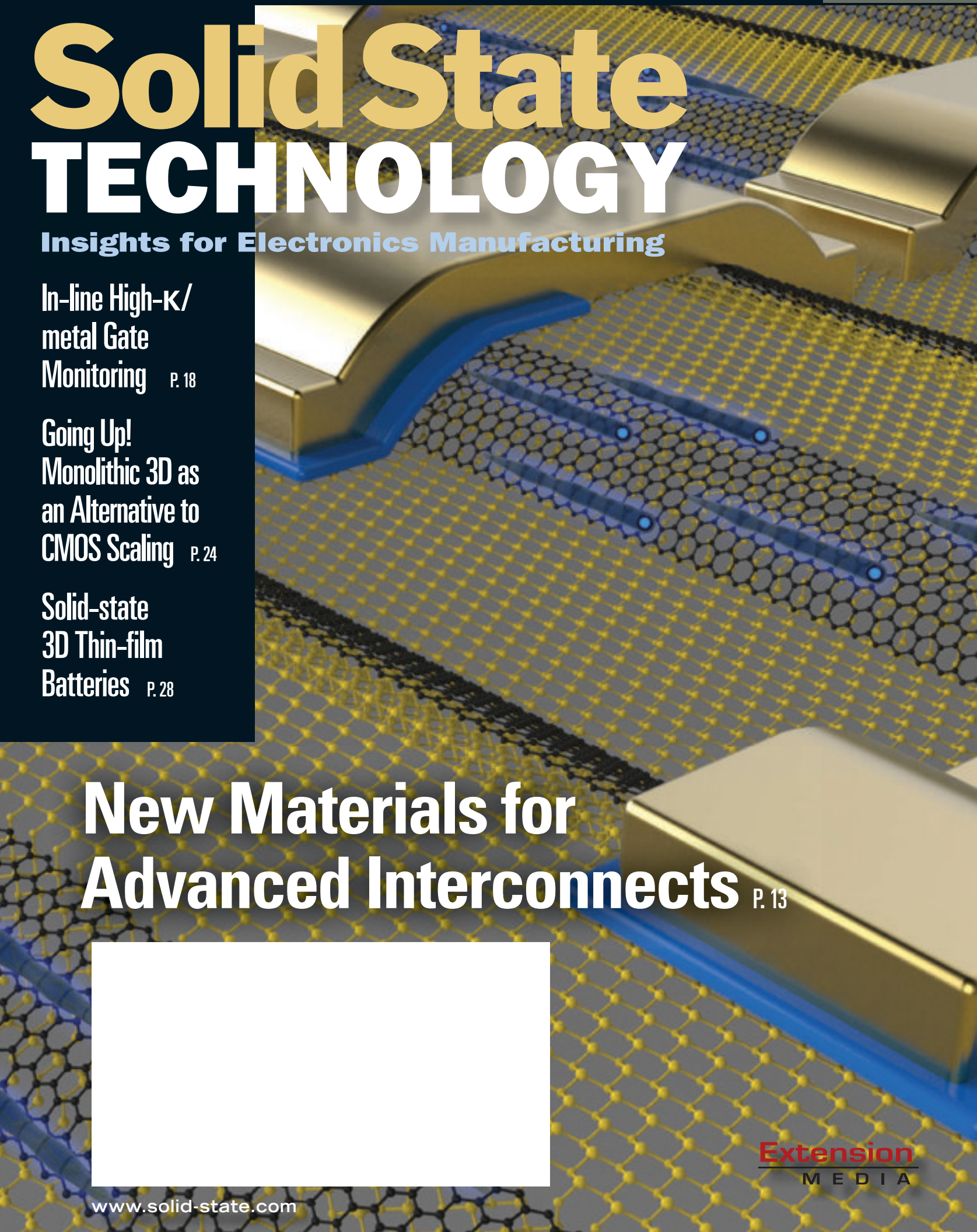

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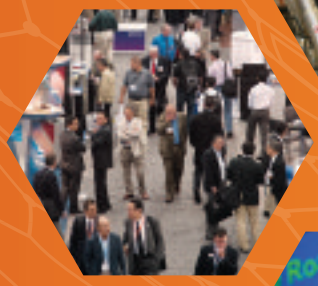

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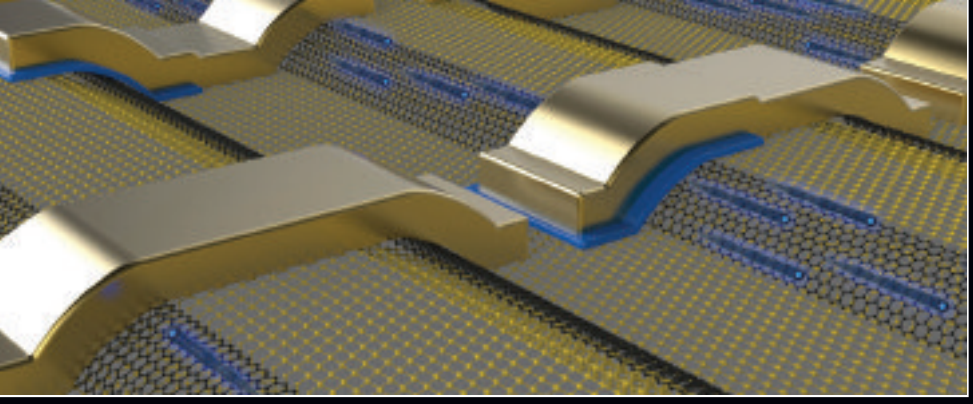

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MAY 2014 VOL. 57 NO.3

Conceptual drawing of an electronic circuit comprised of interconnected graphene nanoribbons that are epitaxially grown on steps etched in silicon. Courtesy of John Hankinson, Georgia Tech.

COVER

FEATURES

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DEPARTMENTS

Web Exclusives

Moore's Law has stopped at 28nm

While many have recently predicted the imminent demise of Moore's Law, we need to recognize that this actually has happened at 28nm. From this point on we will still be able to double the amount of transistors in a single device but not at lower cost. And, for most applications, the cost will actually go up.

http://bit.ly/1oqNWkS

Highlights from the IMAPS Device Packaging Conference

The annual IMAPS Device Packaging Conference in Ft. McDowell, AZ is always a source for the latest packaging information.

http://bit.ly/1fbiKSm

Mission accomplished: Now what?

In the late '80s and '90s, when our magazine staff gathered for dinner we often made a toast: "Here's to chip silicon!" I really believed (and still do) that making electronics more affordable would increase their use and make our lives better and the world a better place to be.

I haven't toasted to cheap silicon for a while. Why? Because that mission has been accomplished.

http://bit.ly/1i8e3iQ

Plug-and-play test strategy for 3D-ICs

Three-dimensional ICs, chips assembled from multiple vertically stacked die, are coming. They offer better performance, reduced power, and improved yield. Yield is typically determined using silicon area as a key factor; the larger the die, the more likely it contains a fabrication defect. One way to improve yield, then, is to segment the large and potentially low-yielding die into multiple smaller die that are individually tested before being placed together in a 3D IC.

http://bit.ly/1fosHj8

n&b news and blogs

Extreme stress for existing foundry/fabless model

In his talk at The ConFab 2014, Qualcomm's Dr. Roawen Chen will describe how the increased performance and the rapid shift from traditional handsets to consumer computing device post a number of manufacturing and supply chain challenges for fabless chip makers.

http://bit.ly/1kqpykf

Insights from the Leading Edge: More IBM rumors

Dr. Phil Garrou addresses reports that GlobalFoundries "...has emerged as the leading candidate to buy IBMs semiconductor operations."

http://bit.ly/1fXDhgN

State of EUVL – Challenges of HVM Introduction

Vivek Bakshi discusses the continued momentum for EUVL as it moves towards high-volume manufacturing.

http://bit.ly/1pth4Od

MEMS – Enter with Care

MEMS – enter with care. Karen Lightman talks about why this is her tagline for MEMS Industry Group's third annual MEMS Executive Congress Europe 2014 recently held in Munich, Germany.

http://bit.ly/1m8cEqz

CD-SEM Sees Beyond >10nm Nodes

At the recent SPIE Advanced Lithography conference, Ofer Adan's keynote presentation focused on how improvements in metrology, multi-patterning techniques and materials can enable 3D memory and the critical dimension (CD) scaling of device designs to sub-10nm nodes. *From SemiMD.com, part of the Solid State Technology network.*

http://bit.ly/1hcdltX

editorial

What's new in the latest ITRS

The newly revamped International Technology Roadmap for Semiconductors was released in early April. It's actually called the 2013 ITRS, which makes it seem already out of date, but that's the way the numbering has always been.

It's a big undertaking, with input from the U.S., Europe, Japan, Korea and Taiwan. Through the cooperative efforts of the global chip manufacturers and equipment suppliers, research communities and consortia, the ITRS identifies critical gaps, technical needs, and potential solutions related to semiconductor technology. Some key findings and predictions of the 2013 ITRS include the following:

• The combination of 3D device architecture and low power devices will usher in a new era of scaling identified in short as "3D Power Scaling." The increase in the number of transistors per unit area will eventually be accomplished by stacking multiple layers of transistors.

• Progress in manipulation of edgeless wrapped materials (e.g., carbon nanotubes, graphene combinations, etc.) offer the promise of ballistic conductors (as shown on this month's cover), which may emerge in the next decade.

• There will be two additional ways of providing novel opportunities for future semiconductor products. The first consists of extending the functionality of the CMOS platform via heterogeneous integration of new technologies, and the second consists of stimulating invention of devices that support new information-processing paradigms.

The ITRS also covers system level integration, including the integration of multiple technologies in a limited space (e.g., GPS, phone, tablet, mobile phones, etc.).

Looking at Long Term Devices and Systems (7-15 years horizon, beyond 2020) the 2013 ITRS reports on completely new devices operating on completely new principles and amenable to support completely new architectures. For instance, spin wave device (SWD) is a type of magnetic logic device exploiting collective spin oscillation (spin waves) for information transmission and processing. No surprise, the manufacturing of integrated circuits, driven by dimensional scaling, will reach the few nanometers range well within the 15-year horizon of the 2013 ITRS.

An addition to the 2013 ITRS edition is a new sub-chapter on big data (BD).The fab is continually becoming more data driven and requirements for data volumes, communication speeds, quality, merging, and usability need to be understood and quantified.

—Pete Singer, Editor-in-Chief

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news

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ASIA | **Toshiba** and **Sandisk** brought lawsuits against SK Hynix for alleged theft of trade secrets.

USA | The Semiconductor Industry Association this week presented its University Research Award to **University of Minnesota** professor Sachin Sapatnekar in recognition of his outstanding contributions to semiconductor research.

ASIA | **STATS ChipPAC** has designed and implemented a new manufacturing method that is a significant paradigm shift from conventional wafer level manufacturing, known as FlexLine.

USA | **: SEMATECH** announced that Ronald Goldblatt, vice president of Technical Strategy and Operations, has been appointed as acting president and chief executive officer.

EUROPE | Researchers from Swiss university **Swiss Federal Institute of Technology Zurich** and **LG Electronics** have developed a method to greatly increase the speed and efficient transmission of gas, liquid and water vapor through perforated graphene.

USA | **Altera** and **Intel** announced their collaboration on the development of multi-die devices that leverage Intel's package and assembly capabilities and Altera's leading-edge programmable logic technology.

ASIA | **Dow Corning** filed a complaint with the Shanghai First Intermediate Court, alleging that Beijing KMT Technology Co., infringed Dow Corning's Chinese patent by manufacturing and selling products using proprietary Dow Corning silicone technology under the Beijing KMT label.

GLOBALFOUNDRIES and Samsung join forces on 14nm finFETs

Fabless companies could skip the 20nm node and move straight to 14nm FinFETs. That is the hope of GLOBALFOUNDRIES and Samsung who are announcing a joint program that offers a single process design kit (PDK) and manufacturing at four different fabs with identical processes. The PDKs are available now, and 14nm manufacturing could move into high volume production by the end of the year.

"This is unprecedented," said Kelvin Low, senior director of marketing at Samsung. "It never has happened in the industry, especially at the very leading edge nodes. We are confident that this will transform the supply chain model," he added.

Fabless companies such as Qualcomm have been lobbying for such multi-sourcing for some time, and are eager to move to FinFETs which offer higher performance and reduced power consumption. 14nm FinFETs offer a 20% improvement in performance and a 35% reduction in power compared to 20nm technology.

"For both Samsung and GLOBALFOUNDRIES, we will be providing our customers with a choice and assurances of supply, enabled by the unprecedented global capacity across our respective manufacturing facilities throughout different locations worldwide," Low said. "For Samsung, we have facilities in the U.S. in Austin. We also have a couple of plants in Korea. For GLOBALFOUNDRIES, the 14nm capacity will be in Malta, NY."

The single process design kit will allow customers to do a single design that is capable of being multi-sourced from different locations.

"This really is a change from the existing supply chain model where customers are trying to design multiple designs to multi-source their products," Low said. "True design compatibility in this collaboration will allow customers to better manage their design NRE and they can focus on bringing the product to market on time. Both companies see this as a necessary advancement of the supply chain model and we start off with the 14nm LPE as well as the 14nm LPP technology node." 14nm LPP is a follow-on offering which has additional performance enhancements as well as power reduction attributes.

Samsung had already developed much of the process technology for LPP and LPE flows to run using 14nm node finFETs, while GLOBALFOUNDRIES was working independently on another 14nm node process variant. The two companies decided to pool resources to save both time and money in bringing 14nm node finFET capability to the commercial IC foundry market.

"Because of customer interest in having that assurance of supply and being able to do one GDS and being able to work off of one common PDK and source at both of our companies, we

decided to work together and go with the 14 LPE and 14 LPP as common offerings between Samsung and GLOBALFOUNDRIES," said Ana Hunter, VP of product management at GLOBALFOUNDRIES.

Low said that Samsung is already running 14nm products in its fab in Korea. The 14nm LPE, for example, was qualified earlier this year.

"We are already in silicon validation of our lead customer products. We expect to ramp production by the end of this year," he said. Design activities started almost three years ago. "Right now, we are seeing a lot more pickup overall by the lead adopters and even other customers following suit, mainly because the marketplace does see that the 14nm FinFET is at the right maturity level for volume production," Low said.

Although there is still lot of activity at 28nm, the technology is considered to be in a mature phase. "We still continue to see healthy, new design-ins," Low said. "Of course, there are a lot of requests to see what additional enhancements we can do at our 28nm node to prolong the lifespan of that node."

What about 20nm? "From Samsung's viewpoint, we see that a relatively short-lived node, mainly because of the overall resonance of FinFETs and the eagerness of customers to migrate from 28nm directly to 14nm FinFETs."

Hunter agrees, noting that 28nm has been in high volume production for several years now. She said GLOBALFOUNDRIES does have 20nm product tapeouts running in the line, but said that she does not see 20nm being a very extensive node in that most customers are eager to get onto FinFETs.

"We do have products running at 20nm, but I think the design efforts will quickly go over to FinFET and we'll see that be a much longer lived node with a lot more product tapeouts," she said.

The companies say the 14nm FinFET offering could be up to 15% smaller than that available from other foundries due to aggressive gate pitch, smaller memory solution and innovative layout schemes for compact logic.

Hunter, having been a VP at Samsung before holding her current position at GLOBALFOUNDRIES, noted that the two companies, along with IBM, have been in collaboration for quite some time on "The Common Platform" at 65, 45, and 28nm nodes, but this announcement is strictly between GF and Samsung.

"We do continue to work with IBM in other areas at the Albany Nanotech center, where there is continuing collaboration on more advanced nodes, on materials research, pathfinding, and advanced module development kind of work," she said.

Fabless customers use a single PDK to do a single design, allowing a single GDS file to be sent to either company. The design-for-manufacturing (DFM) and reticle-enhancement technologies (RET) needed at the 14nm node are challenging.

"We go deep into the collaboration, even to the OPC level and a lot of sharing on DFM as well. It is a very extensive collaboration," confirmed Hunter. "At 14nm the designs are extremely complex, and to be able to truly supply multi-sourcing from one GDS, you have to have that level of collaboration to ensure that the output from all of our factories is the same. That's a huge advantage to customers because the idea that you could source from two different companies without the kind of collaboration that GLOBALFOUNDRIES and Samsung are doing is just simply impossible when you get into 14nm FinFETs. When you get into the complexity of the designs, the databases, the amount of reticle enhancement techniques that are required to be able to print these geometries, you need to have that kind of in-depth collaboration."

Low said that the two companies have a "fabsync" structure running in the background to ensure the fabs are fully synchronized.

"There are a couple of things we are doing proactively," he said. "The technology teams are deeply engaged with each other. We have technology workshops across both companies. We have test chips that are run regularly to ensure that the process continues to stay synchronized. These test chips are not just simple transistors. We have product level elements that we've included to make sure we measure the critical parameters. This is only enabled through open sharing of technology information."

Hunter adds: "We run the same test chips, we share wafers back and forth to measure each other's products to make sure all of our equipment is calibrated, test equipment calibrated, results are the same on exactly the same test chip.We have test-chips with product-level structures that run in all fabs and both companies share all data to ensure that all fabs stay in alignment. Not just SPICE models and SRAMs, but full chip-like design features."

However, customers will have to re-do lithography masks if they want to move manufacturing from one company to the other, in part because of issues with shipping masks. Kevin Low, Samsung's senior director of marketing, commented, "We'll be providing our customers choice and secure supply. At Samsung we have capacity in Texas and Korea."

Cost/transistor for 14nm may not be lower compared to 20nm and 28nm. Hunter said, "To continue with optical lithography, it is challenging to do double-patterning and keep costs low." However, since much of the motivation in moving from 20nm to 14nm is for power-sipping mobile SoCs, by reducing the power consumption by the claimed 35% there could be cost-savings at the packaging level such that the overall product cost is reduced.

To be able to offer essentially the same manufacturing process to customers, GLOBALFOUNDRIES and Samsung had to harmonize not just process recipes but many of the OEM tools used in these fabs.

Hunter says, "To get the same results at this node, it does require engineering down to the tool level and the individual recipe level. That doesn't mean all tools are exactly the same, however, since cost and availability of tools may have been different when the fabs were equipped."

Customers can choose which foundry that choose to work with, and then they can choose to discuss commercial terms such as which specific foundry site may be booked to do the work. ◁▶

By Ed Korczynski and Pete Singer, SemiMD and Solid State Technology

Samsung introduces new flip chip LED packages

Samsung Electronics introduced a new lineup of flip chip LED packages and modules offering enhanced design flexibility and a high degree of reliability. The new offerings, for use in leading-edge LED lighting such as LED bulbs, MR/PAR and downlights, will be available in the market during the second quarter of this year.

"By utilizing an advanced flip chip technology, Samsung has made significant improvements to its LED packages and modules," said Bangwon Oh, senior vice president, LED strategic marketing team, Samsung Electronics.

Samsung's new flip chip (FC) LED package and flip chip on module (FCOM) solutions feature highly efficient and versatile LED structures, created by flipping over blue LED chips and adhering phosphor film to each of them. Unlike conventional LED packages that dispense phosphor and then place a plastic mold over each chip, Samsung's FC package technology can produce LED packages down to a chip-scale size without any mold, enabling more compact lighting fixture designs.

Samsung's new FC and FCOM series can be driven at a current higher than that of conventional LED components, and have

low thermal resistance. The low thermal resistance improves the reliability of the FC and FCOM solutions, resulting in higher flux, and a decrease in the number of packages needed, plus a reduction in the size of the circuit board.

Also, by attaching a cell film, each package gains uniform thickness and lower color deviation. As a result, the FC and FCOM solutions provide a high level of color consistency and ensure the chromaticity control of MacAdam 3-step ellipses.

The new FC and FCOM LED solutions include a middle power LED package (LM131A), a high power LED package (LH141A) and an LED downlight module, all featuring the new Samsung flip chip technology.

Samsung's LM131A and LH141A flip chip packages feature exceptionally compact form factors of 1.22×1.22 millimeters and 1.4×1.4mm, respectively. By excluding a plastic mold, the two packages can function at a high current level in a highly reliable manner, even after long hour of use. These advantages make them ideal for use in LED lighting applications requiring a small form factor with high light output, including LED bulbs and spotlight products such as MRs and PARs.

In addition, the use of a phosphor film assures color quality that satisfies the MacAdam 3-step.

Samsung's new FCOM downlight products are distinguished by their high light output. Compared to a chip-on-board (COB) engine, which has a fixed wattage, the new FCOM permits simple adjustments in the number of FC LED packages to make the module compatible with a variety of electrical drivers of different wattages, in allowing greater design flexibility.

To create a downlight with 1000lm output and 100lm/W efficacy, Samsung FCOMs require a 1.7×1.7 centimeter circuit. Such a small form factor makes these FCOMs well-suited for size-sensitive LED lighting applications, which include LED bulbs, MR/PAR spotlights, downlights and even cove lighting.

Samsung's FCOMs satisfy the MacAdam 3-step and can support MacAdam 2-step, thanks to the color consistency of the chips and a rating of at least 80 on the color rendering index. The new Samsung FCOMs also offer a range of correlated color temperature – from 2700K to 5000K. ◆

Scientists build thinnest-possible LEDs to be stronger, more energy efficient

University of Washington scientists have built the thinnest-known LED that can be used as a source of light energy in electronics. The LED is based off of two-dimensional, flexible semiconductors, making it possible to stack or use in much smaller and more diverse applications than current technology allows.

"We are able to make the thinnest-possible LEDs, only three atoms thick yet mechanically strong. Such thin and foldable LEDs are critical for future portable and integrated electronic devices," said Xiaodong Xu, a UW assistant professor in materials science and engineering and in physics.

Xu along with Jason Ross, a UW materials science and engineering graduate student, co-authored a paper about this technology that appeared online March 9 in Nature Nanotechnology.

Most consumer electronics use three-dimensional LEDs, but these are 10 to 20 times thicker than the LEDs being developed by the UW.

"These are 10,000 times smaller than the thickness of a human hair, yet the light they emit can be seen by standard measurement equipment," Ross said. "This is a huge leap of miniaturization of technology, and because it's a semiconductor, you can do almost everything with it that is possible with existing, three-dimensional silicon technologies," Ross said.

The UW's LED is made from flat sheets of the molecular semiconductor known as tungsten diselenide, a member of a group of two-dimensional materials that have been recently identified as the thinnest-known semiconductors. Researchers use regular adhesive tape to extract a single sheet of this material from thick, layered pieces in a method inspired by the 2010 Nobel Prize in Physics awarded to the University of Manchester for isolating one-atom-thick flakes of carbon, called graphene, from a piece of graphite.

In addition to light-emitting applications, this technology could open doors for using light as interconnects to run nano-scale computer chips instead of standard devices that operate off the movement of electrons, or electricity. The latter process creates a lot of heat and wastes power, whereas sending light through a chip to achieve the same purpose would be highly efficient.

"A promising solution is to replace the electrical interconnect with optical ones, which will maintain the high bandwidth but consume less energy," Xu said. "Our work makes it possible to make highly integrated and energy-efficient devices in areas such as lighting, optical communication and nano lasers."

The research team is working on more efficient ways to create these thin LEDs and looking at what happens when two-dimensional materials are stacked in different ways. Additionally, these materials have been shown to react with polarized light in new ways that no other materials can, and researchers also will continue to pursue those applications.

A close-up view of a single layer of atoms of the semiconductor material, tungsten diselenide, on silicon oxide. The ability to see the contrast of the single layer of atoms against the background shows how strongly these materials interact with light.

Co-authors are Aaron Jones and David Cobden of the UW; Philip Klement of Justus Liebig University in Germany; Nirmal Ghimire, Jiaqiang Yan and D.G. Mandrus of the University of Tennessee and Oak Ridge National Laboratory; Takashi Taniguchi, Kenji Watanabe and Kenji Kitamura of the National Institute for Materials Science in Japan; and Wang Yao of the University of Hong Kong.

The research is funded by the U.S. Department of Energy, Office of Science, the Research Grant Council of Hong Kong, the University Grant Council of Hong Kong and the Croucher Foundation. Ross is supported by a National Science Foundation graduate fellowship.

IMAPS Device Packaging Conference

Dr. Phil Garrou,
Contributing Editor

This year's IMPAS Device Packaging Conference was held in Ft McDowell, AZ. Steve Bezuk, Sr. Dir. of Package Engineering for Qualcomm kicked things off with a talk titled "challenges and directions in mobile device packaging." Qualcomm expects 7 billion smartphone units to be shipped between 2012 and 2017.

Handset thickness continues to be reduced and is now approaching 6mm. Since the battery and the screen are not shrinking chip packaging and the substrate board must make up the difference. Most of these packages are FC and WLP. Bezuk commented that 5 years ago very few of the packages were WLP but now this category accounts for near 50% of the packages IC.

Molded FC die on thin core or coreless substrates are approaching 750um thick and warpage issues are becoming significant. Warpage is dependent on: core thickness, CTE and modulus; EMC thickness over die; die thickness (ratio of Si/EMC).

Solder balls have become a significant fraction of the total package height.

Tighter pitch requirements (< 140µm) have necessitated a move to copper pillar connections which in turn need thermocompression bonding to overcome warpage/flatness issues in such structures.

Thinner packages require thinner EMC above the die which results in increased warpage and requires EMC with higher mold shrinkage and higher modulus.

Having reached a core CTE of 3, reduction in substrate core CTE is no longer an option so the industry is turning to develop materials of increased modulus.

Bezuk proposed that the next move (time undefined) will be from today's FC PoP structures to 2.5/3D moving first to wide IO DRAM on logic and next to logic-on-logic. Although he added that there was no clear infrastructure answer for where interposers will be coming from.

PRISIMARK

Brandon Prior of Prismark continued on the theme of "Mobile packaging and Interconnect trends." Their analysis of the Apple 5S smartphone confirms the Qualcomm comments about increased use of WLP.

Despite all the talk about high density laminate technology approaching < 5µm L/S, Prior indicated that the Apple 5S was the first device to use 50µm L/S and CSPs on a 0.4mm pitch. It is also interesting that caps continue to shrink. 01005 is 0.4 x 0.2 x 0.13mm which is extremely hard to assemble.

The Apple A7 processor is packaged in PoP with the memory package being 1Gb of LPDDR3. The substrate has 27µm L/S and 150/170µm bump pitch. Memory chips are Ag WB which is a lower force assembly process than Cu WB. While these memory chips are still WB, Prismark stated that they expect performance DDR to go FC at the big 3 memory suppliers and expect 5B units shipped by 2018.

FBGA and WLP are in high volume production at 0,4 and 0.35mm pitch. Wafer CSP moving to 0.3mm and below. Prismark forecasts > 28% of CSP/WLCSP to be 0.4mm or less by 2018.

AMD

AMD's keynote presentation by Bryan Black updated us on their thoughts about "Die Stacking and High Bandwidth Memory." Black stated that "while die stacking is catching on in FPGAs, Power Devices, and MEMs, there is nothing in mainstream computing CPUs, GPUs, and APUs …HBM Stacked DRAM will change this!" Black agrees that future nodes will no longer bring down transistor costs which has been a longstanding premise of Moore's Law.

Black adds that die partitioning is challenging and there is significant microarchitectural research to be done since the buss to connect partitioned chips is very complex.

STATSChipPAC

In an attempt to expand the usage of their eWLB technology, STATSChipPAC (SCP) announced FlexLine as a "breakthrough manufacturing method for wafer level packaging". Currently, separate equipment sets are required to manufacture WLCSP from 200 or 300mm wafers whereas the FlexLine process allows them to be manufactured on the same equipment set. ◆

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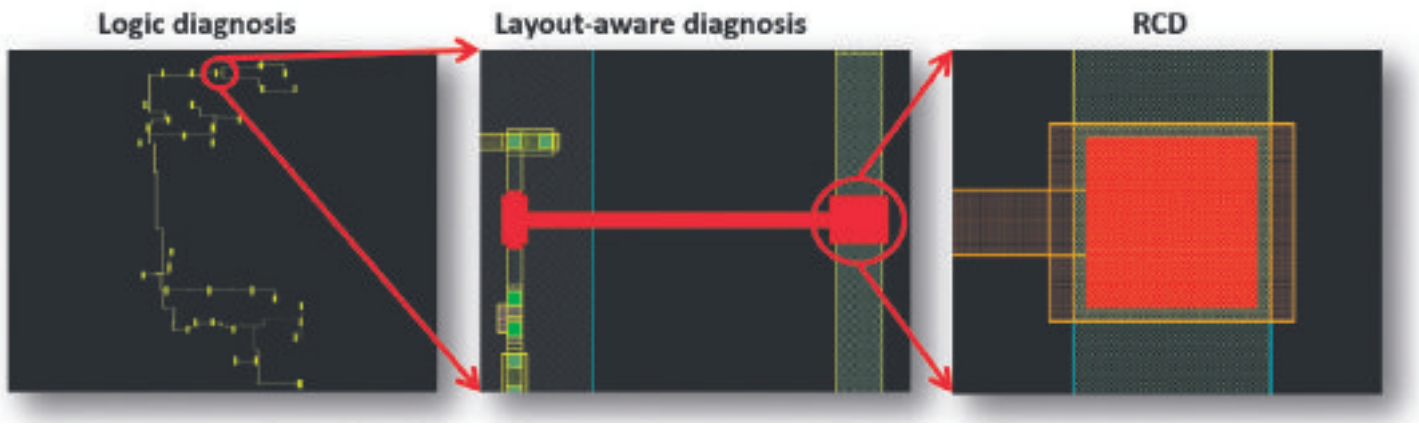

FIGURE 1. Layout-aware diagnosis improves scan diagnosis resolution to a net segment. Root Cause Deconvolution (RCD) leverages statistical enhancement to identify the underlying root cause, in this example, an open VIA defect.

Learn more about RCD as the next step in diagnosis solution enhancement. Where layout-aware diagnosis points to a segment, learn more about RCD as the next step in diagnosis solution enhancement. Where layout-aware diagnosis points to a segment, RCD can isolate a particular root cause in that segment. RCD, a statistical enhancement technology in Tessent Diagnosis and YieldInsight products, is the next step in diagnosis resolution enhancement. It works by analyzing multiple layout diagnosis reports together to identify the underlying defect distribution that is more likely to explain this set of diagnosis results. RCD does not require any additional data beyond what is required for layout-aware diagnosis. This means that RCD fits well into existing diagnosis flows.

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Will interconnect requirements cramp Moore's Law?

Vidhya Ramachandran, Advanced Interconnect Technology Engineer, Qualcomm Technologies

The recent years have seen considerable contention in the semiconductor industry on whether Moore's Law is alive and well.

The impact of on-chip interconnect cost on advanced node technology products, in particular, has generated much discussion and, some would say, discontent. Beyond 28nm, BEoL cost and complexity projections show an explosion and at the upcoming 10nm node, on-chip interconnect costs are projected to exceed 50% of the SoC cost. Technologists from multiple functions in the semiconductor industry have to come together to address this issue, as will be evident at the Workshop "Manufacturing of Interconnect Technologies: Where Are We Now And Where Do We Go From Here?" to be held prior to the International Interconnect Technology and Advanced Metallization Conference (IITC/AMC) on May 20 in San Jose.

Particularly challenging at the 10 nm and 7 nm nodes is lithography. The incumbent is 193i technology, which is now being used to print significantly sub-wavelength features. At the 20nm node this has been accomplished by double patterning, but approaching 7 nm this will require triple patterning, a new wavelength (e.g. EUV), or some other disruptive technology. This, in addition to a steep rise in the number of metal layers in order to route a higher density of transistors and more complex circuitry, influence mask count, process complexity and cycle-time, directly hitting at the heart of cost and yield. Photolithography researchers from GLOBALFOUNDRIES will review advancements in lithography that enable solutions for these issues at the IITC/AMC Workshop.

Many new materials are being introduced to meet RC requirements, such as lower K insulators and thinner and self-formed metal barrier layers. These implementations are not stand-alone changes, but come hand-in-hand with their respective versions of etch, CMP, cleans and so on, moving into new process condition regimes. While these modules pose challenges in development, in manufacturing, where thousands of wafers could be at risk from a single process going out of control, new materials can be particularly problematic. These challenges are driving development of innovations in the methodology for introduction of new materials and processes, process control and yield management for advanced technologies at several industry leaders. New defects and failure mechanisms are being discovered and solved; new metrology methods are enabling more robust process control; and pervasive implementation of automated process control (APC) prevents process excursions.

As we are well-aware, aspects of semiconductor manufacturing that could act independently in the past such as design and process now have to work closer together throughout the entire life-cycle of a product, from conception to manufacturing ramp. We increasingly find that successful manufacturing is driven by "yield-aware" design, with robust follow-up between designers and manufacturers during the fabrication phase. Designers from ARM highlight the interconnect-related challenges of implementing their high performance cores in SoCs at 16 nm and beyond.

With the acute focus on challenges in interconnect manufacturing with meeting Moore's Law projections, interconnect technologists have their work cut out for them. However, the upside is that there is plenty of opportunity for innovation across the board. Some of this will be in evidence at the Panel Discussion to follow the IITC/AMC Workshop, where industry leaders will share their perspectives on how the industry will meet these challenges while remaining cost competitive. As we know, semiconductor engineers are a resourceful lot, and we look forward to all the exciting developments in store for us! ◆

New materials and processes for advanced interconnects

PETE SINGER, *Editor-in-Chief*

Although on-chip interconnects have not been scaling at the same speed as other parts of the chip, new capabilities enabled by graphene and CNTs, among other materials, could soon change that.

Transistor speed used to be the limiting factor for chip performance, but increasingly on-chip or Back End of Line (BEOL) interconnects have become a limiting factor. While transistors and other aspects of ICs have been continually made smaller, interconnect scaling essentially stopped at the 20nm node. In part, this decision was made to save costs (i.e., reuse masks and avoid more complex lithography steps). There was also concern about implementing too many major changes at the same time. "When you have ten layers of metal and let's say six layers of those are close to minimum pitch, it gets very expensive once you start doing double patterning," said Dr. Deepak Chandra Sekar, general co-chair of the upcoming 2014 IITC/AMC joint conference. "With the interconnect layers, people want to save litho costs. That's one reason they are not scaling as much as they used to."

The major reason is that it's difficult to make interconnects much smaller without introducing significant increases in resistivity. "If you scale down and your resistivity goes up exponentially, it can be a problem," Sekar said. "Copper resistivity shoots up when you scale it down because of surface scattering, grain boundary scattering and interface roughness." It's well known that the electrical resistance (R) of the wires, or lines, increases as they are made thinner. It also arises because capacitive coupling (C) can occur among adjacent lines spaced very closely together. Speed or frequency is directly related to the inverse of the RC time constant ($f_c = 1/2\pi RC$).

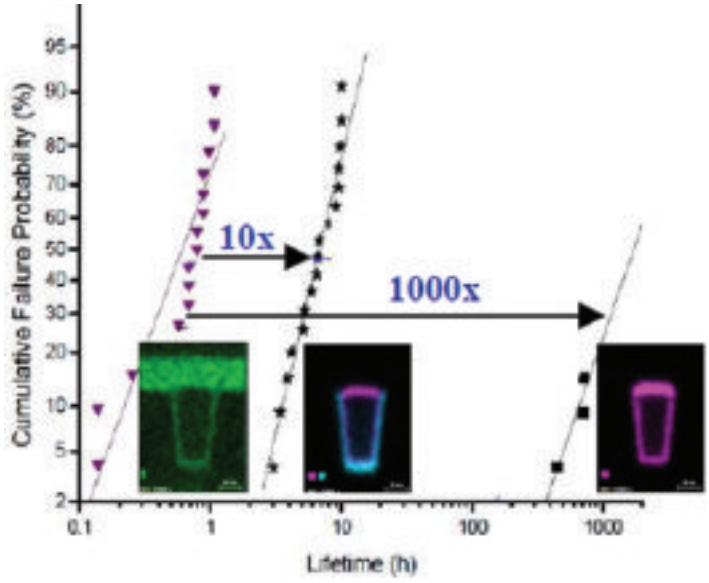

FIGURE 1. Work at IBM and Applied Materials showed a 10x improvement in electromigration lifetimes with multi-layer SiN and selective cobalt cap layers. 1000x improvement in electromigration lifetimes with multi-layer SiN cap, cobalt cap and wrap-around cobalt liners.

Two upcoming conferences are worthy of special note: IITC/AMC and IRPS. The 17th annual International Interconnect Technology Conference (IITC) will be held May 21 – 23, 2014 in conjunction with the 31st Advanced Metallization Conference (AMC) at the Doubletree Hotel in San Jose, California (http://www.ieee.org/conference/iitc). It will be preceded by a day-long workshop on "Manufacturing of Interconnect Technologies:

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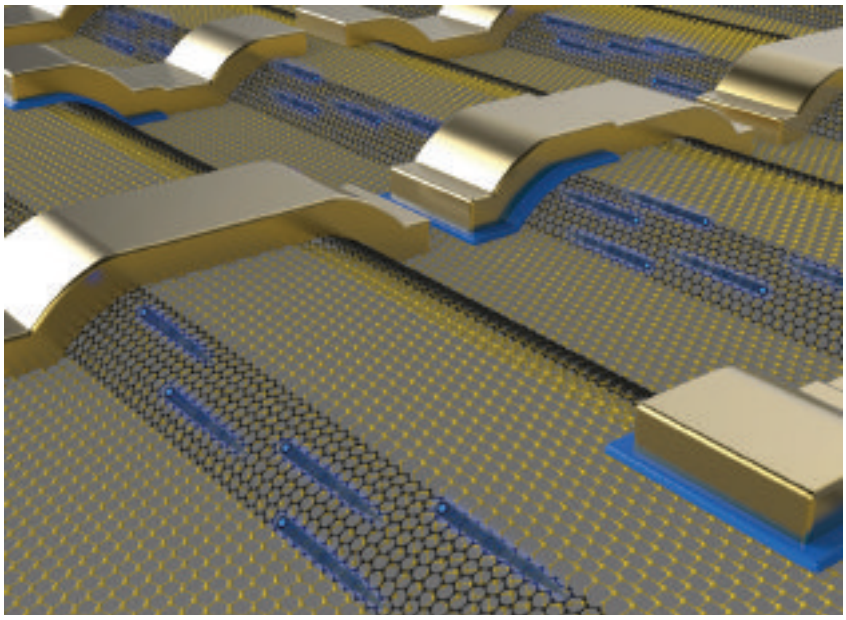

FIGURE 2. Conceptual drawing of an electronic circuit comprised of interconnected graphene nanoribbons (black atoms) that are epitaxially grown on steps etched in silicon carbide (yellow atoms). Electrons (blue) travel ballistically along the ribbon and then from one ribbon to the next via the metal contacts. Electron flow is modulated by electrostatic gates. (Courtesy of John Hankinson, Georgia Tech).

Where are we now and where do we go from here?" on Tuesday, May 20. The International Reliability Physics Symposium (IRPS) will be held June 1-5 at the Hilton Waikoloa Village, Waikoloa, Hawaii (www.irps.org).

Reliability is important because it's another challenge to scaling of interconnects. Both time-dependent-dielectric-breakdown (TDDB) and electromigration lifetimes for interconnects drop rapidly when scaled.

At both IITC/AMC and IRPS, a variety of papers will be presented that look at new materials that could enable continued scaling of conventional interconnects, while also addressing reliability challenges. These range from tweaks to existing processes to radically new strategies that could provide a viable alternative to copper/low-k.

At IITC/AMC, for example, IBM and Applied Materials will present a multi-layer SiN cap process is developed that shows higher breakdown and lower leakage compared to conventional SiCNH caps **(FIGURE 1).** Selective cobalt caps in combination with the multi-layer SiN cap are shown to provide a 10x improvement in electromigration lifetimes. Wrap-around cobalt liners in combination with the cap layer schemes are shown to provide a 1000x improvement in electromigration lifetimes. The paper is titled "Advanced Metal and Dielectric Barrier Cap Films for Cu Low k Interconnects."

Graphene and CNTs

Further out, it appears is if graphene hold tremendous promise as a possible replacement for copper. In work reported earlier this year by Georgia Institute of Technology, it was shown that electrical resistance in nanoribbons of epitaxial graphene changes in discrete steps following quantum mechanical principles **(FIGURE 2)**. The research shows that the graphene nanoribbons act more like optical waveguides or quantum dots, allowing electrons to flow smoothly along the edges of the material. In ordinary conductors such as copper, resistance increases in proportion to the length as electrons encounter more and more impurities while moving through the conductor.

The ballistic transport properties, similar to those observed in cylindrical carbon nanotubes, exceed theoretical conductance predictions for graphene by a factor of 10. The properties were measured in graphene nanoribbons approximately 40nm wide that had been grown on the edges of three-dimensional structures etched into silicon carbide wafers. "This work shows that we can control graphene electrons in very different ways because

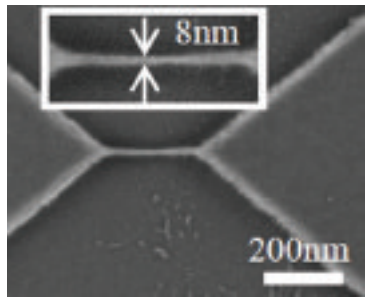

FIGURE 3. Work 8nm wide graphene interconnects.

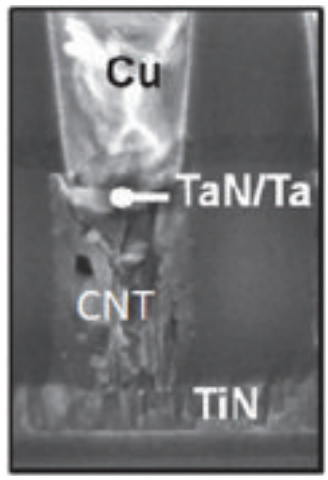

FIGURE 4. Carbon Nanotube (CNT) vias in integrated structures.

the properties are really exceptional," said Walt de Heer, a Regent's professor in the School of Physics at the Georgia Institute of Technology. "This could result in a new class of coherent electronic devices based on room temperature ballistic transport in graphene. Such devices would be very different from what we make today in silicon."

Sekar also highlighted a number of papers that will be presented this year that focus on new materials that could lead to reduced resistivity and enable further interconnect scaling. "There is a lot of excitement about carbon and carbon-copper composites eventually replacing copper," he said. "At IITC this year, we have a couple of papers, one on graphene showing lower resistivity than copper, and then one on carbon nanotubes showing good resistivity as well. They are still a bit far out in the sense that there's a lot more process integration work that needs to be done because these are proof of concept demos, but they show that there might be more beyond copper."

In a paper from AIST, titled "Sub 10nm wide intercalated multi-layer graphene interconnects with low resistivity," work will be presented that demonstrates 8nm wide 6.4nm thick graphene interconnects with a resistivity of 3.2uohm-cm **(FIGURE 3)**, which is significantly better than copper with similar dimensions. This milestone for graphene interconnect research is expected to motivate the process integration research that is required to take the technology to the next level.

Carbon nanotubes (CNTs) have been explored as a material for vertical interconnects for many years since they can handle higher current densities than copper and offer ballistic transport. A paper from imec titled "Electron Mean Free Path for CNT in Vertical Interconnects Approaches Copper," work will be presented that demonstrates a 5x improvement in electron mean free path for CNTs compared to previous work **(FIGURE 4)**. The CNT mean free path of 24-74nm approaches copper. Contact resistance is improved significantly compared to previous work as well.

3D integration

Of course, an alternative to making everything smaller by scaling is to go 3D. That will be addressed by a variety of papers, including one from CEA-Leti focused on 3D monolithic integration. While most of today's through-silicon vias (TSVs) are in the 5µm range, monolithic 3D technologies offer

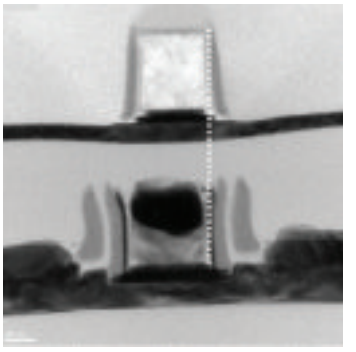

FIGURE 5. Monolithic 3D-ICs produced by Leti.

TSVs in the 50nm range, which allows dense connectivity between different layers in a 3D-IC. In the Leti paper, such dense connectivity is shown to provide 55% area reduction and 47% energy-delay product improvement for a 14nm FPGA design **(FIGURE 5)**. Transistor technologies that allow monolithic 3D integration are experimentally demonstrated. "When you make the TSVs smaller and smaller, you can reduce the length of on-chip wires as well by taking what's on a single now and stacking them into two layers," Sekar said. "That might save a lot of power and area. There's been a lot of talk about monolithic 3D, but these are some of the first few experimental demonstrations showing that it's possible."

Through Silicon Vias (TSVs), an important component of 3D chip stacking technology, typically have a "keep-out zone" around them, where transistors are not placed. This is due to co-efficient of thermal expansion mismatch between the copper TSVs and silicon, which introduces tensile stresses in the silicon and changes transistor performance. These keep-out zones are typically >7µm, which adds constraints for design and leads to die size penalties.

In work from GLOBALFOUNDRIES, a CMP stop layer is specially designed such that it introduces compressive stresses on the silicon and compensates for the tensile stresses introduced due to copper TSVs **(FIGURE 6)**. The result is a near-zero keep-out zone for TSV technology, that is validated with simulations as well as experiments.

Silicon photonics

Perhaps the ultimate ways of sending signals is not with electrons but with photons. Optical interconnects are already in use in telecommunications, and have been implemented at the backplane level on computer systems. Someday, we could see chip-to-chip level optical communication, and perhaps even on-chip.

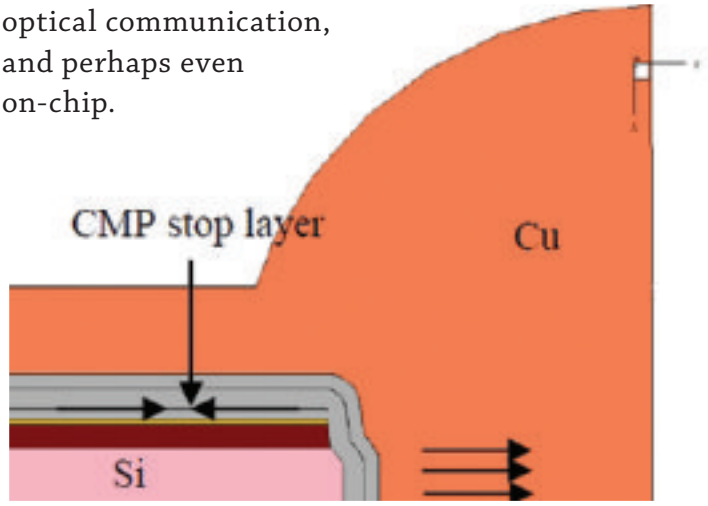

FIGURE 6. Copper shrinkage results in tensile stress in the silicon while CMP stop layer shrinkage results in compressive stress in the silicon.

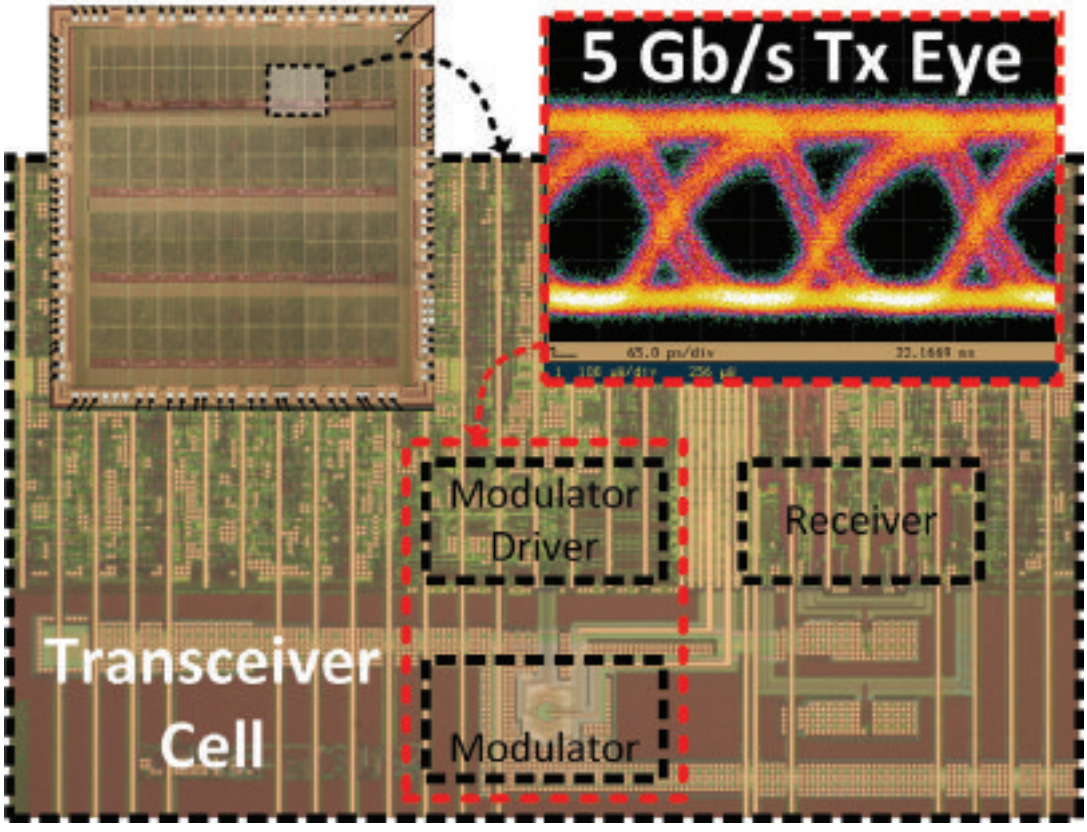

FIGURE 7. At the VLSI Symposium, Micron Technology will describe the first monolithic silicon-photonics-on-bulk-CMOS process flow to connect distant distributed memories.

At IITC, the first talk after the plenary talk is title "Nanophotonic and Interconnects - Status and Future Directions," and will be delivered by one of the original pioneers in the field, David A.B. Miller, who runs the Ginzton Laboratory at Stanford University. "Optical interconnects at progressively shorter distances and higher communications densities demand novel optics and very low operating energies. Optoelectronics with femtojoule or lower energies and compact custom and self-designing optics may enable the lower energy per operation and higher bandwidth density required for continued scaling of information processing, with significant potential impact for systems," Miller says in his summary.

The upcoming Symposia on VLSI Technology & Circuits (http://www.vlsisymposium.org/), scheduled for Honolulu from June 9-12 (Technology) and June 10-13 (Circuits). Of particular note is a highlighted paper from researchers at Micron Technology describing the first monolithic silicon-photonics-on-bulk-CMOS process flow to connect distant distributed memories **(FIGURE 7)**. Features include deep-trench isolation, polysilicon waveguides, grating couplers, filters, modulators, and detectors. Fully functional on-chip CMOS enables transmit/receive operation while minimizing interconnect parasitics. With the addition of an external 1280-nm light source, a fully functional optical link (5 Gb/s with 2.8 pJ/b), capable of WDM (wavelength division multiplexing), has been demonstrated. In addition to the polysilicon resonant detector used in the link, a monolithically integrated SiGe-based photodetector using selective epitaxial growth was also developed.

The basics of copper, low-k and 3D interconnects

Copper lines offer less resistance and higher current-carrying capability than the previously used aluminum lines, but at small geometries surface scattering effects increase the effective resistivity, which has led to interest in alternative conductors such as graphene and carbon nanotubes. Standard silicon dioxide insulator (or dielectric) around the lines creates a high parasitic capacitance at narrow spacings with concomitant signal delays and increased power consumption. This had led to the introduction of and continued search for substitute materials. A dielectric's relative permittivity is expressed as "k." The lower the k, the faster the signal propagation speed and the lower the power consumption. (Vacuum, the perfect low permittivity material, has k=1; silicon dioxide has k~4.) The challenge with dielectric materials with very low k-values is that they are porous and generally more fragile than oxide dielectrics. Carbon-doped oxide (or SiCOH) low k dielectrics can be easily damaged by typical chip-making processes such as exposure to harsh plasma during photoresist-stripping and to chemical-mechanical polishing, used to planarize each interconnect layer.

The semiconductor industry introduced the first carbon-doped low k dielectrics with k~3 in the 90nm technology node. The 45/40nm nodes saw introduction of enhanced SiCOH low k (k~2.7) and early porous ultra low k (ULK, k~2.4). The 32/28nm nodes developed mechanically robust ULK films (k~2.5) which are becoming pervasive in the 22nm technology entering early production. Focus in the 20nm and 14nm nodes has been on patterning challenges but research and development on dielectrics with enhanced mechanical properties and extreme low k (k~2) remains active. Additionally, at the advanced technology nodes' smaller dimensions, there is an increased focus on new materials and processes to improve the reliability and manufacturability of copper based interconnects. These include barrier, seed, copper filling, and capping technologies.

The electronics industry continually strives to place more functions in the same size or smaller packages. One way to do that is with 3D integrated circuits, where individual chips are thinned (usually), stacked and then interconnected so they function as a single unit. These stacks are challenging to fabricate, and despite much progress in recent years the industry is still trying to determine the best ways to accomplish 3D interconnect architecture.

There are a variety of 3D techniques under consideration, but many of them require the etching and filling of relatively large, deep holes through the backside of the wafer, called through-silicon-vias, or TSVs. Processes such as deep etching, highly conformal insulator deposition, and high-aspect-ratio metal fill are needed to create these TSV structures.

Source: IITC/AMC conference committee.

In-line high-κ/metal gate monitoring using picosecond ultrasonics

CHUN WEI HSU, *United Microelectronics Corp., Tainan City, Taiwan;* **JOHNNY DAI**,*Rudolph Technologies, Inc., Budd Lake, New Jersey, USA*

Only a direct measurement of SRAM structures can represent true variations of metal gate height due to CMP process and is strongly affected by the design and layout of pattern, including pattern density, dummy design, and spacing.

The pursuit of Moore's law has dictated the scaling of semiconductor devices and has led to successful shrink of device form structures while delivering significant transistor performance improvements. In order to keep pace with the need for improved performance, new materials and new process integration schemes have been developed. High-K/metal gate technology, introduced by Intel to replace the conventional oxide gate dielectric and polysilicon gate, has truly revolutionized transistor technology more than any other change over the last 40 years. First introduced at the 45nm node, this complex process has now been adopted for advanced nodes as the primary approach to address gate leakage and the reduction in gate capacitance due to poly Si gate electrode depletion issues [1].

Two main integration schemes have been adopted by device manufacturers. The gate first approach (also known as Metal-Inserted Poly Si-MIPS) is similar to the oxynitride/poly process flow and is the preferred method for applications that require lower power that do not need the aggressive scaling of gate thickness [2,3]. The gate last approach (also known as Replacement Metal-Gate or RMG) takes advantage of strain enhancement techniques, such as e-SiGe, and a poly Si removal step and significantly improves hole mobility, making RMG an attractive option for high performance applications. The replacement metal gate approach includes two chemical mechanical polishing (CMP) steps. One is the poly opening polish (POP) process before dummy poly removal and the second is the aluminum CMP (AlCMP) process after work function metal deposition. Known concerns with this AlCMP process are Al dishing/erosion, gate height uniformity control and introduction of various types of defects that affect the performance and yield of the

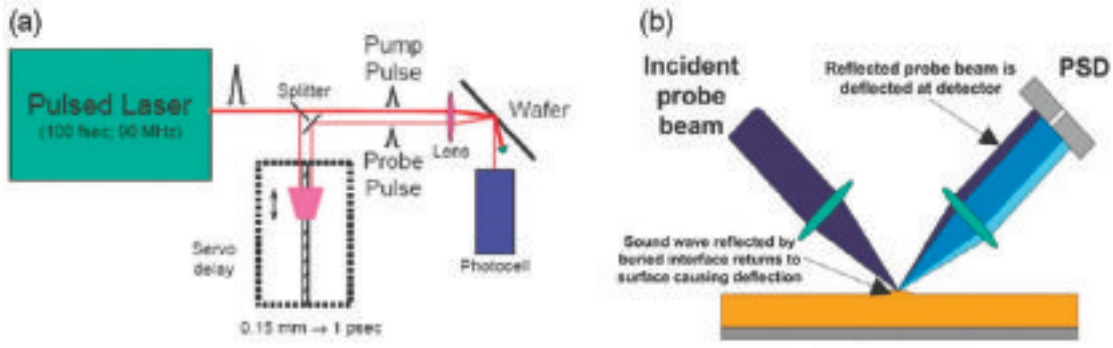

FIGURE 1. (a) Schematic representation of the PULSE set up and (b) position sensitive detection (PSD) method.

CHUN WEI HSU *is a principle engineer at United Microelectronics Corp., Tainan City, Taiwan.* **JOHNNY DAI** *is a system scientist V, Rudolph Technologies, Inc., Budd Lake, New Jersey.*

final device [4]. Control of gate height and uniformity is critical to transistor performance and precisely controlling this height is the primary challenge for the replacement metal gate AlCMP process. Non-uniform gate height can cause gate resistance variation which results in parametric issues for the device. Thinner gate heights can result in over etched contacts [5]. The dimensional tolerance of the AlCMP process is much more challenging (10 times tighter) than the conventional CMP process because the metal gate height is only several hundred Angstroms [6]. Hence, in-line gate height monitoring is necessary for RMG to control gate resistance and avoid over etched contacts.

In this article we evaluate the capability of picosecond ultrasonic sonar measurements for in-line monitoring of high- /metal gate structures and demonstrate the benefits of this technology for measuring various structures, including SRAM, pad array, and line array key, with excellent correlation to cross sectional transmission electron microscopy (TEM). We have shown that only a direct measurement of SRAM structures can represent true variations of the metal gate height due to CMP process and is strongly affected by the design and layout of pattern, including pattern density, dummy design, and spacing. The small spot, non-contact, and non-destructive nature of this technology allows for in-line measurements directly on these structures with excellent repeatability at a very high throughput.

Picosecond ultrasonic measurements

The Picosecond ultrasonic technology (PULSE) is a unique way of measuring opaque film thickness using an ultra-short pulsed laser. Because the technique is non-contact and non-destructive, it can be used directly on product wafers. In addition to thickness measurements, it can measure parameters such as roughness, density, phase and modulus to provide additional information about the process.

FIGURE 1a shows the optics layout of this technology. The system uses a pump-probe measurement technique. A 0.1ps pump laser pulse focused into a 5 7 m2 spot on the wafer surface induces a sharp acoustic wave that travels away from the surface through the film at the speed of sound. At each interface between layers a portion of the acoustic energy is reflected back toward the surface while the rest is transmitted. When the

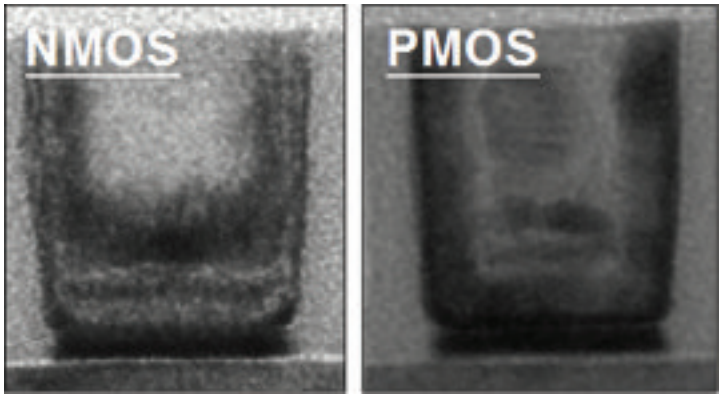

FIGURE 2. TEM cross-section of product wafers generated for characterization using picosecond ultrasonic measurements.

reflected acoustic wave reaches the wafer surface, it is detected by a probe laser pulse, which was diverted from the pump pulse by a beam splitter and routed through a servo-controlled delay circuit to introduce a known variable delay.

There are two different methods of detecting the arrival of the reflected acoustic wave at the surface. The first method is to detect the change of optical reflectivity caused by the strain of acoustic wave. The second method is to detect the deflection of the reflected probe beam that is caused by the deformation of surface due to the acoustic wave. The second method requires a position sensitive detector (PSD) as shown in **FIGURE 1b**.

The PSD method shows better sensitivity and signal-to-noise for measuring thick copper and line array structures. Data reported in this article takes advantage of both measurement methods. The servo-delay controls the time difference between pump and probe, allowing accurate measurement of the round trip travel time of the acoustic wave within the film. Multiplying the one way travel time (half of the roundtrip time) by the speed of sound in the material yields the layer thickness (equation 1). The thicknesses of component layers of a multi-layer film stack can be calculated similarly from the analysis of multiple return echoes from a single measurement.

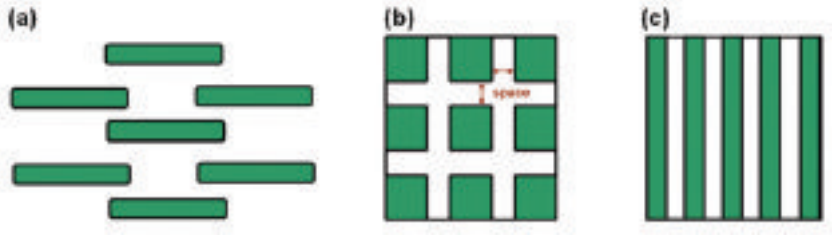

FIGURE 3. Schematic representations of measurement sites (a) SRAM, (b) Pad array (c) Line array key.

(1) $d=(v)(t)/2$

where d is the film thickness in Å, v is the speed of sound in the material in Å/ps and t is the transit time in ps.

Thickness is calculated from first principles and does not require calibration standards or reference wafers. Calibration of the system relies primarily on the positional accuracy of the delay stage. This is calibrated using optical encoders and corresponds to 1-1.5Å of the film thickness. This level of intrinsic matching allows for easy system-to-system matching across wafer fabs.

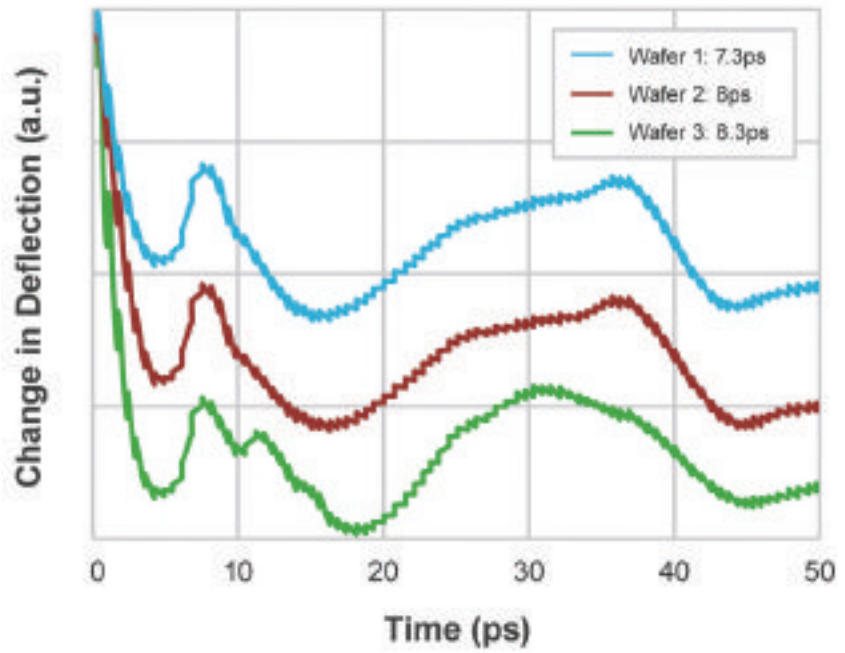

FIGURE 4. Raw data showing change in deflection versus time. The measurements are from DOE skew wafers of varying thickness from the SRAM structure. The large zero peak is the pump laser pulse and the next peak to the left is the first returning echo. The time elapsed to the first echo is seen to increase for the three wafers, corresponding to known increases in thickness.

Experimental

Product wafers including a nominal stack of PVD Al film/ CVD Al seed layer/ PVD Ti wetting layer/ N or P MOSFET work function metals/ TaN etch stop layer/ CVD oxide film/ Si-substrate were prepared **(FIGURE 2)** to systematically study the effects of CMP processes on the stack, specifically, characterization of metal gate height loss and Al metal dishing followed by defect analysis. The AlCMP process was carried out on a rotary type polisher with three polishing platens. Multiple sets of wafers (different products) with varying thickness skew were generated to test the capability of the picosecond ultrasonic technique to measure a wide variety of structures: SRAM, pad array, and line array key (commonly measured by CD metrology tools). The arrays are shown schematically in **FIGURE 3**. The SRAM structure, although challenging

with only 40% metal density, was selected to provide information on true process variation. Pad arrays (75% metal density) and line array keys (50% metal density) were also chosen to provide a comparison with the SRAM structure and to help determine the extent of pattern dependent variations in CMP rates. Structures for both N well and P well stacks of varying array widths were investigated.

Results and discussion

FIGURE 4 shows the raw timing data of a PULSE measurement from a center die on three thickness skew wafers. The time elapsed between the pump pulse and the returning echoes, 7.3ps, 8.0ps, and 8.3ps, can be used to calculate the thickness of the layers (Al gate+work function). Longer times indicate thicker films. Unlike other spectroscopic metrology technologies, which require sophisticated modeling and calibration, picosecond ultrasonic technology provides a simple, direct measurement of thickness.

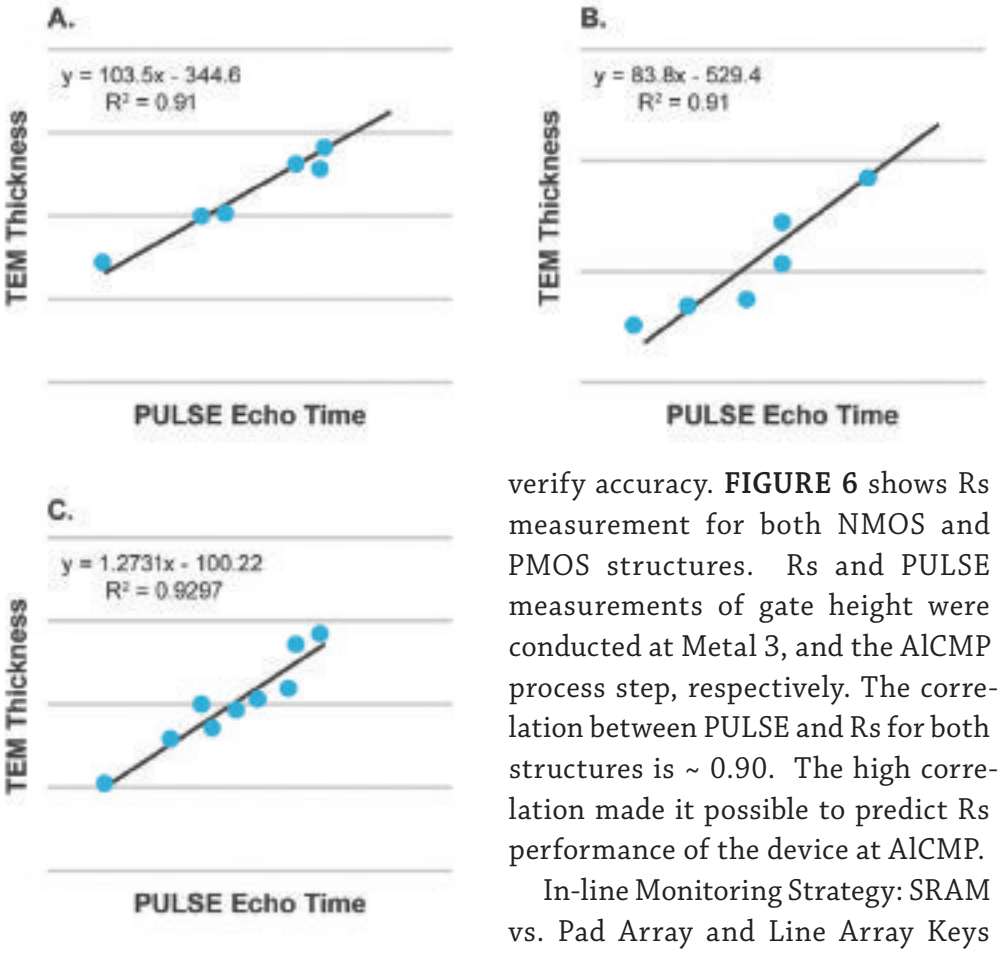

FIGURE 5. Correlation of PULSE vs TEM measurements of (a) SRAM (b) Pad array and (c) Line array.

The accuracy of PULSE measurements for a wide thickness range of all three different structures was verified by comparison to measurements made on cross sectional TEM images. **FIGURE 5 (a), (b) and (c)** show the correlation between picosecond ultrasonic measurements and TEM on SRAM, pad array and line array keys, respectively. Correlation with TEM is excellent for all three structures (R2> 0.9).

PULSE measurements were also compared to resistivity (Rs) measurements to verify accuracy. **FIGURE 6** shows Rs measurement for both NMOS and PMOS structures. Rs and PULSE measurements of gate height were conducted at Metal 3, and the AlCMP process step, respectively. The correlation between PULSE and Rs for both structures is ~ 0.90. The high correlation made it possible to predict Rs performance of the device at AlCMP.

In-line Monitoring Strategy: SRAM vs. Pad Array and Line Array Keys Pad arrays, nominally grids of pads with NMOS structure, or line array keys of varying metal density, are typically used for metrology thickness measurements but provide only an indirect indication of gate height. This study was specifically designed to evaluate picosecond ultrasonic technology's capability to measure SRAM structures as a direct monitor of gate

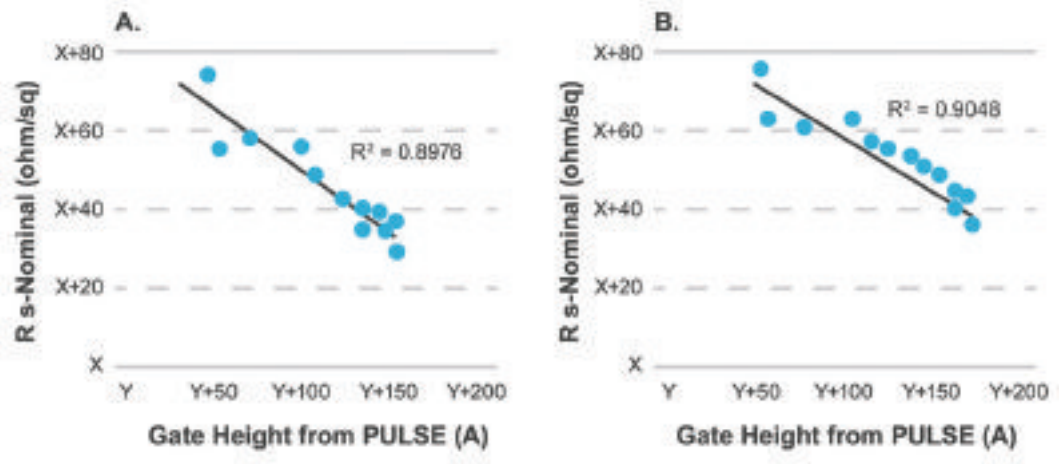

FIGURE 6. Resistivity measurements vs picosecond ultrasonic gate height measurements showing excellent correlation on both (a) NMOS and (b) PMOS devices.

height, and, if successful, to adopt this strategy for in-line monitoring.

Direct measurement of gate heights in SRAM is complicated by the multilayer structure of the NMOS and PMOS devices, which have different work function metals and cross single trench isolation areas that introduce gate height variations. Given the complexity of the stack, concerns also exist regarding the accuracy and reliability of the measurement for in-line use. Measurements on pad and line array keys can only serve as an indirect measurement due to well-known pattern dependent variations in polishing rates. CMP rates are known to be affected by variations in design and layout of the pattern, differences in surrounding areas between grid pads and SRAM, pattern density differences, and effects of a dummy design, all of which can impact thickness measurement on the pads and arrays but does not represent the behavior on the SRAM structure.

Direct picosecond ultrasonic measurements of gate height within the SRAM are feasible and show excellent correlation with TEM and resistivity measurements. Moreover, since the measurements are fast (<2 seconds), PULSE technology allows for sampling of more structures and die on the wafer to better characterize uniformity across wafer. The wafers show very similar profiles and the measurements can help process engineers better understand sources of within wafer variation. These measurements provide useful information for process optimization especially during development.

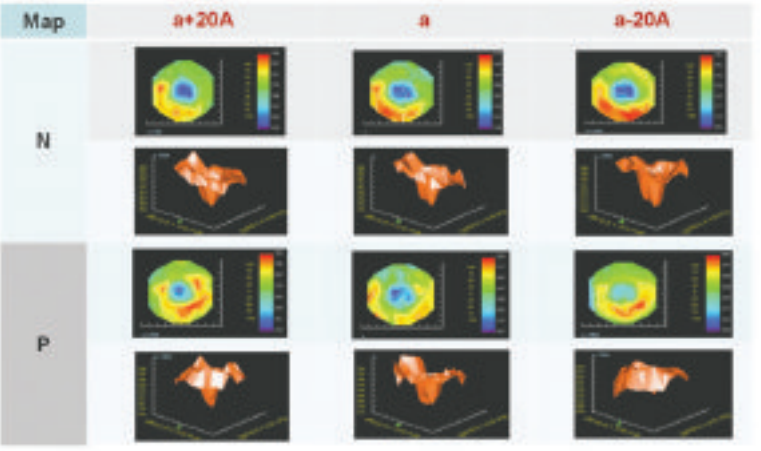

FIGURE 9. Full wafer maps of both NMOS and PMOS devices.

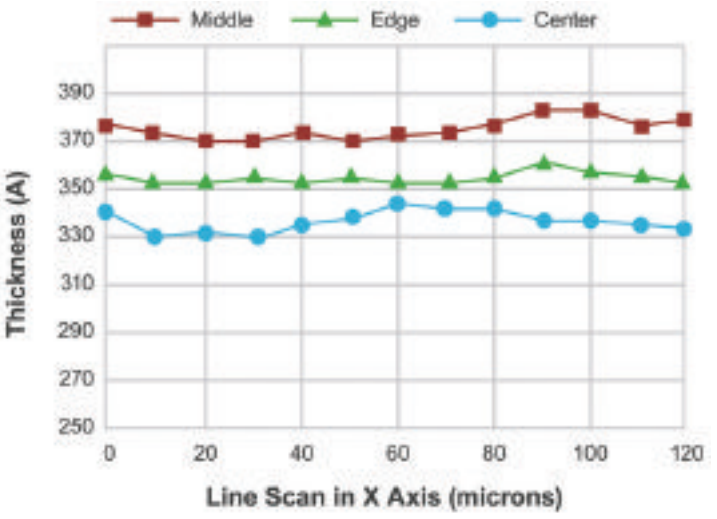

FIGURE 8. High resolution line scan profiles from center, mid and edge die on an SRAM structure.

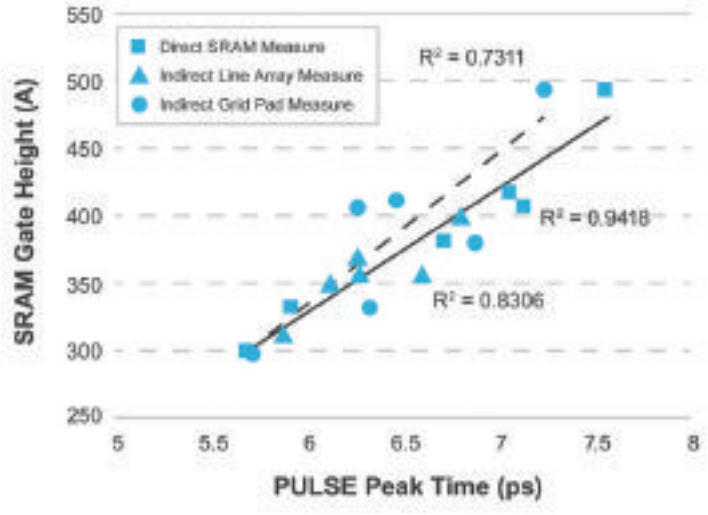

FIGURE 7. Correlation between SRAM gate height vs. PULSE for various structures.

FIGURE 7 shows the correlation between the SRAM gate heights as measured by TEM and PULSE thickness measurements for the various structures. PULSE measurements made directly on SRAM structures show excellent correlation (R2 = 0.94) with SRAM gate height.

Additionally, high resolution scans were performed across the SRAM structures to characterize dishing/erosion profiles. **FIGURE 8** charts the measurements on center, mid and edge die showing the thickness profiles and variations. In general, the wafers showed identical profiles on the three die. Thickness variation was ~20Å within the structure. **FIGURE 9** provides details full wafer maps for both NMOS and PMOS devices. The data collected on these structures was used to better understand the within wafer profiles and guide process optimization.

Finally, measurement repeatability and stability

were evaluated. **TABLE 1** summarizes the results of dynamic (wafer load/unload) repeatability testing performed on SRAM structures across nine sites on a test wafer. The standard deviation is < 0.5% at each site and < 0.2% for the wafer average. **FIGURE 10** shows results of measurement stability over a 10 day period when measuring daily production monitor wafers.

Run	PT1	PT2	PT3	PT4	PT5	PT6	PT7	PT8	PT9	Average	Stdev
1	a+42.4	a+27.1	a-11.8	a+10.4	a+24	a+11.9	a+19.9	a+35.4	a+17.8	a+19.7	15.7
2	a+43.2	a+27.5	a-11.2	a+10.6	a+25.8	a+12.4	a+20.3	a+35.8	a+18.7	a+20.3	15.8
3	a+43.8	a+27.8	a-11.7	a+10.3	a+25.1	a+12.5	a+40.3	a+35.6	a+18.4	a+20.2	16
4	a+42.9	a+27.6	a-11.4	a+10.7	a+25.3	a+12.3	a+20.8	a+35	a+18.3	a+20.2	15.7
5	a+43.3	a+27	a-11.5	a+10	a+25.6	a+12.2	a+20	a+36.3	a+18.6	a+20.2	16
6	a+43.2	a+27.8	a-11.3	a+10	a+25.4	a+12.1	a+20	a+35.9	a+18.4	a+20.2	15.9
7	a+42.6	a+28.2	a-11.3	a+10.3	a+24.7	a+12.5	a+20.2	a+36	a+18.3	a+20.2	15.8
8	a+43.4	a+28.1	a-11.5	a+10.2	a+25.2	a+12.4	a+20.5	a+36.1	a+18.5	a+20.3	16
9	a+43.3	a+28	a-11.5	a+10.1	a+25.8	a+12.4	a+20.6	a+36	a+19	a+20.4	16
10	a+43.5	a+28.6	a-11.3	a+10.2	a+25.2	a+12.2	a+20.3	a+35.8	a+18.7	a+20.4	16
Average	a+43.2	a+27.8	a-11.4	a+10.3	a+25.2	a+12.3	a+20.3	a+35.8	a+18.5	a+20.2	15.9
Range	1.4	1.6	0.6	0.8	1.9	0.9	0.9	1.3	1.2	0.7	0.3
U%	0.31	0.38	0.14	0.19	0.44	0.14	0.21	0.29	0.29	0.18	2.13

TABLE 1

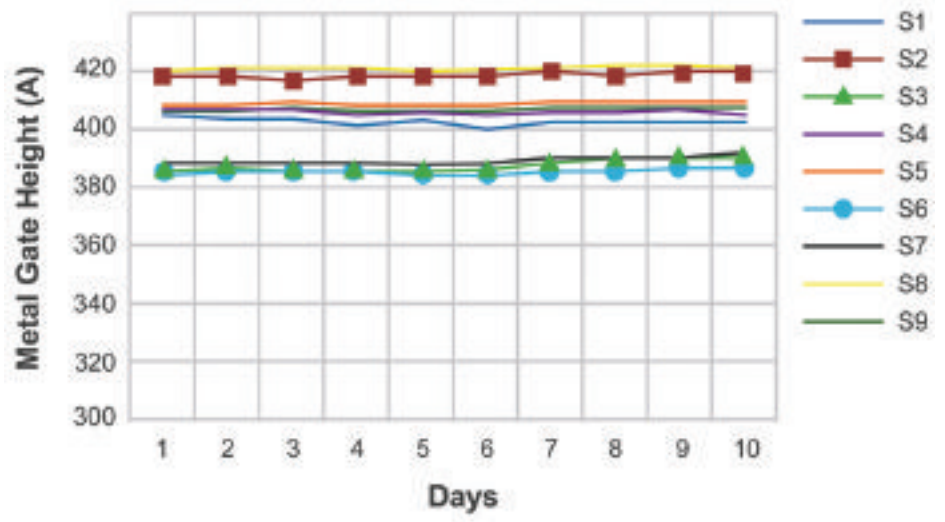

FIGURE 10. Long term stability monitored on daily QC wafers.

Conclusion

PULSE technology is uniquely qualified to provide the information needed for tight process control for the High-K/metal gate applications. Its small spot, non-contact, non-destructive nature permits direct, in-line measurements on product wafers. The measurements provide accurate information to the process area on true thickness variations that can be correlated with device performance. Excellent correlation between PULSE, TEM and resistivity methods has validated the accuracy of the technique. Direct PULSE measurements on SRAM structures provide a means of monitoring gate height that is clearly superior to indirect measurements using pad and line arrays, which are negatively affected by pattern dependent variations. In addition, the picosecond ultrasonic measurement system has demonstrated the repeatability and long term stability required for in-line metrology. Its capability has been proven for both pre- and post-CMP processes. Characterization of work function barrier layer measurement provides an additional benefit for the use of picosecond ultrasonic technology for HKMG process monitoring. ◆

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Going Up! Monolithic 3D as an alternative to CMOS scaling

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The main advantages of M3D are derived from the sequential fabrication of the various transistor layers on the same wafer.

The miniaturization of the MOSFET transistor has been the main booster for the semiconductor industry's rapid growth in the last four decades. Following "Moore's Law", this scaling race has enabled performance increases in integrated circuits at a continuous cost reduction: today's $200 mobile phone has as much calculating power as multi-million-dollar supercomputer 10 years ago! But at 28nm, it seems the race is over: Moore's scaling is facing obstacles – parasitic phenomena, incompressible delays, energy dissipation – that can be overcome with technology, but not in a way that is economically sustainable for everyone. This is where the idea to go 3D comes in: the density and cost dictated by Moore's Law would be achieved not by 2D shrinking but by going up into the third dimension **(FIGURE 1)**.

Piling transistors on top of each other in a "3D" configuration is not new. Stacking techniques using through-silicon vias (TSVs) are currently used for CMOS image sensors, MEMS, and now 3DNAND. In these scenarios, the devices themselves are processed on separate wafers, then aligned and bonded. The TSVs are essentially copper columns added to connect the top and bottom devices. While beneficial in certain cases, the TSV approach faces its own set of challenges with respect to aligning the transistors, the comparatively wide diameters of the TSVs, the pitch and the overall thickness **(FIGURE 2)**.

Monolithic 3D (M3D), which takes a very different approach to stacking transistors on top of each other, is one of the most promising alternatives approaches

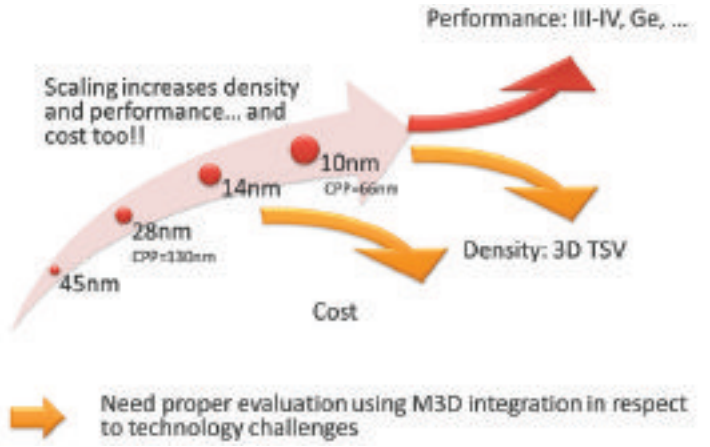

FIGURE 1. 3D provides an alternative to continued scaling.

when going 3D. M3D aims at increasing transistor density "sequentially" – meaning within a single process flow, as opposed to the TSV approach, which is applied to die that have already been processed. Staying within the bounds of a single process flow makes M3D much more cost-effective. M3D will enable an increased density of transistors without requiring the downscaling of their individual features. M3D could also provide a gain in performance by reducing the metal wiring delay, thanks to direct contact between transistor levels. From a cost perspective, M3D appears to offer a competitive advantage over equivalent N+1 scaling nodes: the scaling achieved in node N and even N-1 can be leveraged for another generation.

At CEA-Leti in Grenoble (France), one of the world's most advanced microelectronics R&D centers, CMOS-device teams are exploring various routes

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to meet increased performance requirements of future semiconductor applications. M3D is a primary focus in the search for alternate routes to scaling, in addition to other disruptive approaches such as steep slope devices, mechanical switches based on NEMS and single electron transistors **(FIGURE 3)**.

Leti is known for its expertise in the fields needed to demonstrate and take the industry lead in the M3D concept:

- a strong background-related to SOI devices fabrication
- a long history of process developments in molecular bonding of various substrates and materials, essential for creating a high-quality top active layer
- thorough experience in 3D stacking techniques, including design-tool developments, architecture exploration and test-vehicle or full-circuit implementations.

Leti's M3D program was first launched in 2007. In order to reach the expected performance with an acceptable time to market, M3D must be developed with close, simultaneous attention to applications, design and technology challenges. The success demonstrated since the program launch prompted Qualcomm to partner with Leti in 2014 to explore M3D technology potential for future generations of products.

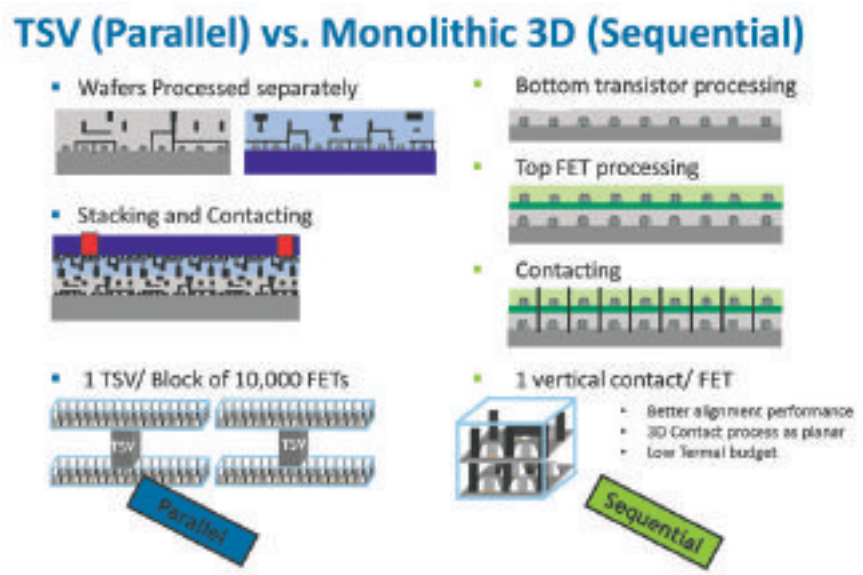

FIGURE 2. Monolithic 3D (M3D) takes a very different approach to stacking transistors on top of each other compared to conventional parallel TSV processing.

Leti's M3D: how it's done

The M3D concept consists of sequentially processing:

- processing a bottom MOS transistor layer
- processing another MOS transistor layer on top of the bottom one with lithographic alignment between the layers
- positioning metal lines between the two layers to allow connections between both transistor levels.
- encapsulating the inter-metal levels in an oxide layer
- bonding a wafer substrate to the top transistor layer using molecular bonding
- a planarization process.

Using an SOI wafer for the top layer molecular bonding provides higher crystalline quality, greater integration

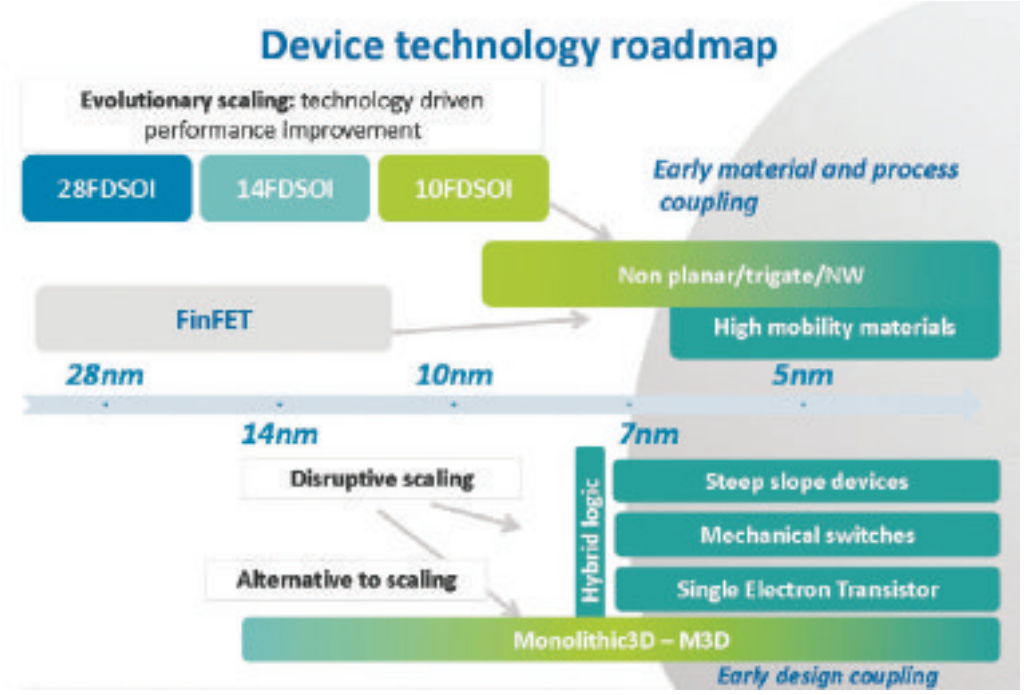

FIGURE 3. At CEA-Leti, M3D is a primary focus in the search for alternate routes to scaling.

density, and accurate thickness control. CEA-Leti has already demonstrated the successful stacking of Si CMOS on Si CMOS, achieving benchmark performance for both layers of transistors. The main process challenge is to develop a sufficiently low-temperature process for the top transistor layer to limit the impact on the lower transistor layers **(FIGURE 4)**.

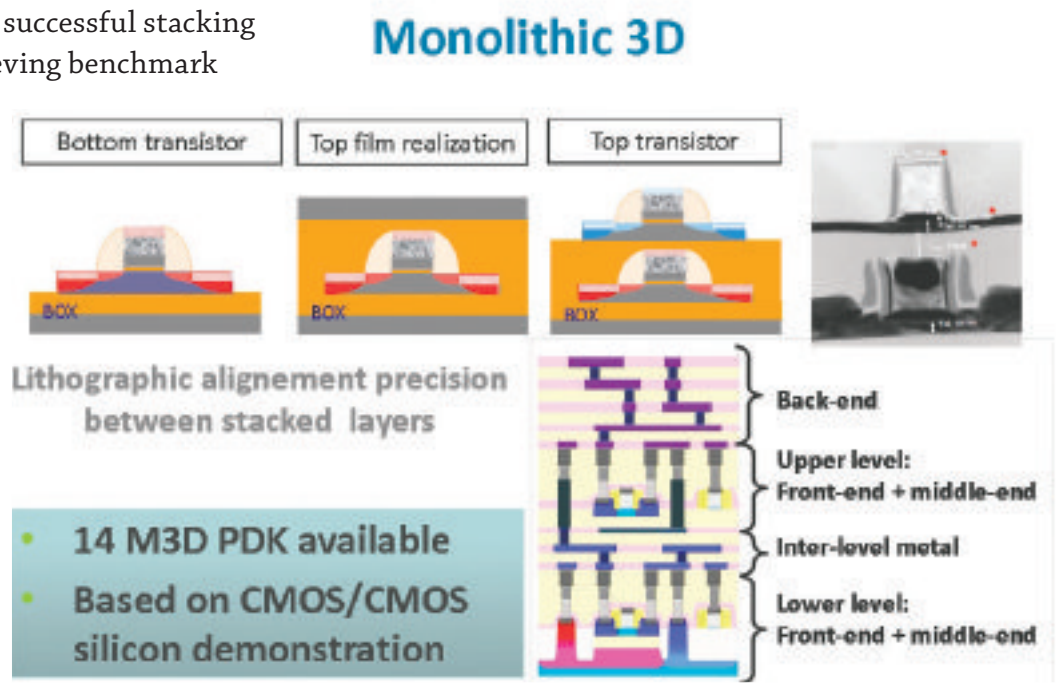

FIGURE 4. The bottom layer can be any CMOS technology, bulk (FinFET or planar) or SOI (fully depleted). The bottom layer is processed with plugs down to the CMOS. Fabrication of inter-metal levels is needed to reduce routing congestion. After molecular bonding on SOI wafer on top of the process bottom layer, the substrate is removed (the BOS serves as a stopping layer). Fabrication of the top layer built on the thin bonded semiconductor layer has contacts to connect the top layer to inter-metal levels.

M3D advantages

The main advantages of M3D are derived from the sequential fabrication of the various transistor layers on the same wafer. It leads to very high alignment accuracy (3D contact pitch <100nm using lithography tools adapted to 14nm production), uses high-density inter-connects, and surpasses 3D-TSV performance at a competitive cost. The inter-metal levels also facilitate design partitioning and architecture exploration **(FIGURE 5)**.

	Alignment (µm)	Diameter(µm)	Pitch(µm)	Minimum Depth(µm)
TSV	0.5 – 1	2 - 4	4 - 8	20 – 50
M3D	0.01	0.1	0.2*	0.1
M3D vs. TSV gain	**50x – 100x**	**20x – 40x**	**20x – 40x**	**200x–500x**

FIGURE 5. Alignment, diater, pitch and minimum depth of TSV and M3D technology. parallel TSV processing.

Leti's M3D approach is of particularly high value for those products that do not really benefit from scaling, especially when cost constraints are stringent. Different design simulations estimate a gain of one-node performance without scaling constraints. Once the remaining challenges are overcome, potential applications range from heterogeneous stacks (imagers, MEMS on logic) to advanced memory structures, advanced processors, programmable logic and various SOCs **(FIGURE 6)**. All those products would benefit greatly from the added value provided by M3D:

- High-circuit density provided by stacking active layers in 3D at minimum-contact pitch level
- Better power dissipation (greater absorption across inter-metal levels surface)
- Increased speed/power performance trade-off by reducing high-resistivity metal wiring length.
- Competitive cost advantage by re-using a given node process scheme without requiring additional/new steps to achieve performance gains.

PDK & model availability

In addition to the M3D technology process flow

development, CEA-Leti is also proposing a Predictive Design Kit (PDK) that provides a primitive M3D product design environment for integrated modeling, simulation, visualization and communication. It also includes validation tools that product designers need to benchmark M3D and explore new architecture concepts. The first M3D PDK version available from CEA-Leti will permit partners to get a first knowledge of the M3D technology, so they can run initial performance assessments regarding density, speed, power and cost. **(FIGURE 7)**.

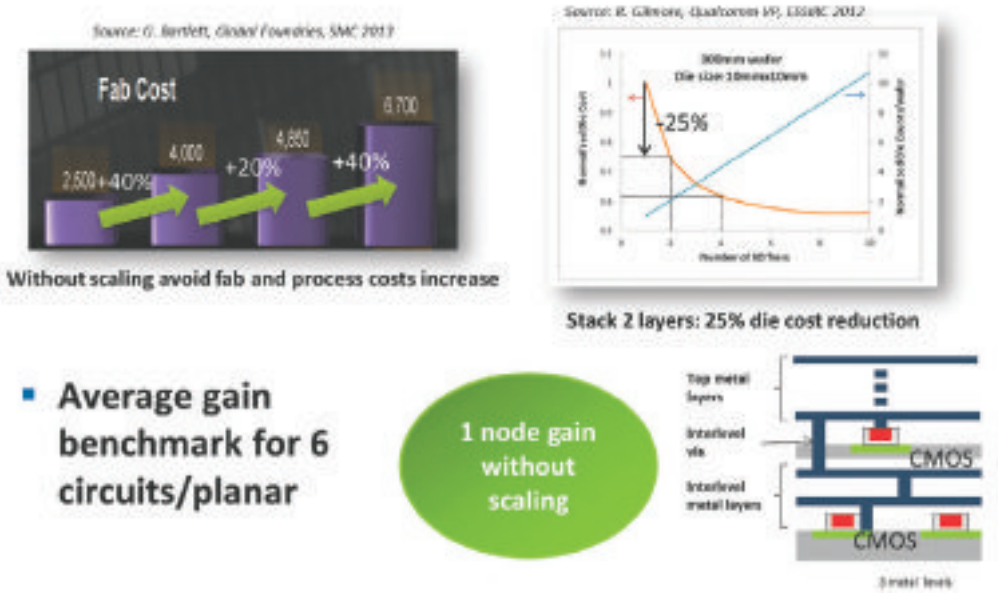

FIGURE 6. Process design kit (PDK) and model availability.

Future development

Part of CEA-Leti's mission is to develop technologies that are ready to transfer to industry, supporting customers in both developing knowledge and implementation on the manufacturing floor. In the case of M3D, CEA-Leti is beginning to build a full ecosystem of partners to enable the rapid industrialization of this technology. Qualcomm, a world leader in wireless technologies, joined CEA-Leti in its M3D R&D program in 2014 and has committed resources to assess the feasibility of the concept.

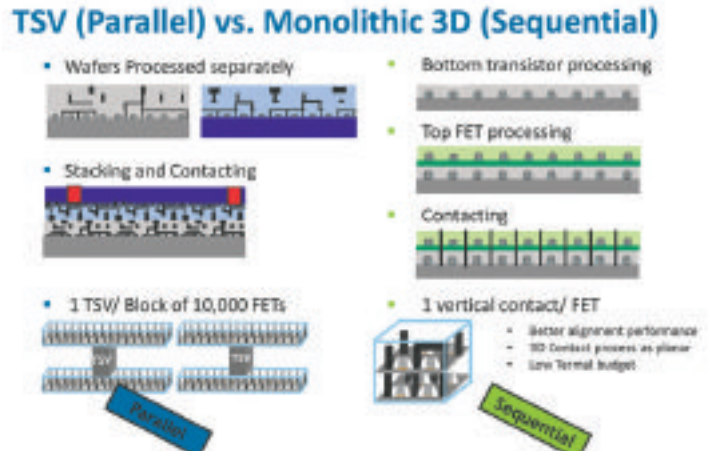

FIGURE 7.

To expand the momentum around M3D, while validating design-and-process assumptions and expected performance through prototyping demonstrators, the ecosystem should also involve a major foundry. CEA-Leti also plans to include additional members of the semiconductor business value chain (device modeling, EDA, process tooling, test, etc.) to form a complete M3D ecosystem, and make M3D a competitive technology for industrial transfer.

In the short term, CEA-Leti is looking for interested companies to engage in an R&D program aimed at validating proof of concept of an M3D integration process flow and its related libraries for advanced CMOS nodes.

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Towards all solid-state 3D thin-film batteries for durable and fast storage

PHILIPPE VEREECKEN, *principal scientist, imec, associate professor, KU Leuven*

One way to make Li-ion batteries more durable, safer, smaller and in particularly faster, is a transition towards all solid-state 3D thin-film Li-ion batteries.

Applications like portable electronics, body area networks, wireless sensing networks and medical implants put severe pressure on energy storage technology development. As these devices become smarter and smaller at the same time, the demand for more powerful batteries with ever smaller volumes, larger storage capacity and higher lifetime grows. Of all known rechargeable systems, lithium ion (Li-ion) batteries provide the highest battery capacity and are therefore most popular for powering these devices. With a market share of more than 75%, they are currently the workhorse of the rechargeable battery industry for portable applications. Besides portable electronics, Li-ion batteries are growing in popularity for large-scale storage solutions, like electric vehicle applications and temporary or local storage in future smart grids. Still, several material, structural and architectural innovations are needed to tune these batteries to the needs of future applications.

From liquid electrolytes to planar all solid-state batteries

Li-ion batteries belong to a class of rechargeable batteries, which means that the chemical conversion of the electrode material is reversible when an opposite cell voltage or current is applied. In a Li-ion battery, lithium ions move from the negative electrode during discharge and back when charging.

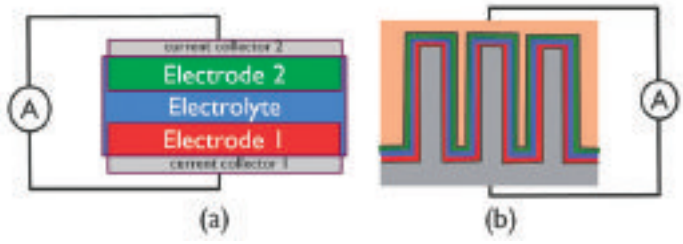

FIGURE 1. Schematic of a planar (a) and 3D thin-film (b) battery with the following stack: current collector/electrode/solid electrolyte/electrode/current collector.

This reversible operation is enabled by using insertion electrodes, from which Li+ ions can be inserted or extracted. The most common positive electrode materials are currently lithium cobalt oxide (LCO), and lithium nickel cobalt manganese oxide (NMC). In the near future also lithium iron phosphate (LFP), lithium magnesium oxide (LMO) and lithium nickel cobalt aluminum oxide (NCA) will be used more and more. As negative electrodes, specialty graphite or Li4Ti5O12 are commonly used. For next generation batteries these might be complemented by silicon and silicon tin composites to increase the battery capacity.

The power characteristics of a battery cell strongly depend on the ionic conductance of the electrolyte which separates the electrodes. Current Li-ion battery technology makes use of liquid electrolyte solutions, consisting of lithium salts (such as LiPF6, LiBF4 or LiClO4) in an organic solvent (alkyl carbonates). They do have a very high

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conductivity of about 5-10S/cm at room temperature. In these battery types, however, the solid-electrolyte interface – which is formed as a result of the decomposition of the electrolyte at the negative electrode – limits the effective conductance (1-0.001S/cm2). Moreover, liquid electrolytes need expensive membranes to separate cathode and anode, and an impermeable casing to avoid leakage. This puts restrictions on the size and design of the batteries. And, since flammable and corrosive liquids are used, they suffer from safety and health issues.

Imec is looking towards solid-state Li-ion batteries which are not only safer but allow scaling and even elimination of certain components. As such, they can be made with a higher effective energy and power density. In addition, they promise a longer lifetime and a broader temperature range of operation. These advantages encourage researchers to find innovative solutions for the main technological challenge: making a stable solid electrolyte component with high enough conductance for ions. An interesting approach is to scale down the thickness of the electrolyte. This way, an acceptable ionic conductance (e.g. 0.1-0.01S/cm2) can be obtained even for solid electrolytes with intrinsically low ion conductivity (e.g. 10-6S/cm). Scaling the electrolyte thickness is most efficiently done in a thin-film configuration and this presents some technical hurdles. Thin electrolyte films could lead to electrical shorts either through pinholes in the film or formation of conductive filaments (cf. a failure mechanism which is at the origin of resistive-RAM). Scaling down the film thickness also magnifies issues at the interfaces as in-diffusion regions may become considerable. This calls for advanced deposition techniques, like atomic layer deposition (ALD), to provide pinhole-free films and control the interfaces and as such the electrical properties of the battery stack.

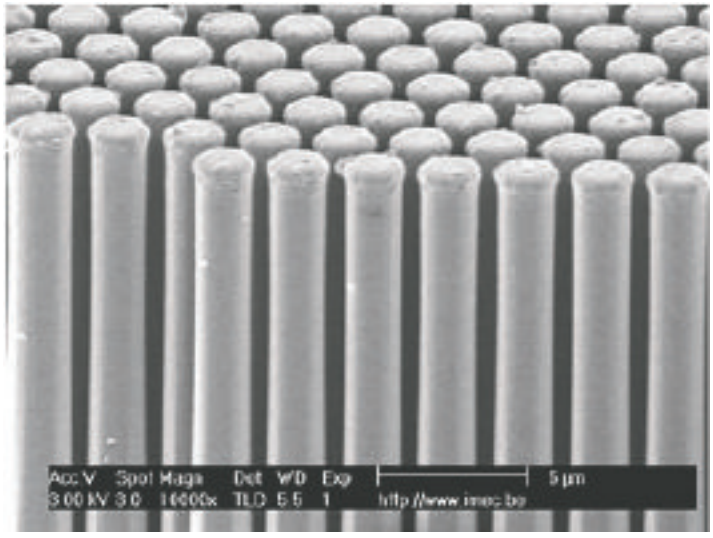

FIGURE 2. The electrode and electrolyte materials should be deposited onto microstructured surfaces of the substrate (e.g., by the creation of silicon pillar structures, in order to maintain the battery capacity). This figure shows coating of a silicon pillar array with a 200nm film of electrochemically deposited MnO2 on a TiN diffusion layer.

From planar batteries to 3D thin-film batteries

A similar film scaling approach can be applied to the electrodes as well. Scaling down the electrode films significantly enhances the charging/discharging rate of the electrodes, and thus the battery power. But thinning down the films also diminishes the battery capacity, which depends directly on the total available amount of electrode material. In planar batteries, electrode films can therefore not be thinned below one micrometer (resulting in a maximum capacity of 0.07mAh/cm2 in case of a 1 µm thin LCO electrode). Fortunately, there is a way to compensate for the loss in electrode material and increase the battery capacity: the effective area can be increased by coating the thin-film stack on a micro- or nanostructured 3D structure (**FIGURE 1**).

A key enabling technology for these 3D thin-film batteries is micro- or nanostructuring of the substrate, for example by creating arrays of etched pillars in silicon. In order to maximize the battery power and capacity, an optimum condition in patterning density and film thickness need to be sought. Next, the thin films must be deposited onto the large surface areas in a conformal, pinhole-free and uniform way. Therefore, we need deposition techniques that allow a conformal coating of electrode and electrolyte materials onto high-aspect ratio 3D structured substrates. One of the options being explored at imec is a conformal stack of manganese and titanium based electrodes with a thin viscoelastic electrolyte interlayer (**FIGURE 2**). To achieve good conformality we rely

on deposition techniques such as electrochemical deposition (ECD), chemical vapor deposition (CVD) and atomic layer deposition (ALD). As a first step, the thin-film batteries are fabricated on a Si platform taking advantage of the existing integrated circuit processing know-how at imec. These micro-batteries will be able to power microsystems such as wireless sensors. In a second stage, the processes and materials will be up-scaled to foil technology so that also batteries for portable electronics and eventually for local storage or electrical vehicles can be made. For this step, the know-how in the System in Foil program and the foil based process integration facilities in Holst Centre, our imec - TNO collaboration in Eindhoven are a big asset.

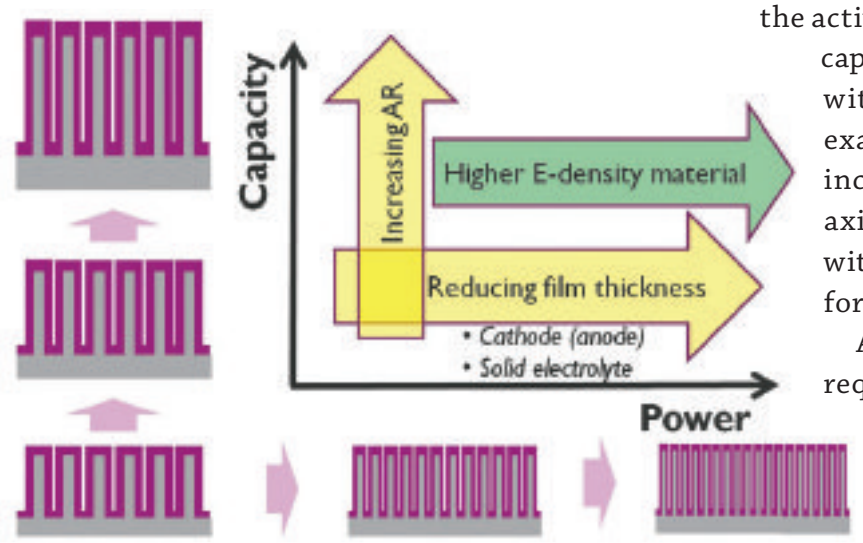

FIGURE 3. Schematic showing the principle of scaling for 3D thin-film batteries.

A scaling technology roadmap

Many of the ideas for innovation in battery technology could well come from the IC industry, where the downscaling of the transistor has driven tremendous research efforts into new materials and nanotechnology. The driver behind the steady pace in scaling is a technology roadmap that sets out the specifications and material options for each new transistor generation. This evolution has led to the development of many new processes and techniques, such as advanced deposition techniques like CVD and ALD. Similar to the scaling of transistor technology (i.e. the transistor gate length and gate oxide), we believe a scaling technology roadmap for 3D thin-film batteries can gradually improve their performance (**FIGURE 3**).

The battery power (or charging and discharging rate) of the thin-film battery can be progressively improved by reducing the thickness of the electrode and electrolyte thin films (x axis in the figure). Each new generation (or node) would therefore require thinner pinhole-free, conformal, chemically uniform layers in ever higher aspect ratio features. Simultaneously, the pattern density of the 3D structures must be increased to maintain the volume of the active electrode material (and hence the battery capacity). Or, more surface area can be provided without changing the pattern density, for example by using nanostructured pillars with increased aspect ratio (as indicated on the y axis of the figure). Alternatively, new materials with higher energy-density can be introduced for additional battery capacity.

As for CMOS scaling, the technological requirements for scaling 3D thin-film battery performance are demanding. We will need ever more advanced patterning, etch and deposition technologies to enable pinhole free, high quality coatings and to obtain conformality in extreme aspect ratios. Nevertheless, we believe that such a roadmap can lead us to ultrafast charging batteries. Such type of batteries could remove the need for more battery capacity for multimedia and computer devices as the battery can be constantly recharged in a wireless environment and thus never runs out. This novel mode of battery use is somewhat similar to that of autonomous microsystems where the battery is integrated with an energy harvester to recharge the battery when energy is available. Such solid-state batteries can indeed enable microsystems with full autonomous operation, needed for example in medical implants or automated sensor systems. The exceptional properties of solid-state batteries may also enable new technologies, like smart solar panels where storage is integrated on the backside of the solar panels, for example integrated in the roof of a car, bus or train.

Flat panel displays get flexible

SARA VER-BRUGGEN, *contributing editor*

Flexible displays have been in R&D and pre-commercial development for several years, but what needs to happen to make volume production a reality, in areas including substrates, materials and production processes?

Semiconductor Manufacturing & Design (SemiMD), discussed recent progress in flexible flat panel displays with Mac McDaniel, Director and Chief Marketing Officer, Display Business Group, Applied Materials, Michael Ciesinski, MD of the Flextech Alliance, and Keri Goodwin, Principal Scientist from the Centre for Process Innovation (CPI), in the UK.

FIGURE 1. Roll to Roll Micro-contact printing line (Source: UniPixel)

SemiMD: Taking a step back and looking at the timeline for flexible display R&D and achievements so far, where is the industry in terms of entering volume production – how close is the industry to resolving those outstanding challenges to volume production, such as cost-effective barrier technologies, for example?

McDaniel: Curved displays are here as evidenced by several curved smartphones and TVs showcased at the Consumer Electronics Show (CES) in January 2014. People are ready for flexible displays, but production volume will take some more time. As the smartphone market matures, brands are embattled in a 'resolution arms race'. The key challenge for the brand makers is to come up with the next big thing that will differentiate their products and spur new demand from consumers. The display plays a key role in defining the device, and a new form factor – like flexible displays – can bring new opportunities to the market, but the technology is not ready for the mass market because of cost and technology challenges.

Ciesinski: FlexTech initiated its R&D programme into flexible displays in 1998 with substantial project funding beginning in 2002 and continuing today. We've worked with companies and R&D organisations in the areas of substrates, encapsulation, barrier coating, roll-to-roll (R2R) manufacturing and other key areas **(FIGURE 1)**. Generally, the supply chain for flexible electronics is adequate but not yet robust, which will occur once large volume production is achieved. In building flat panel displays (FPDs) that industry could build on IC manufacturing strengths and simply scale the

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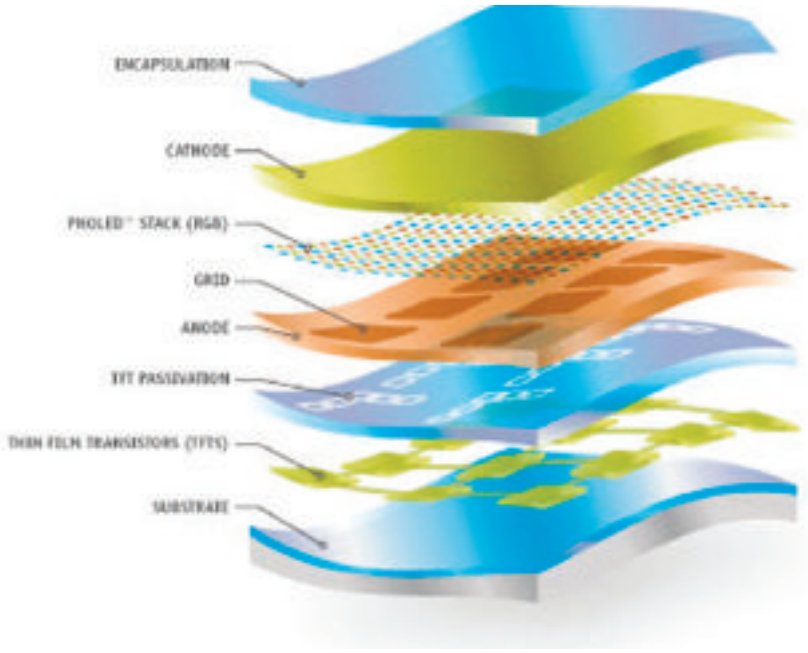

FIGURE 2. A variety of flexible polymeric materials have been evaluated for FOLED use; however, the development of barrier coatings for these substrates and better film properties, such as thermal stability (for the fabrication of high-temperature TFTs) are still required. (Source: Universal Display Corp.)

equipment. For volume manufacturing on a flexible substrate, many new tools and processes have to be developed from scratch, such as metrology, as experts must build a system to account for a substrate that can shrink or expand depending on temperature, and move in multiple directions. As for barriers, several solutions are available and ready for production. The extreme requirements for OLED thin film barriers have been achieved in production and the main focus now is on cost reduction. The materials industry is quite competitive and ready for volume. In order to obtain better utilisation of these materials in production new printing equipment is being developed.

Goodwin: There are still significant challenges to overcome in flexible display volume production. A cost-effective flexible barrier with a very low water transmission vapour rate (WVTR) is still to be developed, this will be required if OLED front-planes are to be used **(FIGURE 2)**. Typically these barriers are still multilayer structures with a mix of inorganic and organic coatings to minimise defect levels. Whilst this can be achieved R2R, perhaps via a combination of sputter deposition and solution processing such as slot die, the cost will ultimately be set by the number of multiple coatings required.

An alternative method may be to use RTR atomic layer deposition (ALD), which should yield a significantly lower level of defects, thereby improving the barrier capability of a single layer and reducing, or removing, the need for multiple coatings. However, process scale up is required. CPI envisages that R2R ALD will play important roles in various aspects of flexible printable electronics, where highly conformal nanoscale thin films are required. CPI has been evaluating ALD technology for several years and recently signed an agreement with Beneq to deliver an ALD system to CPI for pilot scale production.

Layer-to-layer registration is another major challenge to overcome in volume production with flexible substrates typically distorting during processing. This issue can be overcome in several ways such as development of lower temperature processes or development of lamination materials to allow sheet-to-sheet (S2S) production without distortion.

SemiMD: And, in terms of commercialisation for flexible (as opposed to curved) displays what timeframe are we talking?

McDaniel: The approach for early adopters of flexible displays has been a production process that adheres the flexible substrate onto glass, running it through what's mostly the normal rigid OLED processing, and then delaminating that flexible substrate from the rigid one at the end of processing. What remains is a flexible substrate that has all the transistor structures built onto it. However, this is still a complex process, and due to the cost and complexity involved in manufacturing on a high-volume scale, it is still a ways off from full mass production.

Goodwin: Overall, there are multiple approaches to volume production of flexible displays but all require scale up towards a commercialisation

solution, therefore it would be expected that the timeline for a product is still five years away. What is important in the short term is to demonstrate controlled processes that can yield products with good lifetime and performance, which then can be scaled up for commercialisation.

Ciesinski: Displays in a conformable format have been produced and exhibited; a truly flexible and foldable display is much more than that and there are many approaches to achieving this result in the next few years.

SemiMD: Various flexible display R&D has focused on different substrates, different thin film transistor (TFT) materials and so on. Is there likely to be one approach that will make it to volume production?

Ciesinski: Multiple approaches are currently being considered by the market. For example, plastic substrate films from DuPont Teijin and other suppliers have a strong a presence. Corning's introduction of flexible glass provides a competitive choice. As for the display technology, LCDs, OLEDs and electrophoretic displays have all been built in a flexible format. Materials will continue to improve and there will be multiple TFT materials for the next few years.

McDaniel: Materials have a key role to play in the R&D efforts for enabling flexible displays. OLED is promising as the rigid glass encapsulation required to protect the organic material from moisture and air can be replaced by thin film. You can make flexible LCD displays but maintaining the required cell gap between the colour filter and backplane is very difficult to do. Both OLED and LCD require a TFT backplane. A major challenge for the industry is how to move away from rigid glass while not compromising the operation of the TFT when flexed, folded, or bent.

We have discussed the backplane and encapsulation; but for OLED to get to mass production (especially in large sizes); the industry also has to address challenges in EL evaporation such as lifetime of organic materials, low deposition efficiency, low yield from defects and scalability of evaporation technology which affect the cost of volume production but are not necessarily related to the issues around flexibility. All display technologies, including OLED displays, require very high levels of precision in film uniformity and particle control to maintain yield. There is the potential for OLED display production to become less expensive, and Applied Materials is leveraging its expertise in precision materials engineering to help solve these technology hurdles to reduce the cost and complexity.

Goodwin: It is likely that there will be multiple options for volume production. This will depend on final product requirements, such as limits of flexibility, level of resolution of display and cost of display. For example, metal oxide-based TFT displays already demonstrate high performance in terms of the TFT, and therefore can achieve high resolution displays, but ultimately will be very limited in the flexibility.

Organic electronics show excellent flexibility, but historically have tended to have a lower performance for OLED display backplanes and therefore may not achieve the same level of display resolution as metal oxide in the short term. More recently this gap in performance has been closed substantially making organic TFT backplanes a good candidate for a wide variety of display formats and resolutions. In addition OTFT backplanes may ultimately be a lower cost of production. Overall, it is likely that the different TFT technologies will independently develop the substrate types suitable for their processes, for example metal oxide on high temperature substrates and for organics the substrates are likely to be more flexible and suitable for lower temperature processes.

SemiMD: In terms of production equipment and tool advances, which technologies are most promising for enabling volume production of flexible displays?

Goodwin: Metal oxide is currently deposited via industrially used techniques/tools in the display industry, such as sputter deposition. This makes it a likely candidate for early adoption in the display industry, with moderate investment required to

enable scale-up. However, solution-processing of organic based materials is likely to provide a lower cost of manufacture via the route of additive printing and R2R manufacture. CPI is working with a number of SMEs in building scale up capability across a range of printed and plastic electronics technology areas such as OLED, OTFT and barrier encapsulation, to help take forward new research ideas into technology prototypes and then into manufacturing demonstrators.

McDaniel: Flexible and other future bendable form factors in display will require precision engineered materials including thin film technologies that deliver performance with stringent uniformity and defect requirements at lower cost and less power. Advances in CVD and PVD systems for LTPS and metal oxide will play an important role in achieving high resolution but even these processes will require materials modification to support the full promise of flexible displays. One example of a required modification is indium tin oxide (ITO), a mainstay process step in TFT-LCD but as a material may prove to be too brittle in the production of more flexible displays.

Applied is also looking to help display makers mass produce larger scale, more efficient manufacturing processes and advanced materials as a means of gaining economies of scale at the factory.

Ciesinksi: FlexTech has funded and successfully completed projects for key steps in flex display manufacturing, such as lithography and deposition. Clearly various printing technologies and RTR additive manufacturing processes are capable of achieving major advances in flexible display production which will be seen over the next few years.

SemiMD: New display technologies that commercialise successfully have done so because they have enabled new products. The mass volume production of LCDs has helped to initiate smart phones, tablet devices, for example, while e-paper (E-Ink) display technology is largely responsible for e-reader devices such as the ubiquitous Kindle. So what potential new class of consumer/portable electronic device might flexible display technology enable? On the other hand, will the technology, in the nearer term, be more beneficial for enabling rugged/unbreakable display-based electronic devices?

FIGURE 3. A flexible display manufactured at the Arizona State University Flexible Center. The center is unique among the U.S. Army's University centers, having been formed through a 10-year cooperative agreement with Arizona State University in 2004.

McDaniel: There is a lot of potential. Think about what our phones looked like six or seven years ago. Now we're seeing HD-quality screens on a device we can slip into our pockets. We could see flexible displays enabling devices that can be rolled up or folded into more compact shapes. Some studies have said that for a tablet, people prefer semi-rigid displays to something that is flopping around, to provide structure while they're reading it. In the public environment flexible could bring the possibility of more immersive or interactive displays at airports or on billboards, or even on the sides of buildings. There are a lot of possibilities.

Goodwin: Rugged displays are likely to have military applications **(FIGURE 3)** and so may attract funding support from this sector and therefore this may be a route to the first marketable products. However, the learning from the production of those rugged displays can likely be used within new mainstream product development. Many major display manufacturers are already trying to patent areas of interest such as smart watches and early products may focus on these smaller displays. Ultimately, if volume production is possible and

large area displays can be produced then there is a vast range of products that can be envisaged from clothing applications, rollable/foldable phones, large scale advertising hoarding or even replacement of aircraft windows with lightweight displays.

Ciesinksi: Technology adopters fall into several categories. For example, early adopters are those with the first cellular phone, the first tablet, etc. These users are willing to sacrifice elegance or product maturity for functionality. Other adopters waited until smart phones became fully functional before consolidating to a primary device from a combination of a PC, cell phone, and pager. Wearable electronics, as a class, represents a game-changing technology. A wearable device – even with limited functionality – is attractive, for example, to competitive athletes if it can help improve performance even modestly. Once wearable technology matures, it can explode into other markets to monitor the chronically ill, aged/infirm, or paediatric patients. Then, it jumps to the packaging or automotive **(FIGURE 4)** or aerospace markets in the form of sensors.

SemiMD: Once flexible display technologies reach volume production, how fast might the technology establish itself – evolve from niche to mainstream?

Ciesinksi: Successful technologies ramp quickly and displace incumbent technologies ruthlessly. Just consider the displacement of CRTs by FPDs or CCFL backlights by LED backlights. FlexTech believes that flexible electronics – of which flexible displays is a subset – will grow rapidly in multiple markets, led by disposable and wearable electronics. Our recent user survey indicated substantial purchases of flexible electronics by key end users within three years; adoption by large contract manufacturers is already taking place due to their customer demands.

Goodwin: This is likely to be dependent on the product uptake. For example the rise of tablets and smart phones drove the development of OLED frontplane and materials development. The same is likely to happen with flexible displays. Early products may have limited flexibility, for example

FIGURE 4. Atmel's XSense sensors can be used on curved surfaces and edges, facilitating the design of futuristic in-vehicle touchscreens and surfaces.

the already available curved display products from LG and Samsung, but later products will need to show the truly flexible nature of these advanced displays. Once market pull is established a range of products are likely to be developed that will aid the flexible display to become a mainstream product. CPI can play a vital role in the move from niche to mainstream by providing the infrastructure and environment for companies to de-risk and scale up their innovative ideas from concept to market.

McDaniel: Five years ago, when display manufacturers wanted to start bending and curving the design, they faced a new set of struggles. Applied Materials had insights on where the market was heading and was already working on technologies to address the challenges. We have seen similar waves of technology with laptops and smartphones, and the acceleration of flexible or curved display devices or other form factors could take off in a similar manner. Display analyst firms are anticipating strong growth for the flexible and curved displays market over the next several years. For instance, Touch Display Research has forecast flexible and curved displays to achieve 16% of the global display revenue market by 2023 compared with 1% in 2013.

3D EDA brings together proven 2D solutions

ED KORCZYNSKI, *Senior Technical Editor*

Design methodologies and technologies for 2D multi-chip systems are extended into 3D using proprietary tools based on industry standards.

With anticipated economic limits to the continuation of Moore's Law now on the horizon, it seems that moving into the 3rd dimension (3D) by stacking multiple layers of integrated circuits (IC) will be the ultimate expression of CMOS technology. Whether stacking heterogeneous chips using through-silicon vias (TSV), or monolithic approaches to forming multiple active IC layers on a single silicon substrate, 3D ICs should be both smaller and faster compared to functionally equivalent 2D chips and packages.

However, 3D ICs will likely always cost more than doing it in 2D, due to more step being needed in manufacturing. A recent variation of 2D IC packaging with some of the benefits of 3D is the use of silicon interposers containing TSV.

Current state-of-the-art electronic design automation (EDA) tools exist to handle complex IC systems, and can therefore handle complex 3D designs as long as the software has the proper inputs from a foundry's Process-Design Kit. **FIGURE 1** shows the verification flow for a multi-chip system using the "3DSTACK" capability within Mentor Graphics' Calibre platform. Leading IC foundries GlobalFoundries and TSMC as well as 3D IC specialty foundry Tezzaron have all qualified 3DSTACK for their 2.5D and 3D design verifications.

EDA tools have evolved in complexity such that Design-For-Test (DFT) methodologies and technologies now exist to tackle 3D ICs. Steve Pateras, product marketing director, DFT, Design to Silicon Division of Mentor Graphics advised, "If you're stacking multiple die together, you need to work with known good die. The ROI basically changes

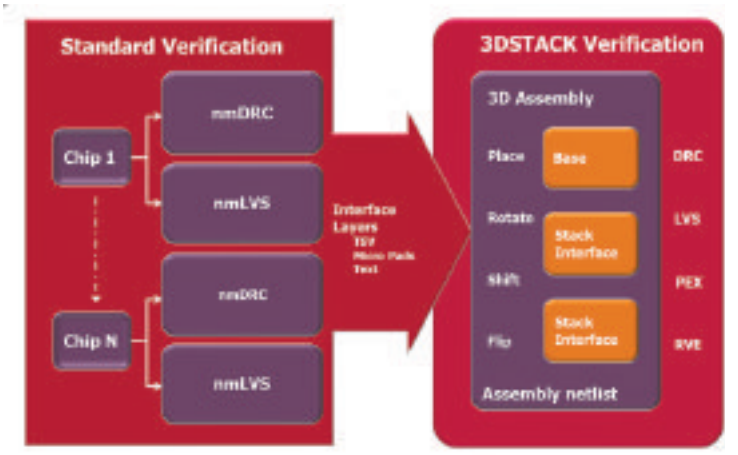

FIGURE 1. "3DSTACK" functionality integrates with existing 2D Design Rule Check (DRC) modules within the Calibre platform. (Source: Mentor Graphics)

for stacking, such that you need to get into a different regime of test." In a die stack we have to think about not just known good die, but die known to be good after they are stacked, too. The latter condition mandates standards for DfT to allow test signals to flow between layers.

The IEEE 1838 working group on 3D interface standards (https://standards.ieee.org/develop/project/1838.html) is intended for heterogeneous integration, allowing for different IC process technologies, design set-ups, test, and design-for-test approaches. The standard defines test access features that enable the transportation of test stimuli and responses for both a target die and its inter-die connections.

FIGURE 2 shows the extra die interfaces that must be physically verified within a 3D IC system stack. Die interfaces can be mis-aligned due to translation or rotation during assembly, and with die from different fabs at

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different geometries it can be non-trivial to ensure that the rights pins are connected.

3D memory stacks are somewhat in their own category since they are primarily designed and manufactured by IDMs, though often with a logic layer on the bottom they are mostly homogenous, and since memory usually runs cooler than logic they generally have no cooling issues. For these reasons 3D memory stacks using wire-bonds have been in volume production for years, Micron leads the development of the Hybrid Memory Cube using TSV, and Samsung leads in growing multiple memory layers on a single silicon chip.

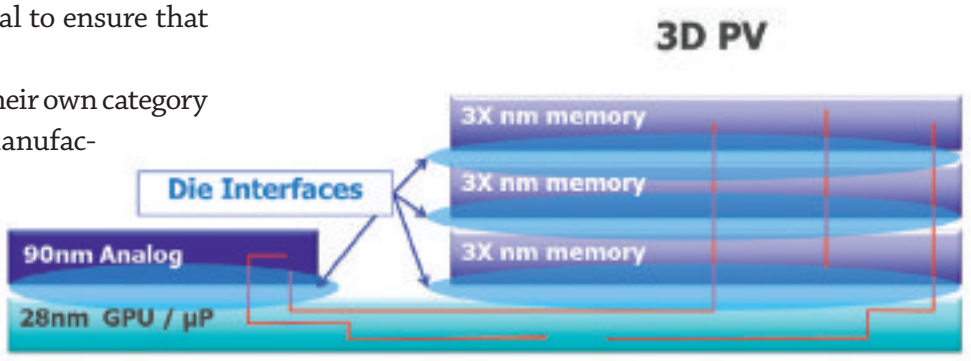

FIGURE 2. Schematic cross-section of a 3D IC system showing the die interfaces that require new Physical Verification (PV) checks. (Source: Mentor Graphics)

Future Demand for 3D Logic

So far, the only known commercial logic chips shipping with TSV are the Xilinx Virtex-7 product, where four 28nm node FPGAs (as reported by Phil Garrou in 2011 in his IFTLE blog http://bit.ly/1pgfYVR) are connected to a silicon interposer. Xilinx has shown that much of the motivation for using 2.5D packaging was to improve yield when working with the maximum number of logic gates in the smallest available process node, and when foundry yields improve with learnings for a given node we would expect that the FPGA would be made using a single-chip 2D solution.

It appears that 2.5D is not so much a stepping-stone to 3D, as it is a clever variant on established 2D advanced packaging options. Silicon interposers with TSV offer certain advantages for integration of high-speed logic in 2D, but due to relatively greater cost compared to other WLP methods will likely only be used for high-margin parts like the Virtex-7. Also, Out-Sourced Assembly and Test (OSAT) companies have been offering both "fan-out" and "fan-in" wafer-level packaging (WLP) options, and heterogeneous integration can certainly be done using these approaches. "We have customers planning on using interposers, but they're planning on lower-cost substrates," commented Michael Buehler-Garcia, senior marketing director for Calibre, Design to Silicon Division of Mentor Graphics.

If high volume CMOS logic will always be most cost-effectively integrated in a single 2D slice of silicon, and heterogeneous integration of CMOS can be done in 2D using FD-SOI substrates, then what remains as the demand driver for future 3D logic stacks? What logic products require heterogeneous integration for basic functionality, would be band-width-limited by 2D packages, and also are anticipated to be shipped in sufficiently high-volume to allow for amortization of the integration costs?

Several vendor have recently launched 100G C form-factor pluggable (CFP, https://en.wikipedia.org/wiki/C_Form-factor_Pluggable) modules to increase speeds while reducing costs in communicating between data servers. ClariPhy produces a CFP SoC using a 28nm CMOS process that is packaged with laser diode chips from Sumitomo Electric Industries' (SEI). "By combining ClariPhy's SoC with SEI's world class indium phosphide optics technology and deep experience in volume manufacturing of pluggable optical modules, we will deliver the benefits of coherent technology to metro and datacenter networks," said Nobu Kuwata, general manager of the Technology and Marketing Department of Sumitomo Electric Device Innovations (SEDI). "We will provide first samples of our 100G coherent CFP next quarter."

Even greater cost and power savings could derive from a revolution in the interconnections used not just between servers but inside the server farms that provide the ubiquitous "cloud computing" we are all coming to enjoy. "It's still a couple of years out, but we're doing research on DARPA projects now," says Buehler-Garcia in reference to work Mentor Graphics is doing to bring the automation of its Calibre platform to this application space.

The EDA industry's ability to handle system-on-chip (SoC) and system-in-package (SiP) layouts means that the differences between designing for 2D, 2.5D, and 3D logic should be minimal. "We don't charge extra for 3D," explained Buehler-Garcia, "it's already part of the deal."

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Domestic outsourcing: A key component in successful reshoring

After nearly a quarter of a century, the off-shoring manufacturing trend that decimated the U.S. manufacturing sector and played a significant role in the slow pace of the current economic recovery seems to be ending. A number of large manufacturers, including NCR, Apple, Google, Caterpillar, Whirlpool and Ford have recently announced plans to return some of their overseas manufacturing to the United States. Even Nissan recently announced it was relocating a manufacturing plant from Mexico to the U.S. Many other American firms are considering taking similar action.

While this reshoring trend might be considered a ripple rather than a wave in the economic waters, it is growing. According to a study conducted in August 2013 by the Boston Consulting Group (BCG), 54 percent of the more than 200 companies surveyed were planning or seriously considering reshoring some of their manufacturing. That is a 17 percent increase over the 37 percent considering reshoring in 2012 when BCG last conducted the survey. Twenty-one percent of respondents said they were actively engaged in reshoring or will do so in the next two years, double the number reporting such activity a year ago.

According to Harry Moser, former CEO of Charmilles Technology Corp. and founder of the Reshoring Initiative, over 50,000 manufacturing jobs returned to the U.S. between 2009 and 2012. In the five years previous, the number returning was close to zero. Those 50,000 jobs constitute about 10 percent of the new manufacturing jobs created in the U.S. over the last three years.

Contributing factors to the reshoring trend

There are a number of global and domestic economic factors that are causing many American, and even some foreign companies, to consider moving their manufacturing operations to American soil. The two most significant are wages and productivity.

For example, according to an April 2013 Bloomberg article, the average pay in Asia almost doubled between 2000 and 2011, while wages increased by only 5 percent in the developed world and by 23 percent worldwide. Labor costs were one of the prime drivers off the off-shoring trend, and this significant rise in labor costs in the region erodes one of the key economic benefits of moving manufacturing to that region.

When that upward wage trend is coupled with differences in the levels of productivity of American and foreign workers, reshoring becomes even more attractive. According to a U.N. report compiled by the International Labor Organization (ILO), American workers out-produced and worked longer hours than their counterparts in Japan, Switzerland and all 27 European Union countries. While workers in Asian countries do tend to work longer than their American counterparts, even this is changing. Chinese workers have recently been demanding shorter hours and in some cases, job tenure after a certain number of years of employment.

Further, even when working fewer hours, American workers consistently out-produce their Chinese counterparts. According to ILO statistics, the average Chinese industrial worker produces $12,642 worth of output per year, while the average Chinese farmer or fisherman produces about $910 worth of output in the same time. By comparison, an American worker in the industrial sector produced $104,606 worth of output and a worker in the farming or fishing sector produced $52,585 per annum.

When one considers the diminishing difference in labor costs and the magnitude of difference in worker productivity, reshoring starts to become a very attractive alternative. It becomes even more attractive if one takes some additional factors into consideration.

Logistics are vastly simplified. The distances parts and finished goods have to be shipped will generally be shorter, which saves on both time and cost. The expenses and risks in maintaining a global supply chain are significantly reduced, as is the time and expense involved in dealing with customs issues. Communication

MARK DANNA, *Vice President Business Development*, **OWENS DESIGN, INC.**

across multiple time zones is also minimized.

Reshoring to the U.S. can also help reduce employee stress and increase productivity, since fewer employee hours will be lost to overseas travel. Business travel expenses will also be reduced. In addition, employees will experience fewer frustrations due to linguistic or cultural misunderstandings, making it easier for them to do their jobs.

Additional potential benefits of reshoring manufacturing to the U.S. include greater security and a more stable political environment, better protection of intellectual property and lower energy costs as the U.S. becomes a global leader in energy production.

In BCG's survey, 43 percent cited labor costs as a factor in their interest in reshoring, 35 percent cited proximity to customers and 34 percent cited quality issues. Additional considerations cited skilled labor, transportation costs and supply chain management efficiencies. According to Moser, when the total cost of ownership of overseas manufacturing is considered, domestic manufacturing in the U.S. is the clear economic winner.

Reshoring challenges

Of course, a decision to move a company's manufacturing back to the U.S. offers its own set of challenges. It takes time to build a manufacturing facility and train workers. This can easily take a couple of years and a considerable investment in capital. In the mean time, one still has to be producing the goods needed to meet customer demand.

Once a company decides to reshore, it has to handle the logistics of ending production in its overseas facilities and ramping up in the new U.S. facility. It also may have to deal with overseas employees and even its host country being less than supportive of its reshoring decision. Indeed, an American factory manager in China was briefly held hostage by his factory workers over rumors the company planned to move its manufacturing back to the U.S.

In addition to the purely logistic issues, it is critical to consider your customers in your reshoring equation. It's vitally important to assure them that your reshoring transition will not interrupt their expected flow of finished products or lead to significant increases in their price.

Easing the reshoring transition with domestic outsourcing

Ironically, a potential solution to these reshoring transitional challenges can be found in outsourcing. In this case, however, it's a domestic outsourcing, rather than overseas outsourcing that offers a viable business solution. A domestic outsourcing partner can provide the engineering and manufacturing resources that are needed to minimize the pain involved reshoring.

Partnering with a domestic design house offers a number of advantages. The outsource partner will have a core of experienced engineers and design teams used to bringing multiple new designs to volume production every year. In addition, most will have access to established U.S. manufacturing facilities capable of producing products in volume. As a result, whether it is bringing an established production line back to the U.S. or building one for a company's next generation product, collaboration with the right outsourcing partner can essentially make a company's reshoring transition seamless from a customer point of view. Of course, the key is picking the right outsource partner.

Picking the right outsourcing partner

The very first things to consider when deciding to choose a domestic outsource partner to smooth your company's reshoring transition is their size and experience in your particular industry. Are they large enough, and do they have the resources to give you the level of manufacturing support you require? On the other hand, are they so large with so many clients that your project won't receive the attention and support needed for it to succeed? Most importantly, do they have experience in your industry or one that is closely related?

An outsourcing company with lots of semiconductor manufacturing experience, for example, may be an excellent partner for a company in other high technology industries such as LED, flat panel or solar manufacturing, but it may not be the best choice for a company manufacturing home appliances.

Finally, you need to consider the kind of working relationship you want to have with your partner. Do you want a very close association with a lot of communication between your team and theirs? Would you rather have a more hands-off approach, where you provide them the project specifications and expect only periodic updates unless a problem arises? Is their preferred working relationship compatible with yours? Getting the answers to all these questions will require research in terms of formal references, word of mouth from others in your industry and online research, but the time spent researching your potential partners upfront will pay dividends in the long run.

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