

Solid State TECHNOLOGY

Insights for Electronics Manufacturing

Monolithic 3D
Processing

P. 18

Diamond for RF
Power Amplifiers

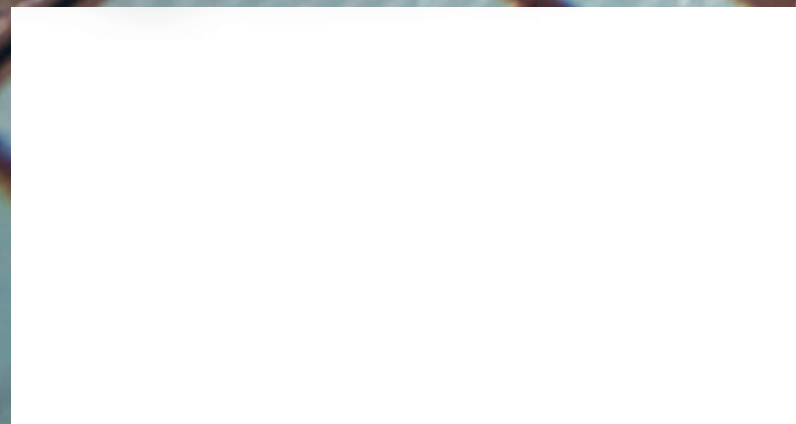
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Structural and
Optical Properties
of Silicon Nitride

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ITRS 2.0: Heterogeneous Integration

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Wafer with poly-SiGe MEMS (accelerometers, resonators, test structures for mechanical testing and for the development of a MEMS packaging process). Source: imec.

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ROADMAP | ITRS 2.0: Heterogeneous Integration

Interconnecting transistors and other components in the IC, in the package, on the printed circuit board and at the system and global network level, are where the future limitations in performance, power, latency and cost reside. *Bill Chen, ASE US, Sunnyvale, CA; Bill Bottoms, 3MT Solutions, Santa Clara, CA, Dave Armstrong, Advantest, Fort Collins, CO; and Atsunobu Isobayashi, Toshiba Kangawa, Japan.*

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3D INTEGRATION | Monolithic 3D processing using non-equilibrium RTP

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IoT demands new standards, better security

At the recent Global Semiconductor Alliance (GSA) "Silicon Summit" one of the topics of discussion was the Internet of Things. Estimates vary, but there could be 30 billion or more devices connected to the internet by 2020.

There is a huge opportunity for the semiconductor industry, and it may require some quick development of standards and new approaches to security.

As reported by our contributing editor Jeff Dorsch, Gregg Bartlett, senior vice president of the Product Management Group at GLOBALFOUNDRIES said "A lot of the infrastructure is in place," yet the lack of IoT standards is inhibiting development.

"IoT demands the continuation of Moore's Law," Bartlett said, touting fully-depleted silicon-on-insulator technology as a cost-effective alternative to FinFET technology. FD-SOI "is the killer technology for IoT," he added.

Also speaking at the event was James Stansberry, senior vice president and general manager of IoT Products at Silicon Laboratories. Energy efficiency is crucial for IoT-related devices, which must be able to operate for 10 years with little or no external power, he said.

Bluetooth Smart, Thread, Wi-Fi, and ZigBee provide the connectivity in IoT networks, with a future role for Long-Term Evolution, according to Stansberry. He also

played up the importance of integration in connected devices. "Nonvolatile memory has to go on the chip" for an IoT system-on-a-chip device, he said.

For 2015, Stansberry predicted a dramatic reduction in energy consumption for IoT devices; low-power connectivity standards will gain traction; and the emergence of more IoT SoCs.

Rahul Patel, Broadcom's senior vice president and general manager of wireless connectivity, addressed health-care applications for the IoT. "Security is key," he said. Reliability, interoperability, and compliance with government regulations are also required, Patel noted.

"My agenda is to scare everyone to death," said Martin Scott, senior vice president and general manager of the Cryptography Research Division at Rambus. Cybersecurity with the IoT is causing much anxiety, he noted. "Silicon can come to the rescue again," he said. "If your system relies on software, it's hackable."

To build trust in IoT devices and networks, the industry needs to turn to silicon-based security, according to Scott. "Silicon is the foundation of trusted services," he concluded.

—Pete Singer, Editor-in-Chief

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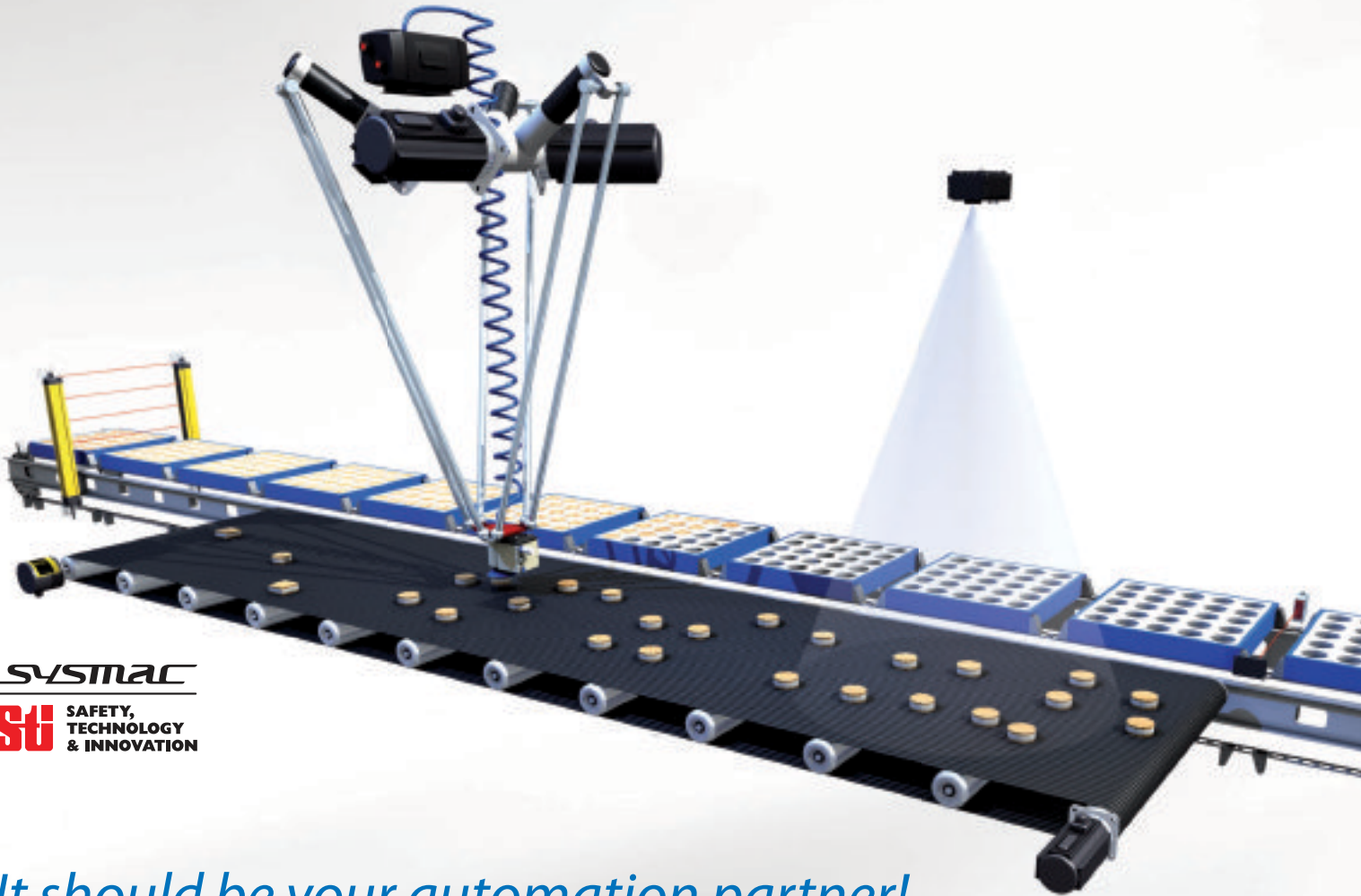
Solid State Technology is published eight times a year by Extension Media LLC, 1786 Street, San Francisco, CA 94107. Copyright © 2015 by Extension Media LLC. All rights reserved. Printed in the U.S.

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1786 18th Street
San Francisco, CA 94107

May 2015, Volume 58, Number 3 • **Solid State Technology** ©2015 (ISSN 0038-111X) **Subscriptions:** Domestic: one year: \$258.00, two years: \$413.00; one year Canada/Mexico: \$360.00, two years: \$573.00; one-year international airmail: \$434.00, two years: \$691.00; Single copy price: \$15.00 in the US, and \$20.00 elsewhere. Digital distribution: \$130.00. You will continue to receive your subscription free of charge. This fee is only for air mail delivery. Address correspondence regarding subscriptions (including change of address) to: **Solid State Technology**, 1786 18th Street, San Francisco, CA 94107-2343. (8 am – 5 pm, PST).

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Web Exclusives

Batteries? We don't need no stinking batteries

We're still used to thinking that low-power chips for "mobile" or "Internet-of-Things (IoT)" applications will be battery powered...but the near ubiquity of lithium-ion cells powering batteries could be threatened by capacitors and energy-harvesting circuits connected to photovoltaic/thermoelectric/piezoelectric micro-power sources.

<http://bit.ly/1DEczEN>

Synopsys founder has plenty of work to do, isn't interested in politics

Aart de Geus is not running for governor of California. The Synopsys chairman and co-CEO denied that speculation in meeting with journalists Monday morning at the 25th annual Synopsys Users Group Conference in Santa Clara, Calif. In any case, Governor Jerry Brown just began his last four-year term, and there's not another gubernatorial election in the Golden State until 2018. (From SemiMD)

<http://bit.ly/1NX6YvL>

Notchless wafer standard approved

450mm notchless wafer standardization has been under discussion for over a year. Driven by the G450C Consortium, the proposed changes will improve wafer symmetry, but more importantly, increase the utilization of wafer surface area.

<http://bit.ly/18Y4v6k>

Insights from the Leading Edge: IBM to share technology with China

According to Reuters, IBM Corp has announced that they will share technology with Chinese firms and will actively help build China's industry. IBM's new approach allows Chinese companies to build everything from semiconductor chips and servers based on IBM architecture, to the software that runs on those machines.

<http://bit.ly/1FrSob0>



Samsung's FinFETs ARE in the Galaxy S6!

The much anticipated Samsung Galaxy S6 made an early appearance in our teardown labs last week, thanks to the diligent skills of our trusted logistics guru. We got our hands on the 4G+ version, the SM-G920I, with what Samsung claims is the world's first octa-core 64 bit operating system.

<http://bit.ly/1lwKcws>

Karen's Hamburg MEMS Roadtrip – A Great Gig

My favorite kind of business travel is when I can combine it with either a visit with friends/family or a site visit to a MEMS Industry Group (MIG) member company. This month, before I headed to Copenhagen to host MEMS Executive Congress Europe 2015, I had the pleasure of doing both. In the immortal words of the Beatles, I went to Hamburg because I had a gig.

<http://bit.ly/1PpcvyO>

2015 SPIE Advanced Lithography EUVL Conference – Summary and Analysis

The SPIE AL EUVL Conference was held from February 22-26, 2015 in San Jose, CA. The atmosphere in this year's EUVL Conference was the most positive toward EUVL that I have ever seen. Here, in this blog, I will summarize the papers and data that caught my attention, give my opinion on the latest status of EUVL, and list the challenges that are still to be addressed.

<http://bit.ly/1Bxm9lm>



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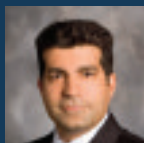
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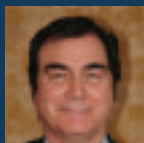
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USA – Cypress and Spansion completed the merger of the two companies in a transaction valued at \$5 billion.

ASIA – TSMC certifies **Synopsys** design tools for 16nm FinFET plus production and for 10nm early design starts

EUROPE – imec and sureCore announced a collaboration on SRAM design IP

USA – Micron and Intel unveiled a new 3D NAND flash memory technology.

ASIA – SEMI hosted **LEDS Taiwan** at TWTC Nangang Exhibition Hall in Taipei.

USA – Ziptronix announced a patent licensing agreement with **Sony Corporation** for application in advanced image sensors.

EUROPE – CEA-Leti announced the launch of Silicon Impulse IC design competence center.

USA – Mentor Graphics announced the acquisition of **Tanner EDA**.

ASIA – STATS ChipPAC announced that **Cavendish Kinetics** has adopted its advanced wafer level packaging technology.

USA – Intel honored 21 companies with Preferred Quality Supplier and Achievement Awards.

USA – ULVAC announced the world's first, low temperature PZT sputtering technology.

ASIA – Semiconductor Manufacturing International Corporation ("SMIC") has appointed Dr. Zixue Zhou as the new chairman and executive director of SMIC.

Freescall and NXP agree to \$40 Billion merger

By Shannon Davis, Web Editor

Chipmaker NXP Semiconductors NV announced that it has agreed to buy Freescale Semiconductor Ltd for \$11.8 billion and merge business operations. The combined enterprise values at just over \$40 billion and will create a new leader in the auto and industrial semiconductor markets.

"Financially, this deal makes sense. By being bigger, you limit the impact of the product cycles and volatile end markets," said RBC analyst Doug Freedman.

NXP anticipates achieving cost savings of \$200 million in the first full year after closing the transaction, with a clear path to \$500 million of annual cost synergies. Freescale shareholders will receive \$6.25 in cash and 0.3521 of an NXP ordinary share for each Freescale common share held at the close of the transaction.

This deal is the fourth semiconductor merger and acquisition so far this year, and it will be the biggest of these by far.

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NXP and GlobalFoundries announce production of 40nm embedded non-volatile memory technology

GLOBALFOUNDRIES, a provider of advanced semiconductor manufacturing technology, and NXP Semiconductor N.V., a semiconductor company for secure connection solutions, today announced that they have jointly developed a next-generation embedded non-volatile memory (eNVM), which has resulted in production of 300mm prototype wafers on GLOBALFOUNDRIES' 40-nanometer (nm) process technology platform. GLOBALFOUNDRIES is the first wafer foundry to develop and qualify 40nm eNVM low-power process technology. Volume production is expected in 2016 at its Singapore facility.

The successful execution of joint development and technology production milestones will enable faster time to market of high density on-chip eNVM for innovative applications in a variety of products including identification, near-field-communication, health-care, and microcontrollers. NXP will leverage GLOBALFOUNDRIES' leading-edge semiconductor manufacturing capability to apply the

Continued on page 8

Apple dictates the ranking of top 10 MEMS manufacturers in 2014

Bosch #1

Bosch reinforced its leadership in the MEMS industry in 2014 with a 16.6 percent increase to \$1167 million up from \$1001 million in 2013. Bosch alone held 12 percent of the very fragmented MEMS market in 2014 compared to 11 percent in 2012.

Bosch took the leadership in 2013 thanks to its design in the Apple iPhone 5s and iPad with its accelerometer. Apple boosted Bosch's MEMS revenue in 2014 again as Bosch is the sole supplier of the pressure sensors added to the iPhone 6 and 6+. Besides Apple, Bosch enjoyed a strong growth of its motion combo sensors with Sony both for gaming with the Sony PS4 and for handsets and tablets. Bosch started going after the consumer MEMS market in 2005 when it created Bosch Sensortec. It added MEMS microphone to its portfolio with the acquisition of Akustica in 2009. Bosch's bet on consumer applications paid off as this segment now accounted for a third of Bosch's total MEMS revenue in 2014 compared to less than 18 percent in 2012.

The legacy automotive business continues to dominate Bosch's MEMS revenue with 67 percent in 2014. Bosch is the undisputed leader in automotive MEMS with 30 percent market shares in 2014 and with revenue more than three times as high as the 2nd largest Automotive MEMS maker Denso.

Texas Instrument #2

Texas Instrument enjoyed a rebound of its Digital Light Processing business in 2014 with an estimated \$805 million up from \$709 million in 2013. The business growth in 2014 was seen mostly in the main business line of DLP business projector segment using TI's Digital Micromirror Device (DMD). TI's DLP business had declined from 2010 to 2013 as Epson – TI's DLP's main competitor with its (non-MEMS) LCD technology – won shares in the projector business. Also the business projector market suffered in the past few years from the competition from low cost LCD flat panels being used as an alternative to projectors for many conference rooms,

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Continued from page 6

Earlier this year, Avago Technologies agreed to would buy wireless networking company Emulex Corp for more than \$600 million, while MaxLinear said it would buy Entropic Communications Inc for \$287 million. In January, Lattice Semiconductor announced the acquisition of Silicon Image for \$600 million.

Freescale was originally created as a division of Motorola in 1948, which would become one of the world's first semiconductor businesses. Freescale would eventually leave Motorola in 2004, to be acquired in 2006 by Blackstone Group LP, Carlyle Group LP, TPG and Permira. Now based out of Austin, Texas, Freescale currently operates in more than 25 countries, while generating net sales of \$4.6 billion in 2014.

NXP is based in Eindhoven, the Netherlands and has operation in more than 25 countries, generating revenue of \$5.7 billion in 2014.

"In the short-term, we will continue to benefit with the secular trend of increasing semiconductor content in auto market. The trend has a positive effect on both companies' portfolio of products. Longer term, the merged company is superbly positioned to become the thought leader in the merging areas of secure cars and Advanced Driver Assistance Systems to facilitate smarter driving," NXP said on a Monday investor call.

The transaction is expected to close the second half of the 2015 calendar year, after which Freescale shareholders will own approximately 32 percent of the combined company.

Credit Suisse acted as financial adviser to NXP, while Morgan Stanley advised Freescale. ▶

Continued from page 6

overall technology to 40nm eNVM that will bring competitive value to end customers.

"We are pleased to see the co-developed 40nm-LP eNVM technology is ready for production in GLOBALFOUNDRIES facility," said Dr. Hai Wang, executive vice president of Technology and Operations at NXP Semiconductor. "GLOBALFOUNDRIES is the first foundry that developed this process technology specifically targeting markets that require embedded non-volatile memory products. The successful release to production will enable NXP to further strengthen our market leadership in offering advanced solutions for secure and near field communication market segments."

"We have a long-standing and close collaboration with NXP across other technology nodes. The successful joint development of eNVM gives us a boost in our confidence in the marketplace as we advance our 40nm technology leadership," said KC Ang, SVP and GM for GLOBALFOUNDRIES Singapore. "We look forward to having additional eNVM technology offerings for future market opportunities."

GLOBALFOUNDRIES' manufacturing site in Singapore is certified by the German Federal Office for Information Security (BSI) for secure IC products manufacturing. In 2012, the foundry received Common Criteria ISO 15408-EAL 6 certification and successfully received renewal in 2014. The company is also a two-time winner of NXP annual supplier award for best foundry services. ▶

Continued from page 7

especially in Asia region. TI won back shares in the projection display market against Epson's LCD technology last year.

STMicroelectronics #3

ST's MEMS business suffered a 19 percent decline in revenue from \$777 million to \$630 million. ST is still the #1 MEMS manufacturer for consumer and mobile applications with 15 percent of this segment. The historical MEMS business of ST i.e. motion sensors for consumer applications has been hit as ST lost its spot in the latest iPhone for the accelerometer in 2013 and for the gyroscope in 2014 and as

well as for the combo motion sensors in the Samsung Galaxy S5. In this game of musical chair ST mitigated the damage however by winning 100 percent of the pressure sensor in the Galaxy S5.

ST has laid in 2014 the foundation for a rebound of its MEMS business in 2015. Especially ST's MEMS microphone is growing very fast thanks to the design win in the iPhone 6 in addition to ST's existing microphone sales into the iPad. ST's MEMS microphone shipment grew more than 2.5 times in 2014 and IHS expects the Apple design win to attract further customers.

The decline of inkjet makers (HP #4th

and Canon #7th)

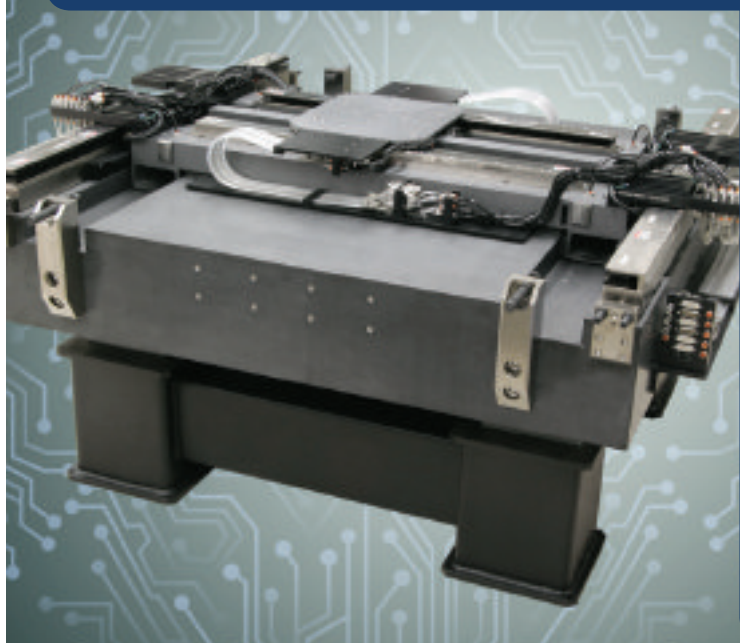
HP #4th and Canon #7th continue to see the revenue associated to their MEMS inkjet printheads declining. Canon saw a slight decline of its inkjet printer sales. Sales of inkjet printers were up 1 percent for HP in 2014 but the shipment of inkjet is declining since HP started the transition from disposable printheads (which are part of the ink cartridge) to permanent printheads in 2006.

Knowles #5

After enjoying a 19 percent and 50 percent growth respectively in 2012 and 2013, Knowles saw its MEMS

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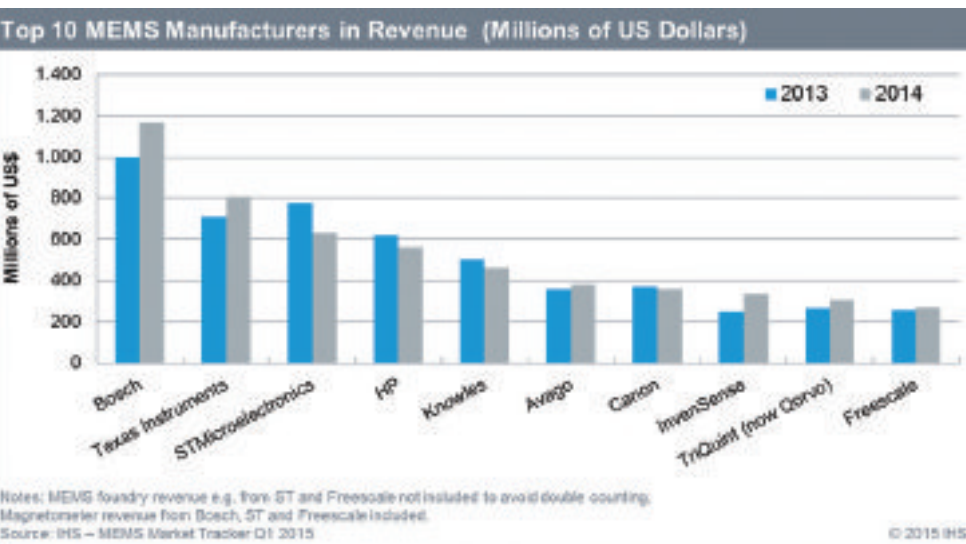
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microphone revenue decline 9 percent from \$505 to \$460 million in 2014. While Apple was largely responsible for the formidable year 2013 as Knowles won a second spot in the iPhone 5S, the decline in 2014 was also related to the iPhone. Early teardowns by IHS of the iPhone 6 and 6+ reveal that Knowles was present with ST and AAC in the first batch of iPhones. Knowles dropped out of the supply chain however due to a technical defect leaving the business to ST, AAC and the new-comer Goertek. Still Knowles remains by far the top MEMS microphone supplier with more than 45 percent units shares. It is also the second largest MEMS manufacturer for consumer and mobile applications with 12 percent revenue share. IHS believes that Knowles will resume with revenue growth in 2015 as it starts shipping to Apple again.

BAW filters makers continue to thrive on LTE (Avago #6th and TriQuint)

Avago and TriQuint grew 6 percent and 15 percent respectively their MEMS based BAW filter business. The LTE band is a boon for the two BAW filter makers, especially in the 2.3 GHz to 2.7 GHz bands, as BAW devices perform better than SAW filters at these frequencies, and solve the coexistence issues of Wi-Fi and LTE. The BAW filter market is currently



experiencing resurgence thanks to LTE and as the number of bands in handsets keeps increasing.

InvenSense # 8

InvenSense was the fastest growing company in the top 10 with an impressive 34 percent jump to \$332 million. The vast majority of his jump comes from InvenSense win of the 6-axis motion combo sensor in the iPhone 6 and 6+. InvenSense has also been very successful with its gyroscope built into camera modules for Optical Image Stabilization (OIS).

Freescale # 10

Rounding up the top 10, Freescale saw its MEMS revenue grow 6 percent to \$271 million in 2014. Automotive continue to make up for around 80 percent of Freescale's. Freescale

enjoyed especially a robust expansion of its pressure sensor sales for Tire Pressure Monitoring Applications.

In March 2015 NXP and Freescale announced a merger. There is no overlap on the sensor side. NXP has had various MEMS developments in the past 10 years (RF MEMS switches, MEMS timing...) but nothing has come in production yet. NXP is however one of the leading magnetic sensor suppliers for automotive. The new entity will become the leading merchant supplier of automotive semiconductor sensors with a very strong position in chassis and safety applications especially. NXP is also the leading suppliers of microcontrollers used as sensor hubs as it produces the sensor hubs for the Apple iPhone and iPads. ◀

Apple watch launch confirms WiFi inside

At the Apple event back on March 9 it was almost a case of last and least for the Apple Watch, after listening through the ResearchKit and new MacBook launches, and more Apple Pay demos. The Watch presentation was almost a case of déjà vu, since we got most of the details last year in the announcement last September.

The one new technical detail that I did pick up on was that the use of WiFi was confirmed – there was no mention of that last year. There was also much emphasis on the ability to use Apple Pay and make calls through the Watch, so we know that there are microphones in there, and it has NFC (near-field communications) capability, but we knew that after the initial launch last year.

The WiFi news was interesting to us, since we did a pseudo-teardown back then, based on Apple's promo video, and we came to the conclusion that the Broadcom BCM4334 was in the Watch. But no mention of WiFi – what gives? I guess they just forgot, and even in the new launch it was just a passing reference.

We identified the BCM4334 from a layout image of the board inside the Watch that we took from a screen capture of the video, and the characteristic footprint of a flip-chip component.

According to Broadcom, "The BCM4334 is a single-chip dual-band combo device supporting 802.11n, bluetooth 4.0+HS & FM receiver. It provides a complete wireless connectivity system with ultra-low power consumption for mass market smartphone devices. Using advanced

design techniques and 40nm process technology to reduce active and idle power, the BCM4334 is designed to address the needs of

highly mobile devices that require minimal power consumption and compact size while delivering dual-band Wi-Fi connectivity."

So we have WiFi confirmed! In the meantime we've been looking at that board a little more, and we have also confirmed that the NFC and NFC booster chips used in the iPhone 6 and 6 Plus are also present.

Again, we looked at the footprints on the board – nothing quite as characteristic as the Broadcom chip, but knowing the size of the chip package and the solder ball array density gives us a good clue. And knowing the size of the BCM4334, we can work out the sizes of the other chips on the board.

In the iPhone 6 the NFC controller was a NXP 65V10, which contained the PN548 die, and an AMS AS3923 NFC power booster; so it's at least a possibility that Apple will be using them in the Watch.

FIGURE 1 is the AS3923 from the iPhone, showing the 5 x 4 solder ball grid on the bottom of the part. Like the Broadcom chip, it is also a flip-chip-on-board (FCOB), so the die size will be characteristic, and while a 5 x 4 grid is certainly not

unique, the combination of the two gives us reasonable confidence that a matching footprint on the Watch board indicates the presence of an AS3923.

Similarly with the NXP 65V10 (**FIGURE 2**): Here we have a 7 x 7 array, but it and the die size coincide with a footprint on the PCB.

Lastly, a business contact pointed out that the motion sensing is likely done by the same Invensense sensor that was used in the iPhones, the MP67B (probably the MPU6700), and when we looked, again the size and solder pads match. We wrote about this after the iPhone analysis, and in its lowest power mode, it can draw less than 10 μ A. ♦



Dick James,
Chipworks



FIGURE 1. Top and bottom images of AMS AS3923



FIGURE 2. Top and bottom images of NXP 65V10

Packaging



Co-Design of chips, packages and boards

Although the Xpedition was announced last week, it has been used in production for over two years. says five companies have been using it, two of which are extremely large semiconductor companies. “It’s a pretty mature technology,” he said.

Traditionally, chip, package and board designers have used relatively archaic means of communicating, including spreadsheets, whiteboard drawings and Microsoft’s VISIO (a diagramming and vector graphics application). Each group often uses different naming conventions as well, which further complicates co-design efforts. “They try to use non-EDA technology to figure out an EDA problem,” said John Park, Methodology Architect, Systems Design Division at Mentor Graphics (Longmont, CO).

A new product from Mentor Graphics called Xpedition® Package Integrator provides a new methodology and platform in addition to a new suite of EDA tools. The platform enables chip, package and board designers to easily see how changing various design elements impact adjacent designs, an industry first.

Xpedition allows designers to pull in existing data in whatever form they’re presently using and examine different design considerations such as connectivity across all three design domains. “We’re aggregating people’s existing flow. We’re not replacing them,” Park said.

Park said the development of Xpedition was driven by the general need to simplify co-design, but also to address new challenges created by the Internet of Things (IoT) and new technology such as 2.5 and 3D integration and through-silicon-vias (TSVs). “You’re talking fairly sophisticated connectivity management when dealing with multiple die, the interposer and modeling that connectivity all the way up to the boards,” Park said. “It’s a pretty

challenging problem for most people who have historically tried to use

spreadsheets to manage that cross-domain connectivity.”

The Xpedition Package Integrator product also provides the industry’s first formal flow for ball grid array (BGA) ball-map planning and optimization based on an “intelligent pin” concept, defined by user rules. In addition, a new multi-mode connectivity management system (incorporating hardware description language (HDL), spreadsheet and graphical schematic) provides cross-domain pin-mapping and system level cross-domain logical verification (**FIGURE 1**).



Pete Singer,
Editor-in-Chief

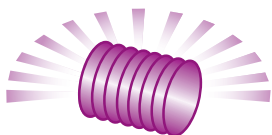


FIGURE 1. With Mentor Graphics Xpedition Package Integrator solution, users manage connectivity in the design environment in which they are most comfortable.

A modern day CPU or GPU has three or four packaging options, such as package-on-package, micro-BGA, or package-on-package (PiP). People are also targeting multiple end form factors. “It’s not a single board anymore,” Park said. “A lot of customers want to look at the device in the context of smartphone platform, a tablet platform or a set-top box platform, for example.”

One of the main advantages of the new platform is cost reduction by efficient layer reduction, optimized interconnect paths, and streamlined/automated control of the design process. “What’s really changing with IoT and with TSVs and expensive packages is people now want to do cross-domain exploration or path finding,” Park said. People evaluate options largely based on cost, performance and reliability. For example, designers want to look at the pros and cons if they take DRAM off the board and move them into the package.

Semiconductors



ITRS 2.0: Heterogeneous Integration

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Interconnecting transistors and other components in the IC, in the package, on the printed circuit board and at the system and global network level, are where the future limitations in performance, power, latency and cost reside.

Heterogeneous Integration refers to the integration of separately manufactured components into a higher level assembly that in the aggregate provides enhanced functionality and improved operating characteristics.

In this definition components should be taken to mean any unit whether individual die, MEMS device, passive component and assembled package or sub-system that are integrated into a single package. The operating characteristics should also be taken in its broadest meaning including characteristics such as system level cost-of-ownership.

The mission of the ITRS Heterogeneous Integration Focus Team is to provide guidance to industry, academia and government to identify key technical challenges with sufficient lead time that they do not become roadblocks preventing the continued progress in electronics that is essential to the future growth of the industry and the realization of the promise of continued positive impact on mankind. The approach is to identify the requirements for heterogeneous integration in the electronics industry through 2030, determine the difficult challenges that must be overcome to meet these requirements and, where possible, identify potential solutions.

Background

The environment is rapidly changing and will require revolutionary changes after 50 years where the change was largely evolutionary. The major factors driving the

need for change are:

- We are approaching the end of Moore's Law scaling
- The emergence of 2.5D and 3D integration techniques
- The emerging world of the internet of everything will cause explosive growth in the need for connectivity
- Mobile devices such as smart phones and tablets are growing rapidly in number and in data communications requirements, driving explosive growth in capacity of the global communications network
- Migration of data, logic and applications to the cloud drives demand for reduction in latency while accommodating this network capacity growth.

Satisfying these emerging demands cannot be accomplished with the current electronics technology and these demands are driving a new and different integration approach. The requirements for power, latency, bandwidth/bandwidth density and cost can only be accomplished by a revolutionary change in the global communications network, with all the components in that network and everything attached to it. Ensuring the reliability of this "future network" in an environment where transistors wear out, will also require innovation in how we design and test the network and its components.

The transistors' power consumption in today's

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network account for less than 10% of total power, total latency and total cost. It is the interconnection of these transistors and other components in the IC, in the package, on the printed circuit board and at the system and global network level, where the future limitations in performance, power, latency and cost reside. Overcoming these limitations will require heterogeneous integration of different materials, different devices (logic, memory, sensors, RF, analog, etc.) and different technologies (electronics, photonics, plasmonics, MEMS and sensors). New materials, manufacturing equipment and processes will be required to accomplish this integration and overcome these limitations.

Difficult challenges

The top-level difficult challenges will be the reduction of power per function, cost per function and latency while continuing the improvements in performance, physical density and reliability. Historically, scaling of transistors has been the primary contributor to meeting required system level improvements. Heterogeneous integration must provide solutions to the non-transistor infrastructure that replace the shortfall from the historical pace of progress we have enjoyed from scaling CMOS. Packaging and test have found it difficult to scale their performance or cost per function to keep pace with transistors and many difficult challenges must be met to maintain the historical pace of progress.

In order to identify the difficult challenges we have selected seven application areas that will drive critical future requirements to focus our work. These areas are:

- Mobile products
- Big data systems and interconnect
- The cloud
- Biomedical products
- Green technology
- The Internet of things
- Automotive components and subsystems

An initial list of difficult challenges for Heterogeneous Integration for these application areas is presented in three categories; (1) on-chip interconnect, (2) assembly and packaging and (3) test. These are analyzed in line with the roadmapping process and will

be used to define the top 10 challenges that have the potential to be “show stoppers” for the seven application areas identified above.

On-chip interconnect difficult challenges

The continued decrease in feature size, increase in transistor count and expansion into 3D structures are presenting many difficult challenges. While challenges in continuous scaling are discussed in the “More Moore” section, the difficult challenges of interconnect technology in devices with 3D structures are listed here. Note that this assumes a 3D structure with TSV, optical interconnects and passive devices in interposer substrates.

- 1. ESD (Electrostatic Discharge):** Plasma damage on transistors by TSV etching especially on via last scheme. Low damage TSV etch process and the layout of protection diodes are the key factors.
- 2. CPI (Chip Package Interaction) Reliability [Process]:** Low fracture toughness of ULK (Ultra Low-k) dielectrics cause failures such as delamination. Material development of ULK with higher modulus and hardness are the key factors.
- 3. CPI (Chip Package Interaction) Reliability [Design]:** A layout optimization is a key for the device using Cu/ULK structure.
- 4. Stress management in TSV [Via Last]:** Yield and reliability in Mx layers where TSV land is a concern.
- 5. Stress management in TSV [Via Middle]:** Stress deformation by copper extrusion in TSV and a KOZ (Keep Out Zone) in transistor layout are the issues.
- 6. Thermal management [Hot Spot]:** Heat dissipation in TSV is an issue. An effective homogenization of hot spot heat either by material or layout optimization are the key factors.
- 7. Thermal management [Warpage]:** Thermal expansion management of each interconnect layer is necessary in thinner Si substrate with TSV.
- 8. Passive Device Integration [Performance]:** Higher Q, in other words, thicker metal lines and lower $\tan \delta$ dielectrics is a key for achieving lower power and lower noise circuits.
- 9. Passive Device Integration [Cost]:** Higher κ

film and higher μ are required for higher density and lower footprint layout.

10. Implementation of Optical Interconnects:

Optical interconnects for signaling, clock distribution, and I/O requires development of a number of optical components such as light sources, photo detectors, modulators, filters and waveguides. On-chip optical interconnects replacing global interconnects requires the breakthrough to overcome the cost issue.

Assembly and packaging difficult challenges

Today assembly and packaging are often the limiting factors in performance, size, latency, power and cost. Although much progress has been made with the introduction of new packaging architectures and processes, with innovations in wafer level packaging and system in package for example, a significantly higher rate of progress is required. The complexity of the challenge is increasing due to unique demands of heterogeneous integration. This includes integration of diverse materials and diverse circuit fabric types into a single SiP architecture and the use of the 3rd dimension.

Difficult packaging challenges by circuit fabric

- **Logic:** Unpredictable hot spot locations, high thermal density, high frequency, unpredictable work load, limited by data bandwidth and data bottle-necks. High bandwidth data access will require new solutions to physical density of bandwidth.
- **Memory:** Thermal density depends on memory type and thermal density differences drive changes in package architecture and materials, thinned device fault models, test & redundancy repair techniques. Packaging must support low latency, high bandwidth large (>1Tb) memory in a hierarchical architecture in a single package and/or SiP).
- **MEMS:** There is a virtually unlimited set of requirements. Issues to be addressed include hermetic vs. non-hermetic, variable functional density, plumbing, stress control, and cost effective test solutions.
- **Photonics:** Extreme sensitivity to thermal changes, O to E and E to O, optical signal connections, new materials, new assembly techniques,

new alignment and test techniques.

- **Plasmonics:** Requirements are yet to be determined, but they will be different from other circuit type. Issues to be addressed include acousto-magneto effects and nonlinear plasmonics.
- **Microfluidics:** Sealing, thermal management and flow control must be incorporated into the package.

Most if not all of these will require new materials and new equipment for assembly and test to meet the 15 year Roadmap requirements.

Difficult packaging challenges by material

- **Semiconductors:** Today the vast majority of semiconductor components are silicon based. In the future both organic and compound semiconductors will be used with a variety of thermal, mechanical and electrical properties; each with unique mechanical, thermal and electrical requirements.
- **Conductors:** Cu has replaced Au and Al in many applications but this is not good enough for future needs. Metal matrix composites and ballistic conductors will be required. Inserting some of these new materials will require new assembly, contacting and joining techniques.
- **Dielectrics:** New high k dielectrics and low k dielectrics will be required. Fracture toughness and interfacial adhesion will be the key parameters. Packaging must provide protection for these fragile materials.
- **Molding compound:** Improved thermal conductivity, thinner layers and lower CTE are key requirements.
- **Adhesives:** Die attach materials, flexible conductors, residue free materials needed or not exist today.
- **Biocompatible materials:** For applications in the healthcare and medical domain (e.g. body patches, implants, smart catheters, electroceuticals), semiconductor-based devices have to be



FIGURE 1. Collaboration priorities.

biocompatible. This involves the integration of new (flexible) materials to comply with specific packaging (form factor) requirements.

Difficult challenges for the testing of heterogeneous devices

The difficulties in testing heterogeneous devices can be broadly separated into three categories: Test Quality Assurance, Test Infrastructure, and Test Design Collaboration.

Test quality assurance needs to comprehend and place achievable quality and reliability metrics for each individual component prior to integration, in order to meet the heterogeneous system quality and reliability targets. Assembly and test flows will become intertwined and interdependent. They need to be constructed in a manner that maintains a cost effective yield loss versus component cost balance and proper component fault isolation and quantification. The industry will be required to integrate components that cannot guarantee KGD without insurmountable cost penalties and this will require integrator visible and accessible repair mechanisms.

Test infrastructure hardware needs to comprehend multiple configurations of the same device to enable test point insertion at partially assembled and fully assembled states. This includes but is not limited to different component heights, asymmetric component locations, and exposed metal contacts (including ESD challenges). Test infrastructure software needs to enable storing and using volume test data for multiple

components that may or may not have been generated within the final integrators data domains but are critical for the final heterogeneous system functionality and quality. It also needs to enable methods for highly granular component tracking for subsequent joint supplier and integrator failure analysis and debug.

Test design collaboration is one of the biggest challenges that the industry will need to overcome. It will be a requirement for heterogeneous highly integrated highly functional systems

to have test features co-designed across component boundaries that have more test coverage and debug capability than simple boundary scans. The challenge of breaking up what was once the responsibility of a wholly contained design for test team across multiple independent entities each trying to protect IP, is only magnified by the additional requirement that the jointly developed test solutions will need to be standardized across multiple competing heterogeneous integrators. Industry wide collaboration on and adherence to test standards will be required in order to maintain cost and time effective design cycles for highly desired components that traditionally has only been required for cross component boundary communication protocols.

The roadmapping process

The objective of ITRS 2.0 for heterogeneous integration is to focus on a limited number of key challenges (10) that have the greatest potential to be “show stoppers”, while leaving other challenges identified and listed but without focus on detailed technical challenges and potential solutions. In this process collaboration with other Focus Teams and Technical Working Groups will be a critical resource. While we will need collaboration with other groups both inside and outside the ITRS some of the collaborations are critical for HI to address its mission. **FIGURE 1** shows the major internal collaborations in three categories.

We expect to review these key challenges and our list of other challenges on a yearly basis and make changes so that our focus keeps up with changes in the key challenges. This will ensure that our efforts remain

focused on the pre-competitive technologies that have the greatest future value to our audience. There are four phases in the process detailed below.

1. Identify challenges for appli-

cation areas: The process would involve collaboration with other focus teams, technical TWGs and other roadmapping groups casting a wide net to identify all gaps and challenges associated with the seven selected application areas as modified from time to time. This list of challenges will be large (perhaps hundreds) and they will be scored by the HI team by difficulty and criticality.

2. Define potential solutions: Using the scoring in phase (1) a number (30-40) will be selected to identify potential solutions. The remainder will be archived for the next cycle of this process. This work will be coordinated with the same collaboration process defined above. These potential solutions will be scored by probable success and cost.

3. Down select to only the 10 most critical challenges: The potential solutions with the lowest probability of success and highest cost will have the potential to be “show stopping” roadblocks. These will be selected using the scoring above and the focus issues for the HI roadmap. The results of this selection process will be communicated to the relevant collaboration partners for their comments.

4. Develop a roadmap of potential solutions for “show stoppers”: The roadmap developed for the “show stopping” roadblocks shall include analysis of the blocking issue and identification of a number of potential solutions. The collaboration shall include detail work with other units of the ITRS, other roadmapping activity such as the Jisso Roadmap, iNEMI Roadmap, Communications Technology Roadmap from MIT. We are continuing to work with the global technical community: industry, research institutes and academia, including the IEEE CPMT Society.

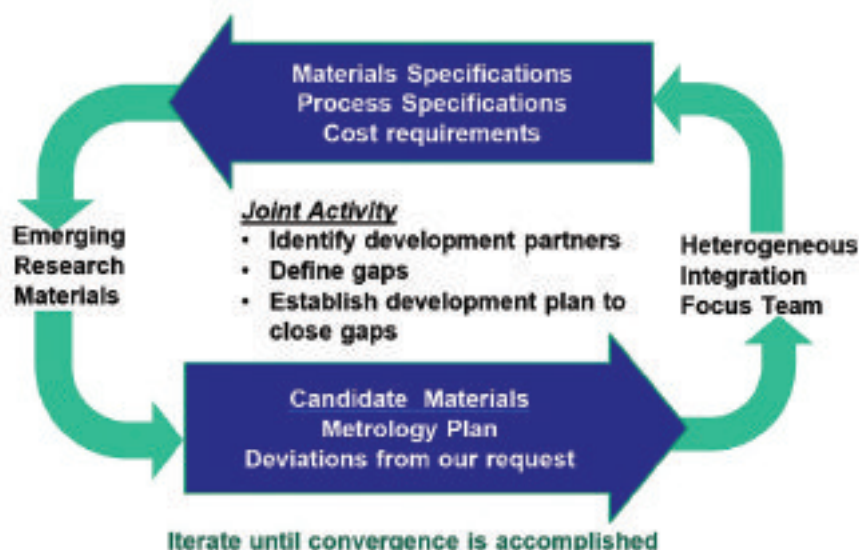


FIGURE 2. Iterative collaboration process

The blocking issues will be specifically investigated by the leading experts within the ITRS structure, academia, industry, government and research organizations to ensure a broad based understanding. Potential solutions will be identified through a similar collaboration process and evaluated through a series of focused workshops similar to the process used by the ERD iTWG. This process is a workshop where there is one proponents and one critic presenting to the group. This is followed by a discussion and a voting process which may have several iterations to reach a consensus.

The cross Focus Team/TWG collaboration will use a procedure of iteration to converge on an understanding of the challenges and potential solutions that is self-consistent across the ITRS structure. An example is illustrated in **FIGURE 2**.

It is critically important that our time horizon include the full 15 years of the ITRS. The work to anticipate the true roadblocks for heterogeneous integration, define potential solutions and implement a successful solution may require the full 15 years. Among the tables we will include 5 year check points of the major challenges for the key issues of cost, power, latency and bandwidth. In order for this table to be useful we will face the challenge of identifying the specific metric or metrics to be used for each application driver as we prepare the Heterogeneous Integration roadmap chapter for 2015 and beyond. ♦

Monolithic 3D processing using non-equilibrium RTP

ED KORCZYNSKI, Senior Technical Editor

When pavement ends the terrain gets rough, as documented in the Emerging Research Materials chapter of newest ITRS.

Slightly more than one year after Qualcomm Technologies announced that it was assessing CEA-Leti's monolithic 3D (M3D) transistor stacking technology, Qualcomm has now announced that M3D will be used instead of through-silicon vias (TSV) in the company's next generation of cellphone handset chips. Since Qualcomm had also been a leading industrial proponent of TSV over the last few years while participating in the imec R&D consortium, this endorsement of M3D is particularly relevant.

Leti's approach to 3D stacking of transistors starts with a conventionally built and locally-interconnected bottom layer of transistors, which are then covered with a top layer of transistors built using relatively low-temperature processes branded as "CoolCube." (<http://electroiq.com/blog/2014/12/leti-will-discuss-coolcube-technology-for-3d-transistor-stacking-at-workshop-preceding-iedm-2014/>) **FIGURE 1** shows a simplified cross-sectional schematic of a CoolCube stack of transistors and interconnects. CoolCube M3D does not transfer a layer of built devices as in the approach using TSV, but instead transfers just a nm-thin layer of homogenous semiconducting material for subsequent device processing.

The reason that completed transistors are not transferred in the first place is because of intrinsic alignment issues, which are eliminated when transistors are instead fabricated on the same wafer. "We have lots of data to prove that alignment precision is as good as can be seen in 2D lithography,

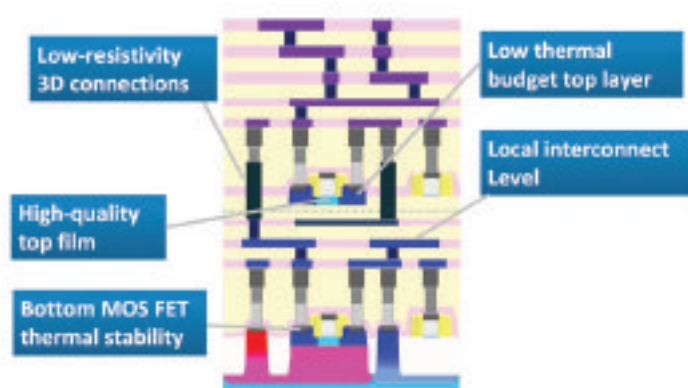


FIGURE 1. Simplified cross-sectional rendering of Monolithic 3D (M3D) transistor stacks, with critical process integration challenges indicated. (Source: CEA-Leti)

typically 3nm," explained Maud Vinet, Leti's advanced CMOS laboratory manager in an exclusive interview with SST.

As discussed in a blog post online at Semiconductor Manufacturing and Design (<http://semimd.com/hars/2014/04/09/going-up-monolithic-3d-as-an-alternative-to-cmos-scaling/>) last year by Leti researchers, the M3D approach consists of sequentially processing:

- processing a bottom MOS transistor layer with local interconnects,
- bonding a wafer substrate to the bottom transistor layer,
- chemical-mechanical planarization (CMP) and SPE of the top layer,
- processing the top device layer,
- forming metal vias between the two device layers

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- as interconnects, and
- standard copper/low-k multi-level interconnect formation.

To transfer a layer of silicon for the top layer of transistors, a cleave-layer is needed within the bulk silicon or else time and money would be wasted in grinding away >95% of the silicon bulk from the backside. For CMOS:CMOS M3D thin silicon-on-insulator (SOI) is the transferred top layer, a logical extension of work done by Leti for decades. The heavy dose ion-implantation that creates the cleave-layer leaves defects in crystalline silicon which require excessively high temperatures to anneal away. Leti's trick to overcome this thermal-budget issue is to use pre-amorphizing implants (PAI) to completely dis-order the silicon before transfer and then solid-phase epitaxy (SPE) post-transfer to grow device-grade single-crystal silicon at ~500°C.

Since neither aluminum nor copper interconnects can withstand this temperature range, the interconnects for the bottom layer of transistors need to be tungsten wires with the highest melting point of any metal but somewhat worse electrical resistance (R). Protection for the lower wires cannot use low-k dielectrics, but must use relatively higher capacitance (C) oxides. However, the increased RC delay in the lower interconnects is more than offset by the orders-of-magnitude reduction in interconnect lengths due to vertical stacking.

M3D Roadmaps

Leti shows data that M3D transistor stacking can provide immediate benefit to industry by combining two 28nm-node CMOS layers instead of trying to design and manufacture a single 14nm-node CMOS layer: area gain 55%, performance gain 23%, and power gain 12%. With cost/transistor now expected to increase with sequential nodes, M3D thus provides a way to reduce cost and risk when developing new ICs.

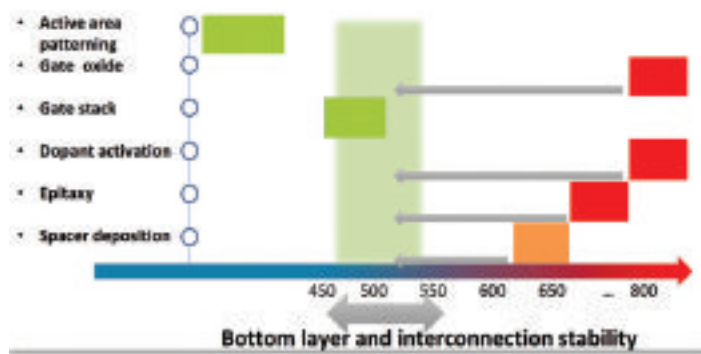


FIGURE 2. Thermal processing ranges for process modules need to be below ~500°C for the top devices in M3D stacks to prevent degradation of the bottom layer. (Source: CEA-Leti)

For the industry to use M3D, there are some unique new unit-processes that will need to ramp into high-volume manufacturing (HVM) to ensure profitable line yield. As presented by C. Fenouillet-Beranger et al. from Leti and ST (paper 27.5) at IEDM2014 in San Francisco, “New Insights on Bottom Layer Thermal

Stability and Laser Annealing Promises for High Performance 3D Monolithic Integration,” due to stability improvement in bottom transistors found through the use of doping nickel-silicide with a noble metal such as platinum, the top MOSFET processing temperature could be relaxed up to 500°C. Laser RTP annealing then allows for the activation of top MOSFETs junctions, which have been characterized morphologically and electrically as promising for high performance ICs.

FIGURE 2 shows the new unit-processes at ≤500°C that need to be developed for top transistor formation:

- * Gate-oxide formation,
- * Dopant activation,
- * Epitaxy, and
- * Spacer deposition.

After the above unit-processes have been integrated into high-yielding process modules for CMOS:CMOS stacking, heterogeneous integration of different types of devices are on the roadmap for M3D. Leti has already shown proof-of-concept for processes that integrate new IC functionalities into future M3D stacks:

- 1) CMOS:CMOS,
- 2) PMOS:NMOS,
- 3) III-V:Ge, and
- 4) MEMS/NEMS:CMOS.

Thomas Ernst, senior scientist, Electron Nanodevice Architectures, Leti, commented to SST, “Any application that will need a ‘pixelated’ device

architecture would likely use M3D. In addition, this approach will work well for integrating new channel materials such as III-V's and germanium, and any materials that can be deposited at relatively low temperatures such as the active layers in gas-sensors or resistive-memory cells."

Non-Equilibrium Thermal Processing

Though the use of an oxide barrier between the active device layers provides significant thermal protection to the bottom layer of devices during top-layer fabrication, the thermal processes of the latter cannot be run at equilibrium. "One way of controlling the thermal budget is to use what we sometimes call the *crème brûlée* approach to only heat the very top surface while keeping the inside cool," explained Vinet. "Everyone knows that you want a nice crispy top surface with cool custard beneath." Using a laser with a short wavelength prevents penetration into lower layers such that essentially all of the energy is absorbed in the surface layer in a manner that can be considered as adiabatic.

Applied Materials has been a supplier-partner with Leti in developing M3D, and the company provided responses from executive technologists to queries from SST about the general industry trend to controlling short pulses of light for thermal processing. "Laser non-equilibrium heating is enabling technology for 3D devices," affirmed Steve Moffatt, chief technology officer, Front End Products, Applied Materials. "The idea is to heat the top layer and not the layers below. To achieve very shallow adiabatic heating the toolset needs to ramp up in less than 100 nsec. In order to get strong absorption in the top surface, shorter wavelengths are useful, less than 800 nm. Laser non-equilibrium heating in this regime can be a critical process for building monolithic 3D structures for SOC and logic devices."

Of course, with ultra-shallow junctions (USJ) and atomic-scale gate-stacks already in use for CMOS transistors at the 22nm-node, non-equilibrium thermal processing has already been used in leading fabs. "Gate dielectric, gate metal, and contact treatments are areas where we have seen non-equilibrium anneals slowly taking the place of conventional RTP," clarified Abhilash Mayur, senior director,

Front End Products, Applied Materials. "For approximate percentages, I would say about 25 percent of thermal processing for logic at the 22nm-node is non-equilibrium, and seen to be heading toward 50 percent at the 10nm-node or lower."

Mayur further explained some of the trade-offs in working on the leading-edge of thermal processing for demanding HVM customers. Pulse-times are in the tens of nsec, with longer pulses tending to allow the heat to diffuse deeper and adversely alter the lower layers, and with shorter pulses tending to induce surface damage or ablation. "Our roadmap is to ensure flexibility in the pulse shape to tailor the heat flow to the specific application," said Mayur.

Now that Qualcomm has endorsed CoolCube M3D as a preferred approach to CMOS:CMOS transistor stacking in the near-term, we may assume that R&D in novel unit-processes has mostly concluded. Presumably there are pilot lots of wafers now being run through commercial foundries to fine-tune M3D integration. With a roadmap for long-term heterogeneous integration that seems both low-cost and low-risk, M3D using non-equilibrium RTP will likely be an important way to integrate new functionalities into future ICs. ♦

Enhanced thermal management solutions for RF power amplifiers

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Synthetic diamond heat spreaders and GaN-on-Diamond wafers have emerged as a leading thermal-management technology for RF Power Amplifiers

GaN-based transistors and their related RF Power Amplifiers (PAs) have emerged as the leading solid-state technology to replace traveling wave tubes in radar, EW (Electronic warfare) systems, and satellite communications, and to replace GaAs transistors in cellular base stations. However, significant thermal limitations prevent GaN PAs from reaching their intrinsic performance capability. Metallized synthetic diamond heat spreaders have recently been used to address this thermal management challenge, particularly in cellular base station and military radar applications.

This article covers several important issues that advanced thermal solutions, particularly for RF power amplifiers, must address. Here, we are presenting new materials, such as CVD (chemical vapor deposition) diamond as a heat spreader to reduce overall package thermal resistance compared to today's more commonly used materials for thermal management. Also, mounting aspects and some new developments regarding the thermal

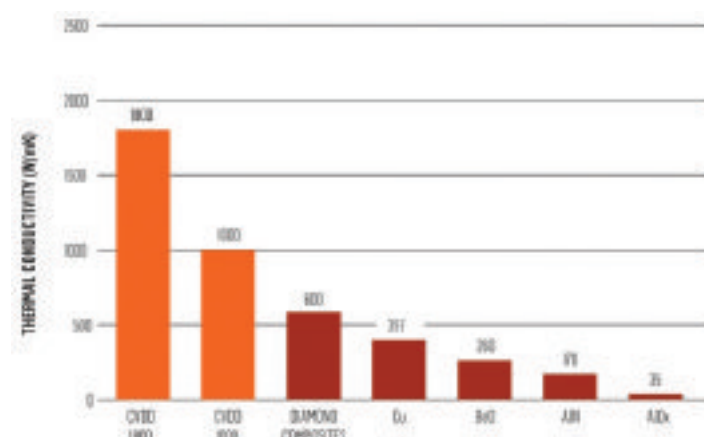


FIGURE 1. Comparison of thermal conductivity of CVD diamond and traditional heat spreading materials [1, 2].

resistance at the bonding interfaces to diamond heat spreaders are discussed.

CVD diamond

Diamond possesses an extraordinary set of properties including the highest known thermal conductivity, stiffness and hardness, combined with high optical transmission across a wide

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wavelength range, low expansion coefficient, and low density. These characteristics can make diamond a material of choice for thermal management to significantly reduce thermal resistance. CVD diamond is now readily commercially available in different grades with thermal conductivities ranging from 1000 to 2000 W/mK. Also very important is the fact that CVD diamond can be engineered to have fully isotropic characteristics, enabling enhanced heat spreading in all directions. **FIGURE 1** shows a comparison of the thermal conductivity of CVD diamond with other materials traditionally used for heat spreading purposes.

On-going development in the technologies to synthesize CVD diamond has enabled it to become readily available in volume at acceptable costs. Unmetallized CVD diamond heat spreaders are available today at a typical volume cost of \$1/mm³. Prices vary dependant on the thermal-conductivity grade used. In some instances, system operation at elevated temperatures can reduce both the initial cost of the cooling sub-system and the on-going operating cost as well. When applied with appropriate die-attach methods, diamond heat spreaders provide reliable solutions for semiconductor packages with significant thermal management challenges [1].

Application notes for the use of CVD Diamond

To obtain the most effective use of the extreme properties of CVD Diamond in overall system design, package integration issues need to be carefully considered. Failure to address any one of these issues will result in a sub-optimal thermal solution. Here are the most important points to be considered:

- Surface preparation

- Mounting techniques
- Diamond thickness
- Functional considerations.
- Metallizations and thermal barrier resistance

Surface preparation: The surfaces of die-level devices have to be machined in a suitable fashion to allow good heat transfer. Surface flatness for heat spreaders should typically be less than 1

micron/mm and the roughness better than Ra < 50 nm, which can be achieved by polishing techniques. Any deficiency in flatness must be compensated for by the mounting techniques which will cause higher thermal resistance.

Mounting techniques: Whereas in some

advanced device applications, such as high-power laser diodes, atomic-force bonding techniques are being considered, most applications currently employ soldering techniques for die attachment to the heat spreader. Again, solder layers should be kept to minimum thickness, particularly for the primary TIM1 (thermal interface material (TIM) between die and heat spreader), to minimize thermal resistance. An important factor in applying solder joints is the expansion mismatch between the CVD diamond and the semiconductor material, as it can significantly influence performance and lifetime. GaAs (Gallium Arsenide) devices up to an edge length of 2.5 mm can be hard soldered to CVD diamond without CTE-mismatch problems. (Note that the CTE for CVD Diamond is 1.0 ppm/K at 300K). For edge lengths greater than 2.5 mm, using a soft solder can avoid excessive stresses in the device. **TABLE 1** shows a wide range of solder materials commercially available to address various needs for soldering processes.

Diamond thickness: The thickness of the CVD diamond is important. For devices with small

SOLDER MATERIAL	COMPOSITION (wt%)	SOFT / HARD	LIQUIDUS TEMP. (°C)	SOLIDUS TEMP. (°C)
InSn	51 / 49	Soft	118	eutectic
InSe	80 / 20	Soft	125	118
InAg	82 / 18	Soft	143	eutectic
In	Pure	Soft	156.6	156.6
InPb	10 / 90	Soft	171	162
SnPbAg	82 / 18 / 1	Soft	179	eutectic
SnPb	83 / 17	Soft	183	eutectic
SnPb	60 / 40	Soft	181	183
AgSn	3.5 / 96.5	Soft	231	eutectic
AuSn	80 / 20	Hard	278	eutectic
AuSn	19 / 81	Hard	355	278
AuGe	88 / 12	Hard	361	eutectic
AuSi	82 / 18	Hard	363	eutectic
AuSn	73 / 27	Hard	378	278

TABLE 1. Summary of soldering materials [2].

hot spots, such as RF amplifiers or laser diodes, a thickness of 250 to 400 microns is sufficient. Diamond's isotropic characteristics effectively spread the heat to reduce maximum operation temperature at constant power output. However, applications with larger heat spots on the order of 1 to 10 mm in diameter require thicker diamond for better results. An example is disk lasers that can have an optical output power of several kW and a power density of about 2kW/cm²; a diamond thickness of several mm has proven to be beneficial to disk laser operation [3].

Functional considerations: There are also functional requirements that may be important. One is the electrical conductivity of the heat spreader. For devices such as laser diodes, it is easiest to run the drive current through the device and use the heat spreader for the ground contact. For other devices, the heat spreader is required to be insulating. As CVD diamond is an intrinsic insulator, this insulation can be maintained by keeping the side faces free of metallization. This could be required for RF amplifiers and transistors, especially at higher frequencies ($f > 2$ GHz).

Thermal simulation helps optimize the heat spreader configuration to find the best solution based on power output needs, material thickness, metallization scheme, heat source geometry and package configuration. For design optimization, it is important that the thermal simulation model includes the complete junction-to-case system, including the device details, all interfaces, materials and the subsequent heat sinking solution.

Metallizations and thermal barrier resistance

Metallizations are an essential component to

the application of CVD diamond in RF Amplifier and similar applications. Typically, for reasons of adhesion, mechanical and thermal robustness, three-layer metallization schemes are used. An example of such a three-layer metallization scheme fundamentally comprises: a) a carbide forming metal layer which forms a carbide bonding to the diamond component; b) a diffusion barrier metal layer disposed over the carbide forming metal layer; and c) a surface metal bonding layer disposed over the diffusion barrier metal which provides both a protective layer and a wettable surface layer onto which a metal solder or metal braze can be applied to bond the diamond heat spreader to die and other device components. A particular example of such a three-layer metallization scheme is Ti / Pt / Au.

High-quality, sputter-deposited, thin-film metallizations are strongly recommended for advanced thermal solutions. As thermal contact resistance between the device and the heat spreader must be minimized, any additional metal interface being added to the system must be avoided. Sputtered layers,

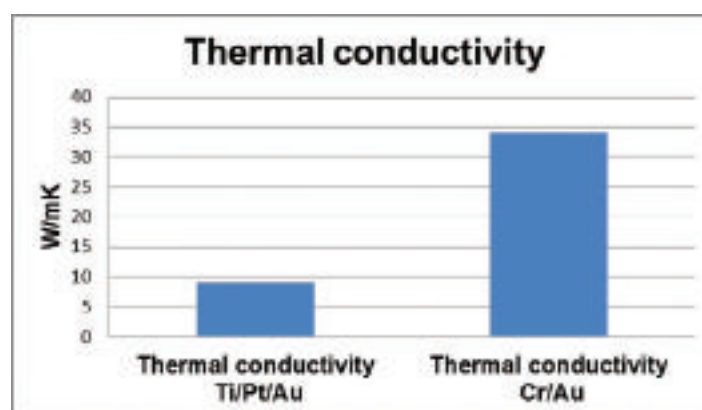


FIGURE 2. Comparison of thermal conductivity of different metallization schemes [4].

especially of titanium, can form a very effective chemical bond with CVD diamond to ensure long-term stability even at elevated temperatures. To separate the required gold attach layer from the titanium adhesion layer, a platinum or titanium / tungsten (TiW) barrier layer is recommended. The Ti/Pt/Au scheme is very commonly used in high-end devices and has excellent characteristics with regards to stability and endurance, even over extended lifetime periods under changing thermal loads. However, this scheme also has a drawback, as the thermal conductivities of the titanium and platinum are relatively low ($T_c = 22$ W/mK and $T_c = 70$ W/mK respectively). In the search for improved materials to be applied, the use of

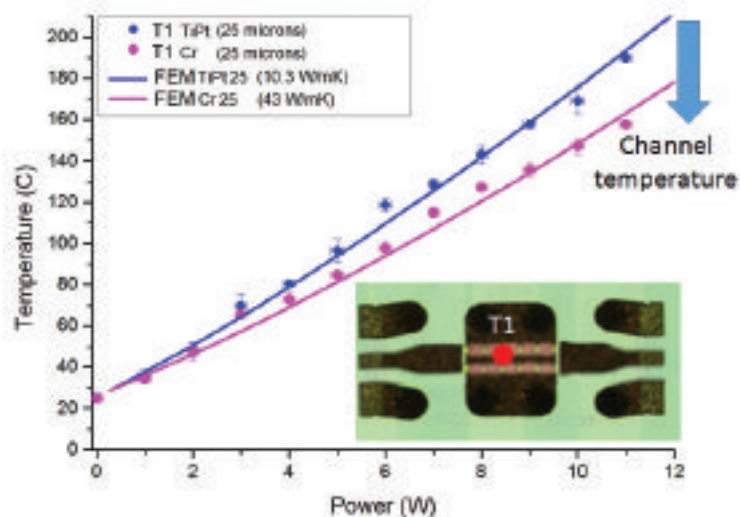
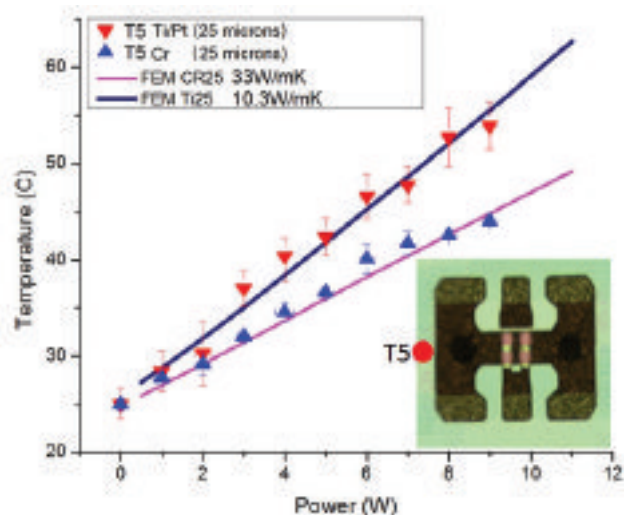


FIGURE 3. Temperatures as a function of power for different metallization schemes and solder thickness [4].

chromium has been identified as a viable alternative. Chromium forms a carbide with diamond and is also readily used as a barrier layer, enabling it to perform both functions at a relatively high thermal conductivity of $T_c = 93.9 \text{ W/mK}$. To test the thermal effectiveness of chromium, samples were prepared at the CDTR (Centre for Device Thermography and Reliability) at Bristol University comparing a standard Ti/Pt/Au (100/120/500nm) metallization with this novel Cr/Au (100/500nm) configuration. The measurements of the thermal conductivity revealed that the thermal conductivity of the Cr/Au metallization is about 4 times higher as compared to the Ti/Pt/Au. Results are shown in **FIGURE 2**.

Application example

To demonstrate the impact of this Cr adhesion/barrier layer advantage versus Ti/Pt/Au, high power GaN on SiC HEMT (High Electron Mobility Transistor) devices were mounted to a CVD Diamond heat spreader. A cap layer of AuSn with a thickness of 25 microns was chosen. To ensure comparable results for all samples prepared, these samples were placed on a temperature stable platform also made from high thermally conductive diamond material. Results are shown in **FIGURE 3**: In the left diagram, the base temperature is plotted for increasing power output from the device. As can be seen, the temperature for the Cr/Au configuration is significantly lower, at 9W

device power output by about 10 degrees C. On the right hand side, the graph shows the temperature as measured on the transistor channel directly. In this case, the lower thermal resistivity of the Cr-based metallization layer decreases the channel temperature by more than 20 degrees C at 9W power output.

This significant temperature reduction will result in as much as a 4 times longer lifetime of the device. Alternatively, such devices could be packaged in smaller footprints, at higher power densities, to make use of this increased effectiveness in heat spreading.

Outlook, future developments

One important finding from the above example is the need to modify device architecture for improved thermal management. The main temperature rise is within the device itself. Here, a thinning of the substrate, to bring it closer to the diamond heat spreader, would further enhance the thermal design. Also, mounting such devices with the active layers facing the diamond would provide even further benefit. An example would be the mounting laser diodes p-face down with the quantum well structures soldered directly against the heat spreader. Another way to bring the device gate junction closer to the diamond is the use of a different substrate altogether. This has been demonstrated by using GaN (Gallium Nitride) on diamond wafers, which remove both the Si

substrate and transition layers, replacing them instead with CVD diamond [5]. The result brings the diamond material within 1 micron of the heat generating gate junctions. Initial users of GaN-on-diamond wafers for RF HEMT devices have demonstrated as much as 3 times the power density when compared to equivalent GaN/SiC (Silicon Carbide) devices, today's leading technology for advanced power devices. [6]

Summary

As can be seen, significant thermal-management improvements to electronic systems can be realized by using advanced materials such as CVD diamond. The integration can be relatively straightforward as the diamond heat spreader can be a direct replacement to AlN (Aluminium nitride), BeO (Berillium oxide) or other advanced ceramics. Attention to detail at the interfaces, both in terms of the choice of metals and its thickness, is important to keep overall thermal resistance low and thereby optimizing the effectiveness of the diamond.

As CVD diamond becomes more attractive as a heat spreader through improved synthesis technology, advanced processing and on-going cost reduction efforts, its use in high power density applications has been increasing. It is expected that this trend will be continued in the years to come in line with the ever increasing need for smaller and more powerful electronic devices and systems.

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Understanding the structural and optical properties of silicon nitride

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Using first-principles calculations, the electronic structures and optical properties that arise on doping-atom-containing silicon nitride systems are reported as a function of dielectric constant, reflectivity, absorption and loss spectra.

The development of hexagonal silicon nitride is concerned predominantly with the design and fabrication of structural materials because of its excellent properties such as high strength, toughness, flexibility and good resistance to thermal shock and oxidation [1-3]. While a great deal is understood of block Si_3N_4 behavior, one of the challenges to exploiting the functionality will be to better understand the variety and corresponding structural features unique to Si_3N_4 . Eliciting a desired output from controlled inputs using pre-designed materials is one of the key aspects of current materials' research field.

A first-principles calculation within the local density approximation suggested that $\beta\text{-Si}_3\text{N}_4$ has a direct band gap of about 4.34 eV. Although the calculated band gap may be somewhat underestimated, owing to the LDA, $\beta\text{-Si}_3\text{N}_4$ is likely to fall into the category of wide-gap semiconductors by appropriate doping [4-5]. Simultaneously, the direct band gap reveals the potential applications as optical or electric devices apart from the structural applications. In order to use $\beta\text{-Si}_3\text{N}_4$ as a semiconductor, it is necessary to find proper dopants.

Recently, there was substantial interest in investigating the properties of Si_3N_4 that combined the

adsorption and doping. Various theoretical methods have been employed to model and understand these behaviors, motivated by the fact that different structures may exhibit desired and fascinating properties. Wang simulated the interaction of O_2 with the $\beta\text{-Si}_3\text{N}_4$ surface and found that the oxidation occurs on the $\beta\text{-Si}_3\text{N}_4$ (0001) surface at 1200°C more easily by means of the calculated significant chemisorption energy and the short adsorption bond length [6]. Oba investigated n- and p-type dopants for cubic silicon nitride and concluded that P and O are preferable for n-type doping, while Al is favorable for p-type doping in terms of the formation and ionization energies [7]. The dependence of the formation energies on the chemical potentials indicates that a proper choice of growth conditions is mandatory for suppressing the incorporation of these impurities into anti and interstitial sites [8]. For the low Al concentration, the material exhibits the dielectric behavior, while the metallic behavior for the high Al concentration [9]. Ching concluded that cations with small radii tend to occupy the tetrahedral site and those with large radii tend to occupy octahedral sites for $\gamma\text{-Si}_3\text{N}_4$, which is likely to show some metallic characteristics at the high Ti concentration [10].

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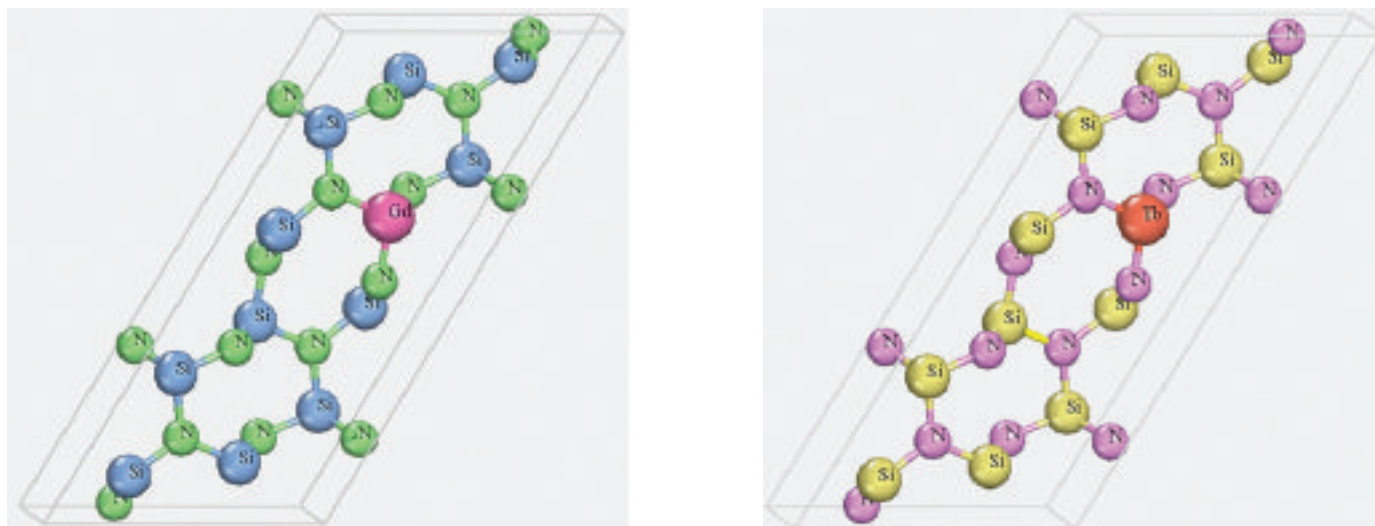


FIGURE 1. Supercells (2×1×1) of doped systems: (a) Ga-doped system; (b) Tb-doped system.

Previously, we have reported the impurity species appropriate to β -Si₃N₄ based on the first-principles calculations [11-13]. In the present contribution, we conducted similar calculations to investigate impurities effects in β -Si₃N₄, as well as the electronic structures and optical properties of rare earth (RE)-doped systems, to obtain the further information in details.

Theoretical approaches and computational procedures

Here, we demonstrated the first-principles calculations using the CASTEP program code with plane-wave pseudopotential (PWP). Our simulation model, detailed in the method section, is summarized in **FIGURE 1** and described briefly here. The hexagonal β -Si₃N₄ unit cell contains two formula units (14 atoms) with a space group P6₃/m. The idealized Si-N layers in an ABAB sequence can depict the structure perfectly. All of the Si atoms are equivalent (6h sites), but there are two inequivalent nitrogen sites: N2c at 2c sites and N6h at 6h sites. The N2c atoms locate in a planar geometry with their three Si nearest neighbors, and N6h atoms locate at slightly puckered sites enclosed by three Si atoms, while Si atoms locate at the center of slightly irregular tetrahedron bonded with one N2c atom and three N6h atoms. Supercells (2×1×1) containing 28 atoms were used to simulate RE-doped β -Si₃N₄. The doping was realized by substituting some Si atoms with Gd and Tb atoms. The core region and valence electrons of the atoms

in the systems were illustrated by the ultrasoft pseudopotential. The lattice constants of primitive cells were determined through calculations using a plane-wave cutoff energy of 770 eV and a 4×4×10 point grid in the irreducible part of the Brillouinzone. The structural optimization was done by relaxing both internal coordinates and the lattice constants by calculating the ab initio forces on the ions, within the Born-Oppenheimer approximation, until the absolute values of the forces were converged to less than 10⁻² eV/Å. The stress level for the equilibrium structure is less than 1×10⁻² GPa and the max displacement is 5×10⁻⁴ Å in supercells.

Results and discussion

Geometry optimization results: Both models are composed of 28-atom, for which the only difference is rare element. The optimization was carried out by relaxing both the internal coordinates and the lattice constants by calculating the ab initio forces on the ions, until the absolute values of the forces were smaller than the set values. The obtained results are summarized in Table 1. Compared to the experiment values, the calculated lattice constants are overestimated within 1%, illustrating a reasonable agreement. Because of the bigger atoms radius of Gd and Tb atoms, the lattice constants and volume increase remarkably after doping. The E_g of Gd-doped system is 0.095 eV, and decreases to 0.073 eV for Tb-doped one due to the narrower distance of the bottom of conduction band and the top of

valence band derived from doping. For the purpose of characterizing the stability of doped structures, the E_b and E_f are brought forward in terms of total energy and total sums of elements free energies, and the atomic chemical potential, respectively, as illustrated in Eqs. (1) and (2).

$$E_b = E_T - E_{sum}$$

$$E_f = E_T - E_{Si_3N_4} + n_{Si}\mu_{Si} - n_X\mu_X$$

where $E_{Si_3N_4}$ and E_T denote the total energies of the supercells before and after doping, respectively. X is doping atom, μ_{Si} and μ_X are the chemical potentials of Si and doping atoms, respectively. Note that E_b of system accounts for its stable degree. The

larger the absolute value is, the more stable the final structure is. The stability of Gd-doped system with small E_b is higher than that of Tb-doped one. The E_f is relative to the chemical potentials of elements and may also exhibit the stability of doped structures. The obtained E_f values for Gd- and Tb-doped systems are 12 and 15 eV, respectively, revealing that the structure of the former is more stable than that of the latter.

Electronic structures: FIGURES 2A and B show the achieved electronic band structures of Gd- and Tb-doped supercells. For Gd-doped system, the E_g drops obviously to 0.095 eV as compared to undoped one (4.336 eV). The valence band (VB) can be divided into three group: the bottom of VB is about -40.94 eV; the next one is in the range of -20.9 and -12.8 eV with a width of 8.1 eV; the top VB locates between -9.62 and 1.15 eV with an extent of 10.77 eV. While for the Tb-doped system, the E_g decreases continuously to 0.073 eV. The VB may also be divided into three group: the bottom of VB is at -42.45 eV; the next one locates between -21.29 and -12.79 eV accompanying a width of 8.5 eV; the top VB is in the range of -9.75 and 0.89 eV with a width of 10.64 eV. It is worth noting that both VBs have higher densities than those of undoped system accompanying the overlap of the energy band although doping with a lower concentration.

In order to analyze further the results according to the band structures, we conduct the densities of states (DOS) coming from the calculations with GGA, as demonstrated in FIGURE 3. The calculated total DOS derives from the partial density (PDOS) of N, Si, Gd, and Tb atoms. The obtained total and partial densities of states for Gd- and Tb-doped systems are displayed in Fig.3a and b, respectively. One can see that for Gd-doped system, there are three valence regions: the lower energy band located between -41.46 and -40.06 eV briefly comes from Gd s orbital electrons; the next energy band in the range of -21.34 and -11.95 eV mainly originates from Gd p and N s orbital electrons; the upper valence band occurs between -9.99 and 1.74 eV is primarily from Gd f and N p states; the conduction band in the range of 3.23 to 6.40 eV principally consists of Si p orbital electrons. The distance between the top valence band

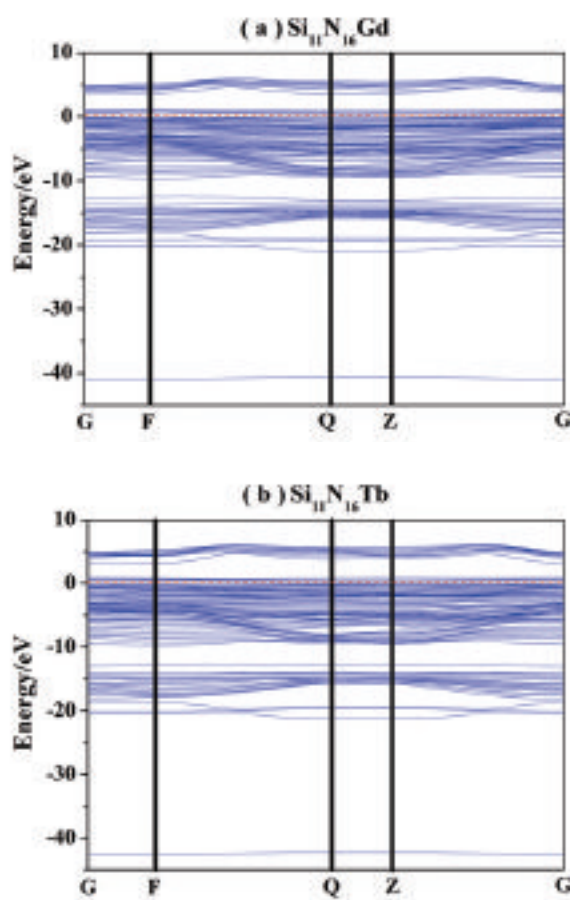


FIGURE 2. Band structures of supercells: (a) Gd-doped system; (b) Tb-doped system.

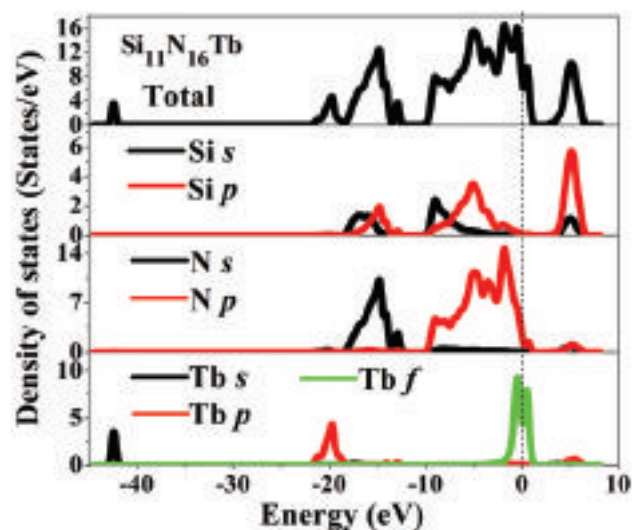
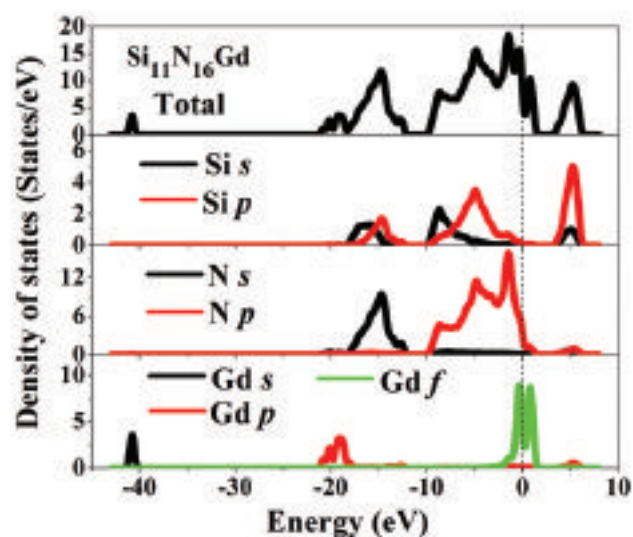


FIGURE 3. Total and partial densities of states: (a) Gd-doped system; (b) Tb-doped system.

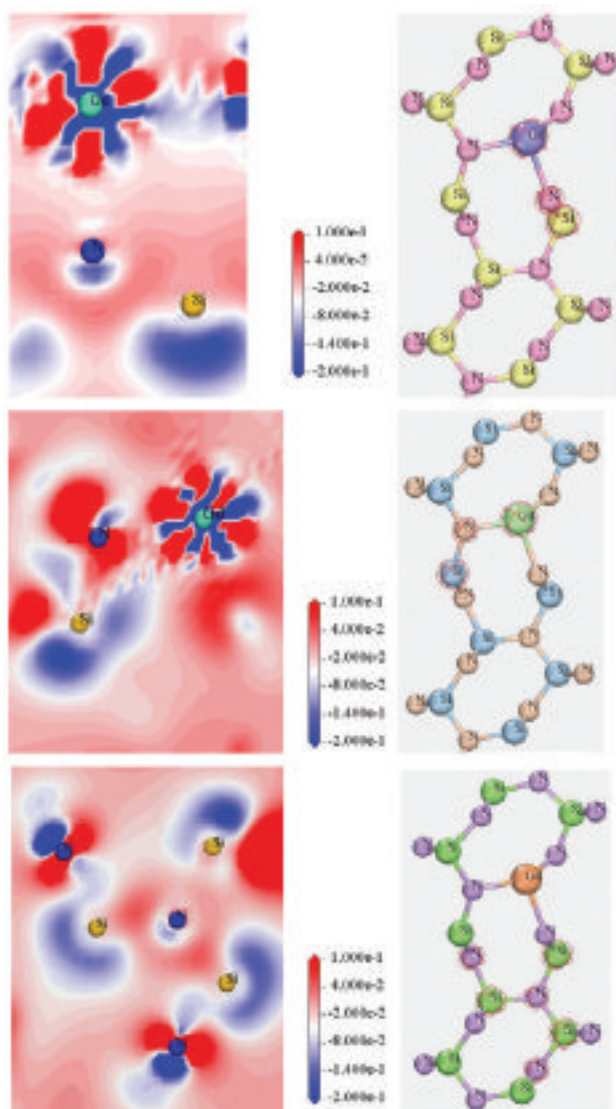


FIGURE 4. Electron density difference maps of Gd-doped system (a) Gd-N-Si; (b) Si-N-Gd; (c) 3N-3Si.

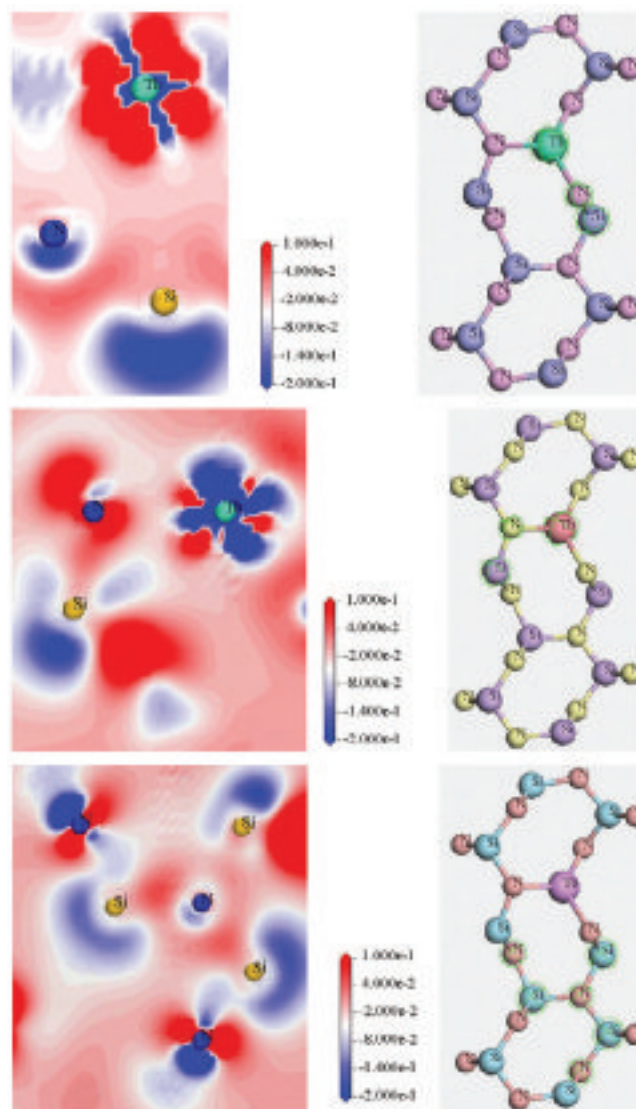


FIGURE 5. Electron density difference maps of Tb-doped system (a) Tb-N-Si; (b) Si-N-Tb; (c) 3N-3Si.

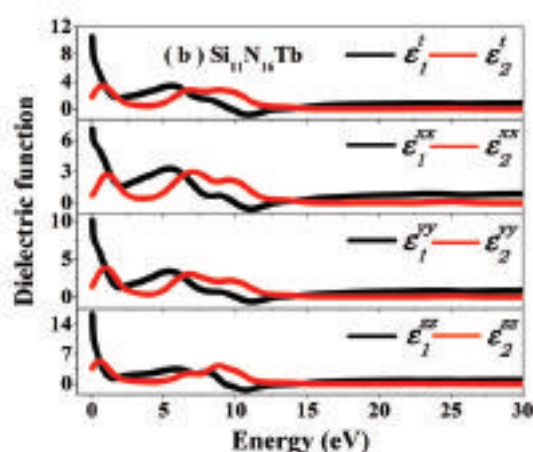
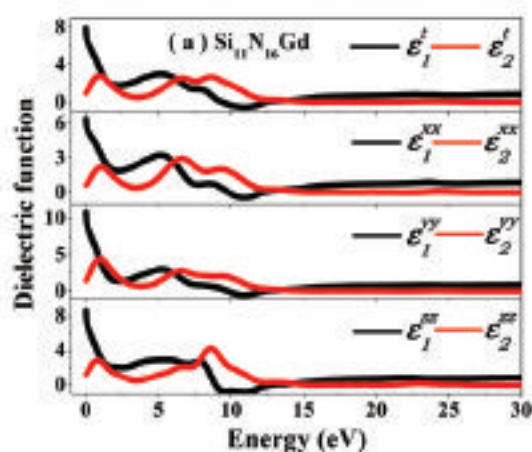


FIGURE 6. The theoretical dielectric function of supercells: (a) Gd-doped system; (b) Tb-doped system.

and the conduction band is about 0.1 eV, which is adequately in reasonable accordance with the results of energy band structures as discussed above. For Tb-doped system, also three valence band parts can be observed: the bottom band ranging from -43.03 to -41.73 eV originates mostly from Tb s orbital electrons; the next one in the middle of -21.71 and -12.31 eV is briefly due to Tb p and N s states; the top valence band located between -10.07 and 1.38 mainly is owing to Tb f and N p orbital electrons; the conduction band between 2.85 and 6.68 eV is composed of Si p states. Summing up, the above, RE doping contributes to the formation of the lower VB of the doped systems, derived from the s orbital electrons of RE, and the formation of narrow band gap, revealing that potential applications in semiconductor devices.

To explore the insights into the comprehension of the charge transfer of both systems, the electron density difference maps in planes containing different atoms are displayed in **FIGURES 4** and **5**. The emerged blue and red parts revealed in pictures represent the electron loss and gain, respectively. It can be seen that the changes in electron density are apparent when Si atom is substituted by Gd or Tb atoms, especially for Tb doping. In the case of both cases, the electron loss, which occurred near the N atom between Si and N atoms and is close to doped atoms, weakens after doping, while the electron loss turns into electron gain with regard to Tb intervention compared to undoped field, weakening the strength of the covalent bond. As we investigate

more carefully these maps, the charge density distributions of non-spherical in both cases can be observed. Concerning the electron loss, the toothed shapes that the pentagonal starfish and latin cross can be seen for the Gd- and Tb-doped systems, respectively.

Optical properties investigation: The optical properties of doped systems are not perfectly understood at all owing to the two particularly challenging problems. Experimentally obtaining the single-crystal samples and property response is difficult and theoretically the works of optical properties of element doped silicon nitride are lack. Due to optical properties not only contain the occupied and unoccupied parts of the electronic structures but also carry the information about the character of bands, it is of underlying importance. In this work, we carry out a complete analysis of doped systems based on first-principles spectroscopy for different optical functions such as imaginary and real parts of the dielectric function, the reflectivity, the absorption spectra and the loss function. Due to the considered systems crystallize in the hexagonal structure with space group P63/m, the dielectric tensor contains three components corresponding to the electric field along the a, b, and c-crystallographic axes, i.e. ϵ_{xx} , ϵ_{yy} , and ϵ_{zz} . The imaginary part $\epsilon_2(\omega)$ is given in equation (3), and the real part $\epsilon_1(\omega)$ can be derived from the imaginary part employing the Kramer-Kronig transformation as shown in equation (4). The absorption coefficient $\eta(\omega)$ and the electron energy loss function $L(\omega)$ can be gained directly related to

$\epsilon_1(\omega)$ and $\epsilon_2(\omega)$ as described in equation (5) and (6).

$$\epsilon_2(\omega) = \frac{e^2 \hbar}{\pi m^2 \omega^2} \sum \sum \int |e P_y|^2 \delta(E_f^K - E_i^K - \hbar \omega) d^3 k$$

$$\epsilon_1(\omega) = 1 + \frac{2}{\pi} P \int_0^\infty \frac{\omega' \epsilon_2(\omega')}{\omega'^2 - \omega^2} d\omega'$$

$$\eta = \sqrt{2\omega} \left[\sqrt{\epsilon_1^2(\omega) + \epsilon_2^2(\omega)} - \epsilon_1(\omega) \right]^{\frac{1}{2}}$$

$$L(\omega) = \epsilon_2(\omega) / \left\{ \epsilon_1^2(\omega) + \epsilon_2^2(\omega) \right\}$$

FIGURE 6 shows the real $\epsilon_1(\omega)$ and imaginary $\epsilon_2(\omega)$ parts of theoretical dielectric function of supercells doped by Gd- and Tb-doped systems. It is meaningful parameter due to the reason that it embodies the basic feature of linear response to an electromagnetic wave and determines the only propagation behavior of the radiation within. One can see that the static dielectric constant obtained at the zero frequency of the real part decreases to

7.97 after Gd doping, and markedly increases to 10.5 for Tb doping with respect to undoped system (8.2) [16], revealing its potential applications in electronics and optics. Compared to the other two directions, ϵ_{yy} and ϵ_{zz} has larger values of 10.76 and 16.1 for Gd- and Tb-doped systems, respectively. Correspondingly, the change is similar to that of imaging part. This reveals that Gd-doped system can exhibit longer life in application as dielectric materials in the low energy regions because of the low static dielectric constant and loss.

FIGURE 7 illustrates the absorption spectra $\eta(\omega)$ of doped systems. It is found that the strong absorption edges locate between 5 and 16 eV, giving the threshold for direct optical transitions between the top valence band and bottom of conduction band. All the parts A_i ($i=t, xx, yy$ and zz) display main peaks located at 10.52, 10.47, 10.51 and 9.19 eV for Gd-doped system and 10.55, 10.71, 10.71 and

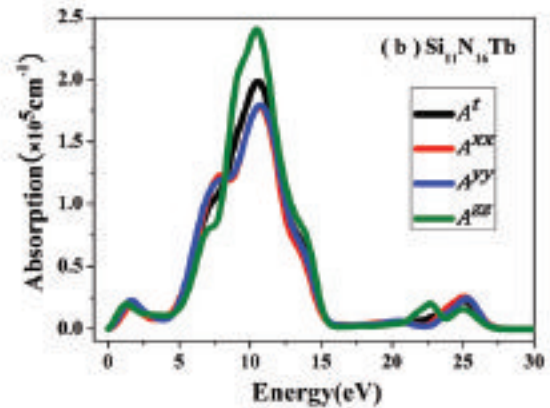
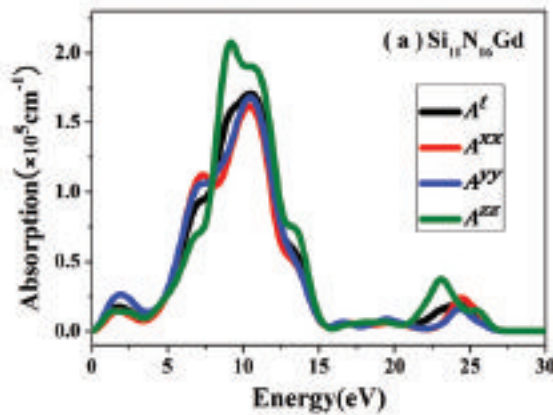


FIGURE 7. The absorption spectra of supercells: (a) Gd-doped system; (b) Tb-doped system.

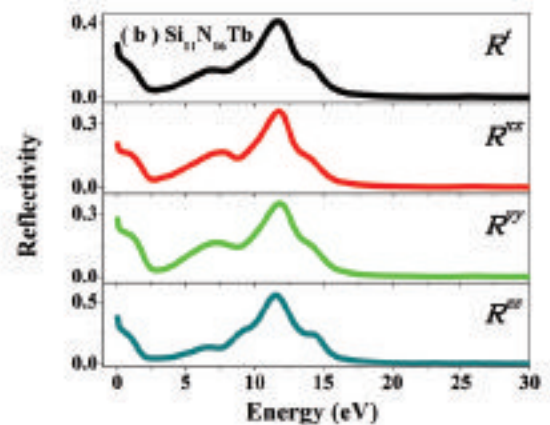
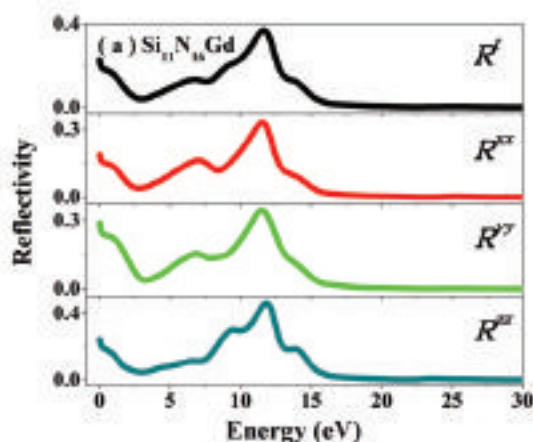


FIGURE 8. The reflectivity spectra of supercells: (a) Gd-doped system; (b) Tb-doped system.

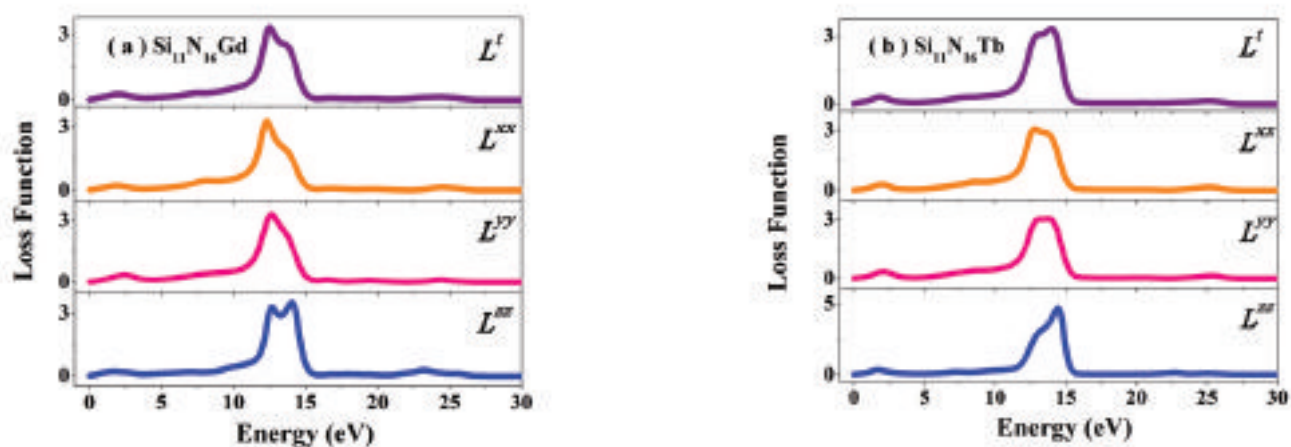


FIGURE 9. The electron energy loss spectra of supercells: (a) Gd-doped system; (b) Tb-doped system.

10.49 eV for Tb-doped system. On the left of the host absorption peaks, the other peaks (about 1.78 and 25 eV) appear, which are attributed to the interband transitions of free electronic carries in the top of VB. The values of the peaks are lower and have a small effect on the host peak, indicating that in the low energy region the doping systems may still exhibit “Transparent Type” compared to undoped system [13], but the range of the edges of the absorption peaks reduced. The obtained reflectivity spectra detailed in **FIGURE 8** is displayed. Spectra profiles are similar for Gd- and Tb-doped of equal peak situations. At the same time, two host peaks all locate at 11.7 eV. It is worth noting that three components R_i ($i=xx, yy$ and zz) display the similar peaks value and positions, which reveals that the optical properties studied here show the characteristics of some isotropy.

FIGURE 9 summarizes the theoretical electron energy loss spectra (EELS) $L(\omega)$ of doped systems, which is in agreement with the imaginary part of the reciprocal of the dielectric function. The peak of EELS is related to the plasma resonance and the frequency interrelated with the peak is the so-called plasma frequency, above which the material exhibits the dielectric behavior, while below which the material behaves like semiconductors and metals. It is found from the results that the host peaks of doped systems are at about 12.5 and 14 eV, respectively, which are lower than that of undoped system (20 eV), indicating that a red-shift phenomenon is present after doping. At the same time, one weak peak appears at 2 eV. As can be seen from the calculation results that the doped systems may display

the semiconductor behavior, which is in agreement with our calculated values of the static dielectric constants. At the same time, it is also concluded that light spreads easily in the lower energy regions for the doping systems.

Conclusions

In summary, using the first-principles calculations, we report on the electronic structures and optical properties that arise on doping-atom-containing silicon nitride systems as a function of dielectric constant, reflectivity, absorption and loss spectra. The results are as follows:

(1) The fully relaxed structural parameters are found to be in good agreement with experimental data. Calculated banding energies of Gd- and Tb-doped systems are -204 and -197 eV, and formation energies are 12 and 15 eV, respectively. It can be readily seen that the structure of the former is more stable than that of the latter.

(2) The electron loss near the N atom between Si and N atoms turns into electron gain with respect to Tb intervention compared to undoped field, weakening the strength of the covalent bond. Concerning the electron loss, the toothed shapes that the pentagonal starfish and latin cross can be observed for the Gd- and Tb-doped systems, respectively.

(3) The absorption band ranges of doped systems become narrower. Both of reflectivity spectra profiles are similar and all locate at 11.7 eV, exhibiting the characteristics of some isotropy. In theoretical electron energy loss spectra, the host peaks of doped

systems locate at about 12.5 and 14 eV, indicating that a red-shift phenomenon occurs after doping.

(4) Gd-doped system can exhibit longer life in application as dielectric materials in the low energy regions because of the low static dielectric constant and loss, as well as transparent type characteristic exhibited in lower energy region.

Acknowledgements

The work was supported by The National Natural Science Foundation of China (51402142, 51164022), The Gansu Provincial Youth Science and Technology Fund Projects (1310RJYA006, 1212RJYA004), Gansu Provincial Science and Technology Support Program (1304GKCA027), Gansu Provincial Department of Construction Project (1201ZTC042).

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TABLE 1. Achieved results in terms of lattice constants (a, b, and c), volume of cell (V), atomic density (ρ), band gap (E_g), total energy (E_t), binding energy (E_b), and formation energy (E_f), as obtained from GGA-PW91 before and after doping. The experimental data come from ref. 14 and 15.

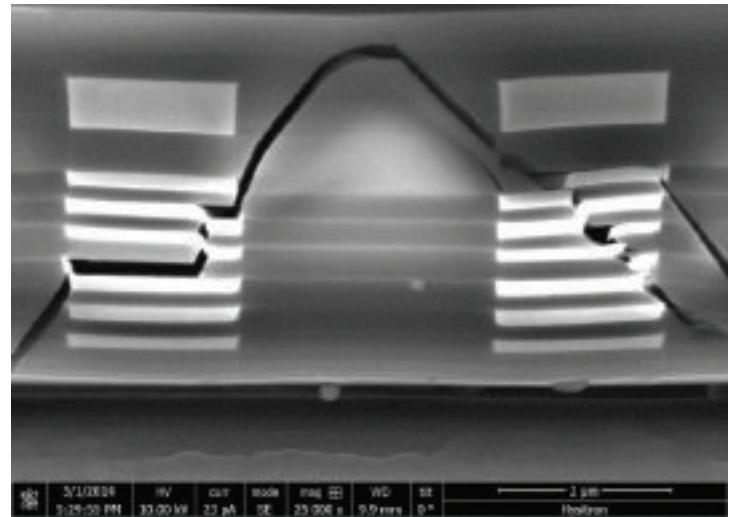
Parameters	Experiment	Experiment	Reference	This work	Parameters	Si ₁₁ N ₁₆ Gd	Si ₁₁ N ₁₆ Tb
a/Å	7.6070	7.6272	7.5572	7.6328	α (degree)	90.8197	91.4855
c/Å	2.9110	2.9182	2.8852	2.9202	β (degree)	90.0093	88.8358
V/ Å ³	145.881	147.016	142.700	147.852	γ (degree)	121.1429	119.9551
xN(2c)	0.3333	0.3333	0.3333	0.3333	a/Å	15.6096	15.5738
yN(2c)	0.6667	0.6667	0.6667	0.6667	b/Å	7.8854	7.7789
zN(2c)	0.2500	0.2500	0.2500	0.2500	c/Å	2.9451	2.9239
xN(6h)	0.3210	0.3399	0.3302	0.3315	V/ Å ³	310.2179	306.7931
yN(6h)	0.0250	0.0357	0.0299	0.0336	ρ (g/cm ³)	3.69	3.74
zN(6h)	0.2500	0.2500	0.2500	0.2500	E _g (eV)	0.095	0.073
xSi(6h)	0.1740	0.1842	0.1742	0.1802	E _t (eV)	-8591	-9068
ySi(6h)	0.7660	0.7704	0.7678	0.7692	E _b (eV)	-204	-197
zSi(6h)	0.2500	0.2500	0.2500	0.2500	E _f (eV)	12	15

Visualizing formation in BEOL

K. VANSTREELS, I. DE WOLF, H. ZAHEDMANESH, H. BENDER, M. GONZALEZ, J. LEFEBVRE, AND S. BHOWMICK, imec, Leuven, Belgium

New tests show in real-time that cracks can run on top of and through metal layers.

Imec, with the help of equipment supplier Hysitron, developed a new test method to study crack formation in Cu/low-k back-end-of-line (BEOL) stacks. By combining a PicoIndenter, a scanning electron microscope (SEM) and unique sample preparation using a focused ion beam (FIB), it becomes possible to visualize in real-time crack initiation and propagation (see video [<https://www.youtube.com/watch?v=HHHCam9rXO0>]). Insight into this reliability issue allows to optimize BEOL design, material choices and process steps to strengthen the BEOL.



SEM picture of crack formation in the back-end-of-line.

Porosity of low-k materials affects the BEOL's mechanical strength

Porous low-k materials are introduced in the BEOL of chips to improve its performance. More specifically, low-k materials prevent leakage between metal interconnections of the circuitry and minimize the time delay. In research, low-k materials with k-values lower than 2.0 are tested. These are very porous and reduce the mechanical strength of the BEOL stack.

Due to the reduced mechanical strength of Cu/low-k BEOL stacks, cracks can be formed when local mechanical stresses become too high. This can occur during chip processing, during packaging, and during use of the end products. The stresses can be caused by temperature fluctuations, due to thermal mismatch of materials; or by shrinkage of materials during curing; by local forces during bonding; or even due to external mechanical impact caused by drop or shock.

Since this crack formation is an important reliability issue for future technology nodes, tests are being developed to gain insight into this problem. For example, there is the four-point bending test and the BABSI test which measure the force at which cracking starts. However, with these tests it is not possible to follow in-situ and in real-time how the crack initiates and propagates through the BEOL stack. With the new test method, this hidden world reveals itself.

The new test

For the new test, a PicoIndenter is integrated into a SEM microscope. The sample has to be prepared in such a way that a beam is formed out of the back-end-of-line stack (see **FIGURE 1**). Imec was able to make such BEOL beams with the Focused Ion Beam (FIB)

This article is based on the paper "In-situ scanning electron microscopy study of fracture events during back-end-of-line microbeam bending tests" which was published in Applied Physics Letters 105, 213102 (2014). **AUTHORS: K. VANSTREELS, I. DE WOLF, H. ZAHEDMANESH, H. BENDER, M. GONZALEZ, J. LEFEBVRE, AND S. BHOWMICK**

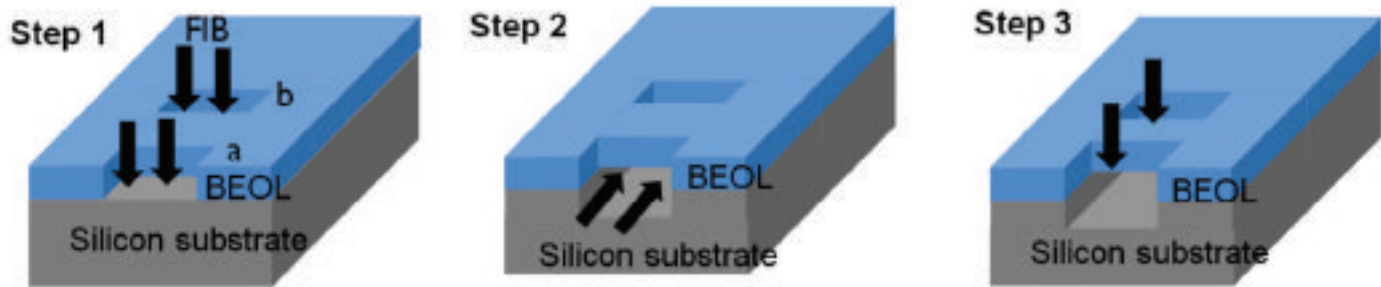


FIGURE 1. Schematic overview of the sample preparation. Using a Focus Ion Beam, a double clamped BEOL beam sample is made.

technique. This involved several steps as depicted in **FIGURE 1**. The sample is then placed in the SEM. With the PicoIndenter, a gradual force is applied on top of the beam while the SEM continuously images the cross-section of the BEOL (side view of the beam). In this way, a movie can be made revealing the crack initiation and propagation, while at the same time measuring the force that is applied (**FIGURE 2**).

Conclusions and future work

This new test has proven to be very relevant for further development of Cu/low-k BEOL stacks. In this phase, only a few BEOL beams – with different dimensions – were tested and measured. From these initial results it can be concluded that cracks run on top of metal layers in this device, and even through metal layers. This can point out that the interface at the top of metal layers should be strengthened for the studied technology, either by BEOL design, material choices or optimization of process steps (such as cleaning).

By setting up more experiments, a model can be made (FEM) to predict crack formation in specific BEOL stacks. The experiments will allow to validate the model. In this way, this new test method is an important tool in the development of reliable chips made in future technology nodes with copper and low-k materials in the back-end-of-line. ◀

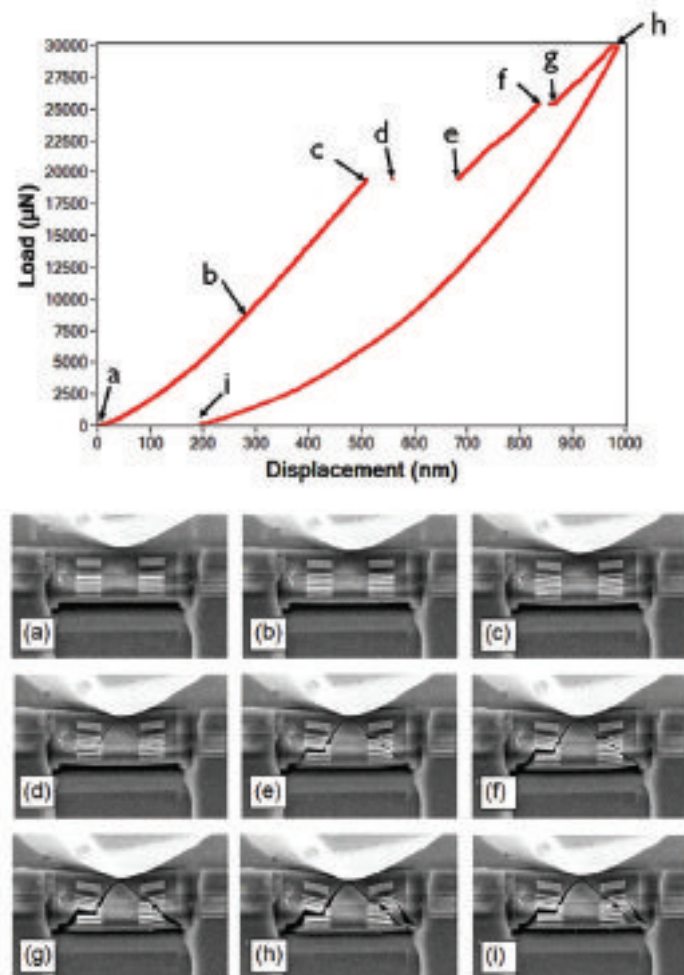


FIGURE 2. Force-displacement curve and corresponding SEM pictures, as measured with the new test method. The pictures reveal beam bending (a to c), crack initiation (d) and crack growth (e to h).

Know Your Enemy

DOUGLAS G. SUTHERLAND and **DAVID W. PRICE**, KLA-Tencor, Milpitas, CA

In a wafer fab there are many different types of variability — all of them are bad.

In the last installment (January 2015, pg. 33) we discussed the idea that uncertainty in measurement is part of the process. Anything that degrades the quality of the measurement also degrades the quality of the process because it introduces more variability into the Statistical Process Control (SPC) charts which are windows into the health of the process. In this paper we will expand upon those ideas.

In the last installment (January 2015, pg. 33) we discussed the idea that uncertainty in measurement is part of the process. Anything that degrades the quality of the measurement also degrades the quality of the process because it introduces more variability into the Statistical Process Control (SPC) charts which are windows into the health of the process. In this paper we will expand upon those ideas.

The fifth fundamental truth of process control for the semiconductor IC industry is:

Variability is the Enemy of a Well Controlled Process.

In a wafer fab there are many different types of variability — all of them are bad.

- Variability in the lot arrival rate, the processing time and the downtime of processing tools, to name just a few sources, all contribute to increased cycle time
- Variability in the physical features (CD, film thickness, side-wall angle, etc.) contribute to increased leakage current, slower part speed, and yield loss
- Variability in the defect rate leads to variability in the final yield, in the infant mortality rate, and in long-term reliability
- Most importantly, variability degrades our ability to monitor small changes in the process – the signal must be greater than the noise in order to be detectable

There is nearly always some way to adjust the average of a given measurement, but the range of values is much harder to control and often much more important. For

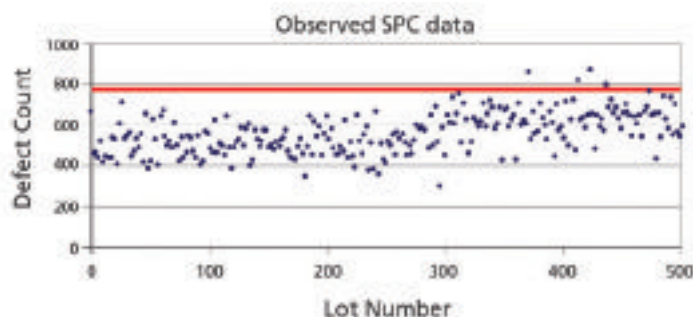
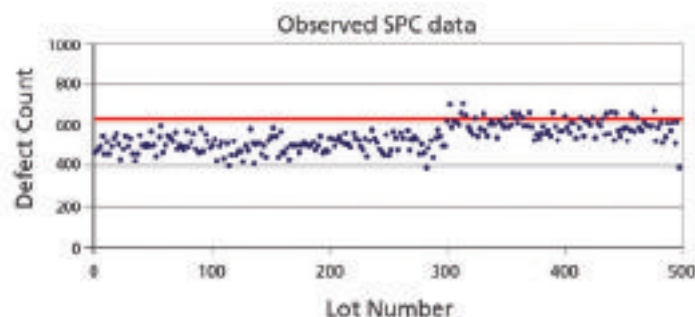


FIGURE 1. Two identical SPC charts showing the defect count at a given step but the chart on the left has half the variability of the chart on the right. The excursion at lot number 300 is detected on the left chart within 8.5 lots (on average) but the same excursion is not detected for 38.6 lots on the chart on the right. Increasing the variability by 2x increases the exposed lots by over 4.5x

DR. DOUGLAS SUTHERLAND and **DR. DAVID W. PRICE** are principal scientist and senior director, respectively, at KLA-Tencor Corp., Milpitas, CA.

example, if a man has his feet in an oven and his head in a freezer, his average body temperature may well be 98° F but that fact won't make him any less dead. Variability kills, and any effort to reduce it is usually time and money well spent.

Variability in defect inspection

FIGURE 1 below shows two simulated SPC charts that monitor the defect count at a given process step. Each chart samples every fifth lot (20 percent lot sampling). Both charts have an excursion at lot number 300 where a defect of interest (DOI) that makes up 10 percent of the total suddenly increases by three-fold. In the left chart the excursion would be caught within 8.5 lots on average, but in the right chart the same excursion would not be caught, on average, until 38.6 lots passed. The only difference is that the chart on the right has twice as much variability.

In general, for an excursion to be caught in a timely fashion it must be large enough to increase the average total defect count by an amount equivalent to three standard deviations of the baseline. If the baseline defect count is very noisy (high variability) then only large excursions will be detectable. Often people think this is the purpose of excursion monitoring: to find the big changes in defectivity. It is not.

In our experience it is nearly always the smaller excursions that cause the most damage simply because they go undetected for prolonged periods of time. The big excursions get a lot of attention and generate a lot of activity but the dollar value of their impact is usually quite small in comparison. It is not uncommon to see low-level excursions cause upwards of \$30,000,000 in yield loss. Large excursions are usually identified very quickly and usually result in a few million dollars of loss.

Other sources of variability in inspection data are low capture rate (CR) and poor CR stability. Defect inspection tools that have low CR will inherently have low CR stability. This means that even if the exact same defects could be moved to a different wafer you would not get the same result because of the different background signal from one wafer to the next. This adds significant variability into the SPC chart and can severely impair the ability to detect changes in the

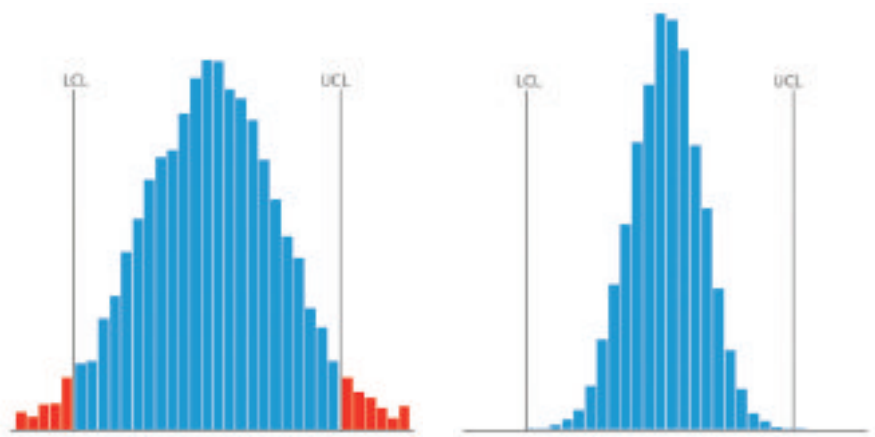


FIGURE 2. The distribution of CD values. The left chart shows a highly variable process and the right chart shows a process that has low variability.

defect level.

It's similar to looking at the stars on two different nights. Sometimes you see them all; sometimes you don't. The stars are still there—it's just that the conditions have changed. Something analogous happens with wafers. The exact same defects may be present but the conditions (film stack, CD, overlay, etc.) have changed. An inspection tool with a tunable wavelength allows you to filter out the background noise in the same way that a radio telescope allows you to see through the clouds. Inspection tools with flexible optical parameter settings (wavelength, aperture, polarization, etc.) produce robust inspections that effectively handle changes in background noise and take the variability out of the defect inspection process.

Variability in metrology

FIGURE 2 shows two different distributions of critical dimension (CD). The chart of the left shows a distribution that spans the full range from the lower control limit (LCL) all the way to the upper control limit (UCL). Any change in the position of the average will result in some part of the tail extending beyond the one of the control limits.

The right hand chart has much less variability. Not only can the average value change a bit in either direction but there is enough room that one may deliberately choose to shift the position of the center point. Depending on the step this may allow one to tune the speed of the part or make trade-offs between part speed and leakage current.

Up to 10 percent of the breadth of these distributions comes from the CD tool used to measure the value in the first place. Contributions to the variability—total measurement uncertainty (TMU)—come from static precision, dynamic precision, long-term stability and matching. Clearly, metrology tools that have better TMU allow more latitude in the fine tuning of process control. This becomes especially important when using feed forward and/or feedback loops that can compound noise in the measurement process.

Obviously the best way to reduce variability is with the process itself. However, process control tools (inspection and metrology) and process control strategies can contribute to that variability in meaningful ways if they are poorly implemented. Metrology and

inspection are the windows into your process: they allow you to see what parts of the process are stable, and more importantly, what parts are changing. The expense of implementing a superior process control strategy is nearly always recouped in terms of reducing variability and making the measurements more sensitive to small changes that can cause the most financial damage.

Author's Note: This is the fifth in a series of 10 installments exploring the fundamental truths about process control—defect inspection and metrology—for the semiconductor industry. Each article in this series introduces one of the 10 fundamental truths and highlights their implications. ◀



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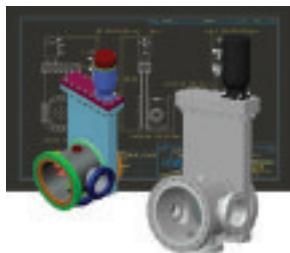
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New approaches to small problems

The market expectations of modern electronics technology are changing the landscape in terms of performance and, in particular, power consumption, and new innovations are putting unprecedented demands on semiconductor devices. Internet of Things devices, for example, largely depend on a range of different sensors, and will require new architectures to handle the unprecedented levels of data and operations running through their slight form factors.

The continued shrinkage of semiconductor dimensions and the matching decreases in microchip size have corresponded to the principles of Moore's Law with an uncanny reliability since the idea's coining in 1965. However, the curtain is now closing on the era of predictable / conventional size reduction due to physical and material limitations.

Thus, in order to continue to deliver increased performance at lower costs and with a smaller footprint, different approaches are being explored. Companies can already combine multiple functions on a single chip—memory and logic devices, for example—or an Internet of Things device running multiple types of sensor through a single chip.

We have always known that we'd reach a point where conventional shrinking of semiconductor dimensions would begin to lose its effect, but now we are starting to tackle it head on. A leading U.S.

semiconductor manufacturer got the ball rolling with their FinFET (or tri-gate) design in 2012 with its 3D transistors allowing designs that minimize current leakage; other companies look set to bring their own 3D chips to market.

At the same time, there's a great deal of experimentation with a range of other approaches to semiconductor redesign. Memory device manufacturers, for instance, are looking to stack memory cells vertically on top of each other in order to make the most of a microchip's limited space. Others, meanwhile, are examining the materials in the hope of using new, more efficient silicon-like materials in their chips.

Regardless of the approach taken, however, this step change in microchip creation means new material demands from chip makers and new manufacturing techniques to go with them.

The semiconductor industry has traditionally had to add new materials and process techniques to enhance the performance of the basic silicon building blocks with tungsten plugs, copper wiring / CMP, high-k metal gates, for example. Now, however, it is beginning to become impossible to extend conventional materials to meet the performance requirements. Germanium is already added to Si to introduce strain, but its high electron mobility means Germanium is also likely to become the material of the Fin itself and will be complemented by a corresponding Fin made of III-V material, in effect integrating three semiconductor materials into a single device.

Further innovation is required in the areas of lithography and etch. This is due to the delay in production suitability of the EUV lithography system proposed to print the very fine structures required for future technology nodes. Complex multi-patterning schemes using conventional lithography are already underway to compensate for this technology delay, requiring the use of carbon hard masks and the introduction of gases such as acetylene, propylene and carbonyl sulphide to the semiconductor fab. Printing the features is only half of the challenge; the structures also need to be etched. The introduction of new materials always presents some etch challenges as all materials etch at slightly different rates and the move to 3D structures, where very deep and narrow features need to be defined through a stack of different materials, will be a particularly difficult challenge to meet.

The microchip industry has continuously evolved to deliver amazing technological advances, but we are now seeing the start of a revolution in microchip design and manufacturing. The revolution will be slow but steady. Such is the pattern of the microchip industry, but it will need a succession of new materials at the ready, and, at Linde, we're prepared to make sure the innovators have everything they need. ◀



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