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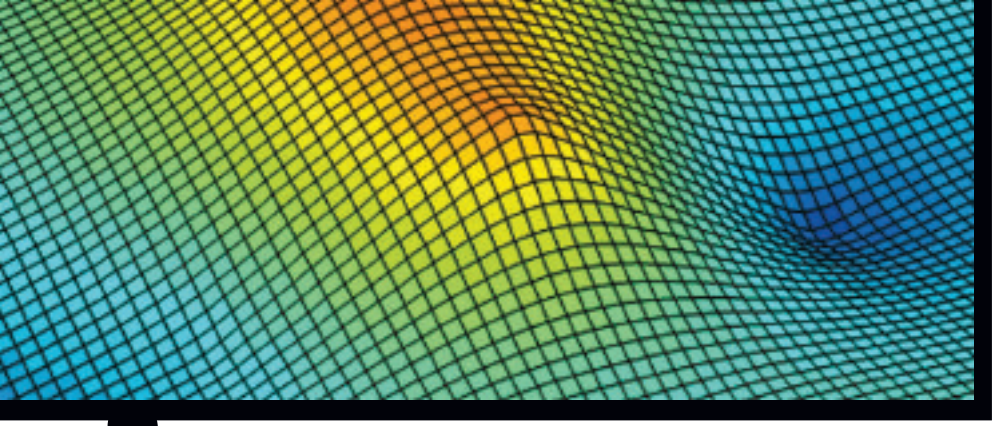


# Solid State TECHNOLOGY®

DECEMBER 2016 VOL. 59 NO. 8


A new approach to bump height measurements uses an interferometric technique to accurately measure bump height and PL thickness.
Source: Rudolph Technologies, Inc.

COVER

## FEATURES



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editorial

# The new driver for semiconductor tech

Over the past 40 years, the electronics industry has gone through three distinct stage or "waves" of evolution. Earlier this year, in a Solid State Technology webcast presentation, Intel's Islam Salama described the waves and how the latest wave is driving the semiconductor industry in new and very different ways. Dr. Salama is responsible for packaging substrate pathfinding of high density interconnects across all Intel products. His team focuses on packaging substrate architectures, process and materials technology building blocks, intellectual property management, and manufacturing ecosystem development.

The first wave occurred in the 1990s, driven mainly by personal computers and enterprise servers. The 2000s saw the very wide adoption of smartphones and cellular phones. "This really provided a very solid platform for industry growth, Salama said.

But today, a major shift is under way. "Starting in 2010, we started to see a generational shift in the IT architecture. This shift is really reshaping every aspect of our economy and industry, and defining the opportunities that are available for growing the industry moving forward," he said. This shift – you guessed it – is driven smart devices, cloud computing and the IoT.

"As we experience pervasive computing behavior, we demand consistency and seamless interface among all our devices as we use them throughout the day," Salama said. "It becomes a cycle. The more pervasive computing becomes, the more demand there is on the cloud and the data center. In the process, you create new application and you try to come up with new devices that keep up with the applications, and the cycle feeds on itself."

Big and small data being generated by the IoT and smartphones is seen as the next big disrupter. In Wave 2 (the 2000s), PCs generated 90 MB/day and smartphones 30MB/day. In Wave 3, the numbers jump dramatically. A connected car, for example, will generate 4TB of data/day, a connected plane, 40TB/Day and a connected factory 1 PB/Day (petabyte (PB) is $10^{15}$ bytes of data).

"Such an explosion of data, driven by our behavior as consumers and the emergence of new applications, will really challenge the infrastructure of the entire network as we know it today," Salama said.

For example, all the sophisticated data analytics that are performed today at the data center need to be pushed downstream. This is particularly true for applications that will become very sensitive to data latency, for example, such as autonomous driving or connected hospitals.

"This is really shaping the future to be concentric around big data, and this is the main reason why data is being viewed today in the industry as the next disruptor and the engine for driving the semiconductor and the information and computing technology moving forward," Salama said.

**—Pete Singer,** Editor-in-Chief


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## Web Exclusives

### Total memory market forecast to increase 10% in 2017

In 2017, IC Insights' forecast the total memory IC market will increase 10% to a new record high of $85.3 billion as gains in average selling prices for DRAM and NAND flash help boost total memory sales. Increases in the memory market are forecast to continue each year through the forecast, with sales topping $100.0 billion for the first time in 2020 and then reaching nearly $110.0 billion in 2021.

**http://bit.ly/2hZ0Td4**

### New fab facilities: China dominates, followed by Americas and Taiwan

SEMI updated the World Fab Forecast report revealing that 62 new front end facilities are expected to begin operation between 2017 and 2020. The 62 facilities and lines range from R&D to high-volume fabs. Most of the newly operating facilities will be volume fabs; only seven are R&Ds or pilot facilities.

**http://bit.ly/2gTEJEt**

### Flexible display shipments to increase sharply in 2017

As more smartphone manufacturers build designs using flexible display technology, shipments of flexible displays are expected to reach 139 million units in 2017, an increase of 135 percent compared to 2016. According to IHS Markit flexible displays are expected to comprise 3.8 percent of total display unit shipments in 2017.

**http://bit.ly/2i1ovhK**

### Semiconductor equipment sales forecast: $40 Billion

SEMI reported that worldwide sales of new semiconductor manufacturing equipment are projected to increase 8.7 percent to $39.7 billion in 2016, according to the SEMI year-end forecast. In 2017, another 9.3 percent growth is expected, resulting in a global semiconductor equipment market totaling $43.4 billion.

**http://bit.ly/2hMbWE4**

## n&b news and blogs

### China to be 15% of world fab capacity by 2018

Currently there are eight Chinese 300mm-diameter silicon IC fabs in operation as 2016 comes to a close. Chinese IC fab capacity now accounts for approximately 7% of worldwide 300mm capacity, as reported by VLSI Research in a recent edition of its Critical Subsystems report. This will expand rapidly, as ten are now under construction and two more have been announced.

**http://bit.ly/2hM4Krz**

### JCET & Qualcomm discuss CPI for die in FOWLP

Phil Garrou, Contributing Editor, reports that, at IMAPS 2016, Lin of JCET discussed CPI (chip package interaction) for 28nm die in eWLB fan out packages. JCET proposes FOWLP as the 3rd wave of packaging. Ray of Qualcomm also examined CPI in FOWLP.

**http://bit.ly/2i15FY5**

### Multibeam patents direct deposition and direct etch

Multibeam Corporation of Santa Clara, California recently announced that its e-beam patent portfolio—36 filed and 25 issued—now includes two innovations that leverage the precision placement of electrons on the wafer to activate chemical processes such as deposition and etch. As per the company's name, multi-column parallel processing chambers will be used to target throughputs usable for commercial high-volume manufacturing (HVM) though the company does not yet have a released product.

**http://bit.ly/2h2AQR6**

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# news

## worldnews

***USA*** - **SEMI** announced the hire of David Anderson as president of the SEMI Americas region.

***ASIA*** - **UMC** celebrated the grand opening of **United Semi**, UMC's 12-inch joint venture wafer fab in Xiamen China.

***USA*** - **Amkor Technology** completed product qualification for its new Silicon Wafer Integrated Fan-Out Technology (SWIFT).

***USA*** - **Cree, Inc.** introduced the XLamp XHP50.2 LED, which delivers up to seven percent more lumens and 10 percent higher lumens-per-watt (LPW) than the first generation XHP50 LED.

***USA AND ASIA*** - **Qualcomm** and **Samsung Electronics** extended their decade-long strategic foundry collaboration to manufacture Qualcomm Technologies' latest Snapdragon premium processor, Qualcomm Snapdragon 835, with Samsung's 10nm FinFET process technology.

***EUROPE*** - **Imec** and **Holst Centre** introduce world's first solid-state multi-ion sensor for IoT applications. It can simultaneously determine pH and chloride levels in fluids.

***USA*** - **Silicon Labs** took the top spot among semiconductor companies achieving $500 million to $1 billion in annual sales at the **Global Semiconductor Alliance (GSA)** awards celebration.

***ASIA*** - **Linde Korea**, a member of The Linde Group, completed the takeover of **Air Liquide** Korea's industrial merchant and electronics on-site and liquid bulk air gases business in South Korea.

***ASIA AND USA*** - **GlobalWafers Co., Ltd.** successfully completed the acquisition of **SunEdison Semiconductor Ltd.**

***ASIA*** - **ChipMOS Technologies Inc.** and **Tsinghua Unigroup Ltd.** announced an agreement to form a joint-venture and to mutually terminate Tsinghua Unigroup's earlier private placement plan.

***USA*** - **MACOM Technology Solutions Holdings, Inc.** entered into a definitive agreement to acquire **Applied Micro Circuits Corporation.**

## Five Top-20 semiconductor suppliers to show double-digit gains in 2016

IC Insights released its November Update to the 2016 McClean Report in November and will release its 20th anniversary edition of The McClean Report in January of next year. The November Update includes the latest semiconductor industry capital spending forecast, a detailed forecast of the IC industry by product type through 2020, and a look at the top-25 semiconductor suppliers expected for 2016. The top-20 2016 semiconductor suppliers are also covered.

The forecasted top-20 worldwide semiconductor (IC and O S D—optoelectronic, sensor, and discrete) sales ranking for 2016 is shown in Figure 1. It includes eight suppliers headquartered in the U.S., three in Japan, three in Taiwan, three in Europe, two in South Korea, and one in Singapore, a relatively broad representation of geographic regions.

The top-20 ranking includes three pure-play foundries (TSMC, GlobalFoundries, and UMC) and five fabless companies. If the three pure-play foundries were excluded from the top-20 ranking, U.S.-based fabless supplier AMD ($4,238 million), China-based fabless supplier HiSilicon ($3,762 million), and Japan-based IDM Sharp ($3,706 million), would have been ranked in the 18th, 19th, and 20th positions, respectively. In August 2016, China-based contract assembler Foxconn bought a controlling interest (66%) in Sharp for $3.8 billion.

In total, the 17 non-foundry companies in the forecasted top 20-ranking are expected to represent 68% of the total $357.1 billion worldwide semiconductor market this year, up 10 points from the 58% share the top 17 companies held in 2006.

IC Insights includes foundries in the top-20 semiconductor supplier ranking since it has always viewed the ranking as a top supplier list, not a marketshare ranking, and realizes that in some cases the semiconductor sales are double counted. With many of our clients being vendors to the semiconductor industry (supplying equipment, chemicals, gases, etc.), excluding large IC manufacturers like the foundries would leave significant

Continued on page 7

## Grenoble team demonstrates world's first qubit device fabricated in standard CMOS process

Leti, an institute of CEA Tech, along with Inac, a fundamental research division of CEA, and the University of Grenoble Alpes have achieved the first demonstration of a quantum-dot-based spin qubit using an industry-standard fabrication process.

Published in the November 24 issue of Nature Communications, and the topic of an invited paper at IEDM 2016, this proof-of-concept breakthrough uses a device fabricated on a 300-mm CMOS fab line. The device consists of a two-gate, p-type transistor with an undoped channel. At low temperature, the first gate defines a quantum dot encoding a hole spin qubit, and the second one defines a quantum dot used for the qubit readout. All electrical, two-axis control of the spin qubit is achieved by applying a phase-tunable microwave modulation to the first gate.

Semiconductor spin qubits reported so far were realized in academic research facilities. Unlike those demonstrations, the present research achievement relies on the

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# High-NA EUV lithography investment

*By Ed Korczynski, Sr. Technical Editor*

Lithography OEM ASML invested EUR 1 billion in cash to buy 24.9% of ZEISS subsidiary Carl Zeiss SMT, and committed to spend EUR ~760 million over the next 6 years on capital expenditures and R&D of an entirely new high numerical aperture (NA) extreme ultra-violet (EUV) lithography tool. Targeting NA >0.5 to be able to print 8 nm half-pitch features, the planned tool will use anamorphic mirrors to reduce shadowing effects from nanometer-scale mask patterns. Clever design and engineering of the mirrors could allow this new NA >0.5 tool to be able to achieve wafer throughputs similar to ASML's current generation of 0.33 NA tools for the same source power and resist speed.

The Numerical Aperture (NA) of an optical system is a dimensionless number that characterizes the range of angles over which the system can accept or emit light. Higher NA systems can resolve finer features by condensing light from a wider range of angles (https://en.wikipedia.org/wiki/Numerical_aperture). Mirror surfaces to reflect EUV "light" are made from over 50 atomic-scale bi-layers of molybdenum (Mo) and silicon (Si), and increasing the width of mirrors to reach higher NA increases the angular spread of the light which results in shadows within patterns.

In the proceedings of last year's European Mask and Lithography Conference, Zeiss researchers reported on "Anamorphic high NA optics enabling EUV lithography with sub 8 nm resolution" (doi:10.1117/12.2196393). The abstract summarizes the inherent challenges of establishing high NA EUVL technology:

For such a high-NA optics a configuration of 4x magnification, full field size of 26 x 33 $mm^2$ and 6'' mask is not

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# Air-Gaps for FinFETs shown at IEDM

Researchers from IBM and Globalfoundries reported on the first use of "air-gaps" as part of the dielectric insulation around active gates of "10nm-node" finFETs at the International Electron Devices Meeting (IEDM). Air-gaps reduce the dielectric capacitance that slows down ICs, so their integration into transistor structures leads to faster logic chips.

## History of Airgaps - ILD and IPD

As this editor recently covered at SemiMD (http://semimd.com/blog/2014/10/31/air-gaps-in-copper-interconnects-for-logic/), in 1998, Ben Shieh—then a researcher at Stanford University and now a foundry interface for Apple Corp.—first published (Shieh, Saraswat & McVittie. IEEE Electron Dev. Lett., January 1998) on the use of controlled pitch design combined with CVD dielectrics to form "pinched-off keyholes" in cross-sections of inter-layer dielectrics (ILD).

In 2007, IBM researchers showed a way to use sacrificial dielectric layers as part of a subtractive process that allows air-gaps to be integrated into any existing dielectric structure. In an interview with this editor at that time, IBM Fellow Dan Edelstein explained, "we use lithography to etch a narrow channel down so it will cap off, then deliberated damage the dielectric and etch so it looks like a balloon. We get a big gap with a drop in capacitance and then a small slot that gets pinched off."

Intel presented on their integration of air-gaps into on-chip interconnects at IITC in 2010 but delayed use until the company's 14nm-node reached production in 2014. 2D-NAND fabs have been using air-gaps as part of the inter-poly dielectric (IPD) for many years, so there is precedent for integration near the gate-stack.

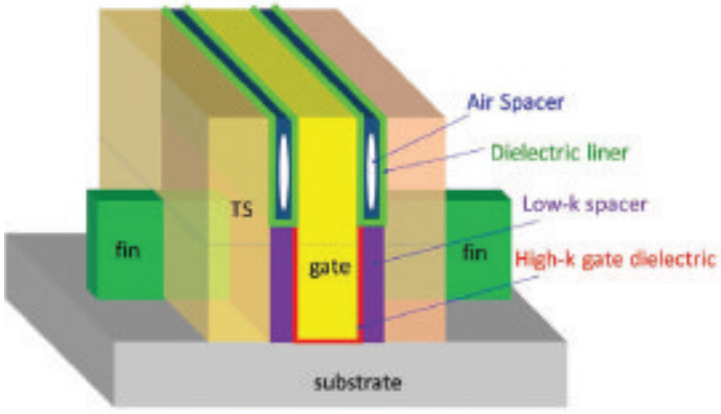



**FIGURE 1.** Schematic of partial air-gaps only above fin tops using dielectric liners to protect gate stacks during air-gap formation for 10nm finFET CMOS and beyond. (source: IEDM 2016, Paper#17.1, Fig.12)

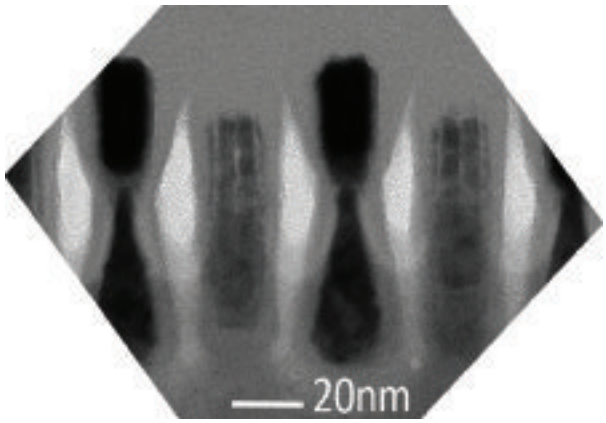



**FIGURE 2.** TEM image of FinFET transistor damage—specifically, erosion of the fin and source-drain epitaxy—by improper etch-back of the air-gaps at 10nm dimensions. (source: IEDM 2016, Paper#17.1, Fig.10)

## Airgaps for finFETs

Now researchers from IBM and Globalfoundries will report in (IEDM Paper #17.1, "Air Spacer for 10nm FinFET CMOS and Beyond," K. Cheng et al) on the first air-gaps used at the transistor level in logic. **Figure 1** shows that for these "10nm-node" finFETs the dielectric spacing—including the air-gap and both sides of the dielectric liner—is about 10 nm. The liner needs to be ~2nm thin so that ~1nm of ultra-low-k sacrificial dielectric remains on either side of the ~5nm air-gap.

These air-gaps reduced capacitance at the transistor level by as much as 25%, and in a ring oscillator test circuit by as much as 15%. The researchers say a partial integration scheme—where the air-gaps are formed only above the tops of fin—minimizes damage to the FinFET, as does the high-selectivity etching process used to fabricate them.

**Figure 2** shows a cross-section transmission electron micrograph (TEM) of what can go wrong with etch-back air-gaps when all of the processes are not properly controlled. Because there are inherent process:design interactions needed to form repeatable air-gaps of desired shapes, this integration scheme should be extendable "beyond" the "10-nm node" to finFETs formed at tighter pitches. However, it seems likely that "5nm-node" logic FETs will use arrays of horizontal silicon nano-wires (NW), for which more complex air-gap integration schemes would seem to be needed. ◆

*Five Top-20 semiconductor suppliers,* Continued from page 4

"holes" in the list of top semiconductor suppliers. As shown in the listing, the foundries and fabless companies are identified. In the April Update to The McClean Report, marketshare rankings of IC suppliers by product type were presented and foundries were excluded from these listings.

Overall, the top-20 list shown in Figure 1 is provided as a guideline to identify which companies are the leading semiconductor suppliers, whether they are IDMs, fabless companies, or foundries.

Nine of the top-20 companies are forecast to have sales of at least $10.0 billion this year. As shown, it is expected to take about $4.5 billion in sales just to make it into the 2016 top-20 semiconductor supplier list. Moreover, if Qualcomm's purchase of NXP is completed, as is expected in late 2017, the combined annual semiconductor sales of these two companies will likely be over $25 billion going forward. Overall, no new entrants are expected to make it into the top-20 ranking in 2016 as compared to the 2015 ranking.

Intel is forecast to remain firmly in control of the number one spot in the top-20 ranking in 2016. In fact, it is expected to increase its lead over Samsung's semiconductor sales from only 24% in 2015 to 29% in 2016. The biggest upward move in the ranking is forecast to be made by Apple, which is expected to jump up three positions in the 2016 ranking as compared to 2015. Other companies that are forecast to make noticeable moves up the ranking include MediaTek and Nvidia, with each company expected to improve by two positions.

Apple is an anomaly in the top-20 ranking with regards to major semiconductor suppliers. The company designs and uses its processors only in its own products—there are no sales of the company's MPUs to other system makers. IC Insights estimates that Apple's custom ARM-based SoC processors will have a "sales value" of $6.5 billion in 2016, which will place them in the 14th position in the forecasted top-20 ranking.

In total, the top-20 semiconductor companies' sales are forecast to increase by 3% this year, which would be two points higher than IC Insights' current worldwide semiconductor market forecast for 2016. Although, in total, the top-20 2016 semiconductor companies are expected to register a 3% increase, there are five companies that are forecast to display a double-digit 2016 jump in sales (Nvidia, MediaTek, Apple, Toshiba, and TSMC) and four that are expected to register a double-digit decline (SK Hynix, Micron, GlobalFoundries, and NXP).

**2016F Top 20 Semiconductor Sales Leaders ($M, Including Foundries)**

| 2016F Rank | 2015 Rank | Company | Headquarters | 2015 Sales* | 2016F Sales* | 2016/2015 Forecast |
|---|---|---|---|---|---|---|
| 1 | 1 | Intel* | U.S. | 52,144 | 56,313 | 8% |
| 2 | 2 | Samsung | South Korea | 42,043 | 43,535 | 4% |
| 3 | 3 | TSMC (1) | Taiwan | 26,439 | 29,324 | 11% |
| 4 | 5 | Qualcomm (2) | U.S. | 16,008 | 15,436 | -4% |
| 5 | 6 | Broadcom Ltd.* (2) | Singapore | 15,183 | 15,332 | 1% |
| 6 | 4 | SK Hynix | South Korea | 16,649 | 14,234 | -15% |
| 7 | 7 | Micron | U.S. | 14,483 | 12,842 | -11% |
| 8 | 8 | TI | U.S. | 12,112 | 12,349 | 2% |
| 9 | 10 | Toshiba | Japan | 9,429 | 10,922 | 16% |
| 10 | 9 | NXP* | Europe | 10,563 | 9,498 | -10% |
| 11 | 13 | MediaTek (2) | Taiwan | 6,699 | 8,610 | 29% |
| 12 | 11 | Infineon | Europe | 6,916 | 7,343 | 6% |
| 13 | 12 | ST | Europe | 6,873 | 6,944 | 1% |
| 14 | 17 | Apple (2,3) | U.S. | 5,531 | 6,493 | 17% |
| 15 | 14 | Sony | Japan | 6,263 | 6,466 | 3% |
| 16 | 18 | Nvidia (2) | U.S. | 4,696 | 6,340 | 35% |
| 17 | 16 | Renesas | Japan | 5,682 | 5,751 | 1% |
| 18 | 15 | GlobalFoundries* (1) | U.S. | 5,729 | 5,085 | -11% |
| 19 | 19 | ON Semi* | U.S. | 4,866 | 4,858 | 0% |
| 20 | 20 | UMC (1) | Taiwan | 4,464 | 4,455 | 0% |
| Total Including Foundries | | | — | 272,772 | 282,130 | 3% |
| Total Without Foundries | | | — | 236,140 | 243,266 | 3% |

(1) Pure-play foundry (2) Fabless supplier
(3) Custom processors for internal use made by TSMC and Samsung foundry services.
*2016 and 2015 sales include Intel/Altera, Broadcom/Avago, NXP/Freescale, GlobalFoundries/IBM, and ON/Fairchild sales for all of 2015 and 2016.
Source: Companies, IC Insights' Strategic Reviews Database

The fastest growing top-20 company this year is forecast to be U.S.-based Nvidia, which is expected to post a huge 35% year-over-year increase in sales. The company is riding a surge of demand for its graphics processor devices (GPUs) and Tegra processors with its year-over-year sales in its latest quarter (ended October 30, 2016) up 63% for gaming, 193% for data center, and 61% for automotive applications.

The second-fastest growing top-20 company in 2016 is expected to be Taiwan-based MediaTek, which is forecast to post a strong 29% increase in sales this year. Although worldwide smartphone unit volume sales are expected to increase by only 4% this year, MediaTek's application processor shipments to the fast-growing China-based smartphone suppliers (e.g., Oppo and Vivo), are forecast to help drive its stellar 2016 increase.

As expected, given the possible acquisitions and mergers that could/will occur over the next few years (e.g., Qualcomm and NXP), the top-20 ranking is likely to undergo a significant amount of upheaval as the semiconductor industry continues along its path to maturity. ◆

***Grenoble team,*** Continued from page 4

technology of FDSOI field-effect transistors. The standard single-gate transistor layout is modified in order to accommodate a second closely spaced gate, which serves for the qubit readout.

Another key innovation lies in the use of a p-type transistor, meaning that the qubit is encoded by the spin of a hole and not the spin of an electron. This specificity makes the qubit electrically controllable with no additional device components required for qubit manipulation.

"Our one-qubit demonstrator brings CMOS technology closer to the emerging field of quantum spintronics," said Silvano De Franceschi, Inac's senior scientist.

Maud Vinet, Leti's advanced CMOS manager and a co-author of the paper, said, "This proof-of-concept result, obtained using a CMOS fab line, is driving a lot of interest from our semiconductor industrial partners, as it represents an opportunity to extend the impact of Si CMOS technology and infrastructure beyond the end of Moore's Law. The way toward the quantum computer is still long, but CEA is leveraging its background in physics and computing, from technology to system and architecture, to build a roadmap toward the quantum calculator."

While superconducting circuits are already providing basic "quantum processors" with several qubits (up to nine), spin qubits in silicon are at a much earlier stage of development. The immediate next steps will be demonstrating a few (n>2) coupled qubits, and developing a strategy for long-range coupling of qubits.

In the long run, "leveraging the integration capabilities of CMOS technology will be a clear asset for large-scale qubit architectures," said De Franceschi. "Within a European collaborative project (see www.mos-quito.eu), we are also developing cryogenic CMOS electronics for the future co-integration of silicon qubits and classical control hardware."

The specific added value of thin-film FDSOI is having a backgate, which can be used to tune the QD electrical state or the dot-to-dot coupling. That avoids the need for an overlapping top gate and the need to deal with the crosstalk. An additional advantage is that conventional FDSOI comes with undoped channels, which is expected to be an advantage for co-integrated control electronics.

It is anticipated that the built-in parallelism in the treatment of quantum information will open new perspectives for cryptography, database searching and simulation of quantum processes. This opportunity is triggering major research initiatives all around the world and, because of that, significant progress can be expected in the coming years. ◆

***High-NA,*** Continued from page 5

feasible anymore. The increased chief ray angle and higher NA at reticle lead to non-acceptable mask shadowing effects. These shadowing effects can only be controlled by increasing the magnification, hence reducing the system productivity or demanding larger mask sizes. We demonstrate that the best compromise in imaging, productivity and field split is a so-called anamorphic magnification and a half field of 26 x 16.5 $mm^2$ but utilizing existing 6'' mask infrastructure.

**Figure 1** shows that ASML plans to introduce such a system after the year 2020, with a throughput of 185 wafers-per-hour (wph) and with overlay of <2 nm. Hans Meiling, ASML vice president of product management EUV, in an exclusive interview with Solid State Technology explained why >0.5 NA capability will not be upgradable on 0.33 NA tools, "the >0.5NA optical path is larger and will require a new platform. The anamorphic imaging will also require stage architectural changes."

Overlay of <2 nm will be critical when patterning 8nm half-pitch features, particularly when stitching lines together between half-fields patterned by single-exposures of EUV. Minimal overlay is also needed for EUV to be used to cut grid lines that are initially formed by pitch-splitting ArFi. In addition to the high NA set of mirrors, engineers will have to improve many parts of the stepper to be able to improve on the 3 nm overlay capability promised for the NXE:3400B 0.33 NA tool ASML plans to ship next year.

"Achieving better overlay requires improvements in wafer and reticle stages regardless of NA," explained Meiling. "The optics are one of the many components that contribute to overlay. Compare to ArF immersion lithography, where the optics NA has been at 1.35 for several generations but platform improvements have provided significant overlay improvements."

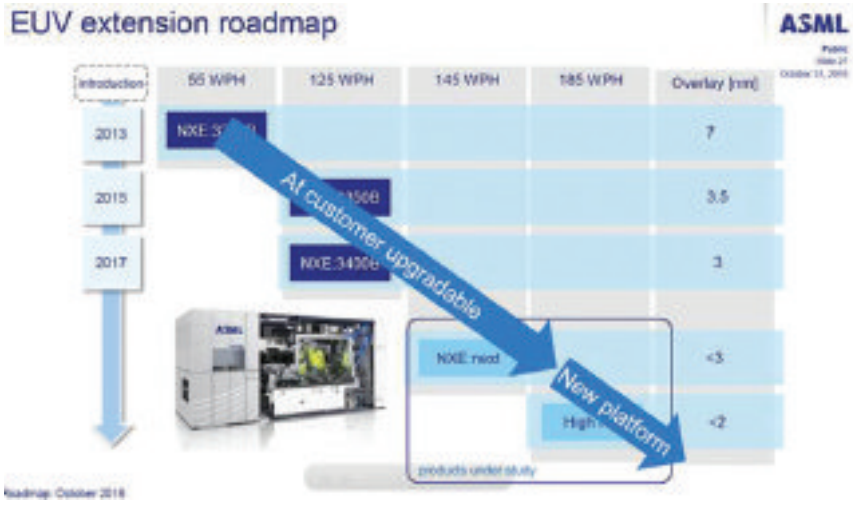



**FIGURE 1.** EUVL stepper product plans for wafers per hour (WPH) and overlay accuracy include change from 0.33 NA to a new >0.5 NA platform. (Source: ASML)

## Manufacturing Capability Plans

**Figure 2** shows that anamorphic systems require anamorphic masks, so moving from 0.33 to >0.5 NA requires re-designed masks. For relatively large chips, two adjacent exposures with two different anamorphic masks will be needed to pattern the same field area which could be imaged with lower resolution by a single 0.33 NA exposure. Obviously, such adjacent exposures of one layer must be properly "stitched" together by design, which is another constraint on electronic design automation (EDA) software.

Though large chips will require twice as many half-field masks, use of anamorphic imaging somewhat reduces the challenges of mask-making. Meiling reminds us that, "With the anamorphic imaging, the 8X direction conditions will actually relax, while the 4X direction will require incremental improvements such as have always been required node-on-node."

ASML and Zeiss report that ideal holes which "obscure" the centers of mirrors can surprisingly allow for increased transmission of EUV by each mirror, up to twice that of the "unobscured" mirrors in the 0.33 NA tool. The holes allow the mirrors to reflect through each-other, so they all line up and reflect better. Theoretically then each >0.5 NA half-field can be exposed twice as fast as a 0.33 NA full-field, though it seems that some system throughput loss will be inevitable. Twice the number of steps across the wafer will have to slow down throughput by some percent.

White two stitched side-by-side >0.5 NA EUVL exposures will be challenging, the generally known alternatives seem likely to provide only lower throughputs and lower yields:

- Double-exposure of full-field using 0.33 NA EUVL,
- Octuple-exposure of full-field using ArFi, or
- Quadruple-exposure of full-field using ArFi complemented by e-beam direct-writing (EbDW) or by directed self-assembly (DSA).

One ASML EUVL system for HVM is expected to cost ~US$100 million. As presented at the company's October 31st Investor Day this year, ASML's modeling indicates that a leading-edge logic fab running ~45k wafer starts per month (WSPM) would need to purchase 7-12 EUV systems to handle an anticipated 6-10 EUV layers within "7nm-node" designs. Assuming that each tool will cost >US$100 million, a leading logic fab would have to invest ~US$1 billion to be able to use EUV for critical lithography layers.

With near US$1 billion in capital investments needed to begin using EUVL, HVM fabs want to be able to get productive value out of the tools over more than a single IC product generation. If a logic fab invests US$1 billion to use 0.33 NA EUVL for the "7nm-node" there is risk that those tools will be unproductive for "5nm-node" designs expected a few years later. Some fabs may choose to push ArFi multi-patterning complemented by another lithography technology for a few years, and delay investment in EUVL until >0.5 NA tools become available. ◁▶

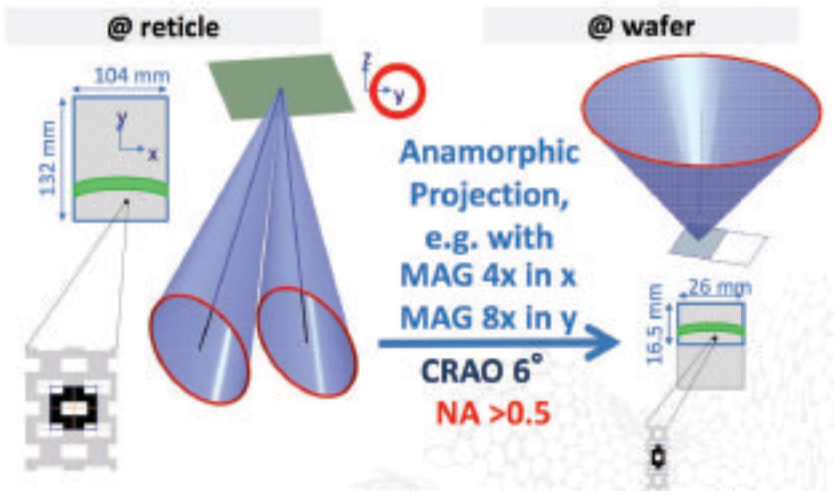



**FIGURE 2.** Anamorphic >0.5 NA EUVL system planned by ASML and Zeiss will magnify mask images by 4x in the x-direction and 8x in the y-direction. (Source: Carl Zeiss SMT)

# Inside Samsung's Galaxy Note 7

DICK JAMES,
Senior Technology Analyst, Chipworks

As usual, within days of the August 19 launch of the Samsung Galaxy Note 7, we had it in pieces and had identified most of the significant components that were inside.

The application processor that drives our phone is the Exynos 8 Octa (Exynos 8890), similar to the Galaxy S7 and S7 edge. It has an eight-core CPU, with four Samsung-designed M1 cores that can run at 2.3 GHz, and four ARM Cortex A53 cores operating at up to 1.6 GHz. The graphics side of the chip uses an ARM Mali-T880 MP12 GPU (with 12 graphics cores). It has a LTE Category12/13 modem and is made with their latest 14LPP finFET process.

Stacked on top of the CPU in the usual package-on-package (PoP) stack, is 4 GB of Samsung LPDDR4 SDRAM. Now that we have 20 nm DRAM processes, the dies are small enough that they are packaged in a 2 x 2 x 2 configuration. The Figure is the plan-view X-ray image showing the wire bonding of the memory chips. The four stacks of two 4-Gb memory dies are mirror-imaged, on both the vertical and horizontal axes.

The dies are just about square (5.4 x 5.1 mm); the use of two-die stacks reduces the package thickness to 0.5 mm. This may be the first time we have seen this particular layout.

The 64 GB of flash memory was supplied by a Toshiba THGBF7G9L4LBATR UFS 2.0 part, fabricated using the latest 15 nm generation process.

### Cameras

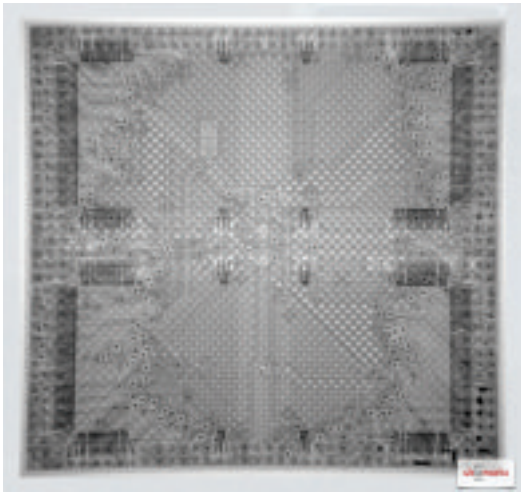
There are three cameras in the Note 7: the usual front- and rear-facing units and an extra one for the iris-scanning security feature of this phone. The main camera is 12 MP with optical image stabilization (OIS) provided by a STMicroelectronics L2GIS 2-axis gyroscope.

The selfie camera is a 5 MP Samsung part and the iris scanner is also Samsung-made, but we have not yet characterized it as to size and technology.

### Sensors

STMicroelectronics supplies all the MEMS motion sensors in the Note 7. In addition to the OIS sensor, there is a LPS25HB pressure sensor and a LSM6DS2 6-axis gyroscope/accelerometer module. All of these have many design wins in phones and wearables.

In addition to the motion sensors, there is an infrared proximity sensor, a heart-rate sensor, and the now ubiquitous fingerprint sensor. The proximity and heart rate sensors appear to be Samsung products, while the fingerprint sensor is reported to be from Synaptics.



### RF front end

The RF front end in a phone these days is a very complex thing. The connectivity specification covers a multitude of bands (2G, 3G, 4G LTE-A), as well as Wi-Fi (802.11 a/b/g/n/ac), Bluetooth v4.2, GPS, A-GPS, GLONASS, BDS, GALILEO, NFC, and wireless charging.

### Touch controllers

The touch control function seems to be distributed in the Note 7, possibly since we also have the S-Pen capability. There is a Cypress CY8CMBR3145 CapSense® Express™ controller, a Samsung S6SY661X, and a Wacom W9018 digitizer, which apparently assesses the different pressure levels applied by the S-Pen to the screen. ◆

## Packaging

# 2D materials may be brittle

ED KORCZYNSKI,
Sr. Technical Editor

International researchers using a novel in situ quantitative tensile testing platform have tested the uniform in-plane loading of freestanding membranes of 2D materials inside a scanning electron microscope (SEM). Led by materials researchers at Rice University, the in situ tensile testing reveals the brittle fracture of large-area molybdenum diselenide (MoSe2) crystals and measures their fracture strength for the first time. Borophene monolayers with a wavy topography are more flexible.

A communication to Advanced Materials online titled "Brittle Fracture of 2D MoSe2" by Yinchao Yang et al. disclosed work by researchers from the USA and China led by Department of Materials Science and NanoEngineering Professor Jun Lou at Rice University, Houston, Texas. His team found that MoSe2 is more brittle than expected, and that flaws as small as one missing atom can initiate catastrophic cracking under strain.

"It turns out not all 2D crystals are equal. Graphene is a lot more robust compared with some of the others we're dealing with right now, like this molybdenum diselenide," says Lou. "We think it has something to do with defects inherent to these materials. It's very hard to detect them. Even if a cluster of vacancies makes a bigger hole, it's difficult to find using any technique."

While all real physical things in our world are inherently built as three-dimensional (3D) structures, a single layer of flat atoms approximates a two-dimensional (2D) structure. Except for special superconducting crystals frozen below the Curie temperature, when electrons flow through 3D materials there are always collisions which increase resistance and heat. However, certain single layers of crystals have atoms aligned such that electron transport is essentially confined within the 2D plane, and those electrons may move "ballistically" without being slowed by collisions.

MoSe2 is a dichalcogenide, a 2D semiconducting material that appears as a graphene-like hexagonal array from above but is actually a sandwich of Mo atoms between two layers of Se chalcogen atoms. MoSe2 is being considered for use as transistors and in next-generation solar cells, photodetectors, and catalysts as well as electronic and optical devices.

The team measured the elastic modulus—the amount of stretching a material can handle and still return to its initial state—of MoSe2 at 177.2 (plus or minus 9.3) gigapascals (GPa). Graphene is more than five times as elastic. The fracture strength—amount of stretching a material can handle before breaking—was measured at 4.8 (plus or minus 2.9) GPa. Graphene is nearly 25 times stronger.

"The important message of this work is the brittle nature of these materials," Lou says. "A lot of people are thinking about using 2D crystals because they're inherently thin. They're thinking about flexible electronics because they are semiconductors and their theoretical elastic strength should be very high. According to our calculations, they can be stretched up to 10 percent. The samples we have tested so far broke at 2 to 3 percent (of the theoretical maximum) at most."

"Wavy" borophene might be better, according to finding of other Rice University scientists. The Rice lab of theoretical physicist Boris Yakobson and experimental collaborators observed examples of naturally undulating metallic borophene—an atom-thick layer of boron—and suggested that transferring it onto an elastic surface would preserve the material's stretchability along with its useful electronic properties.

Highly conductive graphene has promise for flexible electronics, but it is too stiff for devices that must repeatably bend, stretch, compress, or even twist. The Rice researchers found that borophene deposited on a silver substrate develops nanoscale corrugations, and due to weak binding to the silver can be exfoliated for transfer to a flexible surface. The research appeared recently in the American Chemical Society journal Nano Letters. ◆

## Semiconductors

# Improving the accuracy of bump height and coplanarity measurement

**SCOTT BALAK**, *Rudolph Technologies, Inc., Bloomington, MN*

*A new approach to bump height measurements uses an interferometric technique to accurately measure bump height and PL thickness*

Solder bumps are used to connect die to various package components in advanced packaging processes. Bump height and coplanarity are critical to ensuring reliable connections. A bump that is not high enough will not connect, while one that is too tall may prevent connection by neighboring bumps or even damage an electrical tester's probing card. Measuring true bump height quickly and accurately has proven to be a challenge.

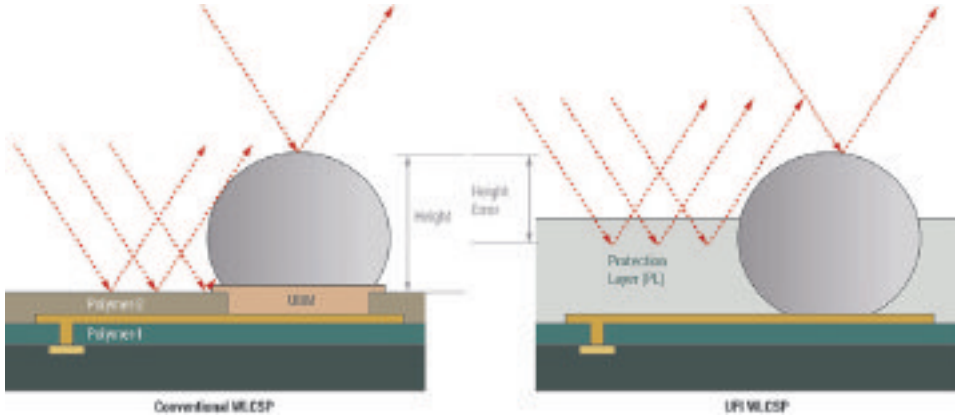



**FIGURE 1.** UFI processes use a protective layer that is semitransparent and varies in thickness. It introduces significant error in bump height/coplanarity measurements.

The measurement has become more challenging with the introduction of processes that eliminate the under bump metal (UBM) layer, used in conventional wafer-level chip scale packages (WLCSP) to improve the bond between the solder ball and the copper redirect pad. Wafer-level chip scale packages have been limited in chip size and ball pitch by the fragility of the solder ball-redirect connection. The intermetallic compounds (IMC) formed there are mechanically weak and subject to fracture under the thermally induced mechanical stress generated by the different expansion coefficients of the silicon die and the package substrate. In UBM-free integration (UFI), the UBM is eliminated and the solder connects directly to the redirect pad. A thick polymer protection layer (PL), usually polyimide (PI) or polybenzoxazole (PBO), helps secure the solder in place and provides stress relief

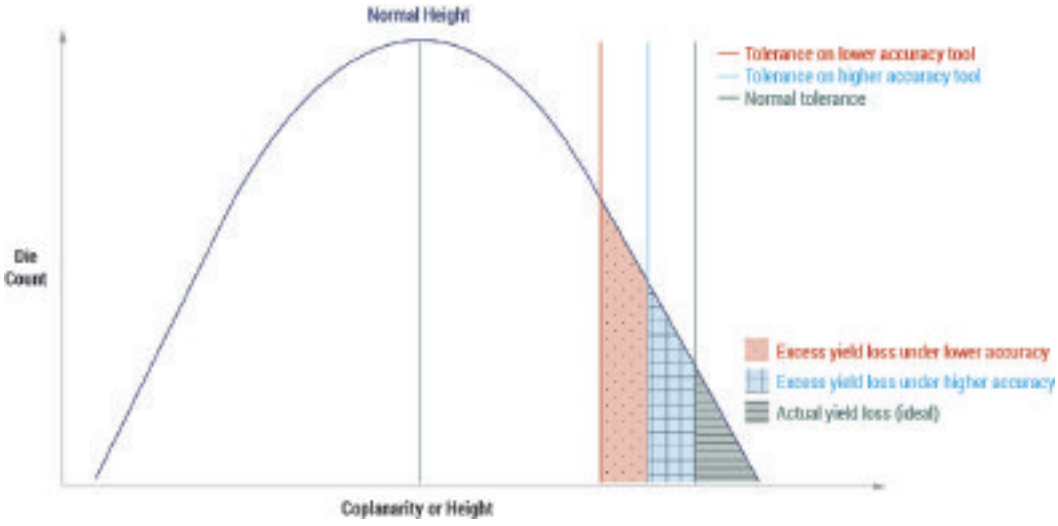



**FIGURE 2.** Inaccurate measurements force process engineers to set a needlessly low tolerance to ensure that true bump height does not fall outside the process window.

**SCOTT BALAK** *is director, Inspection Product Management, Rudolph Technologies, Inc., Bloomington, MN*

between the chip and the substrate. In addition to eliminating the IMC as a source of failure, UFI reduces package cost and cycle time by eliminating layers, and allows a significant reduction in final package thickness. Unfortunately, the PL layer, which is semitransparent and varies in thickness, introduces errors in bump height measurements (**FIGURE 1**).

Many technologies are available that can accurately measure bump height but are too slow to inspect the millions of bumps on a full wafer. Laser triangulation (LT) is fast enough but has difficulty accurately measuring the top surface of the protection layer (PL), which defines the bottom of the bump height measurement. LT measurements consistently locate that surface somewhere within the PL thickness, returning a bump height measurement that is too high. Manufacturers have worked around this problem by subtracting an offset value from the LT measurement. But the correct offset is a function of PL thickness, which can vary across the wafer and from wafer to wafer, thus limiting the accuracy and repeatability of the bump height measurement. To accommodate the deficiencies of the measurement, process engineers must lower the tolerance limit on the process, with the net result being an unnecessary yield loss as bad measurements reject good wafers (**FIGURE 2**). In addition, inaccurate measurements create unnecessary review work as operators revisit inaccurately measured bumps.

## Calibrated measurements

A new approach to bump height measurements uses an interferometric technique to accurately measure bump height and PL thickness at representative locations across the wafer, then calculates offsets to apply to LT measurements in a subsequent, high speed, 100% inspection (**FIGURE 3**).

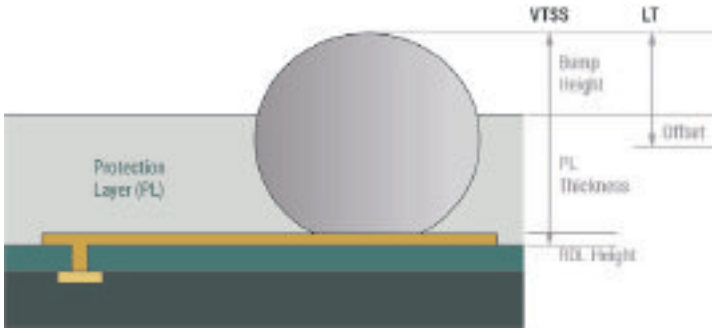



**FIGURE 3.** The VTSS sensor has the required accuracy but is not fast enough for 100% inspection. However, it can be used to calibrate faster LT measurements.

A visible thickness and shape sensor (VTSS) combines the principles of interferometry and reflectometry to accurately detect the top of the bump, the top of the PL and the bottom of the PL. It can also measure step heights at the edges of opaque materials underlying a transparent layer. The VTSS is capable of nanometer scale accuracy and repeatability. It is particularly strong, relative to other measurement technologies, such as chromatic confocal (CC), in its ability to measure thin films. As films become thin, the intensity peaks returned by CC measurements begin to overlap, making it difficult to distinguish top and bottom. PL films are typically in the 3-6µm range, too thin for accurate CC measurements. In contrast, the peaks returned by VTSS are sharp and easily distinguished on films of this thickness (**FIGURE 4**).

## Results

**FIGURE 5** compares VTSS and LT measurements of bump height. The LT measurements report a bump height consistently higher than the VTSS measurements. The data for each representative bump (x-axis) is an average of ten repeat measurements. The difference between the two measurements in this set of data is nearly constant with an average offset of 2.123µm.

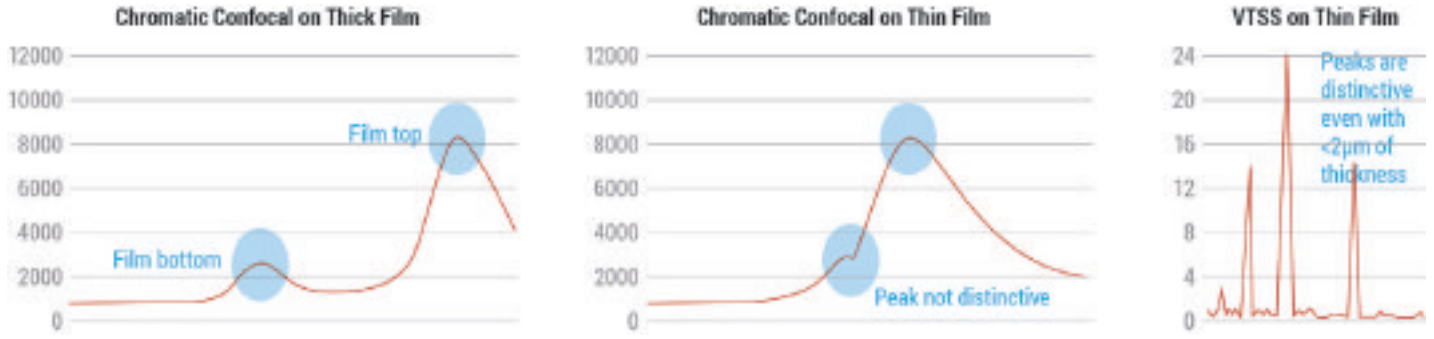



**FIGURE 4.** Other technologies, such as chromatic confocal measurements, provide accurate measurements of thick films (left - 800µm thick film), but have difficulty as the film becomes thin and the signal peaks from the top and bottom surfaces begin to overlap. On the right, VTSS clearly resolves top and bottom surface signals from a 2µm thick film. PL films are typically 3µm – 6µm thick.

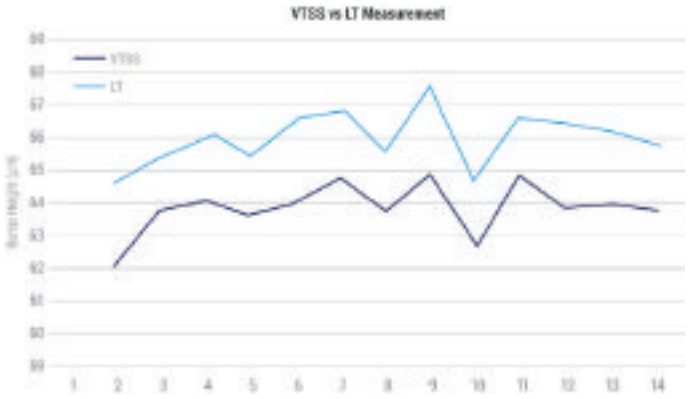



**FIGURE 5.** A comparison of VTSS and LT bump height measurements shows a consistent offset. In this example the LT measurement exceeds the more accurate VTSS measurement by an average of 2.123µm.

**FIGURE 6** shows the results of a repeatability study in which bump heights were measured for ~12,000 bumps from 13 dies across a wafer. The accompanying wafer map shows the locations of the sampled die. 3D height inspection was performed using 5µm spot sensors. The repeatability test was dynamic, meaning the wafer was unloaded and reloaded after each run.

**FIGURES 7** and **8** show the results of whole wafer scans reporting the corrected LT measurements of bump height and coplanarity for all bumps on the wafer. As shown in **FIGURE 9**, the operator can drill down to find results for individual bumps. The pass/fail criteria limit is smaller than the offset provided by the VTSS, meaning that without the pre-measurement the majority of the bumps would be incorrectly reported as failed.

## Conclusions

Accurate bump height and coplanarity measurements are essential to minimize unnecessary yield losses of good but incorrectly measured die and to reduce time spent reviewing incorrectly flagged good die. Laser triangulation is fast enough for 100% inspection but shows consistent measurement errors. This problem is further exacerbated as bump heights shrink and the relative height ratio of the the PL film increases. VTSS measurements, though too slow for 100% measurements, can be used to accurately calibrate LT measurements. In the data presented here the VTSS data demonstrated a repeatability of approximately 0.05µm (average 3 sigma), and the LT measurements a repeatability of approximately 0.362µm (average 3 sigma). Combining the two sensor technologies provides fast, accurate measurements, eliminates unnecessary yield loss and reduces the time spent needlessly reviewing good die. ◆

| 5µm Sensor | Height | Std | 3Std |
|---|---|---|---|
| Average | 63.60042 | 0.120691 | 0.362072 |
| Minimum | 59.73904 | 0.031298 | 0.093893 |
| Maximum | 66.28025 | 0.429421 | 1.288262 |

| 5µm Sensor | Coplanarity | Std | 3Std |
|---|---|---|---|
| Average | -1.29E-09 | 0.115457 | 0.346372 |
| Minimum | -1.96661 | 0.02008 | 0.060239 |
| Maximum | 2.095955 | 0.455163 | 1.365488 |

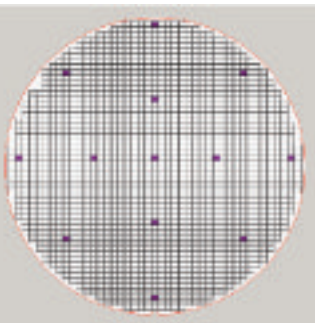


**FIGURE 6.** This repeatability study measured ~12,000 bumps on 13 die distributed at representative locations across the wafer.

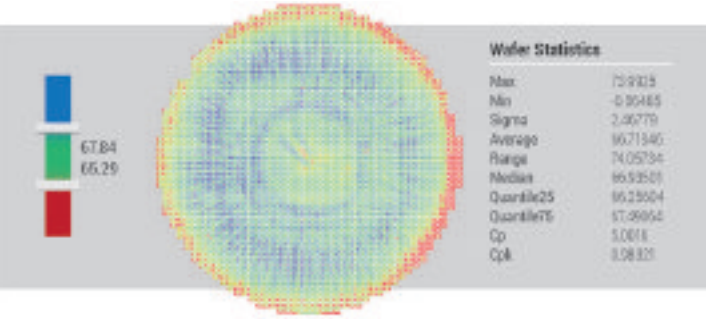



**FIGURE 7.** Corrected LT bump height measurements from a full wafer 100% inspection.

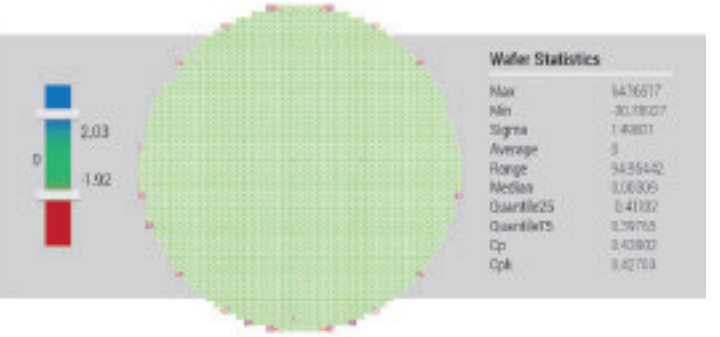



**FIGURE 8.** Corrected LT coplanarity measurements from a full wafer 100% inspection.

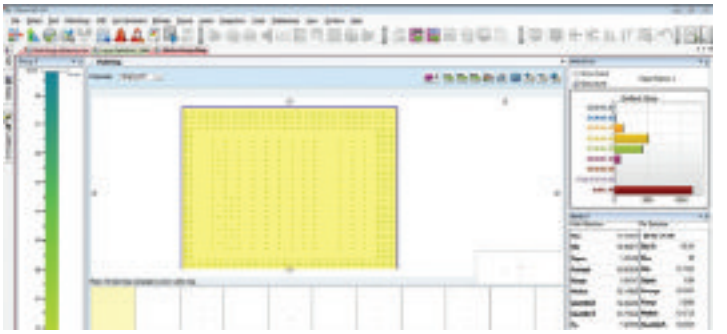


**FIGURE 9.** The operator can recall results for individual bump measurements.

# MRAM takes center stage at IEDM 2016

**DAVID LAMMERS**, *Contributing Editor*

*With good data retention and speed, and medium density, MRAM may have advantages for systems which have large amounts of on-chip SRAM.*

The IEDM 2016 conference, held in early December in San Francisco, was somewhat of a coming-out party for magneto-resistive memory (MRAM). The MRAM presentations at IEDM were complemented by a special MRAM-focused poster session – organized by the IEEE Magnetics Society in cooperation with the IEEE Electron Devices Society (EDS) – with 33 posters and a lively crowd.

And in the opening keynote speech of the 62nd International Electron Devices Meeting, Seok-hee Lee, executive vice president at SK Hynix (Seoul), set the stage by saying that the race is on between DRAM and emerging memories such as MRAM. "Originally, people thought that DRAM scaling would stop. Then engineers in the DRAM and NAND worlds worked hard and pushed out the end further in the future," he said.

While cautioning that MRAM bit cells are larger than in DRAM and thus more more costly, Lee said MRAM has "very strong potential in embedded memory."

SK Hynix is not the only company with a full-blown MRAM development effort underway. Samsung, which earlier bought MRAM startup Grandis and which has a materials-related research relationship with IBM, attracted a standing-room-only crowd to its MRAM paper at IEDM. TSMC is working with TDK on its program, and Sony is using 300mm wafers to build high-performance MRAMs for startup Avalanche Technology.

And one knowledgeable source said "the biggest processor company also has purchased a lot of equipment" for its MRAM development effort.

Dave Eggleston, vice president of emerging memory at GlobalFoundries, said he believes GlobalFoundries is the furthest along on the MRAM optimization curve, partly due to its technology and manufacturing partnership with Everspin Technologies (Chandler, Ariz.). Everspin has been working on MRAM for more than 20 years, and has shipped nearly 60 million discrete MRAMs, largely to the cache buffering and industrial markets.

GlobalFoundries has announced plans to use embedded STT-MRAM in its 22FDX platform, which uses fully-depleted SOI technology, as early as 2018.

Future versions of MRAM– such as spin orbit torque (SOT) MRAM and Voltage Controlled MRAM -- could compete with SRAM and DRAM. Analysts said today's spin-transfer torque STT-MRAM – referring to the torque that arises from the transfer of electron spins to the free magnetic layer -- is vying for commercial adoption as ever-faster processors need higher performance memory subsystems.

STT-MRAM is fast enough to fit in as a new memory layer below the processor and the SRAM-based L1/L2 cache layers, and above DRAM and storage-level NAND flash layers, said Gary Bronner, vice president of research at Rambus Inc.

With good data retention and speed, and medium density, MRAM "may have advantages in the lower-level caches" of systems which have large amounts of on-chip SRAM, Bronner said, due in part to MRAM's smaller cell size than six-transistor SRAM. While DRAM in the sub-20nm nodes faces cost issues as its moves to more complex capacitor structures, Bronner said that "thus far STT-MRAM) is not cheaper than DRAM."

IBM researchers, which pioneered the spin-transfer torque approach to MRAM, are working on a high-performance MRAM technology which could be used in servers.

As of now, MRAM density is limited largely by the size of the transistors required to drive sufficient current to the magnetic tunnel junction (MTJ) to flip its magnetic orientation. Dan Edelstein, an IBM fellow working on MRAM development at IBM Research, said "it is a tall order for MRAM to replace DRAM. But MRAM could be used in system-level memory architectures and as an embedded memory technology."

## PVD and etch challenges

Edelstein, who was a key figure in developing copper interconnects at IBM some twenty years ago, said MRAM only requires a few extra mask layers to be integrated into the BEOL in logic. But there remain major challenges in improving the throughput of the PVD deposition steps required to deposit the complex material stack and to control the interfacial layers.

The PVD steps must deposit approximately 30 layers and control them to Angstrom-level precision. Deposition must occur under very low base pressure, and in oxygen- and water-vapor free environments. While tool vendors are working on productization of 300mm MRAM deposition tools, Edelstein said keeping particles under control and minimizing the maintenance and chamber cleaning are all challenging.

Etching the complex materials stack is even harder. Chemical RIE is not practical for MRAMs at this point, and using ion beam etching (IBE) presents challenges in terms of avoiding re-deposition of material sputtered off during the IBE etch steps for the high-aspect-ratio MTJs.

For the tool vendors, MRAMs present challenges as companies go from R&D to high-volume manufacturing, Edelstein said.

A Samsung MRAM researcher, Y.J. Song, briefly described IBE challenges during an IEDM presentation describing an embedded STT-MRAM with a respectable 8-Mbit density and a cell size of .0364 sq. micron. "We worked to optimize the contact etching," using IBE etch during the patterning steps, he said. The short fail rate was reduced, while keeping the processing temperature at less than 350°C, Song said.

Many of the presentations at IEDM described improvements in key parameters, such as the tunnel magnetic resistance (TMR), cell size, data retention, and read error rates at high temperatures or low operating voltages.

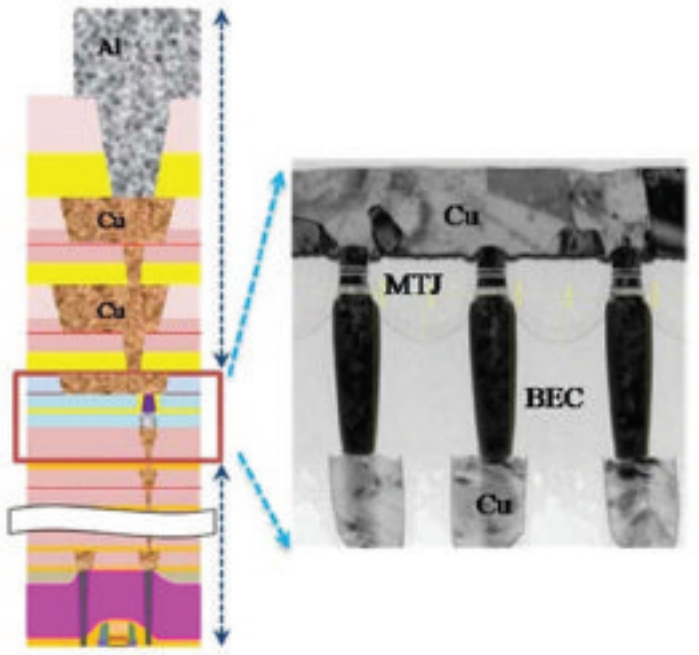



**FIGURE 1.** Samsung embedded an STT-MRAM module in the copper back end of the line (BEOL) of a 28nm logic process. (Source: Samsung presentation at IEDM 2016).

An SK Hynix presentation described a 4-Gbit STT-MRAM optimized as a stand-alone, high-density memory (**FIGURE 1**). "There still are reliability issues for high-density MRAM memory," said SK Hynix's S.-W. Chung. The industry needs to boost the TMR "as high as possible" and work on improving the "not sufficiently long" retention times.

At high temperatures, error rates tend to rise, a concern in certain applications. And since devices are subjected to brief periods of high temperatures during reflow soldering, that issue must be dealt with as well, detailed by a Bosch presentation at IEDM.

## Cleans and encapsulation important

Gouri Sankar Kar, who is coordinating the MRAM research program at the Imec consortium (Leuven, Belgium), said one challenge is to reduce the cell size and pitch without damaging the magnetic properties of the magnetic tunnel junction. For the 28nm logic node, embedded MRAM would be in the range of a 200nm pitch and 45nm critical dimensions (CDs). At the IEDM poster session, Imec presented an 8nm cell size STT-MRAM that could intersect the 10nm logic node, with the MRAM pitch in the 100nm range. GlobalFoundries, Micron, Qualcomm, Sony and TSMC are among the participants in the Imec MRAM effort.

Kar said in addition to the etch challenges, post-patterning treatment and the encapsulation liner can have a major impact on MTJ materials selection. "Some metals can be cleaned immediately, and some not. For the materials stack, patterning (litho and etch) and clean optimization are crucial."

"Chemical etch (RIE) is not really possible at this stage. All the tool vendors are working on physical sputter etch (IBE) where they can limit damage. But I would say all the major tool vendors at this point have good tools," Kar said.

To reach volume manufacturing, tool vendors need to improve the tool up-time and reduce the maintenance cycles. There is a "tail bits" relationship between the rate of bit failures and the health of the chambers that still needs improvement. "The cleanup steps after etching are very, very critical" to the overall effort to improving the cost effectiveness of MRAM, Kar said, adding that he is "very positive" about the future of MRAM technology.

## A complete flow at AMAT

Applied Materials is among the equipment companies participating in the Imec program, with TEL and Canon-Anelva also heavily involved. Beyond that, Applied has developed a complete MRAM manufacturing flow at the company's Dan Maydan Center in Santa Clara, and presented its cooperative work with Qualcomm on MRAM development at IEDM.

In an interview, Er-Xuan Ping, the Applied Materials managing director in charge of memory and materials technologies, said about 20 different layers, including about ten different materials, must be deposited to create the magnetic tunnel junctions. As recently as a few years ago, throughput of this materials stack was "extremely slow," he said. But now Applied's multi-cathode PVD tool, specially developed for MRAM deposition, can deposit 5 Angstrom films in just a few seconds. Throughput is approaching 20 wafers per hour.

Applied Materials "basically created a brand-new PVD chamber" for STT-MRAM, and he said the tool has a new e-chuck, optimized chamber walls and a multi-cathode design.

The MRAM-optimized PVD tool does not have an official name yet, and Ping said he refers to it as multi-cathode PVD. With MRAM requiring deposition of so many different metals and other materials, the Applied tool does not require the wafer to be moved in and out, increasing efficiency. The shape and structure of the chamber wall, Ping said, allow absorption of downstream plasma material so that it doesn't come back as particles.

For etch, Applied has worked to create etching processes that result in very low bit failure rates, but at relatively relaxed pitches in the 130-200nm range. "We have developed new etch technologies so we don't think etch will be a limiting factor. But etch is still challenging, especially for cells with 50nm and smaller cell sizes. We are still in unknown territory there," said Ping.

Jürgen Langer, R&D manager at Singulus Technology (Frankfurt, Germany), said Singulus has developed a production-optimized PVD tool which can deposit "30 material layers in the Angstrom range. We can get 20 wafers per hour throughputs, so I would say this is not a beta tool, it is for production." Langer is shown in **FIGURE 2**.

**FIGURE 2.** Jürgen Langer, R&D manager, presented a poster on MRAM deposition from Singulus Technology (Frankfurt, Germany).

## Where does it fit?

Once the production challenges of making MRAM are ironed out, the question remains: Where will MRAM fit in the systems of tomorrow?

Tom Coughlin, a data storage consultant based in Atascadero, Calif., said embedded MRAM "could have a very important effect for industrial and consumer devices. MRAM could be part of the memory cache layers, providing power advantages over other non-volatile devices." And with its ability to power on and power off without expending energy, MRAM could reduce overall power consumption in smart phones, cutting in to the SRAM and NOR sectors.

"MRAM definitely has a niche, replacing some DRAM and SRAM. It may replace NOR. Flash will continue for mass storage, and then there is the 3D Crosspoint from Intel. I do believe MRAM has a solid basis for being part of that menagerie. We are almost in a Cambrian explosion in memory these days," Coughlin said. ◆

# Industry 4.0: What does it mean to the semiconductor industry?

**FRANCISCO ALMADA LOBO**, *Critical Manufacturing, Moreira da Maia, Portugal*

*Adding intelligence to materials and products facilitates the fully decentralized operations model associated with Industry 4.0.*

Industry 4.0 is coming. It is the next major industrial revolution that will re-define manufacturing as we know it today. But what does Industry 4.0 bring to benefit an industry that already has highly advanced sophisticated manufacturing techniques?

The semiconductor industry is currently not one of those embracing Industry 4.0. Some of the reasons for this are based around the far reaching supply chain the industry uses, some because of the size of batches is still large in some businesses, and some because the idea of gathering greater quantities of information from machines is really not a new concept for the industry. To understand the benefits of Industry 4.0 to semiconductor production, let's first look at exactly what it is.

## A little about Industry 4.0

Industry 4.0 takes innovative developments that are available today and integrates them to produce a modern, smarter production model. It merges real and virtual worlds and is based on Cyber-physical Systems (CPS) and Cyber-physical Production Systems (CPPS), as show in **FIGURE 1**. The model was created to increase business agility, enable cost-effective production of customized products, lower overall production costs, enhance product quality and increase production efficiency. It brings with it new levels of automation and automated decision making that will mean faster responses to production needs and much greater efficiency.

The Industry 4.0 model is inherently a de-centralized one with masses of data being transferred. The reduced cost of computer technology enables it to be embedded into shop floor materials and products. CPS then integrate computational networks with the surrounding physical world and its processes. Using the Industrial Internet of Things (IIoT), products will have the ability to collect and transmit data; communicate with equipment, and take intelligent routing decisions without the need for operator intervention. Cloud computing technology further gives a ready platform to store this data and make it freely available to systems surrounding it.

As CPPS compete to provide services to CPS devices a smart shop floor is created that acts as a marketplace. Adding communication and integration throughout the wider supply chain also means that different manufacturing facilities and even individual processes within a factory can compete for work; creating a Manufacturing as a Service (MaaS) model.

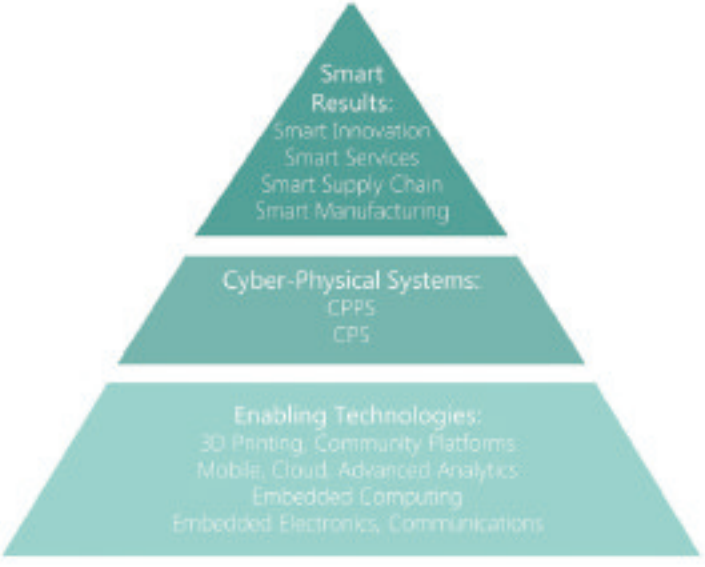



**FIGURE 1.** Industry 4.0 merges real and virtual worlds and is based on Cyber-physical Systems (CPS) and Cyber-physical Production Systems (CPPS)

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With hundreds of devices and shop floor entities producing information, Big Data and advanced analytics are also a major part of Industry 4.0. Simply collecting a lot of data doesn't improve a factory's performance. Advanced analytical software is needed to transform structured and unstructured data into intelligent, usable information. Having huge volumes of data also means this powerful software can be used to help predict production scenarios to further drive efficiencies and improve production strategy.

The intelligent operation and advanced analytics within Industry 4.0 will enable smarter decision making and provide the opportunity to further enhance processes. It will enable new products to be created, tested and introduced at a much faster rate with assured quality, consistency and reliability. The benefits are far reaching and so significant that this revolution will certainly come but the change will be gradual. To be sure not to be left behind, manufacturers will need to plan for the implementation of this predicted industrial revolution.

## What does Industry 4.0 mean for semiconductor manufacturers?

For the semiconductor industry, the high cost of wafers make attaching electronic components to each wafer carrier or FOUP completely viable and presents huge benefits in increased production efficiency. Adding intelligence to materials and products facilitates the fully decentralized operations model associated with Industry 4.0 (**FIGURE 2**). With devices communicating with each other, the increased flexibility and productivity this model produces will make it possible to meet an increasing demand for greater manufacturing mixes and individualized products at much lower costs. For the production of semiconductors in particular, the very nature of the product being manufactured means there may also be opportunity and added benefit for some devices to hold their own information without the need for additional electronics. The information gathered from the decentralized model and analytical software used in Industry 4.0 also makes it easier to account for the cost of each item, resulting in better intelligence for business strategy and product pricing.

Although equipment used in the production of semiconductors already have sensors and transmit intelligent information into wider systems, the concept of the CPPS using the IoT adds a new level of simplicity to this idea. The cost of production within the semiconductor industry also means that even marginal variable improvements through the increased use of big data analytics will have huge financial benefits. The Internet of Things (IoT) will further enhance flexibility in measurement and actuation possibilities and free manufacturers from the time and cost associated with changes to sophisticated interfaces on production equipment.

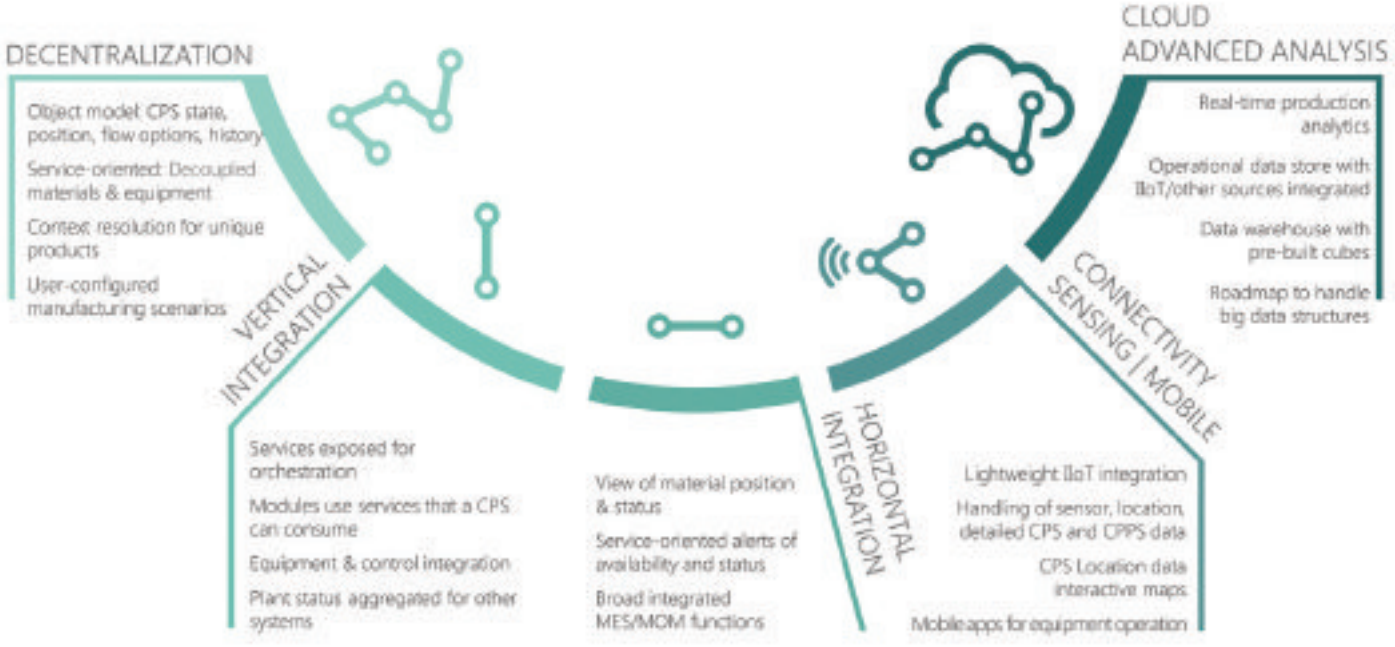


**FIGURE 2.** Adding intelligence to materials and products facilitates the fully decentralized operations model associated with Industry 4.0.

## The smart marketplace

With components interacting with machines and having the information they need within them about the processing steps they require, this creates a smart marketplace where the CPS requests services (demand) and the CPPS provides them (supply). Using mobile communications and cloud computing, this can of course be further expanded into the wider supply chain.

The concept of Manufacturing as a Service (MaaS) is, to some extent, already present in the semiconductor industry. The full supply chain has many different steps and, because of the high value of the product, transportation costs become pretty much irrelevant. This means that processing steps can be geographically distributed and the smart marketplace bidding for the work can extend throughout the world. Different factories may compete with each other for procuring specific processing steps and still be competitive regardless of location. Industry 4.0 gives the industry all the tools it needs for a smart, highly efficient marketplace that can add significant production flexibility while reducing both costs and production times.


**FIGURE 3.** Mobile devices are now more than capable of handling the demanding tasks of an operator workstation and offer the potential to decrease operational costs and increase productivity.

## Benefits of virtual and augmented reality

There are already few manual steps in the semiconductor production process with wafer production in particular using highly automated processes. This means there are few operators to oversee significant amounts of operations and equipment. Industry 4.0 opens up new areas in virtual reality (VR) and augmented reality (AR) that will help keep operations running smoothly.

The visualization and control of the wide spread autonomous elements within the CPS and CPPS in a decentralized production model requires a move away from standard, fixed, desk-top like workstations. Mobile devices are now more than capable of handling the demanding tasks of an operator workstation and offer the potential to decrease operational costs and increase productivity (**FIGURES 3a** and **b**).

Using more comprehensive digital data and mobile computing technology, operators would be able to simply point a tablet at a piece of equipment and get real time information about what is happening. Locations of personnel could also be monitored to make most efficient use of human resources available. For the semiconductor industry; the use of secure, mobile devices further reduces the need to take up space in valuable clean-room environments.

Using mobile interfaces, maintenance technicians will also be able to conveniently move between machines without the need to logon at different workstations.

They can interact with different pieces of equipment and gather information about processes while carrying out tasks such as ordering spare parts all from a single mobile device. For specific operations relating to a piece of equipment, apps that automatically launch onto the technician's tablet depending upon their location may further be used to add important additional information about a piece of equipment. For example, a particular part may be highlighted to be checked or replaced or additional information about specific machine readings highlighted on the display.

With all the amount of data sent by sensors, products and equipment it will also be possible to visualize in real-time the complete status of a production floor using VR 3D maps. Combining information about where personnel are within the factory and which direction they are facing, this further enables the implementation of some compelling AR scenarios. Indeed, the capability of mobile devices and the increase in real-time data available will likely make the wider use of both VR and AR a fundamental part of shop floor operations.

## The Route to Industry 4.0 – the next generation of MES

There are a number of challenges that Industry 4.0 brings with it and its implementation will certainly not happen overnight. The huge benefits the model has to offer, however, can be planned into business strategies and realized over time. One of the first areas to consider is vertical integration of the model. This is important because corporate processes must not be avoided with the autonomy of materials and machines. Business processes for compliance, logistics, engineering, sales or operations all have components inside the plant as well as others that reside beyond the factory that are crucial to a business process being executed effectively. Without these, it's almost impossible to properly manage a production floor of a certain complexity.

Modern Manufacturing Execution Systems (MES) based on decentralized logic offer a platform for the development of the Industry 4.0 model and a natural route to its vertical integration. MES have always been most effective when integrated into Enterprise Resource Planning (ERP) systems 'above' while monitoring and controlling production processes 'below'.

With the CPS and CPPS communicating directly with each other, the MES can trigger business rules or workflows for the complete production process. For example, quality processes may demand that a device may need additional verification steps before processing continues as part of a higher level quality sampling strategy. This requires communication to intersect the business rules so the quality procedures are not bypassed before the device continues through its production processes.

Another area that is reliant on good vertical integration of systems within Industry 4.0 is Statistical Process Control (SPC). SPC requires data to be collected over time from numerous materials passing through the factory. For example, if a device within the CPS knows it needs to collect a measurable variable, this needs to be confirmed against SPC rules that it is within limits. If it is not, corrective action may be required. Flags for such actions need to be triggered in systems above the CPS and, again, the MES is an ideal platform for this.

By its very nature, the concept of a smart shop floor will generate huge volumes of data. An Industry 4.0 MES will need to aggregate this data and put it into a shop floor context. Indeed, to handle the decentralized logic and vertical integration of the autonomous entities on the shop floor, MES manufacturers need to fully expand their systems' capabilities to ensure all plant activities are visible, coordinate, managed and accurately measured.

Future MES can also help to realize the full MaaS. This requires horizontal integration so all functions and services can be consumed by all entities on the shop floor including the CPS smart materials and CPPS smart machines. For individual equipment or processes to be procured in single steps, the MES needs to offer exceptional flexibility to expose all available services, capacity and future production plans. With visibility of the complete supply chain, MES also need to consider security and IP related challenges with multi-dimensional security. This needs to be at a service level but also at individual process, step and equipment levels and at any combination of these.

Ultimately it is envisioned that the Cloud will deliver the storage and the 'anytime, anywhere' ability to handle the volume of data created from sensors, processing and connectivity capability distributed throughout the plant. The manufacturing intelligence needed and provided by MES today therefore also has to expand to better accommodate the diversity and volume of big data. Fast response to any manufacturing issues will come from real-time analysis where advanced techniques such as "in-memory" and complex event processing may be used to drive operational efficiency even further, where the value of the process makes this a viable return on investment.

Support for advanced analytics in MES is needed to analyse historical data fully understand the performance of the manufacturing processes, quality of products and supply chain optimization. Analytics will also help by identifying inefficiencies based on historical data and pointing staff to corrective or preventive actions for those areas.

## Legacy MES

Semiconductor was probably one of the first industries to embrace the idea of MES. First adopters were as early as the 1970s before the term 'MES' was even established. Some of these systems still exist today. The problem is that, as the limits of these early systems were reached; small applications have been added around them to meet modern manufacturing demands. These systems are so embedded into production processes that changing them is like replacing the heart of the factory and is no small consideration. There will, however, be some point where these systems can no longer be patched up to meet needs and factories will need to change to survive. The huge potential benefits Industry 4.0 offers may well be the catalyst to change and the basis of sound strategic planning for the future of a business.

## Summary

One of the main areas of benefit of the Industry 4.0 decentralized model is the ability to individualize products efficiently with high quality results. This benefits all industries as trends show an increased demand for high mix, smaller batches to meet varying consumer demands. More than for many other industries, the high cost of individualized semiconductors makes the value of adding autonomy to customized processes even higher.

MES have been at the heart of the semiconductor industry for many decades but future-ready MES, based on models with de-centralized logic, offer a pathway to realizing the benefits Industry 4.0 has to offer. For semiconductors these benefits centre on reduced production costs, particularly for small production batches; enhanced efficiency of small workforces, and the business and cost reductions to be gained from the MaaS model and smart supply chain.

Although the semiconductor industry has been somewhat protected, competition is still fierce, especially in areas of mass production. In all different manufacturing areas, however, batch sizes will become smaller and the demand for individualized products will increase. Semiconductor manufacturers that can adapt more quickly to this trend will gain competitive edge and ultimately will be the businesses that survive and grow for the future. Without the Industry 4.0 model manufacturers will of course be able to produce in the future context of more customization, but costs will be much higher than for those who embrace this industrial revolution. If the full scope of Industry 4.0 is realized throughout the supply chain with MaaS, it will be even harder for companies that are outside of this model to compete in the smart marketplace.

With the dawn of Industry 4.0, manufacturing is moving into a new era that brings huge benefits and it is unlikely that the semiconductor industry will let itself be left behind! ◆

# Has SOI's turn come around again?

**DAVID LAMMERS**, *Contributing Editor*

*Analysts see another chance for Silicon-on-Insulator technology, as proponents claim technical and cost advantages for fully-depleted SOI.*

When analyst Linley Gwennap is asked about the chances that fully-depleted silicon-on-insulator (FD-SOI) technology will make it in the marketplace, he gives a short history lesson.

First, he makes clear that the discussion is not about "the older SOI," – the partially depleted SOI that required designers to deal with the so-called "kink effect." The FD-SOI being offered by STMicroelectronics and Samsung at 28nm design rules, and by GlobalFoundries at 22nm and 12nm, is a different animal: a fully depleted channel, new IP libraries, and no kink effect.

Bulk planar CMOS transistor scaling came to an end at 28nm, and leading-edge companies such as Intel, TSMC, Samsung, and GlobalFoundries moved into the finFET realm for performance-driven products, said Gwennap, founder of The Linley Group (Mountain View, Calif.) and publisher of The Microprocessor Report, said,

While FD-SOI at the 28nm node was offered by STMicrelectronics, with Samsung coming in as a second source, Gwennap said 28nm FD-SOI was not differentiated enough from 28nm bulk CMOS to justify the extra design and wafer costs. "When STMicro came out with 28 FD, it was more expensive than bulk CMOS, so the value proposition was not that great."

NXP uses 28nm FD-SOI for its iMX 7 and iMX 8 processors, but relatively few other companies did 28nm FD-SOI designs. That may change as 22nm FD-SOI offers a boost in transistor density, and a roadmap to tighter design rules.

"For planar CMOS, Moore's Law came to a dead end at 28nm. Some companies have looked at finFETs and decided that the cost barrier is just too high. They don't have anywhere to go; for a few years now those companies have been at 28nm, they can't justify the move on to finFETs, and they need to figure out how they can offer something new to their customers. For those companies, taking a risk on FD-SOI is starting to look like a good idea," he said.

## A cautious view

Joanne Itow, foundry analyst at Semico Research (Phoenix), also has been observing the ups and downs of SOI technology over the last two decades. The end of the early heyday, marked by PD-SOI-based products from IBM, Advanced Micro Devices, Freescale Semiconductor, and several game system vendors, has led Itow to take a cautious, Show-Me attitude.

"The SOI proponents always said, 'this is the breakout node,' but then it didn't happen. Now, they are saying the Fmax has better results than finFETs, and while we do see some promising results, I'm not sure everybody knows what to do with it. And there may be bottlenecks," such as the design tools and IP cores.

Itow said she has talked to more companies that are looking at FD-SOI, and some of them have teams designing products. "So we are seeing more serious activity than before," Itow said. "I don't see it being the main Qualcomm process for high-volume products like the applications processors in smartphones. But I do see it being looked at for IoT applications that will come on line in a couple of years. And these things always seem to take longer than you think," she said.

Sony Corp. has publicly discussed a GPS IC based on 28nm FD-SOI that is being deployed in a smartwatch sold by Huami, a Chinese brand, which is touting the long battery life of the watch when the GPS function is turned on.

GlobalFoundries claims it has more than 50 companies in various stages of development on its 22FDX process, which enters risk production early next year, and the company plans a 12nm FDX offering in several years.

## IP Libraries put together

The availability of design libraries – both foundation IP and complex cores – is an issue facing FD-SOI. Gwennap said GlobalFoundries has worked with EDA partners, and invested in an IP development company, Invecas, to

develop an IP library for its FDX technology. "Even though GlobalFoundries is basically starting from scratch in terms of putting together an IP library, it doesn't take that long to put together the basic IP, such as the interface cells, that their customers need.

"There is definitely going to be an unusual thing that probably will not be in the existing library, something that either GlobalFoundries or the customers will have to put together. Over time, I believe that the IP portfolio will get built out," Gwennap said.

The salaries paid to design engineers in Asia tend to be less than half of what U.S.-based designers are paid, he noted. That may open up companies "with a lower cost engineering team" in India, China, Taiwan, and elsewhere to "go off in a different direction" and experiment with FD-SOI, Gwennap said.

Philippe Flatresses, a design architect at STMicro, said with the existing FDSOI ecosystem it is possible to design a complete SoC, including processor cores from ARM Ltd., high speed interfaces, USB, MIPI, memory controllers, and other IP from third-party providers including Synopsys and Cadence. Looking at the FD-SOI roadmap, several technology derivatives are under development to address the RF, ultra-low voltage, and other markets. Flatresses said there is a need to extend the IP ecosystem in those areas.

## Wafer costs not A big factor

There was a time when the approximately $500 cost for an SOI wafer from Soitec (Grenoble, France) tipped the scales away from SOI technology for some cost-sensitive applications. Gwennap said when a fully processed 28nm planar CMOS wafer cost about $3,000 from a major foundry, that $500 SOI wafer cost presented a stumbling block to some companies considering FD-SOI.

Now, however, a fully-processed finFET wafer costs $7,000 or more from the major foundries, Gwennap said, and the cost of the SOI wafer is a much smaller fraction of the total cost equation. When companies compare planar FD-SOI to finFETs, that $500 wafer cost, Gwennap said, "just isn't as important as it used to be. And some of the other advantages in terms of cost savings or power savings are pretty attractive in markets where cost is important, such as consumer and IoT products. They present a good chance to get some key design wins."

Soitec claims it can ramp up to 1.5 million FD-SOI wafers a year with its existing facility in 18 months, and has the ability to expand to 3 million wafers if market demand expands.

Jamie Schaeffer, the FDX program manager at GlobalFoundries, acknowledges that the SOI wafers are three to four times more expensive than bulk silicon wafers. Schaeffer said a more important cost factor is in the mask set. A 22FDX chip with eight metal layers can be constructed with "just 39 mask layers, compared with 60 for a finFET design at comparable performance levels." And no double patterning is required for the 22FDX transistors.

## Technology advantages claimed

Soitec senior fellow Bich-Yen Nguyen, who spent much of her career at Freescale Semiconductor in technology development, claims several technical advantages for FD-SOI.

FD-SOI has a high transconductance-to-drain current ratio, is superior in terms of the short channel effect, and has a lower fringing and effective capacitance and lower gate resistance, due partly to a gate-first process approach to the high-k/metal gate steps, Nguyen said.

Back and forward biasing is another unique feature of FD-SOI. "When you apply body-bias, the fT and fmax curves shift to a lower Vt. This is an additional benefit allowing the RF designer to achieve higher fT and fmax at much lower gate voltage (Vg) over a wider Vg range. That is a huge benefit for the RF designer," she said. **FIGURE 1** illustrates the unique benefit of back-bias.

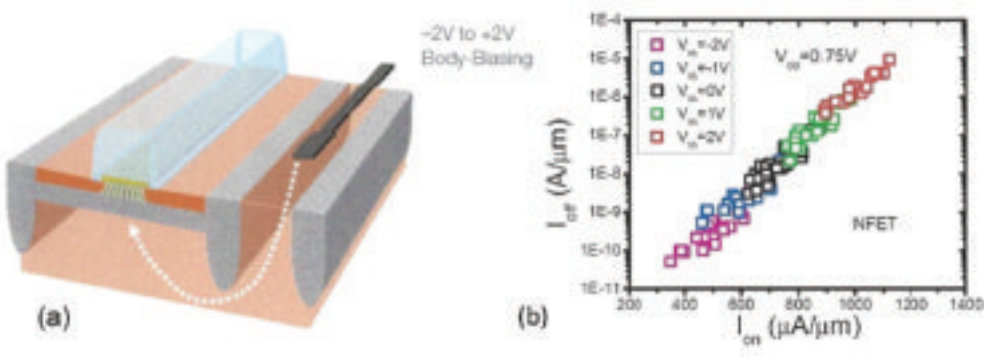


**FIGURE 1.** The unique benefit of back-bias is illustrated.

"To get the full benefit of body bias for power savings or performance improvement, the design teams must consider this feature from the very beginning of product development," she said. While biasing does not require specific EDA tools, and can be achieve with an extended library characterization, design architects must define the best corners for body bias in order to gain in performance and power. And design teams must implement "the right set of IPs to manage body biasing," such as a BB generator, BB monitors, and during testing, a trimming methodology.

Nguyen acknowledged that finFETs have drive-current advantages. But compared with bulk CMOS, FD-SOI has superior electrostatics, which enables scaling of analog/RF devices while maintaining a high transistor gain. And drive current increases as gate length is scaled, she said.

For 14/16 nm finFETs, Nguyen said the gate length is in the 25-30 nm range. The 22FDX transistors have a gate length in the 20nm range. "The very short gate length results in a small gate capacitance, and total lower gate resistance," she said.

For fringing capacitance, the most conservative number is that 22nm FD-SOI is 30 percent lower than leading finFETs, though she said "finFETs have made a lot of progress in this area."

## Analog advantages

It is in the analog and RF areas that FD-SOI offers the most significant advantages, Nguyen said. The fT and fMAX of 350 and 300 GHz, respectively, have been demonstrated by GlobalFoundries for its 22nm FD-SOI technology. For analog devices, she claimed that FD-SOI offers better transistor mismatch, high intrinsic device gain (Gm/Gds ratio), low noise, and flexibility in Vt tuning. **FIGURE 2** shows how 22FDX outperforms finFETs for fT/fMax.

"FDSOI is the only device architecture that meets all those requirements. Bulk planar CMOS suffers from large transistor mismatch due to random dopant fluctuation and low device gain due to poor electrostatics. FinFET technology improves on electrostatics but it lacks the back bias capability."

The undoped channel takes away the random doping effect of a partially depleted (doped) channel, reducing variation by 50-60 percent.

Analog designers using FD-SOI, she said, have "the ability to tune the Vt by back-bias to compensate for process mismatch or drift, and to offer virtually any Vt desired. Near-zero Vt can also be achieved in FD-SOI, which enables low voltage analog design for low power consumption applications."

"If you believe the future is about mobility, about more communications and low power consumption and cost sensitive IoT chips where analog and RF is about 50 percent of the chip, then FD-SOI has a good future.

"No single solution can fit all. The key is to build up the ecosystem, and with time, we are pushing that," she said.

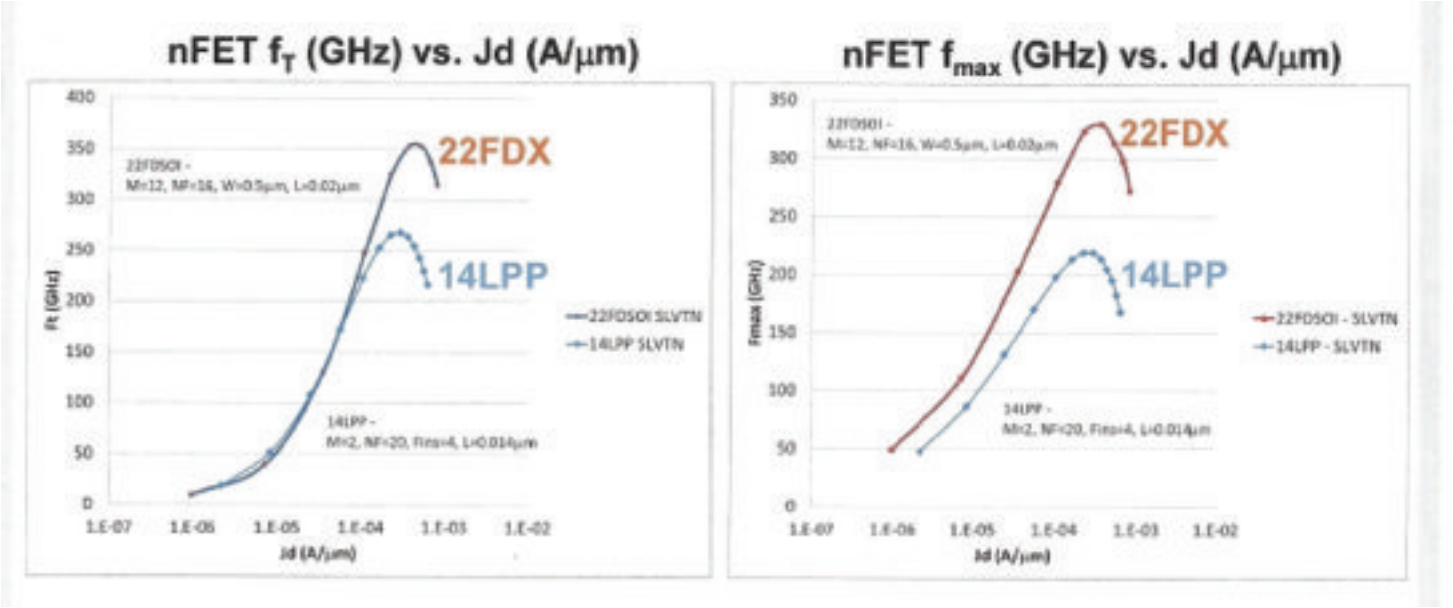


**FIGURE 2.** 22FDX outperforms finFETs for fT/fMax. Source: Global Foundries

# Salami slicing your yield

By **DAVID W. PRICE** *and* **DOUGLAS G. SUTHERLAND**, *KLA-Tencor, Milpitas, CA*

*An inspection strategy that guards only against catastrophic excursions can create the false sense of security.*

In a previous Process Watch article [1], we showed that big excursions are usually easy to detect but finding small excursions requires a combination of high capture rate and low noise. We also made the point that, in our experience, it's usually the smaller excursions which end up costing the fab more in lost product. Catastrophic excursions have a large initial impact but are almost always detected quickly. By contrast, smaller "micro-excursions" sometimes last for weeks, exposing hundreds or thousands of lots to suppressed yield.

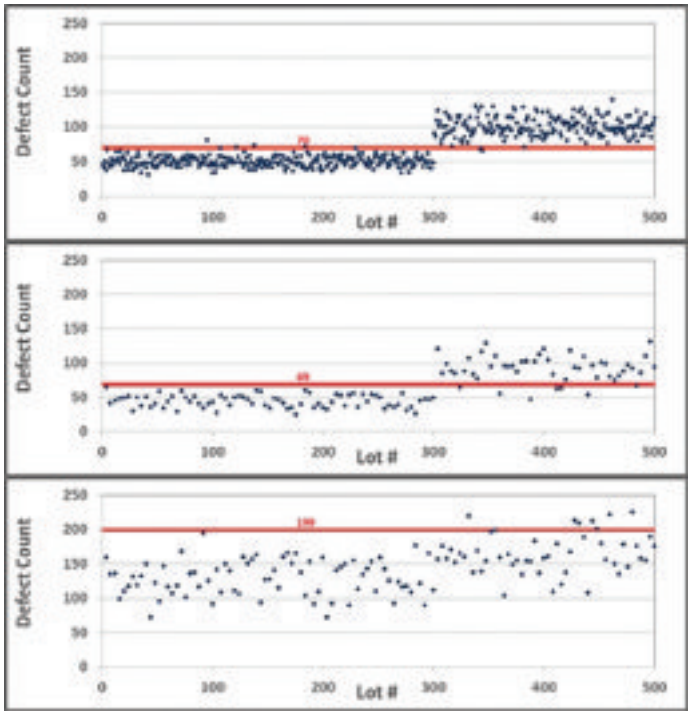


**FIGURE 1.** Illustration of a micro-excursion. Top: what is actually happening in the fab. Middle: the excursion through the lens of an effective control strategy (average 2.5 exposed lots). Bottom: the excursion from the perspective of a compromised inspection strategy (~40 exposed lots).

**FIGURE 1** shows an example of a micro-excursion. For reference, the top chart depicts what is actually happening in the fab with an excursion occurring at lot number 300. The middle chart shows the same excursion through the eyes of an effective inspection strategy; while there is some noise due to sampling and imperfect capture rate, it is generally possible to identify the excursion within a few lots. The bottom chart shows how this excursion would look if the fab employed a compromised inspection strategy—low capture rate, high capture rate variability, or a large number of defects that are not of interest; in this case, dozens of lots are exposed before the fab engineer can identify the excursion with enough confidence to take corrective action.

Unfortunately, the scenario depicted in the bottom of Figure 1 is all too common. Seemingly innocuous cost-saving tactics such as reduced sampling or using a less sensitive inspector can quickly render a control strategy to be ineffective [2]. Moreover, the fab may gain a false sense of security that the layer is being effectively monitored by virtue of its ability to find the larger excursions.

## Micro-Excursions

Table 1 illustrates the difference between catastrophic and micro-excursions. As the name implies, micro-excursions are subtle shifts away from the baseline. Of course, excursions may also take the form of anything in between these two.

Such baseline shifts happen to most, if not all, process tools—after all, that's why fabs employ rigorous preventative maintenance (PM) schedules. But PM's are expensive (parts, labor, lost production time), therefore fabs tend to put them off as long as possible.

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*Over the last 10 years, Dr. Price and Dr. Sutherland have worked directly with more than 50 semiconductor IC manufacturers to help them optimize their overall inspection strategy to achieve the lowest total cost. This series of articles attempts to summarize some of the universal lessons they have observed through these engagements.*

| | Catastrophic Excursion | Micro-Excursion |
|---|---|---|
| Wafer Level Yield Loss | High | Low |
| Baseline Shift | >>3x | < 3x |
| Frequency of Occurrence | Rare | Very Frequent |
| Onset | Step | Step or Drift |
| Ease of Detection | Usually Easy | Very Difficult |
| Typical Duration Before Detection | Short | Long |

**TABLE 1.** Catastrophic vs. Micro-Excursions

Because the individual micro-excursions are so small, they are difficult observe from end-of-line (EOL) yield data. They are frequently only seen in EOL yield data through the cumulative impact of dozens of micro-excursions occurring simultaneously; even then it more often appears to be baseline yield loss. As a result, fab engineers sometimes use the terms "salami slicing" or "penny shaving" since these phrases describe how a series of many small actions can, as an accumulated whole, produce a large result [3].

Micro-excursions are typically brought to an end because: (a) a fab detects them and puts the tool responsible for the excursion down; or, (b) the fab gets lucky and a regular PM resolves the problem and restores the tool to its baseline. In the latter case, the fab may never know there was a problem.

## The superposition of multiple simultaneous micro-excursions

To understand the combined impact of these multiple micro-excursions, it is important to recognize:

1. Micro-excursions on different layers (different process tools) will come and go at different times
2. Micro-excursions have different magnitudes in defectivity or baseline shift
3. Micro-excursions have different durations

In other words, each micro-excursion has a characteristic phase, amplitude and wavelength. Indeed, it is helpful to imagine individual micro-excursions as wave forms which combine to create a cumulative wave form. Mathematically, we can apply the Principle of Superposition [4] to model the resulting impact on yield from the contributing micro-excursions.

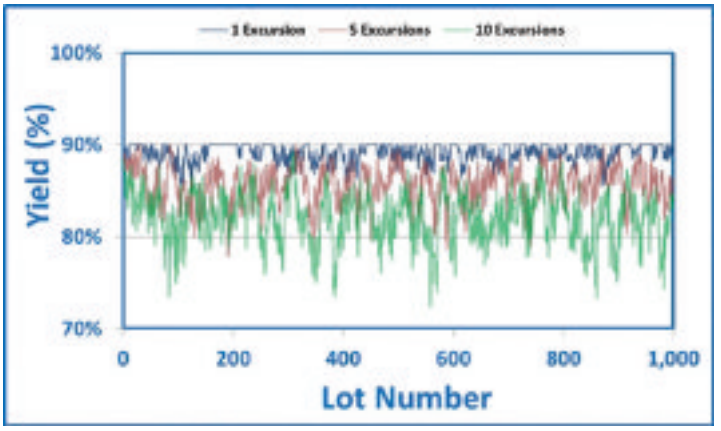


**FIGURE 2.** The cumulative impact of one, five, and 10 simultaneous micro-excursions happening in a 1,000 step process: increased yield loss and yield variation.

**FIGURE 2** illustrates the cumulative effect of one, five, and 10 micro-excursions happening simultaneously in a 1,000 step semiconductor process. In this case, we are assuming a baseline yield of 90 percent, that each micro-excursion has a magnitude of 2 percent baseline yield loss, and that they are detected on the 10th lot after it starts. As expected, the impact of a single micro-excursion is negligible but the combined impact is large.

It is interesting to note that the bottom curve in Figure 2 would seem to suggest that the fab is suffering from a baseline yield problem. However, what appears to be 80 percent baseline yield is actually 90 percent baseline yield with multiple simultaneous micro-excursions, which brings the average yield down to 80 percent. This distinction is important since it points to different approaches in how the fab might go about

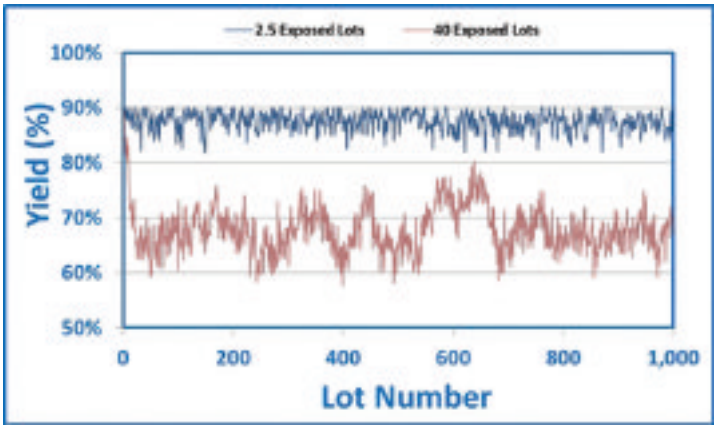


**FIGURE 3.** The impact of 10 simultaneous micro-excursions for the fab with a compromised inspection strategy (brown curve, ~40 lots at risk), and a fab with an effective process tool monitoring strategy (blue curve, ~2.5 lots at risk).

improving the average yield. A true baseline yield problem would suggest that the fab devote resources to run experiments to evaluate potential process improvements (design of experiments (DOEs), split lot experiments, failure analysis, etc.). These activities would ultimately prove frustrating as the engineers would be trying to pinpoint a dozen constantly-changing sources of yield loss.

The fab engineer who correctly surmises that this yield loss is, in fact, driven by micro-excursions would instead focus on implementing tighter process tool monitoring strategies. Specifically, they would examine the sensitivity and frequency of process tool monitor inspections; depending on the process tool, these monitors could be bare wafer inspectors on blanket wafers and/or laser scanning inspectors on product wafers. The goal is to ensure these inspections provide timely detection of small micro-excursions, not just the big excursions.

The impact of an improved process tool monitoring strategy can be seen in **FIGURE 3**. By improving the capture rate (sensitivity), reducing the number of non-critical defects (by doing pre/post inspections or using an effective binning routine), and reducing other sources of noise, the fab can bring the exposed product down from 40 lots to 2.5 lots. This, in turn, significantly reduces the yield loss and yield variation.

## Summary

Most fabs do a good job of finding the catastrophic defect excursions. Micro-excursions are much more common and much harder to detect. There are usually very small excursions happening simultaneously at many different layers that go completely undetected. The superposition of these micro-excursions leads to unexplained yield loss and unexplained yield variation.

As a yield engineer, you must be wary of this. An inspection strategy that guards only against catastrophic excursions can create the false sense of security that the layer is being effectively monitored—when in reality you are missing many of these smaller events that chip away or "salami slice" your yield.

Author's Note: The Process Watch series explores key concepts about process control—defect inspection and metrology—for the semiconductor industry. Following the previous installments, which examined the 10 fundamental truths of process control, this new series of articles highlights additional trends in process control, including successful implementation strategies and the benefits for IC manufacturing.

## References

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# Detecting fluorocarbons with infrared

**STEPHEN D. ANDERSON**, *Sensor Electronics Corp., Savage, MN*

*Detection and measurement of fluorocarbons is key to both process control and safety.*

Fluorocarbons (FCs) are widely used in the semiconductor industry in dry processing applications such as film etching, chemical vapor deposition (CVD), chamber cleaning, and as coolants for semiconductor manufacturing tools. Although toxicity levels are not well established, many FC compounds are considered somewhat toxic. Many FCs are also significant greenhouse gases, while others are flammable. Detection and measurement of FCs is key to both process control and safety. Examples of commonly used FCs in semiconductor manufacturing are given in Table 1.

Table Notes:

1. Although the table may list an FC as non-toxic, many are heavy gases that can cause asphyxiation. Others can cause severe frostbite. Some produce toxic byproducts, such as CO or HF if heated or burned.
2. The naming of organic compounds is often confusing, especially as to whether something is a fluorocarbon (FC) versus a perfluorocarbon (PFC). The latter usually refers to a compound in which all of the hydrogens have been replaced with fluorines. Then, trifluoromethane, for example, is an FC but not a PFC. Note also that the last two table entries don't follow this rule with respect to their common names.
3. The last two table entries have the same formula, C5HF7 , but much different structures and properties. In fact the first listed is a chain (aliphatic) compound while the second is a ring (aromatic). Always buy using the CAS Number and not the formula.

| Gas | Other Name(s) | CAS | Use | Description | Flammability | Toxicity |
|---|---|---|---|---|---|---|
| Difluoromethane $CH_2F_2$ | Freon 32, R 32 | 75-10-5 | High Aspect Etching, Refrigerant | Colorless, Odorless, BP 52 C. | Flammable | Non-Toxic |
| Fluoromethane $CH_3F$ | Freon 41 | 593-53-3 | Etching | Colorless, Sweet Ether-like odor, BP -79 C | Flammable | Non-Toxic |
| Hexafluorobutadiene $C_4F_6$ | Sifren 46 | 685-63-2 | Dielectric Etching | Colorless, Odorless, BP 7 C | Flammable | Irritant |
| Octofluorocyclopentene $C_5F_8$ | | 559-40-0 | Dry Etching | Colorless, Slight Distinct Odor, BP 27 C | Non-Flammable | Toxic |
| Trifluoromethane $CHF_3$ | Fluoroform, R23 | 75-46-7 | High Aspect Etching | Colorless, Odorless, BP -82 C | Non-Flammable | Low Toxicity |
| Octofluorocyclobutane $C_4F_8$ | Freon C 318 | 115-25-3 | Deposition, Etching | Colorless, Slight Ether-like Odor, BP -8 C | Non-Flammable | Low Toxicity |
| Perfluorotripropylamine $(C_3F_7)_3N$ | Fluorinert FC-3283 | 338-83-0 | Heat Transfer Liquid | Colorless, Odorless, BP 130 C | Non-Flammable | Low Toxicity |
| Hexafluoropropene $C_3F_6$ | Hexafluoropropylene | 116-15-4 | Dielectric Etch | Colorless, Odorless, BP -29 C | Non-Flammable | Slight Toxicity, Irritant |
| 3,4,4,4-Tetrafluoro-3-trifluoromethyl-but-1-yne $C_5HF_7$ | (Perfluoroisopropyl) acetylene | 24690-53-7 | Plasma Etch | Limited Data, BP 23 C | Flammable | Irritant |
| 1,3,3,4,4,5,5-Heptafluorocyclopent-1-ene $C_5HF_7$ | 1H-Perfluoro(cyclopent-1-ene) | 1892-03-1 | Dry Etching | Limited Data, Colorless, BP 28 C | Flammable | Toxic |

**TABLE 1.**

## Why infrared?

Among the available gas detection methods are:

- Catalytic bead – Generates heat when exposed to combustible gas.
- Electrochemical cell – Generates electrical current in response to specific gas.
- Photoionization detector (PID) – Ionizes gas using UV light, measures ion current.
- Pyrolyzer – Decomposes gas using heat, measures decomposition products.
- Infrared absorption (IR) – Gas blocks infrared path from source to detector.

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- Metal oxide semiconductor (MOS) – Increases resistance in presence of gas.

To detect FCs, electrochemical cells are eliminated, since none are designed to sense FCs. The PID can also be eliminated because UV light used is not energetic enough to ionize FCs. Catalytic beads are poisoned by halogen compounds and shouldn't be used.

The Pyrolyzer can measure FCs. But, since it destroys the gas being measured, it cannot distinguish one FC from another. It is also difficult to make the Pyrolyzer explosion-proof or intrinsically safe.

MOS sensors require ambient air to operate, are easily contaminated, and are not specific.

IR alone has the ability to sense a specific FC gas.

## The F-C bond

The common feature of FCs is the carbon-fluorine bond. The stretching vibrations of this bond result in infrared (IR) absorption at wavelengths ranging approximately from 7 to 10 micron [1]. The precise wavelength of absorption varies with the overall molecular structure, and is given in **TABLE 2**.

For example, measuring the absorption at 10.4 micron can tell us how much C4F6 is present.

An entire branch of chemical study deals with determining structure from absorption bands and vice-versa.

| Gas | Absorption Wavelength (micron) |
|---|---|
| Difluoromethane $CH_2F_2$ | 8.7 |
| Fluoromethane $CH_3F$ | 9.3 |
| Hexafluorobutadiene $C_4F_6$ | 10.4 |
| Octofluorocyclopentene $C_5F_8$ | 6.3 |
| Trifluoromethane $CHF_3$ | 8.7 |
| Octofluorocyclobutane $C_4F_8$ | 10.5 |
| Fluorinert $(C_3F_7)_3N$ | 9.7* |
| Hexafluoropropylene $C_3F_6$ | 9.6* |
| (Perfluoroisopropyl)acetylene $C_5HF_7$ | * |
| Heptafluorocyclopentene $C_5HF_7$ | 8.7* |

* Under development, subject to change

**TABLE 2.**

Infrared spectrometers, commonly used in these studies, have the ability to sweep through many wavelengths, looking at absorption versus wavelength.

The technique of gas detection by measuring absorption at one wavelength is termed NDIR (non-dispersive infrared). Non-dispersive means that a particular wavelength is selected using a fixed optical filter, in contrast to the variable mechanical filter used in an IR spectrometer. An NDIR is less flexible than an IR spectrometer, but has the advantage of no moving parts or complex optics, making it ideal for industrial environments.

## NDIR

The principle of the NDIR is illustrated in **FIGURE 1**. The IR spectrum at specific points in the NDIR device is included (spectrum plots 1 - 4). The plots assume that target gas is present and absorbing at 7 micron.

The IR source (spectrum 1) is a Graybody source (the term applied to a bsource with an emissivity less than 1), which provides IR light across a range of wavelengths from about 1 to 15 micron. A range of wavelengths is desired so that one source can be used to sense a variety of gases.

The light from the source passes through the target gas in a "waveguide" – a reflective chamber open to the atmosphere. The spectrum at the saveguide output (spectrum 2) shows a notch (attenuation) at 7 micron, due to absorption by the target gas.

The light is next applied to optical filters – the wavelength-selective parts of the NDIR. Each optical filter is a narrow bandpass filter, made from a window with various coatings that "create" optical interference except at wavelengths of interest. A typical filter bandwidth is 0.25 micron.

The target filter passes light in the range of about 6.9 micron to 7.1 micron, resulting in spectrum 3, which shows the effects of both the gas and filter. The NDIR usually includes a reference optical filter – a filter that passes light where the target gas is transparent – as a means of maintaining a fixed gain or sensitivity in the presence of varying Source light levels. In the example, the reference filter at 3 micron passes light in the range of about 2.9 micron to 3.1 micron, resulting in spectrum 4 (Note: The filter bandwidths in Fig. 1 are wider than actual for purposes of illustration).

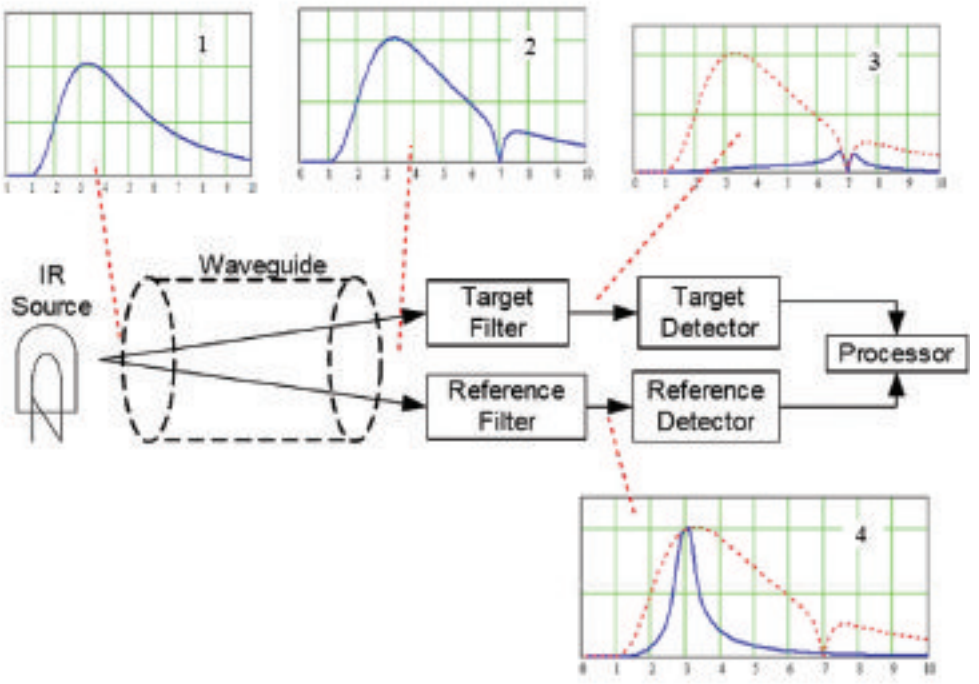


**FIGURE 1.** The principle of the non-dispersive infrared (NDIR) measurement is illustrated.

The outputs of the two filters are applied to separate detectors (bolometer or thermopile) and converted to electrical signals.

The IR source is usually driven by a square wave to create a modulation in the IR output. The resulting AC signal allows for easier removal of offset and drift. For the highest possible modulation frequencies, newer MEMS-based sources with extremely small thermal mass, have recently become available.

Note that an NDIR can be created by other means. For example, the source might be an IR laser diode or IR light-emitting-diode. These alternate sources are generally at a disadvantage to the thermal source because of their limited bandwidth. Tunable laser diodes exist but are very expensive at present. Also, at the receiving end of the light path, an NDIR might use one or more photo-diodes rather than thermal detectors.

## NDIR features

The light absorption by the target gas is exponentially related to gas concentration. This non-linearity is removed using a microcontroller algorithm that is generally different for each FC and each concentration range.

The NDIR also measures temperature and pressure, allowing for ideal gas law correction, which is used when the measurand is concentration rather than density. Temperature measurement also allows for temperature compensation of zero and span.

An NDIR device, as described here, typically measures concentration in the range of 100 ppm to 1000 ppm (by volume) or density in the range of 200 to 2000 milligram / liter. Typical accuracy is 5% of range. Special designs with long optical path length are now available for smaller concentrations.

NDIR maintenance is generally limited to periodic calibration of zero and span, and keeping the optical surfaces free of dust and obstruction. Because the NDIR measures transmittance, it is inherently fail-safe:

No light = Lots of gas (or obstruction or Source fail) = Alarm

The simple and rugged optical system keeps unit cost and maintenance low, while increasing reliability.

## Liquid FCs?

Several FCs are liquids at room temperature or have boiling points close to room temperature. NDIRs are ideal at sensing the liquid vapor, since the NDIR is easily made a part of the calibration setup. All that's needed to calibrate is a controlled temperature and a table of vapor pressure versus temperature at equilibrium.

## Conclusion

The NDIR is proving to be a the instrument of choice in detecting fluorocarbons. Its main features of selectivity, mechanical ruggedness, and operational simplicity are pushing aside other detection methods. Future NDIRs are expected to further this trend with improved ability to pinpoint a given FC gas in the presence of industrial cleaners and other interfering products.

## References

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# Semiconductor materials: restructuring in the supplier base

Earlier this year, the Nikkei Asian Review (and other sources) reported the exit of Sumitomo Metal Mining (SMM) from the leadframe business. Leadframe makers headquartered in Japan have long had a prominent share of the global leadframe market, and SMM has been a top supplier for decades. And just several years ago, SMM and Hitachi Cable integrated their leadframe operations. According to the Nikkei Asian Review article, Chang Wah of Electronic Materials (Taiwan) is acquiring some of the SMM leadframe operations, while the article reports that SMM is negotiating the sale of its power semiconductor leadframe business to Jih Lin Technology (Taiwan).

"Given the pricing pressures in the industry, the trend towards smaller, lower cost leadframes, and the transition to non-leadframe technologies, the long-term outlook for the leadframe market from a business perspective remains very challenging as overall revenue growth is unlikely."


**FIGURE 1.** Worldwide market share of china headquartered leadframe suppliers.

SMM previously exited the bonding wire market in 2012, so this latest announcement reflects the company's move away from commoditized material segments. According to SEMI's own analysis, the leadframe market that has seen very little revenue growth over the past 12 years and it is an industry segment with a large supplier base, with over 30 suppliers globally. The basis for competition in the leadframe business has long been, generally speaking, lowest price and shortest turn-around time. Leadframes are a commodity, though plating and etching capabilities can be a differentiator among the suppliers.

Over the past decade while production facilities in Japan and Southeast Asia closed, many leadframe suppliers shifted production to and increased capabilities in China. Also, China headquartered leadframe suppliers are numerous. These suppliers in China have typically focused on low-lead count and discrete leadframe products for domestic assembly plants, though some companies have expanded capabilities to produce higher value leadframe products. The market share of the China headquartered suppliers has gradually been growing.

Given the pricing pressures in the industry, the trend towards smaller, lower cost leadframes, and the transition to non-leadframe technologies, the long-term outlook for the leadframe market from a business perspective remains very challenging as overall revenue growth is unlikely. Expect further consolidation and the continued emergence of China suppliers in this longstanding packaging material segment.

The SEMI Strategic Material Conference 2017 will be held September 19-20 in San Jose, Calif.

**DAN TRACY**, *senior director, Industry Research & Statistics, SEMI*

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