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NOVEMBER/DECEMBER 2017

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Insights for Electronics Manufacturing

Resin Bleed Out and How to Control It

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CMP Models for Hotspot Detection

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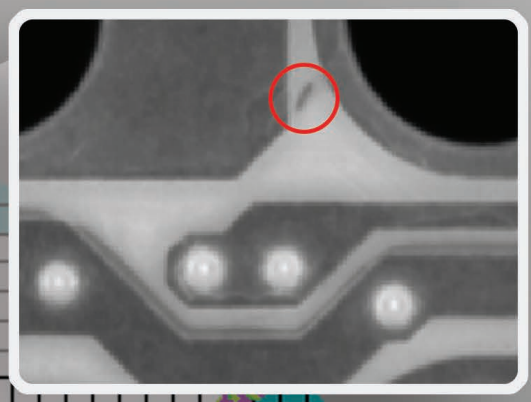

Revealing Previously Hidden Defects P.11

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IBM Distinguished Engineer
Advanced Process
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George Gomba
VP Technology Research
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Tom Sonderman
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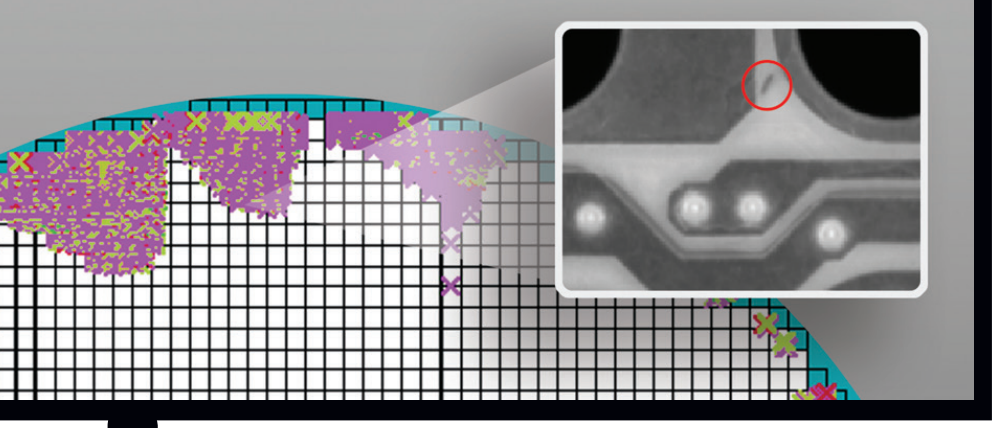

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Clearfind, a new optical technique can reveal defects and contaminants that escape conventional inspection technologies in many advanced packaging applications.

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Rongwei Zhang, Abram Castro and Yong Lin, Semiconductor Packaging, Texas Instruments Inc., Dallas, TX

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The ConFab 2018 Update

A new wave of growth is sweeping through the semiconductor industry, propelled by a vast array of new applications, including artificial intelligence, virtual and augmented reality, automotive, 5G, the IoT, cloud computing, healthcare and many others. The big question facing today's semiconductor manufacturers and their suppliers is how can they best position themselves to take advantage of this tremendous growth.

Finding answers to that question is the goal of The ConFab 2018, to be held May 20-23 at The Cosmopolitan of Las Vegas. Now in its 14th year, The ConFab is a conference and networking event designed to inform and connect leading semiconductor executives from all parts of the supply chain. It is produced by Solid State Technology magazine, the semiconductor industry's oldest and most respected business publication.

Kicking things off will be IBM's Rama Divakaruni, who will speak on "How AI is Driving the New Semiconductor Era." This is hugely important to how semiconductors will be designed and manufactured in the future, because AI --- now in its infancy -- will demand dramatic enhancement in computational performance and efficiency. Fundamental changes will be required in algorithms, systems and chip design. Devices and materials will also need to change.

Rama is well position to address these changes: As an IBM Distinguished Engineer, he is responsible for IBM Advanced Process Technology Research (which includes EUV technologies and advanced unit process and Enablement technologies) as well as the main interface between IBM Semiconductor Research and IBM's Systems Leadership. He is one of IBMs top inventors with over 225+ issued US patents.

We're also pleased to announce several other speakers at this point. Joining us will be George Gomba, VP of technology research at GlobalFoundries. George has overall responsibility for GlobalFoundries' semiconductor technology research programs, including global consortia and strategic supplier management (and, like Rama, has a long history at IBM). The focus of George's talk will be on EUV lithography.

Dan Armbrust, Founder and Director of Silicon Catalyst, the world's first incubator focused exclusively on semiconductor solutions startups will also be on the dais. A frequent speaker at The ConFab, Dan has a great background, including President and Chief Executive Officer of SEMATECH, IBM VP, 300mm Semiconductor Operations, and Strategic Client Exec for IBM's Systems and Technology Group.

Another great speaker is Tom Sonderman, President of SkyWater Technology Foundry. Tom also has a great background including GlobalFoundries' VP of manufacturing technology, and two decases at AMD, where he had global responsibility for development, integration, support and scalability of automation and manufacturing systems in the company's wafer fabrication and assembly operations. Prior to joining SkyWater, Prior to joining SkyWater, Tom was the group vice president and general manager for Rudolph Technologies' Integrated Solutions Group. In this position, he created a Smart Manufacturing ecosystem based on big data platforms, predictive analytics and IoT.

We're so excited about the other speakers we tentatively have lined up, our plans for several thought-provoking panels and much more, so stay tuned. You register and keep up-to-date by visiting www.theconfab.com. For sponsorship inquiries, contact Kerry Hoffman at khoffman@extensionmedia.com. For those interested in attending as a guest or qualifying as a VIP, contact Sally Bixby at sbixby@extensionmedia.com.

—Pete Singer, Editor-in-Chief

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Web Exclusives

The intelligence that leads to artificial intelligence

Artificial intelligence (AI) may be a hot topic today, but SEMI has helped to incubate Big Data and AI since its founding. Early in SEMI's history, SEMI's always intelligent members worked together to introduce International Standards that enabled different pieces of equipment to collect and later pass data. At first, it was for basic interoperability and equipment state analysis. Later, SEMI data protocol Standards allowed process and metrology data to be used locally and across the fab to approach the goals of Smart Manufacturing and AI – for the equipment itself to make adjustments based on incoming wafer data.

http://bit.ly/2jfQ9Jz

IBM Technology influencer to deliver keynote address at The ConFab 2018

The ConFab, to be held May 20-23 at The Cosmopolitan of Las Vegas, is excited to announce IBM's Dr. Rama Divakaruni will be the opening keynote for the 2018 conference. Dr. Divakaruni's presentation is entitled, "How AI is Driving the New Semiconductor Era". He will address the Artificial Intelligence era demands for dramatic enhancement in computational performance and efficiency of AI workloads, and discuss the needs and changes required in algorithms, systems and chip design as well as in devices and materials.

http://bit.ly/2hYbGDf

EUVL technology status update

This blog gives the latest update on the status of EUVL, based on data released this summer from the 2017 EUVL Workshop, 2017 Semicon West and recent announcements.

http://bit.ly/2jdV8ui

n&b news and blogs

Insights from the Leading Edge: ARM on IoT

Will IoT require "dirt cheap" packaging? Those of you following IFTLE's position on IoT know that, while Phil Garrou certainly sees a future where the wireless collection of data proliferates, he sees this, in general, for extreme low cost packaging solutions, certainly not, as some have said in the past, an IoT using 2.5/3D solutions.

http://bit.ly/2zww3AT

Mott memristor chaos could make efficient AI

Congratulations to Suhas Kumar, John Paul Strachan, and R. Stanley Williams of Hewlett Packard Labs in Palo Alto for showing not just how to make a Mott memristor, but that you can create controlled chaos with one. (From SemiMD.com)

http://bit.ly/2mb8mZQ

New frontiers for EUVL

In this blog, Vivek Bakshi focuses on EUV Sources that will enable not only EUVL scanners but also leading-edge metrology needed for EUVL at 7 nm nodes and beyond. He highlights how several papers in the upcoming EUV Source Workshop in Dublin (November 6-8, 2017) will address these topics.

http://bit.ly/2yMLDJu

2017 Global Semiconductor Alliance Award nominees announced

The Global Semiconductor Alliance (GSA) today announced the 2017 award nominees for the GSA Awards Dinner Celebration. Featuring a new Master of Ceremonies format hosted by Wayne Brady, five-time Emmy winner and Grammy nominee, the celebration will take place on Thursday, December 7, 2017, at the Santa Clara Convention Center in Santa Clara, California.

http://bit.ly/2il84om

Please send news articles to sdavis@extensionmedia.com

news

worldnews

ASIA - **NXP** and Chongqing established a center for automotive electronics applications development in China.

USA - **Dialog Semiconductor** announced the completion of its acquisition of Silego Technology.

ASIA - **TowerJazz** and **Yuanchen Microelectronics** announced their new partnership for BSI manufacturing.

USA - **Microsemi** announced plans to acquire the high performance timing business of **Vectron International**.

EUROPE – **CEA-Leti** announced its coordinating a European project to improve drivetrains for electric vehicles.

USA - **sureCore** joined **GLOBALFOUNDRIES'** FDXcelerator Partner Program.

ASIA – **NVIDIA** and **Taiwan's Ministry of Science and Technology** announced plans to accelerate Taiwan AI revolution with NVIDIA AI computing platform.

USA - **Praxair** signed a long-term agreement to supply nitrogen to **GLOBALFOUNDRIES**.

ASIA - **Samsung** announced that its 8nm FinFET process technology, 8LPP (Low Power Plus) has been qualified and is ready for production.

Deep-depletion: A new concept for MOSFETs

Silicon has provided enormous benefits to the power electronics industry. But performance of silicon-based power electronics is nearing maximum capacity.

Enter wide bandgap (WBG) semiconductors. Seen as significantly more energy-efficient, they have emerged as leading contenders in developing field-effect transistors (FETs) for next-generation power electronics. Such FET technology would benefit everything from power-grid distribution of renewable-energy sources to car and train engines.

Diamond is largely recognized as the most ideal material in WBG development, owing to its superior physical properties, which allow devices to operate at much higher temperatures, voltages and frequencies, with reduced semiconductor losses.

A main challenge, however, in realizing the full potential of diamond in an important type of FET — namely, metal-oxide-semiconductor field-effect transistors (MOSFETs) — is the ability to increase the hole channel carrier mobility. This mobility, related to the ease with which current flows, is essential for the on-state current of MOSFETs.

Researchers from France, the United Kingdom and Japan incorporate a new approach to solve this problem by using the deep-depletion regime of bulk-boron-doped diamond MOSFETs. The new proof of concept enables the production of simple diamond MOSFET structures from single boron-doped epilayer stacks. This new method, specific to WBG semiconductors, increases the mobility by an order of magnitude. The results are published this week in Applied Physics Letters, from AIP Publishing.

In a typical MOSFET structure, an oxide layer and then a metal gate are formed on top of a semiconductor, which in this case is diamond. By applying a voltage to the metal gate, the carrier density, and hence the conductivity, of the diamond region just under the gate, the channel, can be changed dramatically. The ability to use this electric "field-effect" to control the

Continued on page 6

A*STAR IME's new multi-chip FOWLP development line to drive innovation and growth in semiconductor industry

A*STAR's Institute of Microelectronics (IME) has established a development line to accelerate the development of fan-out wafer level packaging (FOWLP) capabilities for next-generation Internet of Things (IoT) technologies. The FOWLP development line, which is built upon existing infrastructure at IME's facilities at Singapore Science Park II, and its new facilities at Fusionopolis Two, will allow IME and its partners (see Annex A for list of partners) to develop technologies that serve a wide range of markets such as that of consumer electronics, healthcare and automotive.

The IoT is set to become the next growth driver for the semiconductor industry, as demand for internet-connected devices continues to soar. FOWLP is an emerging breakthrough chip packaging technology platform aimed at meeting the technology requirements of next-generation electronic devices that require ultra- low power consumption rates, smaller package profiles, higher performance; and all made at a lower cost.

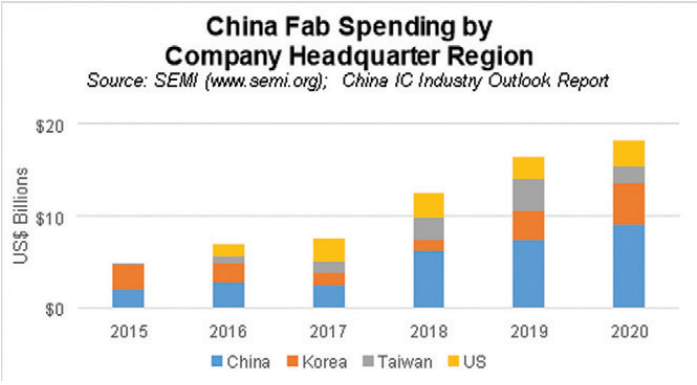
IME's FOWLP development line is equipped with fully automated tools that can perform

Continued on page 6

China IC industry outlook

SEMI, the global industry association and provider of independent electronics market research, announced its new China IC Industry Outlook Report, a comprehensive report for the electronics manufacturing supply chain. With an increasing presence in the global semiconductor manufacturing supply chain, the market opportunities in China are expanding dramatically.

China is the largest consumer of semiconductors in the world, but it currently relies mainly on semiconductor imports to drive its growth. Policies and investment funds are now in place to further advance the progress of indigenous suppliers in China throughout the entire semiconductor supply chain. This shift in policy and related initiatives have created widespread interest in the challenges and opportunities in China.



With at least 15 new fab projects underway or announced in China since 2017, spending on semiconductor fab equipment is forecast to surge to more than $12 billion, annually, by 2018. As a result, China is projected to be the top spending region in fab equipment by 2019, and is likely to approach record all-time levels for annual spending for a single region.

This report covers the full spectrum of the China IC industry within the context of the global semiconductor industry. With more than 60 charts, data tables, and industry maps from SEMI sources, the report reveals the history and the latest industry developments in China across vast geographical areas ranging from coastline cities to the less developed though emerging mid-western regions.

The China IC industry ecosystem outlook covers central and local government policies, public and private funding, the industry value chain from design to manufacturing and equipment to materials suppliers. Key players in each industry sector are highlighted and discussed, along with insights into China domestic companies with respect to their international peers, and potential supply implications from local equipment and material suppliers. The report specifically details semiconductor fab investment in China, as well as the supply chain for domestic equipment and material suppliers. ◆

Broadcom proposes to acquire Qualcomm

Broadcom Limited, a semiconductor device supplier to the wired, wireless, enterprise storage, and industrial end markets, announced a proposal to acquire all of the outstanding shares of Qualcomm Incorporated for per share consideration of $70.00 in cash and stock.

Under Broadcom's proposal, the $70.00 per share to be received by Qualcomm stockholders would consist of $60.00 in cash and $10.00 per share in Broadcom shares. Broadcom's proposal represents a 28% premium over the closing price of Qualcomm common stock on November 2, 2017, the last unaffected trading day prior to media speculation regarding a potential transaction, and a premium of 33% to Qualcomm's unaffected 30-day volume-weighted average price. The Broadcom proposal stands whether Qualcomm's pending acquisition of NXP Semiconductors N.V. ("NXP") is consummated on the currently disclosed terms of $110 per NXP share or the transaction is terminated. The proposed transaction is valued at approximately $130 billion on a pro forma basis, including $25 billion of net debt, giving effect

Continued on page 8

Deep-depletion, Continued from page 4

channel conductivity and switch MOSFETS from conducting (on-state) to highly insulating (off-state) drives their use in power control applications. Many of the diamond MOSFETs demonstrated to date rely on a hydrogen-terminated diamond surface to transfer positively charged carriers, known as holes, into the channel. More recently, operation of oxygen terminated diamond MOS structures in an inversion regime, similar to the common mode of operation of silicon MOSFETS, has been demonstrated. The on-state current of a MOSFET is strongly dependent on the channel mobility and in many of these MOSFET designs, the mobility is sensitive to roughness and defect states at the oxide diamond interface where unwanted carrier scattering occurs.

To address this issue, the researchers explored a different mode of operation, the deep-depletion concept. To build their MOSFET, the researchers deposited a layer of aluminum oxide (Al2O3) at 380 degrees Celsius over an oxygen-terminated thick diamond epitaxial layer. They created holes in the diamond layer by incorporating boron atoms into the layer. Boron has one less valence electron than carbon, so including it leaves a missing electron which acts like the addition of a positive charge, or hole. The bulk epilayer functioned as a thick conducting hole channel. The transistor was switched from the on-state to the off-state by application of a voltage which repelled and depleted the holes — the deep depletion region. In silicon-based transistors, this voltage would have also resulted in formation of an inversion layer and the transistor would not have turned off. The authors were able to demonstrate that the unique properties of diamond, and in particular the large band gap, suppressed formation of the inversion layer allowing operation in the deep depletion regime.

"We fabricated a transistor in which the on-state is ensured by the bulk channel conduction through the boron-doped diamond epilayer," said Julien Pernot, a researcher at the

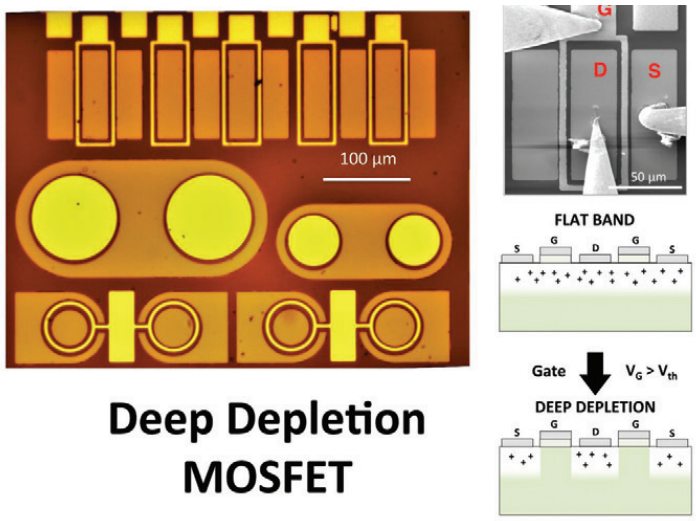


FIGURE. Left: Optical microscope image of the MOSCAPs and diamond deep depletion MOSFETs (D2MOSFETs) of this work. Top right: Scanning electron microscope image of a diamond D2MOSFET under electrical investigation. S: Source, G: Gate, D: Drain. Bottom right: D2MOSFET concept. The on-state of the transistor is ensured thanks to the accumulation or flat band regime. The high mobility channel is the boron-doped diamond epilayer. The off-state is achieved thanks to the deep depletion regime, which is stable only for wide bandgap semiconductors. For a gate voltage larger than a given threshold, the channel is closed because of the deeply and fully depleted layer under the gate. Credit: Institut NÉEL

NEEL Institute in France and an author of the paper. "The off-state is ensured by the thick insulating layer induced by the deep-depletion regime. Our proof of concept paves the way in fully exploiting the potential of diamond for MOSFET applications." The researchers plan to produce these structures through their new startup called DiamFab.

Pernot observed that similar principles of this work could apply to other WBG semiconductors. "Boron is the doping solution for diamond," Pernot said, "but other dopant impurities would likely be suitable to enable other wide bandgap semiconductors to reach a stable deep-depletion regime." ◆

*A*STAR IME,* Continued from page 4

the "mold-first" and "Re-Distribution Layer (RDL)-first" method in multi- chip fabrication. The "RDL-first" method is expected to achieve a higher reliability rate compared to the conventional "mold-first" method traditionally used by the semiconductor industry. IME and its partners will jointly develop tools and processes for next-generation FOWLP technologies such as high speed Copper (Cu) pillar plating, Physical Vapor Deposition (PVD) process to control the wafer warpage, moldable underfilling for Chip-to-Wafer, as well as over molding on wafer with vertical Cu pillar/ Cu wire interconnections using wafer level compression molding, plasma descum of small vias and warpage adjustment, etc.

To unlock the potential of FOWLP and accelerate the development and adoption of these innovative process technologies by the industry, IME has also formed a consortium comprising leading OSATs, Materials, Equipment, EDA, Fabless partners (see Annex A for list of consortium members).

The FOWLP development line consortium will allow members across the value chain to co-share resources on an open innovation platform, and draw upon IME's rich portfolio of advanced packaging capabilities to address the complexities

in system scaling and heterogeneous system integration. The FOWLP development line will be a test-bedding platform through which consortium members could gain new insights on requirements of FOWLP by testing and developing new processes, paving the way for high-volume manufacturing.

The FOWLP development line utilises tools already in use in major OSATs, and will allow processes, materials and integration flows developed at IME to be smoothly transferred. Through this development line, fabless companies could also make quicker decisions on package structure, integration flows, processes, materials and equipment for their new products; so materials and equipment suppliers could expedite the development of their products and increase their adoption.

"The launch of IME's FOWLP development line and consortium will enable us to advance pre-competitive R&D that positions the semiconductor industry for growth opportunities in the thriving IoT market. Through an open and collaborative approach, the consortium will drive the development and the transfer of innovative technologies from pilot-scale to commercial production more easily and quickly," said Dr. Tan Yong Tsong, Executive Director, IME.

"We are extremely proud to be a part of IME's FOWLP consortium and play an active role in this great initiative. This broad industry cooperation will help solve one of the largest challenges faced by the semiconductor industry in the area of achieving higher density in advanced packaging. ERS is committed to developing new thermo-management solutions to enable next generation of FOWLP technologies," said Mr. Klemens Reitinger, Chief Executive Officer, ERS Electronic GmbH.

"We are pleased to be collaborating with IME in this FOWLP development line consortium (DLC). We have benefitted from the experience in the previous consortium on High Density FOWLP, and are confident that with our combined experience and knowledge, the consortium will accelerate the development of FOWLP and establish an innovative cost-effective manufacturing process to further the mass adoption of FOWLP," said Mr. Tong Liang Cheam, Vice President of Corporate Strategy, Kulicke & Soffa.

"It's exciting to participate in this new FOWLP development line at IME to advance chip packaging. Nordson has a successful history of working on innovations in the semiconductor packaging industry, and this consortium is positioned well

A*STAR IME, *Continued*

to produce excellent solutions," said Mr. Joseph Stockunas, Vice President, Advanced Technology – Electronics Systems, Nordson Corporation.

"It is through collaborative efforts, such as that of the FOWLP development line and consortium that the semiconductor ecosystem can advance. Our engagement with the consortium will not only benefit our customers, but the industry as a whole in driving the adoption of this technology for emerging High Bandwidth Memory (HBM) and diverse IoT applications," said Mr. Asim Salim, Vice President of Manufacturing Operations, Open-Silicon. "Through Open- Silicon's extensive experience in 2.5D ASIC design, and the expertise of the consortium, issues like cost will be mitigated, thus enabling OEMs of all sizes to adopt FOWLP technology."

"We are delighted to be a part of IME's FOWLP development line consortium and continue to play an active role in this open innovation initiative. Industry-wide cooperation is key in overcoming the many challenges faced today by the electronics packaging industry. Orbotech is committed to developing new cost- efficient solutions to enable the next generation of advanced packaging technologies, which in turn will impact the industry's next inflection point," said Dr. Abraham Gross, Chief Technology Officer and Head of Innovation, Orbotech.

"As demand for high speed, high bandwidth data connectivity in consumer electronics continues to grow, the performance and cost challenges limiting the implementation of high frequency millimeter wave applications have the potential to be addressed with FOWLP solutions. We look forward to working with the FOWLP development line consortium to realise the benefits of FOWLP technology for mmWave antennae devices in emerging markets such as automotive and the Internet of Things (IoT)," said Mr. Shim Il Kwon, Chief Technology Officer, STATS ChipPAC.

The Institute of Microelectronics (IME) is a research institute of the Science and Engineering Research Council of the Agency for Science, Technology and Research (A*STAR). ◁▶

Broadcom, *Continued from page 5*

to Qualcomm's pending acquisition of NXP on its currently disclosed terms.

"Broadcom's proposal is compelling for stockholders and stakeholders in both companies. Our proposal provides Qualcomm stockholders with a substantial and immediate premium in cash for their shares, as well as the opportunity to participate in the upside potential of the combined company," said Hock Tan, President and Chief Executive Officer of Broadcom. "This complementary transaction will position the combined company as a global communications leader with an impressive portfolio of technologies and products. We would not make this offer if we were not confident that our common global customers would embrace the proposed combination. With greater scale and broader product diversification, the combined company will be positioned to deliver more advanced semiconductor solutions for our global customers and drive enhanced stockholder value."

Tan continued, "We have great respect for the company founded 32 years ago by Irwin Jacobs, Andrew Viterbi and their colleagues, and the revolutionary technologies they developed. Following the combination, Qualcomm will be best positioned to build on its legacy of innovation and invention. Given the common strengths of our businesses and our shared heritage of, and continued focus on, technology innovation, we are confident we can quickly realize the benefits of this compelling transaction for all stakeholders. Importantly, we believe that Qualcommand Broadcom employees will benefit from substantial opportunities for growth and development as part of a larger company."

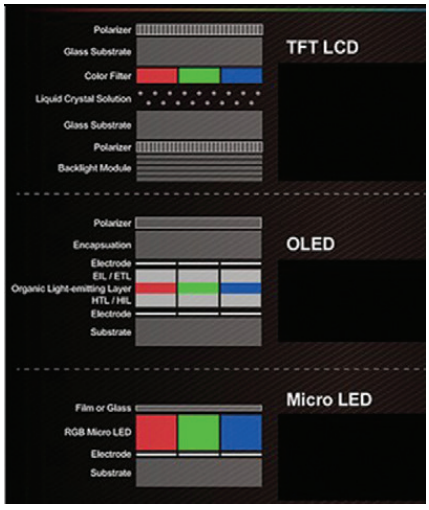
Thomas Krause, Broadcom Chief Financial Officer, added, "The Broadcom business continues to perform very well. Broadcom has completed five major acquisitions since 2013, and has a proven track record of rapidly deleveraging and successfully integrating companies to create value for our stockholders, employees and customers. Given the complementary nature of our products, we are confident that any regulatory requirements necessary to complete a combination with Qualcomm will be met in a timely manner. We look forward to engaging immediately in discussions with Qualcomm so that we can sign a definitive agreement and complete this transaction expeditiously."

"The combined Qualcomm/Broadcom operation would represent the third largest global semiconductor supplier. The Qualcomm shareholders are likely to be split with many viewing this opportunity as a solution to the worsening relations with Apple, whom Broadcom has a good relationship with. The potential merger raises significant questions surrounding the difficult takeover of NXP by Qualcomm and much is still to be discerned regarding the value of the Qualcomm patent holdings and its associated lucrative high-margin revenue stream," said Stuart Carlaw, Chief Research Officer at ABI Research. ◁▶

The case for µLED displays

PHIL GARROU,
Contributing Editor

Earlier this year, DARPA's Microsystems Technology Office (MTO) announced a new Electronics Resurgence Initiative (ERI) "to open pathways for far-reaching improvements in electronics performance well beyond the limits of traditional scaling". Key to the ERI will hopefully be new collaborations among the commercial electronics community, defense industrial base, university researchers, and the DoD. The DoD proposed FY 2018 budget reportedly includes a $75 million allocation for DARPA in support of this, initiative. It is reported that in total we are looking at a $200,000MM program.



The program will focus on the development of new materials for devices, new architectures for integrating those devices into circuits, and software and hardware designs for using these circuits. The program seeks to achieve continued improvements in electronics performance without the benefit of traditional scaling. Bill Chappell, director of DARPA's Microsystems Technology Office (MTO), which will lead the program, announced "For nearly seventy years, the United States has enjoyed the economic and security advantages that have come from national leadership in electronics innovation…..If we want to remain out front, we need to foment an electronics revolution that does not depend on traditional methods of achieving progress. That's the point of this new initiative – to embrace progress through circuit specialization and to wrangle the complexity of the next phase of advances, which will have broad implications on both commercial and national defense interests."He continued "We need to break away from tradition and embrace the kinds of innovations that the new initiative is all about…"

The chip research effort will complement the recently created Joint University Microelectronics Program (JUMP), an electronics research effort co-funded by DARPA and SRC (Semiconductor Research Corporation). Among the chip makers contributing to JUMP are IBM, Intel Corp., Micron Technology and Taiwan Semiconductor Manufacturing Co. SRC members and DARPA are expected to kick in more than $150 million for the five-year project. Focus areas include high-frequency sensor networks, distributed and cognitive computing along with intelligent memory and storage.

The materials portion of the ERI initiative will explore the use of unconventional materials to increase circuit performance without requiring smaller transistors. Although silicon is used for most of the circuits manufactured today, other materials like GaAs, GaN and SiC have made significant inroads into high performance circuits. It is hoped that the initiative will uncover other elements from the Periodic Table that can provide candidate materials for next-generation logic and memory components. One research focus will be to integrate different semiconductor materials on individual chips, and vertical (3D) rather than planar integration of microsystem components.

The architecture portion of the initiative will examine circuit structures such as Graphics processing units (GPUs), which underlie much of the ongoing progress in machine learning, have already demonstrated the performance improvement derived from specialized hardware architectures. The initiative will explore other opportunities, such as "reconfigurable physical structures that adjust to the needs of the software they support".

The design portion of the initiative will focus on developing tools for rapidly designing specialized circuits. Although DARPA has consistently invested in these application-specific integrated circuits (ASICs) for military use, ASICs can be costly and time-consuming to develop. New design tools and an open-source design paradigm could be transformative, enabling innovators to rapidly and cheaply create specialized circuits for a range of commercial applications.

As part of this overall Electronics Resurgence Initiative, DARPA had their kick of meeting for the CHIPS program (Common Heterogeneous Integration and Intellectual Property (IP) Reuse). The CHIPS vision is an ecosystem of discrete modular, IP blocks, which can be assembled into a system using existing and emerging integration technologies. Modularity and reusability of such IP blocks will require electrical and physical interface standards to be widely adopted by the community supporting the CHIPS ecosystem. The CHIPS program hopes to develop the design tools and integration standards required for modular integrated circuit (IC) designs.

Program contractors include Intel, Micron, Cadence, Lockheed Martin, Northrop Grumman, Boeing, Synopsys, Intrinsix Corp., and Jariet Technologies, U. Michigan, Georgia Tech, and North Carolina State. ◆

Packaging

IBM's Khare on A.I.

PETE SINGER,
Editor-in-Chief

Mukesh Khare, VP of IBM Research, talked about the impact artificial intelligence (AI) is going to have on the semiconductor industry during a recent panel session hosted by Applied Materials. He said that today most artificial intelligence is too complex. It requires, training, building models and then doing inferencing using those models. "The reason there is good in artificial intelligence is because of the exponential increase in data, and cheap compute. But, keep in mind that, the compute that we are using right now is the old compute. That compute was built to do spreadsheet, databases, the traditional compute.

"Since that compute is cheap and available, we are making use of it. Even with the cheap and available compute in cloud, it takes months to generate those models. So right now, most of the training is still being done in cloud. Whereas, inferencing, making use from that model is done at the edge. However, going forward, it is not possible because the devices at the edge are continuously generating so much data that you cannot send all the data back to the cloud, generate models, and come back on the edge.

"Eventually, a lot of training needs to move to the edge as well," Khare said. This will require some innovation so that the compute, which is being done right now in cloud, can be transferred over to edge with low-power devices, cheap devices. Applied Materials' CIO Jay Kerley added that innovation has to happen not only at the edge, but in the data center and at the network layer, as well as in the software frameworks. "Not only the AI frameworks, but what's driving compression, de-duplication at the storage layer is absolutely critical as well," he said.

Khare also weighed in on how transistors and memory will need to evolve to meet the demands of new AI computer architectures, "For artificial intelligence in our world, we have to think very differently. This is an inflection, but this is the kind of inflection that world has not seen for last 60 years." He said the world has gone from tabulating system era (1900 to 1940) to the programmable system era in 1950s, which we are still using. "We are entering the era of what we call cognitive computing, which we believe started in 2011, when IBM first demonstrated artificial intelligence through our Watson System, which played Jeopardy," he said.

Khare said "we are still using the technology of programmable systems, such as logic, memory, the traditional way of thinking, and applying it to AI, because that's the best we've got."

AI needs more innovation at all levels, Khare said. "You have to think about systems level optimization, chip design level optimization, device level optimization, and eventually materials level optimization," he said. "The artificial workloads that are coming out are very different. They do not require the traditional way of thinking — they require the way the brain thinks. These are the brain inspired systems that will start to evolve."

Khare believes analog compute might hold the answer. "Analog compute is where compute started many, many years ago. It was never adopted because the precision was not high enough, so there were a lot of errors. But the brain doesn't think in 32 bits, our brain thinks analog, right? So we have to bring those technologies to the forefront," he said. "In research at IBM we can see that there could be several orders of magnitude reduction in power, or improvement in efficiency that's possible by introducing some of those concepts, which are more brain inspired."

Christos Georgiopoulos (former Intel VP and professor who was also on the panel) said a new compute model is required for A.I. "It's important to understand that the traditional workloads that we all knew and loved for the last forty years, don't apply with A.I. They are completely new workloads that require very different type of capabilities from the machines that you build," he said. "With these new kind of workloads, you're going to require not only new architectures, you're going to require new system level design. And you're going to require new capabilities like frameworks. He said TensorFlow, which is an open-source software library for machine intelligence originally developed by researchers and engineers working on the Google Brain Team, seems to be the biggest framework right now. "Google made it public for only one very good reason. The TPU that they have created runs TensorFlow better than any other hardware around. Well, guess what? If you write something on TensorFlow, you want to go to the Google backend to run it, because you know you're going to get great results. These kind of architectures are getting created right now that we're going to see a lot more of," he said. ◆

Semiconductors

Reveal previously invisible defects and contaminants in advanced packaging applications

GURVINDER SINGH, *Director, Product Management, Rudolph Technologies, Inc., Wilmington, MA*

A new illumination technology compares favorably to conventional bright field illumination.

A new optical technique can reveal defects and contaminants that escape conventional inspection technologies in many advanced packaging applications. As wafer level packaging (WLP), and especially fan-out wafer and panel level packaging (FOWLP/FOPLP), gains broader acceptance, certain classes of defects that are characteristic of these processes present significant challenges to standard optical inspection tools. A new optical technology demonstrates increased sensitivity to transparent defects, such as residual dielectric films and photoresist, which are only marginally visible with conventional tools. At the same time, it is less sensitive to nuisance defects, such as those caused by the varying contrast and texture of grains in metal films, that should correctly be ignored.

Challenges in advanced packaging applications

Advanced packaging processes often involve the use of front-end-like technologies in back-end applications. Fan-out packaging is no exception, and, not surprisingly, it is following a similar development path, with increasing circuit complexity accompanied by shrinking circuit geometries. Redistribution layer (RDL) line widths, which were around 20µm in early implementations, will soon reach 2µm and are unlikely to stop there. Just as front-end processes placed increasing emphasis on enhanced process monitoring and control, advanced packaging processes will be forced to include more and better inspection and metrology capability at critical steps to maintain control and improve yields.

Advanced packaging processes, such as fan-out, face unique challenges that, for inspection systems, result in overcounting nuisance defects and undercounting yield-robbing critical defects. These advanced packaging techniques make extensive use of metal and organic polymers. Layers of metal are used to define conductive paths and organic polymer dielectric

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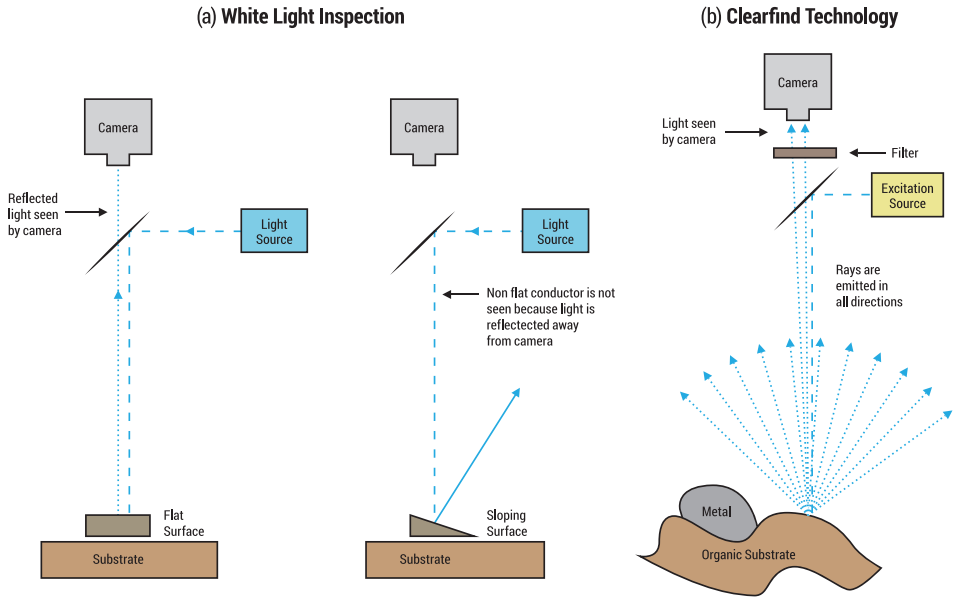

FIGURE 1. Simplified illustrations of the differences between traditional white light inspection systems (a) and CF technology (b).

materials are used to provide insulation between conductors and planar surfaces between the layers. Dark field and bright field inspection results often include tens of thousands of nuisance defects. These occur because the inspection algorithms are designed to find random aberrations in highly repeatable patterns and the variable grain patterns of metal conductors appear as defects when are not. If not excluded, their large numbers can quickly overwhelm the real defects. Metal grain features can be as large as 50µm, much larger than RDL lines, which are currently as small as 2µm, and likely to reach 1µm in the near future.

Another class of defects that has proven difficult for conventional optical inspection techniques is caused by the presence of organic residues left after etching and descumming operations. They are hard to find because these materials tend to be transparent at visible wavelengths, yielding little signal in bright field and dark field inspection. They can be especially troublesome when they occur on contacts such as bumps and pillars. The new illumination method effectively eliminates nuisance noise from metal surface textures and enhances signal strength from organic defects.

Clearfind™ technology

The results presented here were all acquired using a Firefly™ inspection system (Rudolph Technologies) that incorporates the new Clearfind (CF) illumination technology[1]. The new method takes advantage of the fact that many organic polymers exhibit distinctive optical properties that are not present in metals, silicon or other common inorganic materials used in semiconductor manufacturing. These properties tend to be unique to organic molecules displaying a high degree of conjugation, such as polycyclic aromatic hydrocarbons, and in linear or branched chain organic polymers with multiple regularly interspersed pi-bonds. This phenomenon results in the generation of a readily detectable, high color-contrast signal when the feature is appropriately illuminated against a metallic or other inorganic surface. The emission tends to be anisotropic and therefore less sensitive to surface topography that could potentially direct most ordinary bright field or dark field reflected light away from the detector. This results in increased sensitivity to organic residues and reduced sensitivity to interference from surrounding features. The method has the additional advantage of being relatively insensitive to signal variations caused by metal grains. **FIGURE 1** presents a simplified illustration comparing the new technology to traditional white light inspection.

The light source for the new technology is laser based, rather than the broadband source typically used in white light inspection systems. Thus, the light output is more stable in terms of both spectral range and output power. Autofocusing of the samples is accomplished using a patented high speed, near infrared-based laser triangulation system that maintains a constant distance between the imaging optics and the area being scanned. Images are acquired at high speed with a high-resolution camera. The result images compared in this article using bright

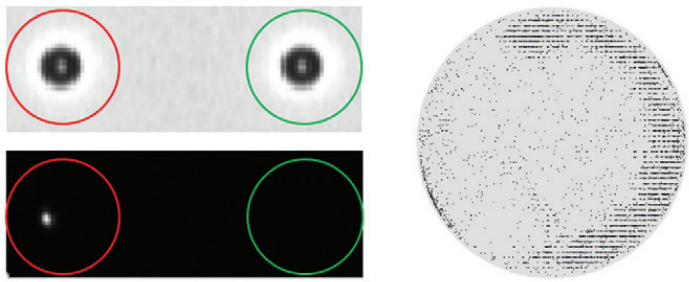

FIGURE 2. (a) (Upper set) in this pair of bright field images the TSV nails look the same. (Lower set) In this pair of CF technology images the residue is clearly visible in the left nail. (b) A full wafer map showing the concentration of defects toward the right edge of the wafer.

field, dark field and CF technology were all acquired on the same inspection platform using different illumination techniques.

Through Silicon Via (TSV)

The sample is a 300mm silicon wafer with revealed TSV pillars[2]. TSV nail diameter is about 8µm and the distance between TSVs is about 56µm. The TSVs are on the backside of the wafer and the front side of the wafer is attached to a carrier.

In **FIGURE 2a**, the top shows a bright field image of two TSVs. The TSV on the left, circled in red, is covered with unetched organic residue and the TSV on the right, circled in green, is completely exposed. In the bright field image both TSVs look good and the residue is not visible. The images at the bottom left of figure 2 were acquired with CF technology and show the same TSVs. The TSV on the left, circled in red, has a bright blob while the one on the right, circled in green, is completely dark. The organic residue remaining on the left TSV now emits a readily detectable signal.

FIGURE 2b shows the inspection result from the full TSV wafer. The dots on the wafer map represent defect locations. There is a heavy concentration of organic residue on TSVs on the right side of the wafer. Metal pads approximately 35µm in diameter will be placed on top of the TSVs. Any organic residue between the TSV and the pad can cause deplanarization, which may result in connectivity issues when the die is stacked together. In addition, organic residue can increase the resistance of the contact when the die is stacked. If the defects are found before the next process step the wafer can be reworked.

Under Bump Metal (UBM)

The sample is a 300mm wafer with RDL and under bump metallization (UBM). The UBM pads are about 50µm wide. In **FIGURE 3a**, the bright field image of two UBM pads shows the left pad is completely exposed and the right pad is covered with unetched organic film. However, the film is transparent and both pads look good in this image. Note the random metal texture visible in the bright field image, which adds noise and makes sensitive inspection for small defects more difficult. The image at lower left, acquired with CF technology, shows the same pads. The left pad, with no residue, appears black. The right pad, covered by residue, is significantly brighter. Also note that the metal texture seen in the bright field image with absent in CF illumination, permitting sensitive inspection for defects down to the pixel level.

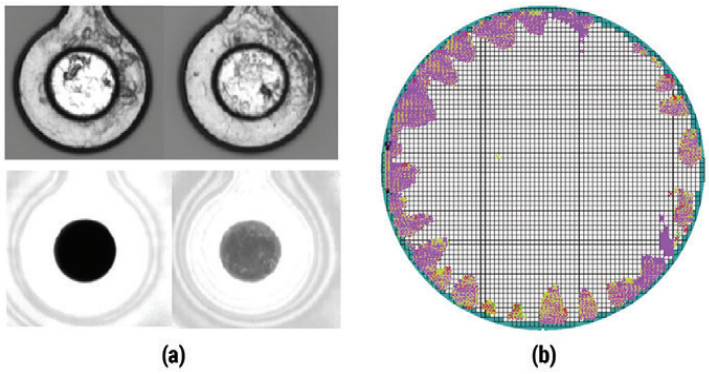

FIGURE 3. (a) UBM pads – In each pair the left pad is clear and the right pad is covered by an organic residue. In the bright field images (upper set) the two pads look the same and the graininess of the metal is clearly visible. In the CF images (lower set) the clear pad on the left is dark while the covered pad to the right is brighter. (b) The wafer map shows the distribution of defects concentrated near the wafer edges.

FIGURE 3b shows a map of the full wafer where there is a heavy concentration of defects on UBM pads near the edge of the wafer. As in the TSV example, residue remaining on the UBM pads can cause increased resistance or loss of connectivity to a bump deposited on the pad. Bumps deposited on the residue are higher than normal bumps,

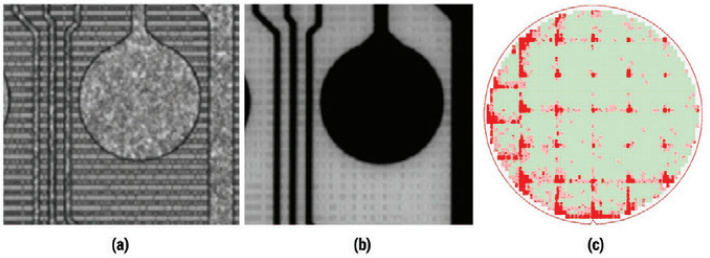

Figure 4. (a) bright field image shows considerable metal graininess, making it difficult to distinguish top layer metal from underlying metal visible through an interposed transparent layer. The metal graininess interferes with the detection of small defects. (b) CF technology suppressed the graininess in both the top layer metal and underlying metal layers, and there is good contrast between the top metal features and the transparent organic layer. (c) The full wafer map reveals a rectangular pattern that corresponds to the photolithography reticle.

leading to loss of coplanarity and connectivity issues. If the problem is found before starting the bump process, the wafer can be reworked and the residues removed.

Redistribution Layer (RDL)

The sample is a 300mm molding compound wafer for fan-out packaging. **FIGURE 4a** shows a bright field image that includes a UBM pad and several RDL lines. The middle image shows the same area viewed with the new illumination technology. In the bright field image, the metal of the UBM pad and the RDL lines is very similar to the underlying metal visible through an interposed transparent film. The texture and graininess of the metals add noise to the image, increasing the difficulty of detecting small defects. Inspection with bright field illumination resulted in high nuisance defect counts without finding real process issues on the wafer. In **FIGURE 4b**, the top surface metal features, RDL and UBM, stand out against the background of the transparent film, while the underlying metal features are barely visible. **FIGURE 4c** shows a full wafer map acquired using CF technology and reveals a rectangular pattern that corresponds to the reticle of the lithography tool. The rectangular pattern was not visible in the bright field wafer map.

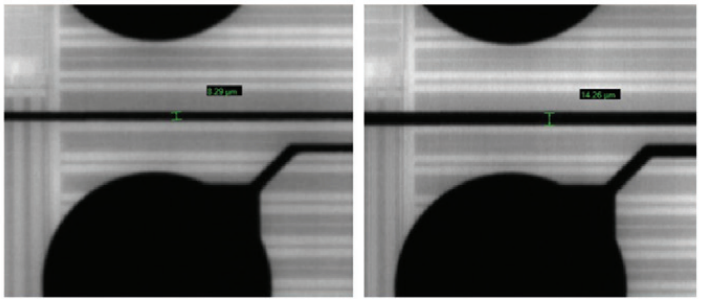

FIGURE 5. Further inspection with the new technology revealed thinned RDL lines (left) near the lower left corner of the reticle. The thinning was not detectable with bright field inspection.

FIGURE 5 shows additional RDL inspection results on the same wafer. CF technology revealed thinner lines toward the lower left corner of the reticle pattern. Ultimately, it was determined that these thinner lines were caused by a defect in the condenser lens of the lithography tool. The improved contrast between the first layer metal features in the underlying organic film, and the reduced noise, permitted more accurate and sensitive measurements using the new illumination technology. A bright field inspection of 20 wafers containing the same defect did not detect any thinner lines.

Photoresist

The sample is a 300mm patterned silicon wafer from a large memory manufacturer[3]. It contains die approxi-

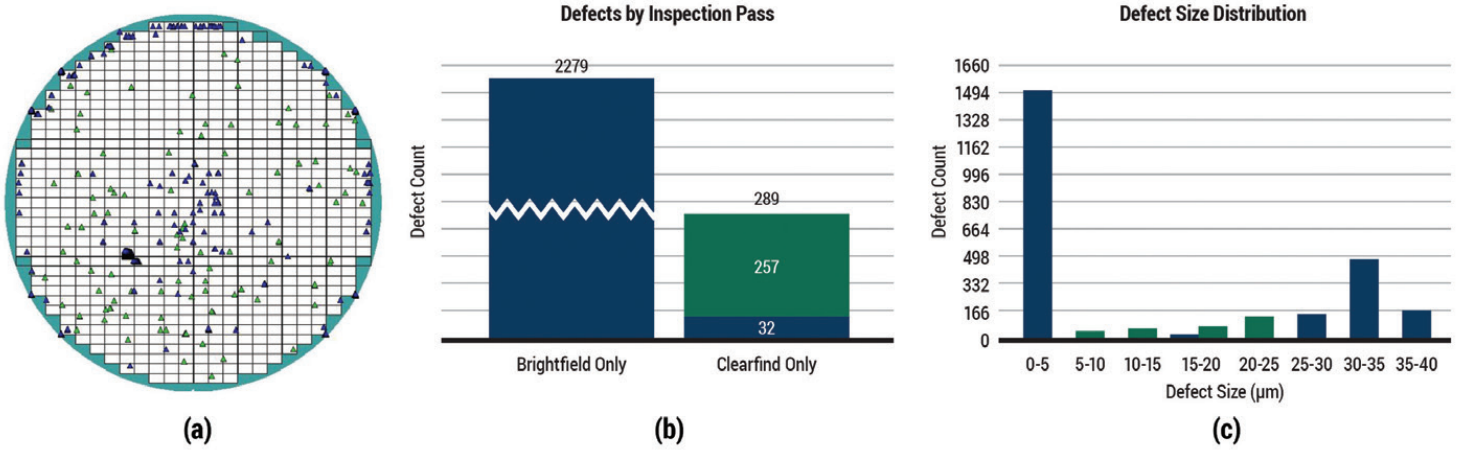

FIGURE 6. (a) A full wafer map shows defects detected by bright field (blue triangles) and CF technology (green triangles). (b) The bar graph shows the overlap between bright field defects and CF defects. (c) The bar graph shows the size distribution of the defects detected by each type of illumination.

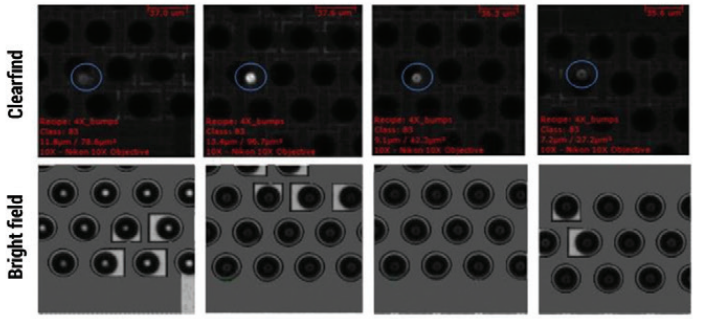

FIGURE 7. Comparing CFCF technology results (upper) and bright field results of the same defects.

mately 11.7mm x 7.6mm in size, and containing arrays of about 9,000 metal pillars, each pillar approximately 22µm in diameter. The customer was interested to know if the new illumination technology would find defects not found by bright field inspection. **FIGURE 6a** shows a wafer map overlaying bright field defects (blue triangles) and CF defects (green triangles). In both cases the defects appear to be randomly distributed and not clustered. As depicted by the bar chart in **FIGURE 6b**, bright field illumination found 2,279 defects compared to 289 defects found by CF technology. Most interestingly, only 32 of the defects found by CF technology were also found with bright field inspection. 257 defects would have been missed by bright field inspection. The bar chart (**FIGURE 6c**) shows the size distribution of defects discovered by both techniques. Bright field inspection found a very large number of small defects (less than 5µm) and more defects larger than 25µm. Defects found by the CF technology were between 5-25µm in size.

FIGURE 7 compares CF technology results (top) and bright field results (bottom). Each vertical pair shows a defect missed by bright field inspection and detected by CF technology. The enhanced brightness and circular shape of the defects detected by the new method strongly imply that they are associated with polymer residues. The enhanced brightness of the defects against the very black background is a unique and valuable feature of CF technology. Overall, these results demonstrate the value of supplementing bright field inspection with CF technology. All of the defects found by CF technology were of sufficient size to impact yield.

Conclusion

Results shown here demonstrate the benefits of imaging with the new CF illumination technology when compared to conventional bright field illumination. The new technology allows detection of transparent organic residues that are not visible with bright field illumination. It was also shown to detect types and sizes of defects that were not detected by bright field inspection. Equally important, its ability to reduce noise caused by metal texture and graininess significantly improves its sensitivity to small defects on metal features and dramatically reduces the detection of nuisance defects.

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Solutions for controlling resin bleed out

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The hows and whys of resin bleed-out (RBO) are discussed, as well as the impact it makes and how to control it.

Die attach pastes, which consist of resin, curing agent, catalyst, filler and additives, have been extensively used to attach die onto lead frames in various electronic packages such as small outline integrated circuit (SOIC), thin-shrink small outline package (TSSOP), quad flat package (QFP) and quad-flat no-lead (QFN). One of the issues commonly encountered during package assembly is resin bleed-out (RBO), or epoxy bleed out (EBO). RBO is the separation of some formulation ingredients in the paste from the bulk paste (see **FIGURE 1**). Depending on die attach paste formulations and lead frame surface chemistry and morphology, bleeding ingredients can be solvents, reactive diluents, low-molecular-weight resins, catalysts, and additives like adhesion promoter. Resin bleed out tends to occur on high energy surfaces such as metal lead frames without any organic coating. In particular, if plasma cleaning is utilized to remove the contaminants prior to assembly, the bleeding issue may become more pronounced due to the increase in surface energy. Bleed-out can occur once die attach pastes are dispensed on to lead frames or during thermal curing. As microelectronics continue to move towards smaller form factor, higher reliability and higher performance, control of RBO becomes increasingly critical for packages where there is a very little clearance between die and die pad edge, or between one die and another in multi-chip modules (MCMs).

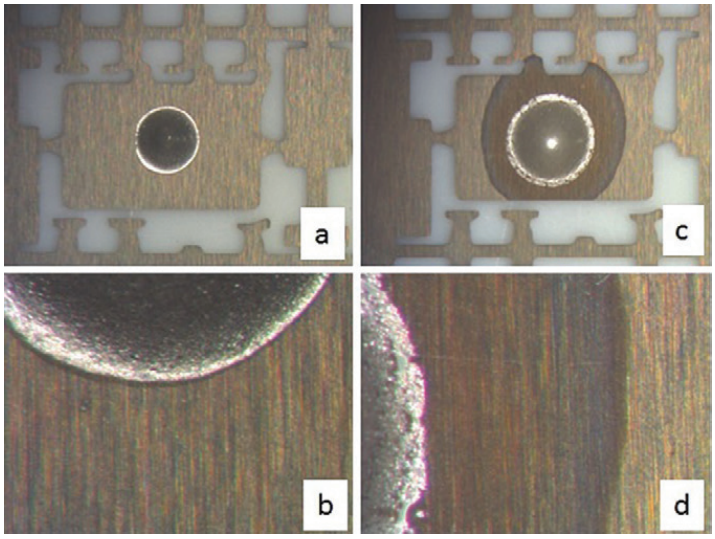

FIGURE 1. Examples of RBO: (a) Minor RBO of die attach paste 1 on a metal lead frame, (b) enlarged image of (a); (c) Severe RBO of die attach paste 2 on a metal lead frame, (d) enlarged image of (c).

How resin bleed-out occurs

When die attach paste is dispensed onto a solid surface like lead frame surface, the paste will typically wet the surface partially. The adhesive force between die attach paste and lead frame surface causes the paste to spread while the cohesive force within the bulk paste will hold the ingredients together and avoid contact with a lead frame surface. The adhesive and cohesive forces are the intermolecular forces such as hydrogen bonding and Van der Waals forces. So the degree of wetting will depend on the balance between adhesive force and cohesive force. Bleed-out occurs when the adhesive force of some formulation ingredients to the substrate is stronger than the cohesive force within the paste. The driving force for bleed out is to minimize the surface energy of the substrate by wetting.

Impact of resin bleed-out

Resin bleed-out can cause several issues if it is not well controlled.

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- If the formulation ingredients bleed from the periphery of the die attach pastes and covers the wire bonding area, then issues like non-stick on pad (NSOP) and weak wire bond can occur. It can also be an issue if bleeding occurs from the die attach fillet along die edge to the die top, contaminating the bond pad on die top surface [1].

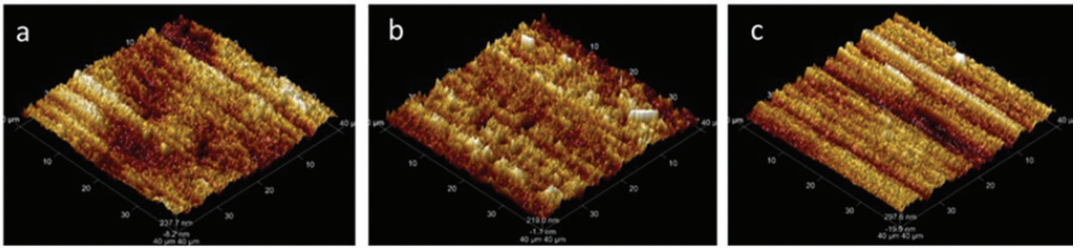

FIGURE 3. AFM images of (a) LF1, (b) LF2 and (c) LF3

- Resin bleed-out may affect the adhesion of mold compound to die pad or mold compound to die top surface, both of which can lead to delamination. In particular, die top delamination is strictly not allowed in wire-bonded packages because it can cause the ball bond to be mechanically lifted, thereby leading to electrical failures during temperature cycling [2].

- As the formulation ingredients bleed out of the bulk paste, the composition of die attach paste under die may change accordingly. This can impact the adhesion of die attach to lead frame adversely, leading to an adhesive failure [3].

Influence of surface roughness

There are many factors that can cause resin bleed-out, such as low surface tension of die attach pastes, high surface energy of metal lead frames, surface contamination, surface porosity and surface roughness. Here we will focus on the impact of surface roughness, which is critical to achieve high package reliability. Two die attach pastes were dispensed onto three lead frames with different surface roughness. The surface roughness of these three lead frames was characterized by Atomic Force Microscopy (AFM) using the roughness average (Ra) and the roughness ratio (r) (**FIGURE 2**). The roughness average (Ra) represents the arithmetic average of the deviations from the center plane. The roughness ratio is the ratio between the actual 3-D surface area calculated by AFM and the flat surface. The 3D morphologies of lead

frames are shown in **FIGURE 3**. It was found that (a) there is a good correlation between the roughness ratio and resin bleed-out. As the surface roughness ratio increases, the bleeding becomes increasingly worse; (b) LF1 and LF2 have almost same Ra, but the bleeding performance of DA3 and DA4 are different. This indicates that the roughness average is not a good index for RBO; (c) DA4 is more resistant to bleed out than DA3.

The relationship between surface roughness and the wettability has been described by Young equation (Equ. 1) and Wenzel equation (Equ. 2).

$$\cos Øy=(YS-YSL)/YL \quad (1)Ø$$
$$\cos öm=r\cos Øy \quad (2)$$

Where Ys, YL, YSL are surface tensions of the solid, liquid and interfacial tension between die attach paste and lead frame, respectively; Øy is the Young contact angle, Øm is the measured contact angle, and r is the roughness ratio. As the surface roughness increases, the better the wetting, and the worse the bleed-out if the contact angle is < 90o [4]. This is the case for die attach paste on a metal surface without anti-EBO coating.

Approaches to control resin bleed out

There are several approaches to control or eliminate resin bleed-out. These approaches include modifying formulation by selecting appropriate anti-EBO, using die attach film (DAF)/B-stage epoxy, controlling surface roughness, creating mechanical barrier, and lowering the surface energy of lead frames by surface coating.

- Modifying formulations. Generally, anti-bleeding agents are added to die attach pastes to reduce or eliminate RBO. Different anti-bleeding agents may have different working mechanisms. Some anti-bleeding agents are added to enhance the cohesiveness of the pastes while others are added to form a thin layer with a surface energy lower than the pastes themselves on a lead frame surface [5]. Therefore, tailoring die attach adhesives with appropriate anti-bleeding agents is critical to prevent RBO on different types of lead frames, while maintaining high adhesion to metal lead frames to achieve high reliability.

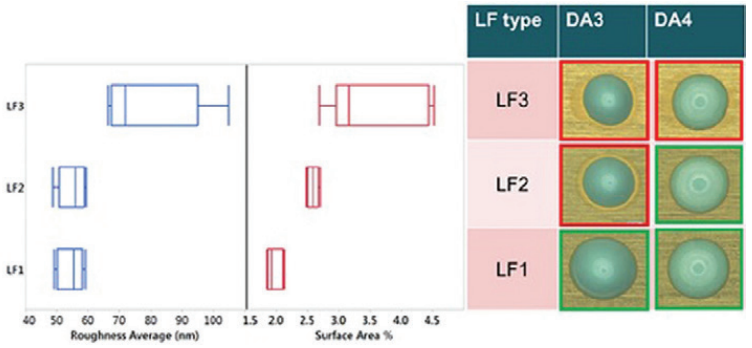

FIGURE 2. The correlation of surface roughness with resin bleed-out. Roughness ratio r = 1 + surface area%.

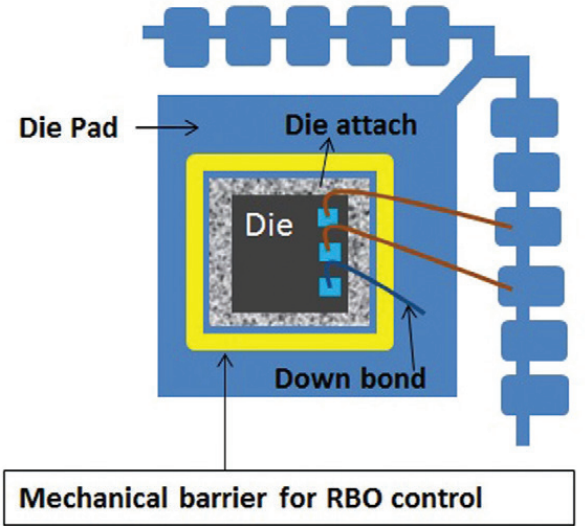

FIGURE 4. Mechanical barriers for controlling resin bleed-out. Mechanical barriers can be grooves on lead frames or low surface energy barrier materials printed on lead frames.

- Die Attach Film/B-stage Epoxy. The simplest and most effective way to eliminate RBO is to use die attach films or B-stage materials. However, there are limitations associated with this approach. These can include high material cost and capital investment, difficulty to achieve high adhesion and thus high reliability, and limited thermal performance of these materials.

Mechanical barriers. In some cases, grooves on lead frames are designed in between die attach area and wire bond area to reduce resin bleed-out, as shown in **FIGURE 4**. This is a simple and cost-effective process. However, this approach may not work well if the bleeding is severe. Similarly, some low surface energy insulating film around a chip can be printed to confine the un-cure pastes to the space defined by the printed pattern [5].

- Vacuum baking. Vacuum baking of ceramic substrates with gold or other metal surfaces has been reported to reduce bleed-out. Several mechanisms were proposed: (a) through removal of polar surface contaminant, which promotes bleed-out of lighter organic resin by dipole attraction or chemical reaction [6]; (b) through reducing the surface energy of the plating surface by the formation of Ni2O3 [7]; (c) through producing a coating of hydrocarbon by oil back streaming to

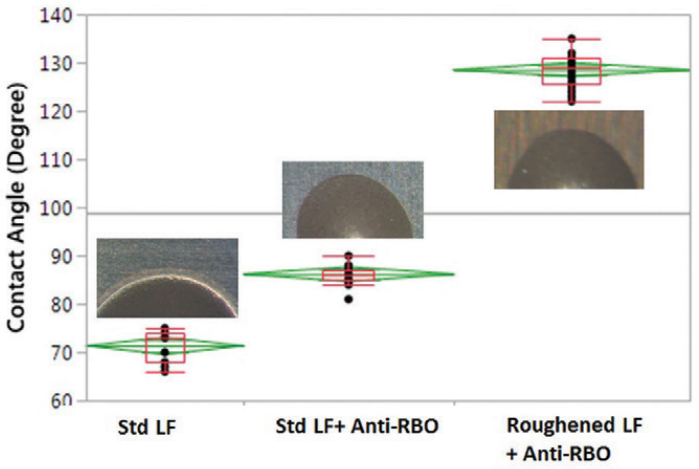

FIGURE 5. Water contact angle on three types of lead frames. Images are a die attach paste dispensed on these three types of lead frames.

reduce the surface energy [8]. The method is not recommended either due to lack of controllability or due to the detrimental effect on wire bonding quality [7]. A more controlled method to reduce or eliminate RBO is to treat the surface with known chemicals and controlled processes, as discussed below.

- Low surface energy coating. Roughened lead frames have been utilized to enhance package reliability, particularly to meet Automotive Grade 0 requirements or beyond, as they increase surface contact area and enhance mechanical interlocking. As shown in Fig. 2, a small increase in roughness can result in a severe bleed-out. Therefore, increasing surface roughness will promote bleed-out if there is no anti-EBO on the surface. According to Young's equation, decreasing surface energy will increase the contact angle, i.e. decreasing the wetting of the surface. Therefore, in roughened lead frame manufacturing, a solution of low surface energy material is used to treat roughened lead frames to lower their surface energy to reduce or eliminate RBO. Alternatively, a thin layer of film can be deposited onto the assembly surface by gas plasma technology to modify the surface energy [9]. **FIGURE 5** shows water contact angles of lead frames with or without anti-EBO treatment. The anti-EBO coating will increase the contact angle on standard lead frame as explained by Young's equation. Compared with standard lead frames, roughened lead frames have an increasing roughness and the anti-EBO coating on roughened lead frames further increases contact angle significantly. This can be explained by Wenzel equation, which demonstrates that adding surface roughness will increase surface hydrophobicity if the surface is chemically hydrophobic. In addition, Fig. 5 shows the resin bleed-out performances of a die attach paste (DA2) on these three types of lead frames. Bleed out was observed on the standard lead frame without anti-EBO, but there was no bleeding on both standard and roughened lead frame with anti-EBO coating. The low surface energy anti-EBO coating eliminates resin bleed out.

Summary

This article provides an understanding of how bleeding occurs, the impact of bleeding, and methods to control bleeding. Bleeding is the result of the interaction between die attach pastes and metal lead frames. In particular, we studied the influence of surface roughness on RBO of different die attach materials, and found that there is a good correlation between the roughness ratio and bleed-out performance. Reducing the surface roughness will reduce or eliminate RBO. It is noteworthy that there is a line between reducing roughness to achieve no RBO and increasing roughness to ensure excellent delamination performance for lead frames without Anti-EBO. In terms of die attach pastes, the most effective way to control RBO seems to be the surface coating with anti-RBO without affecting other performances like delamination, or combining this method with others to provide an even better solution.

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How to build CMP models for hotspot detection

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CMP modeling has become a powerful tool for both process engineers and chip designers.

Over the last two decades, chemical mechanical polishing (CMP) has become a mainstay in the IC manufacturing process. Foundries employ it to remove excess materials from silicon wafers and to smooth wafer layers, such as front-end-of-line (FEOL) layers like shallow trench isolation (STI) and back-end-of-line (BEOL) layers like metal interconnect. As one might expect, with the introduction of each new process, CMP has become exponentially more sophisticated, and employed with greater frequency. And the process is not without risks—CMP can create new defects through over- and under-polishing.

What's perhaps not so widely understood is that the root cause of many CMP issues actually originates in design-specific layout issues that can be corrected before manufacturing by the use of dummy fill, slotting, or simply the redesign of some cells. To address these CMP hotspot issues proactively, you first need an accurate CMP model and analysis method to find hotspots in your design that are likely to pose problems during CMP, and then you need to employ the appropriate methods to fix those problems.

Let's take a look at how to build CMP models for CMP simulation, run analysis, and perform hotspot detection.

CMP modeling

Due to the complex nature of today's CMP process, creating an accurate CMP model that takes into account the complicated chemical and mechanical mechanisms of polishing is a multi-faceted challenge. Current CMP modeling includes modeling of the polishing processes and numerous deposition and etch processes, including copper (Cu) electrochemical deposition (ECD), chemical vapor deposition (CVD), high-density plasma (HDP) CVD, spin-on dielectric (SOD), and etchback.

The basic concept of CMP modeling is to extract geometrical properties of the patterns on the layout, and predict post-polishing thickness variation for each pattern dependent on its position on the chip. To begin, a full chip is divided by windows of fixed size. For each window, geometric characteristics of a pattern in the window are extracted and used for simulation, as shown in **FIGURE 1**.

Pattern density is defined as the ratio of total area of polygons in a window divided by the area of the window. Numerous studies show that pattern density, combined with the width of polygons, the space between them, and the perimeter of polygons, plays a critical role in characterizing the results of the polishing process.

After Cu ECD, the surface profile of BEOL metal layers is very non-planar, with numerous bumps and valleys. Because large bumps have a strong impact on polishing

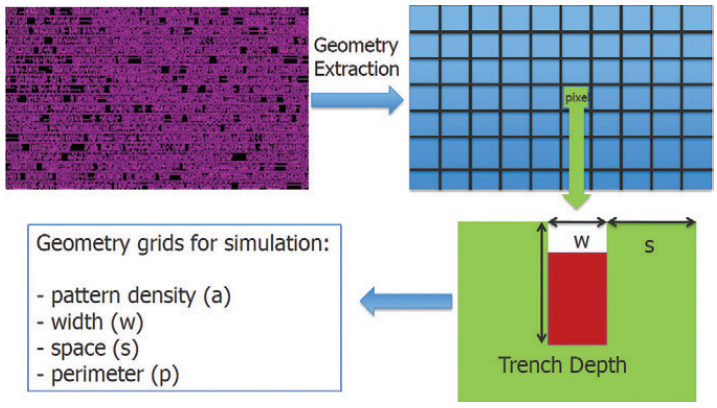

FIGURE 1. Geometry data extraction from a layout.

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results, and may delay barrier layer opening under the bumps and nearby areas, modeling of the post-ECD surface profile is critical to ensuring high-accuracy CMP modeling. Non-planar surface profiles are also typical for FEOL layers after isotropic oxide layer (TEOS) deposition, HDP-CVD, SOD, flowable CVD, and other processes.

The CMP model must not only simulate polishing results for multiple materials due to the patterns' geometry specifics, but also capture long-range polishing effects specific to a given CMP process. For example, it is well-established that pad pressure and bending, which lead to pressure redistribution within die and wafer, are mainly responsible for long-range effects in CMP, so the model must account for these factors.

CMP test chips and measurements

A key step in CMP model building is the calibration of deposition and CMP planarity models with measurement data collected from test chips. This allows you to select the best model parameters that truly reproduce process conditions at your targeted foundry. After deposition and polishing steps, measurements are collected via line scans, cross-section images, and a measurement data table is filled with erosion, dishing, and thickness data. Layer stack information, deposited layers thicknesses, and CMP process conditions are used to fill the recipe file of a process. Using the recipe file and measurement data table, model parameters are calibrated. **FIGURE 2** illustrates the CMP model building flow.

Because test chips play such a critical role in accurate CMP modeling, test chip design must take into account long-range effects of the CMP process, the ability to collect

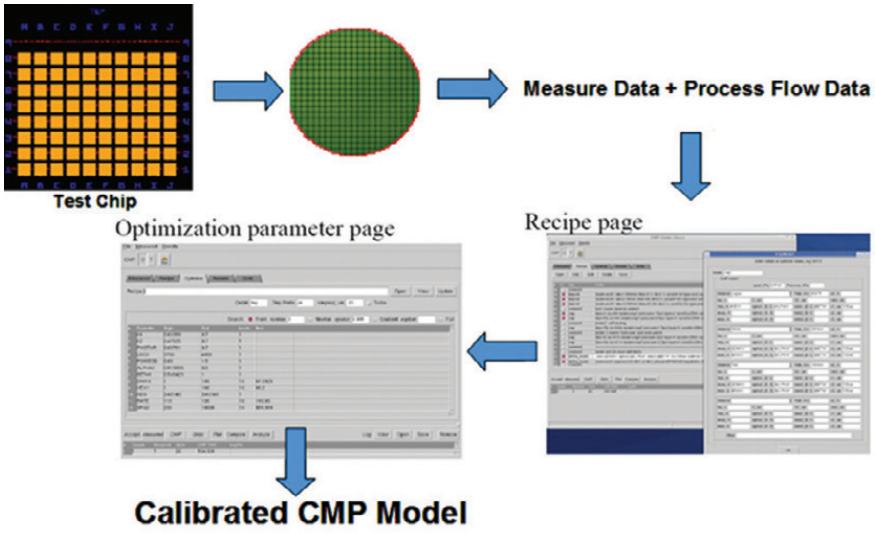

FIGURE 2. CMP model building flow.

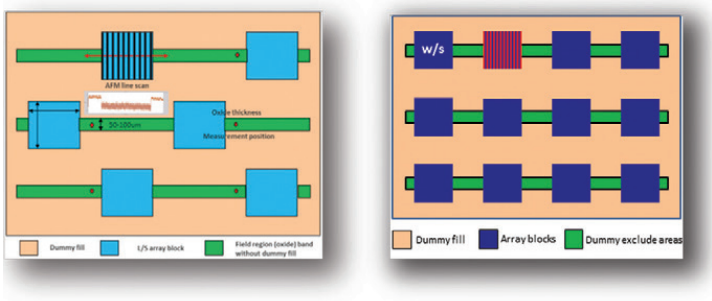

FIGURE 2. CMP model building flow.

high-quality measurements, and multi-layer stacking of test pattern structures for FEOL and some BEOL layers in a way that minimizes multi-layer effects. The size of a test chip and the number of structures must be selected in a way that provides good coverage of width, space, perimeter, and pattern density values supported by the technology node, without violating design rule checking (DRC) constraints.

For BEOL metal layers, a CMP test chip usually consists of periodically-placed array blocks of parallel trenches of different widths with differing spaces between them. Spaces between test patterns should be large enough to avoid pattern interactions due to CMP long-range effects. Process conditions usually require dummy fill between array blocks. To get high-quality line scan data, dummy exclude areas should be reserved between array blocks. **FIGURE 3** shows examples of two CMP test chip layouts.

For CMP model building, an atomic force microscope (AFM) scanner or other profiler tool is often used to collect erosion and dishing data from the line scans over these test patterns (**FIGURE 4**).

Normally, transmission electron microscopy (TEM) or scanning electron microscopy (SEM) cross-section images are used to obtain oxide, nitride, or metal thickness values. To avoid multi-layer stacking effects, either part of a layer or all of the layer may be covered by dummy fill to prevent the effect of surface profile variation of the underlying layer on test patterns at higher layers.

FEOL CMP modeling

Design of CMP test chips is more challenging for FEOL layers. The restrictive design rules of advanced technology nodes don't support long parallel trenches. Instead, short array lines of similarly-oriented rectangles separated by a variety of spacing values in both the horizontal

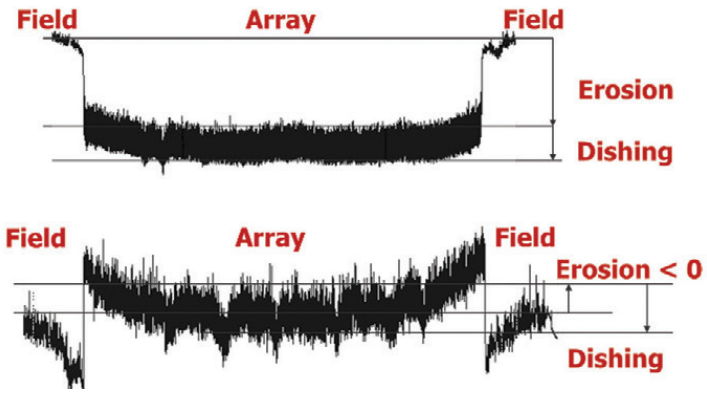

FIGURE 4. Erosion and dishing data from line scans.

and vertical directions, known as islands, are used in test pattern blocks. This layout poses a challenge for scanner positioning and data collection, because the scanner may pass between the rectangles and fail to collect the oxide-to-nitride transition height difference. To minimize this possibility, the space between rectangles that is orthogonal to the scanner direction is set to the minimal possible value, and the space in the scanner direction is varied (**FIGURE 5**). Also, a scanner will make two or three passes over test patterns, with each pass separated by some distance from the others, and the most appropriate scan line data can then be selected for modeling.

High-K metal gate

The specifics of HKMG and Al RMG technology require that test chip patterns of POP and Al RMG be the inverse of each other. At POP, the sacrificial polysilicon (poly) layer is removed, and the Al layer is deposited and polished. The inverse (or negative) of the poly layer is used for oxide deposition and polishing at POP step modeling. For Al RMG, the poly layer is used. Sufficient test wafers must be reserved and processed to collect the required measurements for POP and Al RMG steps.

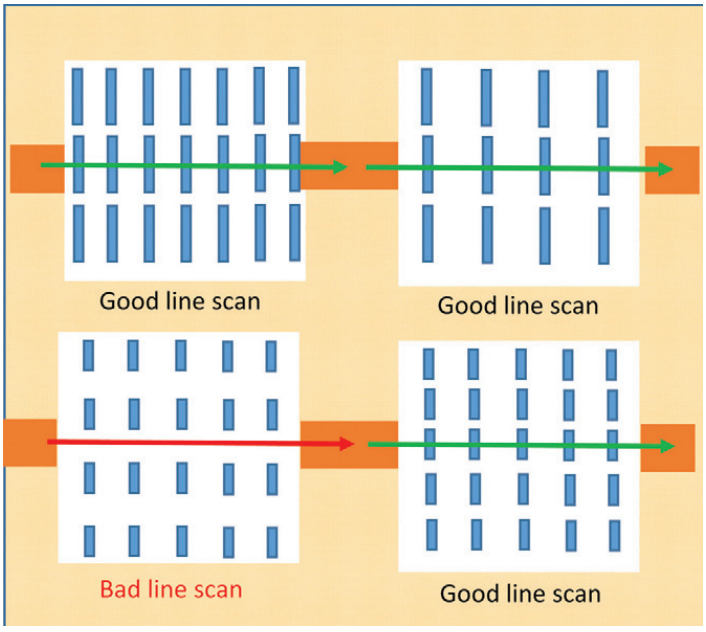

FIGURE 5. FEOL CMP test chip specifics and line scan directions.

Etchback

Because the deposited oxide pattern depends on the underlying pattern, the surface profile after oxide deposition may be highly non-planar, with large variations in oxide thickness and density. In oxide polishing processes like shallow trench isolation (STI) CMP, inter-level dielectric (ILD) CMP, inter-metal dielectric (IMD) CMP, and others, a reverse etchback process is often used prior to the polishing step to prevent film pattern density mismatches over the design that lead to post-CMP film thickness variation.

In reverse etchback, a second mask is used to etch back raised areas in the deposited film by lowering the film density. An etchback mask is usually designed by shrinking the features of the layout by a fixed amount (etchback bias). For STI processes, the underlying nitride is used as an etch stop layer. For large features,

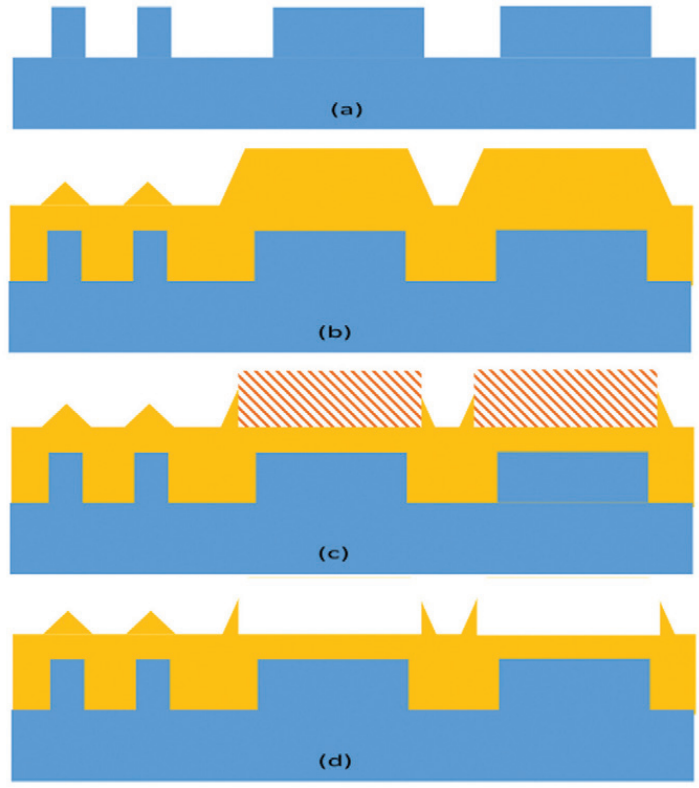

FIGURE 6. Schematic view of HDP-CVD selective reverse etchback. (a) Initial pattern, (b) Deposited oxide pattern, (c) Selective reverse etchback mask, (d) Oxide pattern after etchback.directions.

this reverse etchback removes a majority of the raised material, resulting in lower oxide density.

Selective reverse etchback refers to the customization of the etchback mask that results in less material removal than the nominal etchback process. It is accomplished by replacing a large etchback feature with an array of selective etchback cells, or even the complete removal of etchback features in some regions. A selective reverse etchback mask actually consists of two masks: one mask selects the areas where the etchback is performed (or not performed), while the other mask defines the features for etchback. For example, selective reverse etchback may be used after the HDP-CVD deposition process over large space areas where large raised oxide islands appear after deposition, as shown in **FIGURE 6**.

Modeling of the etchback process assumes modification of post- deposition profile geometry and height data due to oxide removal over large oxide areas, as defined by the selective and nominal etchback masks. The post-CMP profile trend may significantly change due to etchback (**FIGURE 7**).

Hotspots detection using CMP simulation

To find hotspots in the design, electronic design automation (EDA) vendors offer CMP modeling tools and simulators/analyzers. For example, Mentor's Calibre® CMP ModelBuilder tool supports models for the deposition processes mentioned above, and it is able to generate post-deposition profiles for polishing. The Calibre CMP ModelBuilder geometry extraction step calculates pattern density, weighted average width, space, perimeter, and other characteristics for each window, and passes them to the CMP model for simulation. The Calibre CMP ModelBuilder tool then calculates local pressure distribution due to surface profile height variation, and defines local removal rates depending on local pattern geometry and dishing. Time evolution of the polishing profile is modeled until the CMP stop condition is satisfied. Numerous CMP stop conditions used by CMP tools are supported by the simulator, and users may select the one appropriate for their process.

After the CMP model is built, designers can then use the Calibre CMPAnalyzer tool, which provides automated multi-layer CMP simulation, hotspot detection, and analysis. Designers input the GDS or OAS file of a design into the Calibre CMPAnalyzer tool, specify the layer numbers that must be simulated, and select the best recipe file of the process created by the Calibre CMP ModelBuilder tool.

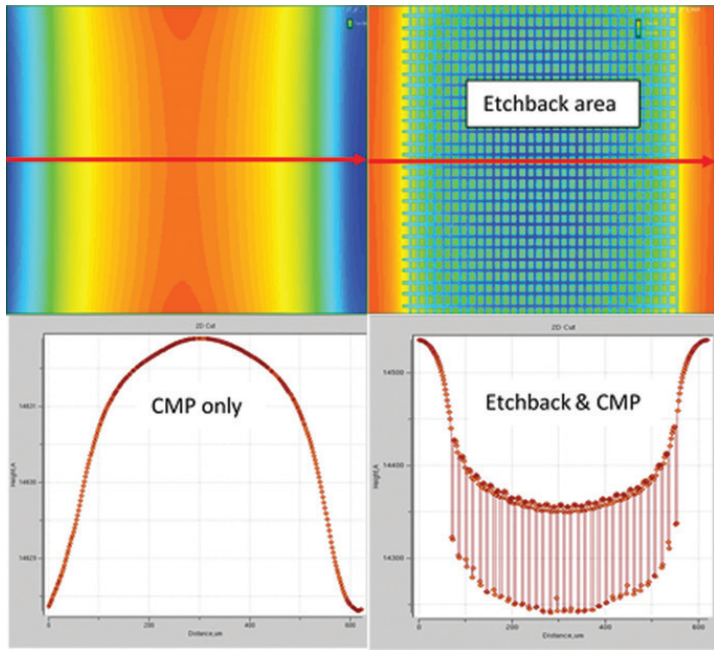

FIGURE 7. Post-CMP surface profile change due to etchback.

With the Calibre CMPAnalyzer tool, designers can then perform numerous Boolean layer operations like OR, AND, and NOT to prepare the layers for CMP simulation. Moreover, they may use a large set of Calibre Standard Verification Rule Format (SVRF) commands to generate layers for CMP simulation. This is especially useful for modern FEOL layers construction, since numerous layers are used to define STI and other layers due to double and triple patterning.

The Calibre CMPAnalyzer multi-layer CMP simulation flow supports different layer stacking options that can be used for CMP simulation of each layer to study multi-layer stacking effects and possible hotspots due to multi-layer stacking. The Calibre CMPAnalyzer tool also supports custom hotspot scripts, in which users define their own criteria for hotspots checking. Users can also generate color maps and histograms of simulated data to easily visualize post-polishing profiles and possible hotspot areas.

They can detect erosion, dishing, and depth-of-focus hotspots by using multi-layer simulation with defined threshold values for hotspots. Users can also generate simulated line scan and profile plots for measured line scan data comparison for CMP model validation and simulated surface profile analysis. ◆

3D acoustic images expand their usefulness

TOM ADAMS, *Sonoscan, Inc., Elk Grove Village, IL*

3D acoustic imaging is useful for measuring the heights of bumps on BGAs, flip chips, and other devices. But it can also be used to image and quantify depth/height variation of features within a particular sample.

Three-dimensional acoustic images, like three-dimensional light images, differ from their two-dimensional counterparts by displaying the z dimension in addition to x and y dimensions. The first 3D acoustic images were made around by 20 years ago at Sonoscan, who invented the technique. The technology can display the surface topography of a sample, or its internal profile at a desired depth.

The C-SAM® acoustic micro imaging tools that make the 3D images have a transducer that pulses ultrasound at a given frequency at or into the sample thousands of times a second as the transducer scans back and forth above the surface of the sample. A pulse of ultrasound leaving the transducer travels first through a water couplant, supplied constantly by a water jet attached to the transducer. Every time ultrasound exits one material/fluid and enters another, some of the ultrasound is reflected to the transducer; as a result, a portion of the pulse is reflected by the water-to-sample surface interface. The rest of the pulse crosses the surface interface and travels deeper into the sample.

In most acoustic imaging, the concern is with the amplitude of the returned echoes from the interior of the sample. A well bonded interface between silicon and epoxy will reflect a small amount of the pulse. The amount of ultrasound reflected causes a specific amplitude in the return echo. The echo amplitude is measured and then displayed in the acoustic image by an assigned color value for that amplitude. The highest amplitude echoes essentially indicate 100% reflection and are produced only by the interface between a solid and a gas. All gap-type defects meet this definition. By measuring the amplitude of the reflected signal and identifying those having near-total reflection, an acoustic micro imaging (AMI) tool can detect voids, cracks, non-bonds and other gap-type anomalies that threaten the longevity of a part.

3D imaging, however, cares about the position in time of a reflection from a given plane such as the surface of the sample. By measuring the distance, in time, from the end of the transducer to the front surface, AMI can assign a color value to each location in time that the front surface occurs. In this way a color representation of the topography is made. Plastic BGA packages, for example, are notorious for having internal defects that disturb the flatness of the package's surface. By assigning a color to each height variation, the locations of surface disturbances are easily detected. The same method can be used to image unpopulated printed circuit boards to ensure that they are flat enough to avoid placing stress on connections. Samples imaged in 3D are viewed at an angle from the vertical perspective in order to make local height differences visible.

Recently the method has been used in a different role - measuring the height, before substrate attachment, of the solder bumps on BGAs. A precise vertical range is set - in acoustic terms, a gate. If the tops of all the solder bumps fall within the small vertical range defined by the gate, successful bonding of all bumps to the substrate is more likely.

The basics of imaging rounded bumps are essentially the same as for imaging flat surfaces. The sides of the bump may send back little or no signal, but in this

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investigation, they are not the area of interest. The color of the top of the bump is what matters, because it indicates whether the top lies within the narrow vertical range for successful bonding. Interpretation of the image is simplified by software that stretches the image of each solder bump vertically. If the solder bumps were imaged in their actual height, the gate in which the top should lie would be tiny and hard to see. Stretching each bump vertically does not change

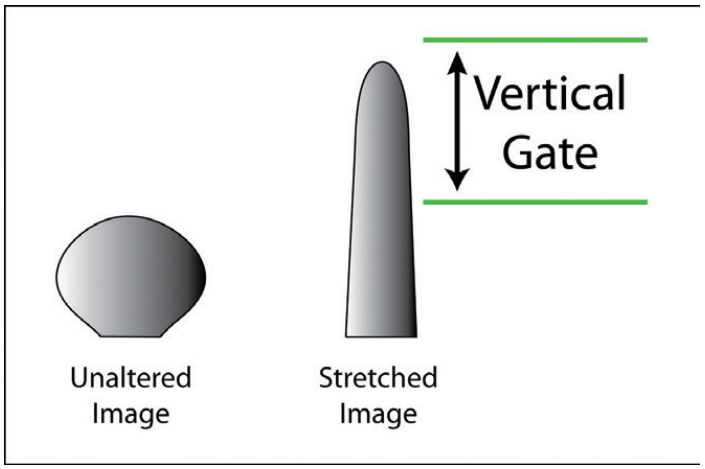

FIGURE 1. 3D imaging stretches the bump image to make accept/reject determination easier.

the measurement, it simply makes the results easier to interpret.

FIGURE 1 shows an acoustic side view image of a solder bump in its unstretched form, and the stretched form of its acoustic image. (Acoustic side views of internal features can be made by Sonoscan's Q-BAM™ imaging mode, designed for non-destructive cross sectioning.) Even after the image is stretched, it may represent a vertical extent of only several microns. If bumps were imaged without vertical exaggeration, distinguishing accept from reject might be very difficult or even impossible. The amount of stretching needed for the bumps on a particular part type of BGAs, and the vertical extent of the gate that will yield the best

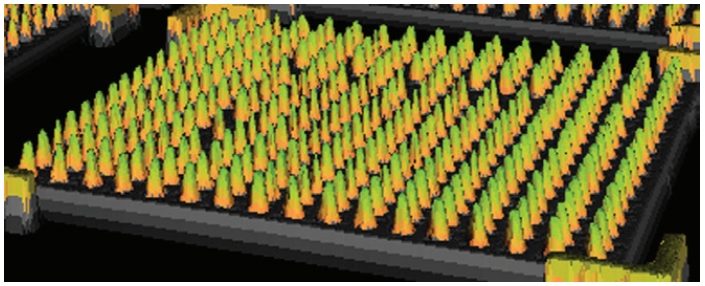

FIGURE 2. Stretched acoustic image of bumps on one BGA.

results can typically be determined from previous experience with a BGA. Overall, what matters is not the precise configuration of the gate but ensuring that all bumps are very close to each other in height.

FIGURE 2 is the stretched 3D image of the solder bumps on one BGA before placement onto a PCB. The desired condition is that the top surface of the bump lie within the thin horizontal slice colored green in the image. **FIGURE 3** is a magnified view of a small section of Fig. 2.

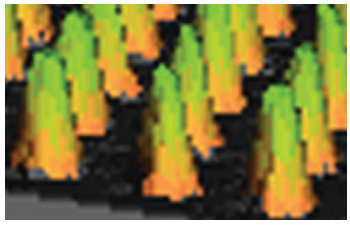

FIGURE 3. Small portion of Fig. 2 magnified.

All the bumps in this BGA have tops that lie within the vertical "green" gate. There are no bumps toppled by other colors, a condition that would reveal that the bump might not bond to the substrate as well. The black areas in the figure are locations where no bump is present. BGAs like this are loaded into JEDEC-style trays and imaged in large quantities. Identification and removal of BGAs having one or more unsuitable bumps can be automated. The failure criteria are completely customizable depending on the level of tolerance a particular sample is held to.

FIGURE 4. Small portion of a BGA having unacceptable variation in bump height.

FIGURE 4 is a small portion of the 3D image of a BGA where results were not quite so uniform. The desired color for the top of each bump here is red. As shown red is the top color on many of the bumps, especially in the left half of the image. But elsewhere there are bumps with pink, orange and other top colors. This is a BGA that may not make good contact with the PCB. Further down the assembly line this sample would likely experience immediate or early electrical failures due to attachment issues.

Location information can become useful to large scale production companies that are trying to understand their process better. If there are trends that suggest a specific location on the BGA is having a bump height problem, then there maybe something related to the process, handling, or materials being used that could

be causing the issue. The measurement can be taken simultaneously while scanning in standard reflection mode. There is no addition in scan time or reduction in UPH to make this measurement.

3D imaging can also be used to depict strictly internal features. The operator sets two vertical values - an internal gate - to define the top and bottom of the desired depth measurement. This mode is known as profile mode imaging. When imaging in profile mode, only the echoes that occur within the depth of the gate are used for imaging. Signals outside of the gate are ignored. Because this is 3D imaging inside the part, the variation is measured relative to the top surface of the part.

3D acoustic imaging is useful for measuring the heights of bumps on BGAs, flip chips, and other devices. But it can also be used to image and quantify depth/height variation of features within a particular sample. Measuring the distance of each of the thousands of x-y locations across the entire top surface of a tilted die can reveal how much of a threat to longevity the tilt is. It may even be helpful to stretch the image vertically to make so that the tilt could be easily seen to the human eye. Depending on the gate and depth chosen for a given profile mode image, it is possible to discern defects that occur at different height locations. This can be useful by showing that two similar looking defects may not be occurring at the exact same depth within the part. For example, you may have a void within the molding compound just a few microns before the lead frame. In standard reflection mode imaging, it would be impossible to determine if the defect occurred just before the lead (inclusion within the mold compound) or if the defect was a result of poor bonding directly to the lead frame. The is because standard reflection mode imaging only measures the amplitude of a given echo and not its location in time. Using profile mode, the depth location information is displayed using a color bar to depict the height information. In this way, defects that occur at different heights will also be assigned a different color value. This is the value of 3D acoustic imaging: mapping Time-Distance relationships at the surface or internally for a given sample in a manner that is useful and easy to interpret.

Surface preparation technology provides pristine and stable hydrogen passivated semiconductor surfaces

ROBERT PAGLIARO, *RP Innovative Engineering Solutions, LLC, Mesa, AZ*

A new technology enables dramatically lower thermal budget capability that is enabling to thermal processes like epitaxy, CVD and diffusion, without any semiconductor material consumption.

As semiconductor based electronic devices have become smaller, faster, smarter, 3-dimensional, and multi-functional the methods and materials required to fabricate them demand novel approaches to be developed and implemented in the device manufacturing facilities. Amongst the most challenging requirements are the need to lower the thermal budgets of the front end thermal processes and to minimize the semiconductor material consumption that comes with the conventional oxidizing (hydrogen peroxide and ozone based chemistries) wet cleaning processes chemistries such as APM, HPM, SPM and SOM.

A novel wet surface preparation method that removes existing surface contamination and native oxide from semiconductor surfaces and then passivates them with a pristine and stable hydrogen passivated surface has been developed and commercialized by APET Co, Ltd. in a system called the TeraDox. This patented technology enables dramatically lower thermal budget capability that is enabling to thermal processes like epitaxy, CVD and diffusion, without any semiconductor material consumption.

The TeraDox system is an enhanced version of the APET FRD (HF etching, Rinse and Dry). The name TeraDox implies the ability to provide a process chemistry with < 1 ppb impurities, particularly dissolved oxygen, which allows for producing pristine and stable H-passivated semiconductor surfaces. Dilute HF and HCl (dHF and dHCl) are the etching chemistries used for removing the native and chemical oxides from Si, SiGe and Ge surfaces. The TeraDox system has a single vessel wet processor and a wafer transfer/drying hood that allows for a segue between the load, chemical fill, etch, insitu-rinse, dry and unload steps of the process sequence, while keeping the process chemistry and the wafers in a continuous ambient of ultra-pure N_2. This equipment and process design eliminate the exposure of the wafers to air and minimizes gas permeation throughout the entire oxide removal and H-passivation process sequence. These are all critical elements to achieving the best surface quality results.

While there are a variety of important parameters towards achieving a pristine and stable H-passivated surface one of the most enabling ingredients to the APET TeraDox process and equipment IP is the PPT level degassing capability for the UPW and aqueous chemicals used in the H-passivation process. The unique UPW and chemical degassing apparatus require an optimized hardware configuration with membrane contactors and facilities used for the vacuum + UHP N_2 sweep gas to achieve a DO degassing efficiency > 99.999%. This ultra-high degassing

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efficiency allows for a Dissolved Oxygen (DO) concentration capability of < 100 ppt.

It has been well proven and documented by multiple world-renowned surface scientists [1,2,3] since the late 1980s that the level of dissolved oxygen (DO), as well as other dissolved impurities (such as CO2, TOC, silica and N_2), has a direct impact on the efficiency of H-passivation and the native oxide (initial and changing thickness vs. queue time) that follows the removal of native and chemical oxides from semiconductor surfaces. Queue time (Q-time) is the amount of time that the H-passivated wafer are exposed to air before being placed in an inert environment for the subsequent process step (epi, poly silicon, metal, ion implantation etc.). It can be seen in **FIGURE 1** how native oxide regrowth occurs after HF treatment in air and UPW vs. exposure time [1].

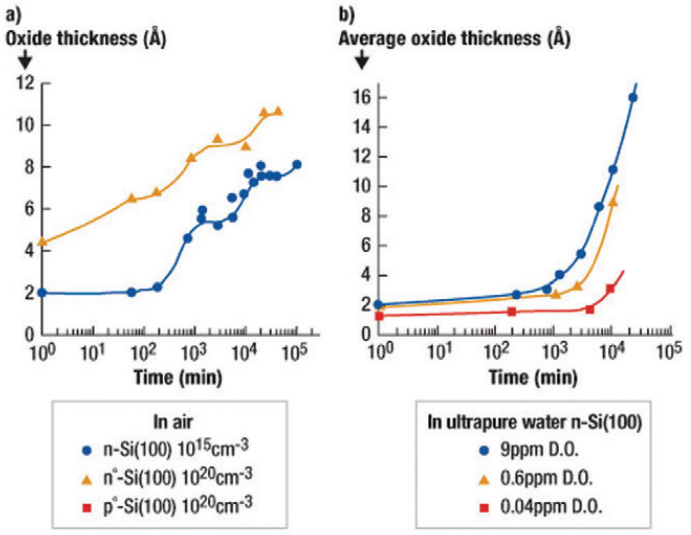

FIGURE 1. Post-HF etch native oxide thickness vs. exposure time to air and UPW.

A similar DO vs. surface oxide and carbon relationship is also verified using encapsulated SIMS. This method uses dynamic SIMS to measure the amount of O, C that are trapped at the epi layer/silicon wafer interface. This has been a widely used characterization method to assess a pre-low temperature epi surface preparation process' hydrogen surface passivation quality since the early 90s. The typical epi cap is ~80-150nm and is deposited using a 650°C SiH4 source deposition process. The objective is to be able to minimize the thermal budget of the pre-deposition bake step which is required to remove any surface oxides and organics to allow perfect epitaxial deposition with no contaminants or defects at the interface.

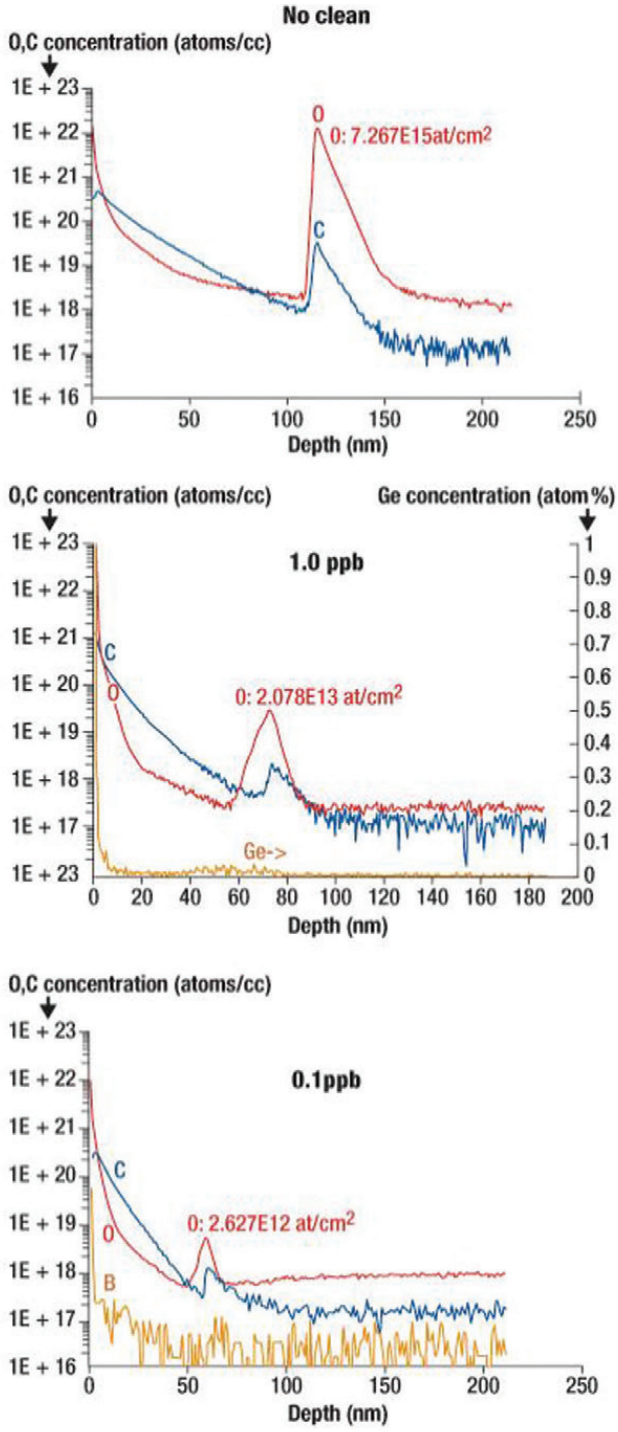

FIGURE 2. SIMS profiles demonstrating the interfacial aerial oxide and carbon densities vs. the HF last wet clean using UPW DO @ 1 ppb and 0.1 ppb + SiGe cap using a 650C no bake SiH4 + GeH4 deposition process.

FIGURE 2 demonstrates how the encapsulated SIMS interface O (areal oxide density, AOD) using a 650°C SiH4 no bake Si deposition process is strongly dependent on the DO concentration. Three samples are depicted with different surface preparation conditions, a reference wafer with no surface preparation, a wafer dHF wet processed

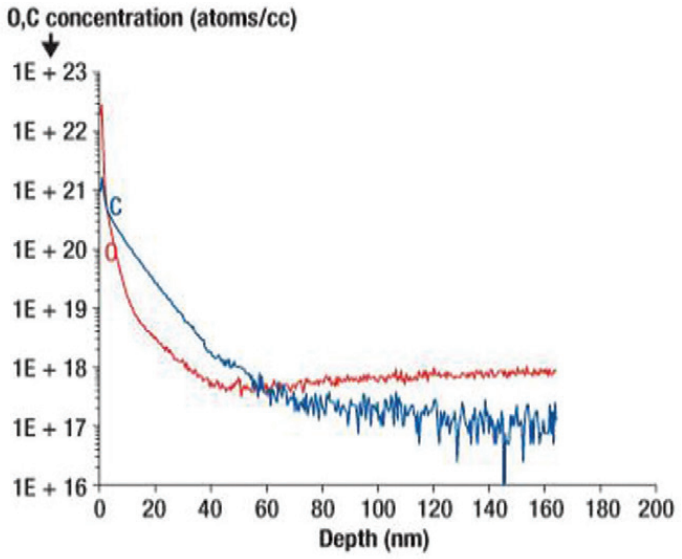

FIGURE 3. Encapsulated SIMS profile demonstrating no detectable oxide or carbon (DL ~ 1E11 at/cm^2) with the APET HF last wet clean using UPW with DO @ 0.1ppb + Si cap using 700C-80T-60s bake + 650C SiH4 deposition process

with the UPW DO ~ 1ppb, and a wafer dHF wet processed with the DO ~0.1 ppb.

It can be seen in **FIGURE 3** how applying a 700C/80T/60s bake before a 650C Si deposition process with the UPW DO at 0.1ppb yields non-detectable O and C. This SIMS data info is relatively old (2010) but is still good for reference. The current APET TeraDox wet process capability can provide non-detectable O and C without a bake before the 650°C Si deposition process.

As mentioned earlier, undesirable native oxide thickness increases with queue time on H-passivated Si, SiGe and Ge surfaces. So, it is important to minimize the Q-time between the H-passivation process and the subsequent process step, but the quality and stability of the H-passivation does need to accommodate practical queue times in a manufacturing environment. The H-passivation from the APET TeraDox process has proven to be stable enough for up to at least 8-hour Q-times for most low temperature process applications, which makes it suitable for most semiconductor device manufacturing facilities.

Aside from the low surface oxygen benefit from having ultra-low DO in this process there are other very important benefits to this as well. Having ultra-low DO prevents water marks, microroughness (faceting), bacterial contamination and material consumption. If there is no DO in the UPW or the etching chemistry then there is no competing mechanism to simultaneously oxidize and etch the semiconductor material during the oxide etch and insitu-rinse steps. If the surface is being oxidized/etched then orientation selective faceting will occur. Faceting leads to generation a mix of mono-, di- and tri- hydride terminations on the different orientations of the semiconductor surface. An example is silicon (100), which if it is kept atomically smooth after the oxide is removed by HF, the surface will be dominated by di-hydride terminations. If the surface is faceted it will contain lower energy mono-hydride terminations. Higher energy hydride bonds lead to better surface stability while the lower energy hydride bonds make the surface less stable and will re-oxidize faster with Q-time.

So in general, the pristineness and the atomic smoothness of the semiconductor surface are what dictates the quality and stability of the H-passivating surface preparation process.

While the TeraDox process performance has continued to improve with the new innovations, the capabilities have surpassed the detection limits of conventional measurement methods like encapsulated SIMS characterization. Encapsulated SIMS also has a lot of drawbacks and limitations which make it an impractical process monitoring method in manufacturing facilities. The need to have a more sensitive measurement method that can measure "as processed" surfaces in a fast, real time and non-destructive manner had become an urgent requirement.

There are a variety of very good electrical and optical measurement methods that have been in use for many years, but most of them do not provide surface specific information directly. Surface parameters such as surface recombination velocity and lifetime (SRV and Ts) can be calculated relatively accurately using multiple step procedures by measurement methods such as uPCD, QSS-PC, PL and SPV. SRV (surface recombination velocity) and Ts (surface recombination lifetime) are extremely sensitive to surface contamination such as C, O metals and dopants as well as microroughness. This diverse sensitivity make it ideal for assessing surface preparation methods.

Until recently, only one measurement technique has been found that can measure the SRV and Teff (effective lifetime) of the surface directly and quickly on as processed H-passivated wafers. While doing a lot of research for the ideal measurement method to pair with the APET TeraDox H-passivation process, it was discovered that an enhanced version of the CADIPT

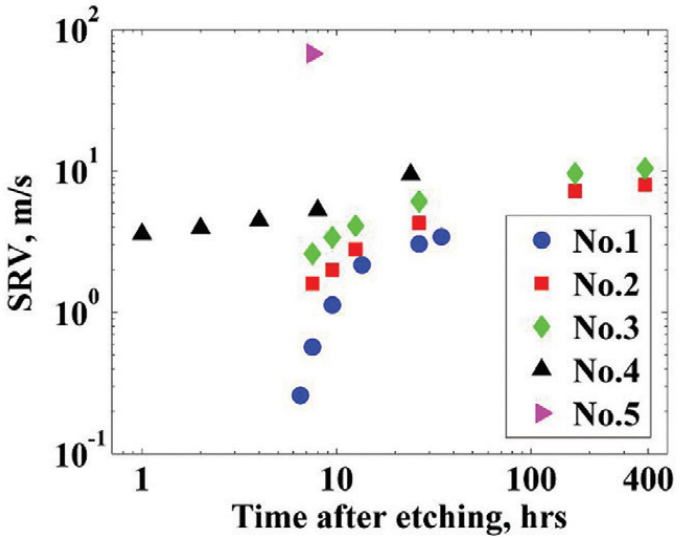

FIGURE 4. Q-LIC SRV measurements vs Q-time for four different HF last wet processes.
No. 1: APET TeraDox with UPW DO @ 40 ppt
No. 2: APET TeraDox with UPW DO @ 400 ppb
No. 3: FSI SAT with non-degassed UPW DO @ ~ 2ppm
No. 4: UT R&D wet bench with non-degassed UPW
No. 5: unprocessed control wafer
Note: SRV measurements for Q-times < 6.5 hrs. not available for No. 1, 2, 3 and 5 due to the transport time of the samples from the surface preparation tools in Baltimore, MD to the PCR-LIC tool at the University of Toronto.

department at the University of Toronto's PCR-LIC technology, called Quantitative Lock-in Carrierography and Imaging (Q-LIC), could have the unique and enabling capabilities needed for this application. After completing an array of screening and optimization testing over the course of 8 months, the results have validated Q-LIC as an ideal measurement method for "as processed" H-passivated surfaces. In **FIGURE 4** the plot demonstrates the SRV vs Q-time for four different wet cleans and an unprocessed control. The data shows strong evidence of the differentiation between different H-passivation methods (process and equipment), the level of DO in the wet process chemistry, and the dynamically changing surface state over time.

APET currently has five patents, related to this technology, integrated on the commercially available TeraDox wet process equipment, four of which include the use of vacuum/N_2 sweep degassing with membrane contactors for both the UPW and chemical degassing.

The UPW degassing is done in a separate stand-alone module (called the APET Dox unit) that treats up to 60 lpm of UPW before going to the main unit. All Dox units are guaranteed to have DO < 1 ppb, but all of the units in use to date achieve < 200 ppt. The most recently installed Dox unit system has a base DO level of ~30-40 ppt. Aside from the importance of PPT level degassing of the UPW much attention has also been given towards the design and materials used in the entire TeraDox system to prevent gas permeation into the UPW supply and the process chemistry to achieve optimum H-passivation.

The most recent TeraDox related patent that was issued to APET was for chemical degassing. The degassing of the HF and HCl are typically overlooked in this application. Typically, HF comes in ~48% and HCl in ~37% concentrations with the balance of these supplied mixtures is in DO saturated water. So even diluted etching chemistries of up to 400 (UPW) :1 (chemical) ratios will typically still produce a composite DO of > 3ppb in the process vessel, even if the UPW supply is degassed to 0 ppt. Having the unique chemical degassing capability to < 1ppb DO significant improves the overall performance of the H-passivation process. The chemical degassing apparatus is integrated into the HF and HCl chemical delivery lines inside the TeraDox system's main unit.

In summary, APET has developed and commercialized a unique and enabling wet surface preparation technology, the TeraDox process and equipment, that can produce pristine and stable hydrogen passivated semiconductor surfaces. While there are several critical factors and innovations that enable the TeraDox's unique process performance capabilities, the fully integrated "dry in/dry out" system design and the unique PPT level degassing of the process chemistries are the most facilitating features on the TeraDox system.

Acknowledgement

A special thanks to Dr. Andreas Mandelis and his staff at the University of Toronto for their support in optimizing their Q-LIC system to provide data for this paper as well as demonstrating a suitable measurement method for the "as processed" H-passivation application.

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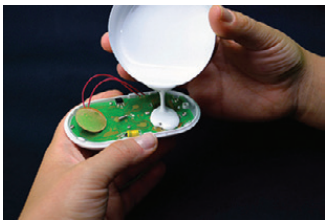

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Smart management in the sub-fab improves safety, reliability, cost and yield

With the prospects of large 450mm wafers going nowhere, IC manufacturers are increasing efforts to maximize fabrication plants using 300mm and 200mm diameter silicon substrates. The number of 300mm wafer production-class fabs in operation worldwide is expected to increase each year between now and 2021 to reach 123 compared to 98 in 2016, according to the forecast in IC Insights' Global Wafer Capacity 2017-2021 report.

Significant opportunities to improve safety, reliability and yield still remain in our industry, many of them to be found in the sub-fab, where the critical systems that supply vacuum and treat exhaust gases are to be found—out of sight and, too often, out of mind. Properly handling and removing noxious components in the exhaust flow clearly impacts the safety of fab personnel and the quality of the local environment. As for reliability, when the sub-fab fails the process is down. And yield—the yield of many tools depends directly on steady, high-quality vacuum. "Smart" management of sub-fab systems can improve safety, reliability, yield, and energy efficiency, all of which contribute directly to the bottom line.

For example, consider high-flow CVD processes, which are finding increasing application in high-volume production of 3D-NAND, DRAM and other devices. The process precursors and their decomposition products can present a flammability risk and, unless properly controlled, can condense as hazardous materials in process exhausts. Such condensation can cause a variety of operational problems, including process shut-downs when pipes become blocked, exhaust pipe fires when fluorine reacts with residual silicon compounds, and HF vapour releases when pipes are exposed to atmosphere during cleaning.

Several approaches may be used to address these concerns, alone or in combination. The entire exhaust assembly may be heated to maintain a thermal profile that eliminates condensation, though eliminating all cold spots can pose practical difficulties and constant monitoring is required. Exhaust gases may be diluted to mitigate flammability risks, but the cost of the additional diluting gas (N2) becomes prohibitive at high flows. The total cost of ownership for high dilution flows must also include increased capital investment, operating cost and sub-fab space requirements for additional abatement capacity.

Andrew Chambers,
Senior Product Manager, Edwards Ltd.

A smart dilution strategy would continuously adjust the flow of dilution gas based on information from the process tool. Is flammable gas flowing? Is oxidant gas present? If the process gas is non-flammable, can dilution be eliminated entirely? When only a flammable gas is flowing, how much can dilution be relaxed while still maintaining the mixture below the lower flammability limit; or can it be allowed to exceed the LFL, since there is no concurrently flowing oxidant? When flammable gases flow concurrently with oxidizing gases, what dilution is required to keep the concentration of flammable gas below its LFL, with a sufficient safety margin to allow for fault scenarios? What is the best dilution for cleaning gases to optimize the safety and efficiency in their abatement? Answers to these questions and more can be found by analyzing information from the process tool and can be used in a smart dilution strategy to ensure safety, and maximize reliability and yield while minimizing cost.

Information from the process tool can also be used to control the operation of the abatement system. When only flammable gas is flowing with low or moderate dilution, the abatement system can be operated in a "low fire" mode, minimizing consumption of fuel, city water and process cooling water. When flammable and oxidizing gases flow concurrently and high dilution flow is used, the abatement can be switched into a "high fire" mode to ensure full destruction of the process chemicals.

Coupled with smart operation, smart system design can further improve safety, reliability and cost. Consider the problem of gas leaks. Leaks from process exhaust pipes can lead to fires, equipment damage and harm to sub-fab personnel. Local gas leak detectors can protect personnel but risk process shut-down and product loss. Rigorous leak checking procedures can reduce the risk of leaks following maintenance, but cannot prevent progressive seal degradation or leaks that occur during normal operation. A smart design integrates pumps, abatement and all connecting piping in a single unit, engineered for performance and safety and thoroughly tested at all stages of manufacturing and installation. Integration also permits exhaust integrity checking, double-containment, accurate and consistent exhaust temperature control, and tool-connected "smart" operation and provides single-vendor responsibility for maintenance and performance.

Opportunities for improvements abound, but taking advantage of them requires a smart approach based on broad experience and thorough understanding of semiconductor manufacturing processes. ◆

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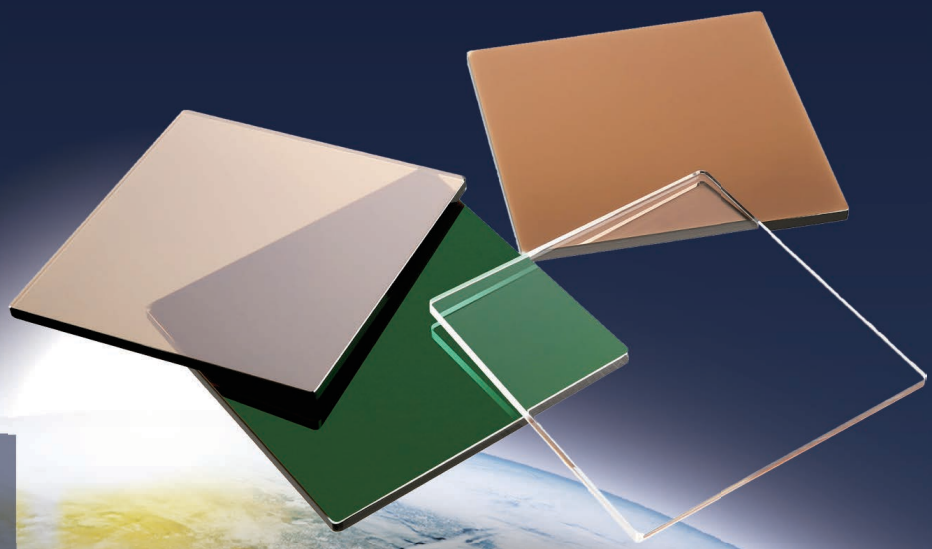

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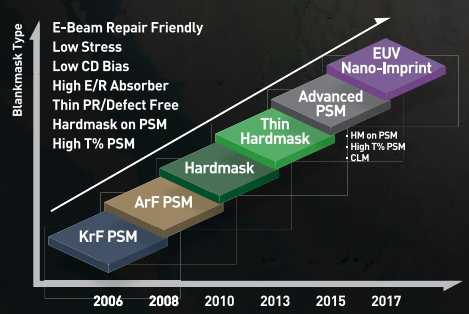

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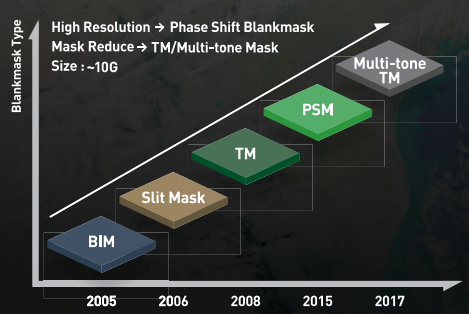

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