

Solid State TECHNOLOGY

Insights for Electronics Manufacturing

**Threshold Voltage
Tuning for 10nm**

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**Managing Oxide
Growth**

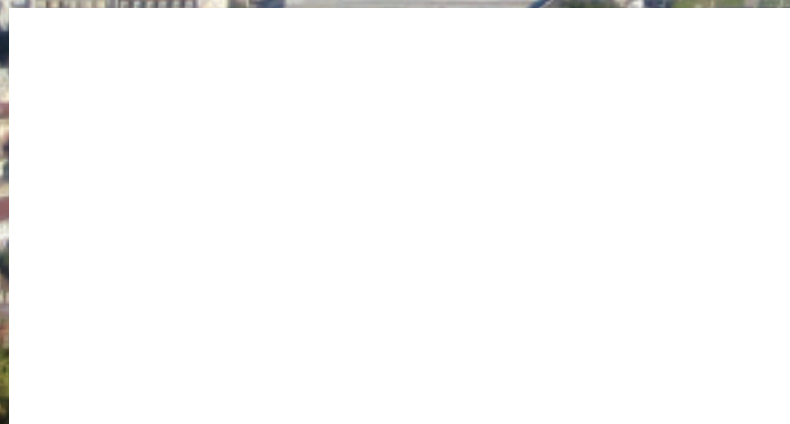
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OCTOBER 2014 VOL. 57 NO.7

The iconic "bubble" cable cars in Grenoble, home to SEMICON Europa 2014.

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All parts of the semiconductor supply chain will come together at the ALPEXPO center in Grenoble, France.
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Web Exclusives

Insights from the Leading Edge: ECTC Coverage

The advent of 2.5 and 3DIC has caused revisions in the way area array bump interconnect is carried out. Dr. Phil Garrou reviews presentations from ECTC on thermo-compression bonding, breaking down sessions hosted by Qualcomm, STATSChipPAC and Toray.

<http://bit.ly/XoPIBi>

Leti integrates everything

Ed Korczyński knows how wafers feel when moving through a fab. From SemiMD, part of the Solid State Technology network.

<http://bit.ly/1qhwUp8>

Monolithic 3D breakthrough at IEEE S3S 2014

In the upcoming 2014 IEEE S3S conference (October 6-9), MonolithIC 3D will unveil a breakthrough flow that is game-changing for 3D IC. For the first time ever monolithic 3D ("M3DI") could be built using the existing fab and the existing transistor flow. From SemiMD, part of the Solid State Technology network.

<http://bit.ly/1toHkta>

Internet of Things infographic

The global IoT market is poised for explosive growth. By 2020, the market is expected to soar to \$7.1 trillion. This infographic, courtesy of Jabil, gives an good overview of what will be connected (even garbage bins!).

<http://bit.ly/1wsXh17>

Design and manufacturing technology

The fabless-foundry relationship in commercial IC manufacturing was established during an era of fab technology predictability—clear litho roadmaps for smaller and cheaper devices—but the future of fab technology seems unpredictable. The complexity which must be managed by a fabless company has already increased to justify leaders such as Apple or Qualcomm investing in technology R&D with foundries and with EDA- and OEM-companies. To gain some insight into these issues, we recently asked leading industry visionaries to answer a few questions.

<http://bit.ly/1meaALx>



Sensory Shanghai

Stephen Whalley was in Shanghai to co-host the inaugural MEMS Industry Group (MIG) Conference Shanghai, September 11-12th, with local partners, the Shanghai Industrial Technology Research Institute (SITRI) and the Shanghai Institute of Microsystem and Information Technology (SIMIT). The theme was the Internet of Things and how the MEMS and Sensors supply chain needs to evolve to address the explosive growth in China.

<http://bit.ly/1miQdn2>

Intel releases new packaging, test technologies for 14nm foundries

Intel Corporation announced two new technologies for Intel Custom Foundry customers that need cost-effective advanced packaging and test technologies.

<http://bit.ly/1tpbEnk>

Scientists craft a semiconductor only three atoms thick

Scientists have developed what they believe is the thinnest-possible semiconductor, a new class of nanoscale materials made in sheets only three atoms thick.

<http://bit.ly/1wlJLcC>

What's in a name? Innovation for humanity

The project names Gooru, Nanoly, and Sanergy are intriguing. The fact these names represent efforts all over the world, from India to Latin America to Africa, peaks curiosity. And, the actual work of the 2014 Tech Laureates is absolutely amazing. From SemiMD, part of the Solid State Technology network.

<http://bit.ly/1svTRqp>



A salute to European technology

I'm looking forward to SEMICON Europa this month, which will be held for the first time in France, in Grenoble. There's not a big airport, so I'm flying into Geneva and hopping on a bus for a 2 hour ride (the other choice is Lyon, which is closer but a bit more expensive to fly into). I suspect this might also be the first SEMICON that is not close to a major airport,

"I hope to see you in Grenoble!"

but Heinz Kundert, president of SEMI Europe, tells me that the show will be 40% larger than it was last year in Dresden. It also has an impressive 70 sessions with 300 speakers.

Europe has always been a powerhouse when it comes to semiconductor research. The work at imec, CEA-Leti and Fraunhofer alone is truly amazing and world class. The challenge has always been taking that research and commercializing it. Part of that challenge is that the bulk of the world's semiconductor manufacturing is not in Europe, but in Asia and the U.S.

Yet there are significant manufacturing operations in Europe, notably fabs run by Infineon,

STMicroelectronics, GlobalFoundries, Bosch, TI, NXP, Altis, LFoundry, Philips Lumileds, XFAB, AMS, Analog Devices and Freescale.

Like Europe itself, these fabs are diverse. There's a large variety in the products they produce, volume, wafer size, technology and even the level of automation.

What's promising is that this diversity could actually work to Europe's advantage when it comes to the booming application in IoT and biomedical. As Kundert notes in this month's cover story, "It's a big challenge, but we believe if somebody can manage it successfully, it's Europe. We are very experienced in those types of applications," he said.

Supporting all of this is the "10-100-20" program announced last year. It's an ambitious strategy to double the economic value of semiconductor production in Europe in the 2020-2025 timeframe. This goal is to achieve this by an unprecedented public/private investment partnership with 10 billion Euros in public/private funding and 100 billion Euros from the industry. I believe the research and desire is there, so it will be interesting to see how that unfolds. I hope to see you in Grenoble!

—Pete Singer, Editor-in-Chief

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news

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USA | David Bell joined **Triad Semiconductor's** board of directors.

ASIA | **Oxford Instruments** launched its third annual Indian nanotechnology seminars in Kolkata and Delhi.

USA | **GLOBALFOUNDRIES** and the **Semiconductor Research Corporation** announced a new research scholarship program for undergraduate engineering students.

EUROPE | **Element Six** was selected by the European Commission's Seventh Framework Programme for Research and Technological Development to help develop a new ultrafast pulse disk laser.

USA | **NVIDIA** filed complaints against Samsung and Qualcomm for allegedly infringing NVIDIA GPU patents.

ASIA | **Samsung** adopted ProPlus Designs' 14nm FinFET process.

USA | **SEMI** successfully appealed to the U.S. government to review the validity of current export controls on semiconductor etch equipment.

ASIA | **SEMICON Taiwan** was held in Taipei.

USA | **GLOBALFOUNDRIES** announced that Louis "Lou" Lupin joined the company as senior vice president and chief legal officer.

ASIA | **United Microelectronics Corporation (UMC)** will join Fujitsu's new foundry company.

USA | **UC Santa Barbara** researchers developed ultra sensitive biosensor from molybdenite semiconductor.

For electronics beyond silicon, a new contender emerges

Silicon has few serious competitors as the material of choice in the electronics industry. Yet transistors, the switchable valves that control the flow of electrons in a circuit, cannot simply keep shrinking to meet the needs of powerful, compact devices; physical limitations like energy consumption and heat dissipation are too significant.

Now, using a quantum material called a correlated oxide, Harvard researchers have achieved a reversible change in electrical resistance of eight orders of magnitude, a result the researchers are calling "colossal." In short, they have engineered this material to perform comparably with the best silicon switches.

The finding arose in what may seem an unlikely spot: a laboratory usually devoted to studying fuel cells—the kind that run on methane or hydrogen—led by Shriram Ramanathan, Associate Professor of Materials Science at the Harvard School of Engineering and Applied Sciences (SEAS). The researchers' familiarity with thin films and ionic

transport enabled them to exploit chemistry, rather than temperature, to achieve the dramatic result.

Because the correlated oxides can function equally well at room temperature or a few hundred degrees above it, it would be easy to integrate them into existing electronic devices and fabrication methods. The discovery, published in *Nature Communications*, therefore firmly establishes correlated oxides as promising semiconductors for future three-dimensional integrated circuits as well as for adaptive, tunable photonic devices.

Challenging silicon

Although electronics manufacturers continue to pack greater speed and functionality into smaller packages, the performance of silicon-based components will soon hit a wall.

"Traditional silicon transistors have fundamental scaling limitations," says Ramanathan. "If you shrink them beyond a certain minimum feature size, they

Continued on page 7

Rudolph introduces new acoustic metrology and defect inspection technology for 3DIC and advanced packaging applications

Rudolph Technologies has introduced its new SONUS Technology for measuring thick films and film stacks used in copper pillar bumps and for detecting defects, such as voids, in through silicon vias (TSVs). Copper pillar bumps are a critical component of many advanced packaging technologies and TSVs provide a means for signals to pass through multiple vertically stacked chips in three dimensional integrated circuits

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Sapphire display covers featured in Apple smart watches but not in iPhone 6

The long wait is finally over. From a sapphire industry standpoint, Apple killed the suspense within the first 10 minutes by announcing that its new 4.7" and 5.5" iPhone 6 and iPhone 6 plus will both feature a traditional ion-exchange strengthened glass display cover. Sapphire remains in the camera lens cover and the touch ID sensor, features that were already present on the iPhone5 S.

In its recent report on the sapphire industry, Yole Développement analysts wrote that they believe that technical and manufacturing issues at various levels of the supply chain have prevented Apple from using

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Fairchild Semiconductor to close two facilities, cutting 15% of workforce

Fairchild Semiconductor announced it will eliminate its internal five-inch and significantly reduce six-inch wafer fabrication lines, resulting in the closure of its manufacturing and assembly facilities in West Jordan, Utah and Penang, Malaysia, as well as the remaining five-inch wafer fabrication lines in Bucheon, South Korea.

Following the moves, Fairchild will operate production lines using eight-inch wafers in Maine and Pennsylvania, and retain one six-inch factory in Bucheon.

"Fairchild will also continue operating assembly and test facilities in Cebu, Philippines and Suzhou, China," said Mark Thompson, Fairchild's chairman and CEO.

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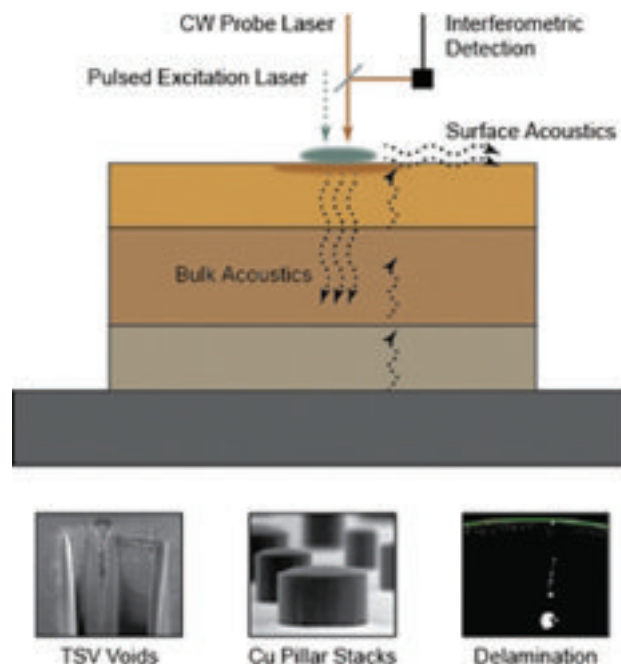
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(3DIC). The new SONUS Technology is non-contact and non-destructive, and is designed to provide faster, less costly measurements and greater sensitivity to smaller defects than existing alternatives such as X-ray tomography and acoustic microscopy.

"SONUS Technology meets a critical need for measuring and inspecting the structures used to connect chips to each other and to the outside world," said Tim Kryman, Rudolph's director of metrology product management. "Copper pillar bumps and TSVs are critical interconnect technologies enabling 2.5D and 3D packaging. The mechanical integrity of the interconnect and final device performance are directly dependent on tight control of the plating processes used to create copper pillar bumps. Likewise, the quality of the TSV fill is critical to the electrical performance of stacked devices. This new technology allows us to measure individual films and film stacks with thicknesses up to 100µm, and detect voids as small as 0.5µm in TSVs with aspect ratios of 10:1 or greater."

Kryman added, "SONUS Technology builds on the expertise we developed in acoustic metrology for our industry-standard MetaPULSE systems, which are widely used for front-end metal film metrology. By offering similar improvements in yield and time-to-profitability in high volume manufacturing (HVM), SONUS offers a compelling value proposition to advanced packaging customers."

Both MetaPULSE and SONUS systems use a laser to initiate an acoustic disturbance at the surface of the sample. As the acoustic wave travels down through the film stack, it is partially reflected at interfaces between different materials. Although the detection schemes are different, the reflected waves are detected when they return to the surface and the elapsed time is used to calculate the thickness of each layer. In the case of SONUS Technology, two lasers are used. The first laser excites the sample and the second probes for the returning acoustics. This decouples excitation and detection allowing SONUS to continuously probe the sample resulting in a much larger film thickness range. So, where MetaPULSE can measure metal films and stacks to ~10 microns, SONUS can measure films in excess of 100 microns. In addition, SONUS Technology's use of interferometry to characterize the surface displacement provides a rich data set that can be analyzed to not only characterize film thickness, but perform defect detection.



The primary alternatives for such measurements are X-ray based tomographic analysis and acoustic microscopy. SONUS Technology's ability to detect voids as small as half a micrometer is approximately twice as good as current X-ray techniques, which have a spatial resolution of about 1 micrometer. Acoustic microscopy can make similar measurements, but the sample must be immersed in water, which, though not strictly destructive, does effectively preclude the return of the sample to production. SONUS is both non-contact and non-destructive and is designed for R&D and high-volume manufacturing.

In the run up to the product introduction, Rudolph worked closely with TEL NEXX to develop SONUS-based process control for pillar bump and TSV plating processes. Arthur Keigler, chief technology officer of TEL NEXX, said, "We are attracted by the opportunity SONUS Technology offers our mutual customers in the advanced packaging market. The ability to measure multi-metal film stacks for Cu pillar, and then continue to use the same tool for TSV void detection offers immediate productivity and cost benefits to manufacturing and development groups alike."

While Rudolph is initially focused on using the technology for copper pillar bump process metrology and TSV inspection, they are also investigating other applications, ranging from detecting film delamination to metrology and process control for MEMS fabrication processes. ◀

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don't quite behave as they should."

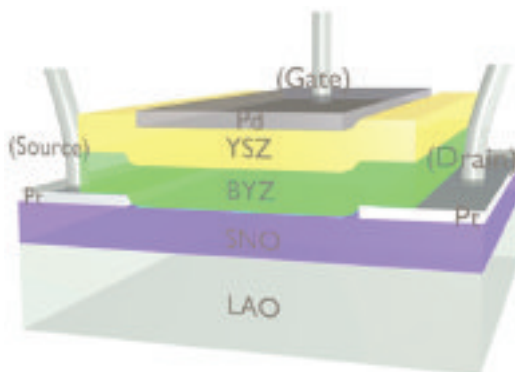
Yet silicon transistors are hard to beat, with an on/off ratio of at least 104 required for practical use. "It's a pretty high bar to cross," Ramanathan explains, adding that until now, experiments using correlated oxides have produced changes of only about a factor of 10, or 100 at most, near room temperature. But Ramanathan and his team have crafted a new transistor, made primarily of an oxide called samarium nickelate, that in practical operation achieves an on/off ratio of greater than 105—that is, comparable to state-of-the-art silicon transistors. In future work the researchers will investigate the device's switching dynamics and power dissipation; meanwhile, this advance represents an important proof of concept. "Our orbital transistor could really push the frontiers of this field and say, you know what? This is a material that can challenge silicon," Ramanathan says.

Solid-state chemical doping

Materials scientists have been studying the family of correlated oxides for years, but the field is still in its infancy, with most research aimed at establishing the materials' basic physical properties.

"We have just discovered how to dope these materials, which is a foundational step in the use of any semiconductor," says Ramanathan.

Doping is the process of introducing different atoms into the crystal structure of a material, and it affects how easily electrons can move through it—that is, to what extent it resists or conducts electricity. Doping typically effects this change by increasing the number of available electrons, but this study was different. The Harvard team manipu-



A new type of correlated transistor where the transistor action is gated by an ionic field. Image courtesy of Jian Shi.

lated the band gap, the energy barrier to electron flow.

"By a certain choice of dopants—in this case, hydrogen or lithium—we can widen or narrow the band gap in this material, deterministically moving electrons in and out of their orbitals," Ramanathan says. That's a fundamentally different approach than is used in other semiconductors. The traditional method changes the energy level to meet the target; the new method moves the target itself.

In this orbital transistor, protons and electrons move in or out of the samarium nickelate when an electric field is applied, regardless of temperature, so the device can be operated in the same conditions as conventional electronics. It is solid-state, meaning it involves no liquids, gases, or moving mechanical parts. And, in the absence of power, the material remembers its present state—an important feature for energy efficiency.

"That's the beauty of this work," says Ramanathan. "It's an exotic effect, but in principle it's highly compatible with traditional electronic devices."

Quantum materials


Unlike silicon, samarium nickelate and other correlated oxides are quantum materials, meaning that quantum-

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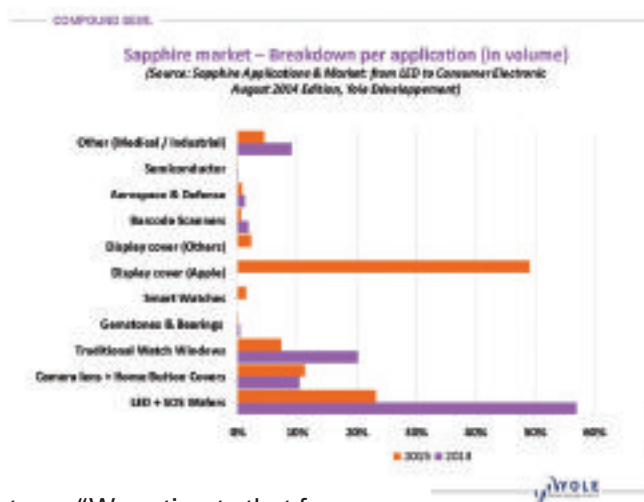
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sapphire as the display cover in this year iteration of its iPhone. An important feature of the design of the new iPhone is that the case doesn't wrap around the display cover. To protect the edges and, more specifically the corners, the part features a complex shape with smooth curves. This design resulted in fairly low finishing yields with sapphire which drove the cost to above \$40 per part.

Apple focused the show on the long anticipated smart watch, announced in three customizable versions named "Apple Watch", "Apple Watch Sport" and "Apple Watch Edition". Both the "Watch" and "Edition" versions feature a sapphire display cover on the front. On the back, a zirconia ceramic cover with four sapphire lenses protects a heart rate sensor. The "Sport" model however relies on strengthened ion-exchange glass for the display cover and the lenses. The watches come in 2 case sizes of 38 and 42 mm. The sapphire display cover is a 2.5D design with a surface curved toward the edges that blends in smoothly with the watch case.



"We estimate that for the largest model, those covers are manufactured from long sapphire bars of 40 x 34 mm cross section sliced at a pitch of about 1.8 mm," said Dr Eric Virey, Senior Analyst at Yole Développement. "The 4 lenses on the back appear to have dimensions fairly similar to the one featured on the iPhone camera lens cover," he adds. The watches however won't be available until "early 2015."

This raises the question of the status of GTAT mega-sapphire plant in Mesa, Arizona. The company might have to wait another year for an opportunity of a design win in the next iPhone. On a positive side, the company and the downstream supply chain might use this additional time to debottleneck

their process and possibly take the "Hyperion" lamination technology from advanced R&D to a manufacturing-ready level that could bring a real disruption in the way to use sapphire in displays.

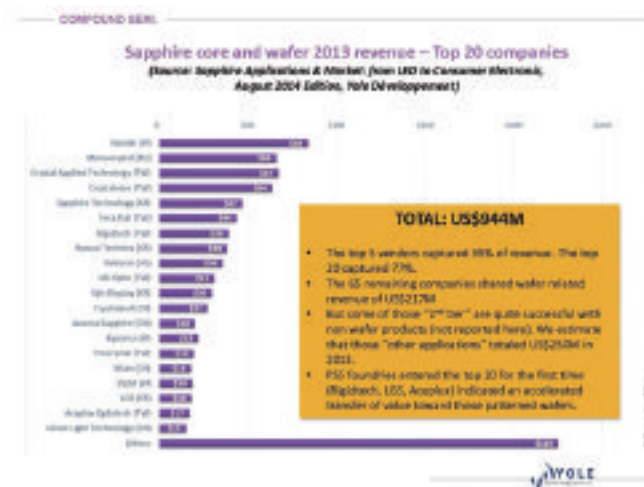
But for now, smart watches won't provide enough upside to hit initial revenue targets. Apple currently sources

sapphire for this product from multiple suppliers, most located in China. "Even if GTAT was supplying a significant fraction of Apple smart watches, we estimate that total revenue derived from this opportunity wouldn't exceed \$45m in 2014, far from the company's initial revenue guidance for its sapphire business," said Eric Virey. "If Apple wants to help GTAT, it could also shift more of its other sapphire needs away from its current suppliers.

Under those circumstances, it will also be interesting to see if GTAT revises guidance for 2014 and if it receives the last US\$139M installment of the \$578M of prepayment promised by Apple before the end of the year. If so, this would show that Apple still supports GTAT and the overall project. GTAT was initially expected to start paying back this sum over quarterly installments starting in 2015 and we'll also see if Apple tries to enforce this," he commented.

Apple has nevertheless generated a lot of excitement in the sapphire industry since the announcement of its partnership with GTAT. It remains to be seen if, after adopting sapphire for the camera lens cover in 2012 and in the home button in 2013, the Apple Watch announcement is the last stop or just another step of the journey. Various OEMs have recently introduced smartphones featuring sapphire display covers. Kyocera introduced its sapphire Brigadier to the US Market in August and on September 4th, Huawei announced its "P7 Sapphire edition."

Xiaomi, a fast growing Apple competitor on the Chinese market also plans a limited edition featuring sapphire.



Continued from page 5

operating assembly and test facilities in Cebu, Philippines and Suzhou, China," said Mark Thompson, Fairchild's chairman and CEO.

In its official release, Fairchild said these cuts are a part of Fairchild's ongoing initiative to enhance manufacturing capabilities, improve product quality, and lower costs resulting in greater supply chain flexibility and responsiveness for our customers.

Closures of both facilities and Fairchild's remaining five-inch wafer fabrication lines in Bucheon, South Korea, are planned to occur from Q2 to Q4 2015.

"An adaptive supply chain must be the foundation of any global manufacturer's operations in the increasingly dynamic semiconductor solutions market," said Mr. Thompson. "The realignment we are announcing

will maximize the utilization of eight-inch factories and reduce the complexity of our manufacturing footprint, while creating the flexibility to support ongoing customer demand through a greater use of external manufacturing sources. Fairchild will continue operating eight-inch wafer fabrication lines in South Portland, Maine and Mountain Top, Pennsylvania, as well as the Bucheon six- and eight-inch fabrication lines."

Through the combined actions, Fairchild expects to incur approximately \$36 million in cash restructuring and other costs. The company also plans to record during the closure process non-cash charges of approximately \$25 million for accelerated depreciation. Once completed, the company expects to realize annual savings of approximately \$45 to \$55 million from a second quarter of 2014 financial baseline. Of these estimated savings, approximately 75 percent are expected to be cash savings, with the balance attributable to lower depreciation costs. ▶

To the exception of Kyocera's Brigadier, which specifically targets the market of rugged smartphone, most of those announcements were intended at testing the market and showing capabilities ahead of a possible Apple announcement. None will come anywhere close to the iPhone in term of volume potential.

This September 9th event might therefore signals the death of sapphire as a display cover in smartphones. But after the tremendous buzz generated by the Apple and GTAT partnership, and following the positive reviews received by the first sapphire smartphones, the lack of a "sapphire iPhone" announcement might instead create a vacuum that Apple competitors will be eager to fill before Apple potentially enters the market.

"In any case, 2015 will be a pivotal year: the idea of using the material for smartphones display covers will either materialize in multiple devices and transform the industry, or just crash and burn," Eric Virey concluded. ▶

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mechanical interactions have a dominant influence over the material properties—and not just at small scales.

"If you have two electrons in adjacent orbitals, and the orbitals are not completely filled, in a traditional material the electrons can move from one orbital to another. But in the correlated oxides, the electrons repulse each other so much that they cannot move," Ramanathan explains. "The occupancy of the orbitals and the ability of electrons to move in the crystal are very closely tied together—or 'correlated.' Fundamentally, that's what dictates whether the material behaves as an insulator or a metal."

Ramanathan and others at SEAS have successfully manipulated the metal-insulator transition in vanadium oxide, too. In 2012, they demonstrated a tunable device that can absorb 99.75% of infrared light, appearing black to infrared cameras.

Similarly, samarium nickelate is likely to catch the attention of applied physicists developing photonic and optoelectronic devices.

"Opening and closing the band gap means you can now manipulate the ways in which electromagnetic radiation interacts with your material," says Jian Shi, lead author of the paper in *Nature Communications*. He completed the research as a postdoctoral fellow in Ramanathan's lab at Harvard SEAS and joined the

faculty of Rensselaer Polytechnic Institute this fall. "Just by applying an electric field, you're dynamically controlling how light interacts with this material."

Further ahead, researchers at the Center for Integrated Quantum Materials, established at Harvard in 2013 through a grant from the National Science Foundation, aim to develop an entirely new class of quantum electronic devices and systems that will transform signal processing and computation.

Ramanathan compares the current state of quantum materials research to the 1950s, when transistors were newly invented and physicists were still making sense of them. "We are basically in that era for these new quantum materials," he says. "This is an exciting time to think about establishing the basic, fundamental properties. In the coming decade or so, this could really mature into a very exciting device platform."

You Zhou, a graduate student at Harvard SEAS, was co-lead author of the paper in *Nature Communications*. The research was supported by grants from the National Science Foundation (NSF) (CCF-0926148) and the National Academy of Sciences, as well as an NSF Faculty Early Career Development (CAREER) Award to Prof. Ramanathan (DMR-0952794). ▶

Intel Announces EMIB

Intel recently announced that a new technology “Embedded Multi-die Interconnect Bridge” or EMIB will be available to 14nm foundry customers.

They claim it is a “... lower cost and simpler 2.5D packaging approach for very high density interconnects between heterogeneous dies on a single package.” While neither Intel nor any initial press reports gave any indication of exactly what this means, it is highly likely that this is tied to the issuance of patent application publication US 2014/0070380 A1 published March 13 2014.

In simplified form interconnect bridges (“silicon glass or ceramic”) are embedded in a laminate substrate and connected with flip chip as shown in

FIGURE 1:

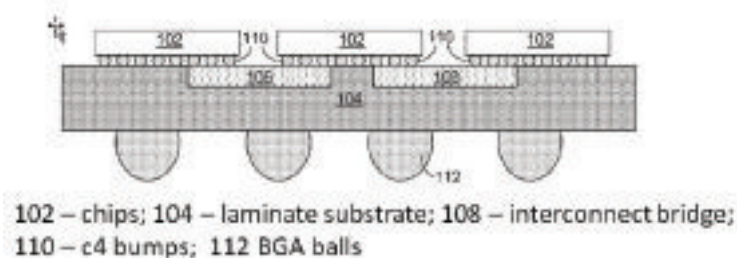


FIGURE 1. Bridge interconnect as described in recent Intel patent.

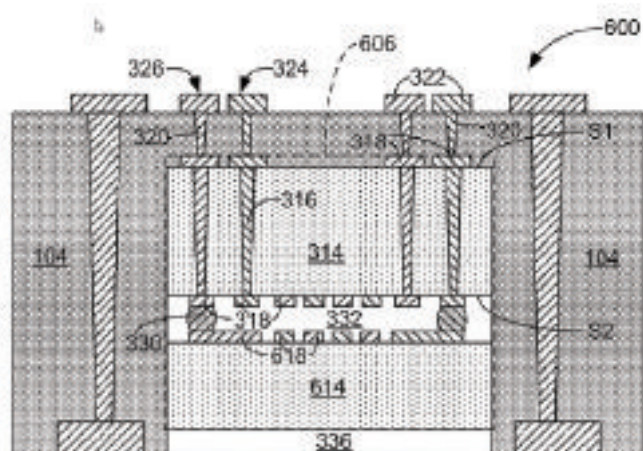


FIGURE 2. Intel EMIB Module in cross-section

Packaging



A cross section of the package (**FIGURE 2**) is more revealing showing connections through the laminate and connections through the bridge substrate (316) which would be TSV in the case of a silicon bridge substrate. The underside of the bridge substrate (314) may be connected to another bridge substrate for further interconnect routing as shown below.

While there is no silicon interposer, there do appear to be TSV in the embedded interconnect substrate as shown below. While removing complexity from the IC fabrication by eliminating TSV from the foundry process, the packaging operation becomes much more complex.

Since the 2.5D interposer has been reduced in size to the interconnect bridges, this may reduce cost, but will increase signal length vs a true 3D stack or a silicon interposer 2.5D.

While Intel released the following description: “Instead of an expensive silicon interposer with TSV (through silicon via), a small silicon bridge chip is embedded in the package, enabling very high density die-to-die connections only where needed.” I think this is somewhat misleading.

The packaging analogy to what they have done is as follows: A high density bumped chip could be put down on to a high density build up PWB, but in most cases the high density bumped chip is placed on a smaller BGA substrate which is then put onto a lower density, lower cost PWB. The latter is the lower cost solution. In this case, large expensive high density interposers are avoided, and the much smaller EMIB are used for the high density interconnect. It will be interesting to see what if any the cost differential will be here.

Intel also announced the availability of its High Density Modular Test (HDMT) platform. HDMT, a combination of hardware and software modules, is Intel’s test technology platform that, until now, was only available internally for Intel products. It is now available to customers of Intel Custom Foundry. ◀



Dr. Phil Garrou,
Contributing Editor

EUV and mask complexity

EUV and mask complexity were the hot topics at this year's SPIE Photomask Technology conference in Monterey, Calif.

Extreme-ultraviolet lithography systems will be available to pattern critical layers of semiconductors at the 10-nanometer process node, and EUV will completely take over from 193nm immersion lithography equipment at 7nm, according to Martin van den Brink, president and chief technology officer of ASML Holding.

Giving the keynote presentation, Martin offered a lengthy update on his company's progress with EUV technology.

Sources for the next-generation lithography systems are now able to produce 77 watts of power, and ASML is shooting for 81W by the end of 2014, Martin said.

The power figure is significant since it indicates how many wafers the litho system can process, a key milestone in EUV's progress toward becoming a volume manufacturing technology. With an 80W power source, ASML's EUV systems could turn out 800 wafers a day, he noted.

The goal is to get to 1,000 wafers per day. ASML has lately taken to specifying throughput rates in daily production, not wafers per hour, since many wafer fabs are running nearly all the time at present.

ASML's overarching goal is providing "affordable scaling," Martin asserted, through what he called "holistic lithography." This involves both immersion litho scanners and EUV machines, he said.

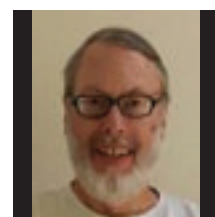
Martin offered a product roadmap over the next four years, concluding with manufacturing of semiconductors with 7nm features in 2018.

The ASML president acknowledged that the development of EUV has been halting over the years, while asserting that his company has made "major progress" with EUV. He said the EUV program represented "a grinding project, going on for 10 years."

For all of EUV's complications and travails, "nothing is impossible," Martin told a packed auditorium at the

Monterey Conference Center.

With many producers of photomasks in attendance at the conference, Martin promised, "We are not planning to make a significant change in mask infrastructure" for EUV. He added, "What you are investing today will be useful next year, and the year after that."



Jeff Dorsch,
Contributing Editor

SPIE panel tackles mask complexity

Photomasks that take two-and-a-half days to write. Mask data preparation that enters into Big Data territory. And what happens when extreme-ultraviolet lithography really, truly arrives?

These were among the issues addressed by eight panelists in a session "Mask Complexity: How to Solve the Issues?" The panelists were generally optimistic on prospects for resolving the various issues in question. Dong-Hoon Chung of Samsung Electronics said solutions to the thorny challenges in designing, preparing, and manufacturing masks were "not impossible."

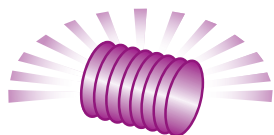
Bala Thumma of Synopsys said he was "going to take the optimistic view" regarding mask-making challenges. "Scaling is going to continue," he added.

"We are not at the breaking point yet," Thumma said. "Far from it!" Electronic design automation companies like Synopsys will continue to improve their software tools, he asserted. Mask manufacturers will also benefit from "strong partnerships" with vendors of semiconductor manufacturing equipment, and "strong support from semiconductor companies," he said.

To resolve the issue of burgeoning data volumes in mask design and manufacture, Suichiro Ohara of Nippon Control System proposed the solution of a unified data format – specifically MALY and OASIS.MASK software. Shusuke Yoshitake of NuFlare Technology later said, "OASIS is gaining, but GDSII still predominates."

Several panelists took the long-term view and looked beyond the coming era of EUV lithography to when multiple-beam mask writers and actinic inspection of masks will be required. EUV and actinic technology, it was generally agreed, will arrive at the 7-nanometer process node, possibly in 2017 or 2018. ♦

Semiconductors





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- RR Solution Syntheses of Inorganic Functional/Multifunctional Materials
- SS Oxide Thin Films and Nanostructures for Advanced Electrical, Optical and Magnetic Applications
- TT Metal Oxides—From Advanced Fabrication and Interfaces to Energy and Sensing Applications
- UU Titanium Oxides—From Fundamental Understanding to Applications
- VV Science and Technology of Superconducting Materials
- WW Ultrafast Dynamics in Complex Functional Materials
- XX Multiscale Modeling and Experiments on Microstructural Evolution in Nuclear Materials
- YY Insights for Energy Materials Using *In-Situ* Characterization
- ZZ Materials Information Using Novel Techniques in Electron Microscopy

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SEMICON Europa heads to Grenoble

PETE SINGER, Editor-in-Chief

All parts of the semiconductor supply chain will come together at the ALPEXPO center in Grenoble, France.

SEMICON Europa will be held in France for the first time, on October 7-9, in Grenoble. Located in south-eastern France, at the foot of the French Alps, Grenoble is one of the most important scientific centers in Europa, home to CEA-Leti, Soitec and the GIANT innovation campus (Grenoble Innovation for Advanced New Technologies). It's also home to the iconic "bubble" cable cars shown on this issue's cover.

Heinz Kundert, president of SEMI Europe, said the show has evolved from just being a place for buyers and sellers of equipment and materials to meet. "We have adapted the entire SEMICON format to allow the entire supply chain to come together in different ways. It's a rebirth of SEMICON in Europe," he said. "We are trying to really understand the supply chain as a total concept and what needs to be changed to be successful in the future."

The show will feature an expanded exhibition (40 percent larger) and a conference of more than 70 sessions with 300 speakers.

In addition to a new "Innovation Village" that will showcase 35 European start-ups, the event host the 18th Fab Managers Forum, which is themed "Improving Productivity for Mature Fabs." Speakers from imec, Infineon AG and Bosch will present on Internet of Things, Automation Level in Fabs, and Smart Connected Sensor Devices.

The prospect for future 450mm wafer processing,



Heinz Kundert hands a 450mm wafer to European Commission vice president Neelie Kroes.

as well other technical and business challenges in semiconductor and related micro and nano-electronics industries, will also be addressed. In a two-day special program, "450mm Innovations and Synergies for Smaller Diameters," leaders will present on progress, research, and collaboration on the future of the semiconductor manufacturing. The session includes presentations from Global 450 Consortium, European Commission, ASM Europe BV, and RECIF Technologies.

In addition, a Secondary Equipment Session, themed "Fundamental to European Competitiveness?" will feature presentations from Infineon Technologies AG, STMicroelectronics, and Robert Bosch GmbH.

Other conference programs at SEMICON Europa will explore critical issues in Fab Management, Advanced Packaging, 3DIC, Test and MEMS.

Growth in Europe

The European semiconductor equipment market is expected to grow along with the world market. Global capital spending on semiconductor equipment is projected to grow 21.1 percent in 2014 and 21.0 percent in 2015. According to the August edition of the SEMI World Fab Forecast, semiconductor equipment spending will increase from \$29 billion in 2013 to \$42 billion in 2015.

SEMI projects back-to-back years of double-digit growth in Europe and Mid-East semiconductor equipment sales. The SEMI outlook forecasts that the European/Mid-East semiconductor equipment market will grow 11 percent in 2014 (reaching \$1.9 billion) and 100 percent in 2015 (reaching \$3.8 billion). In terms of percentage of worldwide sales, the Europe/MidEast region's share is expected to increase from 5.9 percent in 2013 to 9.0 percent in 2015.

Kundert notes that Europe is home to a diverse set of semiconductor manufacturing companies, including Intel (in Ireland), Infineon (which is in the process of buying International Rectifier), GlobalFoundries (in Dresden), STMicroelectronics and Bosch. This diversity makes Europe well-suited to tackle the Internet of Things and More-than-Moore. "It's a big challenge, but we believe if somebody can manage it successfully, it's Europe. We are very experienced in those types of applications," Kundert said.

Europe is home to many leading semiconductor research groups, including imec, CEA-Leti and Fraunhofer. These groups are supported by a variety of government efforts, including the "10-100-20" effort announced last year by European Commission vice president Neelie Kroes (see photo) and supported by SEMI.

10-100-20 is an ambitious strategy to double the economic value of semiconductor production in Europe in the 2020-2025 timeframe. This will be achieved by an unprecedented public/private investment partnership with 10 billion Euros in public/private funding and 100 billion Euros from the industry.

The roadmap, published on 14 February 2014, was drafted by the Electronic Leaders Group (ELG), that was set up by the European Commission and consists of: ARM, ASML, CEA, Fraunhofer, Globalfoundries, imec, Infineon, Intel, NXP, SOITEC, STMicroelectronics (A

copy can be downloaded from <http://www.semi.org/eu/node/8506>). There's been good progress, but Kundert cautioned that "such an initiative takes time."

Another notable effort is the new Industry 4.0 (or "industrie 4.0") out of Germany, which aims to define the fourth industrial revolution. The first industrial revolution was the mechanization of production using water and steam power, it was followed by the second industrial revolution which introduced mass production with the help of electric power, followed by the digital revolution, which was the use of electronics and IT to further automate production. "In the project, semiconductor technology plays an important role. Industry 4.0 or the fourth industrial revolution could be a reality in about 10 to 20 years," Kundert explained. "Germany is pushing extremely strong right now to build on semiconductors," he added.

"All in all, we see increased activity in national and local government initiatives," Kundert said.



SEMICON Power

For the first time, SEMICON Europa 2014 will offer two new power-related technical forums: Power Electronics Conference and Low Power Conference. Energy efficiency is a key challenge and advances in power microelectronics, batteries, mobility, and energy harvesting systems are making power management smarter to reduce energy consumption. The two new power conferences focus on how innovators and their technologies are building energy-optimized applications.

The theme of the Low Power Conference is "Highly Energy Efficient Nanotechnologies and Applications." The number of connected electronics devices is

35 European start-ups showcased at Innovation Village



At SEMICON Europa, attendees and exhibitors will delve into the technologies that shape the future of the microtech, nanotech, medtech and cleantech industries. Representing the entire supply chain from materials to electronic systems and services, 35 major European start-ups will participate in the Innovation Village and present their new technologies.

Innovation Village consists of a start-up exhibition (7-9 October), Silicon Innovation Forum (7 October) and Innovation Conference (8 October). As part of the Silicon Innovation Forum, all selected start-ups will have the opportunity to “pitch” to investors and SEMICON Europa visitors. The pitch session will be followed by a start-up panel discussion “Fundraising for the Future Champions of European Electronics,” led by Jean-Pascal Bost of SATT-GIFT with panelists: Jacques Husser (Sigfox), Eric Baissus (Kalray), Serguei Okhonin (ActLight) and Mike Thompson (Hotblock Onboard).

The Innovation Conference, sponsored by Fidal Innovation, will feature keynote speakers such as Nicolas Leterrier (Schneider Electric) on Innovation Practices and Dan Armbrust (Silicon Catalyst) on Lean Innovation. Christine Vaca (Gate1) will act as the conference chair.

“For the inaugural SEMICON Europa in Grenoble, our team was intent on developing a program that would highlight the strength of the local and the European ecosystems in innovation and new technology,” explains Anne-Marie Dutron, director

of the SEMI Grenoble office. “At Innovation Village, visitors will discover the creativity of 35 European start-up companies, presenting their products, partnership and investment opportunities.”

Participating start-ups were chosen by a selection committee which included ten of the most recognizable venture firms in the industry: Applied Ventures LLC, Robert Bosch Venture GmbH, TEL Venture, 3M Ventures, CEA Investissement, Samsung Ventures, Air Liquid Electronics, ASTER Capital, VTT Ventures, and Capital-E.

Start-ups include ActLight (Switzerland), BlinkSight (France), BluWireless Technology (UK), Calao-Systems (France) and Silicon Line (Germany). For more information about Innovation Village, participating start-ups or about the Innovation Conference, please visit the SEMICON Europa website: www.semiconeuropa.org/Segments/InnovationVillage

All events in Innovation Village, including the three-day start-up exhibition, Silicon Innovation Forum and Innovation Conference will be available at no charge for all SEMICON Europa guests and visitors.

Silicon Line

The company is a provider of ultra-low power optical link technology for mobile and consumer electronics markets. Silicon Line products enable power-efficient optical transportation of video, images, voice and data at the multi - gigabit speeds demanded by both today and tomorrows digital consumer lifestyles. The company is VC founded since 2007.

Nessos Information Technologies SA

Nessos is a software development company that targets custom integrated solutions with advanced software engineering requirements. Nessos' self-financed research and development department is focused on Big Data/ Big Computation applications and mobile services. The company's paiRing is its latest research and development product. It is a smart ring that enables you to instantly share your feelings, your mood and words of love with your significant other. The paiRing is described as an "elegant ring" which connects wirelessly with paiRing apps-enabled smartphone, offering various ways of communication.

eVaderis

The company offers energy efficient, low power mixed-signal data-centric control processors combining silicon technologies and disruptive non volatile resistive memories (NVRM).

The company will sell these products to wireless Machine to Machine (M2M) system integrators, serving the long - term battery volume - intensive smart sensors, data loggers, wearable computers markets, and more generally, the exploding market of the Internet of Things (IoT).

Wavelens

Wavelens is developing disruptive optical MEMS solutions aimed at improving cameras image quality by making easier the integration of optical functions such as autofocus, image stabilization and zoom.

ActLight SA

The company is focused on the field of CMOS photonics, developing new type photodetectors and improving photovoltaic energy harvesting technology. ActLight is a fabless company, specializing in the Intellectual Property (IP) of these areas. It also provides supporting services like design and technology advice for its customers.

Irlynx

Irlynx is a French start-up based in Grenoble that develops and commercializes infrared sensors to detect and characterize human being activity at lower cost while respecting private life. Thanks to a unique infrared detection technology, the Irlynx optoelectronic modules, which embed pre-processing image algorithms, speed up time to market of more innovative and interactive products.

Pollen Technology

POLLEN Technology is a software company that provides a product portfolio dedicated to easy and safe nanomaterials production and integration. Its products integrate the latest ISO regulations to ensure traceability and environmental/health security. Adaptative technology is covering a large scope from semiconductor industry, cosmetics, chemistry and automotive.

Exagan

Exagan is a supplier of GaN-based transistor devices for power supply, electrical automotive, solar panel and industrial application. With a unique and proprietary technology, Exagan is accelerating transition of power electronics industry towards more efficient production and conversion systems to reduce CO2 emission, by enabling large scale adoption of GaN-on-Silicon power technology.

AVALUN SAS

Created in 2013, the company currently offers the LabPad, a mobile point-of-care (POC) device. As rapid In Vitro Diagnostic (IVD) is a fast-growing market, LapPad technology responds to a demand for a tool designed to carry out multiple tests. LapPad allows for patients to be monitored at home or during an emergency and more generally, assists healthcare professionals (doctors, pharmacists, nurses), whom practice would be clearly incompatible with a plethora of different instruments. Using the same imaging components as a smartphone to create a fully integrated miniature microscope, LabPad is a portable minilab that can perform many tests on the same device, such as blood coagulation, glucose or cholesterol. A patient or a healthcare professional just needs to insert the appropriate micro-cuvette in the device, draw a droplet of blood from the patient's finger and deposit it on the micro-cuvette. It allows for a number of medical tests to be taken by one single instrument. The development of this technology is the result of over 10 years of research at CEA-Léti.

Noivion

Noivion developed and patented a new thin film deposition technique named Ionized Jet Deposition (IJD). IJD is an electron ablation technology that offers advantages in terms of film quality and stoichiometry conservation combined with high productivity, competitive cost and industrial scalability. IJD sources and equipment have the unique capability to enable mass production of complex compounds coatings by a quick and single deposition step opening new opportunities for the semiconductor manufacturing industry. Successful applications include CIGS and YBCO deposition. IJD is also an ideal solution for the deposition of high melting point metals, TCOs, hard oxides, nitrides, carbides that are feasible by non reactive or reactive process with high target utilization. IJD sources are available now as prototypes to selected users. The release of a commercial version is expected within 2014. The company says that it believes in 5 years IJD can become a mature thin film industrial manufacturing solution.



CALAO Systems

CALAO Systems is the specialist of onboard connected computers based on ARM processor architecture and Linux open source software, integrating electronic technologies and telecommunications. Calao - system offers an easy access for electronic specialist - or not - of high-tech products, to customers that operate in the industrial market, M2M and the Internet of Things. The company is headquartered in Grenoble.

Heyday

Heyday Integrated Circuits concepts and develops semiconductor ICs for the power conversion market. Heyday IC products increase integration, reduce component count and improve performance of AC-DC and DC-DC power conversion products.

Smoltek AB

Smoltek offers a proprietary conductive nano - scale carbon technology tailored to support the future needs of the semiconductor industry.

PETsys Electronics - Medical PET Detectors, S.A.

HPETsys Electronics SA developed new PET detectors for next generation of medical PET scanners, enabling high resolution images and increased sensitivity, at lower cost, for early cancer detection and monitoring. This is a major step in the fight against cancer. The company is now selling our patent pending ASIC's evaluation kit. The company has already secured 1 million Euros, and says another 1 million Euros is needed for the next 18 months phase (starting in May 2015), after which it will be self-sufficient.

Scint-X

The company develops structured scintillators. Partnering with leading manufacturers of x-ray detection systems, it is in the process of transforming digital x-ray detection systems so as to produce images with unprecedented levels of resolution and contrast. The technology is primarily used in markets such as Medical (Mammography, General Medical & Dental), Security (Non Destructive Test) and Industrial applications. Currently scintillators are so called needle scintillators which are grown from a CsI material base. Scint-X has developed a structured scintillator using MEMS deep Si DRIE technologies to create a honeycombed structured scintillator combined with a highly reflective mirror finish on the sidewalls thereby increasing the x - ray absorption for significantly better DQE and MTF. This gives up to 4x improvement in contrast and 2x improvement in resolution.

Grapheat

Grapheat is a young startup specialized in the production and integration of monolayer high - quality of graphene on wafers and substrates for specific applications. We especially target production of transparent, conducting and flexible electrodes. The company also offers customized solutions for integration of graphene in prefabricated structures by innovative lamination techniques.



Gridbee Communications

Gridbee Communications is developing innovative long range mesh network solution for connected objects. The solution is fully standard, auto-configurable, auto-scalable and auto-manageable.

Enerstone

Enerstone works with rechargeable battery manufacturers and integrators to improve the charge quality of their batteries, providing a considerable competitive advantage on the commodity battery market. Its battery management technology and proven expertise in battery optimization can help rechargeable battery manufacturers and integrators preserve the initial factory capacity of their batteries charge after charge, for better performance and lower overdesign costs.

Nocilis Materials

Nocilis Materials AB offers various silicon based semiconductor materials, including SiGeSnC alloys for various photonic applications and silicon photonic integrated circuits. Nocilis also offers bandgap engineered material SGOI and GOI as substrates or for RF&MW applications.

growing exponentially. According to Jean-Marc Chery, COO STMicroelectronics, to sustain this growth, the semiconductor industry needs a real breakthrough in energy efficiency — both for connected devices and for the communication infrastructure. At the same time, the traditional planar bulk CMOS technology is plateauing in power consumption and performance beyond 28nm, so breakthrough solutions for energy efficient systems are mandatory to continue the growth.

Sessions include: Market Analysis; Technology Energy Efficiency; Processors; Energy Efficient Design; Energy Efficient EDA Tools; and Applications. Speaker highlights include:

- STMicroelectronics: Jean-Marc Chery, COO
- GLOBALFOUNDRIES: Manfred Horstmann, director, Products and Integration
- Qualcomm Technologies: Mustafa Badaroglu, senior program manager
- Cadence Design Systems, Inc.: Marcus Binning, senior AE manager
- IBS, Inc.: Handel Jones, CEO,
- Hewlett-Packard: Rémi Barbarin, CTO
- Schneider Electric: Gilles Chabanis, manager, Pervasive Sensing

The Power Electronics Conference is themed “The Ultimate Path to CO₂ Reduction.” Modern power semiconductors play an essential role in energy conservation and worldwide CO₂ reduction. Philippe Roussel, business unit manager at Yole Developpement, will present the keynote on market and technology overview of the Power Electronics industry, including a look at the impact of Wide BandGap (WBG) Devices. He believes that the emergence of new WBG technologies such as SiC and GaN will reshape the established power electronics industry, especially on the high-voltage side. SiC and GaN offer benefits (higher frequency switching, power density, and more) that may dramatically help improve the power conversion efficiency. Yole believes that this could lead to lower CO₂ emission if both SiC and GaN can emerge from labs to mass production. SiC transitioned a few years ago and GaN is starting the commercialization curve. By 2020, WBG devices are expected to generate more than \$1 billion according to Yole.

The session highlights include:

- Applications session — speakers from CEA/LETI,

EpiGaN, European Center for Power Electronics e.V. (ECPE), Infineon, European Commission, Renault, and Supergrid Institute.

- Technology and Materials session — presenters from Fairchild, Infineon Technologies AG, SiCrystal AG, Siltronic AG, Soitec, ST Catania, and Yole Developpement.

Imaging without limits

The Imaging Without Limits Conference will address the rising demands of imaging systems in mobile, medical, automotive and other technology applications. Until recently, the imaging market was based primarily on mobile phone based applications. However, new technologies for imaging-based applications are now being introduced — including wearable electronics (e.g. smart watches), automotive, tablets, machine vision, security and surveillance, and medical applications.

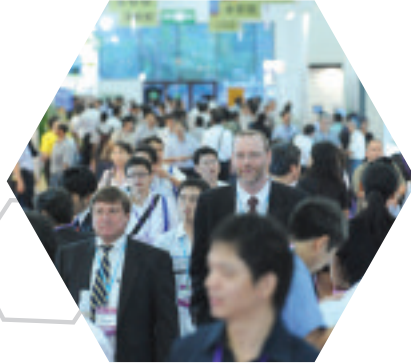
Covering a broad range of imaging systems, the two-day conference will explore the promise of imaging-related systems, existing applications and new applications and technologies now on the horizon. Keynote speakers include Eric Fossum, Dartmouth University and the father of CIS, and Pascal Brosset, chief innovation officer of Schneider Electric. The first day will address applications (mobile, automotive, industrial, medical) and technologies (sensors, optics, processing and packaging) while the second day will delve into specific implementation techniques.

According to Yole Developpement, the CMOS Image Sensor (CIS) market is expected to grow at a 10 percent CAGR in revenue in the five-year period from 2013 to 2018, growing from US\$ 7.8 billion in 2013 to \$12.8 billion in 2018. While many applications drive the integration of CMOS image sensors, mobile phones accounted for approximately 66 percent of total shipments in 2013. But other new applications — including tablets and automotive — are set to drive the future growth of this industry. Tablets also significantly contribute to the market growth with a 17 percent CAGR over 2013-2018.

The next wave of imaging will likely focus on automotive applications because additional image sensors are necessary for many of the safety improvements required by new government regulations. CAGR for CIS automotive applications is expected to

without
limits.

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increase 36 percent between 2013 and 2018. Yole states that the market is “expected to reach about \$700 million in 2018, and will drive the need for high-performance sensors: global shutter, high dynamic range, and high sensitivity. The requirements of the automotive market are hence completely different from the mobile phone market, which is still in the race for higher resolution and smaller pixels.”

In addition, Yole also sees several other applications with a high CAGR, including wearable devices (103 percent), machine vision (33 percent), and camera pills (32 percent).

Key companies involved in the imaging conference and exposition include: ARM, Asia Optical-EtherO, Audi, European Space Agency, French Institute of Vision, Hamamatsu, Heptagon, Microsoft, Schneider, Sofradir and STM. Many research centers are also involved — CEA-LETI, CSEM, Fondazione Bruno Kezler, Fraunhofer Institut, Grenoble University Hospital, and more. Start-up and SMEs involved in the conference include: Aldebaran, Awaiba, CMOSIS, Caeleste, Mesa, Blue Eye Video, ISD, Kaleido, Multix, NikkoIA, NIT, Pyxalis, Yole, and Wavelens.

Plastic electronics

The Plastics Electronics Conference and Exposition, focusing on the latest developments in printed, organic and large area electronics, will co-locate with SEMICON Europa. Plastic Electronics 2014 (PE 2014) is themed “Enabling Applications beyond Limits in Electronics.”

According to analysts, the plastics electronics market is growing rapidly and is expected to reach \$13 billion by 2020 driven by increasing applications in the semiconductor and electronics market. Applications like large area displays, solar panels and printed electronics are now responsible for a substantial portion of the PE market, and emerging applications like OLED, thin-film batteries, and sensors are emerging growth opportunities.

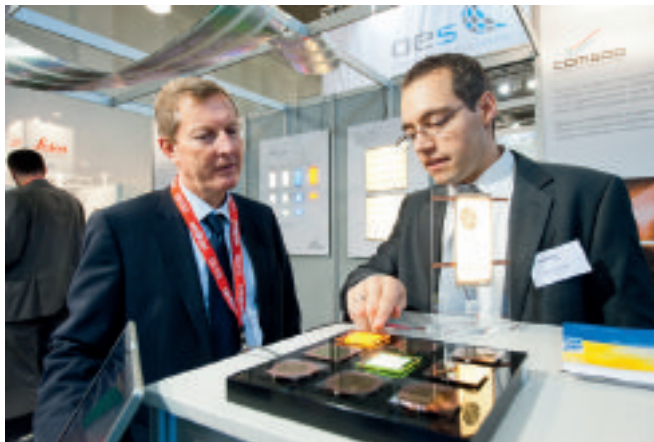
Manufacturability of plastic electronics has made major steps in the last year, moving from research level

to industrial relevance. Still, numerous barriers to commercialization must be overcome — from material development to integration, manufacturing, processing, and assembly issues.

Plastic electronics’ imminent transition from the R&D phase to the industrialization stage is highlighted by several keynote presentations at the PE2014. Fiddian Warman, founder and managing director, SODA, will present on, “How design type approaches can be effective in facilitating innovative technological development and open up new markets and opportunities,” and John Heitzinger, president, Soligie, Inc., will delve into “Advances in Additive Manufacturing of Electronics.”

The exposition and conference cover the entire span of Plastic Electronics — Hybrid and Heterogeneous Integration; Organic Electronics; OLEDs, Displays, and Lighting; and Flexible Photovoltaics — offering the latest developments for engineers, material experts, manufacturing professionals and industry strategists. Highlights are:

- Business Case session — speakers from imec, ISORG, Nokia, Philips Research, Plastic Logic, SODA, STMicroelectronics, Valeo, and Yole Development.
- Manufacturing Panel Discussion on “Building a Leadership Position in PE” — panelists from Bosch, Cambridge, CEA, Joanneum Research, and Ynvisible.
- Manufacturing Session — presenters from Applied Materials, Beneque, CEA Tech, Dupont Teijin Films UK Ltd, Joanneum Research, NovaCentrix, Roth and Rau B.V., Soligie, Universal Laser Systems, Ynvisible — as well as Cambridge University, the European Commission, and VTT (Finland).
- Technologies/Materials Session — features speakers from Arkema, Arizona State University, CEA-LITEN, Corning, Fraunhofer, imec, and Sunchon National University. ◀



Threshold voltage tuning for 10nm and beyond CMOS integration

NAOMI YOSHIDA, KEPING HAN, MATTHEW BEACH, XINLIANG LU, RAYMOND HUNG, HAO CHEN, WEI TANG, YU LEI, JING ZHOU, MIAO JIN, KUN XU, ANUP PHATAK, SHIYU SUN, SAJJAD HASSAN, SRINIVAS GANDIKOTA, CHORNG-PING CHANG and ADAM BRAN, Applied Materials, Santa Clara, CA

A novel metal gate integration scheme to achieve precise threshold voltage (VT) control for multiple VTs is described.

At very small process geometries, precise control of electrical conductivity is difficult to maintain. The industry requires a viable replacement-gate FinFET architecture to continue scaling high performance CMOS [1, 2] technology and designs. Furthermore, cost-effective and precise VT control to achieve multiple VTs is essential for future ULSI fabrication to achieve optimal power consumption and performance.

In this study, using WFM full fill and combining two techniques — the novel metal composition and ion implantation into the WFM process, we successfully realized three critical aspects for the metal gate for 10 nanometer and beyond. These are: 1) precise effective work function (eWF) control over a 600 millivolt (mV) tuning range to achieve multiple VT, 2) maintaining conductivity for a sub-15 nanometer

gate trench, and 3) compatibility to the self-aligned contact (SAC).

A metal oxide semiconductor capacitor (MOSCAP) was used to evaluate the impact of the metal composition and beam line ion implantation on eWF. Ion

implantation was performed for some of the samples after high-k dielectric and work function metal deposition on blanket wafers. High frequency capacitance voltage (HFCV) and current voltage (IV) measurements were recorded for the MOSCAP samples. A single damascene structure was used to measure sub-20 nanometer line resistance. A planar MOSFET was also used for evaluating impact on VT and variability.

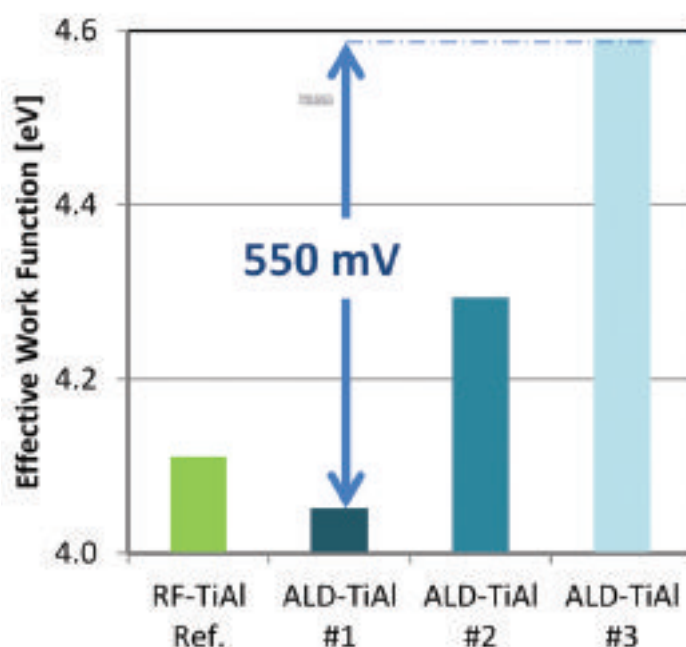


FIGURE 1. nWFM composition impact on eWF.

Work function modulation

FIGURE 1 shows eWF with three compositions of NMOS WF metals (nWFM) compared with RF-PVD titanium aluminum (TiAl) that was used as the nWFM reference metal. Results demonstrated that the difference between the highest and lowest WF was 550 mV and is attributed to the ALD

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TiAl composition. Nitrogen ion implantation into the ALD TiAl enabled further WF tuning by 100-150 mV steps. This made possible a WF range from near the Si conduction band edge of 4.1 electron volts (eV) for NMOS low VT to above mid-gap 4.7 eV. The WF shift corresponded well to the different dose levels; therefore we demonstrated that ion implantation can be used to pinpoint the target WF. In addition, we found that ion implantation into ALD TiAl does not degrade the gate leakage current and effective oxide thickness (EOT) performance.

Maintaining metal gate conductance for 10nm node

According to the ITRS roadmap, a gate length of 17 nanometers is expected for the 10 nanometer technology node [3]. The problem is that after the high-k cap and etch stop depositions, the gate will have limited space left for the metal fill process [4]. One solution is to fully or mostly fill the trench with WF metal. Using an advanced ALD TiAl deposition process, we were able to fill 13 nanometer wide trenches without any gapfill voids.

FIGURE 2 shows the extendible conductance

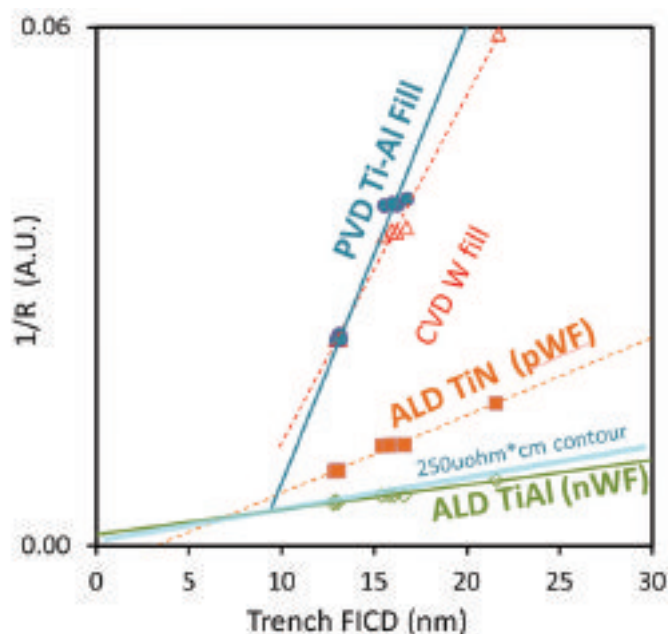


FIGURE 2. Conductance curves of various metals filling small trenches.

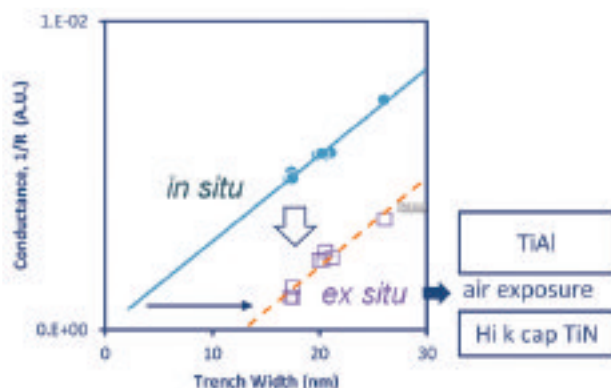


FIGURE 3. Effect of air exposure in between TiN barrier and nWF metal on conductance below 30 nanometers.

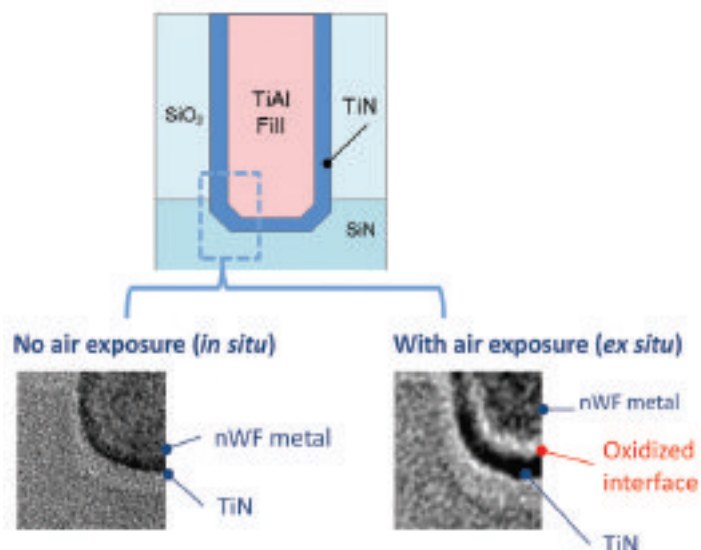


FIGURE 4. TEM images at interface of TiN barrier and nWFM. The ex situ sample shows oxidized interface by air exposure.

of the ALD TiAl and WF fill process.

It is known that NMOS low WF metals are more prone to oxidation than high WF PMOS films such as titanium nitride (TiN) and that air exposure affects VT control [5]. In our study, degradation on the conductance curves from air

exposure was also observed (**FIGURE 3**). The air exposed sample showed a large offset of the conductance curve

to the right while maintaining the slope, i.e. differential resistivity. The TEM (**FIGURE 4**) shows an additional layer between the TiN barrier and ALD TiAl. Scanning transmission electron microscope-electron energy loss spectroscopy analysis confirmed high oxygen in the white interface. Thus, it is critical to have an in situ ALD TiAl process on the high k TiN cap to maintain conductivity for the 10 nanometer node.

Self-aligned contact compatibility and CMOS VT tuning

At the 22 nanometer technology node, a metal gate SAC is necessary to scale contacted gate pitch [1]. This requires a well-controlled etch back of the metal gate, with subsequent capping of the etch

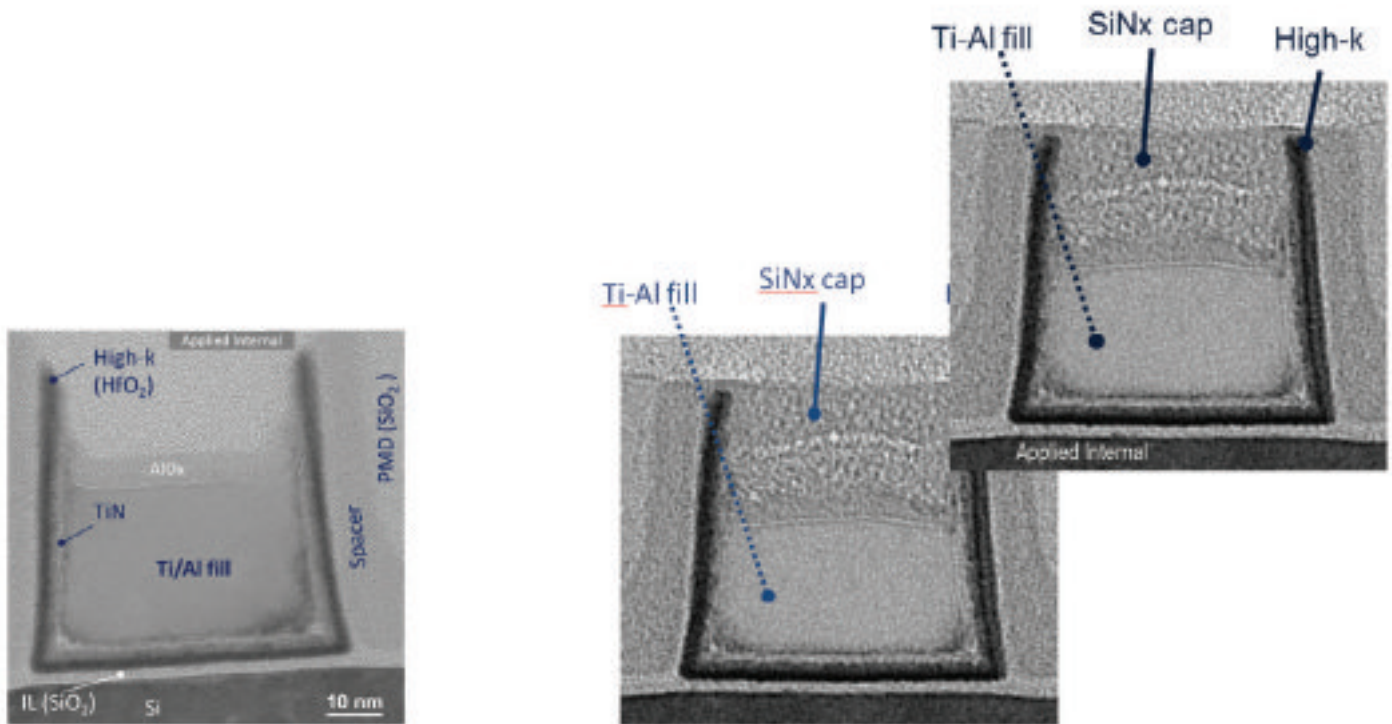


FIGURE 5. Cross-sectional TEM images show controlled etch back of ALD TiAl fill metal gate for SAC integration. The left and middle images after recess etch-back. The right image is after Cap Nitride CMP.

stop material such as silicon nitride (SiN) to prevent contact to gate shorts. Tungsten (W) has been used in volume production because it offers a robust etch back process. In our study, we demonstrated that a controlled recess etch can be achieved with the more conductive TiAl fill compared to W (**FIGURE 5**). In addition, after metal etch back, a SAC cap was successfully formed with a high density plasma (HDP) SiN fill and chemical mechanical planarization (CMP).

Multiple WF metals need to be integrated for CMOS VT tuning for NMOS and PMOS. In our study we examined the CMOS ALD TiAl flow for four VT tunings. From the results, we propose a new process flow: 1) after the high-k and etch stop layer deposition steps, a fully clustered barrier TiN and nWFM be deposited. Some areas can be masked by photoresist (PR) and the exposed area modified by ion implantation. 2) Etch off the first nWFM layer from the PMOS areas. 3) Deposit the second WF (N-3) and barrier. 4) Perform second ion implantation to shift the WF of the third device. 5) Lastly, ALD TiAl is again etched off from the PMOS area WFM (TiN),

followed by W or Al fill to fill the remaining gap. The last TiN material serves as the highest WF as well as the barrier layer for W or Al. This flow provides four VTs and metal fill with a clustered nWFM film stack.

Conclusion

Metal WF modulation for VT tuning using a new scheme tunable in the range of 600 mV was successfully demonstrated for 10 nanometer CMOS integration. Ion implantation dose control enabled continuous WF tuning for multiple VT targets. Metal gate conductance data showed the benefit of in situ processing with a TiN barrier and NMOS WF metal. Based on the results, a CMOS flow with NMOS WF-first was proposed for multi-VT tuning.

References

1. C. Auth et al., VLSI Tech. Sym. Dig., p. 131, (2012)
2. P. Packan et al., IEDM Tech. Dig., p. 659, (2009)
3. ITRS Roadmap 2011 Edition
4. N. Yoshida, et al., VLSI Tech. Sym. Dig., p. 81, (2012)
5. A. Veloso, et al., VLSI Tech. Sym. Dig., p. 33, (2012) ◀

Outlook: Healthy equipment spending into 2015

CHRISTIAN GREGOR DIESELDORFF, SEMI, San Jose, CA

Equipment spending shows strong growth for 2014 and 2015; slow capacity additions

The general consensus for the semiconductor industry is for this year's positive trend to continue into 2015 as both revenue growth and unit shipment growth are expected to be in the mid- to high- single digit range. SEMI just published the World Fab Forecast report at the end of August, listing major investments for 216 facilities in 2014 and over 200 projects in 2015. The report predicts growth of 21% for Front End fab equipment spending in 2014 (including new, used, and in-house), for total spending of US\$34.9

billion, with current scenarios ranging from 19% to 24%.

Front end fab equipment spending is projected to grow another 20% in 2015 to \$42 billion. According to the SEMI World Fab Forecast data, this means that 2015 spending could mark a historical record high, surpassing the previous peak years of 2007 (\$39 billion) and 2011 (\$40 billion).

About 90% of all equipment spending is for 300mm fabs, and, interestingly, the report also shows increased fab equipment spending for 200mm facilities, growing by 10% in 2014. Equipment spending for wafer sizes less than 200mm is also expected to grow by a healthy 12%

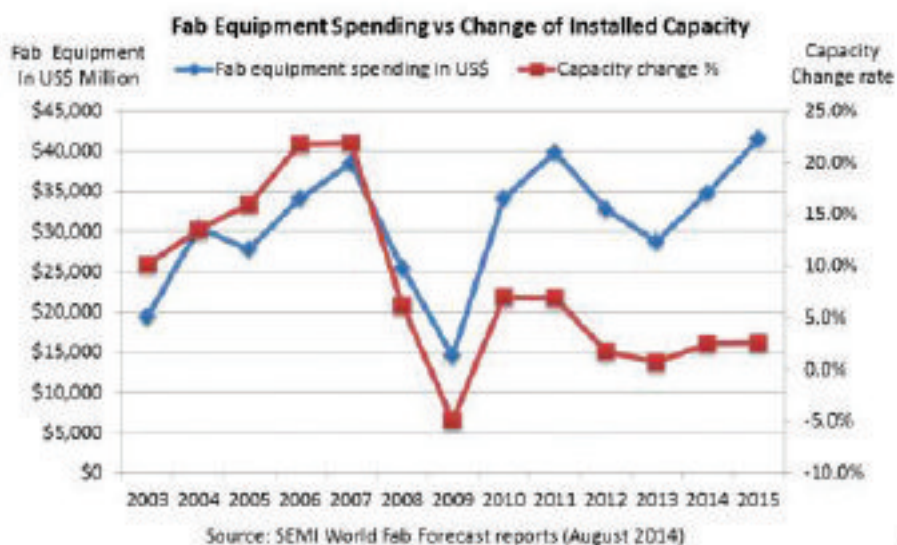


FIGURE 1. Fab equipment spending since 2003 and the change of installed capacity (excluding discretes and LEDs).

in 2015 which includes LEDs and MEMS fabs.

According to the World Fab Forecast, the five regions spending the most in 2014 will be Taiwan (\$9.7 billion), Americas (\$7.8 billion), Korea (\$6.8 billion), China (\$4.6 billion), and Japan (\$1.9 billion). In 2015, the same regions will lead: Taiwan (\$12 billion), Korea (\$8 billion), Americas (\$7.9 billion), China (\$5 billion), and Japan (\$4.2 billion). Spending in Europe is expected to nearly double to \$3.8 billion.

Seven companies are expected to spend \$2 billion or more in 2014, representing almost 80% of all fab equipment spending for Front End facilities. A similar pattern will prevail in 2015.

Worldwide installed capacity falls below 3% mark

As **FIGURE 1** illustrates, before the last economic downturn, most equipment spending was for adding new capacity. The World Fab Forecast report shows that in 2010 and 2011, fab equipment spending growth rates increased dramatically, but installed capacity grew by only 7% in both years. Then in 2012 and 2013, growth for installed capacity sagged even further with only 2% and even less growth. Previously, growth rates less than 2% have been observed only during severe economic downturns (2001 and 2009).

Industry segments, such as foundries, see continuous capacity expansion, though other segments show much lower growth — thus pulling down the total global growth rate for installed capacity to below the 3% mark. Although spending on equipment, some leading-edge product segments experience a loss of fab capacity and, looking closer at this phenomenon, two major trends are observed.

First, coming out of the 2009 downturn, SEMI reports that companies are spending much more on upgrading existing fabs. From 2005-2008, yearly average spending on upgrading technology was about \$6 billion compared to the period of 2011-2015 when the yearly average increased to \$14 billion for upgrading existing fabs. Second, leading-edge fabs experience a loss of capacity when transitioning to leading-edge technology. This is largely observed with nodes below 30/28nm with the increasing complexity and process steps resulting in a -8% to -15% reduction in capacity for fabs.

In addition to foundries, the World Fab Forecast report captures capacities across all industry segments as well as System LSI, Analog, Power, MEMS, LED, Memory and Logic/MPUs. The

Logic/MPU sector is also expected to see some positive capacity expansion for 2014 and 2015. Flash capacity is expected to increase by 4% in 2014. Although we see more DRAM capacity coming online, DRAM is now slowly coming out of declining territory with -3% in 2014 and reaching close to zero by end of 2015.

More DRAM capacity?

Over the past three to four years, some major players (such as Samsung, Micron, and SK Hynix) have switched fabs from DRAM to System LSI or Flash. In addition, other companies stopped DRAM production of some fabs completely,

contributing to declining DRAM capacity.

Equipment spending levels for DRAM fabs in 2012 and 2013 were near the \$4 billion mark annually and are described by some industry observers as being at “maintenance level.” Increased spending is expected for DRAM in 2014 and 2015, yet although

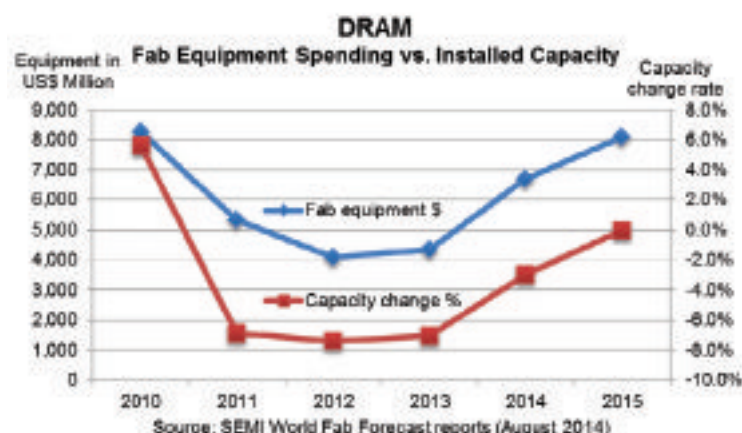
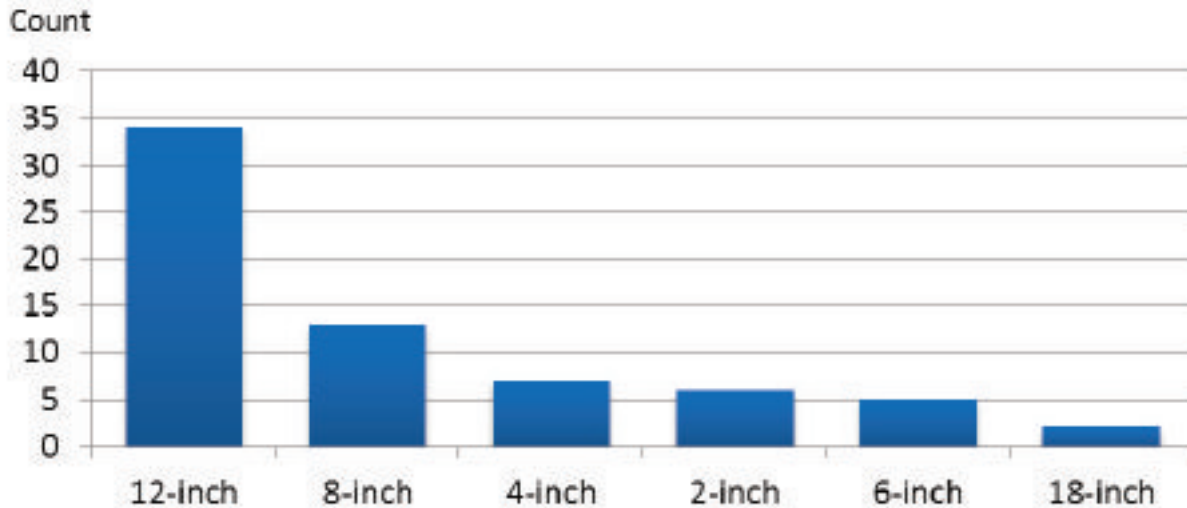


FIGURE 2. Fab equipment spending is compared to the change rate of capacity for DRAM.

more capacity is being added — the rates are still negative until the end of 2015 (**FIGURE 2**).

As discussed above, SEMI reports that leading-edge DRAM fabs undergo a double-digit capacity loss when upgraded due to an increase in processing steps and complexity. Since the end of last year, Samsung is in the process of adding additional DRAM capacity with two new lines — Line 16 (ramping up this year) and its new Line 17 (the first new DRAM fab ramped since the last economic downturn). In addition SK Hynix is ramping up its M14 DRAM line in 2016. We expect the impact to overall DRAM capacity expansion to occur in 2015 when this fab begins to ramp up. Even if this fab ramps to about half of its potential, the change rate for installed DRAM capacity would still not be positive by end of next year.

Future Facilities by Wafer Size Starting Production in 2014 or Later



Source: SEMI World Fab Forecast report (August 2014)

FIGURE 3. Count of known facilities (Volume fabs to R&D) in the World Fab Forecast report with various probabilities which are expected to start production in 2014 to 2020.

Over \$6 billion for fab construction projects

The SEMI World Fab Forecast also provides detailed data about fab construction projects underway. Construction spending is expected to total \$6.7 billion in 2014 and over \$5 billion in 2015. Leading regions in spending for 2014 will be Taiwan, Americas, and Korea. In 2015, the highest spending will be seen in Europe/Mideast, followed by Taiwan and Japan.

Only five companies show strong spending numbers for new fabs or refurbishing existing fabs. Their combined fab construction spending accounts for 88% of all worldwide fab construction spending for Front End facilities.

In 2014, the SEMI report shows 16 new fab construction projects (six alone for 300mm) and 10 fab construction project in 2015 (four for 300mm). Most construction spending in 2014 is for Foundries (\$3.1 billion) followed by Memory (\$2.5 billion) and Logic. In 2015, Memory will have most spending with (\$2.3 billion) closely followed by Foundries (\$2.2 billion).

The report lists currently 1150 facilities with 68 future facilities with various probabilities which have started or will start volume production in 2014 or later (**FIGURE 3**).

As it looks right now, SEMI reports that the outlook is positive for 2014 for the chip-making industry compared to the previous few years and the outlook for 2015 also remains healthy. However, given the current investment trends for spending at the advanced technology nodes and the decline in construction related activity, we continue to expect worldwide capacity expansion to remain in the low-single digits in the next three to five years. ◀▶

Process Watch: Sampling matters

DAVID W. PRICE and DOUGLAS G. SUTHERLAND, KLA-Tencor, Milpitas, CA

An optimum sampling strategy comes down to weighing the cost of process control against the benefit of capturing the defect or other excursion in a timely manner.

The first step in a process control strategy is being capable (i.e. able to identify the problems that are limiting a factory's baseline yield). After a capable strategy is in place, a factory can turn to optimizing the strategy to make it cost-effective—ensuring that the factory achieves maximum return on their investment. In most cases, this optimization is made through the introduction of sampling.

In general, process control sampling takes into account:

- the number of measurement sites per wafer for metrology (or wafer area for defect inspection)
- the number of wafers per lot that are measured
- the percentage of measured lots

In this article, it is assumed that the first two sampling components—sites per wafer and wafers per lot, are part of your capability strategy (addressed in the previous article), and that the word sampling refers simply to the percentage of the measured lots.

Sampling is a unique concept to process control—you can't sub-sample wafers to be etched, for example. The degree to which a factory will sample is based on the probability, projected from historical data, that an excursion will occur and the potential impact of that excursion. Determining an optimum sampling strategy comes down to weighing the cost of process control against the benefit of capturing the defect or other excursion in a timely manner.

The second fundamental truth of process control for the semiconductor IC industry is:

It is always more cost-effective to over-inspect than to under-inspect

For simplicity, let's assume that the probability that the process control tool will detect the excursion is fixed. That means that we're neglecting the fact that some types of excursions are easier to detect than others. We will cover this topic in a later series installment.

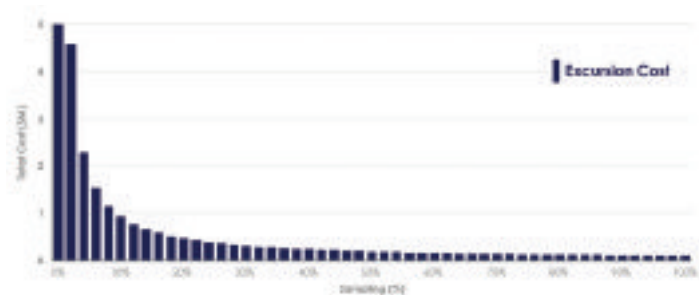


FIGURE 1A.

The economic impact of this excursion is a function of the number of exposed lots per excursion, the number of excursions per year, the yield loss per excursion, and the cost of the twenty-five wafers in the exposed lots. These quantities can be estimated and plotted as a function of the sampling rate (**FIGURE 1A**). Thus, lower sampling leads to more yield loss when an excursion occurs simply because there are more lots between inspections. The excursion cost is reciprocal of the sampling rate—very high at low sampling and

decreasing at $1/x$ as the sampling rate, x , increases.

The capital cost of sampling is a function of the process control tool price, the resources used to operate it and the tool's throughput and sensitivity. These quantities are estimated and plotted as a function of a sampling rate in **FIGURE 1B**. The capital costs increase linearly with the sampling rate because more tool capacity is required as the sampling rate increases.

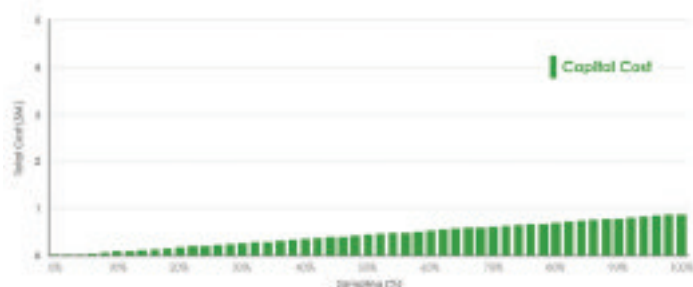


FIGURE 1B.

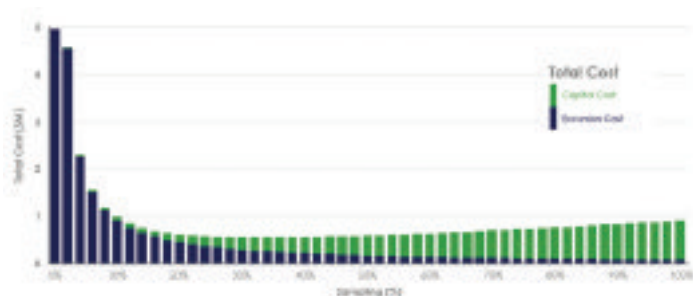


FIGURE 1C.

The total cost is the sum of the excursion and the capital cost, and the shape of the resulting curve is depicted in **FIGURE 1C**. A minimum in this curve indicates an optimum sampling rate—the point of lowest total cost. When there is no minimum, the optimum sampling rate is 100 percent, a scenario that frequently occurs for metrology.

At the optimum sampling rate, any reduction in sampling would result in more yield loss than capital savings, and any increase in sampling would result in more capital cost than the prevented yield loss (see **FIGURE 1C**). While the overall shape of the curve is governed mainly by the lot sampling rate, with other input assumptions shifting the minimum left or right, the curve consistently delivers the message that under-sampling is riskier (i.e., more costly) than over-sampling. Measuring

too few sites per wafers, wafers per lot, or lots per run is a high-cost way of running a manufacturing line.

In this model, the optimum sampling rate is proportional to the square root of the excursion cost and inversely proportional to the square root of the capital cost. In other words, a stable process does not need to be measured as frequently as a process having frequent excursions, but the relationship is not linear. If you were to decrease the excursion frequency by a factor of four, then you would be able to cut the sampling rate by a factor of two, to retain the minimum total cost.

Because of the mathematical nature of this curve, the total cost to the right of the optimum (higher sampling) is always less riskier than being off by the same amount to the left of the optimum (lower sampling). In other words:

$$\text{Total cost } (x_0 + \Delta x) < \text{Total cost } (x_0 - \Delta x)$$

where x_0 is the sampling rate with the lowest total cost.

There are other reasons to err on the side of over-sampling. Data is usually cheaper than the experienced engineering expertise required to draw conclusions. In a time-to-market based environment, such as the semiconductor industry, you cannot allow your decision makers to be data-starved; the data needs to be readily available to drive appropriate corrective actions. Indeed, of all the activities required for baseline yield learning-engineering talent, inspection data, processed wafers—the cost of the inspection is the least expensive.

Author's Note: Sampling Matters is the second in a series of 10 installments that explores the fundamental truths about process control—defect inspection and metrology—for the semiconductor industry. Each article introduces one of the 10 fundamental truths and highlights their implications. ♦

Managing oxide growth on in-process storage wafers for cost and yield impact

SURESH BILIGIRI, Rorze Automation, Fremont, CA

A system is described that mitigates unintended oxide growth for bare wafers while in-process storage and potentially post process at tools using nitrogen purge.

Unintended oxide growth on wafers while in storage or while in process is an important cause of excess process variability that can lead to poor yield and product quality.

To understand and eliminate the undesired oxide growth on wafers while in storage or between processes, we evaluated and compared wafers storied in a nitrogen-based environment to wafers stored in normal cleanroom environment. Important issues to consider:

- A typical wafer goes through a clean cycle prior to wafer moves.
- There are waste chemical handling costs involved in the handling, treatment and disposal of waste chemicals.
- If the oxide growth levels are uncertain then metrology of these wafer before wafer move has to be performed and this adds more cost to the process.
- If the oxide growth has exceeded the specification then a second re-cleaning cost is added to the process.
- Due to stringent environmental controls and corporate responsibility in green initiatives the cost of handling the waste chemicals will have an

impact of greater than twice the first cleaning.

- Each time a wafer is handled, the risk of loss increases causing an impact on yield.
- In a high demand situation where the fab utilization is approaching the high numbers, the re-clean adds costs and a negatively impacts production volumes.

In order to assess the impact of the unintended oxide growth, tests were conducted at a semiconductor manufacturing fab using a standard bare wafer stocker (BWS600 by Rorze) and a nitrogen purge type stocker (BWS1600 N2 by Rorze). The wafers were removed from each to test for oxide growth and returned to storage after measuring. The tests were repeated with the same set of wafers and data is shared here.

The Rorze BWS1600 N₂ consists of wafer PODS (about the size of a FOUP) that are stacked on a carousel. Each POD with 25 wafers is purged with N₂ continually. In order to minimize the use of nitrogen and to create a very low O₂ level, the POD has independent access door for each wafer slot on the POD (9mm door). This method (Rorze patent pending) offers N₂ environment for wafers inside even during the wafer transfer from and to the POD with minimum ambient air interaction. The system and the storage

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method is shown in **FIGURE 1**.

FIGURES 2 and 3 shows the N_2 and O_2 purging sequence data. Note that:

1. When the shutter door is open, O_2 density will be increased because of mixture of air of mini-environment (FFU) is forced into the POD/container environment.
2. While the shutter is open, N_2 gas supply volume will be increased from 5 L/min to 20 L/min from the POD that helps to reduce O_2 density inside the POD.
3. At any given time, when the shutter is open, even with the strong FFU flow as the wafer on end-effector directs flow from FFU the N_2 concentration in the POD does not go above 5000 PPM

The results of the oxide growth measurements on wafers stored in N_2 environment (Rorze BWS1600 N_2) were obtained on a regular frequency (Day 1, 3, 6, 7, 10, 14 & 21).

Measurements were made using "Rudolph S3000A" metrology thickness tool. To ensure the effect is uniform

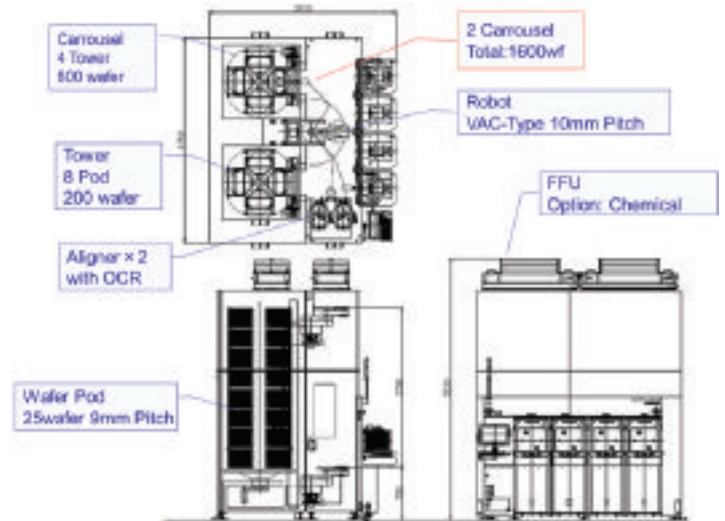


FIGURE 1. The design is executed for minimal consumption of N_2 as well as to mitigate the hazards of excess N_2 in the fab.

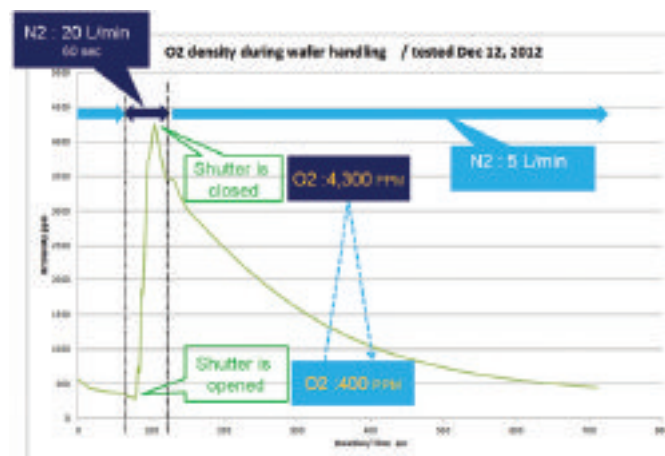


FIGURE 2. O_2 density during wafer handling.

across the stored area, wafers were placed in different PODS inside (C8 is at top on the carousal close to FFU and C1 is farthest from FFU at the bottom).

An identical test method was executed by storing wafers in a bare wafer storage unit where wafer was exposed to the fab environment but in a clean storage area (Rorze BWS600)

Results of the tests are shown in **FIGURE 4**. Wafers were set at different locations in the stocker to test the influence of storage location on rate of oxide growth. We found no noticeable difference in oxide growth for different cassettes. Even after 21 days with intermittent extraction to monitor growth (every three days), all wafers had less than 1.7Angstrom thickness oxide growth. The impact of oxide growth without intermittent exposure could be much smaller.

Cost analysis

As per an earlier Sematech model that takes into account the cost of materials, capital tool costs, uptime in the fab etc. for wafer clean per wafer pass following were the costs estimated and noted below. (Data reference provide by Mr. Rob Randhawa, Founder & CEO of Planar Semiconductor)

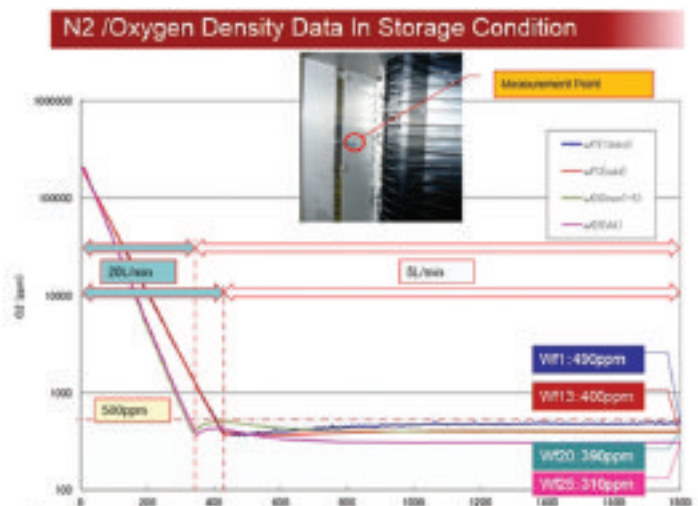


FIGURE 3. N_2 /oxygen density data during storage conditions.

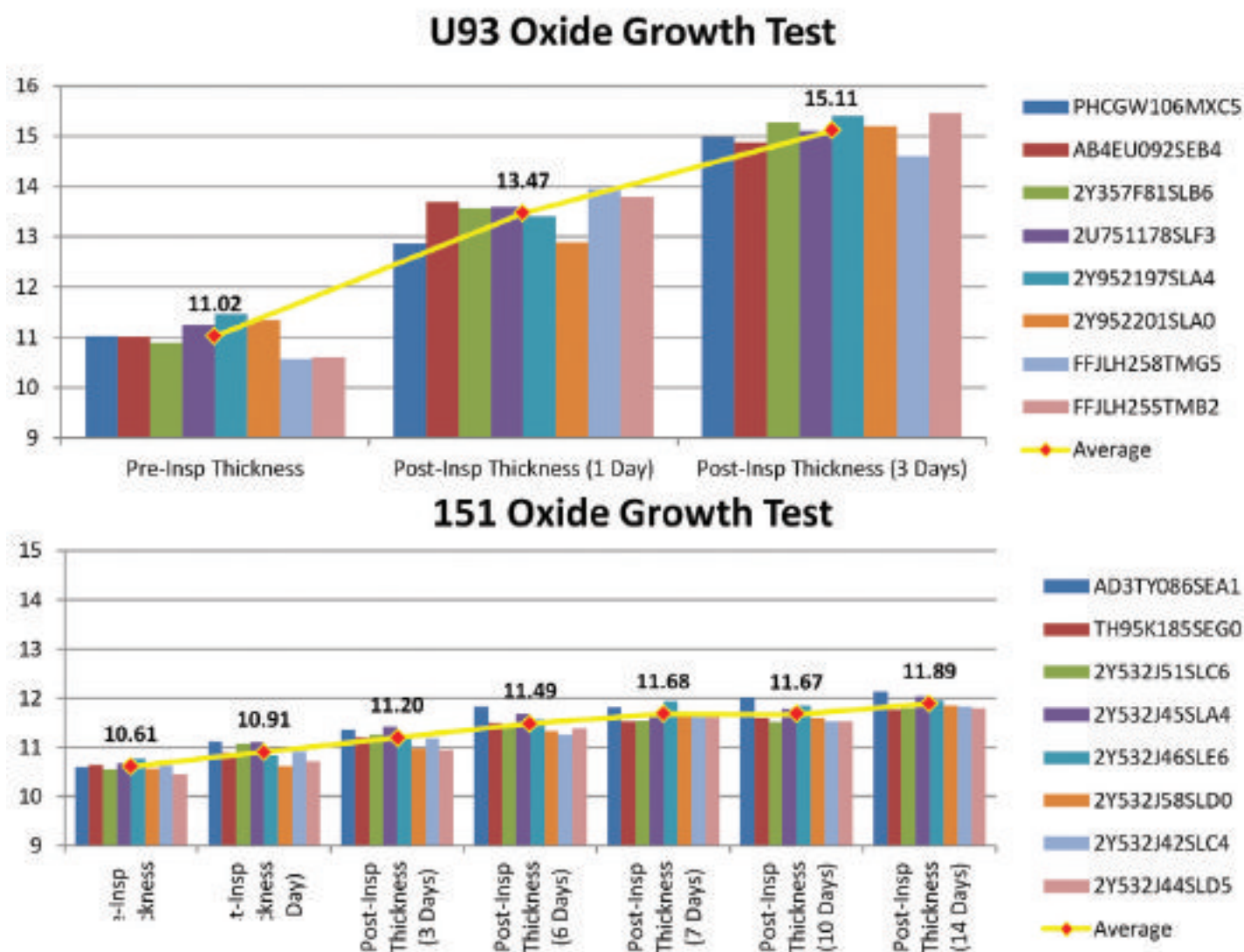


FIGURE 4. Oxide growth is small even after 21 days.

- Single wafer cleaning cost per wafer using DI water based cleaning only: \$1.90 per wafer – 300mm wafer
- Single wafer cleaning cost per wafer using standard chemicals without the IPA: \$2.30 per wafer – 300mm wafer
- Single wafer cleaning cost per wafer using standard chemicals + IPA: \$ 3.60 per wafer – 300mm wafer – This includes the reprocess cost of IPA

Based on the initial results we see, there is a substantial benefit to employ this technology that will help to make strides in continuing to help on cost controls while the technology node advances. The opportunity to eliminate the risk of oxide growth can potentially go beyond the wafer clean and to “in-process storage” where a wafer lot is in queue for the next step. There is a risk of delay where the wafer could continue to gain oxide growth resulting in

potential yield loss and a domino effect of reduced productivity and a risk of not meeting demand.

As technology proceeds to smaller nodes, the tolerance for variations within atomic layers are not acceptable as it will impact performance and yield, necessitating such products and technologies to keep the cost down.

Tools such as the N₂ purged bare wafer stocker can save anywhere from about \$900,000 to about \$1.7 million per year and easily pay off the cost of the system within a year or two.

Acknowledgements

Rob Randhawa, Founder and CEO of Planar semiconductor for sharing wafer cleaning costs, K.Sakata, Design Engineering Manager, at Rorze Corporation for technical details of the BWS1600/BWS3200 N₂ purge system. ◀

The mystery of reed relays: Understanding specifications

KEVIN MALLETT, Pickering Electronics, Clacton-on-Sea, Essex, U.K.

Specifications of reed relays, which are used for current switching in ATE and other applications are explained, including carry current, lifetime, minimum switch capacity, hot switching, operating speed and thermoelectric switching.

Reed relays, which use an electromagnet to control one or more reed switches without requiring an armature, are used for instrumentation and automatic test equipment (ATE), high voltage switching, low thermal EMF, direct drive from CMOS, RF switching and other specialized applications.

Reed relays are deceptively simple devices in principle. They contain a reed switch, a coil for creating a magnetic field, an optional diode for handling back EMF from the coil, a package and a method of connecting to the reed switch and the coil to outside of the package. The reed switch is itself a simple device in principle and relatively low cost to manufacture thanks to modern manufacturing technology.

The reed switch has two shaped metal blades made of a ferromagnetic material (roughly 50:50 nickel iron) and glass envelope that serves to both hold the metal blades in place and to provide a hermetic seal that prevents any contaminants entering the critical contact areas inside the glass envelope. Most (but not all) reed switches have open contacts in their normal state.

If a magnetic field is applied along the axis of the reed blades the field is intensified in the reed blades because of their ferromagnetic nature, the open contacts of the reed blades are attracted to each other and the blades deflect to close the gap. With enough applied field the blades make contact and electrical contact is made.

The only movable part in the reed switch is the deflection of the blades, there are no pivot points or

materials trying to slide past each other. The reed switch is considered to have no moving parts, and that means there are no parts that mechanically wear. The contact area is enclosed in a hermetically sealed envelope with inert gasses, or in the case of high voltage switches a vacuum, so the switch area is sealed against external contamination. This gives the reed switch an exceptionally long mechanical life

Inevitably in practice the issues are a little more complicated. The ferromagnetic material is not a good conductor and in particular the material does not make a good switch contact. So the reed blades have to have a precious metal cover in the contact area, the precious metal may not stick to the blade material very well so an underlying metal barrier may be required to ensure good adherence. Some types of reed relay use mercury wetted contacts, consequently reed relays that use plated contacts are often referred to as “dry” reed relays. The metals can be added by selective plating or by sputtering processes. Where the reed blade passes through the glass envelope any plating (in many cases there may be none) requires controlling to avoid adversely affecting the glass to metal hermetic seal. Outside the glass seal the reed blades have to be suitably finished to allow them to be soldered or welded into the reed relay package, usually requiring a different plating finish to that used inside the glass envelope.

The materials used for the precious metal contact areas inside the glass envelope have a significant impact

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on the reed switch (and therefore the relay) characteristics. Some materials have excellent contact resistance stability; others resist the mechanical erosion that occurs during hot switch events. Commonly used materials are ruthenium, rhodium and iridium— all of which are in the relatively rare platinum precious metal group. Tungsten is often used for high power or high voltage reed switches due to its high melting point. The material for the contact is chosen to best suit the target performance - bearing in mind the material chosen can also have a significant impact on manufacturing cost. Sealed in a long, narrow glass tube, the contacts are protected from corrosion, and are usually plated with silver, which has very low resistivity but is prone to corrosion when exposed, rather than corrosion-resistant but more resistive gold as used in the exposed contacts of high quality relays. The glass envelope may contain multiple reed switches or multiple reed switches can be inserted into a single bobbin and actuate simultaneously. As the moving parts are small and lightweight, reed relays can switch much faster than relays with armatures. They are mechanically simple, making for reliability and long life.

This article reviews and explains common specifications used for reed relays (**FIGURE 1**).

Carry current

Carry current is the current that the reed relay can support through its contact without long term damage. The life of the relay should be indefinite under this condition though some reed relays may also have a pulse current rating which can be applied to the relay without damage.

The carry current is determined primarily by the contact resistance of the relay and the heat sinking to the environment. As the current increases the temperature of the reed blades increases until it reaches a temperature where the material is no longer ferromag-

netic (Curie Temperature). Once that temperature is reached the relay contacts may open since the blades no longer respond to the magnetic field. The blade temperature is clearly dependent upon the current and relay path resistance – the normal assumption is that this is a square law (with current) relationship. In reality, the temperature rise is significantly more than a square law since the metallic resistance also increases with temperature, the magnetic field drops with temperature because of coil resistance rise and the mechanical properties of the blade can change. Consequently like all relays, exceeding the rating can result in a type of thermal runaway.

The packaging of the reed switch has a significant impact on the temperature rise, a lead frame tends to conduct heat to the outside world while the plastic encapsulation materials insulate it. The packaged reed relay will always have a lower current rating than that of the reed switch because manufacturers quote the rating with the reed switch directly exposed (no coil, no plastic packaging). The coil power will also add to the heating effect. Consequently Pickering Electronics always de-rates the reed relay ratings to ensure that the relay switch

remains within its design limits.

There is also another subtle effect that occurs as the carry current increases – the signal creates its own magnetic field that twists the blades and therefore can modulate the contact resistance. The blade twisting may start to see a contact resistance rise as the blade contact area reduces or changes.

Care must be taken not to exceed the relays ratings and pulse ratings should take account of the square law relationship between current and temperature.

It becomes difficult to manufacture reed relays with a carry current of greater than 2A because the contact area has to be increased and that tends to make the bladed stiffer and require a higher magnetic field strength to operate them.



FIGURE 1. Reed relays are used for current switching in ATE and other applications.

Lifetime

The lifetime of reed relays is critically dependent on the load conditions the reed switch encounters. For reed relays which are instrument grade the mechanical lifetime is much greater than 1 billion operations – they are mechanically simple devices that rely purely on the deflection of a blade to operate and there are consequently fewer wear out mechanisms.

The blade contact area though still wears as they are opened and closed. If the signal load when the blade closes or opens is low then the wear out is very slow, as the load increases and hot switching (interruption or closure of a signal line carrying significant current or voltage) occurs higher temperatures are generated at the contact interface and this makes the materials more prone to wear. DC signals can also result in the migration of metal from one contact to another and without regular polarity reversal eventually the underlying contact materials are exposed with their poorer conduction characteristics. Hot switching can also create a temporary plasma in the contact area with high local temperatures, rapid operation of a relay under load can start to raise the contacts temperature to an extent where premature wear out can occur.

The life of an instrument grade reed relay can vary by three orders of magnitude according to the load conditions, perhaps 5 billion operations under no or light load to 5 million operations at a heavy load.

Minimum switch capacity

Some types of relay have a minimum switch capacity, if the relay is closed on a very low level signal (current or voltage) oxide or debris on the relay contacts can remain at the interface and cause a higher than expected resistance, or even an open circuit. This tends not to be the case with reed relays because the precious metal contacts are sealed in a hermetic glass envelope containing inert gas. Minimum switch capacity tends to be a characteristic of higher power mechanical (EMR) relays.

Hot switching

Hot switching occurs whenever a relay contact is opened or closed with a signal (current and voltage) is present. As the contacts move apart or close an arc can be created

which transfers material from one contact to another, or simply redistributing the material. As the contact plating is damaged the resistance will eventually start to rise until the relay is no longer fit for the intended application.

For reed relays hot switching tests are always conducted into resistive loads. The hot switch capacity of a reed relay is typically quoted at a current/voltage that results in the number of operations that the relay will support around 10 million operations. The data sheet specifies a hot switch current (the limiting factor at low voltages), a hot switch voltage (limiting factor at low current) and a power (from the product of the open contact voltage and the closed contact current).

Operating speed

The operate time is the time from when the relay coil is energized or de-energized to when the contact reaches a stable position.

For a normally open contact when the coil is energized the current, and therefore the magnetic field, in the coil rises until the blades start to move closer together until they make contact. The contacts may impact each other sufficiently rapidly that there is bounce where for a short duration the contact is intermittently closed then opened. The operate time should be the time from when the relay coil was energized until the contacts are stably closed.

If the coil is driven from a higher than specified coil voltage the closing speed of the relay will be faster, however once the contacts make there may be more contact bounce as they meet with greater force. Overdriving the coil can also increase the release time since the magnetic field takes longer to collapse to the point where the contacts start to open.

For a normally open Form A (SPST) contact the release time is the time from when the coil is de-energized to when the contact is open. This operate time can be dependent on how the reed relay is driven, the presence of a protection diode on the coil will increase the release time. Typically, the release time is around one half the operate time.

Soft and hard weld failures

Operation of reed relays (or EMRs) under high load conditions causes one of the most common failure

mechanisms for relays – a failure where the contacts are welded together. By convention these welds are classified as being either soft or hard failures. In the event of hard failure the contacts tend to be welded together and nothing will separate them. This is an easy fault to identify. Soft failures

occur where the contacts sick but eventually come apart without any additional assistance. The failure is caused by small areas on the contact welding together, but the weld area is sufficiently small that the reed blades will separate because of their sprung nature. They could spring apart very quickly, or it may take several seconds to spring apart depending on how hard the weld is.

In either case the impact on the user is that the switching function of the relay is impaired and this is likely to have an adverse impact on the user application. So in either case the relay will require replacing since the defect is unlikely to improve with time. The cause of the weld will also need to be investigated and corrected.

Thermoelectric EMF

The cause of thermoelectric voltages is often misunderstood by users, and often misrepresented in articles and on the internet. The effect of thermoelectric EMF's is to generate a small voltage (measured in microvolts) across the relay terminals when the relay is closed (**FIGURE 2**).

The voltage arises whenever a metal wire has a temperature gradient across it (the Seebeck Effect), if one end of the wire is at a different temperature to the other then a voltage will appear which is dependent on the temperature difference and the materials that make up the wire. Reed relays use a mix of metals, and these can have different temperature drops across them which results in a voltage appearing at the relay connection terminals. The voltage is not created at a connection junction. Nickel iron has quite a strong thermoelectric EMF, so designing reed relays with low thermal EMF's can be a challenge.

The number and type of materials varies according

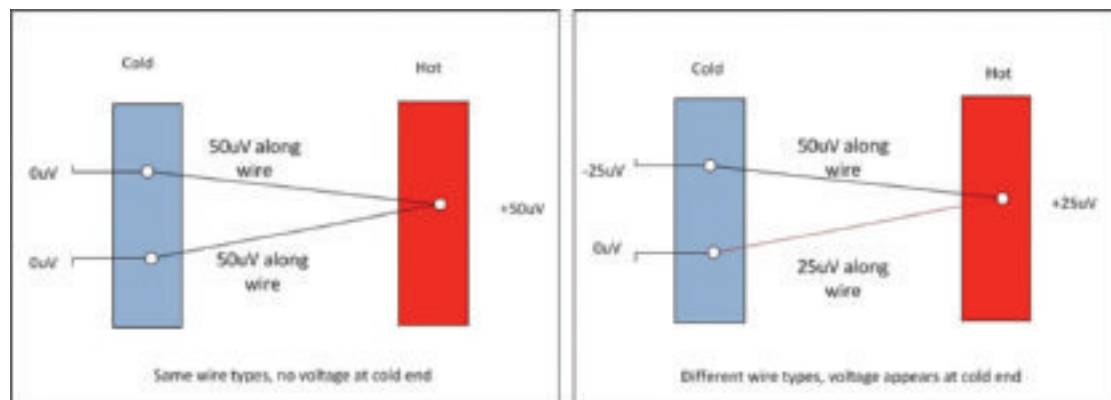


FIGURE 2. Thermoelectric EMF's are used to generate a small voltage (measured in microvolts) across the relay terminals when the relay is closed.

to the way the reed switch is designed and how it is packaged. If the relay was perfectly symmetric in construction (so the materials used from each contact to the reed switch were the same and the reed itself was perfectly symmetric in all materials and dimensions) and all heat sources in the relay body (primarily due to the coil) then this would be the case. However in reality the symmetry is not perfect so a residual voltage will arise.

Users can also degrade the performance by how they use the relay. When mounted on a PCB if the PCB has a temperature profile across it then that will generate an additional thermal EMF. Relay manufacturers usually assume that the thermal EMF is zero when the relay is first closed since up to that point no heat source exists inside the relay body. However, a temperature profile across the PCB (caused by the presence of other heat sources or forced air cooling) will create a thermal EMF.

Reed relays that have excellent Thermal EMF performance are typically designed to be as symmetric in design as possible and to use highly efficient coils to avoid heating the reed switch. Typically though, this results in a physically larger relay.

Two pole designs often quote the Differential Thermal EMF, this is the voltage generated between the two switches (usually) in a single package.

Assuming the relay design is reasonably symmetrical to a first order the voltage in one switch is the same as the other, so the differential voltage can be much smaller for the relay. Differential and single ended Thermo Electric EMF numbers should not be directly compared or confused with each other. ♦

High performance, cost-effective dicing of SiC wafers

3D-Micromac AG, a supplier of laser micromachining workstations, introduces the microDICE system which brings TLS-Dicing technology (Thermal-Laser-Separation) to semiconductor's back-end. The microDICE separates wafers, including SiC, into dies with an outstanding edge quality while increasing the yield and the throughput.

Due to the contactless laser machining method, there is no tool wear and no expensive consumables required. This results in excellent cost of ownership during the whole life-time of the dicing system.

Compared to traditional separation technologies microDICE provides a much higher process speed and better throughput enabling high-volume production of SiC based devices.



Next-generation MEMS etch and deposition equipment

memsstar Limited launched its ORBIS platform of etch and deposition process tools for MEMS manufacturing. ORBIS systems deliver the industry's most advanced single-wafer process capability, required to meet the uniformity and repeatability requirements for advanced MEMS manufacturing.

"Adoption of MEMS technology is increasing rapidly, with the explosion of mobile devices, the 'Internet of Things' and the trillion sensors roadmap," said Tony McKie, CEO of memsstar. "With such diversity in applications and increasing performance and capability, manufacturers are clearly demanding process advances, as smaller, high-functionality MEMS devices can no longer tolerate process variations that impact performance. Our new ORBIS platforms build on our first-generation systems to deliver significant process and hardware enhancements that advance manufacturing capability and performance in the MEMS industry."

The ORBIS platform enhances memsstar's production-proven and unique processing technology, which has seen strong market acceptance and has become an enabling technology for next-generation MEMS manufacturing. On the process side, enhancements built into the ORBIS platform include fully integrated process monitoring and endpoint control, as well as a new high-

selectivity package. At the same time, the platform's hardware has been upgraded, which results in even better uniformity and repeatability, critical to improving yield.

The new ORBIS platform consists of three models:

- ORBIS ALPHA™ targets institutions and universities involved in MEMS research and development (R&D) with a system based on memsstar's production-proven continuous-flow processing technology to enable next-generation process development on a cost-effective platform.
- ORBIS 1000 is a single-wafer vacuum loadlock system designed for commercial R&D. It uses the same processing techniques as memsstar's volume production systems, and can be easily upgraded to a production system as business conditions change. Supported process modules include XERIX™ oxide and silicon vapor phase etch and AURIX™ SAM coatings.
- ORBIS 3000 is a fully automated single-wafer platform that delivers the industry's most advanced MEMS manufacturing capability in the industry

for high-volume production. It also supports the XERIX etch and AURIX coatings process modules.

“We have spent a considerable time working with customers to enhance our single-wafer architecture and technology to ensure that it will meet their manufacturing requirements now and in the future. The ORBIS platform incorporates all of these advances, increasing system performance and delivering the industry’s most advanced release etch and surface modification equipment to our customers,” concluded McKie.

GF Piping Systems develops 450mm SYGEF Piping System

To prepare for the inevitable transition to a 450mm wafer size, GF Piping Systems is introducing a complete 450mm SYGEF PVDF Piping System, including a new Fittings concept and IR Plus welding.

The current 315mm Polyvinylidene Fluoride (PVDF) pipes and fittings have been available for years using a very stable extrusion and injection molding process. In addition, GFPS secured the availability of sufficient PVDF for future Piping System Requirements. Since



several chip makers, among them some industry leaders, see the transition to 450mm wafers as inevitable, GF Piping Systems decided to be prepared in advance and elected to develop a product line of 355mm, 400mm and 450mm PVDF piping to meet the six criteria of high

purity, along with the associated welding equipment suitable for conveying UPW in advanced semiconductor wafer factories.

Very little challenge can be seen in scaling the pipe extrusion process from 315mm to 450mm. However, GF Piping Systems decided to employ a completely new approach for the injection molding of fittings. Remarkable advantages can be realized by making sectional pieces, instead of molding the entire fitting in one piece. For example, from this patent pending process, shortened tees, elbows and reducers can be injection molded in smaller, more energy-efficient machines that are suitable for clean room conditions. The extension ends can be welded to these components in limitless combinations according to the desired functionality, using thermal plastic welding equipment.

New IR welding equipment

Having safe, clean pipes and fittings is only half of the equation needed for successfully commissioning a UPW piping system. One must also have a way to install it without contamination. To accomplish this, GF Piping Systems chose to draw upon its thermal plastic welding process. New plastic welding equipment was developed specifically to handle the new sizes up to 450mm. The new plastic thermal welding machine has an insertable/removable facing tool and heater head, just like the smaller-sized equipment that the industry has come to trust. The non-contact IR (infrared) heating reduces the risk of contamination and omits the need for equalization. The overlap feature eliminates variation of bead sizes and joining force inconsistencies due to pipeline drag forces. Overlap also allows very precise installation. Lastly, cooling times can be reduced because less energy is brought in by the controlled process.

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Foundry, EDA partnership eases move to advanced process nodes

Partnerships are the lifeblood of the semiconductor industry, and when moving to new advanced nodes, industry trends show closer partnerships and deeper collaborations between foundries, EDA vendors and design companies to ease the transition.

It's fitting, then, for me to pay homage to a successful and long-term partnership between a foundry and an EDA tool supplier.

A leading semiconductor foundry and an EDA vendor with design-for-yield (DFY) solutions have enjoyed a long-term partnership. Recently, they worked together to leverage DFY technologies for process technology development and design flow enhancement. The goals were to improve SRAM yield and provide faster turnaround of a new process platform development.

The foundry used the EDA firm's high-sigma DFY solution to optimize its SRAM yield for 28nm processes development. Early this year, it announced 28nm readiness for multi-project wafer (MPW) customers. One of the reasons it was able to release the 28nm process with acceptable SRAM yield in a short time was due to a new methodology for SRAM yield ramping that deployed a DFY engine.

During advanced technology development, the time spent on SRAM yield ramping is significant because statistical process variation, particularly local

variation between two identical neighboring devices sometimes called mismatch, limits SRAM parametric yield. The impact of local process variation increases when moving to smaller CMOS technology nodes.

In the meantime, supply voltage is reduced, so operating regions are smaller. The difficulty achieving high yield for SRAM is greater because smaller nodes require higher SRAM density. Such challenges require very high sigma robustness or high SRAM bitcell yield. Statistically, the analysis for the SRAM bitcell at 28nm needs to be at around 6σ , while FinFET technology at 16/14nm sets even higher sigma requirements for SRAM bitcell yield.

During technology development, foundry engineers improve the process to solve defect-related yield issues first. Design-for-manufacturing methodologies can be used to eliminate some systematic process variations. However, many random process variations, such as random dopant fluctuations (RDF), line edge and width roughness (LER, LWR), are fundamental limiting factors for parametric yield particular to SRAM.

Traditionally, foundry engineers rely on experience and know-how from previous node development efforts to analyze and decide how to run different process splits for different process improvement scenarios to optimize SRAM yield. These efforts are often time-consuming and less effective at advanced nodes like 28nm because the optimization margin is much smaller.

The fab's new SRAM yielding flow used a high sigma statistical simulator as the core engine. It provided fast and accurate 3-7+ σ yield prediction and optimization functions for memory, logic and analog circuit designs. During process development, the tool proved its technology advantages in both accuracy and performance, and was validated by silicon in several rounds of tape outs throughout the development process.

The flow saved months ramping up SRAM yield for the 28nm process node. It reduced iteration time and saved wafer cost. Process engineers now only need to fabricate selective wafers to validate simulation results. They know which direction is optimal and have guidelines to run process splits that will help them identify the best conditions and converge on the best yield. They gained greater certainty as they saw more simulation-to-silicon correlation data as the project progressed.

Overall, this is a highly successful and mutually beneficial partnership, and the value of DFY to process technology development, is obvious. The same DFY methodology can be used for memory designers as SRAM yield is their primary target as well. The only difference is it tunes design variables using the same methodology, flow and tool solutions.

It's easy to see the value of a tight collaboration between the foundry, EDA vendor and design companies and why it will be a trend on top of the "foundry-fabless" business model.



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