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OCTOBER 2015 VOL. 58 NO. 7

The availability of reliable, highly automated, high-volume aligned wafer bonding systems and processes was one of the keys to the growth of MEMS over the past 15 years (Source: EVG).

COVER

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COLUMNS

DEPARTMENTS

editorial

The ConFab Advisory Board Expanded

Please join me welcoming our news members of the Advisory Board for our annual conference and networking event, The ConFab. New members include: Pinyen Lin, Director of Etch Engineering, G450C and Deputy Director, TSMC; Robert Cappel, Senior Director Corporate Marketing, KLA-Tencor; William Chen, Fellow and Senior Technical Advisor, ASE; L.T. Guttadauro, Executive Director, Fab Owners Association; Li Li, Distinguished Engineer, Cisco Systems; Ariel Meyuhas, COO, The MAX Group; Gary Patton, CTO and Head of Worldwide R&D, GLOBALFOUNDRIES and Elton Peace, General Manager North America Regional Operations, Lam Research.

> "The ConFab program will focus on The Economics of Semiconductor Manufacturing and Design."

The new members will be joining the existing Advisory Board, comprised of David Bennett, VP Alliances, GLOBALFOUNDRIES; Janice M. Golda, Director, Lithography Capital Equipment Development, Intel Corporation; Devan Iyer, Director Worldwide Semiconductor Packaging Operations, Texas Instruments; Lori Nye, COO/Executive Director Customer Operations, Brewer Science; Ken Rygler, President, Rygler Associates (founder of Toppan Photomasks); Sima Salamati, VP, Fab Operations, imec; Hans Stork, CTO, ON Semiconductor Corporation; Aubrey Tobey, President, ACT International; Geoffrey Yeap, VP of Technology, Qualcomm Inc.; and Abe Yee, Sr. Director, Advanced Technology and Package Development, Nvidia Corporation.

Now in its 12th year, The ConFab will be held June 12-15, 2016 at The Encore at The Wynn in Las Vegas. The conference program will focus on "The Economics of Semiconductor Manufacturing and Design". Topics will include:

- How IoT is Driving the Semiconductor Industry
- Filling the Fabs of the Future: A Guide to Hot New Applications
- MEMS Sensor Fusion and More then Moore
- The Limits of Scaling: Understanding the Challenges of sub-10nm Manufacturing
- Fabless, Foundries and OSATs: Optimizing the Supply Chain
- System Integration, Advanced Packaging + 3D Integration
- China's New Role in the Global Semiconductor Industry
- Legacy Fabs and the Resurgence of 200mm
- The Impact of Continued Consolidation Across the Supply Chain
- Wearables and Bioelectronics: The Cusp of a Revolution?
- Tackling Rising R&D Costs in the Semiconductor Industry

The ConFab is an executive-level conference and networking event for business leaders from the semiconductor manufacturing and design industry. The event features a high-level conference program, networking events and business meetings with purchasing decision makers and influencers. More information on The ConFab may be found at www.theconfab.com. Please join us!

—Pete Singer, Editor-in-Chief

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92% of Attendees responded the QUALITY OF THE CONFERENCE met or exceeded their expectations

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Web Exclusives

The changing (and challenging) IC reliability landscape

It seems that a laser focus on integrated circuit (IC) reliability is all around us now. Gone are the days when a little "over design," or additional design margin, could cover the reliability issues in a design layout. Designers now need to articulate to partners, both internal and external, just how well their designs function over time and within their intended environment.

http://bit.ly/1Pok8nq

Process Watch: Risky business

The authors focus on strategies for managing risk associated with the most difficult steps in the process, focusing in this installment on a fundamental truth of process control: High-Stakes Problems Require a Layered Process Control Strategy. As the margins of error steadily decrease with each new design node, the number of parameters that can wreak havoc on the process continues to rise, they note.

http://bit.ly/1FrEsnS

Neon gas supply issues dog the semiconductor industry

The armed conflict in Ukraine, where most of the world's supply of neon gas for semiconductor manufacturing and other industrial applications is produced, is leading lithography equipment vendors to offer ways to reduce use of neon, which is utilized as a buffer gas for argon fluoride and krypton fluoride gases employed in lasers for chip production.

http://bit.ly/1Kt5udw

S3S – The conference for IoT technologies

The upcoming IEEE S3S Conference 2015 in Sonoma, CA, on October 5-8, will focus on key technologies for the IoT era. It is now accepted that the needs for the emerging IoT market are different from those that drive the high-volume PC and smart-phone market.

http://bit.ly/1NK7JLP

n&b news and blogs

Knowm to deliver configurable artificial neural networks

Knowm Inc., a start-up pioneering next-generation advanced computing architectures and technology, announced the availability of artificial neural-network (ANN) chips built using memristors with bi-directional incremental learning capability.

http://bit.ly/1OOgaqI

300mm ams fab bet on IoT

It is a big deal that Austrian-headquartered ams AG—world leader in production of IC sensors, RFID chips, and power-supplies—has announced plans to set up a new silicon wafer manufacturing line in up-state New York.

http://bit.ly/1Kt3bXY

Insights from the Leading Edge: Semicon Taiwan

Phil Garrou reports on The System Integration by 3D SiP forum held during Semicon Taiwan. The forum invited global experts to discuss the development of 3DIC and 2.5DIC packaging and alternative solutions. Presentations were made by Cisco, AMD, SK Hynix, ASE, Altera, Amkor, Teledyne and Cadence. The forum chairman was ASE's CP Hung.

http://bit.ly/1PoiQsT

Comfortable consumer EEG headset shown by Imec and Holst Centre

A new wireless electroencephalogram (EEG) headset that is comfortable while providing medical-grade data acquisition has been shown by the partnership of imec, the Holst Centre, and the Industrial Design Engineering (IDE) department of TU Delft.

http://bit.ly/1LL36ga

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USA – **IBM** launched two new business units that will apply the company's knowledge in Big Data, advanced analytics and cognitive computing to the IoT and Educations markets.

USA – **Qualcomm** acquired **Capsule Technologie**, a global provider of medical device integration and clinical data management solutions.

USA – **Intersil** acquired **Great Wall Semiconductor**, a private technology company developing power metal-oxide semiconductor field-effect transistor (MOSFET) technology for cloud computing, space and consumer applications.

ASIA AND USA – **ASE** Chairman Jason Chang received the **SEMI** award for advancements of copper wire bonding technology during Semicon Tawian.

EUROPE – With the help of a semiconductor quantum dot, physicists at the **University of Basel** in Switzerland have developed a new type of light source that emits single photons.

USA – **M/A-COM** shipped more than one million GaN-on-Silicon (GaN on Si) RF power devices.

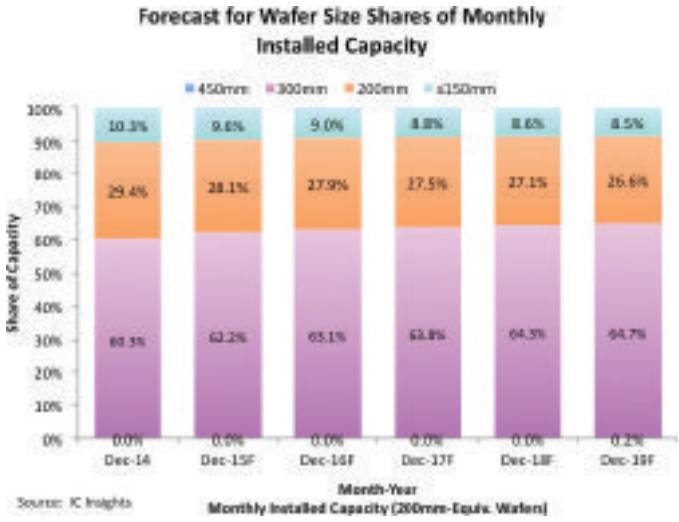
USA AND EUROPE – **Nordson** acquired Munich, Germany-based **MatriX Technologies GmbH**, a manufacturer of automated X-ray inspection equipment.

Companies maximize 300mm, 200mm wafers; slow progress on 450mm

Larger wafer diameters provide more chips per wafer at a modest increase in material and process costs, resulting in reduced chip costs, according to IC Insights. Historically, transitions to larger diameter wafers have provided cost reductions greater than 20% per unit area. However, enormous financial and technology hurdles continue to plague the development of, and the transition to, 450mm wafers. As a result, the transition to larger diameter wafer has slowed dramatically and companies are maximizing their efficiency using 300mm and 200mm wafers. IC Insights' Global Wafer Capacity 2015-2019 report shows that worldwide capacity by wafer size was dominated by 300mm wafers in 2014 and is forecast to continue increasing through 2019 (Figure 1).

Efforts to develop 450mm wafer technology continue to make some progress, but the pace of development slowed

Continued on page 10



Dialog Semiconductor to acquire Atmel for $4.6 billion

Dialog Semiconductor and Atmel Corp. announced that Dialog has agreed to acquire Atmel in a cash and stock transaction for total consideration of approximately $4.6 billion. The acquisition creates a global leader in both Power Management (defined as power management solutions for mobile platforms including smartphones, tablets, portable PCs and wearable-type devices) and Embedded Processing solutions. The transaction results in a company that supports Mobile Power, IoT and Automotive customers. The combined company will address a market opportunity of approximately $20 billion by 2019.

Dialog will complement its position in Power Management ICs with a portfolio of proprietary and ARM based microcontrollers in addition to high performance ICs for connectivity, touch and security. Dialog will also leverage Atmel's established sales channels to diversify its customer base. Through realized synergies, the combination could deliver an improved operating model and enable new revenue growth opportunities.

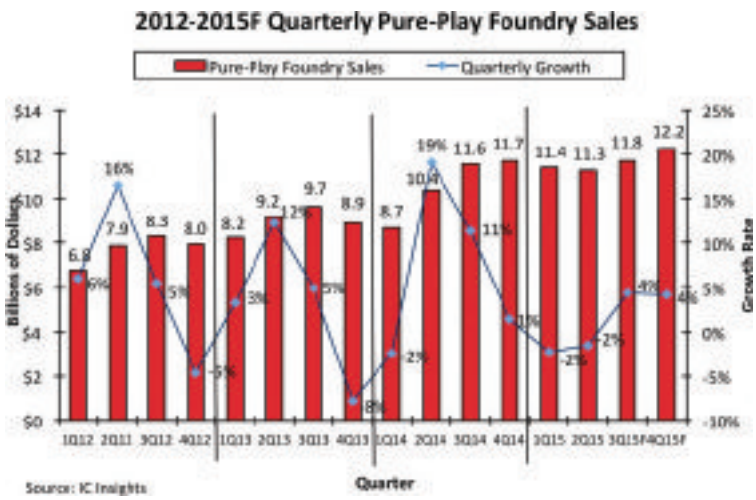
Continued on page 10

Pure-play foundry sales forecast to surpass $12B in fourth quarter 2015

The pure-play foundry market is forecast to grow to an all-time high of $12.2 billion in 4Q15, following several quarters in which sales remained between $11.3 and $11.8 billion, based on IC Insights' updated foundry forecast presented in the August Update to The McClean Report 2015 (Figure 1). IC Insights defines a pure-play foundry as a company that does not offer a significant amount of IC products of its own design, but instead focuses on producing ICs for other companies (e.g., TSMC, GlobalFoundries, UMC, SMIC, etc.).

The quarterly pure-play IC foundry market has recently displayed a seasonal pattern in which the best growth rate takes place in the second quarter of the year and a sales downturn occurs in the fourth quarter. Given that about 98 percent of pure-play foundries' sales are to IDMs and fabless companies that will re-sell the devices they purchase from the foundry, it makes sense that the pure-play foundries' strongest seasonal quarter (second quarter) is one quarter earlier than the total IC industry's strongest seasonal quarter (third quarter).

However, as shown in the figure, 2015 is not expected to display the typical pure-play foundry quarterly revenue pattern. Although 1Q15 registered its usual weakness, 2Q15 showed a sequential decline, rather than an increase. In 2012, 2013, and 2014, second quarter pure-play foundry revenue showed strong double-digit growth. In 2Q15, results were decidedly atypical with a 2 percent decline in pure-play foundry sales. The primary reason behind



the 2Q15 sales decline was the 5 percent 2Q15/1Q15 revenue decline by foundry giant TSMC. TSMC's 5 percent sequential decline was equivalent to a $366 million drop in its revenue.

For 4Q15, IC Insights forecasts that the quarterly pure-play foundry market will show a higher than normal growth rate of 4 percent. With most of the inventory adjustments that held back growth in the first half of the year expected to be completed by the end of 3Q15, 4Q15 is forecast to register enough growth to boost the quarterly pure-play foundry market to over $12.0 billion for the first time.

Leti demos MEMS fabrication on its 300mm line, pointing the way to lower manufacturing costs

In what may be a first for the MEMS industry, CEA-Leti has manufactured micro-accelerometers on 300mm wafers, a development that could lead to significantly lower MEMS manufacturing costs.

"With more than 200 people involved on micro-systems R&D, Leti is one of the world's leading research institutes on MEMS, and this demonstration that our 200mm MEMS platform is now compatible with 300mm wafer fabrication shows a significant opportunity to cut MEMS production costs," said Leti CEO Marie Semeria. "This will be especially important with the worldwide expansion of the Internet of Things and continued growing demand for MEMS in mobile devices."

Leti is a pioneer and leader in MEMS research and development for sensors and actuators. Building on more than 30 years of MEMS R&D, Leti continues to focus on innovative sensor technologies.

The most advanced is its M&NEMS technology platform based on detection by piezo-resistive silicon nanowires, which reduce sensor size and improve performances of multi-axis sensors. Leti's inertial-sensor manufacturing concept enables the design and fabrication of combo sensors, such as three-axis accelerometers, three-axis gyroscopes and three-axis magnetometers on the same chip. This is a key component for Internet of Things (IoT) applications.

Leti's M&NEMS concept, developed with 200mm technology, is currently being transferred to an industrial partner. Demonstration of this technology on 300mm wafers has shown very promising results.

In addition to lowering costs, manufacturing MEMS with 300mm technology enables 3D integration using MEMS CMOS processes in more advanced nodes than on 200mm, and the use of 3D through-silicon-vias (TSV), which is already available in 300mm technology. ◆

Rising flexible display technology patents herald future market growth

With a recent sharp rise in the number of patent applications for flexible display technologies, the market for various types of flexible displays is expected to broaden. According to IHS, 312 patents for flexible displays were filed with the United States Patent and Trademark Office in 2014; user-interface technology was the most active sector for patent applications. Flexible displays accounted for 62 percent of US display patent applications last year.

"Flexible displays are next-generation display panels fabricated on a paper-thin and flexible substrate, so that they can be bent and rolled without damage," said Ian Lim, Senior Analyst of Intellectual Property for IHS Technology. "These types of displays, which lend themselves to far wider applications than conventional rigid displays, are projected to create an entirely new display market and replace existing non-flexible display solutions."

Based on the latest information from the IHS Flexible Display Patent Report–which covers patents related to flexible displays issued in the US, in 2014, focusing on materials, manufacturing technology and applied devices–Samsung Electronics filed half of all new flexible display patents in the United States, followed by LG Electronics at 17 percent. Most of these patent applications focus on preventing image degradation, reducing device distortion and providing a range of user interfaces for bendable and foldable displays. Patents on parts and manufacturing technologies that primarily focus on the use of polyimide flexible substrates and metal nanowire in organic light-emitting diode (OLED) displays were also popular.

"Patents for flexible display device technologies outnumber those for flexible display parts and manufacturing technologies in recent patents, indicating that the flexible display market is entering a period of maturing growth," Lim said. "As manufacturer requirements for flexible displays grow, battles to acquire relevant patents will only become fiercer." ◆

Purdue and Stanford profs recognized at annual SRC conference

Semiconductor Research Corporation (SRC), the world's leading university-research consortium for semiconductors and related technologies, presented its highest honors Sept. 21 to professors from Purdue University and Stanford University at SRC's annual TECHCON conference in Austin, Texas.

Dr. Kaushik Roy, the Edward Tiedemann Distinguished Professor of Electrical & Computer Engineering at Purdue University, received this year's SRC Aristotle Award for outstanding teaching and a deep commitment to the educational experience of his students. With SRC support, Roy's team at Purdue has made numerous research contributions to the industry in areas including low-power electronics, scaled CMOS devices and circuits and spintronics.

Additionally, Dr. Muhammad A. Alam, the Jai N. Gupta professor of Electrical and Computer Engineering at Purdue, and Dr. Subhasish Mitra, associate professor in the Department of Electrical Engineering and Department of Computer Science at Stanford University, were awarded SRC Technical Excellence Awards for their respective SRC-supported research.

Selected by SRC member companies and SRC staff, the award-winning faculty and research teams will be recognized for their exemplary impact on semiconductor productivity through cultivation of technology and talent.

"Advanced research has been instrumental in propelling the semiconductor industry forward, and we are recognizing these valuable researchers and their teams for the critical work they have performed in helping the industry achieve technological triumphs," said Ken Hansen, SRC CEO and President.

Dr. Roy's present research interests include spintronics, low-power electronics and brain and bio-inspired computing enabled by emerging technologies.

Dr. Alam's microelectronics and nanotechnology research includes the physics of electronic, optoelectronic and bioelectronics devices, as well as the reliability limits of CMOS devices and computational modeling.

Dr. Mitra's research interests include robust system design; VLSI design; CAD; validation and test, including Quick Error Detection Technology (QED); emerging nanotechnologies and emerging neuroscience applications.

SUNY poly announces JDA with INFICON

SUNY Polytechnic Institute's Colleges of Nanoscale Science and Engineering and Inficon, Inc. announced plans for a joint research and development alliance on advanced semiconductor manufacturing technology. The 2-year R&D agreement will leverage SUNY Poly CNSE's globally recognized state-of-the-art capabilities and INFICON's in-situ monitoring technologies that are enabling the "smart factories" of the future with real time nanoscale process control. The joint alliance will also formally launch a new Advanced Manufacturing Performance (AMP) Center dedicated to the component, sub-system and site-service companies that support the advanced manufacturing processes in a broad array of industries. The AMP Center is expected to lead to the creation of 50 jobs and will leverage the operations at the NanoTech Albany Complex while expanding to the Computer Chip Commercialization Center (QUAD-C) in Marcy with dedicated R&D capabilities, which will also support new advanced manufacturing operations recently announced by Governor Andrew Cuomo.

The establishment of the semiconductor research and development partnership with SUNY Poly CNSE will characterize precursor and/or byproduct compounds containing phosphorus, arsenic, antimony, gallium, and/or indium that may evolve from the surface of wafers during and/or following various processes throughout the semiconductor manufacturing sequence; identify and develop methods for detecting and analyzing such compounds; and improve and develop sensor technologies and equipment that embody or incorporate such methods.

Companies Maximize, *Continued from page 6*

significantly in 2014. Now, by most accounts, volume production using 450mm wafers is not expected before 2020, although pilot production could start a year or two before. IC Insights shows 450mm wafers accounting for a very slim share of installed capacity in 2019.

For the most part, 300mm fabs are, and will continue to be, limited to production of high-volume, commodity-type devices like DRAMs and flash memories; image sensors and power management devices; and complex logic and microcomponent ICs with large die sizes; and by foundries, which can fill a 300mm fab by combining wafer orders from many sources.

At the end of 2014, there were 87 production-class IC fabs utilizing 300mm wafers (Figure 2). There are several 300mm R&D IC fabs and a few high-volume 300mm fabs around the world that make "non-IC" products such as image sensors and discretes, but these are not included in the count shown in the chart.

Only once -- in 2013 -- has the number of 300mm wafer fabs declined. That year, three large fabs operated by ProMOS and Powerchip closed and setbacks delayed the opening of several new 300mm fabs until 2014. By the end of 2019, there are expected to be 23 more 300mm wafer fabs in operation than there were at the close of 2014. The number of 300mm fabs will likely peak between 115-120, which assumes 450mm fabs will enter volume production in the future. For comparison, the greatest number of volume-production 200mm wafer fabs in operation was 210 (the number declined to 154 fabs at the end of 2014).

The list of companies with the most 300mm wafer capacity includes memory suppliers Samsung, Micron, SK Hynix, and Toshiba/SanDisk; the industry's biggest IC manufacturer and dominant MPU supplier Intel; and the world's two largest pure-play foundries TSMC and GlobalFoundries. These companies offer the types of ICs that benefit most from using the largest wafer size available to best amortize the manufacturing cost per die.

The number of fabs running 200mm wafers will continue to be profitable for many more years and be used to fabricate numerous types of ICs including specialty memories, display drivers, microcontrollers, analog products, and MEMS-based devices. Devices like these are practical to make in fully depreciated 200mm fabs that were used to produce devices now made on 300mm wafers. TSMC, TI, and UMC remain the three companies with the greatest amount of 200mm wafer fab capacity.

Dialog Semiconductor, *Continued from page 6*

"The rationale for the transaction we are proposing today is clear – and the potential this combination holds is exciting. By bringing together our technologies, world-class talent and broad distribution channels we will create a new, powerful force in the semiconductor space. Our new, enlarged company will be a diversified, high-growth market leader in Mobile Power, IoT and Automotive. We firmly believe that by combining Power Management, Microcontrollers, Connectivity and Security technologies, we will create a strong platform for innovation and growth in the large and attractive market segments we serve. This is an important and proud milestone in the evolution of our Dialog story," said Jalal Bagherli, Dialog Chief Executive Officer.

The transaction is expected to close in the first quarter of the 2016 calendar year. In 2017, the first full year following closing, the transaction is expected to be accretive to Dialog's underlying earnings.

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Intel and ASM look to TCB

PHIL GARROU,
Contributing Editor

In the September column, we looked at some of the key thermo-compression bonding (TCB) papers at ECTC. Is there any question that TCB is real and will be the next big bonding technology? The focus this month is more on this very important new assembly process from Intel and ASM.

Intel introduced TCB into high volume manufacturing in 2014. As substrate and die become thinner and solder bump sizes and pitches get smaller, the thin organic substrate tends to warp at room temp and as the temp is increased during the reflow process. The thin die can also demonstrate temperature dependent warpage, which can come into play during the reflow process. The extent of warpage of the substrate and die at high temperatures can overcome the natural solder surface tension force leading to die misalignment with respect to the substrate, resulting in tilt, non-contact opens (NCO) and in some cases solder ball bridging (SBB). **FIGURE 1** shows these various defects.

In the Intel TCB process, the substrate with pre-applied flux is held flat on the hot pedestal under vacuum. The die is picked up by the bond head, held securely and flat on the bond head with vacuum. After the die is aligned with the substrate, the bond head comes down and stops when the die touches the substrate. A constant force is then applied while the die is heated up quickly beyond the solidus temperature. As soon as the solder joint melts, the die is moved further down (solder chase) to ensure all solder joints are in contact. The die is held in position allowing the solder to reflow completely, and to wet the bump pads and copper pillars. While the solder is still in the molten state, the bond head retracts upwards controlling the solder joint height. The bond head then releases the vacuum holding the die and moves away as the solder joints have solidified. The major process parameters, i.e temperature, force and displacement are continuously monitored during the TCB bonding process.

Large differences in the CTE between the organic substrate and die results in different magnitude of expansions when heated which can lead to serious bump offset at corners. To minimize the thermal expansion mismatch, the substrate is processed at a lower temperature (e.g. 140°C) while the die and solder is rapidly heated up for reflow and cooled down for solidification using a pulse heater with heating ramp rate exceeding 100°C/s and cooling ramp rate exceeding 50°C/s. This reduces the heat transfer to the substrate. The bulk of the substrate can remain at low temperature and does not expand extensively.

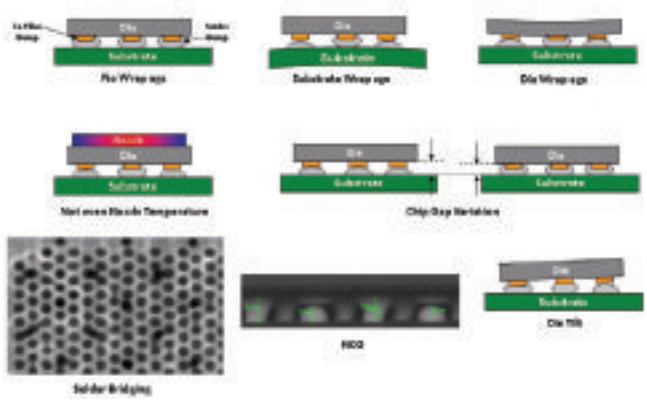

FIGURE 1. Common defects in the TCB process.

In another ASM paper on TCB they examined what they call liquid phase contact (LPC) TCB. The goal is to increase the throughput of the TCB process. Process flow is shown below. Flux is printed or sprayed on the substrate. Then the bonding head picks up a die from the carrier at an elevated temperature, but below the solder melting point. Then the bonding head is heated up to a temperature higher than the solder melting point and the chip is aligned with the substrate. The chip is then contacted and wetted on the substrate at a predetermined bonding height. After a predetermined bonding time, the bonding head can move is cooled down to a temperature below the melting point of solder. They claim this results in attachment of 1200 units/hr vs 600 for the standard TCB flux process. ◆

Packaging

TSMC forum emphasizes industry collaboration

JEFF DORSCH,
Contributing Editor

Taiwan Semiconductor Manufacturing kicked off its Open Innovation Platform (OIP) Ecosystem Forum with thanks – not for another beautiful day in Silicon Valley, but for the collaborative work it does with its customers, suppliers, and other industry partners.

Rick Cassidy, the foundry's senior vice president and president of TSMC North America, kicked off the all-day event in Santa Clara, Calif., saying he wanted to debunk the myth of the "lone creative genius" in the chip business. "It is a lot of geniuses working together," he said. "Innovation happens collectively."

While there has been much attention paid to the slowing growth in the smartphone market, mobile technology will continue to be a significant driver for the semiconductor industry, according to Cassidy. He reviewed the areas of mobile technology, the Internet of Things, and automotive electronics.

"IoT will require an incredible amount of interconnection technology," Cassidy said.

Between IoT and automotive tech, there will be "a very significant amount of data that's going to be needed to be stored and processed," he added.

Cassidy emphasized TSMC's relations with its many collaborators, large and small. "We're a pure-play foundry," he said. "We do not have any products."

He added, "Nobody does yield better than TSMC."

Cassidy noted that TSMC will spend more than $2.2 billion this year on research and development, compared with more than $1.9 billion last year. The foundry's capital expenditure budget for 2015 is $10.5 billion to $11 billion, up from $9.5 billion in 2014, he added.

The opening session also heard from Jack Sun, TSMC's vice president of R&D and chief technology officer, and Cliff Hou, vice president of the R&D design technology platform, as well as executives of Avago Technologies and Xilinx, two TSMC customers.

Semiconductors

While TSMC continues to fine-tune its 16-nanometer FinFET process, the world's largest silicon foundry will begin making chips with 10nm features later this year and will put 7nm chips into risk production in early 2017.

Jack Sun, TSMC's vice president of research and development and chief technology officer, said the 7nm process node will offer significant enhancements in speed, power, and device density. Processors, graphics processing units, and field-programmable gate arrays will benefit from 7nm technology, along with mobile and networking chips. He noted that TSMC has been able to turn out a functional test chip with 7nm features, implemented in a static random-access memory.

Cliff Hou, the company's vice president of research and development/design and technology platform, said the foundry has collaborated with ARM Holdings on core implementation for scaling to 7nm. The transition from 10nm to 7nm will provide an area reduction of 40 percent to 45 percent, he added.

TSMC is looking toward employing extreme-ultraviolet lithography, direct self-assembly, and multi-beam electron-beam lithography to fabricate 7nm chips, Sun said. The company is working with ASML Holding on laser light sources with 90 watts of power, he added. Sun also said "settings are being finalized" for EUV systems capable of producing 125 wafers per hour.

Hou noted that the foundry put its 16nm FinFET Plus (16FF+) process into volume production earlier this year and introduced its 16FFC process, a "compact," lower-cost version of 16FF+. TSMC will put 16FFC into NTO in the second quarter of 2016, he added.

Sun said TSMC is developing embedded resistive RAM and embedded magnetoresistive RAM technology to complement its SRAMs and flash memory devices.

He also reviewed the company's wafer-level packaging technology, the chip-on-wafer-on-substrate (CoWoS) packaging and its integrated fan-out (InFO) packaging. InFO, a multichip package, will go into production next year and "could replace flip chip," Sun said.

Wafer bonding for high performance MEMS, power devices, and RF components

ERIC F. PABO, CHRISTOPH FLÖTGEN, BERNHARD REBHAN, PAUL LINDNER *and* **THOMAS UHRMANN,** *EV Group, St. Florian, Austria*

Recent trends and future directions for wafer bonding are reviewed, with a focus on MEMS.

All devices and products are evaluated to varying degrees on the following factors: 1) availability or assurance of supply, 2) cooling requirements, 3) cost, 4) ease of integration, 5) ease of use, 6) performance, 7) power requirements, 8) reliability, 9) size, and 10) weight. MEMS devices are no exception and the explosive growth of MEMS devices during the last decade was driven by substantial improvements in some of the aforementioned variables. MEMS manufacturing is based on patterning, deposition and etch technologies developed over the last 50 years for the manufacturing of ICs along with the relatively new technologies of aligned wafer bonding and deep reactive ion etch (DRIE). This article will review the recent trends and future directions for wafer bonding with a focus on MEMS along with some mention of wafer bonding for RF and power devices.

The incredible growth in MEMS over the last 20 years has been enabled by the development of the DRIE process by Bosch and by aligned wafer bonding. Many MEMS devices have very small moving parts, which must be protected from the external environment. Initially, this was done using special packages at the die level, which was relatively expensive. Wafer-level capping of MEMS devices seals a wafer's worth of MEMS devices in one operation, and these capped devices can then be packaged in a much simpler and lower-cost package. Anodic bonding and glass frit bonding were the initial bonding processes used for MEMS and are often referred to as "tried and true." However, both of these processes have challenges, and as a result, few new MEMS products and processes are being developed using these processes.

Anodic bonding requires the presence of Na or some other alkali ion which causes several problems. The first is that Na ions are driven to the exterior of the wafer during the bonding process and will accumulate on the bonding tooling, requiring the tooling be cleaned on a periodic basis. The second is that Na can cause CMOS circuits to fail – preventing anodic bonding from being used to combine MEMS and CMOS. Almost all MEMS devices require a CMOS ASIC to process the output signal from the MEMS device. Historically, this integration has been done at the package level with wire bonding but now some high-volume products are available where the integration of the CMOS and the MEMS is done as part of the wafer-level capping process. Also, anodic bonding typically requires a maximum process temperature of over 400°C and the presence of a strong electric field during bonding. The high temperature influences the throughput of the bonding process and some devices cannot tolerate the high electric field.

Even though the majority of the MEMS parts that exist

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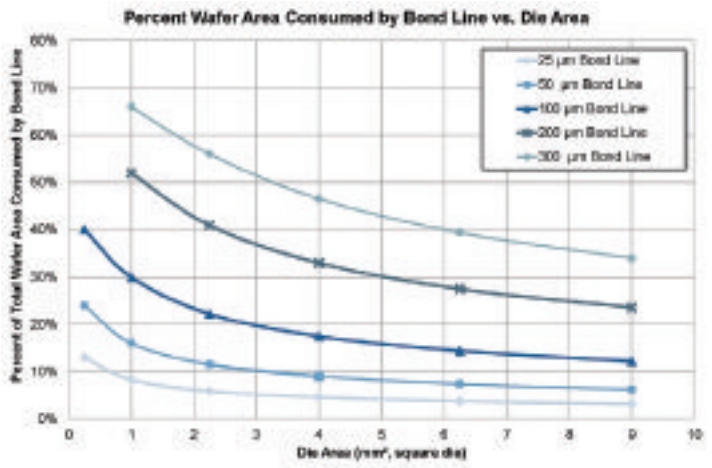

FIGURE 1. Plot showing the percentage of the surface area of a wafer consumed by bond line vs die area and bond line width. In the calculation the die dimensions were calculated from the center of the bond lines.

today were probably bonded using glass frit, this wafer bonding process has several challenges as well. The major one is that the glass frit is applied and patterned using a silk screen process, which has a typical resolution in the 250 to 300µm range. This means that as the size of the MEMS die decreases, an ever greater percentage of the wafer surface is consumed by the bond line, which limits the number of die per wafer and increases the cost per die. **FIGURE 1** shows the effect of bond line width and die size on the percentage of the wafer surface that is consumed by the bond line [1]. Also, many of the glass frits contain Pb to lower the glass transition temperature. Although the amount of Pb is very small, there is widespread concern regarding the use of Pb and being RoHS (Restriction of Hazardous Substance) compliant.

Both anodic bonding and glass frit bonds are nonconductive and therefore not suitable for the formation of connections to electrically conductive through silicon vias (TSVs) at the same time as the seal ring is formed. This means that these processes are not as suitable for the 3D integration of CMOS and MEMS.

For MEMS applications there is a strong trend toward the use of metal-based wafer bonding; in particular, liquid metal-based processes such as solder, eutectic and transient liquid phase (TLP). This trend is driven by the aforementioned challenges with anodic and glass frit bonding. Moving from glass frit to a metal-based bonding for a die size of $2mm^2$ can result in up to a 100% increase in the die per wafer. This doubling of the die per wafer will result in an approximately 50% decrease in the cost per MEMS die.

Some of the metal-based aligned-wafer-bonding processes that are currently used in high-volume manufacturing are: Au-Au thermo-compression bonding, which has been in volume production for over 10 years; and Al-Ge eutectic bonding, which is very popular even though it requires a very careful process setup and control

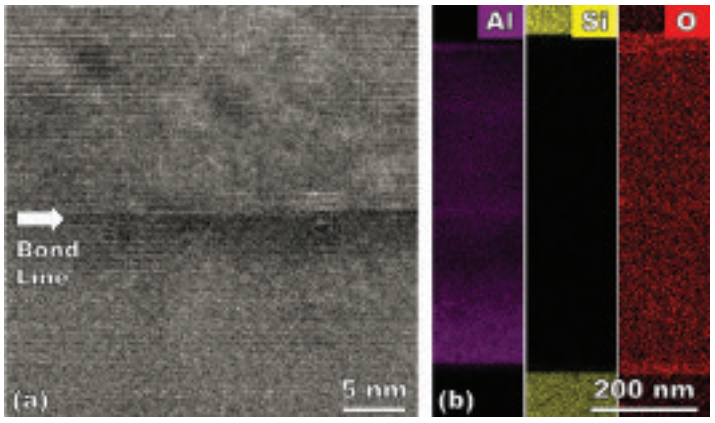

FIGURE 2. (a) High resolution transmission microscopy (HRTEM) image of Al-Al bond performed using EVG ComBond® process, showing no amorphous layer. (b) Energy dispersive x-ray spectroscopy (EDXS) elemental analysis of the bond cross section showing from left to right Al, Si, and O. Note that there is no concentration of O at the interface. The uniform level of O across the Al layer is likely caused by exposure to ambient atmosphere during sample preparation (HRTEM and EDXS analysis performed by Fraunhofer IWM Halle).

and has a peak process temperature of over 400°C. Cu-Sn transient liquid phase (TLP) wafer bonding, another metal-based process, is used in low-volume production of hermetically sealed devices such as micro-bolometers [2] but is not currently used in medium- or high-volume production. Cu-Sn TLP wafer bonding also requires very careful design and control of the metal stack as well as the bonding process.

The maximum process temperature that is required for a bonding process has three significant effects. The first is that the bonding process takes longer as the maximum process temperature increases due to the increased time required to heat up to the bonding temperature from the loading temperature and the time required to cool down to the unload temperature. The bonding process time determines the throughput of the wafer bonder(s) and factors into the cost of ownership (CoO) for the bonding process. The second is that the process temperature required for bonding may damage the devices on the wafers being bonded. The aluminum metallization of certain CMOS devices may be damaged at temperatures greater than 450°C. The VOx or vanadium oxide used on the sensor pixels for micro-bolometers will be damaged by temperatures greater than 200°C. The third is the internal stress that is created when wafers with mismatched coefficients of thermal expansion (CTE) are bonded together at an elevated temperature. In this case the higher the bonding temperature, the higher the internal stress at room temperature.

Unless the bonding metals are noble metals such as Au, oxides will form on the metal layer and have a negative effect on the bonding process - making an oxide management strategy necessary. This oxide management strategy can have elements that prevent the oxide from growing using special storage conditions or coatings, removing the oxide before bonding, and heating in an inert or reducing environment. In some cases, the bonding process can also be adjusted to overcome the effect of the oxides by increasing the pressure, temperature and time for the bonding process.

There is substantial interest in bonding processes and equipment that are capable of removing the native oxide from metals and other materials prior to wafer bonding and preventing the regrowth of oxide. Equipment capable of running such a process will have several substantial advantages. The first is that it will allow materials that have been previously difficult to bond to be bonded at or near room temperature. For example, Al-Al thermo-compression wafer bonding without the removal of the native oxide has previously been demonstrated, but required a process temperature of greater than 500°C, which made the process unattractive for production [3]. Low temperature Al-Al thermo-compression bonding has been demonstrated by using a special surface treatment and doing all handling in a high vacuum environment **(FIGURE 2)**. A low-temperature Al-Al thermo-compression bonding process has the advantage of using an inexpensive readily available conductive material and increased throughput due to the low process temperature. In addition to being used to form the seal ring, this low-temperature Al-Al bonding could be used for the 3D integration of MEMS and CMOS through the use of TSVs filled with Al.

This surface pretreatment and handling in high vacuum enables covalent bonding of two wafers at or near room temperature with no oxide in the interface. This process has several very significant advantages. The first is that the low process temperature allows the bonding of substrates with substantially different CTE such as $LiNbO_3$ or $LiTaO_3$ to Si or glass. This combination of materials has drawn the interest of RF filter manufacturers due to its ability to reduce the temperature sensitivity of surface acoustic wave (SAW) devices. The second

FIGURE 3. EVG580® cluster tool for high vacuum bonding and room temperature covalent bonding.

is that materials with both a CTE mismatch and a lattice mismatch can be bonded together without the development of major crystalline defects that can arise when forming the material stack by growing one crystalline layer on top of another when there is a lattice mismatch. One interesting possibility is bonding GaN to diamond for applications where large amounts of heat must be removed from the GaN device. In addition, bonding a thin layer of monocrystalline SiC to a polycrystalline SiC could offer wafers with the electrical performance of monocrystalline SiC at a cost closer to the cost of polycrystalline SiC. Another application of this bonding process is to join materials such as GaInP, GaAs, GaInAsP and GaInAs for fabrication of quadruple junction concentrated solar cells with record conversion efficiency of 44.7% [4, 5].

A high-vacuum cluster tool capable of aligned wafer bonding offers significant advantages for MEMS applications where the vacuum level in the cavity after bonding is important, such as gyroscopes and micro-bolometers **(FIGURE 3)** [6]. Modules can be added to the base cluster tool to enable the wafers to be baked out at a controlled elevated temperature prior to alignment and bonding in high vacuum. Getter activation can also be done in the bake-out module without loading or saturating the getter, as all subsequent steps are done in high vacuum. For devices where getter activation requires a high temperature and the other wafer has thermal limits, two bake-out chambers allow a high-temperate bake-out and getter activation while the other chamber performs a lower-temperature bake out. For example, micro-bolometers that used vanadium oxide on the detector pixel have a thermal limit of about 200°C, whereas the cap wafer contains a getter that should be activated around 400°C. Also, the high-vacuum capability is beneficial for producing devices that are heated and use vacuum for thermal isolation because a higher vacuum reduces the heat loss, which reduces the power required to maintain the fixed temperature.

This high-vacuum cluster tool allows the separation of the process steps of bake out, surface treatment, alignment and bonding as well as allows the tool to be configured to the specific application needs. Also, the cluster tool base makes it possible to develop modules for specific applications without redesigning the entire tool.

The availability of reliable, highly automated, high-volume aligned wafer bonding systems and processes was one of the keys to the growth of MEMS over the past 15 years. The next 15 years are expected to be an exciting period of advancement for aligned wafer bonding as new equipment and processes are introduced, such as the tools and processes that allow separate pre-processing of the top and bottom wafer, as well as all handling, alignment, and bonding in vacuum. The cluster tools that will be used to do this will allow for further innovation by adding new modules to the cluster tool. In addition, the ability to remove surface oxides prior to bonding, prevent these oxides from reforming, bond at or near room temperature, and have a strong, oxide-free, optically transparent, conductive bond with very low metal contamination will allow many new product innovations for RF filters, power devices and even products that have not yet been thought of.

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The future of MEMS in the IoT

PETE SINGER, *Editor-in-Chief*

The ripples from MEMS have been building slowly for years and are quickly converging with the Internet of Things (IoT).

In advance of SEMI's recent European MEMS Summit, held September 17-18 in Milan, Italy , we asked members of the conference steering committee about what's happening in the world of MEMS. Answers came from:

- Stefan Finkbeiner, CEO Bosch Sensortec
- Benedetto Vigna, Executive Vice President and General Manager, Analog MEMS, and Sensors Group, STMicroelectronics
- Christophe Zinck, Senior Application Engineering Manager, ASE Group
- Eric Mounier, Senior Analyst MEMS, Yole Developpement
- Martina Vogel, Officer of the Director of the Institute, Fraunhofer ENAS
- Yann Guillou, Business Development Manager and MEMS Summit event Manager, SEMI Europe Grenoble Office

Q: What do you see as the big trends and challenges in MEMS and their applications, particularly with regard to the IoT.

"The application of MEMS sensors to the IoT-enabled markets (e.g. wearables, smart home, etc.) will require sensors to shrink further and to work even more power-efficient as in smartphones," said Dr. Stefan Finkbeiner, CEO Bosch Sensortec. "In particular, the application side of the sensor will demand more attention. The value-add of a sensor must be convincing to become designed into a certain product," he added.

Finkbeiner said he sees a big market pull for gas sensors such as the Bosch in-door air quality sensor, the BME680. "That trend is visible for the smartphone as well as for the IoT-enabled markets, like for example the Smart Home market," he said.

Martina Vogel, officer of the director of the institute, Fraunhofer ENAS, said: "We see, that MEMS exist almost everywhere in our daily lives – in our homes, our cars, our workplaces – and yet they go largely unnoticed. Despite this low profile, microsystems have undergone rapid development in the last two decades, evolving from

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miniaturized single-function systems into increasingly complex integrated systems. From our point of view we call these complex integrated systems, smart integrated systems.

From performance point of view we distinguish between different generations of smart systems. The first and the second generation entered into diverse applications. The first generation of Smart Systems consisted of several packages of components connected on a single substrate, or printed circuit board. These devices are commercially available in medical applications such as hearing aids and pacemakers, as well as in automotive applications such as airbag systems. The best-known example of a second-generation Smart System is the ubiquitous smart phone, which has seen great commercial success.

Smart systems of the third generation are self-sufficient intelligent technical systems or subsystems with advanced functionality, which bring together sensing, actuation and data processing, informatics / communications. Therefore these systems are not only able to sense but to diagnose, describe and manage any given situation. They are highly reliable and their operation is further enhanced by their ability to mutually address, identify and work in consort with each other. Such smart systems will be the hardware basis for the internet of things (IoT)."

From technology point of view, Vogel said such systems "are not limited to silicon–based technologies but integrate polymer-based technologies, printing technologies (e.g. for printed antennas, printed sensors, displays or batteries), different nanotechnologies (e.g spintronic devices, CNT based devices or devices based on embedded nanoparticles) and even embroidering technologies for sensors."

Benedetto Vigna, Executive Vice President and General Manager, Analog MEMS, and Sensors Group, STMicroelectronics, said: "The next wave of MEMS development is moving toward actuation and, while the ripples from these beautiful little machines have been building slowly for years, they are converging quickly with the Internet of Things (IoT). We are beginning to see new applications such as tiny mirrors that enable people to interact more naturally with technology, smaller, faster autofocus solutions for mobile phones, and new types of printheads for 3D printing -- and this is just the beginning."

Christophe Zinck, senior application engineering manager, ASE Group, said the big trends and challenges from his perspective are "form factor (especially height), co-integration (flexibility to be used in different modules/ SiP (in term of packaging of course but also compatibility with different wireless standard), power consumption and, of course, cost."

Eric Mounier, senior analyst MEMS, Yole Developpement, said: "For us, MEMS is just a technology among others that could answer the IoT's requirements for sensors. Indeed, type of sensing required for IoT is very broad: Inertial sensing, chemical sensing , pressure sensing, light sensing … any physical event.

Sensor for the internet of things follow several requirements, Mournier says:

- Low power consumption (Due to the integration in wireless battery powered modules)
- Small form factor (Due to the need for small wireless sensors)
- Low cost (As IoT large expansion lies in the availability of low cost sensors)

For now, several sensing solutions exist in different fields (inertial sensors in smartphones for example). But strong challenges still have to be overcome:

- New sensing solutions (such as MEMS chemical sensors, etc.)
- Low cost, highly integrated solutions (via 3D stacking, etc.)

MARTINA VOGEL,
Officer of the Director of the Institute, Fraunhofer ENAS

YANN GUILLOU,
Business Development Manager and MEMS Summit event Manager, SEMI Europe Grenoble Office

- Standardization; The IoT is the accumulation of thousands of different applications requiring low cost solutions, but with limited volumes. Developing one sensor per application is not possible due to development costs.

"I am pretty confident MEMS will be used for IoT, specially for gas/chemical sensing. MEMS technologies for gas sensors have many advantages compared to other technologies: Up to 50% size reduction and cost reduction, CMOS scalable technology," Mournier said. "With cost and miniaturization to be a driving force for consumer and industrial Iot applications, it opens the way to new technologies such as MEMS."

Q: Sensor fusion is an intriguing thought and the ultimate device might have multiple sensors integrated with energy harvesting, a thin film battery, a microprocessor/ASIC, wireless communication capability, etc. How far away from that are we? What are the big challenges? Is it cost? Integration? Packaging? Form factor? What are the leading applications?

ST's Vigna said "We are already well on the sensor-fusion path that contains multiple sensors integrated with a thin-film battery, a microprocessor/ASIC, and wireless communication capability. The two technical challenges are low-power radio and high-efficiency (energy) harvester."

Finkbeiner said Bosch Sensortec already provides leading edge sensor fusion SW integrated within a multi-sensor 9-axis device powered by an ARM µController. "This single package device - the BNO055 - is already available and specifically targeting at motion sensing and orientation detection applications in the IoT-enabled markets. Energy harvesting and thin film batteries might still be a bit too far away from being capable of offering enough energy for this particular use case at reasonably small size. But there's a lot of research in this area. The challenges? Yes, cost/price is always the main driver. Small size is also important. It allows for small form factor products and better placement flexibility."

Fraunhofer's Vogel said there is a lot of work carried out with in ECSEL and especially EPoSS. "EPoSS the industry driven Euroean Platform on smart system integration is just working more than 10 years in this field," she said. "Big challenges are of course packaging and integration from technology point of view. But also issues like big data handling and data security in the internet need to be solved."

Vogel said market reports concerning IoT predict two trends:

- Printed electronic systems that will enable - low cost sensing. Printing technologies, such as roll-to-roll (R2R) will enable extremely large volumes and low cost. Also expect disposable devices with a short lifespan.
- Sensor "swarms" for inorganic sensing. Devices will have complete integration of sensing, processing RF, energy harvesting, on single small chip (<1mm2).

ASE's Zinck said he didn't see things going that far, "but each sensor fusion is quite specific and current modules are often using custom ASIC, MEMS, etc. The next big challenge is flexibility for co-integration and this will require availability of bare die on the market, otherwise small and efficient SiPs won't be easily available if you cannot mix best solutions available on the market (in terms of performance and cost, of course).

Zinck said there are also lots of challenges regarding packaging, including compartmental shielding to avoid parasitic between components, antenna on package (especially for wearable), and test.

Q: We're hearing a lot about wearables and medical applications, but what about applications in the smart home, smart city, smart grid, industrial and, of course, automotive ?

Vigna said: "There are already numerous applications for MEMS in Smart Environments, Smart Driving, and Smart Things and many of ST's customers are leading that charge by combining elements of ST's complete portfolio. We've got customers using ST MEMS, MCUs, analog and power, and connectivity products in smart thermostats, smart lighting, smart meters, and Smart Driving applications. If you're not hearing enough about these, it is only because the wearable and medical applications may be sexier."

Finkbeiner said: The sensors for the other IoT-enabled markets like smart home, smart grid etc. are available or already being developed … what is lacking is the corresponding infrastructure, that means the upper layers for aggregating, collecting and intelligent interpretation of the vast sensor data and bringing them into the cloud. This will for example require standards how to handle sensor data at an higher, more abstract level. But that's

beyond the domain of the MEMS sensor suppliers. At Bosch we have therefore founded Bosch Connected Devices & Solutions, a business unit which develops complete solutions based upon our MEMS sensors.

Vogel said: "Just several years ago Frost and Sullivan pointed out that smart is the new green. The concept of 'Smart Earth' is, in fact, the in-depth application of a new generation of network and information technologies. Smart cities arise worldwide. Global concepts for smart production are under development. The Internet of Things - IoT - including smart grid, smart health, smart city, smart buildings, smart home, smart production and smart mobility provides not only big opportunities but is requesting more highly integrated smart systems from the hardware side. The total number of connected devices is expected to grow rapidly. Electronic components and systems are a pervasive key enabling technology, impacting all industrial branches and almost all aspects of life."

Zinck said: "Wearables and medical are driving SiPs developments as low power and very aggressive from factor, at low cost are mandatory. Smart home, smart city, etc. are using a lot of MEMS and sensors, but the challenges are not exactly the same, some are similar in particular for Smart home (low power, wireless modules, etc.) but there is less pressure on form factors."

Automotive is a different topic, says Zinck. "The trend we can see is to go smaller for sure, but for the moment it implies move away from leaded packages to leadless, with specific technology developments like wettable flank QFN. Also for automotive two categories have to be clearly distinguished:

- Non-safety applications (like Infotainment): basically similar trend as consumer MEMS, with more and more sensors in the cabin (uphones, pressure, etc.)
- Safety applications: very robust have to be used, but some "intelligent SiPs" are already available like QFN 7x7 TPMS (featuring an accelerometer + ASIC + pressure sensor).

Q: Europe in general is very strong in MEMS for various reasons. Why does it make sense to have the MEMS Summit in Europe?

SEMI's Yann Guillou said Europe is home to several strong IDMs in MEMS, and most notably home to Bosch and STMicroelectronics. "These MEMS leaders are often identified as the industry's 'Titans'. These IDMs have contributed enormously to the European industry, but they have also benefited from a strong value chain in the region: RTOs, equipment and materials companies, foundries, etc. Having such leaders in the region is definitively a differentiating factor for Europe in a MEMS and sensor industry that is facing mounting competition. With the IoT, many new business opportunities may arise and increase the competition. This might shake up the current state of the industry," he said.

Organizing such event in Europe was pretty straightforward. We took this decision more than 1 year ago and it looks like this decision was right. Today more than 200 people are already registered for this event and we expect to go beyond. I see lot of non-European companies planning to attend, including many US and Asian companies. Interest is strong in Asia for this event. People from Korea, Taiwan and China will be attending. As an example, we will be pleased to receive the visit of a Chinese delegation interested to develop business and technology partnerships with European companies.

The use of sapphire in mobile device and LED industries: Part 2

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The use of sapphire in the manufacturing of Light Emitting Diodes (LEDs) is covered in the second part of a two part series.

In Part 1 of this article we discussed the optical and mechanical properties of sapphire and its use in the mobile device industry. In part 2 we will discuss the use of sapphire in the LED process including some of the newer technologies that produce these devices.

Solid state lighting (or "LED bulbs" as they are commonly known) have become a mainstream product in our culture. Their longer life time and lower power usage (along with the banning of incandescent bulbs) have ensured that more and more consumers are moving to this type of lighting. Like a fluorescent light (where the white light is produced by a phosphor coating excited by the excited gas molecules) solid state lights use a phosphor excited by the short wavelength light emitted by an LED. What you may not know is that about 8 out of every 10 LED bulbs sold uses sapphire as the starting material for their manufacturing process.

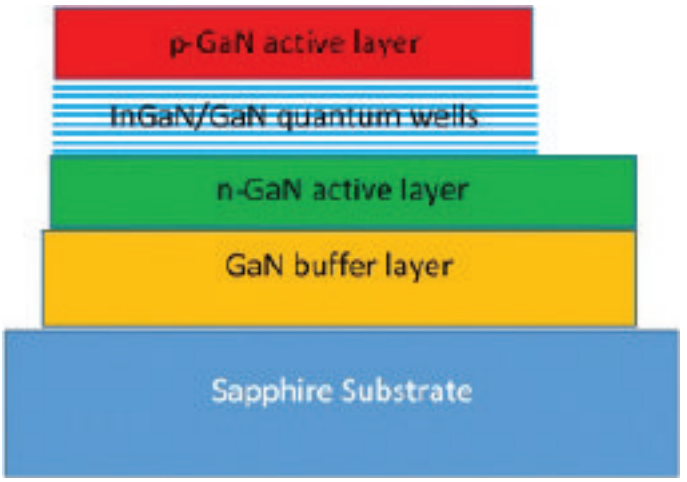

FIGURE 1. Typical cross-section of an LED device (not to scale)

As we summarized in part 1, sapphire has some good points: hard, strong, optically transparent and chemically inert (there is a reason high end watches use sapphire crystals) and some bad points: hard, strong, and chemically inert (which is why sapphire crystals are more expensive than glass). What we did not discuss is that single crystal sapphire has turned out to be an ideal material on which to grow the layers of material needed to make an LED.

As **FIGURE 1** shows an LED is made by growing epitaxial layers of Gallium Nitride (GaN), AlGan or InGaN on a substrate. Ideally one would use GaN as the substrate material (similar to growing epitaxial Si on Si for integrated circuits) as this would result in the highest quality material and thus the most efficient LED's. Unfortunately GaN substrates are very difficult to make in any reasonable size and the costs have ruled out using this approach except in certain niche markets. The three main substrate alternatives have been silicon (Si), silicon carbide (SiC) and sapphire.

As a substrate material Si would be expected to be the best choice due to its high quality, low cost and ready availability. To date, the quality of GaN type layers grown on

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FIGURE 2. A schematic of the process used to produce non patterned sapphire wafers for LEDs.

Si has not been sufficient for large scale manufacturing processes. Work continues on improving this process and although it may one day dominate the process it currently remains a small part of the business.

SiC substrates are higher cost than Si but have been successfully used for LED manufacturing processes. Much of the LEDs produced by Cree (who also manufacture SiC substrates) use this type of substrate. However, the higher cost and limited availability of 6 inch SiC material means that the majority of LED producers use sapphire.

Thus sapphire substrates account for the majority of LED devices produced [1]. Although not as cheap as Si they are cheaper than SiC, available from a number of manufacturers and are able to survive the high temperature processes needed to produce a short wavelength LED. **FIGURE 2** schematically shows the production process for a typical non-patterned sapphire wafer.

The sapphire production process starts when a seed crystal and a mixture of aluminum oxide and crackle (un-crystallized sapphire material) is heated in a crucible. Included in this mix is a cookie-sized seed crystal which forms the pattern to be replicated as the crystal grows. Each furnace manufacturer has its own special recipe which heats the material using a specific temperature/time profile based on the size of melt and the type of crystal to be grown. Once the correct growth temperature is reached the melt is cooled (this process can take two weeks depending on the amount of sapphire being produced) using another set of carefully controlled time/temperature profiles. When done correctly, the cookie-sized seed grows and produces a single-crystal sapphire boule. **(FIGURE 3).** In reality, two weeks is a long time and any number of can go arise during this process including gas bubbles, mechanical faults such as cracks and contamination. Each of these problems affects the sapphire and its crystal properties. Each crystal fault can become a nucleation site for defects in the epitaxy grown on wafers produced from the boule. There is a clear correlation between the time taken to grow a boule and the potential quality of the boule produced. Many of the problems encountered in the upscaling of the sapphire production process have come from trying to grow large boules at high speeds.

At this point in the process you have a boule which in fact has the wrong crystal orientation for growing GaN epitaxy. Unlike the Si crystal growth process where the cylindrical boules can be ground to size and then cut into wafers, sapphire boules are often cored at right angles to the boule axis. Some companies produce sapphire using a silicon like process [2] but the majority of sapphire produced has to be cored. Thus the next step in the process is to "core-drill" a boule to produce one or more smaller round cylinders (ingots) depending on the original boule size and the size of wafers to be produced.

The ability to grow large sized boules on a regular basis is not in question; most important is how much of that boule is bubble-, crack- and impurity-free. In some cases the boules are inspected with various metrology techniques to determine which sections of the boule can be used and which cannot. The section of the boules not used is recycled into the original growth process (unless contaminated). Obviously if one is producing 6 inch wafers larger volumes of the boule need to be defect free than if one is producing 2 inch or 4 inch. Currently most of the LEDs produced are produced on 4 inch wafers with a few newer 6 inch lines and a number of older 2 inch lines. 8 inch sapphire wafers do exists but are not in mass production at this time.

FIGURE 3. Sapphire boules of various sizes.

FIGURE 4. Sapphire wafers before epitaxial layer deposition.

The process after this is very similar to that used in the silicon industry to produce the wafers which will be used as substrates. A diamond saw (remember, Sapphire is a very hard material) is used to cur the ingot into a number of thin disc shapes by cutting perpendicular to the ingot's long sides. Each of these discs is then ground to its final size, surface-ground and mechanically and chemically polished to produce sapphire substrates. These substrates, after cleaning, can be used as starting material for the epitaxial process used to produce the LED structure. **FIGURE 4** shows some pictures of typical 2, 4 and 5 inch sapphire substrates. As discussed earlier the more defect free the surface is the better the quality of epitaxial film that can be grown. The video listed in reference [3] produced by GTAT shows many of the steps discussed above.

Recently one further step has been taken to produce what are called patterned sapphire substrates (PSS). The multiple quantum well layer shown in Fig. 1 is the layer that generates light in an LED. As you can imagine this

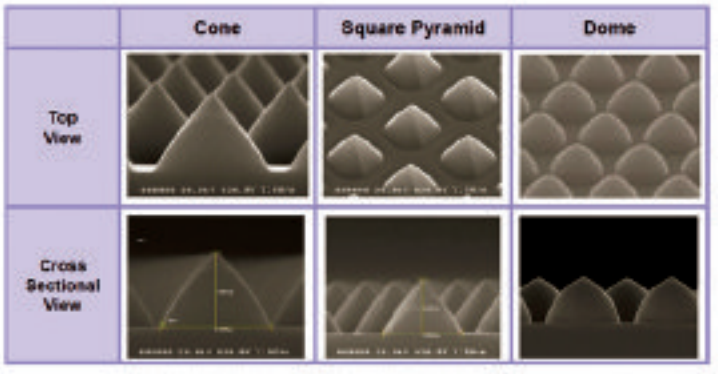

FIGURE 5. SEM micrographs of PSS patterned sapphire wafers.

light is emitted in all directions. However, once packaged most LED's emit light from only one surface of the device. In the case of Fig. 1 a typical package collects the light emitted from the top of the device. This of course means that all of the light emitted in any other direction is wasted. In particular since sapphire is transparent little of the light emitted toward the substrate can be used.

One obvious solution to this would be to coat the substrate with something that reflects the light (i.e. metal). Unfortunately this interferes with the epitaxial layer growth process, producing poor devices. One partial solution to the reflection problem is to pattern the sapphire surface such that it reflects light. This pattern can be a series of microscopic pyramidal structures or more rounded bump like structures on the surface. **FIGURE 5** shows top and side view SEM pictures of some of the patterns produced by manufacturers. These patterns scatter the light and reflect some of it back towards the surface of the device increasing the light output from the LED. In addition to increasing the apparent light output a number of manufacturers have claimed that epitaxial layers grown on patterned substrates is of better quality than that grown on bare sapphire substrates.

Patterned substrates can be produced by the manufacturer of the sapphire substrates. However, factories now exist which begin with a non-patterned substrate and produce specific patterns (normally via chemical etch) for specific LED manufacturers.

Once valued only as a gemstone, sapphire is now an engineered material with a wide variety of industrial uses. These two article have concentrated on its use in mobile devices for everything from camera lens covers to touch sensors and touch screens to the starting material on which most of the solid state lights produced are made. Cost of the material continues to be a limiting factor in its widespread adoption for certain industries. However, as the technology for producing sapphire matures material costs are decreasing and in some ways sapphire substrates have become a commodity rather than a rarity.

Additional reading and viewing material

1. http://rubicontechnology.com/sites/default/files/Opportunities%20for%20Sapphire%20White%20Paper-Rubicon%20Technology.pdf

2. http://www.arc-energy.com/products-services/CHES/Foundations/1

3. https://www.youtube.com/embed/mHrDXyQGSK0

What lies beneath? 50 years of enabling Moore's Law

MIKE CZERNIAK, *Edwards UK, Crawley, England*

Vacuum technology trends can be seen over the period of innovation defined by Moore's Law, particularly in the areas of increasing shaft speed, management of pumping power, and the use computer modeling.

The sub-fab lies beneath. And down there in that thicket of pipes amidst the hum of vacuum pumps, the sentinel of gas combustors and the pulse of muscular machinery doing real work -- innovation has also played a crucial role in enabling Moore's Law. Without it the glamor boys up top with their bunny suits and FOUPS would not have achieved the marvelous feats of engineering derring-do for which they are so deservedly celebrated.

Vacuum and abatement are two of the most critical functions of the sub-fab. Many process tools require vacuum in the process chamber to permit the process to function. Vacuum pumps not only provide the required vacuum, they also remove unused process gases and by-products. Abatement systems then treat those gasses so they are safe to release or dispose. Vacuum and abatement systems in the sub-fab have had to innovate just as dramatically as the exposure, deposition and etch tools of the fab. In many cases, new processes would not have been possible without new vacuum pumps that could handle new materials and new abatement systems that could make those materials safe for release or disposal.

Moore's Law

Moore's Law originated in a paper published in 1965 and titled "Cramming More Components onto Integrated Circuits", written by Gordon Moore, then director of research and engineering at Fairchild Semiconductor [1]. In it Moore observed that the economics of the integrated circuit manufacturing process defined a minimum cost at a certain number of components per circuit and that this number had been doubling every two years as the

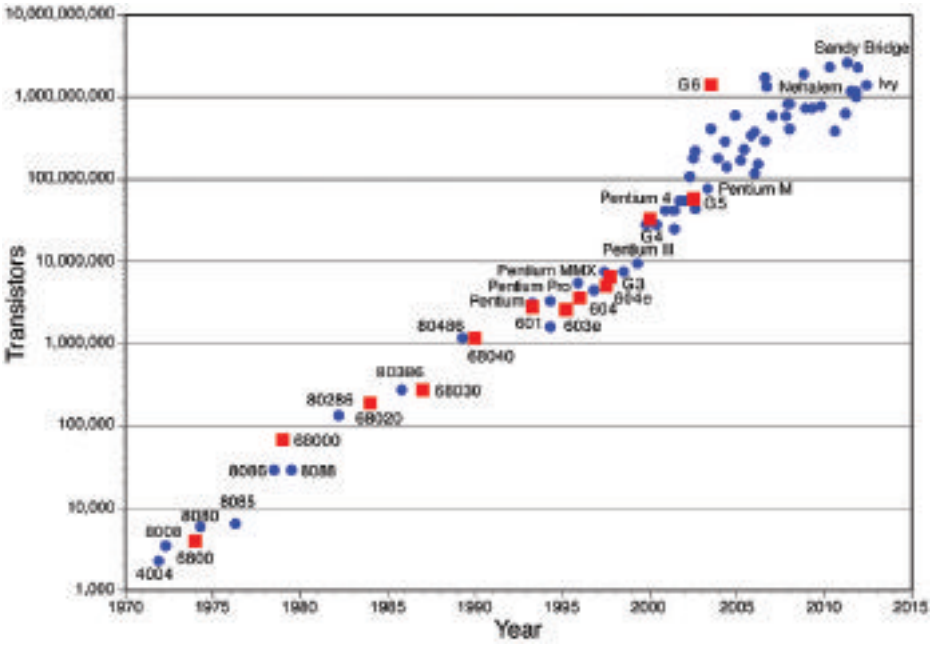

FIGURE 1. A plot of the increasing number of transistors per CPU confirms the accuracy of Moore's prediction. Note that the vertical axis is log scale.

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manufacturing technology evolved. He believed that the trend would continue for at least the short term, and perhaps as long as ten years. His observation became a mantra for the industry, soon to be known as Moore's Law **(FIGURE 1).**

More an astute observation than a law, Moore's Law is remarkable in several respects. First, the rate of improvement it predicts, doubling every two years, is unheard in any other major industry. In "Moore's Curse" (IEEE, March 2015) Vaclav Smil calculated historical rates of improvement for a variety of essential industries over the last couple of centuries and found typical rates of a few percent, and order of magnitude less than Moore's rate [2]. Second, is its longevity. Moore thought it was good for the short term, perhaps as long as ten years. This is perhaps due, at least partly, to the unique role Moore's Law has assumed within the semiconductor industry where it has become both a guide to and driver of the pace of innovation. The Law has become a guiding principle – you shall introduce a new generation with double the performance every two years. It is a rule to live by, enshrined in the industry's roadmap, and violated only at great peril. Only painfully did Intel recently admit that the doubling period for its latest generation appeared to have stretched to something more like two and a half years [3]. To an extent the Law is a self-fulfilling prophecy, which some have argued works to the detriment of the industry when it forces the release of new processes before they are fully optimized. Whatever you might think of it, the Law's persistence is remarkable. The literature is full of dire predictions of its demise, all of which, at least so far, have proven premature.

Finally we must ask, what is meant by the names assigned to each new node? What exactly does 14 nm, the current state of the art, mean? Although Moore originally described the number of components per integrated circuit, the Law was soon interpreted to apply to the density of transistors in a circuit. This was variously construed. Some measured it as the size of the smallest feature that could be created, which determined the length of the transistor gate. Others pointed to the spacing between the lines of the first layer of metal conductors connecting the transistors, the metal-1 half-pitch. These may have been a fairly accurate measures twenty years ago at the 0.35 μm node, but node names have since steadily lost their connection to physical features of the device. It would be difficult to point to any physical dimension at the 14 nm node that is actually 14 nm. For instance, the FinFET transistor in a 22 nm chip is 35 nm long and the fin is 8 nm wide.

What remains true is that in each successive generation the transistors are smaller and more densely packed and performance is significantly increased. Each generation seems to be named with a smaller number that is approximately 70% of the previous generation, reflecting the fact that a 70% shrink in linear dimension equates to a 50% reduction in area and therefore a nominal doubling in transistor density.

Enabling Moore's Law in the sub-fab: A brief chronology

In the 1980s new semiconductor processes and increasing gas flows associated with larger diameter wafers led to problems with aggressive chemicals and solids collecting in the oil used in oil-lubricated "wet" pumps, resulting in short service intervals and high cost of ownership. These were resolved by the development and introduction of oil-free "dry pumps" which have subsequently become the semiconductor industry standard.

Dry rotary pumps require extremely tight running clearances and multiple stages to achieve a practical level of vacuum. Additional cost of these machines, however was more than offset by the benefits offered to semiconductor manufacturing. Dry pumps use a variety of pumping mechanisms -- roots, claw, screw and scroll **(FIGURE 2).**

Many of these are new concepts, but modern machining capabilities made it possible to produce them at a realistic cost, the most notable being Edwards' introduction of the first oil-free dry pump in the 1980's. Each pumping mechanism has been successfully deployed and each has its own advantages and disadvantages in a given application. The scroll pump, for example, is unique in its ability to economically scale down to much smaller sizes.

In the early 1990s it became apparent that with the introduction of dry pumps, the pump oil no longer acted as a "wet scrubber" to collect process by-product gases, which therefore passed into the exhaust system. The solution was the development of the Gas Reactor Column (GRC) to chemically capture process exhaust gases in a disposable/recyclable cartridge, minimizing exhaust emissions to the atmosphere.

At about the same, new, more aggressive process gases being used in leading-edge semiconductor processes posed significant challenges for turbo molecular pumps (TMPs) due to the damage they caused to the

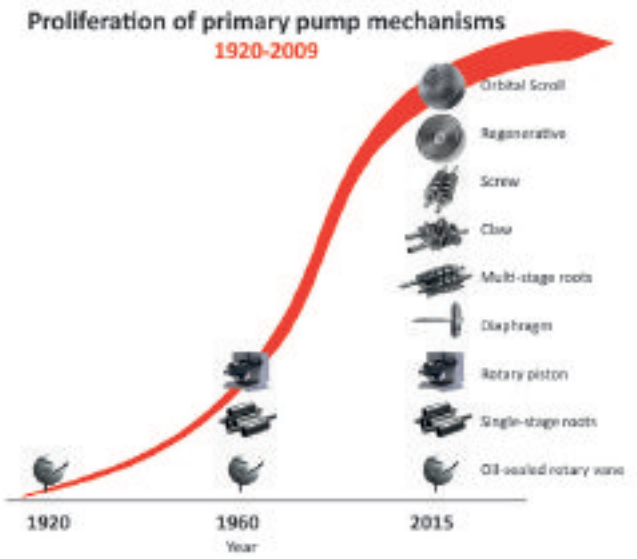

FIGURE 2. Innovation in vacuum technology, inspired by innovation in semiconductor manufacturing process, led to a proliferation of pumping mechanisms, each best suited for particular applications.

mechanical bearings used to support their high-speed rotating shafts (typically ~40,000 rpm). Turbo pumps use rapidly spinning blades to impart direction to gas molecules, propelling them through multiple stages of increasing pressure. Early turbo pumps used oil- or grease-lubricated bearings. Similar to the problems encountered with oil sealed rotary pumps, the new process chemicals tended to degrade the oil, frequently causing pumping failures in as little as a few weeks. This problem was solved by introducing magnetic bearings to levitate the pump drive shaft and eliminate the need for lubricating oil.

In the mid-1990s the semiconductor industry started to use perfluorinated compounds (PFC's) as a convenient source of chamber cleaning and etch gases. However, since only ~30% of the input gas was consumed in the process chamber, there were considerable PFC emissions to the atmosphere. Of particular concern was CF_4 due to its half-life of 50,000 years. The solution was the Thermal Processor Unit which offered the first system with proven destruction reaction efficiency (DRE) of 90% or more for CF_4.

In the 2000's safety concerns regarding the increasing use of toxic gases led to increasing concerns about the abatement of these materials before they were released to the environment and the safety of personnel within the fab. Integrated vacuum and abatement systems, where everything is contained in a sealed and extracted enclosure, offer a significant improvement in safety. Integrated systems have since been refined with improvements such as a common control system, reduced footprint and installation costs, and shorter pipelines to reduce operating and maintenance costs.

Abatement systems have continued to evolve. New processes using new materials often require a different approach the abatement. For example, new technologies were developed for high hydrogen processes, copper interconnects and low k dielectrics.

Trends and prospects

Certain vacuum technology trends can be seen over this history of innovation, particularly in the areas of increasing shaft speed, management of pumping power, and the use computer modeling to monitor performance and predict when maintenance will be required so that it can be synchronized with other activities in the fab.

Shaft Speed

When dry pumps were first introduced, they typically operated at around 3,000 to 3,600 rpm. Today's dry pumps use electric drives to run considerably faster, typically 6,000 rpm for claw, screw, and multi-stage roots pumps **(FIGURE 3).**

Increasing a pump's rotational speed delivers a number of advantages. It makes it possible to build more compact pumps and motors, with less internal leakage, which in turn, enables a reduction in the number of pump stages required. It also allows the speed to be reduced when wafers are not being processed, thereby saving energy. Combined, these benefits help reduce the overall pump cost.

Each type of pumping mechanism has different characteristics in the size and shape of volume to fill. A scroll mechanism, with a narrow, ported inlet and long, thin volume space, is one of the slowest pumping mechanisms to fill, so its performance does not increase in proportion to increasing shaft speed. Most scroll pumps operate at just 1500 rpm. A roots mechanism, by contrast, has a very large opening and a short volume length, enabling it to fill quickly allowing efficient use of higher shaft speeds.

The conductance ceiling for roots and screw pumps is probably ~15,000 rpm. Achieving this speed, will require incremental improvements in materials, bearings, and drives. It is likely that we will reach the conductance ceiling for most of the current primary pumping mechanisms within the next decade, although some, such as roots and screw mechanisms, may prove more durable than others.

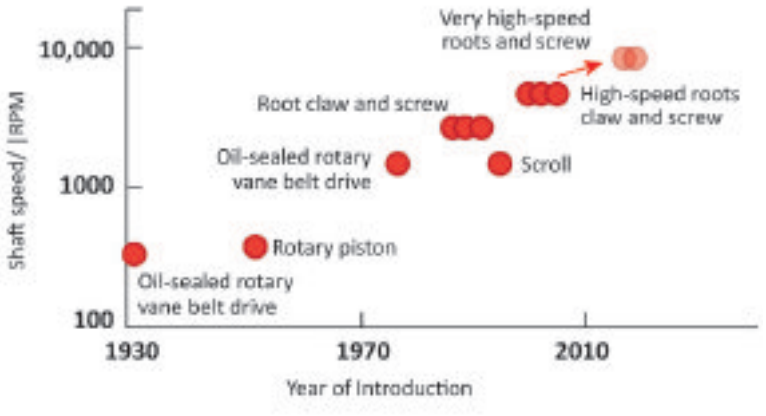

FIGURE 3. Vacuum pump shaft speed has also increased at an exponential rate during the 50 years of Moore's Law.

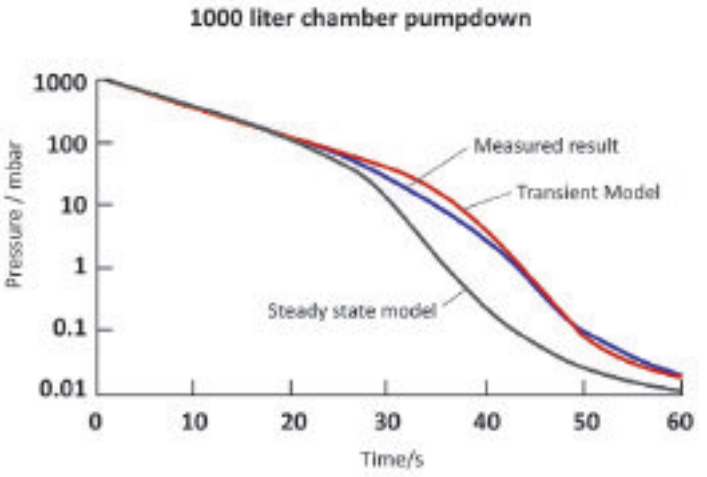

FIGURE 4. Computer modeling allows engineers to experiment with changes the design of vacuum and abatement systems without actually building to system. The plot compares modeled performance to actual performance in pumping down a 1000 liter chamber.

Turbomolecular pump conductance is governed by blade speed and molecular velocities. Turbo performance has been limited primarily by the maximum speed the bearings and rotor can withstand. The industry is looking for new materials that are lighter and stronger to enable increased speed. While this pump type may be reaching its conductive limit on heavier gases, it is far from reaching it for lighter gases, such as hydrogen. This may take a much longer time to achieve.

Power management

Significant advances have been made in improving the energy efficiency of both vacuum pumps and abatement systems. Improvements in pump design have increased energy efficiency. Variable speed motors and controllers allow better matching of the motor speed to varying pump requirements. Idle mode allows both pumps and abatement systems to go into a low power mode when not in use. Improvements in burner design have reduced the fuel consumption of combustion based abatement. With the increase in concern about environmental impact and carbon foot print continued improvement in this area can be expected.

Modeling

Computer modeling has been applied extensively to all stages of pump performance. Such variables as stage size, running clearance, leakage, and conductance can all be modeled quite effectively. This allows design simulation and the optimization of performance, such as the shape of the power and speed curve. In this way, a pump can be designed for specific duties, such as load lock pumping or processing high hydrogen flows **(FIGURE 4).**

Vacuum pumps of the future will be more reliable and capable of operating for longer periods of time before requiring maintenance. They will be safer to operate, will occupy less fab space, run cleaner and require less power, as well as generate less noise, vibration, and heat. They will also have improved corrosion resistance and the ability to run hotter when required.

As a result, vacuum pumps will be more environmentally friendly, running cleaner and using less power to help reduce their carbon footprint. In addition, they will likely make much greater use of recycled materials and use fewer consumables, thereby helping to reduce overall pump costs. The pumps will be easier to clean, repair, and rebuild for reuse.

Likely technical developments will also include higher shaft speeds, a growing proliferation of pump mechanisms and combinations of mechanisms to increase performance. Finally, vacuum pumps will incorporate new materials and improved modelling to further sharpen performance and reduce system and operating costs.

References

1. G. Moore, "Cramming more Components onto Integrated Circuits" in Electronics, April 19, 1965.

2. V. Smil, "Moore's Curse" in IEEE Spectrum, March 19, 2015.

3. R. Courtland, "The Status of Moore's Law: It's Complicated" in IEEE Spectrum October 28, 2013. ◆

Taking 2D materials from lab to fab, and to technology

STEFAN DE GENDT, CEDRIC HUYGHEBAERT, IULIANA RADU *and* **AARON THEAN,** *imec, Leuven, Belgium.*

Due to their exciting properties, 2D crystals like graphene and transition metal dichalcogenides promise to become the material of the future.

As we enter into the era of functional scaling where the cross-roads of More-Moore and More-Than-Moore meet, the search for new devices and their enabling material comes to the forefront of technology research. 2D crystals provide very interesting form-factors with respect to traditional 3D crystals (bulk, Si, and III-V semiconductors). In this elegant 2D form, electronic structure, mechanical flexibility, defect formation, and electronic and optical sensitivity become dramatically different. Aaron Thean: "As researchers at imec explore the physics and applications of such material, it is now becoming important to find a wafer-scale path towards technology implementation and integration of these novel materials." Working closely with research teams across universities and industry partners, the first important step for imec is to enable the flake-to-wafer transition, while concurrently exploring the material, and device-to-circuit applications. The work will build new infrastructure (e.g. epitaxy, metrology, patterning, and electrical characterizations, etc.) around it.

Graphene and beyond

A 2D material is basically formed as a regular network in two dimensions, not extending in the third dimension. It is a monolayer-type of material, where monolayer should be understood as 'up to a few monolayers'. The most known 2D material is graphene, a crystalline monolayer of carbon atoms arranged in a hexagonal honeycomb lattice structure. Recently, the exploration of 2D materials has moved beyond graphene. Stefan De Gendt: "2D materials cover all classes of materials, from semiconductors to insulators to metals. Graphene is a prominent example of a (semi-)metal. Transition metal dichalcogenides (or MX2 with M a transition metal and X a chalcogen such as sulfur or selenium) and hexagonal boron nitrides are well known examples of 2D semiconductors and insulators, respectively."

2D materials: the new silicon?

Many of these materials exhibit remarkable properties that can be exploited in a range of applications. Cedric Huyghebaert: "Graphene, for example, is a fantastic electronic and thermal conductor. It has a record thermal conductivity, a very high intrinsic mobility, a high current density and long mean free path of electrons. Its surface is chemically inert, it has a low surface energy and no out-of-plane dangling bonds. MX2 have versatile properties that complement those of graphene. For example, they have a wide range of bandgaps as opposed to graphene, where the bandgap is absent. In case of graphene, we have to open the bandgap by using e.g. graphene nanoribbons or bilayer graphene."

2D materials represent interesting alternatives to Si-based transistors. Iuliana Radu: "When scaling the gate length of a traditional Si-based MOSFET, overlapping junctions lead to short channel effects which degrade transistor performance. By introducing 2D materials in the channel of the MOSFET, they could show superior

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immunity to short channel effects. 2D materials could therefore extend traditional CMOS scaling beyond its current limits. They are also being considered for tunnel-FET (or TFET) applications, where carrier transport happens through band-to-band tunneling. In principle, 2D materials have no dangling bonds at the interfaces. These dangling bonds are one of the main limiters for TFETs with conventional semiconductors and limit strongly their performance."

2D materials hold promises in other domains as well. Cedric Huyghebaert: "Many applications become possible by integrating these exciting materials in a monolithic way on top of CMOS. In (bio)sensing applications, for example, owing to their ability to adsorb and desorb various atoms and molecules. Or in optoelectronics, where the combination of a low absorption and high carrier mobility turns out very beneficial. Researchers are also assessing the potential of 2D materials to replace copper wires in back-end-of-line interconnects. Finally, 2D materials have been considered for application in domains such as plasmonics, photovoltaics and energy storage, and as transparent electrodes. In the latter applications, the requirements for graphene are less stringent than in aggressive transistor scaling. Therefore, the first graphene-based commercial products will most likely be introduced in one of these domains."

The hamburger experience

Stefan De Gendt: "Ultimately, they potentially enable the engineering of new nano-based stacks: sandwich structures that are composed of various 2D materials, including semiconductors, metals and insulators. This view was nicely described at the 2013 IEDM conference, by the plenary speaker Andrea Ferrari. If you take a hamburger, it's a layered combination of various ingredients, each with a specific flavor. But it's the combination of all these layers that makes the hamburger a unique experience. The same will potentially hold for stacks made up of different 2D materials."

From flakes to large-area synthesis

Applications based on graphene and other 2D materials have become very popular. Many of the above concepts have been successfully demonstrated and have been comprehensively described in scientific journals. However, so far, most of the demonstrations are limited to the lab, using 2D materials in the form of small exfoliated flakes. Iuliana Radu: "The real challenge today is maturing these concepts from flake-based devices towards real products that can be mass produced; only then, can they revolutionize multiple industries. And this has become a key goal at imec. Our goal is to demonstrate the manufacturability of these devices in a 300mm CMOS environment. And we house the expertise to run process flows on these materials **(FIGURE 1)**. At imec, we work on all the unit process steps and on the sequence of steps towards an end application (e.g. TFETs, optical I/O, interconnects), and combine this with modeling and device benchmarking. We also take part in the Graphene Flagship, Europe's 1 billion euro program that covers the whole value chain from materials production to components and systems."

The road towards manufacturability

Due to the nature of the 2D materials, almost every unit process step such as contacting, doping, gate engineering, patterning and etch, etc, is a challenge. These steps, combined with the ability to integrate them into a cleanroom compatible process flow, are however essential to progress towards applications.

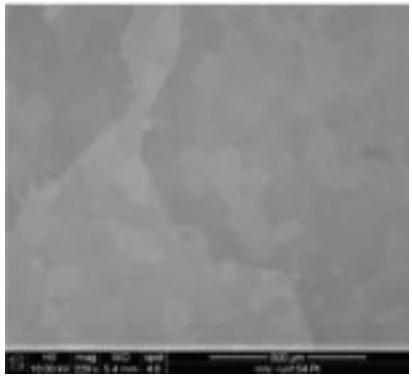

FIGURE 1. Contacts to 2D material: Aggressively scaled contacts to 2D material in order to assess the scaling potential of the material.

Cedric Huyghebaert: "A first challenge is related to the growth of these materials on large area templates, and their subsequent transfer to the final substrate. Graphene, for example, is typically grown on a metal template at high temperatures, up to 1000°C. The template is crucial, since the quality of graphene is very much dependent on the quality of the underlying template. Usually, the better the quality of graphene, the more difficult the transfer process becomes. At imec, we are actively working on the growth and defect-free transfer of graphene **(FIGURES 2 and 3)**. In collaboration with AIXTRON, we focus on the synthesis of large area graphene using AIXTRON BM technology, compatible with 200 and 300mm processes. For the transfer, we rely on our knowledge on 3D Si integration processes. We also work on growth of MX2 materials by a direct sulfurization process or by atomic layer deposition in the 200 and 300mm imec fabs."

Another hurdle is doping of the 2D semiconducting materials, which is needed to tune their energy levels and control their properties. Cedric Huyghebaert: "In the classical way, doping a semiconductor material means replacing an atom in the 3D structure. If you replace an atom in a 2D structure, you have a defect. So we have to consider different ways of doping these materials. At imec, we do this in collaboration with universities. We explore the possibility of achieving for example a semi-permanent doping by interaction with chemical molecules. Besides doping, contacting is also a challenge. The contribution of the electrodes to the total resistance of the device needs to be as low as possible. We therefore look into materials and architectures that allow for the lowest possible contact resistance."

Several applications require a dielectric to be grown on top of the active semiconducting material. Stefan De Gendt: "In case of 2D materials, you have an almost perfectly passivated material, with no anchoring sites for the dielectric to nucleate. Consequently, the more perfect the 2D material, the more defective the dielectric on top may be." Aaron Thean: "This is completely unlike 3D semiconductor processing, where a large part of material functionalization is achieved by surface and bulk material bond breaking and forming reactions, like dopant activation, oxidation, etc. This potential almost dangling-bond free weakly-interacting Van-Der-Waals nano-sheet system gives rise to new process challenges, as well as new opportunities like surface molecular doping and multi-layer channel stacking. One such approach is to transfer a 2D dielectric material to the 2D semiconducting material – like the hamburger experience described before." Imec is working on understanding how to passivate, dope and grow dielectrics on various 2D materials. And there is patterning and etch, litho, and finally, characterization. Iuliana Radu: "We are used to work with 3D bulk materials. But when you need to characterize only one or a few monolayers, there is hardly any material that can take part in the measurement. Therefore, the signals obtained with any classical characterization technique are extremely weak. And this requires new characterization strategies. At imec, we have established procedures that rely in a first phase on the physical characterization of the initial material properties. As the quality of the materials improve, we will cross-correlate physical characterization and electrical behavior of the layers."

Demonstrating the potential

At IEDM 2014, imec and its associated lab at Ghent University have demonstrated an integrated graphene optical modulator on silicon. Cedric Huyghebaert: "Integrated optical modulators with high modulation speed, small footprint and broadband a-thermal operation are highly desired for future chip-level optical interconnects. Due to its fast tunable absorption over a wide spectral range, graphene is well suited to achieve this. We could demonstrate a hybrid graphene-silicon modulator at bit rates up to 10Gb/s. This shows that it is possible to introduce CVD-grown graphene in a high quality Si platform and obtain a performance that can compete with traditional SiGe-based modulators. Moreover, if CVD graphene quality becomes more mature and can be brought into production, we will most probably end up with a device that is far less expensive than today's optical components." ◆

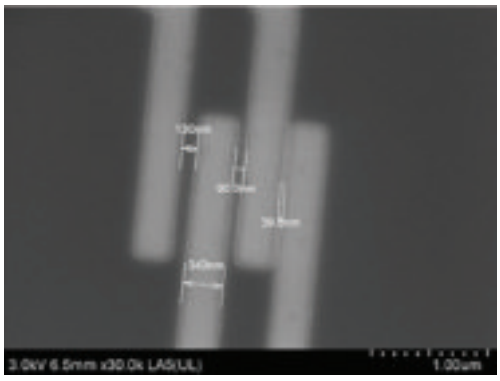

FIGURE 2. Graphene TLM device process: Graphene TLM (transfer length method) device process based on e-beam lithography.

FIGURE 3. Graphene on Pt: Monolayer of graphene grown on Pt foil.

Increasing process steps and the tyranny of numbers

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Forward-looking observations are discussed that will further accelerate the adoption of process control.

Moving to the next design rule can be stressful for the inspection and metrology engineer. Like everything else in the fab, process control generally doesn't get any easier as design rules shrink and new processes are introduced.

The eighth fundamental truth of process control for the semiconductor IC industry is:

Process Control Requirements Increase with Each Design Rule

This statement has proven to be historically accurate, as evidenced by the increase in process control spending as a percentage of wafer front-end (WFE) total costs. This article, however, will focus on a few of the forward-looking observations that we believe will further accelerate the adoption of process control.

The historical increase in process control with shrinking design rules has been driven largely by the introduction of key technical inflections. Recent examples for logic/foundry include immersion lithography, high-k metal gates, gate-last integration, and FinFET transistor structures. These high profile process changes required enormous engineering focus and led to the implementation of new inspection and metrology steps to characterize the associated defectivity and drive yield learning.

While the industry will continue to face significant technical challenges (next-generation lithography being the most obvious example), there is another factor emerging which will play an equally large role in setting the inspection and metrology strategy for the 16/14nm design node and beyond.

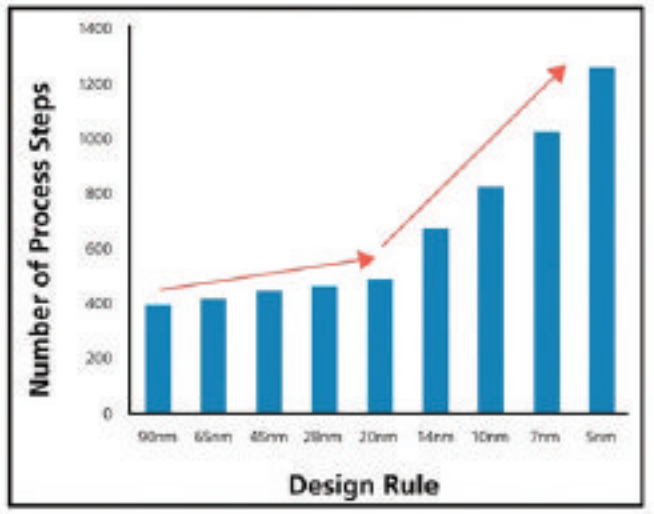

FIGURE 1. The number of process steps will increase dramatically, starting at 16/14nm. [source: IC Knowledge Strategic Cost Model, KLA-Tencor internal data].

FIGURE 1 shows the number of process steps as a function of design rule for a generic logic/foundry process. Up to the 20nm node, there has been a very modest increase in process steps with design rule shrinks due to, for example, more metal levels and the addition of hard mask steps. But starting at 16/14nm, there will be an unprecedented increase in the number of process steps. This jump in process steps will be driven by:

- The shift from 2D to 3D transistor structures in both logic and memory

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- More complicated integration in both the front end and back end
- The push-out of EUV lithography, leading to massive numbers of multi-patterning steps

Process tool defectivity

Because of this increase in process steps—and the accumulative nature of yield loss—fabs must reduce the defectivity at each individual step in order to achieve the same final yield. **FIGURE 2** shows the total yield as a function of the number of process steps where the average per-step yield is held constant. Prior to 16/14nm, this effect was scarcely noticeable since the total increase in process steps was minimal.

Moving forward, fab defect reduction teams must continue to resolve the challenging new technical inflections. But they must also place more focus on driving down defectivity at all process steps:

1. Line Yield: To maintain the same line yield (wafers out / wafers in), there must be fewer excursions and less scrap at each step
2. Die Yield: Every operation in the fab must be held to a tighter specification for defect density (D0) and variation (Cpk)

To make matters worse, defect inspection and metrology operations will continue to become more difficult. The defect count must go down even as the number of yield-relevant defects increases and the detection task becomes harder. Similarly, the variability in metrology measurements must be reduced even as those measurements become more difficult to make.

Impact on cycle time

The increase in process steps has another downside: increased cycle time. If cycle time increases in proportion to the number of process steps then it follows from Figure 1 that the cycle time will roughly double from the 20nm to the 10nm node. One publication has even suggested that the cycle time may double from 20nm to an advanced 16nm process [2].

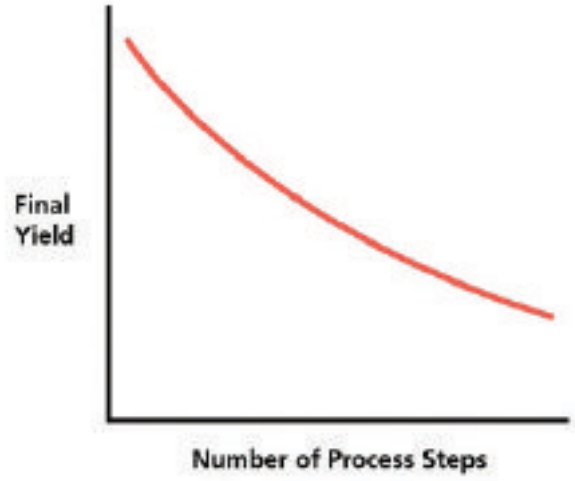

FIGURE 2. The Cumulative (Final) Yield is the product of the per-step yield for each unit operation in the process flow. This chart shows that, for a given average per-step yield, the final yield will decrease as the number of process steps increases.

The fab's ability to do yield learning via feedback from electrical test and physical failure analysis (PFA) is directly tied to the "hot lot" cycle time. Longer hot-lot cycle times mean fewer opportunities for these long-loop learning cycles as device manufacturers try to ramp yield and deliver products to market. More emphasis must therefore be placed on in-line yield learning methodologies.

Sampling pressure

Finally, more process steps will increase the manufacturing cost per wafer. In the second article in this series, Sampling Matters, we showed that the ideal sampling rate (that which provides the lowest total cost to the fab) goes with the square root of the device manufacturing cost. In other words, if the manufacturing cost increases by 30 percent then the corresponding process control sampling rate needs to increase by 14 percent (everything else being constant) to stay at the lowest total cost. This sampling increase will put further pressure on the fab's inspection and metrology teams.

Summary

In summary, each new design rule will introduce:

- Technical inflections that require engineering focus and innovation, as well as the implementation of new process control methodologies
- More process steps that must be directly monitored
- Tighter controls and lower defect density at each individual step due to the compounding nature of yield loss
- Longer cycle times, resulting in more reliance on in-line (vs. end-of-line) techniques for yield learning
- Higher stakes (greater economic impact to the fab) in the event of an excursion due to the higher wafer manufacturing costs, which will put pressure on the fab to increase inspection and metrology sampling

The cascade of challenges that flows from the increase in process steps is sometimes referred to as the "Tyranny of Numbers." For further exploration of how fabs are adapting their process control strategy for new design rules, please contact the authors of this article.

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Europe's secondary industry in the spotlight

The dramatic shift from the trend for increasingly advanced technology to a vast array and volume of application-based devices presents Europe with a huge opportunity. Europe is a world leader in several major market segments – think automotive and healthcare as two examples – and many more are developing and growing at a rapid rate. Europe has the technology and manufacturing skills to satisfy these new markets but they must be addressed cost effectively – and that's where the use of secondary equipment and related services comes in.

While Moore's Law continues to drive the production of advanced devices, the broadening of the "More than Moore" market is poised to explode. All indicators are pointing to a major expansion in applications to support a massive increase in data interchange through sensors and related devices. The devices used to support these applications will range from simple sensors to complex packages but most can, and will, be built by "lower" technology level manufacturing equipment.

This equipment will, in many cases, be required to be "remanufactured" and "repurposed" but will allow semiconductor suppliers to extend the use of their depreciated equipment and/or bring in additional equipment, matched to their process needs, at reduced cost. In many cases this older equipment will need to be supported by advanced manufacturing control techniques and new test and packaging capabilities.

SEMI market research shows that investment in "legacy" fabs is important in manufacturing semiconductor products, including the emerging Internet of Things (IoT) class of devices and sensors, and remains a sizeable portion of the industries manufacturing base:

- 150mm and 200mm fab capacity represent approximately 40 percent of the total installed fab capacity
- 200mm fab capacity is on the rise, led by foundries that are increasing 200mm capacity by about 7 percent through to 2016 compared to 2012 levels
- New applications related to mobility, sensing, and IoT are expected to provide opportunities for manufacturers with 200mm fabs

PETER CONNOCK, *Chairman of memsstar**

Out of the total US$ 27 billion spent in 2013 on fab equipment and US$ 31 billion spent on fab equipment in 2014, secondary fab equipment represents approximately 5 percent of the total, or US$ 1.5 billion, annually, according to SEMI's 2015 secondary fab equipment market report. For 2014, 200mm fab investments by leading foundries and IDMs resulted in a 45 percent increase in spending for secondary 200mm equipment.

Secondary equipment will form at least part of the strategy of almost anyone manufacturing or developing semiconductors in Europe. In many cases, it is an essential capability for competitive production. As the secondary equipment industry increases its strategic importance to semiconductor manufacturers and researchers it is critical that the corresponding supply chain ensures a supply of quality equipment, support and services to meet rapidly developing consumer needs.

Common challenges across the supply chain include:

- How to generate cooperation across Europe between secondary equipment users and suppliers and what sort of cooperation is needed?
- How to ensure the availability of sufficient engineering resource to support the European secondary installed base?
- Are there shortages of donor systems or critical components that are restricting the use of secondary equipment and, if so, how might this be resolved

Europe's secondary industry will be in the spotlight during two sessions at SEMICON Europa 2015:

- Secondary Equipment Session – Enabling the Internet of "Everything"?
- SEA Europe 'Round Table' Meeting

The sessions are organised by the SEMI SEA Europe Group and are open to everyone associated with the secondary industry, be they device manufacturer or supplier, interested in the development of a vibrant industry providing critical support to cost effective manufacturing in Europe.

**The author is also co-chair of the European SEMI Secondary Equipment and Applications Special Interest Group.* ◆

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