Sold State Insights for Electronics Manufacturing

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Solid State TECHNOLOGY

OCTOBER 2016 VOL. 59 NO. 7

Computational Fluid Dynamic Modeling was used to model temperature and fuel flow around the pilot assembly of the combustor used in the Edwards exhaust management system. Source: Edwards.

FEATURES



SOVER

EXHAUST MANAGEMENT | Managing particle flows in process exhaust for safety and profitability Solid particles in the abatement exhaust must be properly managed, and in some cases, substantially reduced from the gas stream before it is released into the environment.

Chris Jones, Edwards Vacuum, Ltd., Clevedon, U.K



PARAMETRIC TEST | van der Pauw and Hall voltage measurements with a parameter analyzer van der Pauw measurements with a parameter analyzer are examined followed by a look at Hall effects measurements. *Jeongdong Choe, TechInsights, Ottawa, Canada*



BUSINESS | What is your China strategy?

China has renewed its investments in displays, packaging, and both 200mm and 300mm front-end fab capacity. *Dave Lammers, Contributing Editor*



CONTAMINATION CONTROL | Reducing ESD in semiconductor fluoropolymer

fluid handling systems while maintaining chemical purity

Fluoropolymer Electrostatic Discharge (ESD) tubing reduces electrostatic charge to levels below the ignition energy of flammable semiconductor chemicals and maintains chemical purity, ensuring safety and improving process yields. *Mark Caulfield, John Leys, Jim Linder and Brett Reichow, Entegris, Billerica, MA*



CONFERENCE | Preview: 2016 IEEE International Electron Devices Meeting The 62nd annual IEDM will be held in San Francisco December 3 - 7, 2016.

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editorial

The ConFab 2017, May 14-17, in San Diego

I'm delighted to announce that The ConFab, our premier semiconductor manufacturing conference and networking event, will be held at the iconic Hotel del Coronado in San Diego on May 14-17, 2017. For more than 12 years, The ConFab, an invitation-only executive conference, has been the destination for key industry influencers and decision-makers to connect and collaborate on critical issues.

The ConFab is the best place to seek a deeper understanding on these and other important issues, offering a unique blend of market insights, technology forecasts and strategic assessments of the challenges and opportunities facing semiconductor manufacturers. In changing times, it's critical for people to get together in a relaxed setting, learn what's new, connect with old friends, make new acquaintances and find new business opportunities, and that's what The ConFab is all about.

I'm also pleased to announce the addition of David J. Mount to The ConFab team as marketing and business development manager. Mount has a rich history in the semiconductor manufacturing equipment business and will be instrumental in guiding continued growth, and expanding into new high growth areas. Mainstream semiconductor technology will remain the central focus of The ConFab, and the conference will be expanded with additional speakers, panelists, and VIP attendees who will participate from other fast growing and emerging areas. These include biomedical, automotive, IoT, MEMS, LEDs, displays, thin film batteries, photonics and advanced packaging. From both the device maker and the equipment supplier perspective, The ConFab 2017 is a must-attend networking conference for business leaders.

The ConFab conference program is guided by a stellar Advisory Board, with high level representatives from GlobalFoundries, Texas Instruments, TSMC, Cisco, Samsung, Intel, Lam Research, KLA-Tencor, ASE, NVIDIA, the Fab Owners Association and elsewhere.

Details on the invitation-only conference are at: www. theconfab.com. For sponsorship inquiries, contact Kerry Hoffman at khoffman@extensionmedia.com. For those interested in attending as a guest or qualifying as a VIP, contact Sally Bixby at sbixby@extensionmedia.com.

-Pete Singer, Editor-in-Chief

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Web Exclusives

Linde launches Asian R&D Center in Taiwan

Timed in coordination with SEMICON Taiwan 2016 happening in early September, The Linde Group launched a new electronics R&D Center in Taichung, Taiwan. "We had a fabulous opening, with 35 to 40 customers and 20 people from the Taiwanese government such as ITRI," said Carl Jackson, Head of Electronics, Technology and Innovation at The Linde Group, in an exclusive interview with SemiMD. This new R&D center represents an investment of approximately EUR 5m to support local customers and development partners throughout the Asia Pacific region with its state-of-the-art analytical and product development laboratory.

http://bit.ly/2ddD0e7

Silicon as disruptive platform for IoT applications

Marie Semeria, chief executive officer of CEA-Leti, sat down with SemiMD during SEMICON West to discuss how the French R&D and pilot manufacturing campus—located at the foot of the beautiful French alps near Grenoble—is expanding the scope of it's activities to develop systems solutions for the Internet-of-Things (IoT). (From SemiMD.com) http://bit.ly/2cXtj3n

Edwards Vacuum on safety protocols in the fab environment

Pete Singer and Geoffrey Stoddart, Global Services Marketing Director, Edwards Vacuum, met up at SEMICON West 2016 to discuss ROI associated with safety investments in a fab setting, effective communication on fab safety topics, and raising awareness of safe wafer processing practices.

http://bit.ly/2cLLEzl



The ConFab 2017 expands

The semiconductor industry is rapidly evolving and changing. Consolidations, mergers and acquisitions in the entire supply chain, the end of Moore's Law (as we knew it), and the success of the foundry model has led us to seek new directions and expansions for The ConFab.

http://bit.ly/2cpKGtX

Sony introduces Ziptronix DBI technology in Samsung Galaxy S7

Many of us stated in 2007 that further advances could be obtained by removing the CMOS circuitry to a separate layer and forming a true 3D chip stack, but the technology implementation had to wait while the industry first converted to back side imaging technology.

http://bit.ly/2cZgXdl

Samsung's Galaxy Note 7 is more than the batteries

As usual, within days of the August 19 launch of the Samsung Galaxy Note 7, the Chipworks lab had it in pieces and had identified most of the significant components that were inside.

http://bit.ly/2cyJcuY

Global semiconductor sales rebound in July

The Semiconductor Industry Association (SIA) announced worldwide sales of semiconductors reached \$27.1 billion for the month of July 2016, an increase of 2.6 percent compared to the previous month's total of \$26.4 billion.

http://bit.ly/2deGXRM

Established technology nodes: The most popular kid at the dance

While the market potential of established nodes is growing, so is the complexity and difficulty of validating designs that push these nodes far beyond their original capabilities. The new reality is challenging designers using EDA tools that were not available when the nodes were brand new. We're learning that EDA tools are not frozen to the node, but must advance at these advanced established nodes just as they do at the leading-edge nodes. Design teams working at advanced established nodes have the option to upgrade their tools and make their life much easier.

http://bit.ly/2bDSg62

Please send news articles to sdavis@extensionmedia.com

worldnews

ASIA – TSMC and Synopsys announced a collaboration to develop an interface and foundation IP for 7nm FinFET process.

USA - Nordson Corporation announced it plans to combine its existing screw and barrel operations in Youngstown, Ohio; New Castle, Pennsylvania; and Pulaski, Virginia into a single expanded manufacturing center of excellence in Austintown, Ohio.

ASIA - Applied Materials and the Institute of Microelectronics announced a five-year extension of their research collaboration at the Centre of Excellence in Advanced Packaging in Singapore.

USA - GLOBALFOUNDRIES introduced a scalable, embedded magnetoresistive non-volatile memory technology (eMRAM) on its 22FDX platform.

EUROPE - Nanoelectronics research center **imec** announced that Kris Myny, one of its young scientists, has been awarded an ERC Starting Grant. The grant of 1.5 million euros is earmarked to open up new research horizons in the field of thin-film transistor technology.

USA - Semiconductor Research Corporation presented its highest honors Sept. 12 to professors from University of California, Berkeley and University of Minnesota at SRC's annual TECHCON conference in Austin, Texas.

ASIA - Qualcomm Incorporated announced the opening of Qualcomm Communication Technologies Co. Ltd., a semiconductor test facility in the Waigaoqiao free-trade zone in Shanghai.

USA - SPTS Technologies announced its collaboration with Novati Technologies to establish Novati's new plasma dicing line at their fab in Austin, Texas.



GLOBALFOUNDRIES extends FDX roadmap with 12nm FD-SOI technology

GLOBALFOUNDRIES unveiled a new 12nm FD-SOI semiconductor technology, extending its leadership position by offering the industry's first multi-node FD-SOI roadmap. Building on the success of its 22FDX offering, the company's next-generation 12FDX platform is designed to enable the intelligent systems of tomorrow across a range of applications, from mobile computing and 5G connectivity to artificial intelligence and autonomous vehicles.

As the world becomes more and more integrated through billions of connected devices, many emerging applications demand a new approach to semiconductor innovation. The chips that make these applications possible are evolving into mini-systems, with increased integration of intelligent components including wireless connectivity, non-volatile memory, and power management—all while driving ultra-low power consumption. GLOBALFOUNDRIES' new 12FDX technology is specifically architected to deliver these unprecedented levels of system integration, design flexibility, and power scaling. 12FDX sets a new standard for system integration, providing an optimized platform for combining radio frequency (RF), analog, embedded memory, and advanced logic onto a single chip. The technology also provides the industry's widest range of dynamic voltage scaling and unmatched design flexibility via software-controlled transistors—capable of delivering peak performance when and where it is needed, while balancing static and dynamic power for the ultimate energy efficiency.

"Some applications require the unsurpassed performance of FinFET transistors, but the vast majority of connected devices need high levels of integration and more flexibility for performance and power consumption, at costs FinFET cannot achieve," said GLOBALFOUNDRIES CEO Sanjay Jha. "Our 22FDX and 12FDX technologies fill a gap in the industry's roadmap by providing an alternative path for the next generation of connected intelligent systems. And with

Continued on page 7

Lam Research introduces dielectric atomic layer etching capability for advanced logic

Lam Research Corp., an advanced manufacturer of semiconductor equipment, today announced that it is expanding its atomic layer etching (ALE) portfolio with the addition of ALE capability on its Flex dielectric etch systems. Enabled by Lam's Advanced Mixed Mode Pulsing (AMMP) technology, the new ALE process has demonstrated the atomic-level control needed to address key challenges in scaling logic devices to 10nm and below. First in the industry to use plasma-enhanced ALE in production for dielectric films, the latest Flex system has been adopted as tool of record for highvolume manufacturing of logic devices.

"From transistor and contact creation to interconnect patterning, a new level of precision is needed by logic manufacturers to continue scaling beyond the 10nm technology node," said Vahid Vahedi, group vice president, Etch Product Group. "For device-enabling applications like selfaligned contacts, where etch helps create critical structures, conventional technologies do not provide sufficient control for the stringent specifications now demanded. Our latest Flex product with dielectric ALE

Continued on page 8

TowerJazz and SMIC's sales forecast to surge in 2016

IC Insights released its August Update to the 2016 McClean Report earlier this month. This Update included an update of the semiconductor industry capital spending forecast, a look at the top-25 semiconductor suppliers for 1H16, including a forecast for the full year ranking, and Part 1 of an extensive analysis of the IC foundry industry (the ranking of the top-10 pure-play foundries is covered in this research bulletin).

In 2014, the pure-play IC foundry market registered a strong 17% increase, the largest increase since 2010 and eight points greater than the 9% increase in the worldwide IC market. In 2015, the pure-play foundry market showed a 6% increase, about one-third the rate of growth in the previous year, but seven points higher than the total IC market growth rate of -1%. For 2016, the pure-play foundry market is expected to increase by 9% and greatly outperform the growth rate of total IC market, which is forecast to drop by 2% this year.

Top 10 Pure-Play Foundry Companies

2016F Kank	2015 Rank	Company (Headquarters)	2014 Sules (386)	1613 % Dunge	2814 Share at Total	2015 Sales (3M)	15/14 % Change	2915 Share at Total	States (BM)	1815 % Change	2016 Strate of Total
T	1	TSMC (Taiward	34,975	25%	88%	26,438	4%	68%	38,879	8%	88%
	2	GipbalFoundries (U.S.)1	4,355	8%	18%	5,818	15%	11%	5,645	12%	11%
	. 2	LINC Group (Talwan)	4,331	8%	18%	4,464	275	10%	4,490	1%	#76
4	4	SMIC (China)	1,976	8%	5%	2,234	14%	5%	2,859	37%	4%
		TowerJazz (Innel)	828	64%	2%	961	18%	25	1,245	30%	3%
	-5	Powership (Talward	1,291	8%	. 3%	1,268	-2%	3%	1,240	4%	3%
1	7	Verguard (Taleon)	790	11%	2%	736	-75	2%	780	4%	1%
		Hua Hong Sami (China)	665	14%	275	613	4%	194	780	8%	1%
		Dongbu HiTek (5. Korwa)	581	20%	1%	593	18%	115	640	8%	1%
10	10	SSMC (Singapore)	480	-3%	175	414	-115	7%	470	(1%)	115
	-	Others	2,130	3%	375	2,262	375	875	2,485	3%	- 8%
-	-	Total	42,396	17%	100%	45,192	4%	100%	48.195	9%	100%

Source: 12 Insights, company reports

Figure 1 shows that the top 10 pure-play foundries are expected to hold 95% of the total pure-play foundry market this year. This year, the "Big 4" pure-play foundries (i.e., TSMC, GlobalFoundries, UMC, and SMIC) are forecast to hold

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Fab equipment spending ascending

By Christian G. Dieseldorff, Industry Research & Statistics Group at SEMI

SEMI's Industry Research and Statistics group has published its August update of the World Fab Forecast report. The report has served the industry for 24 years, observing and analyzing spending, capacity, and technology changes for all front-end facilities worldwide, from high-volume to R&D fabs. SEMI's latest data show increasing equipment spending, reaching 4.1 percent YOY in 2016 and 10.6 percent in 2017. **Figure 1** (below) shows a forecast of -2 percent decline from 2H2015 to 1H2016 and an 18 percent increase from 1H2016 to. 2H2016.

The largest growth drivers for the industry are mobile devices (including devices using SSDs), automotive, and soon anticipated to be IoT, with these applications, in many cases, requiring 3D NAND and Logic 10nm/7nm.

The SEMI report indicates that the two industry segments leading to the biggest increase in 2H16 are Foundry (29 percent) and Memory (21 percent). Growth in Memory is driven by a significant increase in 3D NAND spending in 2016. Comparing 2016 to 2017, Foundry growth remains quite steady, with a 14 percent increase in 2016 and 13 percent in 2017.

Companies like Samsung, Micron, Flash Alliance, Intel, and SK Hynix drive Memory growth with 3D NAND to an astounding 152 percent increase in 2016 and 29 percent in 2017. However, utilization of all this equipment is still low in 2016 but is expected to increase in 2017.

Looking at other product segments, DRAM equipment spending is expected to decline by 31 percent in 2016 and then recover slightly with 2 percent growth in 2017. Power

Fab Equipment Spending by Quarter



FIGURE 1.

Region	2015	2016	2017	Change 2016	Change 2017
Americas	\$ 5,031	\$ 4,714	\$ 5,041	-6.3%	6.9%
China	\$ 4,787	\$ 7,869	\$ 7.422	64.4%	-5.7%
Europe & Mideast	\$ 2,104	\$ 1,530	\$ 2,446	-27.3%	59.9%
Japan	\$ 5,402	\$ 4,495	\$ 5,059	-16.8%	12.5%
Korea	\$ 8,083	\$ 6,797	\$ 9,127	-15.9%	34.3%
SE Asia	\$ 1,079	\$ 2,778	\$ 2,746	157.5%	-1.2%
Taiwan	\$ 9,505	\$ 9,268	\$ 9,584	-2.5%	3.4%
Total	\$ 35,991	\$ 37,452	\$ 41.474	4.1%	10.6%

Fab Equipment Spending by Region

Source: World Fab Forecast report, SEMI August 2016

FIGURE 2.

devices also show strong growth with 25 percent in 2016 and 16 percent in 2017. The Analog segment will slump by -15 percent in 2016 but increase by 20 percent in 2017. Similarly, MPU will drop -20 percent in 2016 and then is expected to increase by 48 percent in 2017.

Comparing spending by region in 2016, SE Asia shows the largest growth, with 157 percent in 2016, driven mainly by 3D NAND (see **Figure 2**).

China, in third place for overall spending, shows 64 percent growth for 2016 primarily due to 3D NAND by non-Chinese companies, closely followed by Foundry companies. Although the largest spenders in China currently are overseas device companies, China-based chipmakers are starting to pick up investment activity.

By contrast, the largest growth rate in 2017 is in Europe/ Mideast with about 60 percent which is mainly due to ramping of 10nm facilities. Korea is in second place for total spending, mainly driven by Samsung's investment in DRAM and Flash. Japan in third place driven by Flash Alliance (3D NAND).

The World Fab Forecast report provides more detailed information by company and fab for construction spending, equipment spending and capacities by region and product type. Since the last publication in May 2016, the SEMI research team has made over 330 changes to 300 facilities/lines. This includes 27 new records and 18 records closed.

For information about semiconductor manufacturing for the remainder of 2016 and in 2017, and for details about capex for construction projects, fab equipping, technology levels, and products, order the SEMI World Fab Forecast Report.

The report, in Excel format, tracks spending and capacities for over 1,100 facilities including over 82 future facilities, across industry segments from Analog, Power, Logic, MPU, Memory, and Foundry to MEMS and LEDs facilities. Using a bottoms-up approach methodology, the SEMI Fab Forecast provides highlevel summaries and graphs, and in-depth analyses of capital expenditures, capacities, technology and products by fab.

The SEMI Worldwide Semiconductor Equipment Market Subscription (WWSEMS) data tracks only new equipment for fabs and test and assembly and packaging houses. The SEMI World Fab Forecast and its related Fab Database reports track any equipment needed to ramp fabs, upgrade technology nodes, and expand or change wafer size, including new equipment, used equipment, or in-house equipment. Also check out the Opto/LED Fab Forecast. Learn more about the SEMI fab databases at: www.semi.org/MarketInfo/FabDatabase and www.youtube.com/user/SEMImktstats ◆

GLOBALFOUNDRIES, Continued from page 4

our FDX platforms, the cost of design is significantly lower, reopening the door for advanced node migration and spurring increased innovation across the ecosystem."

GLOBALFOUNDRIES' new 12FDX technology is built on a 12nm fully-depleted silicon-on-insulator (FD-SOI) platform, enabling the performance of 10nm FinFET with better power consumption and lower cost than 16nm FinFET. The platform offers a full node of scaling benefit, delivering a 15 percent performance boost over today's FinFET technologies and as much as 50 percent lower power consumption.

"Chip manufacturing is no longer one-shrink-fits-all. While FinFET is the technology of choice for the highest-performance products, the industry roadmap is less clear for many cost-sensitive mobile and IoT products, which require the lowest possible power while still delivering adequate clock speeds," said Linley Gwennap, founder and principal analyst of the Linley Group. "GLOBALFOUNDRIES' 22FDX and 12FDX technologies are well positioned to fill this gap by offering an alternative migration path for advanced node designs,

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particularly those seeking to reduce power without increasing die cost. Today, GLOBALFOUNDRIES is the only purveyor of FD-SOI at 22nm and below, giving it a clear differentiation."

"When 22FDX first came out from GLOBALFOUNDRIES, I saw some game-changing features. The real-time tradeoffs in power and performance could not be ignored by those needing to differentiate their designs," said G. Dan Hutcheson, chairman and CEO of VLSI Research. "Now with its new 12FDX offering, GLOBALFOUNDRIES is showing a clear commitment to delivering a roadmap for this technology — especially for IoT and Automotive, which are the most disruptive forces in the market today. GLOBALFOUNDRIES' FD-SOI technologies will be a critical enabler of this disruption."

"FD-SOI technology can provide real-time trade-offs in power, performance and cost for those needing to differentiate their designs," said Handel Jones, founder and CEO, IBS, Inc. "GLOBALFOUNDRIES' new 12FDX offering delivers the industry's first FD-SOI roadmap that brings the lowest cost migration path for advanced node design, enabling tomorrow's connected systems for Intelligent Clients, 5G, AR/VR, Automotive markets."

GLOBALFOUNDRIES Fab 1 in Dresden, Germany is currently putting the conditions in place to enable the site's 12FDX development activities and subsequent manufacturing. Customer product tape-outs are expected to begin in the first half of 2019.

"We are excited about the GLOBALFOUNDRIES 12FDX offering and the value it can provide to customers in China," said Dr. Xi Wang, Director General, Academician of Chinese Academy of Sciences, Shanghai Institute of Microsystem and Information Technology. "Extending the FD-SOI roadmap will enable customers in markets such as mobile, IoT, and automotive to leverage the power efficiency and performance benefits of the FDX technologies to create competitive products."

"NXP's next generation of i.MX multimedia applications processors are leveraging the benefits of FD-SOI to achieve both leadership in power efficiency and scaling performance-on-demand for automotive, industrial and consumer applications," said Ron Martino, vice president, i.MX applications processor product line at NXP Semiconductors. "GLOBALFOUNDRIES' 12FDX technology is a great addition to the industry because it provides a next generation node for FD-SOI that will further extend planar device capability to deliver lower risk, wider dynamic range, and compelling costperformance for smart, connected and secure systems of tomorrow."

"As one of the first movers of design for FD-SOI, VeriSilicon leverages its Silicon Platform as a Service (SiPaaS) together with experience in delivering best-in-class IPs and design services for SoCs," said Wayne Dai, president and CEO of VeriSilicon. "The unique benefits of FD-SOI technologies enable us to differentiate in the automotive, IoT, mobility, and consumer market segments. We look forward to extending our collaboration with GLOBALFOUNDRIES on their 12FDX offering and providing high-quality, low-power and costeffective solutions to our customers for the China market."

"12FDX development will deliver another breakthrough in power, performance, and intelligent scaling as 12nm is best for double patterning and delivers best system performance and power at the lowest process complexity," said Marie Semeria, CEO of Leti, an institute of CEA Tech. "We are pleased to see the results of the collaboration between the Leti teams and GLOBALFOUNDRIES in the U.S. and Germany extending the roadmap for FD-SOI technology, which will become the best platform for full system on chip integration of connected devices."

"We are very pleased to see a strong momentum and a very solid adoption from fabless customers in 22FDX offering. Now this new 12FDX offering will further expand FD-SOI market adoption," said Paul Boudre, Soitec CEO. "At Soitec, we are fully prepared to support GLOBALFOUNDRIES with high volumes, high quality FD-SOI substrates from 22nm to 12nm. This is an amazing opportunity for our industry just in time to support a big wave of new mobile and connected applications."

LAM Research, Continued from page 4

delivers atomic-scale control with proven productivity to meet customers' key requirements."

To continue logic device scaling, chipmakers are adopting new integration schemes such as those using self-aligned contacts (SACs) in order to address issues like RC delay. As a result, contact etch has become one of the most crucial processes, directly impacting both wafer yield and transistor performance. In order to define critical device structures with high fidelity, the etch process requires directional (anisotropic) capability with ultra-high selectivity, while also delivering the productivity needed for manufacturing. For next-generation logic and foundry applications, Lam's Flex dielectric etch systems offer the industry's most advanced capacitively coupled plasma (CCP) reactor, featuring a unique, smallvolume design to deliver repeatable results. The latest system uses proprietary AMMP technology to enable ALE of dielectric films such as silicon dioxide (SiO2). This capability results in a 2x improvement in selectivity over previous dielectric etch technologies while delivering atomic-level control.

TowerJazz and SMIC, Continued from page 5

an imposing 84% share of the total worldwide pure-play IC foundry market. As shown, TSMC is expected to hold a 58% marketshare in 2016, down one point from 2015, as its sales are forecast to increase by \$2.1 billion this year, up from a \$1.5 billion increase in 2015. GlobalFoundries, UMC, and SMIC's combined share is expected to be 26% this year, the same as in 2015.

The two top-10 pure-play foundry companies that are forecast to display the highest growth rates this year are Israel-based TowerJazz, which is expected to edge-out Powerchip for the 5th spot in the pure-play foundry ranking in 2016, and China-based SMIC, with 30% and 27% sales increases, respectively. TowerJazz and SMIC have been on a very strong growth curve over the past few years. TowerJazz is expected to grow from \$505 million in sales in 2013 to \$1,245 million in 2016 (a 35% CAGR) while SMIC is forecast to more than double its revenue from 2011 (\$1,220 million) to 2016 (\$2,850 million) and register a 19% CAGR over this five-year timeperiod. Eight of the top-10 pure-play foundries listed in Figure 1 are based in the Asia-Pacific region. Israel-based TowerJazz, and U.S.-headquartered GlobalFoundries are the only non-Asia-Pacific companies in the top-10 group. While LFoundry is currently headquartered in Avezzano, Italy, China-based SMIC agreed in 2Q16 to purchase 70% of the company for approximately \$55 million. Since LFoundry has an installed capacity of 40K 200mm wafers/month, the acquisition of a controlling interest in the company essentially serves to immediately expand SMIC's capacity by 13% this year.

Although SMIC is forecast to register strong sales growth of 27% this year, Chinese foundries, in total, are expected to hold only 8.2% of the pure-play foundry market in 2016, down 5.1 points from the peak share of 13.3% reached in 2006 and 2007. IC Insights believes that the total Chinese company share of the pure-play foundry market will increase through 2020, as the China-based foundries take advantage of the huge amount of government and private investment that will be flowing into the Chinese semiconductor market infrastructure over the next five years.

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CMOS image sensor update

Toshiba was the first to commercially implement CMOS image sensors with backside TSV last technologies in 2007. Many of us stated in 2007 that further advances could be obtained by removing the CMOS circuitry to a separate layer and forming a true 3D chip stack, but the technology implementation had to wait while the industry first converted to back side imaging technology.

With a conventional front-illumination structure, the metal wiring above the sensor's photo-diodes impede photon gathering. A back-illuminated structure increases the amount of light that enters each pixel due to the lack of obstacles such as metal wiring and transistors that have been moved to the reverse of the silicon substrate.

The next generation, as expected, combined both BSI and stacking. Conventional CMOS image sensor technology creates the pixel function and analog logic circuitry on the same chip. The motivations for stacked chip CIS include: optimization of each function in the stack, adding functionality to the stack and decreasing form factor.

Since the pixel section and circuit section are formed as independent chips, each function can be separately optimized, enabling the pixel section to deliver higher image quality while the circuit section can be specialized for higher functionality. In addition, faster signal processing and lower power consumption can also be achieved through the use of leading process for the chip containing the circuits.

The 2014 image sensor market was estimated by Techno Systems Research with Sony as the top seller of image sensors with 40.2% market share, followed by OmniVision (15.7%), Samsung (15.2%) and others with 28.9%.

Sony is clearly leading in commercializing the latest CIS packaging technologies. Some of the biggest names in tech use Sony sensors: The iPhone 6 camera has a Sony sensor, as does the Samsung Galaxy S6, Motorola phones, Nikon DSLRs, and Olympus mirrorless cameras.

Earlier in 2016 it was reported that there are two versions of the Samsung Galaxy S7. One has a Samsung stacked

ISOCELL sensor (S5K2L1) and the other a special Sony stacked sensor (IMX260).

PHIL GARROU, Contributing Editor

The recent Chipworks teardown of the Samsung Galaxy S7 with a Sony IMX 260 revealed BSI stacked technology. Furthermore, it revealed the first reported use of the Ziptronix (now Tessera) Direct Bond interconnect (DBI) technology rather than prior oxide –oxide bonding with subsequent TSVs connecting through the oxide interface. This BSI-stacked DBI technology is possibly the next step in the CIS roadmap.

The Chipworks cross-section reveals a 5 metal (Cu) CMOS image sensor (CIS) die and a 7 metal (6 Cu + 1 Al) image signal processor (ISP) die. The Cu-Cu vias are 3.0 μ m wide and have a 14 μ m pitch in the peripheral regions. In the active pixel array they are also 3.0 μ m wide, but have a pitch of 6.0 μ m.

Omnivision was the first to sample BSI in 2007 but costs were too high and adoption was thus very low. In 2015 Omnivision announced their OV 16880 a 16-megapixel image sensor built on OmniVision's PureCel-S[™] stacked die technology.

Samsung's first entrant into stacked technology with TSV was also at 16MP with the Samsung S5K3P3SX in late 2014. The CIS die is face-to-face bonded to a 65nm Samsung image signal processor die and connected with W based TSV. The CIS die is fabricated on a 65nm CMOS process with 5 levels of interconnect.

In early 2015 On Semiconductor (Aptina) introduced its first stacked CMOS sensor the AR 1335 with $1.1\mu m$ pixels. It resulted in a smaller die footprint, higher pixel performance and better power consumption compared to their traditional monolithic non-stacked designs. They announced that it would be introduced in commercial products in late 2015.

In late 2015, Olympus announced the OL 20150702-1 a new 3D stacked 16MP CMOS image sensor. �

Packaging



3D-NAND deposition and etch integration



k ED KORCZYNSKI, n- Sr. Technical Editor

3D-NAND chips are in production or pilot-line manufacturing at all major memory manufacturers, and they are expected to rapidly replace most 2D-NAND chips in most applications due to lower costs and greater reliability. Unlike 2D-NAND which was enabled by lithography, 3D-NAND is deposition and etch enabled. "With 3D-NAND you're talking about 40nm devices, while the most advanced 2D-NAND is running out of steam due to the limited countable number of stored electrons-per-cell, and in terms of the repeatability due to parasitics between adjacent cells," said Harmeet Singh, corporate vice president of Lam Research.

Though each NAND manufacturer has different terminology for their unique 3D variant, from a manufacturing process integration perspective they all share similar challenges in the following simplified process sequences:

- 1. Deposition of 32-64 pairs of blanket "mold stack" thin-films,
- 2. Word-line hole etch through all layers and selective fill of NAND cell materials, and
- 3. Formation of "staircase" contacts to each cell layer.

Each of these unique process modules is needed to form the 3D arrays of NVM cells.

For the "mold stack" deposition of blanket alternating layers, it is vital for the blanket PVD to be defect-free since any defects are mirrored and magnified in upper-layers. All layers must also be stress-free since the stress in each deposited layer accumulates as strain in the underlying silicon wafer, and with over 32 layers the additive strain can easily warp wafers so much that lithographic overlay mismatch induces significant yield loss. Controlled-stress backside thin-film depositions can also be used to balance the stress of front-side films.

"The difficult etch of the hole, the materials are different so the challenges is different," commented Singh about the different types of 3D-NAND now being manufactured by leading fabs. "During this conference, one of our customer presented that they do not see the hole diameters shrinking, so at this point it appears to us that shrinking hole diameters will not happen until after the stacking in z-dimension reaches some limit."

Tri-Layer Resist (TLR) stacks for the hole patterning allow for the amorphous carbon hardmask material to be tuned

Semiconductors



for maximum etch resistance without having to compromise the resolution of the photo-active layer needed for patterning. Carbon mask is over 3 microns thick and carbonetching is usually responsive to

temperature, so Lam's latest wafer-chuck for etching features >100 temperature control zones.

The Figure shows a simplified cross-sectional schematic of how the unique "staircase" wordline contacts are cost-effectively manufactured. The established process of record (POR) for forming the "stairs" uses a single mask exposure of thick KrF photoresist—at 248nm wavelength—to etch 8 sets of stairs controlled by a precise resist trim. The trimming step controls the location of the steps such that they align with the contact mask, and so must be tightly controlled to minimize any misalignment yield loss.



FIGURE 1. A) Simplified cross-sectional schematic of the staircase etch for 3D-NAND contacts using thick photoresist, B) which allows for controlled resist trimming to expose the next "stair" such that C) successive trimming creates 8-16 steps from a single initial photomask exposure.

Lam is working on ways to tighten the trimming etch uniformity such that 16 sets of stairs can be repeatably etched from a single KrF mask exposure. Halving the relative rate of vertical etch to lateral etch of the KrF resist allows for the same resist thickness to be used for double the number of etches, saving lithography cost. "We see an amazing future ahead because we are just at the beginning of this technology," commented Singh. \triangleleft

Managing particle flows in process exhaust for safety and profitability

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Solid particles in the abatement exhaust must be properly managed, and in some cases, substantially reduced from the gas stream before it is released into the environment.

any semiconductor manufacturing processes create solid particles in the process exhaust. Like other exhaust contaminants, these must be properly managed, and in many cases, removed from the stream before it is released into the environment. The permitted release levels vary for particles of different sizes and compositions, depending on their toxicity or potential to damage the environment. Regulations governing particle releases are evolving rapidly. However, the management of particulate flows in process exhaust is also important due to its potential impact on the process itself. Left unmanaged, particulate accumulations can result in shut downs for unplanned maintenance, excessive and premature wear and costly repairs, all of which directly affect the profitability of the manufacturing operation.

Solids may be formed in the exhaust stream of a semiconductor manufacturing process from a number of sources. One important source, though not the focus of this discussion, is the condensation of process gases in vacuum pump exhausts. If not controlled with a thermal management system (e.g. Smart TMS, Edwards) that maintains the pipe surfaces at a sufficiently high temperature, this condensation can quickly accumulate and force a halt to the

manufacturing process. This article will discuss issues further downstream in the abatement process, where toxic volatile compounds are converted to more benign forms, some of which form solid particles that must then be removed from the exhaust gases. Many of these solids are oxides formed when gases, such as tungsten hexafluoride, silane, organo- and halo- silanes and others, are exposed to heat, air, and water. The particles are typically amorphous, i.e. non-crystalline. Many abatement processes use combustion to supply the heat needed to decompose toxic compounds and chemically convert them to a more harmless form. The particles thus formed have varying sizes and may be hydrophilic (formed from halosilanes), hydrophobic (formed from organsilanes) or mixed (mixed chlorides or silicon, aluminum and boron, for example), depending on the species combusted and the nature of the combustion process. Particle sizes can range from tens of nanometers to tens of microns. As shown in **FIGURE 1**, the size of the particles depends on, among other factors, the length of the combustion flame. Longer flames maintain the components at high temperature for a longer periods and result in the formation of larger particles.

The behavior of particles once released into the



FIGURE 1. A longer flame maintains the combusting components at higher temperature for a longer time and results in the formation of larger particles.

environment varies depending on their sizes. Coarse particles, with diameters ranging from 2.5 μ m to 10 μ m, result largely from processes such as erosion, agriculture, or mining and include crustal dust, pollens, fungal spores,

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biological debris and sea salt. Because of their large size, these particles persist in the atmosphere for only a few hours or days. Fine particles, which range from 2.5μ m to 0.1μ m and include the particles of concern in semiconductor manufacturing exhaust, may be the direct result of a combustion processes or may also be formed by photochemical reactions between volatile organic compounds (VOC) and oxides in the presence of sunlight. Fine particles can stay suspended in ambient air for days to weeks. Ultrafine particles, less than 0.1μ m, are generated by high temperature combustion or formed from the nucleation of atmospheric gases. Ultrafine particles are quickly removed from the atmosphere (minutes to hours) via diffusion to surfaces or coagulation, adsorption and condensing into fine particles.

Regulatory environment

Regulations governing the release of particles into the atmosphere are developing quickly worldwide as scientists expand their knowledge of the particles' impacts on health and the environment. In addition to regulations governing emissions by particle size, there are specific regulations regarding especially harmful species, such as heavy metals, carcinogens and toxics. For example, the presence of an adsorbed species, like hydrofluoric acid (HF), on oxide particles increases the toxicity of the parent material.

In 2013 the United States Environmental Protection Agency specified an average daily limit of $150\mu g/m^3$ for coarse particles and $35\mu g/m^3$ for fine particles, and an average annual limit of $12\mu g/m^3$ for fine particles (down from $15\mu g/m^3$ in 2006). China, as of 2012, imposed limits based on both particle size and type, with permitted daily levels for coarse particles of $50\mu g/m^3$ and $150\mu g/m^3$ for type I and type II, respectively and $35\mu g/m^3$ and $75\mu g/m^3$, respectively for fine particles. China also limits annual averages for both sizes and types. The European Commission, the World Health Organization and the Australian National Environmental Council, among others, all specify their own limits. It is clearly incumbent on manufacturers to know and satisfy their local regulations. [1]

Health considerations

The health of employees in manufacturing facilities and people living near manufacturing operations is clearly a high priority for our industry. Epidemiological studies have provided plausible evidence that exposure to particulate material (PM) can impact health in a number of ways, including pulmonary and systemic inflammation, oxidative stress response, protein modification, stimulation of the autonomic nervous system, exaggerated allergic reactions, pro-coagulation activity, and suppression of immune response in the lungs.

Some studies have provided good news as well, specifically, that the amorphous silica particles produced during the abatement of gases used in semiconductor manufacturing have much less impact on lung function than the crystalline silica particles more often encountered in mining and building industries. These studies looked specifically at the effects of pure silica particles, an important caveat. Silica and other dusts that may have acids, such as HF, adsorbed on the particle surface constitute substantially greater health risks than the simple oxide. Other particulate oxides also represent serious health challenges. These include oxides of antimony, arsenic, barium, chromium, cobalt, nickel, phosphorus, tellurium and selenium.

Abatement performance

Just as condensed material deposited in the vacuum lines can shut down the production process, the accumulation of combustion-generated particulates can degrade the performance of the whole facility. In a typical pointof-use (POU) abatement system, after combustion the exhaust gases pass through a series of operations designed to remove particulates and other by-products. In the example shown in **FIGURE 2** these include a water weir, quench tanks, a packed-bed scrubber and an atomized spray. Atomizing spray systems, in particular, have been shown to improve solids removal performance from 50 to 75 percent. Blockages can occur at the damper, in duct spurs leading from the abatement to the main duct, in



FIGURE 2. The accumulation of combustion generated particulates can degrade abatement system performance.

the main duct, before or within the scrubber. In addition to blockages, failure to remove particulate at the primary abatement unit can also lead to environmental discharges and visible plumes at stacks. Any blockage will result in a process shutdown for system maintenance, lasting from a few hours to an entire day.

Mitigation options

A number of approaches exist for removing particulates downstream of the abatement system. One solution does not fit all and it is important to pick the one that best addresses the specific challenges. **FIGURE 3** shows performance characteristics for various technologies. For example, highly toxic particles may require much higher removal rates than less harmful particles.



	Description	Powder	Non-volatile	powder dep
LOC#	Description	problem	Physical	Thermal
1	Bypass valves, inist pipes	Too much	1	
2	Orificies	Too much	1	
1	Quadiants, inject ports	Too much	1	
۴.	Nuzzlen	Too much	1	
5	Underside of head (ceramic, t/c)	Too much		2
6	Porous ceramic liner	Too much		Y
7	Weir-liner interlace	Too much	ĺ.	*
8	Quench sprays and tank	Not enough		1
9	Scrubbing tower	Not enough		
10	Exhaust damper	Too much	1	
11	Outlet duct	Too much	1	

FIGURE 3. Performance characteristics for various particle removal technologies downstream of the abatement system. Courtesy: Waste-to-Energy Research and Technology Council (greyed out area not relevant to solids).

Edwards' standard solution (**FIGURE 4**) for POU removal of fine particles is a wet electrostatic precipitator (WESP). A WESP uses electrostatic forces to remove particles. It requires power, water and pneumatics and can remove up to 95 percent of silica particles at flow rates of $1m^3/$ min, 85% at $2m^3/$ min. WESP technology can be scaled to handle an entire facility. In one example, Edwards partnered in the installation of a large scale dual WESP integrated with a packed-bed wet scrubber and designed it to meet the specific challenges of arsenic abatement. The system ultimately demonstrated a 99 percent removal rate to meet the stringent requirements of the Chinese government for this highly toxic substance.

Alternative technologies that may be appropriate, but have not been evaluated for use in the management of waste gases from semiconductor manufacturing, are the Rotoclone family (from AAF International). POU units handle flow rates of $30m^3/min$, removing >97 percent of 1µm particles and >99.8 percent of 10µm particles. Duct-based Rotoclones with flow rates up to $1250m^3/min$ remove as much as 86 percent of 1µm particles and 99 percent of 10µm particles. Rotoclones require power, water, pneumatics and a drain.

More conventionally, a Venturi scrubber can be configured for various flow and removal rates. As a rule,

smaller units controlling a low concentration waste stream will be much more expensive per unit of volumetric flow than larger units cleaning high pollutant-load flows. Venturi scrubbers can handle mists and flammable or explosive dusts. They have relatively low maintenance requirements, are simple in design and easy to install. Their collection efficiency can be varied. They can cool hot gases and neutralize corrosive gases. They are susceptible to corrosion and must be protected from freezing. Treated gases may require reheating to avoid a visible water plume. The collected particulate material

may be contaminated and not recyclable, requiring expensive disposal of the waste sludge.

Filtration is another alternative for particle removal. It is normally restricted to the management of dry dusts at flow rates of 5 to 250m³/min. Removal rates higher than 99.9 percent are achievable. We have seen a limited number of large filter installations for the removal of hydrophobic silica solids at relative humidities as high as 80 percent. It is not clear how the presence of hydrophilic powder might impact the performance of these facilities.

In cases of highly toxic particles, high efficiency air particle (HEPA) filters can provide very high removal rates, higher than 99.999 percent. However, HEPA filters are appropriate only for very low contaminant concen-



FIGURE 4. POU WESP uses electrostatic forces to remove particulates from the exhaust stream. It can remove up to 95 percent of silica particles at a flow rate of 1m³/min.

trations. Edwards has been partnering with third-party suppliers regarding HEPA filtration for highly toxic dusts such as those generated during arsine management. These solutions are often used for highly toxic materials so they are often designed with bag-in-bag-out capability to eliminate potential exposure of maintenance personnel to the removed contaminants. Typically, these critical installations are also designed as dual systems with auto turnover to allow continuous operation of one system while the redundant system is serviced. HEPA technology can scale from POU to full facility.

Conclusion

All of these technologies are available now, but not all have been demonstrated in semiconductor manufacturing. Semiconductor manufacturers have long used POU WESPs and Venturi scrubbers and are very familiar with HEPA filtration systems, but primarily for particulate removal for air conditioning. Conventional filters are in operation on flat panel display exhausts (mainly on burner only dry abated CVD processes). Some of the technologies we have described, however, have not been proven in semiconductor applications, but are well developed and widely accepted in other industries. Rotoclone systems, for instance, are UL and CE certified, but have not been SEMI qualified. As semiconductor manufacturing processes continue to evolve, it will behove manufacturers to stay current on available technologies and consider alternatives as performance and cost requirements dictate.

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van der Pauw and Hall voltage measurements with a parameter analyzer

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van der Pauw measurements with a parameter analyzer are examined followed by a look at Hall effects measurements.

emiconductor material research and device testing often involves determining the resistivity and Hall mobility of a sample. The resistivity of a particular semiconductor material primarily depends on the bulk doping used. In a device, the resistivity can affect the capacitance, the series resistance, and the threshold voltage, so it's important to perform this measurement carefully and accurately.

The resistivity of the semiconductor material is often determined using a four-point probe or Kelvin technique where two of the probes are used to source current and the other two probes are used to measure voltage. Using four probes eliminates measurement errors due to probe resistance, spreading resistance under each probe, and contact resistance between each metal probe and the semiconductor material. Because a high impedance voltmeter draws little current, the voltage drops are very small.

One useful Kelvin technique for determining the resistivity of a semiconductor material is the van der Pauw (vdp) method using a parameter analyzer with high input impedance and accurate low current sourcing. This article first looks at van der Pauw measurements with a parameter analyzer followed by a look at Hall effects measurements.

van der Pauw resistivity measurements

The van der Pauw method involves applying a current and measuring voltage using four small contacts on the circumference of a flat, arbitrarily shaped sample of uniform thickness. This method is particularly useful for



FIGURE 1. van der Pauw resistivity conventions.

measuring very small samples because geometric spacing of the contacts is unimportant, meaning that effects due to a sample's size are irrelevant.

Using this method, the resistivity is derived from a total of eight measurements that are made around the periphery of the sample using the configurations shown in **FIGURE 1.**

Once all the voltage measurements are taken, two values of resistivity, ρA and ρB , are derived as follows:

$$\begin{split} \rho_A &= \frac{\pi}{\ln 2} \ f_A t_{_B} \ \frac{(V_1 - V_2 + V_3 - V_4)}{4I} \\ \rho_B &= \frac{\pi}{\ln 2} \ f_B t_{_B} \ \frac{(V_5 - V_6 + V_7 - V_8)}{4I} \end{split}$$

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where: ρA and ρB are volume resistivities in ohm-cm

t_s is the sample thickness in cm

 $V_1 - V_8$ represents the voltages measured by the voltmeter

I is the current through the sample in amperes

 f_A and f_B are geometrical factors based on sample symmetry. They are related to the two resistance ratios Q_A and Q_B as shown in the following equations ($f_A = f_B = 1$ for perfect symmetry).

 $\mathbf{Q}_{\!_{A}}$ and $\mathbf{Q}_{\!_{B}}$ are calculated using the measured voltages as follows:

$$Q_{A} = \frac{V_{1} - V_{2}}{V_{3} - V_{4}}$$
$$Q_{B} = \frac{V_{5} - V_{6}}{V_{7} - V_{8}}$$

Also, Q and f are related as follows:

$$\frac{Q-1}{Q+1} = \frac{f}{0.693} \operatorname{arc \, cosh}\left(\frac{e^{0.693/f}}{2}\right)$$

A plot of this function is shown in **FIGURE 2.** The value of f can be found from this plot once Q has been calculated.

Once $\rho_{_A}$ and $\rho_{_B}$ are known, the average resistivity ($\rho_{_{AVG}})$ can be determined as follows:

$$\rho_{AVG} = \frac{\rho_A + \rho_B}{2}$$

The electrical measurements for determining van der Pauw resistivity require a current source and a voltmeter. To automate measurements, it's possible to use a programmable switch to switch the current source and the voltmeter to all sides of the sample. However, a parameter analyzer offers greater efficiency.

A parameter analyzer with four source measure units (SMU) and four preamps (for high resistance measurements) is well-suited for performing van der Pauw resistivity measurements, and enables measurements of resistances greater than 1012Ω . A key advantage is that each SMU instrument can be configured as a current source



FIGURE 2. Plot of f vs. Q.

or as a voltmeter with no external switching required. This eliminates leakage and offsets errors caused by mechanical switches as well as the need for additional instruments and programming.

For high resistance materials, a current source that can output very small current with a high output impedance is necessary. A differential electrometer with high input impedance is required to minimize loading effects on the sample.

Each terminal of the sample is connected to one SMU instrument, so a parameter analyzer with four SMU instruments is required. A diagram of how the four SMUs are configured for each of the tests is shown in **FIGURE 3.** For each test, three of the SMU instruments are configured as a current bias and a voltmeter. One of the SMUs applies the test current and the other two SMUs are used as high impedance voltmeters with a test current of zero amps on a low current range (typically 1nA range). The fourth SMU instrument is set to common. The voltage difference is calculated between the two SMU instruments set up as high impedance voltmeters. This measurement setup is duplicated around the sample, with each of the four SMU instruments changing functions in each of the four tests. The test current and voltage differences between the terminals from the four tests are used to calculate resistivity.

For high resistance samples, it's necessary to determine the settling time of the measurement. This is done by sourcing current into two terminals of the sample and



FIGURE 3. SMU Instrument Configurations for van der Pauw Measurements.

measuring the voltage difference between the other two terminals. The settling time can be determined by graphing the voltage difference versus the time of the measurement. A timing graph of a very high resistance material is shown in **FIGURE 4**. Note that settling time needs to be determined every time for different materials; however, it's not necessary for low resistance materials since they have a short settling time.



FIGURE 4. Voltage vs. time graph of a very high resistance sample.

Hall voltage measurements

Hall effect measurements are important to semiconductor material characterization because from the Hall voltage, the conductivity type, carrier density, and mobility can be derived. With an applied magnetic field, the Hall voltage can be measured using the configurations shown in **FIGURE 5.**

With a positive magnetic field, B, current is applied between terminals 1 and 3, and the voltage drop (V_{2-4+}) is measured between terminals 2 and 4. When the current is reversed, the voltage drop (V_{4-2+}) is measured. Next, current is applied between terminals 2 and 4, and



the voltage drop $(V_{_{1-3+}})$ between terminals 1 and 3 is measured. Then the current is reversed and the voltage $(V_{_{3-1+}})$ is measured again.

Then the magnetic field, B, is reversed and the procedure is repeated again, measuring the four voltages: (V_{2-4-}) , (V_{4-2-}) , (V_{1-3-}) , and (V_{3-1-}) .

From the eight Hall voltage measurements, the average Hall coefficient can be calculated as follows:

$$\begin{split} \mathsf{R}_{\mathsf{HC}} &= \ \frac{\mathsf{t}_{\mathsf{g}} \left(\mathsf{V}_{\mathsf{4-2+}} - \mathsf{V}_{\mathsf{2-4+}} + \mathsf{V}_{\mathsf{2-4-}} - \mathsf{V}_{\mathsf{4-2-}}\right)}{\mathsf{4BI}} \\ \mathsf{R}_{\mathsf{HD}} &= \ \frac{\mathsf{t}_{\mathsf{g}} \left(\mathsf{V}_{\mathsf{3-1+}} - \mathsf{V}_{\mathsf{1-3+}} + \mathsf{V}_{\mathsf{1-3-}} - \mathsf{V}_{\mathsf{3-1-}}\right)}{\mathsf{4BI}} \end{split}$$

where: R_{HC} and R_{HD} are Hall coefficients in cm³/C

 t_s is the sample thickness in cm

V represents the voltages measured by the voltmeter

I is the current through the sample in amperes

B is the magnetic flux in Vs/cm² ($1 \text{ Vs/cm}^2 = 10^8 \text{ gauss}$)

Once $R_{_{\rm HC}}$ and $R_{_{\rm HD}}$ have been calculated, the average Hall coefficient ($R_{_{\rm HAVG}}$) can be determined as follows:

$$R_{HAVG} = \frac{R_{HC} + R_{HD}}{2}$$

From the resistivity (pAVG) and the Hall coefficient ($R_{_{\rm HAVG}}$), the mobility (µH) can be calculated:



For successful resistivity measurements, potential sources of errors need to be considered. Here are the errors sources you are most likely to encounter.

Electrostatic Interference -- Electrostatic interference occurs when an electrically charged object is brought near an uncharged object. Usually, the effects of the interference are not noticeable because the charge dissipates rapidly at low resistance levels. However, high resistance materials do not allow the charge to decay quickly and unstable measurements may result. The erroneous readings may be due to either DC or AC electrostatic fields.

To minimize the effects of these fields, an electrostatic shield can be built to enclose the sensitive circuitry. The shield should be made from a conductive material and connected to the low impedance (FORCE LO) terminal of the test instrument. The cabling in the circuit must also be shielded.

Leakage Current -- For high resistance samples, leakage current may degrade measurements. The leakage current is due to the insulation resistance of the cables, probes, and test fixturing. Leakage current may be minimized by using good quality insulators, by reducing humidity, and by using guarding.

A guard is a conductor connected to a low impedance point in the circuit that is nearly at the same potential as the high impedance lead being guarded. Using triax cabling and fixturing will ensure that the high impedance terminal of the sample is guarded. The guard connection will also reduce measurement time since the cable capacitance will no longer affect the time constant of the measurement.

Light -- Currents generated by photoconductive effects can degrade measurements, especially on high resistance samples. To prevent this, the sample should be placed in a dark chamber.

Temperature --Thermoelectric voltages may also affect measurement accuracy. Temperature gradients may result if the sample temperature is not uniform. Thermoelectric voltages may also be generated from sample heating caused by the source current. Heating from the source current will more likely affect low resistance samples, because a higher test current is needed to make the voltage measurements easier. Temperature fluctuations in the laboratory environment may also affect measurements. Because semiconductors have a relatively large temperature coefficient, temperature variations in the laboratory may need to be compensated for by using correction factors.

Carrier Injection -- To prevent minority/majority carrier injection from influencing resistivity measurements, the voltage difference between the two voltage sensing terminals should be kept at less than 100mV, ideally 25mV, since the thermal voltage, kt/q, is approximately 26mV. The test current should be kept as low as possible without affecting the measurement precision.

Conclusion

The van der Pauw technique in conjunction with a parameter analyzer is a proven method for determining the resistivity of very small samples because geometric spacing of the contacts is unimportant. Hall effect measurements are important to semiconductor material characterization for determining conductivity type, carrier density, and mobility. Some parameter analyzers may include built-in configurable tests that include the necessary calculations.

For successful measurements, it's important to consider potential sources of error including electronics interference, leakage current and environmental factor such as light and temperature. Resistivity can impact the characteristics of a device, serving as reminder of the importance of making accurate and repeatable measurements. \blacklozenge **BUSINESS**

What is your China strategy?

DAVE LAMMERS, Contributing Editor

China has renewed its investments in displays, packaging, and both 200mm and 300mm front-end fab capacity.

quipment vendors have a lot on their plates now, with memory customers pushing 3D NAND, foundries advancing to the 7 nm node, and 200mm fabs clamoring to come up with hard-to-find tools.

China, which has renewed its investments in displays, packaging, and both 200mm and 300mm front-end fab capacity, is another challenge.

"All the managers in my company are scrambling to adjust their budgets so they can support China. I can tell you people are booking lots of flights to Shanghai," said one engineer at a major equipment supplier.

Bill McClean, president of IC Insights (Scottsdale, AZ), said China is fast becoming a center for 3D NAND production, as several companies expand production in China. Intel is converting its Dalian, China fab partly to 3D NAND, and Toshiba might very well make a deal in China to build a 3D NAND fab there, he said.

"China could be the 3D NAND capital of the world," McClean said at The ConFab conference in Las Vegas. While the U.S. government limits exports of leading-edge technologies on national security concerns, 3D NAND relies more on overlay and etch techniques at relaxed (40nm) design rules, he noted.

"Since the 3D NAND makers are not pushing feature sizes, it doesn't raise red flags like if Chinese companies wanted FinFET technology. That is when the alarms go off," McClean said.

However, McClean said the 3D NAND market is not immune to the oversupply issues that now face the DRAM makers. "I've seen this rodeo before," McClean said.

China's domestic IC market is slightly more than \$100 billion, McClean said, while chip production in China was about \$13 billion last year, representing just under 5 percent of worldwide production (**FIGURE 1**).



China IC Market vs. China IC Production Trends

FIGURE 1. China's domestic IC market is slightly more than \$100 billion, while chip production in China was about \$13 billion last year. Source: IC Insights.

The difference between consumption and domestic production, referred to as the delta, is made up by imports. "This 13 percent (from domestic suppliers) drives the Chinese government crazy. Yes, they will close that gap a little bit, but not to the extent that they think," McClean told The ConFab audience in mid-June.

Robert Maire, who consulted for SMIC on its initial public offering in the United States, spoke at length about China at the SEMI Advanced Semiconductor Manufacturing Conference (ASMC) in Saratoga Springs, N.Y. Amid the mergers and acquisition frenzy of last year, China managed to pull off the acquisitions of CMOS image sensor vendor Omnivision, memory maker ISSI, the RF business of NXP, Pericom Semiconductor, and Mattson Technology. (McClean said he believes that if the Omnivision acquisition were attempted in today's more China-wary environment that Washington would block the deal).

Maire, principal at Semiconductor Advisors (New York), said China is far behind in its domestic semiconductor production equipment business. "If China has 14nm production capacity, but buys all of its equipment from abroad, it doesn't really help them that much. China is getting started in equipment, but it has a lot of catching up to do."

Scott Foster, a partner in market intelligence firm TAP Japan (Tokyo), said China must have an international scope in the equipment sector if it hopes to compete with the likes of Applied, Lam, and other well-established vendors. A few of Japan's equipment suppliers are succeeding while operating in relatively narrow niches, but overall, competing globally is a challenge for mid-sized Japanese equipment companies. "If this is what is happening to Japanese equipment vendors, what chance do Chinese companies have?" Foster said.

Packaging may prove to be key

Skeptics of China's prospects might take a long look at China's success in packaging, an area where China is succeeding, in part by acquisitions of Asia-based companies, notably STATS ChipPAC (Singapore), which was acquired by Jiangsu Changjiang Electronics Technology Co. (JCET) last year. Separately, SMIC and JCET formed a joint venture to focus on chip scale packaging, wafer bumping, and fan-out wafer level packaging. The packaging joint venture is located 90 minutes from Shanghai, said Sonny Hui, senior vice president of worldwide marketing at SMIC.

Jim Walker, the packaging analyst at market research firm Gartner, said China-based packaging is now valued at nearly half (43 percent) of all worldwide packaging value by IDMs and OSATs. While the packaging industry overall is dealing with price pressures, the advent of wafer level packaging, and other forms of multi-chip integration, bodes well for the higher end of the back-end industry.

"As the semiconductor industry matures and Moore's Law scaling slows, multi-chip integration via packaging is providing system vendors with a faster time-to-market, and a lower-cost means, of solving system-level challenges," Walker said.

Packaging multiple chips in a module is likely to play a key role in the Internet of Things (IoT) markets, Walker said. Automotive, medical, home, and consumer solutions are all "heavily reliant on packaging," he said.

Sam Wang, a Gartner analyst who focuses on foundries, pointed out at Semicon West that China's semiconductor industry faces continued challenges

Kateeva turns to China funds

China is often lumped together with other Asian nations as a country that has a government-led, me-too, follower mentality. But increasingly, China is either proving innovative itself, or able to quickly adopt innovations from the West.



Conor Madigan, co-founder of Kateeva.

At the Innovation Forum at Semicon West, Conor Madigan, co-founder of ink jet printer startup Kateeva (Newark, Calif.) spoke about the readiness of Chinese venture capital funds to step in where Silicon Valley-based VCs were overly hesitant. China proved a more receptive place to raise money than the United States, though the early establishment of the M.I.T. spinout did come from U.S. based sources.

After its initial development effort, Kateeva figured it needed more than \$100 million to

accomplish its goals. After making the rounds to raise funds in the United States without success, Kateeva turned to China, where five different funds eventually became investors.

Asked why Chinese investors were willing to back Kateeva when funds in the United States and other Asian countries were reluctant, Madigan pointed to a confluence of factors.

The Chinese government had identified OLED displays as a focus of its Five Year Plan. The follow-on economic plan further identified inkjet technology as a critical technology. Investors in China favor companies which can provide the equipment for products, such as OLEDs, which have the government's blessing and financial support. That government support reduced the investment risks in ways that are not readily seen in Japan or the United States, he said.

Madigan had studied OLEDs as an undergraduate at Princeton University, and then studied under an M.I.T. professor who had developed ink jet technology for large formats.

Though an early goal was to use large-format inkjet to deposit the RGB materials in OLEDs, the Kateeva team learned that its YieldJet system could be adapted to solve a more urgent problem: thin film encapsulation (TFE). It "pivoted" on the advice of an early customer, which fortunately already had developed the "ink" which under UV light would form a uniform encapsulation layer for the large OLED substrates required for TVs and other large display applications.

Two display companies in China identified Kateeva as a strategic partner, which allowed Kateeva to raise money from private Chinese VC funds, rather than taking money from regional government funds which might have asked Kateeva to locate its manufacturing operations in their local area.

Madigan also pointed to the tendency of U.S.-based venture capital funds to favor software companies over manufacturing-focused opportunities. As VCs make money in software-related startups, the funds gradually have more partners and investors which favor software because that is what they are familiar with.

VC fund managers with backgrounds in software "want to invest in the space that they understand. In the United States, that often means software, because you pick companies in the space that you understand."

in a hotly contested foundry market. Few China-based foundries have enjoyed the strong growth that SMIC has demonstrated, he said. (SMIC has been "running at very high utilizations, and we are working very hard to solve the problem," said SMIC's Hui.)

While SMIC has enjoyed double-digit growth for several years, the five second-tier Chinese foundries – — Shanghai Huahong Grace, CSMC, HuaLi, XMC, and ASMC — saw declining revenues year-over-year in 2015. Overall, Chinabased foundries accounted for just 7.8 percent of total worldwide foundry capacity last year, and the overall growth rate by Chinese foundries "is way below the expectations of the Chinese government," Wang said.

China-based companies are focusing partly on MEMS and other devices made on 200mm wafers, including analog, sensors, and power. SMIC's Hui said "most of our customers don't see much benefit to migrate to 12-inch. 200mm still has a lot of potential; just consider the hundreds of products still made on 180nm technology, which was developed 20 years ago. Many customers still see that as a sweet spot."

Foster, who has three decades of tech-watching experience from his base in Tokyo, said the 200mm wafer fabs being built in China will make products that "do not need the gigantic scale" required of Intel, TSMC, Samsung and Toshiba. **FIGURE 2**, courtesy of SEMI, shows the seventeen 200mm wafer fabs/lines that are expected begin operation in 2015 to 2019. Six of the seventeen will be in China.

Starting					
Americas	1		1		1
China			4	2	
Europe & Mideast	1	1	1		
Japan	1	1			
Korea					
SE Asia		1		1	
Taiwan		1			
Scarce: 200mm Fab 0	autoria report, W	ionici Palo Porec	ant (performinant)	y July 2016, 5E	Mộ

FIGURE 2. Of the seventeen 200mm wafer fabs/lines that are expected begin operation in 2015 to 2019, six will be in China. Source: SEMI

"After decades of trying, China has found a market-based strategy: building scale and experience from the bottom up. In the long run, this is likely to be far more effective than going out to buy foreign companies," Foster said.

Display is another area China is counting on. In an Aug. 18 conference call following a strong quarter, Applied Materials chief financial officer Bob Halliday told analysts: "In display, we recorded record orders of \$803 million with more than half coming from projects in China."

The Applied CFO also said, "Just listening to the Chinese government, they're in this for a long-term and their interest in investing in the semiconductor industry is probably only going to increase." \diamond

Reducing ESD in semiconductor fluoropolymer fluid handling systems while maintaining chemical purity

MARK CAULFIELD, JOHN LEYS, JIM LINDER and BRETT REICHOW, Entegris, Billerica, MA

Fluoropolymer Electrostatic Discharge (ESD) tubing reduces electrostatic charge to levels below the ignition energy of flammable semiconductor chemicals and maintains chemical purity, ensuring safety and improving process yields.

emiconductor processes, such as photolithography and wet etch and clean, have become more metal sensitive at advanced process nodes. As a result, extracted metals from chemical delivery systems can cause critical wafer defects that negatively impact process yields. To counter this negative yield impact, fabs have converted many of their stainless steel fluid handling systems that had been traditionally selected for use with flammable solvents to fluoropolymer systems. The change to fluoropolymers resulted in reduced extracted metals in the process chemicals.

However, the increased use of fluoropolymer systems creates new concerns with ESD in components such as PFA tubing. Solvents used in the semiconductor industry have low-conductivity, which enables them to generate and hold electrical charge. When these solvents are transported in fluoropolymer systems there is a significantly greater risk of static charge generation and discharge due to the nonconductive nature of the fluoropolymer materials and the low conductivity properties of the solvents. ESD events generated in fluoropolymer systems that are transferring flammable solvents can create leak paths through the



FIGURE 1. Example of electrical discharge through the PFA tubing wall (0.062" diameter wall thickness).

tubing and possible ignition of the surrounding, potentially flammable, solvent-rich environment. An example of an ESD-created leak path through PFA tubing is shown in **FIGURE 1**.

Factors influencing static charge accumulation

Low-conductivity fluid flowing in nonconductive tubing can cause charge separation at the fluid-tube wall boundary as shown in **FIGURE 2**. This separation of charge is similar to what happens when two materials move with respect to each other and transfer charge as shown in **FIGURE**







FIGURE 3. Charge transfer caused by movement .1

3. A charge is created as a result of the transfer of electrons and is similar to the charge that develops by walking across a carpet in dry conditions.

Tubing characteristics affecting charge generation

Table 1 lists the tubing characteristics that are factors for charge generation and accumulation. For each characteristic, the effect on the electric field strength is noted. As an example, as the inner diameter of the tube increases there is more surface area for charge generation, resulting in increased charge and electric field strength.

Tube Characteristic	Static Charge Generation or Accumulation
Inside diameter increases	Increases
Conductivity of the tube material increases	Decreases
Tube length increases	Increases
Resistance per unit length of tube increases	Increases
Dielectric constant of the tube wall material increases	Increases
Volume resistivity of the tube wall material increases	Increases
Surface resistivity of the tube wall material increases	Increases

TABLE 1. Tube characteristics affecting the charge that develops on the tube

The overall mechanism of charge generation and accumulation in fluid handling systems is highly complex. A model for this charge generation and accumulation mechanism is described in Walmsley, H. L. (1996).[2] This model describes the factors influencing static charge generation and accumulation as a result of fluid flow in fluid handling systems.

Fluid properties and conditions affecting charge generation

Table 2 lists the fluid characteristics that affect charge gener-
ation and accumulation. National Fire Protection Association
(NFPA®) 77 9.3.3.1 reads, "In grounded systems, the conduc-

Liquid Properties	Static Charge Generation or Accumulation
Conductivity increases	Decreases
Flow velocity increases	Increases
Dielectric constant increases	Increases
Relaxation time constant increases	Increases

TABLE 2. Fluid properties affecting the amount of chargegenerated or accumulated

tivity of the liquid phase has the most effect on the accumulation of charge in the liquid or on materials suspended in it." [3]

Table 3 lists some low-conductivity chemistries used in the industry.

Gas or Vapor	Conductivity Pi Siemen/Meter (co (pS/m)
nBA	4300	
PGMEA	3 × 104	
nMP	2 × 10 ⁴	- 1
Water – DI 18 mega-ohm-cm	5.5 × 10 ⁸	
Acetone	6 × 10 ⁿ	2
IPA	6 × 10 ⁶	
Cyclohexanone	10.9 × 10 ⁸	
Methanol	4.4 × 10 ⁷	- 1
Ethyl Lactate	1 × 10 ⁸	
Water - Air Distilled	1 × 10 ⁹	

TABLE 3. Conductivity of fluids commonly used in semiconductor processes

An example of a high-flow velocity ESD event in a non-solvent application

In the process of cleaning a newly installed PFA chemical line, dilute chemistry is introduced into the line followed by a nitrogen purge then ultrapure DI water. Before fully concentrated chemical can be introduced into the bulk delivery line, the water must be removed. To remove the final DI rinse water, high-purity dry nitrogen is forced through the lines at high velocities. The high-purity nitro- gen, along with the water droplets that cling to the inside diameter of the tube, can generate and hold significant static charge. These flow conditions can result in ESD events causing pinholes in tubing and fluid handling components. The same mechanism of charge generation and accumulation may also occur when processing with high-purity steam.

PFA systems for solvent chemical distribution could also go through a DI water flush and nitrogen purge sequence. However, it is far more common to perform only a nitrogen purge, which, when introduced, can cause an ESD event.

Potential effects of ESD on fluoropolymer fluid handling systems

Dielectric strength is the measure of a material's insulating strength. NFPA 77 defines the dielectric strength as "the maximum electrical field the material can withstand without electrical breakdown". [3]

Dielectric strength is usually specified in volts/mm of thickness. As wall thickness and dielectric strength increase



Standard fluoropolymer tubing, such as PFA, is a very good insulator with high dielectric strength. PFA's insulating properties make it difficult to ground and also contribute to charge generation and storage in tubing systems. There have been field instances where the generated charge was able to create a discharge path through the tubing wall and cause a leak. After the electrical discharge creates the first fluid leak path, it is likely that subsequent static generation will discharge through that same leak path at lower charge levels.

A spark from the outside of the tube to ground may ignite a solvent-laden environment

Two conditions that must be present to start a fire or explosion are an electrical discharge of sufficient energy and a flammable or combustible environment. A flammable solvent leak caused by discharge through the tubing wall or a discharge from the out- side of the tube to ground could cause an explosion.

The energy of a spark and its ability to ignite a flammable fluid or gas is directly related to the square of the voltage level of the discharge as shown in Equation 1. [3] As voltage increases, the energy available to cause ignition in a flammable environment increases.

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\mathbf{W} = \frac{1}{2} \mathbf{C} \mathbf{V}^2
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Where:

W = energy (joules)

- C = capacitance (farads)
- V = potential difference (volts)

To assess whether the electrical discharge energy is sufficient to cause ignition, the Minimum Ignition Energy (MIE) value of the fluid or vapor is considered. **Table 4** lists MIE's of commonly used semiconductor fluids

Gas or Vapor	MIE Millijoules (mJ)	
Methanol	0.14	ele .
Acetone	0.19	Less
IPA	0.21	flar

TABLE 4. Mie of fluids commonly used in semiconductorprocesses

ESD tubing: proposed solution for mitigating electrostatic discharge

NFPA 77 lists several strategies for mitigating the amount of charge accumulation in electrically nonconductive pipes as a result of electrically nonconductive fluid flow. [4] Several of these are:

- 1. Reduce flow velocity
- 2. Reduce wall resistivity to less than 10^8 ohm-m
- 3. Increase the breakdown strength of the pipe wall material by:
 - a. Increasing thickness
 - b. Changing material to one with higher breakdown strength
- 4. Increase conductivity of fluids. (Unlike other industries this is rarely a possibility in the semiconductor process industry where any added particles, especially conductive, are not permitted.)
- 5. Incorporating an external grounded conductive layer on the piping



FIGURE 4. Entegris FluoroLine ESD tubing minimizes potential issues related to electrostatic discharge in the fab.

Entegris has chosen strategy #5 and has developed FluoroLine® tubing with static dissipative PFA stripes on the outside of the tubing that can be connected to ground (see **FIGURE 4**). Charge accumulation that develops on the outside of the tube as a result of fluid flow is redirected to external

ground paths (**FIGURE 5**). This approach is consistent with the NFPA 77 observation that, "Carbon black can be added to some plastics or rubbers to increase conductivity." [3] Carbon-filled plastics and rubber particles are sometimes sufficiently conductive to be grounded like metal objects.



FIGURE 5. 1/2" FluoroLine Electrostatic Dissipative tubing.

CONTAMINATION CONTROL



FIGURE 6. Test setup of four-foot and 28-foot tube lengths.

The purpose of having coextruded, PFA carbon stripes only on the outer diameter is to preserve the cleanliness of the tubing's pure PFA inner layer. Stripes were also used so the fluid can be seen inside the tubing.

Test assemblies were made to hold four-foot and 28-foot long samples of tubing that simulate how customers would use this tubing (**FIGURE 6**). The tube ends were attached to PFA fittings, the same fittings customers use, so that charge would not be discharged through the end connections.

To simulate a common flow condition used by customers during the commissioning of their systems, an alternating flow of non-conducting 18 Mohm Deionized (DI) water and Extreme Clean Dry Air (XCDA[®] purge gas) was used. **Table 5** lists the flow ranges of XCDA and DI water along with the corresponding pressures at the tube inlet.

Flow Rate	XCDA Inlet Pressure	XCDA Flow Rate	DI Water Flow Rate
100%	72 psi	200 SCFH	1.2 gal/min
75%	36 psi	150 SCFH	0.9 gal/min
50%	16 psi	100 SCFH	0.6 gal/min
25%	5 psi	50 SCFH	0.3 gal/min
Ar	mbient temperati % i	ure: 20°C-22.4°C RH: 19-25%	C (68°F-72.4°F)
1	DI water resistan	ce: 18.9-17.9 m	ohm

DI water conductivity: 5.91 × 106-5.59 × 106 pS/m

TABLE 5. Pressure and flow conditions

Tube Tested	Material	OD	Wall Thickness	28' Length	4' Length
Entegris FluoroLine ESD tube, EPLAT=04	PFA, ESD PFA stripes	0.25"	0.039"	х	Х
Entegris XKT250-047	PFA	0.25"	0.047"	Х	Х
1∕7" tube	304 stainless steel	0.25"	0.098"		х

TABLE 6. Tube and materials tested for electrostatic discharge



FIGURE 7. Monroe Electronics 257C-1, 20 KV to 20 KV electrostatic field meter testing ESD charge.

The 100% flow rate was the maximum flow through the tube that could be achieved with the test setup. Reduced flow rates were tested to determine the effect of flow rate on the level of charge generated.

A Monroe Electronics 257C-1, 20 KV to -20 KV electrostatic field meter was used to measure the charge level 1 cm from the outside of the tube (**FIGURE 7**). A resistivity meter was used to monitor the resistance of the DI water during the tests.

Note: Clean nitrogen and XCDA, because of their extreme cleanliness, are good insulators and thus possess the ability to create and hold large electrical potential.

Test procedure

- Tube was cut to length and installed in the fixtures with nonconductive PFA polymer fittings at each end. Tube samples, fittings and probe tips were wiped down with IPA after installation.
- DI water resistance was measured and monitored throughout the test.
- The electrostatic voltage field meter was placed with the probe at 1 cm distance from the tube OD.
- Alternating flows of DI water and XCDA were introduced to the tube and the field strength was measured at three different locations along the length of the tube. Each tube was subjected to this flow condition with and without a conductive ground strap connecting the tube to ground. In addition, the flow rate was reduced to 75%, 50% and 25% of the maximum flow rate to determine how the level of charge was affected.

Test conclusions

- 1. Grounding standard PFA tubing does not reduce the field voltage on the outside of the tube that is produced by flowing XCDA and DI water on the inside. Up to 20 KV field voltage was measured with the XCDA/DI water delivery system (Figure 8).
- 2. Grounding ESD PFA tubing and stainless steel does significantly reduce the field voltage on the outside of the tube that is produced by flowing XCDA and DI water flowing on the inside (**FIGURE 8**).
- 3. The field voltage developed along four- and 28-foot tube lengths does not vary significantly for PFA, ESD PFA and stainless steel.
- 4. With reduced flow rates, the maximum absolute field voltage was reduced for both grounded ESD PFA and PFA tubing (**FIGURE 9**).
- 5. No fluid leak paths were generated throughout this testing in either the PFA or ESD PFA tube.
- 6. The capacitance of a four-inch long PFA tube was measured to be 56 pF. Using this capaci- tance value and 20 KV levels of voltage measured by the field meter in this test, the energy of discharge is calculated as 11.2 mJ. This energy level exceeds the MIE of fluids listed in Table 4 and would be expected to cause fumes from these fluids to ignite.

Applying this same equation to grounded ESD tubing where a maximum of 1.5 KV field was measured along with 52 pF capacitance, the discharge energy was calculated at 0.059 mJ and was below the threshold of ignition energy of the fluids listed in Table 4.

Conclusion

As semiconductor processes such as photolithography and wet etch and clean become more metal sensitive at advanced process nodes, fabs are converting to fluoropolymer fluid handling systems. The increased use of fluoropolymer systems creates new concerns with electrostatic discharge (ESD) in components such as PFA tubing. Electrostatic discharge increases the risks of leaks, flammability and potential explosions.

Solvents transported in fluoropolymer systems pose a significantly greater risk of static charge generation and discharge due to the nonconductive nature of the fluoropolymer materials and the frequent low-conductivity properties of the solvents. Understanding the factors that influence static charge generation and

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FIGURE 8. Field voltage on the outside of the tube.



FIGURE 9. Field voltage on the outside of the tube with reduced internal flow rates.

accumulation in a fluoropolymer fluid handling system, Entegris developed an effective solution that is proven to dissipate static charge accumulation on the exterior of the tubing. Entegris' FluoroLine ESD tubing has external static dissipative PFA carbon stripes that redirect charge accumulation from the outside of the tube to external ground paths. This tubing maintains chemical purity, and when properly grounded, minimizes electrostatic discharge events, helping to increase process yields while ensuring safety.

References

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Preview: 2016 IEEE International Electron Devices Meeting

The 62nd annual IEDM will be held in San Francisco December 3 - 7, 2016.

or more than six decades, the annual IEEE International Electron Devices Meeting (IEDM) has been the world's largest and most influential forum for technologists to unveil breakthroughs in transistors and related micro/nanoelectronics devices.

That tradition continues this year with a few new twists, including a supplier exhibition and a later papersubmission deadline (August 10) of a final, four-page paper. Accepted papers will appear in the proceedings without any changes. This streamlined process will ensure that even as the pace of innovation in electronics quickens, IEDM remains the place to learn about the latest and most important developments.

The 62nd annual IEDM will be held in San Francisco December 3 - 7, 2016, beginning with a weekend program of 90-minute tutorials and all-day Short Courses taught by industry leaders and world experts in their respective technical disciplines. These weekend events will precede a technical program of some 220 papers and a rich offering of other events including thought-provoking plenary talks, spirited evening panels, special focus sessions on topics of great interest, IEEE awards and an event for entrepreneurs



FIGURE. The city of San Francisco is just south of the Golden Gate Bridge. Credit: Lewis Sommer, San Francisco Convention and Visitors Bureau

sponsored by IEDM and IEEE Women in Engineering.

"The industry is moving forward at an accelerated pace to match the increasing complexity of today's world, and a later submission deadline enables us to shorten the time between when results are achieved in the lab and when they are presented at the IEDM," said Dr. Martin Giles, IEDM 2016 Publicity Chair, Intel Fellow, and Director of Transistor Technology Variation in Intel's Technology and Manufacturing Group.

Tibor Grasser, IEDM 2016 Exhibits Chair, IEEE Fellow and Head of the Institute for Microelectronics at TU Wien, added, "We have decided to have a supplier exhibition in conjunction with the technical program this year, as an added way to provide attendees with the knowledge and information they need to advance the state-of-the-art."

Here are some of the noteworthy events that will take place at this year's IEDM:

Special Focus Sessions

- Wearable Electronics and Internet of Things (IoT) -Wearable technology offers great promise for communications, fitness tracking, health monitoring, speech therapy, elder care/assisted living and many other applications. This Special Focus Session has been organized to benchmark wearable electronics technologies, to address applications with comprehensive system demonstrations, and to learn industrial perspectives about the gaps, challenges and opportunities for wider uses of wearable and IoT technologies. Papers on flexible/stretchable electronics, MEMs, display devices, sensors, printed electronics, organic devices and 2-D material devices enabling wearables/IoT devices also will be featured.
- **Quantum Computing** As traditional CMOS scaling enters the post-Moore's Law era, quantum computing has emerged as a possible candidate for further device scaling because it exploits the laws of quantum physics and may make much more powerful computers possible. This Special Focus Session will explore relevant semiconductor-related fabrication issues and will brainstorm R&D directions for new



materials, devices, circuits, and manufacturing approaches for the scalable integration of a large number of qubits with CMOS technology, operating at cryogenic temperatures for the realization of quantum computers.

- **System-Level Impact of Power Devices** While there are forums that serve circuit experts for the exchange of ideas and the reporting of breakthroughs, there hasn't been a suitable forum for bringing device and circuit experts together to consider impacts at the system level, even though that would be fruitful due to the interactions of circuits and devices. IEDM aims to serve as the forum for their dialogue, and so this Special Focus Session has been organized. Papers are expected to explore the system-level impact of power devices, and also to describe various types of power devices targeting the full range of power/power conversion applications such as hybrid vehicles, utility and grid control, computing/telecom power supplies, motor drives, and wireless power transfer.
- Ultra-High-Speed Electronics There have been many advances and breakthroughs in ultra-high-speed electronics for communications, security and imaging applications, but technology gaps continue to prevent spectrum above millimeter-wave frequencies from being fully used. This Special Focus Session has been organized to discuss, showcase and benchmark advanced ultra-high speed devices and circuits based on high-electron-mobility transistors (HEMTs), heterojunction bipolar transistors (HBTs) and conventional CMOS devices; high-speed interconnect; antennas for ultra-highspeed systems; ultra-high-frequency oscillators; and to discuss other possible applications.

90-Minute Tutorials – Saturday, Dec. 3

A program of 90-minute tutorial sessions on emerging technologies will be presented by experts in the fields, to bridge the gap between textbook-level knowledge and leading-edge current research. Advance registration is recommended.

- The Struggle to Keep Scaling BEOL, and What We Can Do Next, Dr. Rod Augur, Distinguished Member of the Technical Staff, GlobalFoundries – Looking ahead, it's the interconnect that threatens further cost-effective scaling. The tutorial will cover challenges and trade-offs in backend-of-the-line (BEOL) scaling, and will evaluate emerging devices from a scaled-BEOL viewpoint.
- Electronic Circuits and Architectures for Neuromorphic Computing Platforms, *Prof. Giacomo Indiveri*, *Univ. of Zurich and ETH Zurich* – This tutorial will cover the principles and origins of neuromorphic (i.e., brain-inspired) engineering, examples of neuromorphic circuits, how neural network architectures can be used to build large-scale multi-

core neuromorphic processors, and some specific application areas well-suited for neuromorphic computing technologies.

- Physical Characterization of Advanced Devices, *Prof. Robert Wallace, Univ. Texas at Dallas* – This tutorial will cover the hardware, physics, and chemistry that enable modern physical characterization of novel electronic materials, and will explore how these techniques can shed light on electronic materials research and development, and on the resultant devices. In addition to introducing examples of novel electronic materials for device applications, example techniques discussed will include high-resolution electron microscopy, scanning tunneling microscopy and spectroscopy, dynamic x-ray photoelectron spectroscopy, and ion mass spectrometry. The detection limits of these techniques and how they relate to device behavior also will be discussed.
- Present and Future of FEOL Reliability—from Dielectric Trap Properties to Reliable Circuit Operation, Dr. Ben Kaczer, Principal Scientist, Imec – This tutorial will introduce the main degradation mechanisms occurring in present-day CMOS. The reliability of novel devices (SiGe, IIIV, gate-all-around nanowires, junctionless FETs, tunnel FETs), of deeply-scaled devices, and of circuits (e.g., "reliability-aware" designs) will be covered in detail. The tutorial will give attendees an overview and background in this area sufficient to allow them to follow and participate in any discussion on reliability in general, and on front-endof-the-line (FEOL) reliability in particular.
- Spinelectronics: From Basic Phenomena to Magnetoresistive Memory (MRAM) Applications, Dr. Bernard Dieny, Chief Scientist, Spintec CEA -- This tutorial will cover spintronics phenomena, magnetic tunnel junctions (growth, magnetic and transport properties), field-written MRAM (toggle and thermally assisted MRAM), STT-MRAM (principle and status of development), 3-terminal MRAM and innovative architectures that benefit from these highendurance non-volatile memories.
- Technologies for IoT and Wearable Applications, Including Advances in Cost-Effective and Reliable Embedded Non-Volatile Memories, Dr. Ali Keshavarzi, Vice President of R&D, Cypress Semiconductor -- This tutorial will cover a range of technology opportunities for IoT and wearable applications, including embedded non-volatile memories (eNVM), IPs and integrated solutions based on charge-trap memory technologies such as SONOS for low power (LP) and ultra-low-power (ULP) for advanced technology nodes. Technologies will be described for various integrated IoT, wearable and energy-harvesting systems using programmable systems-on-chips (SoCs) with digital and analog capabilities, along with low-energy Bluetooth radio, WiFi radio, solar cells, sensors, actuators, and power management ICs. Advanced



small form-factor packaging technologies useful for system integration also will be described.

Short Courses – Sunday, Dec. 4

The Short Courses provide the opportunity to learn about important areas and developments, and to benefit from direct contact with world experts. Advance registration is recommended.

1. Technology Options at the 5-Nanometer Node, organized by An Steegen and Dan Mocuta of Imec (Sr. Vice President of Technology Development/Director of Logic Device and Integration, respectively) – This course will describe the complex technological challenges at the 5nm node and explore innovative potential solutions. It begins with an in-depth discussion of patterning strategies being pursued to print critical features. Then, a pair of lectures will provide an overview of current transistor technologies and their relative strengths/ weaknesses in the context of various applications such as mobility, data centers and IoT. Strategies for effective mitigation of performance-limiting parasitic resistance and capacitance will be discussed, and advanced interconnect technologies including postcopper materials options for BEOL and MEOL applications will be addressed. Lastly, metrology challenges for in-line and end-of-line process technologies will be discussed. The intent of the course is to provide a thorough understanding in process technology targets at the 5nm node and their potential solutions. Attendees will have the opportunity to learn about advanced technology options that are being actively pursued in the industry from leading technologists.

The course consists of lectures from six distinguished speakers:

- Nano Patterning Challenges at the 5nm Node, Akihisa Sekiguchi, VP & Deputy GM, SPE Marketing and Process Development Division, Tokyo Electron, Japan
- Novel Channel Materials for High-Performance and Low-Power CMOS, Nadine Collaert, Distinguished Member of the Technical Staff, imec, Belgium
- **Transistor Options & Challenges for 5nm Technology,** Aaron Thean, Professor of Electrical & Computer Engineering, National University of Singapore
- Low Resistance Contacts to Enable 5nm Node Technology: Patterning, Etch, Clean, Metallization

and Device Performance, Reza Arghavani, Managing Director, Lam Research, USA

- Parasitic R and C Mitigation Options for BEOL and MOL in N5 Technology, Theodorus Standaert, Sr. Engineering Mgr., Manager, Process Integration, IBM, USA
- **Metrology Challenges for 5nm Technology,** Ofer Adan, Technologist and Global Product Manager, Member of the Technical Staff, Applied Materials, Israel
- 2. Design/Technology Enablers for Computing Applications, organized by John Chen, Vice President of Technology and Foundry Management, NVIDIA - This course will describe how various design techniques and process technologies can enable computing applications, beginning with the relative advantages and disadvantages of processors such as CPU, GPU and FPGA with regard to today's high data demands. It then will cover how memory becomes a bottleneck, and will discuss various emerging memory technologies to mitigate the problem. Because managing power dissipation has become critical, it also will offer a broad perspective on power efficiency in computing and how interconnect plays a pivotal role in both performance and energy efficiency. Finally, 2.5-D and 3-D advanced packaging technology is discussed for system integration.

The course consists of lectures from five distinguished speakers:

- The Rise of Massively Parallel Processing: Why the Demands of Big Data and Power Efficiency are Changing the Computing Landscape, Liam Madden, Corporate VP, Hardware & Systems Development, Xilinx, USA
- Breaking the Memory Bottleneck in Computing Applications with Emerging Memory Technologies: a Design and Technology Perspective, Gabriel Molas, PhD Engineer, Leti, France
- Power Management with Integrated Power Devices... and how GaN Changes the Story, Alberto Doronzo, Power System/Apps Engineer, Texas Instruments, USA
- Interconnect Challenges for Future Computing, William J. Dally, Chief Scientist and Sr. VP of Research, NVIDIA, and Stanford Professor, USA
- Advanced Packaging Technologies for System Integration, Douglas Yu, Sr. Director, TSMC, Taiwan ◆

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industry forum

Moore's Law did indeed stop at 28nm

As we predicted two and a half years back, the industry is bifurcating, and just a few products pursue scaling to 7nm while the majority of designs stay on 28nm or older nodes.

Our March 2014 blog "Moore's Law has stopped at 28nm!" has recently been reconfirmed. At the time we wrote: "From this point on we will still be able to double the amount of transistors in a single device but not at lower cost. And, for most applications, the cost will actually go up." This reconfirmation can be found in the IBS cost analysis table slide (FIGURE 1), presented at the early Sept FD-SOI event in Shanghai. Even Intel has given up on its "every two years" but still claims it can keep reducing transistor cost. Yet Intel's underwhelming successes as a foundry suggests otherwise. We have discussed it in a blog titled "Intel -- The Litmus Test," and it was essentially repeated by SemiWiki's story "Apple will NEVER use Intel Custom Foundry!"

This discussion seems academic now, as the actual engineering costs of devices in advanced nodes have shown themselves to be too expensive for much of the industry. Consequently, and as predicted, the industry is bifurcating, with a few products pursuing scaling to 7nm while the

Technology	Gates/mm ² (KU)	Gate utilization (%)	Used gatesimm ² (KU)	Parametric yield impact (Δ from D ₆ yield)	Actual used gates/mm ² (KU)	Gates/ wafer (MU)	Wafer cost (\$)	Wafer cost (Δ)	Cost per 100M gate (\$)
Souu	637	85	546	97	532	33,631	1,357.62	+	4.01
65nm	1,109	83	919	96	885	56,330	1,585.71	16.8	2.82
45/40nm	2,139	78	1,677	92	1,538	97,842	1,898.83	19.7	1.94
28nm	4,262	77	3,282	87	2,855	181,658	2,361.84	24.4	1.30
20nm	6,992	65	4,524	73	3,293	209,541	2,981.75	26.2	1.42
16/14nm	10,488	64	6,712	67	4,497	286,140	4,081.22	36.9	1.43
10nm	14,957	60	8,974	62	5,564	354,013	5,126.35	25.6	1.45
7nm	17,085	59	10,080	60	6,048	384,813	5,859.28	14.3	1.52

majority of designs use 28nm or older nodes.

Yes, the 50-year march of Moore's' Law has ended, and the industry is now facing a new reality.

This is good news for innovation, as a diversity of choices helps support new ideas

FIGURE 1. Gate costs continue to rise each generation for FinFETs, IBS predicts.

As reported by EE Times – "Chip Process War Heats Up", and Handel Jones of IBS is quoted as saying "28nm node is likely to be the biggest process of all through 2025." IBS prediction was seconded by a Samsung executive at Semicon West 2016 who showed a foil with the comment "28nm will have the lowest cost per transistor of any node." and new technologies such as 3D NAND, FDSOI, MEMS and others. These technologies will enable new markets and products such as the emerging market of IoT. \blacklozenge



ZVI OR-BACH, President & CEO, MonolithIC 3D Inc.

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