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How to Solve the BEOL RC Delay Problem? P.17

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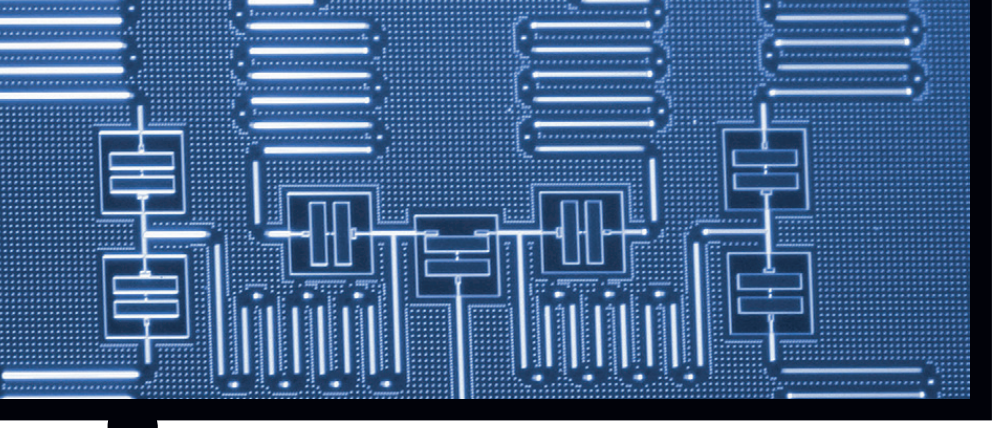

Solid State TECHNOLOGY®

OCTOBER 2017 VOL. 60 NO. 7

IBM scientists successfully used six qubits on this seven-qubit quantum processor to simulate molecules. See related stories on pages 6 and 7.

COVER

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editorial

Enabling the A.I. era

There's a strongly held belief now that the way in which semiconductors will be designed and manufactured in the future will be largely determined by a variety of rapidly growing applications, including artificial intelligence/deep learning, virtual and augmented reality, 5G, automotive, the IoT and many other uses, such as bioelectronics and drones.

The key question for most semiconductor manufacturers is how can they benefit from these trends? One of the goals of a recent panel assembled by Applied Materials for an investor day in New York was to answer that question.

The panel, focused on "enabling the A.I. era," was moderated by Sundeep Bajikar (former Sellside Analyst, ASIC Design Engineer). The panelists were: Christos Georgiopoulos (former Intel VP, professor), Matt Johnson (SVP in Automotive at NXP), Jay Kerley (CIO of Applied Materials), Mukesh Khare (VP of IBM Research) and Praful Krishna (CEO of Coseer). The panel discussion included three debates: the first one was "Data: Use or Discard"; the second was "Cloud versus Edge"; and the third was "Logic versus Memory."

"There's a consensus view that there will be an explosion of data generation across multiple new categories of devices," said Bajikar, noting that the most important one is the self-driving car. NXP's Johnson responded that "when it comes to data generation, automotive is seeing amazing growth." He noted the megatrends in this space: the autonomy, connectivity, the driver experience, and electrification of the vehicle. "These are changing automotive in huge ways. But if you look underneath that, AI is tied to all of these," he said.

He said that estimates of data generation by the hour are somewhere from 25 gigabytes per hour on the low end, up to 250 gigabytes or more per hour on the high end. or even more in some estimates. "It's going to be, by the second, the largest data generator that we've seen ever, and it's really going to have a huge impact on all of us."

Intel's Georgiopoulos agrees that there's an enormous amount of infrastructure that's getting built right now. "That infrastructure is consisting of both the ability to generate the data, but also the ability to process the data both on the edge as well as on the cloud," he said. The good news is that sorting that data may be getting a little easier. "One of the more important things over the last four or five years has been the quality of the data that's getting generated, which diminishes the need for extreme algorithmic development," he said. "The better data we get, the more reasonable the AI neural networks can be and the simpler the AI networks can be for us to extract information that we need and turn the data information into dollars." Check out our website at www.solid-state.com for a full report on the panel.

—Pete Singer, Editor-in-Chief

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Web Exclusives

Comparing XPoint memory architecture with NAND and DRAM products

There has been a great deal of speculation around the composition of Intel's Optane XPoint memory technology. TechInsights set about to find answers.

http://bit.ly/2yjGmWu

A 1,000x improvement in computer systems using current fabs and process

Next week, as part of the IEEE S3S 2017 program, MonolithIC 3D Inc. will present a paper (18.3) titled "A 1,000x Improvement in Computer Systems by Bridging the Processor Memory Gap".

http://bit.ly/2z6qfuP

Robotics and chip industries in Japan

Japan chip industry finds growth opportunities in robotics; explored at SEMICON Japan (December 13-15) in Tokyo.

http://bit.ly/2ia1lSa

New 3D packaging & integration committee

The SEMI International Standards Committee, at their SEMICON West 2017 meeting, approved the transformation of the existing 3D Stacked IC Committee and Assembly & Packaging Committee into a single, unified 3D Packaging and Integration Committee.

http://bit.ly/2gCnBWD

DARPA calls for Monolithic 3D – 3DSoC

Learn all about Monolithic 3D at IEEE S3S.

http://bit.ly/2ymQzn6

n&b news and blogs

Insights from the Leading Edge: iPhone 8 teardown

TechInsights has begun their teardown of the new iPhone 8.

http://bit.ly/2yfyKXl

Reliability for the real (new) world

With electronics moving into virtually every facet of our lives, designers are facing unique challenges as they create (or re-engineer) designs for new high-reliability, environmentally-demanding applications like automotive and medical. (From SemiMD)

http://bit.ly/2wUKXwV

The case for µLED displays

It is true, as Shakespeare one said, that "A rose by any other name would smell as sweet" but ... in our times, it is important to have an unambiguous name that clearly indicates what you are talking about. Unfortunately, this is not the case for micro LED displays (µLED Displays).

http://bit.ly/2yfqtTz

XPoint NVM array process engineering

From first principles of process engineering, we can make educated guesses as to the process flows and challenges in creating this type of non-volatile memory (NVM) integrated circuit (IC). Evolution of device technology over more than fifteen years has resulted in cross-point arrays connecting precise stacks of chalcogenide materials. Intel with "Optane" and Micron with "QuantX" branded ICs can now claim success in commercializing what has always looked good in R&D but was notoriously difficult to make in high-volume manufacturing (HVM).

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EUROPE - **Leti** held a workshop on Oct. 17 to present updates on their progress developing CoolCube high-density 3D sequential, monolithic-integration technology, and their supporting design-and-manufacturing ecosystems.

USA - **GLOBALFOUNDRIES** unveiled AutoPro, a new platform designed to provide automotive customers a broad set of technology solutions and manufacturing services that minimize certification efforts and speed time-to-market.

ASIA – **Toshiba Memory Corp.** will invest approximately 110 billion yen as a second investment in Fab 6 for the installation of additional manufacturing equipment in the Phase-1 clean room.

EUROPE - **EVG** and **SwissLitho** announced plans to develop joint nanoimprint lithography solution for 3D optical structures with single-nanometer accuracy

USA - **Solar-Tectic LLC** received a patent for III-V thin-film tandem high-performance solar cell and LED technology.

ASIA - **ON Semiconductor** agreed to purchase 30 percent incremental share of Fujitsu's 8-inch wafer fab in Aizu-Wakamatsu, Japan.

USA - **COMET Group** announced the opening of Lab One, its customer-centric technology and application center in San Jose, CA.

ASIA - **Soitec** launched an FD-SOI pilot line in Singapore, the first stage in beginning FD-SOI production in Singapore and providing multi-site FD-SOI substrate sourcing to the global semiconductor market.

EUROPE – **Soitec** and **GLOBALFOUNDRIES** enter into long-term supply agreement on FD-SOI wafers.

ASIA - **Samsung Electronics** joined the Semiconductor Research Corporation's research consortium.

IBM pioneers new approach to simulate chemistry with quantum computing

IBM scientists have developed a new approach to simulate molecules on a quantum computer that may one day help revolutionize chemistry and materials science. The scientists successfully used a seven-qubit quantum processor to address the molecular structure problem for beryllium hydride (BeH_2) – the largest molecule simulated on a quantum computer to date. The results demonstrate a path of exploration for near-term quantum systems to enhance our understanding of complex chemical reactions that could lead to practical applications.

The team implemented a novel algorithm that is efficient with respect to the number of quantum operations required for the simulation. Using six qubits of a seven-qubit processor they were able to measure BeH_2's lowest energy state, a key measurement for understanding chemical reactions. While this model of BeH_2 can be simulated on a classical computer, IBM's approach has the potential to scale towards investigating larger molecules that would traditionally be seen to be beyond the scope of classical computational methods, as more powerful quantum systems get built. The results were published today as the cover of the peer-reviewed journal Nature.*

To help showcase how quantum computers are adept to simulating molecules, developers and users of the IBM Q experience are now able to access a quantum chemistry Jupyter Notebook. The open source quantum chemistry Jupyter Notebook (available through the open access QISKit github repo) allows users to explore a method of ground state energy simulation for small molecules such as hydrogen and lithium hydride. Over a year ago, IBM launched the IBM Q experience by placing a robust five-qubit quantum computer on

Continued on page 10

Gartner identifies the top 10 strategic technology trends for 2018

Gartner, Inc. this month highlighted the top strategic technology trends that will impact most organizations in 2018. Analysts presented their findings during Gartner Symposium/ITxpo, which took place October 1-5.

Gartner defines a strategic technology trend as one with substantial disruptive potential that is beginning to break out of an emerging state into broader impact and use, or which are rapidly growing trends with a high degree of volatility reaching tipping points over the next five years.

"Gartner's top 10 strategic technology trends for 2018 tie into the Intelligent Digital Mesh. The intelligent digital mesh is a foundation for future digital business and ecosystems," said David Cearley, vice president and Gartner Fellow. "IT leaders must factor these technology trends into their innovation strategies or risk losing ground to those that do."

The first three strategic technology trends explore how artificial intelligence (AI) and machine learning are seeping into virtually everything and represent a major battleground for technology providers over the next five years. The next four trends focus on blending the digital and physical worlds to create an immersive, digitally enhanced environment. The last three refer to exploiting connections between an expanding set of people and businesses, as well as devices, content and services to deliver digital business outcomes.

The top 10 strategic technology trends for 2018 are:

AI foundation

Creating systems that learn, adapt and potentially act autonomously will be a major battleground for technology vendors through at

Continued on page 12

Intel delivers 17-qubit superconducting chip with advanced packaging to QuTech

Intel announced the delivery of a 17-qubit superconducting test chip for quantum computing to QuTech, Intel's quantum research partner in the Netherlands. The new chip was fabricated by Intel and features a unique design to achieve improved yield and performance.

The delivery of this chip demonstrates the fast progress Intel and QuTech are making in researching and developing a working quantum computing system. It also underscores the importance of material science and semiconductor manufacturing in realizing the promise of quantum computing.

Quantum computing, in essence, is the ultimate in parallel computing, with the potential to tackle problems conventional computers can't handle. For example, quantum computers may simulate nature to advance research in chemistry, materials science and molecular modeling – like helping to create a new catalyst to sequester carbon dioxide, or create a room temperature superconductor or discover new drugs.

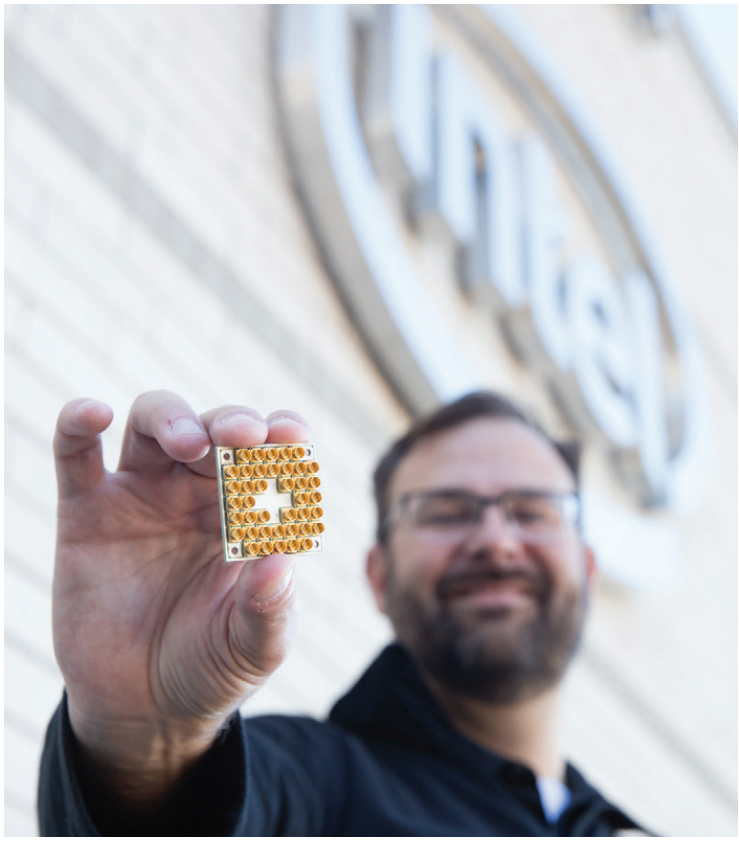
However, despite much experimental progress and speculation, there are inherent challenges to building viable, large-scale quantum systems that produce accurate outputs. Making qubits (the building blocks of quantum computing) uniform and stable is one such obstacle.

Qubits are tremendously fragile: Any noise or unintended observation of them can cause data loss. This fragility requires them to operate at about 20 millikelvin – 250 times colder than deep space. This extreme operating environment makes the packaging of qubits key to their performance and function. Intel's Components Research Group (CR) in Oregon and Assembly Test and Technology Development (ATTD) teams in Arizona are pushing the limits of chip design and packaging technology to address quantum computing's unique challenges.

About the size of a quarter (in a package about the size of a half-dollar coin), the new 17-qubit test chip's improved design features include:

- New architecture allowing improved reliability, thermal performance and reduced radio frequency (RF) interference between qubits.
- A scalable interconnect scheme that allows for 10 to 100 times more signals into and out of the chip as compared to wirebonded chips.
- Advanced processes, materials and designs that enable Intel's packaging to scale for quantum integrated circuits, which are much larger than conventional silicon chips.

"Our quantum research has progressed to the point where our partner QuTech is simulating quantum algorithm workloads,



and Intel is fabricating new qubit test chips on a regular basis in our leading-edge manufacturing facilities," said Dr. Michael Mayberry, corporate vice president and managing director of Intel Labs. "Intel's expertise in fabrication, control electronics and architecture sets us apart and will serve us well as we venture into new computing paradigms, from neuromorphic to quantum computing."

Intel's collaborative relationship with QuTech to accelerate advancements in quantum computing began in 2015. Since that time, the collaboration has achieved many milestones – from demonstrating key circuit blocks for an integrated cryogenic-CMOS control system to developing a spin qubit fabrication flow on Intel's 300mm process technology and developing this unique packaging solution for superconducting qubits. Through this partnership, the time from design and fabrication to test has been greatly accelerated.

"With this test chip, we'll focus on connecting, controlling and measuring multiple, entangled qubits towards an error correction scheme and a logical qubit," said professor Leo DiCarlo of QuTech. "This work will allow us to uncover new insights in quantum computing that will shape the next stage of development."

Advancing the quantum computing system

Intel and QuTech's work in quantum computing goes beyond the development and testing of superconducting qubit devices.

Continued on page 8

Intel delivers, Continued from page 7

The collaboration spans the entire quantum system – or "stack" – from qubit devices to the hardware and software architecture required to control these devices as well as quantum applications. All of these elements are essential to advancing quantum computing from research to reality.

Also, unlike others, Intel is investigating multiple qubit types. These include the superconducting qubits incorporated into this newest test chip, and an alternative type called spin qubits in silicon. These spin qubits resemble a single electron transistor similar in many ways to conventional transistors and potentially able to be manufactured with comparable processes.

While quantum computers promise greater efficiency and performance to handle certain problems, they won't replace the need for conventional computing or other emerging technologies like neuromorphic computing. We'll need the technical advances that Moore's law delivers in order to invent and scale these emerging technologies.

Intel is investing not only to invent new ways of computing, but also to advance the foundation of Moore's Law, which makes this future possible. ◆

Semiconductor industry records best second quarter in three years

Despite a slightly down first quarter, the semiconductor industry achieved near record growth in the second quarter of 2017, posting a 6.1 percent growth from the previous quarter, according to IHS Markit (Nasdaq: INFO). Global revenue came in at $101.4 billion, up from $95.6 billion in the first quarter of 2017. This is the highest growth the industry has seen in the second quarter since 2014.

The memory chip market set records in the second quarter, growing 10.7 percent to a new high of $30.2 billion with DRAM and NOR flash memory leading the charge, growing 14 percent and 12.3 percent quarter-on-quarter, respectively.

"The DRAM market had another quarter of record revenues on the strength of higher prices and growth in shipments," said Mike Howard, director for DRAM memory and storage at IHS Markit. "Anxiety about product availability in the previous third and fourth quarters weighed on the industry. This led many DRAM buyers to build inventory — putting additional pressure on the already tight market. This year is shaping up to smash all DRAM revenue records and will easily pass the $60 billion mark."

"For NOR, the supply-demand balance has tightened raising average selling prices and revenue," said Clifford Leimbach, senior analyst for memory and storage at IHS Markit. "This mature memory technology has been in a steady decline for many years, but some market suppliers are reducing supply or leaving the market, which has tightened supply recently, resulting in the increase of revenue."

In terms of application, consumer electronics and data processing saw the most growth, increasing in revenue by 7.9 percent and 6.8 percent, respectively, quarter-on-quarter. A lot of this growth can be attributed to the continual growth in memory pricing, as supply still remains tight.

Industrial semiconductors showed the third highest growth rate at 6.4 percent during the same period. This growth can be attributable to multiple segments, such as commercial and military avionics, digital signage, network video surveillance, HVAC, smart meters, traction, PV inverters, LED lighting and medical electronics including cardiac equipment, hearing aids and imaging systems.

Top 5 semiconductor companies (Q2-17)

Q1-17 Rank	Q2-17 Rank	Company Name	Q1-17 Revenue ($Million)	Q2-17 Revenue ($Million)	QoQ Growth	Market Share
1	1	Intel	14,009	14,469	3.3%	14.3%
2	2	Samsung Electronics	12,799	14,388	12.4%	14.2%
3	3	SK Hynix	5,507	5,884	6.8%	5.8%
4	4	Micron Technology	4,711	5,352	13.6%	5.3%
5	5	Broadcom Limited	4,021	4,186	4.1%	4.1%
		Top 5 Companies	41,047	44,279	7.9%	43.7%
		Total Semiconductor	**95,574**	**101,426**	6.1%	100%

Source: IHS Markit © 2017 IHS Markit

Another trend in the industrial market is increasing factory automation, which alone is driving growth for discrete power transistors, thyristors, rectifiers and power diodes. The market for these devices is expected to reach $8 billion in 2021, up from $5.7 billion in 2015.

Intel remains the number one semiconductor supplier in the world, followed by Samsung Electronics by a slight margin. IHS Markit does not include foundry operations and other non-semiconductor revenue in the semiconductor market rankings.

Among the top 20 semiconductor suppliers, Advanced Micro Devices (AMD) and nVidia achieved the highest revenue growth quarter over quarter by 24.7 percent and 14.6 percent, respectively. There was no market share movement in the top 10 semiconductor suppliers. However, seven of the 10 companies in the 11 to 20 market share slots did change market share. ◆

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IBM pioneers, Continued from page 6

the cloud for anyone to freely access, and most recently upgraded to a 16-qubit processor available for beta access.

"Thanks to Nobel laureate Richard Feynman, if the public knows one thing about quantum, it knows that nature is quantum mechanical. This is what our latest research is proving – we have the potential to use quantum computers to boost our knowledge of natural phenomena in the world," said Dario Gil, vice president of AI research and IBM Q, IBM Research. "Over the next few years, we anticipate IBM Q systems' capabilities to surpass what today's conventional computers can do, and start becoming a tool for experts in areas such as chemistry, biology, healthcare and materials science."

"The IBM team carried out an impressive series of experiments that holds the record as the largest molecule ever simulated on a quantum computer," said Alán Aspuru-Guzik, professor of chemistry and chemical biology at Harvard University. "When quantum computers are able to carry out chemical simulations in a numerically exact way, most likely when we have error correction in place and a large number of logical qubits, the field will be disrupted. Exact predictions will result in molecular design that does not need calibration with experiment. This may lead to the discovery of new small-molecule drugs or organic materials."

Instead of forcing previously known classical computing methods onto quantum hardware, the scientists reversed the approach by building an algorithm suited to the capability of the current available quantum devices. This allows for extracting the maximal quantum computational power to solve problems that grow exponentially more difficult for classical computers. To characterize the computational power, IBM has adopted a new metric, Quantum Volume. It accounts for the number and quality of qubits, circuit connectivity, and error rates of operations.

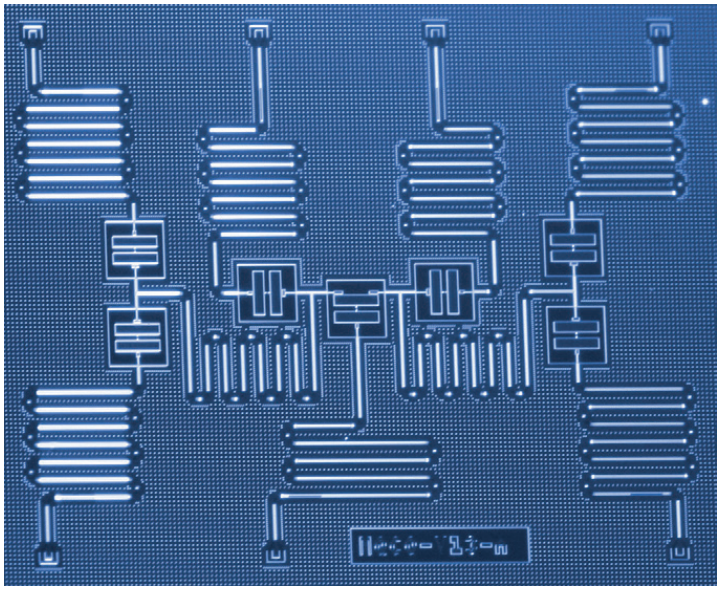


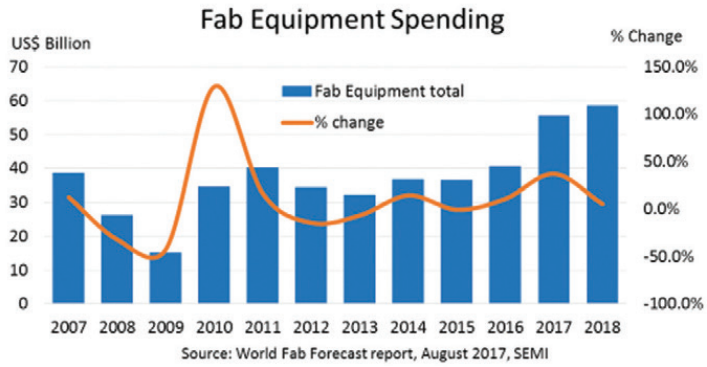
FIGURE 1. IBM scientists have developed a new approach to simulate molecules on a quantum computer that may one day help revolutionize chemistry and materials science. The scientists successfully used six qubits on a purpose-built seven-qubit quantum processor to address the molecular structure problem for beryllium hydride (BeH_2) – the largest molecule simulated on a quantum computer to date.

For future quantum applications, IBM anticipates certain parts of a problem to be run on a classical machine while the most computationally difficult tasks might be off-loaded to the quantum computer. This is how businesses and industries will be able to adopt quantum computing into their technology infrastructure and solutions. To get started today, developers, programmers and researchers can run quantum algorithms, work with individual quantum bits, and explore tutorials and simulations on the IBM Q experience. As well, IBM has commercial partners exploring practical quantum applications through the IBM Research Frontiers Institute. ◈

Fab equipment spending breaking industry records

The latest update to the World Fab Forecast report, published on September 5, 2017 by SEMI, again reveals record spending for fab equipment. Out of the 296 Front End facilities and lines tracked by SEMI, the report shows 30 facilities and lines with over $500 million in fab equipment spending. 2017 fab equipment spending (new and refurbished) is expected to increase by 37 percent, reaching a new annual spending record of about US$55 billion. The SEMI World Fab Forecast also forecasts that in 2018, fab equipment spending will increase even more, another 5 percent, for another record high of about $58 billion. The last record spending was in 2011 with about $40 billion. The spending in 2017 is now expected to top that by about $15 billion.

Examining 2017 spending by region, SEMI reports that the largest equipment spending region is Korea, which increases to about $19.5 billion in spending for 2017 from the $8.5 billion reported in 2016. This represents 130 percent growth year-over-year. In 2018, the World Fab Forecast



report predicts that Korea will remain the largest spending region, while China will move up to second place with $12.5 billion (66 percent growth YoY) in equipment spending. Double-digit growth is also projected for Americas, Japan, and Europe/Mideast, while other regions growth is projected to remain below 10 percent.

The World Fab Forecast report estimates that Samsung is expected to more than double its fab equipment spending in 2017, to $16-$17 billion for Front End equipment, with another $15 billion in spending for 2018. Other memory companies are also forecast to make major spending increases, accounting for a total of $30 billion in memory-related spending for the year. Other market segments, such as Foundry ($17.8 billion), MPU ($3 billion), Logic ($1.8 billion), and Discrete with Power and LED ($1.8 billion), will also invest huge amounts on equipment. These same product segments also dominate spending into 2018.

In both 2017 and 2018, Samsung will drive the largest level in fab spending the industry has ever seen. While a single company can dominate spending trends, SEMI's World Fab Forecast report also shows that a single region, China, can surge ahead and significantly impact spending. Worldwide, the World Fab Forecast tracks 62 active construction projects in 2017 and 42 projects for 2018, with many of these in China. ◆

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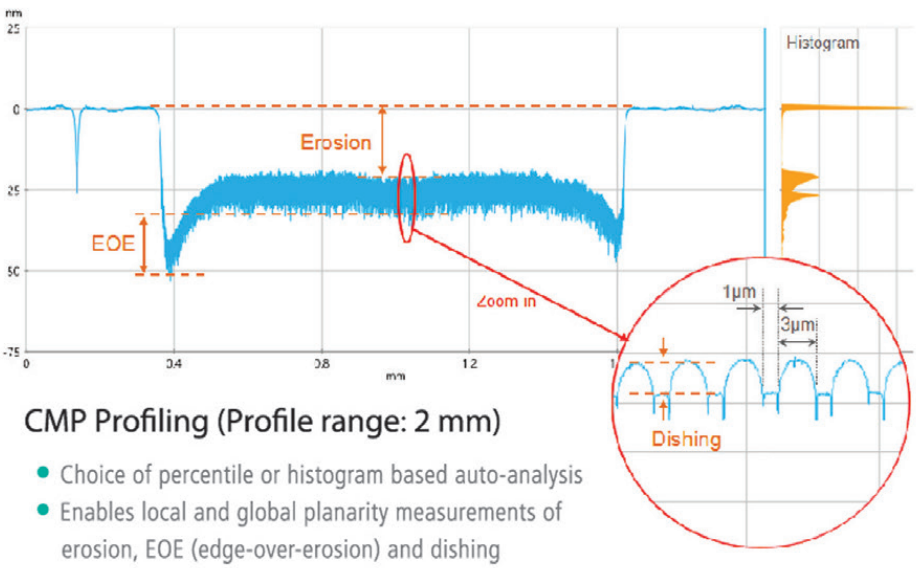

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Gartner identifies, Continued from page 6

least 2020. The ability to use AI to enhance decision making, reinvent business models and ecosystems, and remake the customer experience will drive the payoff for digital initiatives through 2025.

"AI techniques are evolving rapidly and organizations will need to invest significantly in skills, processes and tools to successfully exploit these techniques and build AI-enhanced systems," said Mr. Cearley. "Investment areas can include data preparation, integration, algorithm and training methodology selection, and model creation. Multiple constituencies including data scientists, developers and business process owners will need to work together."

Intelligent apps and analytics

Over the next few years, virtually every app, application and service will incorporate some level of AI. Some of these apps will be obvious intelligent apps that could not exist without AI and machine learning. Others will be unobtrusive users of AI that provide intelligence behind the scenes. Intelligent apps create a new intelligent intermediary layer between people and systems and have the potential to transform the nature of work and the structure of the workplace.

"Explore intelligent apps as a way of augmenting human activity and not simply as a way of replacing people," said Mr. Cearley. "Augmented analytics is a particularly strategic growing area which uses machine learning to automate data preparation, insight discovery and insight sharing for a broad range of business users, operational workers and citizen data scientists."

AI has become the next major battleground in a wide range of software and service markets, including aspects of enterprise resource planning (ERP). Packaged software and service providers should outline how they'll be using AI to add business value in new versions in the form of advanced analytics, intelligent processes and advanced user experiences.

Intelligent things

Intelligent things are physical things that go beyond the execution of rigid programming models to exploit AI to deliver advanced behaviors and interact more naturally with their surroundings and with people. AI is driving advances for new intelligent things (such as autonomous vehicles, robots and drones) and delivering enhanced capability to many existing things (such as Internet of Things [IoT] connected consumer and industrial systems).

"Currently, the use of autonomous vehicles in controlled settings (for example, in farming and mining) is a rapidly growing area of intelligent things. We are likely to see examples of autonomous vehicles on limited, well-defined and controlled roadways by 2022, but general use of autonomous cars will likely require a person in the driver's seat in case the technology should unexpectedly fail," said Mr. Cearley. "For at least the next five years, we expect that semiautonomous scenarios requiring a driver will dominate. During this time, manufacturers will test the technology more rigorously, and the nontechnology issues such as regulations, legal issues and cultural acceptance will be addressed."

Digital twin

A digital twin refers to the digital representation of a real-world entity or system. Digital twins in the context of IoT projects is particularly promising over the next three to five years and is leading the interest in digital twins today. Well-designed digital twins of assets have the potential to significantly improve enterprise decision making. These digital twins are linked to their real-world counterparts and are used to understand the state of the thing or system, respond to changes, improve operations and add value. Organizations will implement digital twins simply at first, then evolve them over time, improving their ability to collect and visualize the right data, apply the right analytics and rules, and respond effectively to business objectives.

"Over time, digital representations of virtually every aspect of our world will be connected dynamically with their real-world counterpart and with one another and infused with AI-based capabilities to enable advanced simulation, operation and analysis," said Mr. Cearley. "City planners, digital marketers, healthcare professionals and industrial planners will all benefit from this long-term shift to the integrated digital twin world."

Cloud to the edge

Edge computing describes a computing topology in which information processing, and content collection and delivery, are placed closer to the sources of this information. Connectivity and latency challenges, bandwidth constraints and greater functionality embedded at the edge favors distributed models. Enterprises should begin using edge design patterns in their infrastructure architectures — particularly for those with significant IoT elements.

While many view cloud and edge as competing approaches, cloud is a style of computing where elastically scalable technology capabilities are delivered as a service and does not inherently mandate a centralized model.

"When used as complementary concepts, cloud can be the style of computing used to create a service-oriented model and a centralized control and coordination structure with edge being used as a delivery style allowing for disconnected or distributed process execution of aspects of the cloud service," said Mr. Cearley.

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Conversational platforms

Conversational platforms will drive the next big paradigm shift in how humans interact with the digital world. The burden of translating intent shifts from user to computer. The platform takes a question or command from the user and then responds by executing some function, presenting some content or asking for additional input. Over the next few years, conversational interfaces will become a primary design goal for user interaction and be delivered in dedicated hardware, core OS features, platforms and applications.

"Conversational platforms have reached a tipping point in terms of understanding language and basic user intent, but they still fall short," said Mr. Cearley. "The challenge that conversational platforms face is that users must communicate in a very structured way, and this is often a frustrating experience. A primary differentiator among conversational platforms will be the robustness of their conversational models and the application programming interface (API) and event models used to access, invoke and orchestrate third-party services to deliver complex outcomes."

Immersive experience

While conversational interfaces are changing how people control the digital world, virtual, augmented and mixed reality are changing the way that people perceive and interact with the digital world. The virtual reality (VR) and augmented reality (AR) market is currently adolescent and fragmented. Interest is high, resulting in many novelty VR applications that deliver little real business value outside of advanced entertainment, such as video games and 360-degree spherical videos. To drive real tangible business benefit, enterprises must examine specific real-life scenarios where VR and AR can be applied to make employees more productive and enhance the design, training and visualization processes.

Mixed reality, a type of immersion that merges and extends the technical functionality of both AR and VR, is emerging as the immersive experience of choice providing a compelling technology that optimizes its interface to better match how people view and interact with their world. Mixed reality exists along a spectrum and includes head-mounted displays (HMDs) for augmented or virtual reality as well as smartphone and tablet-based AR and use of environmental sensors. Mixed reality represents the span of how people perceive and interact with the digital world.

Blockchain

Blockchain is evolving from a digital currency infrastructure into a platform for digital transformation. Blockchain technologies offer a radical departure from the current centralized transaction and record-keeping mechanisms and can serve as a foundation of disruptive digital business for both established enterprises and startups. Although the hype surrounding blockchains originally focused on the financial services industry, blockchains have many potential applications, including government, healthcare, manufacturing, media distribution, identity verification, title registry and supply chain. Although it holds long-term promise and will undoubtedly create disruption, blockchain promise outstrips blockchain reality, and many of the associated technologies are immature for the next two to three years.

Event driven

Central to digital business is the idea that the business is always sensing and ready to exploit new digital business moments. Business events could be anything that is noted digitally, reflecting the discovery of notable states or state changes, for example, completion of a purchase order, or an aircraft landing. With the use of event brokers, IoT, cloud computing, blockchain, in-memory data management and AI, business events can be detected faster and analyzed in greater detail. But technology alone without cultural and leadership change does not deliver the full value of the event-driven model. Digital business drives the need for IT leaders, planners and architects to embrace event thinking.

Continuous adaptive risk and trust

To securely enable digital business initiatives in a world of advanced, targeted attacks, security and risk management leaders must adopt a continuous adaptive risk and trust assessment (CARTA) approach to allow real-time, risk and trust-based decision making with adaptive responses. Security infrastructure must be adaptive everywhere, to embrace the opportunity — and manage the risks — that comes delivering security that moves at the speed of digital business.

As part of a CARTA approach, organizations must overcome the barriers between security teams and application teams, much as DevOps tools and processes overcome the divide between development and operations. Information security architects must integrate security testing at multiple points into DevOps workflows in a collaborative way that is largely transparent to developers, and preserves the teamwork, agility and speed of DevOps and agile development environments, delivering "DevSecOps." CARTA can also be applied at runtime with approaches such as deception technologies. Advances in technologies such as virtualization and software-defined networking has made it easier to deploy, manage and monitor "adaptive honeypots" — the basic component of network-based deception.

Gartner clients can learn more in the Gartner Special Report "Top Strategic Technology Trends for 2018." Additional detailed analysis on each tech trend can be found in the Smarter With Gartner article "Gartner Top 10 Strategic Technology Trends for 2018." ◆

DARPA's new initiative

PHIL GARROU,
Contributing Editor

Earlier this year, DARPA's Microsystems Technology Office (MTO) announced a new Electronics Resurgence Initiative (ERI) "to open pathways for far-reaching improvements in electronics performance well beyond the limits of traditional scaling". Key to the ERI will hopefully be new collaborations among the commercial electronics community, defense industrial base, university researchers, and the DoD. The DoD proposed FY 2018 budget reportedly includes a $75 million allocation for DARPA in support of this, initiative. It is reported that in total we are looking at a $200,000MM program.

The program will focus on the development of new materials for devices, new architectures for integrating those devices into circuits, and software and hardware designs for using these circuits. The program seeks to achieve continued improvements in electronics performance without the benefit of traditional scaling. Bill Chappell, director of DARPA's Microsystems Technology Office (MTO), which will lead the program, announced "For nearly seventy years, the United States has enjoyed the economic and security advantages that have come from national leadership in electronics innovation…..If we want to remain out front, we need to foment an electronics revolution that does not depend on traditional methods of achieving progress. That's the point of this new initiative – to embrace progress through circuit specialization and to wrangle the complexity of the next phase of advances, which will have broad implications on both commercial and national defense interests. "He continued "We need to break away from tradition and embrace the kinds of innovations that the new initiative is all about…"

The chip research effort will complement the recently created Joint University Microelectronics Program (JUMP), an electronics research effort co-funded by DARPA and SRC (Semiconductor Research Corporation). Among the chip makers contributing to JUMP are IBM, Intel Corp., Micron Technology and Taiwan Semiconductor Manufacturing Co. SRC members and DARPA are expected to kick in more than $150 million for the five-year project. Focus areas include high-frequency sensor networks, distributed and cognitive computing along with intelligent memory and storage.

The materials portion of the ERI initiative will explore the use of unconventional materials to increase circuit performance without requiring smaller transistors. Although silicon is used for most of the circuits manufactured today, other materials like GaAs, GaN and SiC have made significant inroads into high performance circuits. It is hoped that the initiative will uncover other elements from the Periodic Table that can provide candidate materials for next-generation logic and memory components. One research focus will be to integrate different semiconductor materials on individual chips, and vertical (3D) rather than planar integration of microsystem components.

The architecture portion of the initiative will examine circuit structures such as Graphics processing units (GPUs), which underlie much of the ongoing progress in machine learning, have already demonstrated the performance improvement derived from specialized hardware architectures. The initiative will explore other opportunities, such as "reconfigurable physical structures that adjust to the needs of the software they support".

The design portion of the initiative will focus on developing tools for rapidly designing specialized circuits. Although DARPA has consistently invested in these application-specific integrated circuits (ASICs) for military use, ASICs can be costly and time-consuming to develop. New design tools and an open-source design paradigm could be transformative, enabling innovators to rapidly and cheaply create specialized circuits for a range of commercial applications.

As part of this overall Electronics Resurgence Initiative, DARPA had their kick of meeting for the CHIPS program (Common Heterogeneous Integration and Intellectual Property (IP) Reuse). The CHIPS vision is an ecosystem of discrete modular, IP blocks, which can be assembled into a system using existing and emerging integration technologies. Modularity and reusability of such IP blocks will require electrical and physical interface standards to be widely adopted by the community supporting the CHIPS ecosystem. The CHIPS program hopes to develop the design tools and integration standards required for modular integrated circuit (IC) designs.

Program contractors include Intel, Micron, Cadence, Lockheed Martin, Northrop Grumman, Boeing, Synopsys, Intrinsix Corp., and Jariet Technologies, U. Michigan, Georgia Tech, and North Carolina State. ◆

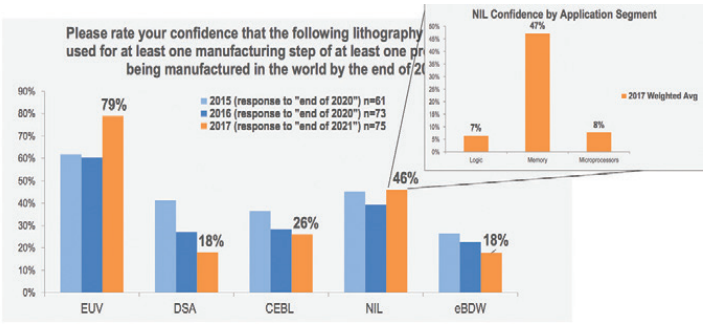
Packaging

EUV leads the next generation litho race

ED KORCZYNSKI,
Sr. Technical Editor

As previously reported by Solid State Technology, the eBeam Initiative recently reported the results of its lithography perceptions and mask-makers' surveys. After the survey results were presented at the 2017 Photomask Technology Symposium, Aki Fujimura, CEO of D2S, the managing company sponsor of the eBeam Initiative, spoke with Solid State Technology about the survey results and current challenges in advanced lithography.

The Figure shows the consensus opinions of 75 luminaries from 40 companies who provided inputs to the perceptions survey regarding which Next-Generation Lithography (NGL) technologies will be used in volume manufacturing over the next few years. "We don't want to interpret these data too much, but at the same time the information should be representative because people will be making business decisions based on this," said Fujimura.



Industry consensus survey results that different Next-Generation Lithography (NGL) technologies will be used in High-Volume Manufacturing (HVM) of ICs over the next few years, including Extreme Ultra-Violet (EUV), Directed Self-Assembly (DSA), Complementary E-Beam Lithography (CEBL), Nano-Imprint Lithography (NIL), and E-Beam Direct Write (eBDW). (Source: eBeam Initiative)

Confidence in Extreme Ultra-Violet (EUV) lithography is now strong, with 79 percent of respondents predicting it will be used in HVM by the end of 2021, a huge increase from 33 percent just three years ago. Another indication of aggregate confidence in EUVL technology readiness is that only 7 percent of respondents thought that "actinic mask inspection" would never be used in manufacturing, significantly reduced from 22 percent just last year.

"Asking luminaries is very meaningful, and obviously the answers are highly correlated with where the industry will be spending on technologies," explained Fujimura. "The predictability of these sorts of things is very high. In particular in an industry with confidentiality issue, what people 'think' is going to happen typically reflects what they know but cannot say."

Fujimura sees EUVL technology receiving most of the investment for next-generation lithography (NGL), "Because EUV is a universal technology. Whether you're a memory or logic maker it's useful for all applications. Whereas nano-imprint is only useful for defect-resistant designs like memory."

Vivek Bakshi's recent blog post details the current status of EUVL technology evolution. With practical limits on the source-power, many organization are looking at ways to increase the sensitivity of photoresist so as to increases the throughput of EUVL processes. Unfortunately, the physics and chemistry of photoresists means that there are inherent trade-offs between the best Resolution and Line-width-roughness (LWR) and Sensitivity, termed the "RLS triangle".

Mask-making metrics

The business dynamics of making photomasks provides leading indicators of the IC fab industry's technology directions. A lot of work has been devoted to keeping mask write times consistent compared with last year, while the average complexity of masks continues to increase with Reticle Enhancement Technologies (RET) to extend the resolution of optical lithography. Even with write times equal, the average mask turn-around time (TAT) is significantly greater for more critical layers, approaching 12 days for 7nm- to 10nm-node masks.

"A lot of the increase in mask TAT is coming from the data-preparation time," explained Fujimura. "This is important for the economics and the logistics of mask shops." The weighted average of mask data preparation time reported in the survey is significantly greater for finer masks, exceeding 21 hours for 7nm- to 10nm-nodes. Data per mask continues to increase; the most dense mask now averages 0.94 TB, and the most dense mask single mask takes 2.2 TB. ◆

Semiconductors

How to solve the BEOL RC delay problem?

ZSOLT TOKEI, *imec, Leuven, Belgium*

The RC delay issues started a few nodes ago, and the problems are becoming worse.

With the 7nm technology node in the development phase and the 5nm node moving into development, transistor scaling gets ever more complex. On top of that, the performance benefits gained at the front-end-of-line (i.e., the transistors) can easily be undone if the back-end-of-line can't come along. BEOL processing involves the creation of stacked layers of Cu wires that electrically interconnect the transistors in the chip. Today, high-end logic chips easily have 12 to 15 levels of Cu wires. With each technology node, this Cu wiring scheme becomes more complex, mainly because there are more transistors to connect with an ever tighter pitch. Shrinking dimensions also means the wires have a reduced cross-sectional area, which drives up the resistance-capacitance product (RC) of the interconnect system. And this results in strongly increasing signal delay. The RC delay issues started a few nodes ago, and the problems are becoming worse. For example, a delay of more than 30% is expected when moving from the 10nm to the 7nm node.

The current BEOL flow

Cu-based dual damascene has been the workhorse process flow for interconnects since its introduction in the mid 1990s. A simple dual damascene flow starts with the deposition of a low-k dielectric material on a structure. These low-k films are designed to reduce the capacitance and the delay in the ICs. In a next step, this dielectric layer is covered with an oxide and a resist, and vias and trenches are formed using lithography and etch steps. These vias connect one metal layer with the layer above or below. Then, a metallic barrier layer is added to prevent Cu atoms from migrating into the low-k materials (**FIGURE 1**). The barrier layers are deposited with physical vapor deposition, using materials such as tantalum and tantalum nitride, and subsequently coated by a Cu seed barrier. In a final step, this structure is electroplated by Cu in a chemical mechanical polishing (CMP) step.

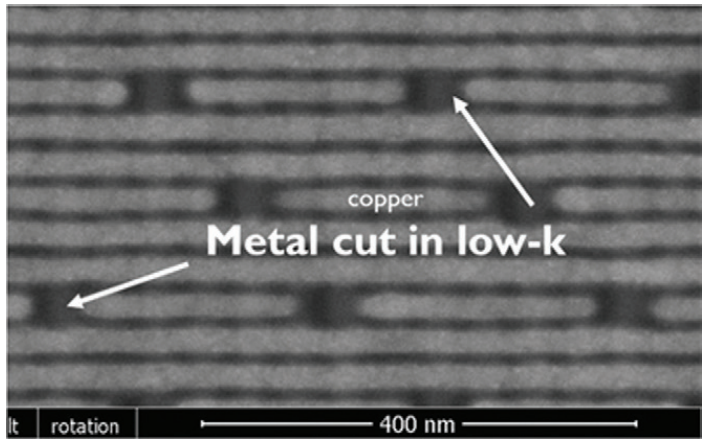


FIGURE 1. Tight pitch copper lines embedded into a low-k material. The metal cuts (or blocks) were enabled by a tone-inversion flow.

A 5nm technology full dual damascene module

The semiconductor industry is hugely in favor of extending the current dual damascene technology as long as possible before moving to a new process. And this starts with incremental changes to the current technology, which should suffice for further scaling to at least the 5nm technology node. Researchers at imec have demonstrated a full dual damascene module for the 5nm technology node. At this node, the BEOL process becomes extremely complex, and interconnects are designed at very tight pitches. For example, a 50% area scaling in logic and 60% scaling of an SRAM cell from 7nm to 5nm results in a gate pitch at around 42nm and an intermediate first routing metal at 32nm pitch (or 16nm half pitch, which is half the distance between identical features). In these BEOL layers, trenches are created which are then filled with metal in a final metallization step. In order to create electrically functional lines, perpendicular block layers to the trenches are added, where metal traces are not formed. One of the many challenges to scaling the interconnects relates to the patterning

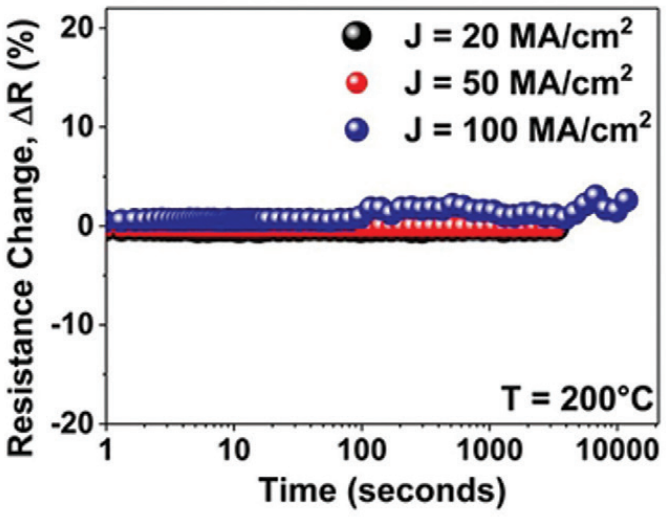


FIGURE 2. Time dependent behavior of Ru nanowires under thermoelectric stress.

options. Patterning these tight pitch layers is no longer possible by using single immersion lithography and direct etch steps. Only multi-patterning – which is known to be very costly and complex – is possible either by immersion or by EUV or by a combination of immersion and EUV exposures to form a single metal layer. At IITC, imec showed a full integration flow using multi-patterning, which enables the patterning of tight-pitch metal-cut (the blocks), and effectively scaling the trench critical dimension to 12nm at 16nm half pitch. The researchers also looked at the reliability, for example at electromigration issues caused by the movement of atoms in the interconnect wires. They demonstrated the ability of imec's Cu metallization scheme at 16nm critical dimension with extendibility to 12nm width, and investigated full ruthenium (Ru) metallization as copper replacement.

Scaling the BEOL beyond the 5nm node

For the technology nodes below the 5nm, the team of imec is investigating a plethora of options and comparing their merits. Options include new materials for conductors and dielectrics, barrier layers, vias, and new ways to deposit them; innovative BEOL architectures for making 2.5D/3D structures; new patterning schemes; co-optimization of system and technology, etc.

For example, to achieve manufacturable processes and at the same time control the RC delay, scaling boosters, such as fully self-aligned vias, are increasingly being used. Via alignment is a critical step in the BEOL process, as it defines the contact area between subsequent interconnect levels. Any misalignment impacts both resistance and reliability. Imec's team has shown the necessity of using a fully self-aligned via to achieve overlay specifications, and proposed a process flow for 12nm half pitch structures.

Also, self-assembled monolayers (SAMs) open routes to new dielectric and conductor schemes. SAMs composed of sub-1nm organic chains and terminated with desired functional groups can help engineering thin-film dielectric and metal interfaces, and can strongly inhibit interfacial diffusion. The use of SAMs has been a topic of research for the past ten years. Imec has now moved this promising concept from lab to fab, and combined SAMs with a barrier/liner/metallization scheme on a full wafer. The researchers investigated the implications on the performance and scaling ability of this process flow, and demonstrated a ~18% reduction in the RC of 22nm half-pitch dual damascene interconnects, due to a better interface and thinner barrier.

For conventional BEOL metallization, a barrier layer is coated by a Cu seed barrier, and this structure is electroplated with low-resistive Cu, which acts as the conductor. But when moving to sub-10nm interconnects, the resistivity of Cu continues to increase. At the same time, the diffusion barrier – which is highly resistive and difficult to scale – is taking up more space, thereby increasing the overall resistance of the barrier/Cu structure. Therefore, alternative metals are being investigated that could possibly serve as a replacement for Cu and do not require a diffusion barrier. Among the potential candidates, such as Co, Ni, Mo, etc., platinum-group metals, especially ruthenium (Ru), have shown great promise due to their low bulk resistivity and resistance to oxidation. They also have a high melting point which can result in better electromigration behavior (**FIGURE 2**). Imec has realized Ru nanowires with 58nm2 cross section area. The nanowires exhibit low resistivity and robust wafer-level reliability. For example, a very high current carrying capacity with fusing currents as high as 720MA/cm2 was demonstrated.

At the 2017 IITC conference, this author was invited to take part in a panel discussion, organized by Applied Materials, to discuss the latest developments in metallization at single-digit nodes, the challenges and bottlenecks arising at these very small dimensions, and new application-driven requirements. Distinguished speakers from the technical field reviewed viable solutions for extending the current technology and alternative options were discussed. From the

discussion it is clear that the biggest immediate benefit can be found in the area of conductors – both from the material side as well as design. Indeed, it is driving the replacement of copper at specific metallization levels. Other avenues – such as dielectric innovations, functionality in the BEOL or 2D materials – remain interesting options for the R&D pipeline.

As an option that is further out, spin wave propagation in conductors is an alternative signaling to traditional electron based propagation.

Adding additional functionality in the BEOL

In the future, more and more technology options may get dictated by the requirements of systems or even applications. This could result in a separate technology for e.g. high-performance computing, low-power mobile communication, chips for use in medical applications, or dedicated chips for IoT sensors. Along the same lines, imec is investigating the benefits of introducing additional functionality in the BEOL.

More specifically, imec is evaluating the possibility of integrating thin-film organic transistors – with typically low-leakage level – into the BEOL interconnect circuitry of Si FinFETs. The potential advantages of fabricating them together are mainly a reduced power consumption and improved area saving. A variety of circuits can fully utilize the benefits of this hybrid processing, including portable applications, eDRAM, displays and FPGA applications. As a concrete example, imec researchers are currently merging imec's expertise in BEOL technologies and in thin-film-based flat panel displays, thereby opening opportunities for new applications... ◆

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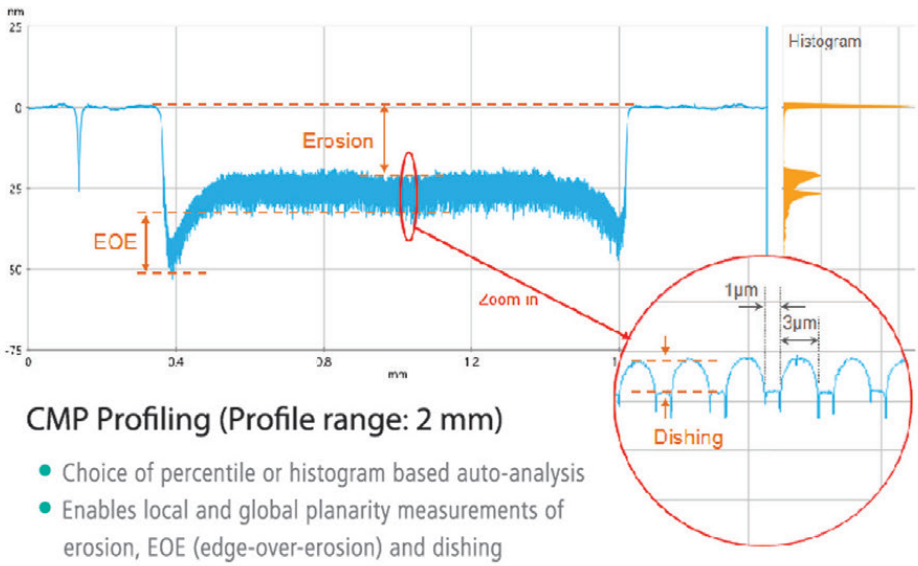

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Embedded FPGAs offer SoC flexibility

DAVE LAMMERS, *Contributing Editor*

With mask costs rising and the need for flexibility growing, companies are beginning to adopt embedded field programmable gate arrays in their SoC designs.

It was back in 1985 that Ross Freeman invented the FPGA, gaining a fundamental patent (#4,870,302) that promised engineers the ability to use "open gates" that could be "programmed to add new functionality, adapt to changing standards or specifications, and make last-minute design changes."

Freeman, a co-founder of Xilinx, died in 1989, too soon to see the emerging development of embedded field programmable logic arrays (eFPGAs). The IP cores offer system-on-chip (SoC) designers an ability to create hardware accelerators and to support changing algorithms. Proponents claim the approach provides advantages to artificial intelligence (AI) processors, automotive ICs, and the SoCs used in data centers, software-defined networks, 5G wireless, encryption, and other emerging applications.

With mask costs escalating rapidly, eFPGAs offer a way to customize SoCs without spinning new silicon. While eFPGAs cannot compete with custom silicon in terms of die area, the flexibility, speed, and power consumption are proving attractive.

Semico Research analyst Rich Wawrzyniak, who tracks the SoC market, said he considers eFPGAs to be "a very profound development in the industry, a capability that is going to get used in lots of places that we haven't even imagined yet."

While Altera, now owned by Intel, and Xilinx, have not ventured publicly into the embedded space, Wawrzyniak noted that a lively bunch of competitors are moving to offer eFPGA intellectual property (IP) cores.

Multiple competitors enter eFPGA field

Achronix Semiconductor (Santa Clara, Calif.) has branched out from its early base in stand-alone FPGAs, using Intel's 22nm process, to an IP model. It is emphasizing its embeddable Speedcore eFPGAs that can be added to SoCs using TSMC's 16FF foundry process. 7nm IP cores are under development.

Efinix Inc. (Santa Clara, Calif.) recently rolled out its Efinix Programmable Accelerator (EPA) technology.

Efinix (efinixinc.com) claims that its programmable arrays can either compete with established stand-alone FPGAs on performance, but at half the power, or can be added as IP cores to SoCs. The Efinix Programmable Accelerator technology can provide a look up table (LUT)-based logic cell or a routing switch, among other functions, the company said.

Efinix was founded by several managers with engineering experience at Altera Corp. at various times in their careers -- Sammy Cheung, Tony Ngai, Jay Schleicher, and Kar Keng Chua -- and has financial backing from two Malaysia-based investment funds.

Flex Logix Technologies, (Mountain View, Calif.) an eFPGA startup founded in 2014, recently gained formal

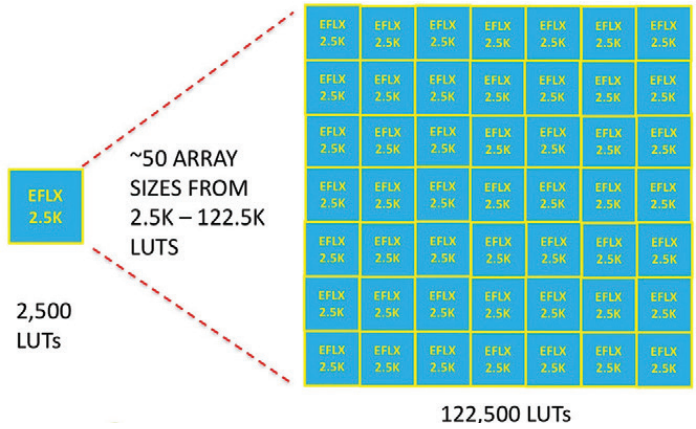


FIGURE 1. Flex Logix embedded FPGAs are constructed modularly, using an EFLX-2.5K IP core. (Source: Flex Logix)

admittance to TSMC's IP Alliance program. It supports a wide array of foundry processes, providing embedded FPGA IP and software tools for TSMC's 16FFC/FF+, 28HPM/HPC, and 40ULP/LP.

QuickLogic adds SMIC to foundry roster

Menta is another competitor in the FPGA space. Based in Montpellier, France, Menta is a privately held company founded a decade ago that offers programmable logic IP targeted to both GLOBALFOUNDRIES (14LPP) and TSMC (28HPM and 28HPC+) processes.

Menta offers either pre-configured IP blocks, or custom IPs for SoCs or ASICs. The French company supports its IP with a tool set, called Origami, which generates a bitstream from RTL, including synthesis. Menta said it has fielded four generations of products that in use by customers now "for meeting the sometimes conflicting requirements of changing standards, security updates and shrinking time-to-market windows of mobile and consumer products, IoT devices, networking and automotive ICs."

QuickLogic, a Silicon Valley stalwart founded in 1988, also is expanding its eFPGA capability. In mid-September, QuickLogic (Sunnyvale, Calif.) (quicklogic.com) announced that its eFPGA IP can now be used with the 40nm low-leakage process at Shanghai-based Semiconductor Manufacturing International Corp. (SMIC). QuickLogic also offers its eFPGA technology on several of the mature GLOBALFOUNDRIES processes, and is participating in the foundry's 22FDX IP program.

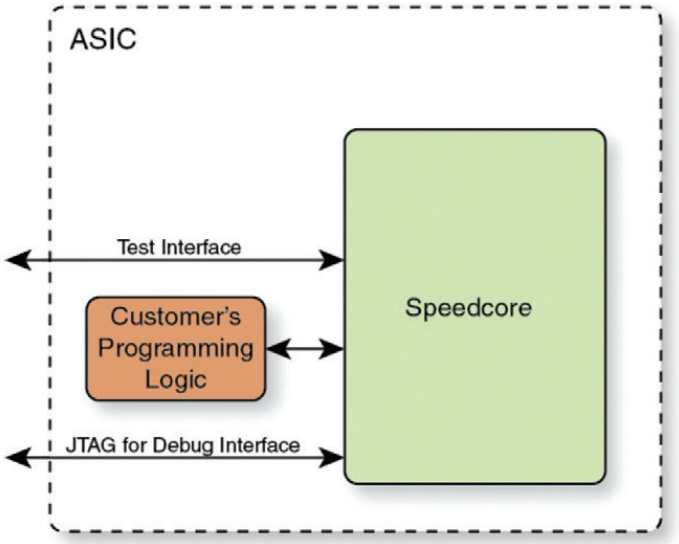


FIGURE 2. Achronix offers Speedcore eFPGAs, based on the same architecture as its standalone FPGAs. (Source: Achronix Semiconductor)

Wawrzyniak, who tracks the SoC market for Semico Research, said an important market is artificial intelligence, using eFPGA gates to add a flexible convolutional neural network (CNN) capability. Indeed, Flex Logix said one of its earliest adopters is an AI research group at Harvard University that is developing a programmable AI processor.

A seminal capability

The U.S. government's Defense Advanced Projects Agency (DARPA) also has supported Flex Logix by taking a license, endorsing an eFPGA capability for defense and aerospace ICs used by the U.S. military.

With security being such a concern for the Internet of Things edge devices market, Wawrzyniak said eFPGA gates could be used to secure IoT devices against hackers, a potentially large market.

"The major use is in apps and instances where people need some programmability. This is a seminal, basic capability. How many times have you heard someone say, 'I wish I could put a little bit of programmability into my SoC.' People are going to take this and run with it in ways we can't imagine," he said.

Bob Wheeler, networking analyst at The Linley Group, said the intellectual property (IP) model makes sense for startups. Achronix, during the dozen years it developed and then fielded its standalone FPGAs, "was on a very ambitious road, competing with Altera and Xilinx. Achronix went down the road of developing parts, and that is a tall order."

While the cost of running an IP company is less than fielding stand-alone parts, Wheeler said "People don't appreciate the cost of developing the software tools, to program the FPGA and configure the IP." The compiler, in particular, is a key challenge facing any FPGA vendor.

Wheeler said Achronix has gained credibility for its tools, including its compiler, after fielding its high-performance discrete FPGAs in 2016, made on Intel's 22nm process.

And Wheeler cautioned that IP companies face the business challenge of getting a fair return on their development efforts, especially for low-cost IoT solutions where companies maintain tight budgets for the IP that they license.

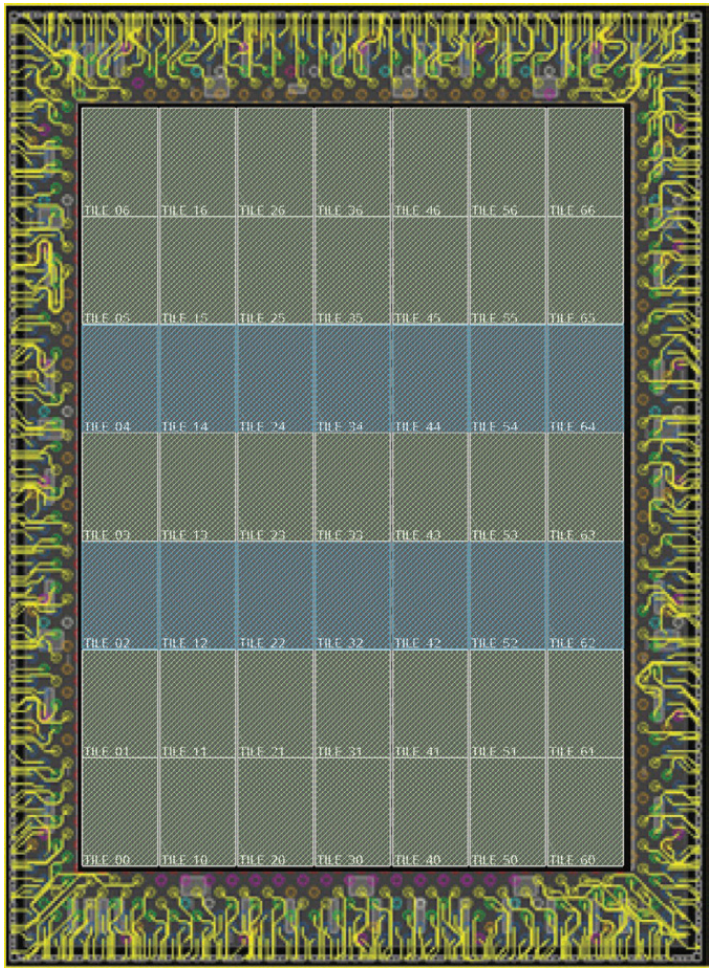


FIGURE 3. Flex Logix supports several process generations at foundry TSMC. The 16nm test chip is being evaluated. (Source: Flex Logix)

Achronix earlier this year announced that its 2017 revenues will exceed $100 million, based on a seven-times increase in sales of its Speedster 22i FPGA family, as well as licensing of its Speedcore embedded IP products, targeted to TSMC's leading-edge 16 nm node, with 7nm process technology for design starts beginning in the second half of this year. Achronix revenues "began to significantly ramp in 2016 and the company reached profitability in Q1 2017," said CEO Robert Blake.

Escalating mask costs

Geoff Tate, now the CEO of Flex Logix Technologies, earlier headed up Rambus for 15 years. Tate said Flex Logix uses a hierarchical interconnect, developed by co-founder Cheng Wang and others while he earned his doctorate at UCLA. The innovative interconnect approach garnered the Lewis Outstanding Paper award for Wang and three co-authors at the 2014 International Solid-State Circuits Conference (ISSCC), and attracted attention from venture capitalists at Lux Ventures and Eclipse Ventures.

Tate said one of those VCs came to him one day and asked for an evaluation of Wang & Co.'s technology. Tate met with Wang, a native of Shanghai, and found him to be anything but a prima donna with a great idea. "He seemed very motivated, not just an R&D guy."

While most FPGAs use a mesh interconnect in an X-Y grid of wires, Wang had come up with a hierarchical interconnect that provided high density without sacrificing performance, and proved its potential with prototype chips at UCLA.

"Chips need to be more flexible and adaptable. FPGAs give you another level of programmability," Tate noted.

Meanwhile, potential customers in networking, data centers, and other markets were looking for ways to make their designs more flexible. An embedded FPGA block could help customers adapt a design to new wireless and networking protocols. Since mask costs were escalating, to an estimated $5 million for 16nm designs and more than double that for 7nm SoCs, customers had another reason to risk working with a startup.

TSMC has supported Flex Logix, in mid-September awarding the company the TSMC Open Innovation Platform's Partner of the Year Award for 2017 in the category of New IP.

"Our lead customer has a working chip, with embedded FPGA on it. They are in the process of debugging rest of their chip. Overall, we are still in the early stages of market development," Tate said, explaining that semiconductor companies are understandably risk-averse when it comes to their IP choices.

Asked about the status of its 16nm test chip, Tate said "the silicon is out of the fab. The next step is packaging, then evaluation board assembly. We should be doing validation testing starting in late September."

Potential customers are in the process of sending engineers to Flex Logix to look at metrics of the largest 16nm arrays, such as IR drop, vest vectors, switching simulations, and the like. "They making sure we are testing in a thorough fashion. If we screw them over, they'll tell everybody, so we have got to get it right the first time," Tate said. ◆

2017 sees advances in connected devices, memory

STACY WEGNER, *Ottawa, Canada, and* **JEONGDONG CHOE**, *Ottawa, Canada*

The technologies to watch identified by TechInsights analysts at the beginning of the year have not been disappointing.

TechInsights analysts have been keeping an intent watch on where technology has progressed, how it's changing, and what new developments are emerging. At the end of the first quarter, our analysts shared their insights and thoughts about what to keep an eye on as the year unfolds. In this article, they provide an update on what 2017 has delivered so far.

Intelligent, connected devices

As we wrote earlier this year, in 2016, wearables were extremely interesting mainly because there was so much uncertainty around whether or not the market would be viable. Some, no, many, say the wearables market will cool off and possibly just expire. At TechInsights, we do will not speculate about whether this market is going to survive. We will report what we find and analyze what is currently being sold. Apple, Samsung, and Huawei have all released smartwatches for what would parallel a "flagship" in the mobile market (**FIGURE 1**). Fitness bands are becoming even "smarter" and combining sensors where possible. Perhaps one of the most notable developments is Nokia's acquisition and complete integration of Withings into its existing brands.

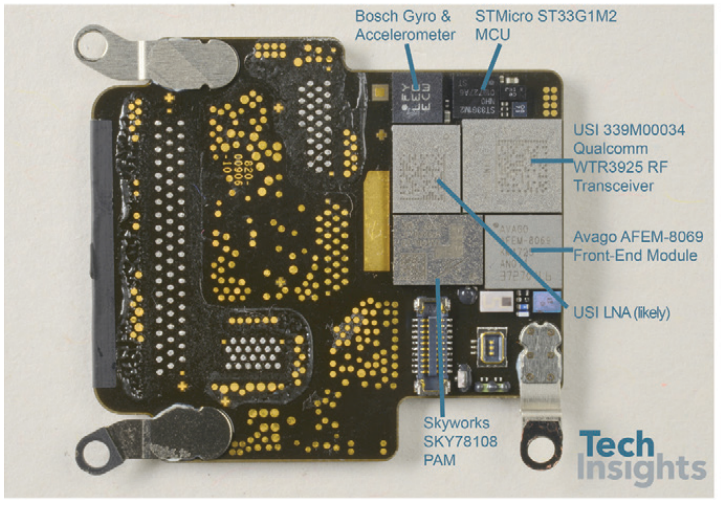


FIGURE 1. Circuit board of the Apple Watch Series 3.

STACY WEGNER *is a Product Manager, and* **JEONGDONG CHOE**, *Ph.D., Senior Technical Fellow, Technology Intelligence, TechInsights, Ottawa, Canada.*

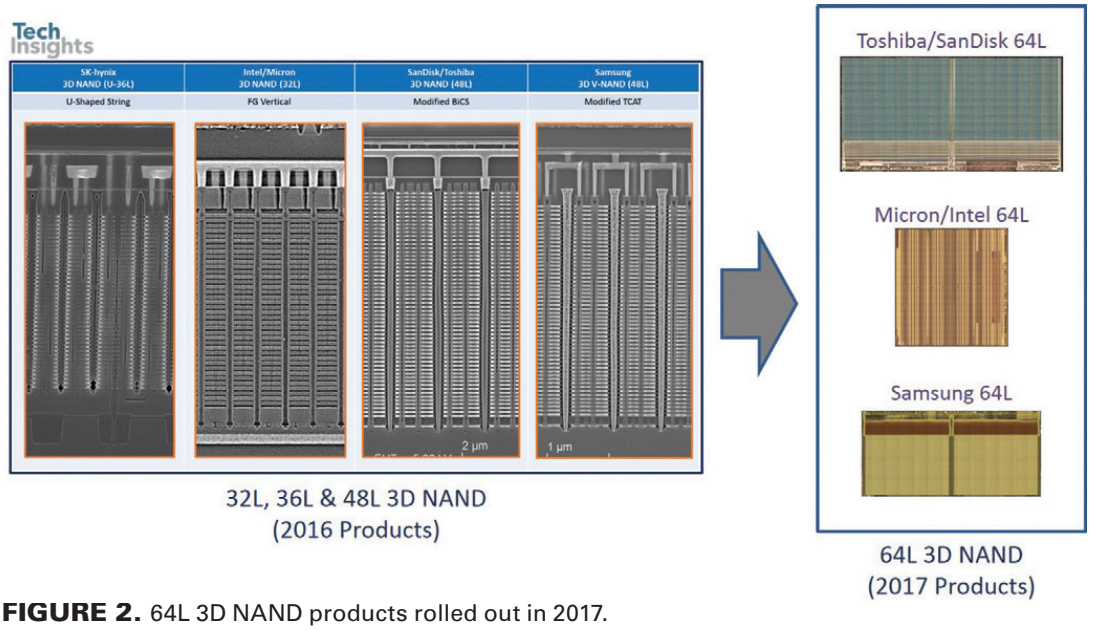


FIGURE 2. 64L 3D NAND products rolled out in 2017.

We are witnessing the "rise of the machines," in products from scales and hair brushes to rice cookers. Primarily these devices offer consumers convenience. For example, with a connected scale, instead of recording your weight manually, the smart scales do the job for you, syncing with various health apps so you can track your weight over time. The connected hair brush provides insights into your hair's manageability, frizziness, dryness, split ends and breakage to provide a hair quality score. Brushing patterns, pressure applied and brush stroke counts are analyzed to measure effectiveness of brushing habits and a personal diagnosis is provided with tips and real-time product recommendations. The most common connected devices include refrigerators, lights, washing machines, thermostats, and televisions.

One dominant example is the ever-popular Amazon Echo, which has taken on a life of its own and is generating spin-off markets and competition. In July, it was reported that Amazon's Alexa voice platform passed 15,000 skills — the voice-powered apps that run on devices like the Echo speaker, Echo Dot, newer Echo Show and others. The figure is up from the 10,000 skills Amazon officially announced in February. Amazon's Alexa is building out an entire voice app ecosystem putting it much further ahead than its nearest competitor. The success seen with Echo has motivated other companies like Google, Lenovo, LG, Samsung and Apple to release competitive speakers, however it is estimated that Amazon is expected to control 70 percent of the market this year. In addition, Amazon and Microsoft recently announced a partnership to better integrate their digital assistants. This cross-platform integration provides users with access to Cortana features that Alexa is missing, and vice versa. Finally, the high-performance far-field microphones found in Amazon Echo products may soon find their way to other hardware companies as Amazon announced that the technology is available to those who want to integrate into the Alexa Experience. With its new reference solution, it's never been easier for device makers to integrate Alexa and offer their customers the same voice experiences.

In the mobile market overall, we are seeing a strong emergence of devices targeted for the very hot market of India. The mobile devices for this market range from supporting 15 or more cellular bands to as few as five cellular bands, and that is for smartphones. At TechInsights, we will be analyzing OEMs in India like Micromax, Intex, and Lava to see how

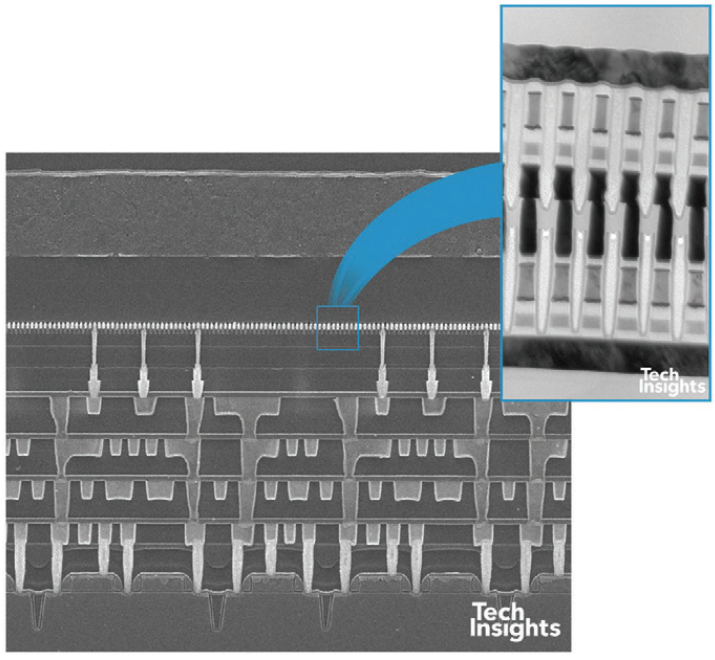


FIGURE 3. Intel X-point Memory Array X-section SEM and TEM images.

they approach dealing with strong competitors like Samsung and Xiaomi.

Memory devices

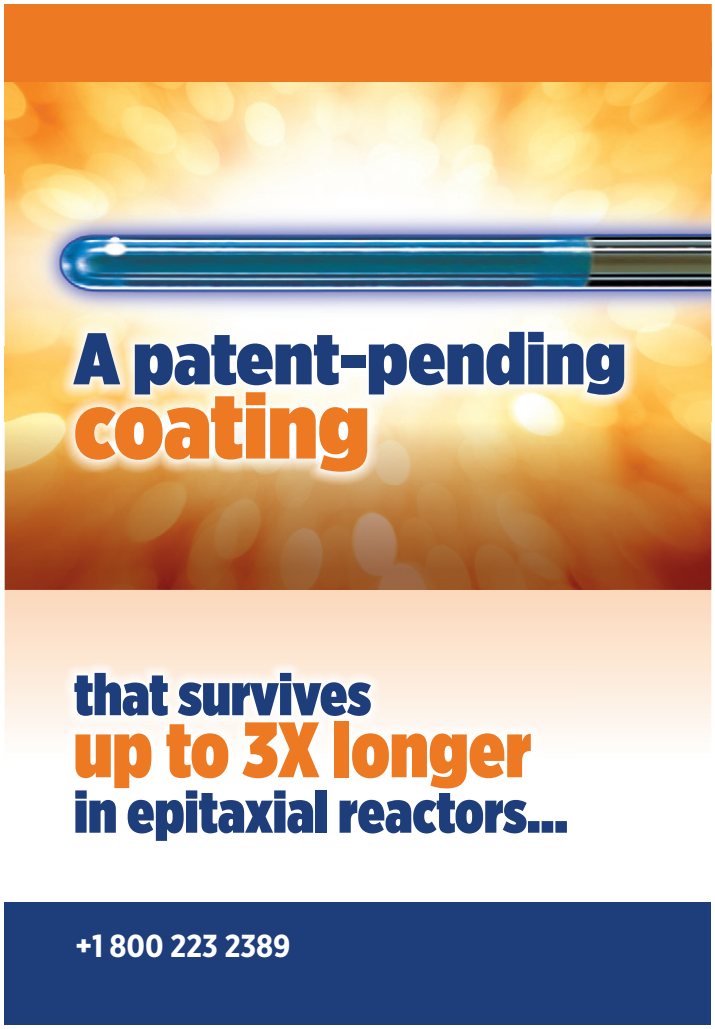
In early 2017, 32L and 48L 3D NAND products were common and all the NAND players were eager to develop next generation 3D NAND products such as 64L and 128L. 3D NAND has been jumping into 64L (**FIGURE 2**). Samsung, Western Digital, Toshiba, Intel, and Micron already revealed CS or mass-products on the market. SK Hynix also showed their 72L NAND die as a CS product. In the second half of this year, we will see 64L and 72L NAND products on the commercial market. For n+1 generation with 96L or 128L, we expect that two-stacked cell array architecture for 3D NAND would be adopted in 2018. Micron/Intel will keep their own FG based 3D NAND cell structure for the next generation.

Referring to DRAM, all the major players already used their advanced process technology for cell array integration such as an advanced ALD for high-k dielectrics, low damage plasma etching and honeycomb capacitor structure. Buried WL, landing pad and plug for a capacitor node, and MESH structure are still main stream. Samsung 18nm DRAM products for DDR4 and LPDDR4X are on the market. SK Hynix and Micron will reveal the same tech node DRAM products in this year. n+1 generation with 15nm or 16nm node will be next in 2018. Once 6F2 15nm DRAM cell technology is successful, 4F2 DRAM products such as a capacitorless DRAM might be delayed. In 2018, 18nm and 15nm DRAM technology will be used for GDDR6 and LPDDR5.

When it comes to emerging memory, 3D XPoint memory technology is a hot potato (**FIGURE 3**). The XPoint products from Intel are on the market as an Optane SSD with 16GB and 32GB. Performance including retention, reliability and speed are not matched as expected, but they used a double stacked memory cell between M4 and M5 on the memory array. It's a PCM with GST based material. An OTS with Se-As-Ge-Si is added between the PCM and the electrode (WL or BL). We expect to see multiple (triple or quadruple) stacked XPoint memory architecture within a couple years. For other emerging memory such as STT-MRAM, PCRAM and ReRAM, we're waiting on some commercial products from Adesto (CBRAM 45nm, RM33 series) and Everspin (STT-MRAM pMTJ 256Mb, AUP-AXL-M128).

Conclusion

The technologies to watch identified by TechInsights analysts at the beginning of the year have not been disappointing. As our analysts continue to examine and reveal the innovations others can't inside advanced technology, we will continue to share our findings on these and new technologies as they emerge, including how they are used, how they impact the market, and how they will be changed by the next discovery or invention.



Temperature impact on UHP pressure transducer performance

YANLI CHEN, *Ph.D. and* **MATTHEW MILBURN**, *P.E., UCT, Hayward, CA*

The temperature impact on the performance of UHP pressure transducers is discussed.

As the semiconductor industry develops new films that require heated delivery systems, all related components need to be characterized at elevated temperatures. Vacuum pressure measurement components, typically called manometers, have been used at elevated temperatures for many years. In fact, many of the vacuum measurement transducers are internally heated to a known temperature to stabilize the mechanical relationships between moving parts and the sensors used to measure the movement. This stabilization enables the precision and inaccuracy of the measurement to be greatly improved. For positive pressure UHP transducers, this elevated temperature characterization has not been done. Based on the testing performed at UCT, temperature related performance variations are very real and must be carefully considered before choosing a positive pressure transducer for elevated temperature use. Since the industry is driving toward higher delivery system operating temperatures, temperature effects will become more important.

The UHP pressure transducer is a widely-used component in the semiconductor industry and the performance is very important for process control and process monitoring. Selecting a proper UHP pressure transducer with good performance for the specific application is challenging, because different UHP pressure transducers manufacturers have different parameters listed in their data and specification sheets. Behind the data presented, it was found that different test procedures and data processing methods were used to determine and report performance characteristics. This reality creates a situation where, without standardized test method or reporting format, neither the specifier nor the end user can compare the performance of different brands of pressure transducers. To date, the industry has not recognized the full scope of the specification problem nor developed a standardized testing and reporting program. A new push toward standardization has become available with the publishing of SEMI F113 "Test Method For Pressure Transducers Used In Gas Delivery Systems" in November of 2016.

In order to have a better understanding about the performance of different UHP pressure transducer manufacturers' products, UCT initialized a comprehensive performance evaluation project with a participation of three major UHP pressure transducer manufacturers (MFG A, MFG B and MFG C). The totality of the project covered a total of nine test categories, including warm up time test, input voltage sensitivity test, repeatability, linearity, hysteresis and inaccuracy test, reproducibility test, thermal coefficient test, drift test, accelerated lift cycle test, proof and burst test. The topic of this paper is the thermal coefficient test. Interested readers can find the other article "Comprehensive performance evaluation of UHP pressure transducers" published on the VOL. 59 NO. 4 of Solid State Technology (June 2016), which demonstrated the test method of repeatability, linearity, hysteresis and inaccuracy.

Ideally, a pressure transducer would sense pressure and remain unaffected by other environmental changes. In reality, however, the signal output of every pressure transducer is somewhat affected by variations in environment and fluid temperature. Temperature changes can cause the expansion and contraction of the sensor materials, fill fluids, housings, and electronics. Temperature changes also can affect the sensor's resistors and electrical connections through the thermoelectric effects. Typically, a sensor's behavior regarding changes in temperature is characterized by two temperature coefficients: temperature effect on zero (TC zero) and temperature effect on span (TC Span). TC zero is expressed as a percentage of full scale and indicates the greatest deviation of a pressure transducer at zero setpoint per equal temperature change (such as 10K or 50°C) during the operating temperature range. TC span is also expressed as a percentage of full scale and indicates the greatest deviation of a pressure transducer at 100%FS setpoint per equal temperature change (such as 10K or 50°C) during the operating temperature range. **FIGURES 1, 2 and 3** list the TC zero and TC span of pressure transducer products of MFG A, MFG B and MFG C, respectively.

Zero and Span Temperature Coefficient (each):
±0.50 % FS (68°F to 140°F, 20°C to 60°C)

FIGURE 1. Thermal Coefficient Specification of MFG A products.

Temperature coefficients within rated temperature range (active compensated):	
Mean TC zero	=0.10 % of span /10K
Mean TC range	=0.15 % of span /10K

FIGURE 2. Thermal Coefficient Specification of MFG B products

Thermal Effects[1)]	
Compensated Range °F (°C)	+15 to +150 (-9 to +65)
Zero Shift %FS/100°F (%FS/50°C)	2.0 (1.8)
Span Shift %FS/100°F (%FS/50°C)	2.0 (1.8)

[1)] Units calibrated at nominal 70°F. Maximum thermal error computed from this datum.

FIGURE 3. Thermal Coefficient Specification of MFG C products.

Comparing the three thermal coefficient specifications above for MFG A, MFG B and MFC C, it is not possible to conclude which manufacturer's product is the best for thermal behavior. Therefore, a standard test method and data process for thermal effects evaluation is needed.

Test setup and procedure

Three major UHP pressure transducer manufacturer (MFG A, MFG B, and MFG C) participated in this comprehensive performance evaluation project by providing test samples. **Table 1** shows the detailed information of all the devices under tests (DUTs). Twelve DUTs were installed in a test fixture designed by UCT for running simultaneous tests. The schematic of the test fixture is shown in **FIGURE 4**. The benefit of this design is to save significant time that would be otherwise used for assembly, disassembly, and testing, and eliminates the potential for setup errors if each transducer was tested separately in the battery of tests.

The test was conducted in a temperature controlled environmental chamber (see **Figure 5**). The following sequence of steps were taken:

Manufacturer	MFG A	MFG B	MFG C
Pressure Range	0–250 psia	-14.7–235.3 psig	-14.7–235.3 psig
Output Voltage (VDC)	0-10	0-10	2-10
Excitation Voltage (VDC)	13-32	14-30	12-30
Fitting Type	VCR-M	VCR-F	VCR-M
Sample Quantity	4	4	4

TABLE 1. Detailed information of DUTs

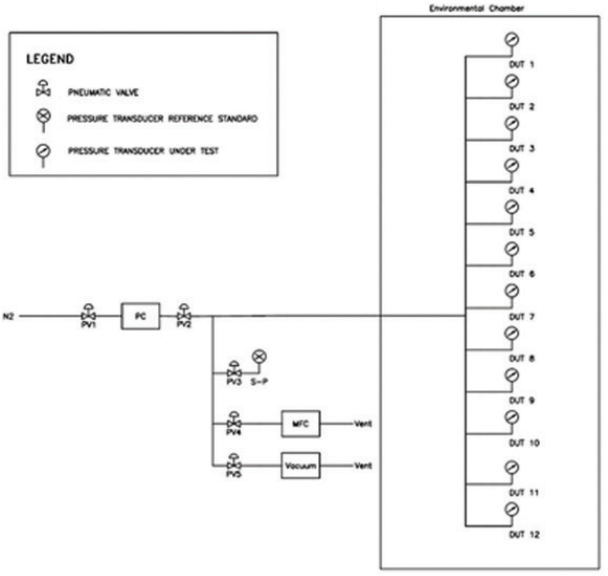
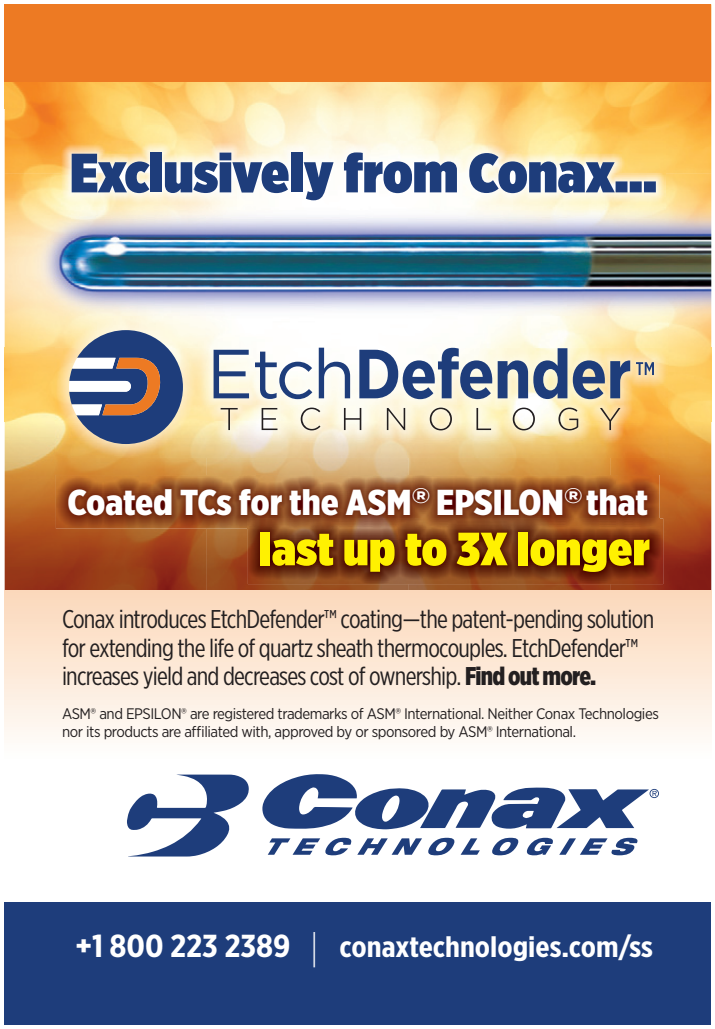


FIGURE 4. Schematic of the test fixture.

- A leak integrity test
- Make the initial zero adjustment per the manufacturer's instructions
- Adjust the temperature of the environmental chamber to 0°C and allow the temperature to stabilize for a minimum period of two hours.



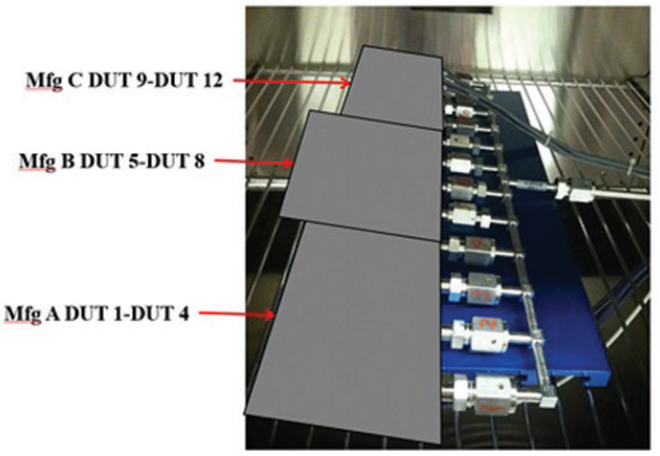


FIGURE 5. Picture of all DUTs inside the environmental chamber.

- Adjust the pressure to 0%FS (-14.7 psig), and record the signal output of all the DUTs and the pressure reference device after the pressure stabilization.
- Adjust the pressure to 100%FS (235.3 psig), and record the signal output of all the DUTs and the pressure reference device after the pressure stabilization.
- Repeat the same procedure for the temperature setpoints of 20°C, 40°C and 60°C at the pressure setpoints of 0%FS and 100%FS.

Results and discussion

The TC zero (0%FS) and TC span (100%FS) values of all DUTs are listed in **Table 2**. For each manufacturer's sample group, the highest value for the thermal coefficients at zero and span are highlighted in red; the lowest value for the thermal coefficients at zero and span are highlighted in green. To reiterate, the smaller the TC value, the better.

- For the DUTs from MFG A, the smallest TC zero is 0.0022%FS/°C and the smallest TC span is 0.0324%FS/°C.
- For the DUTs from MFG B, the smallest TC zero is 0.0012%FS/°C and the smallest TC span is 0.0099%FS/°C.
- For the DUTs from MFG C, the smallest TC zero is 0.0102%FS/°C and the smallest TC span is 0.0215%FS/°C.
- For the DUTs from MFG A, the largest TC zero is 0.0127%FS/°C and the largest TC span is 0.0564%FS/°C.
- For the DUTs from MFG B, the largest TC zero is 0.0042%FS/°C and the largest TC span is 0.0155%FS/°C.
- For the DUTs from MFG C, the largest TC zero is 0.0283%FS/°C and the largest TC span is 0.0354%FS/°C.

The extreme TC values for each manufacturer are summarized in **Table 3**. As shown in this table, the MFG B product has the lowest value (0.0042%FS/°C) and MFG C product has the highest value (0.0283%FS/°C) for the TC zero. For the TC span, the MFG B product still has the lowest value (0.0155%FS/°C), and the MFG A product has the highest value (0.0564%FS/°C).

MFG	Tag #	TC Zero (%FS/°C)	TC Span (%FS/°C)
A	DUT 1	0.0042	0.0564
	DUT 2	0.0127	0.0324
	DUT 3	0.0117	0.0564
	DUT 4	0.0022	0.0554
B	DUT 5	0.0012	0.0099
	DUT 6	0.0042	0.0155
	DUT 7	0.0027	0.0120
	DUT 8	0.0022	0.0114
C	DUT 9	0.0177	0.0235
	DUT 10	0.0102	0.0215
	DUT 11	0.0283	0.0354
	DUT 12	0.0252	0.0323

TABLE 2. Summary of thermal coefficient of All DUTs

MFG	TC Zero (%FS/°C)	TC Span (%FS/°C)
A	0.0127	0.0564
B	0.0042	0.0155
C	0.0283	0.0354

TABLE 3. Summary of thermal coefficient of all manufacturers' DUTs

To compare the results to the published specification from MFG A, the results needed to be converted and are listed in **Table 4**.

MFG	Tag #	TC Zero (%FS/°F)	TC Span (%FS/°F)
A	DUT 1	0.0023	0.0313
	DUT 2	0.0071	0.0180
	DUT 3	0.0065	0.0313
	DUT 4	0.0012	0.0308

TABLE 4. Summary of Thermal Coefficient of MFG A DUTs

Comparing test results with the published specifications (**FIGURE 1**), the MFG A devices are meeting their thermal coefficient specification.

To compare the results to the published specification from MFG B, the results needed to be converted and are listed in **Table 5**.

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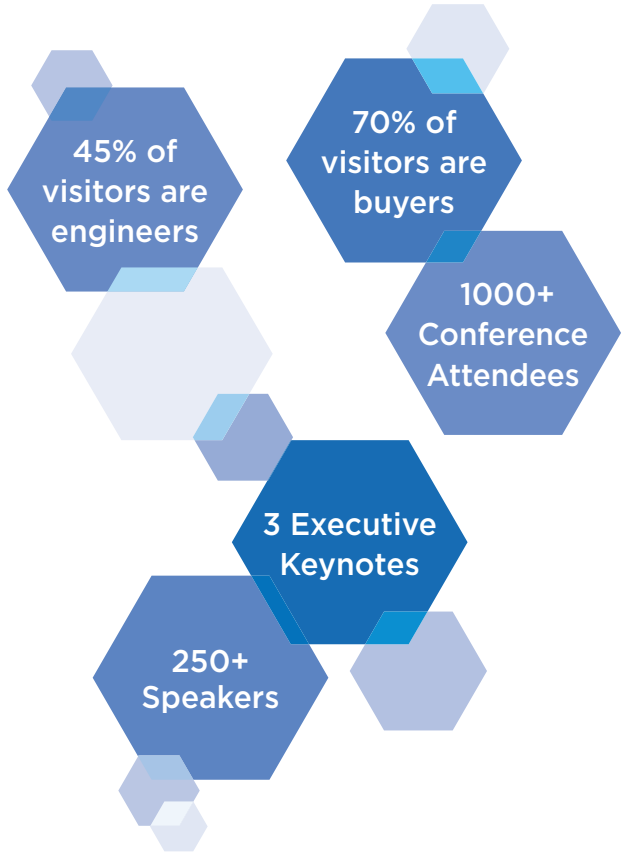

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MFG	Tag #	TC Zero (%FS/10K)	TC Span (%FS/10K)
B	DUT 5	0.0120	0.0990
	DUT 6	0.0420	0.1550
	DUT 7	0.0270	0.1200
	DUT 8	0.0220	0.1140

TABLE 5. Summary of Thermal Coefficient of MFG B DUTs

Compared with the published specifications (**FIGURE 2**), the MFG B devices are meeting their thermal coefficient specification at zero. All the MFG B devices except DUT 6 meet the of the thermal coefficient specification at span. However, the TC span for DUT 6 is 0.15550%FS/10K, which is very close to the specification value (0.15%FS/10K).

To compare the results to the published specification from MFG C, the results needed to be converted and are listed in **Table 6**.

MFG	Tag #	TC Zero (%FS/50°C)	TC Span (%FS/50°C)
C	DUT 9	0.8850	1.1763
	DUT 10	0.5100	1.0725
	DUT 11	1.4163	1.7700
	DUT 12	1.2600	1.6138

TABLE 6. Summary of Thermal Coefficient of MFG C DUTs

Compared to the published MFG C specifications (**FIGURE 3**), the MFG C devices are meeting their thermal coefficient specification.

The error change with the temperature increase of all the DUTs at 0%FS is shown graphically in **FIGURE 6**. Comparing the three plots, it can be seen that the DUTs from manufacturer C have the largest thermal variation across the temperature range of the test as well as device to device variation. The DUTs from manufacturer B have the smallest thermal variation across the temperature range of the test as well as device to device variation.

The error change with the temperature increase of all the DUTs at 100%FS is shown graphically in **FIGURE 7**. Comparing the three plots, it can be seen that the DUTs from manufacturer C have the largest thermal variation across the temperature range of the test as well as device to device variation. The DUTs from manufacturer B have the smallest fluctuation across the temperature range.

Conclusion

Based on this study, transducers marketed as comparable to each other display dramatically different performance levels within a relatively small temperature range which could lead to process reproducibility challenges. As the demand for higher temperature applications increases, these temperature performance variances will become more pronounced. These variations may prove to be very problematic with tool-to-tool process replication or when a transducer is replaced as a repair activity and the new transducer does not have the same performance characteristic as the old unit. The test results also demonstrate that the published specifications need to be standardized to improve direct comparison by end users. In addition, a uniform test procedure and data processing method needs to be adopted by the industry. The pressure measurement task force of SEMI North America Gases and Facilities Committee has developed and published a new pressure transducer measurement standard in November of 2016 based on this study.

Temperature-related shift not only contributes to the overall inaccuracy of a pressure transducer in a particular application, but they also factor into the economics of designing and manufacturing pressure transducers. This is due to the fact that temperature compensation is a complex, time-consuming, and expensive process that requires a significantly larger investment in production equipment and a deeper understanding of the influencing parameters.

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5. **SEMI F62-1111**
   Test method for determining mass flow controller performance characteristics from ambient and gas temperature effects
6. **SEMI F113-1116**
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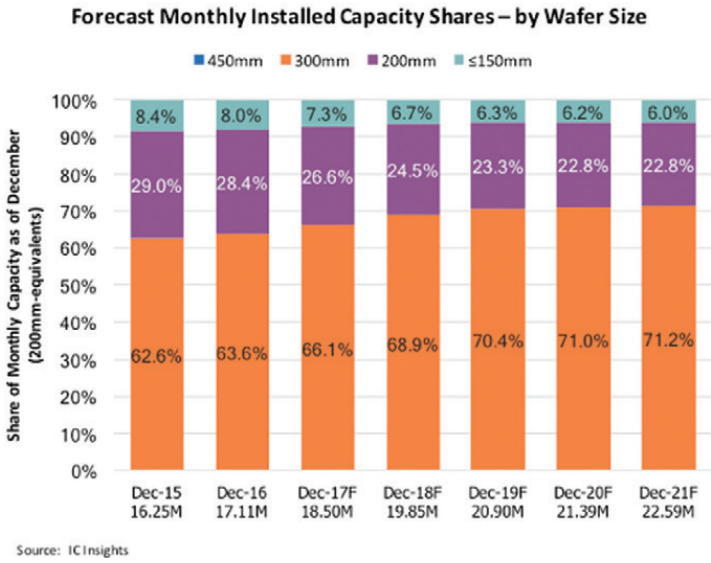
IC makers maximize 300mm, 200mm wafer capacity

With the prospects of large 450mm wafers going nowhere, IC manufacturers are increasing efforts to maximize fabrication plants using 300mm and 200mm diameter silicon substrates. The number of 300mm wafer production-class fabs in operation worldwide is expected to increase each year between now and 2021 to reach 123 compared to 98 in 2016, according to the forecast in IC Insights' Global Wafer Capacity 2017-2021 report.

As shown in FIGURE 1, 300mm wafers represented 63.6% of worldwide IC fab capacity at the end of 2016 and are projected to reach 71.2% by the end of 2021, which translates into a compound annual growth rate (CAGR) of 8.1% in terms of silicon area for processing by plant equipment in the five-year period.

The report's count of 98 production-class 300mm fabs in use worldwide at the end of 2016 excludes numerous R&D front-end lines and a few high-volume 300mm plants that make non-IC semiconductors (such as power transistors). Currently, there are eight 300mm wafer fabs that have opened or are scheduled to open in 2017, which is the highest number in one year since 2014 when seven were added, says the Global Wafer Capacity report. Another nine are scheduled to open in 2018. Virtually all these new fabs will be for DRAM, flash memory, or foundry capacity, according to the report.

Even though 300mm wafers are now the majority wafer size in use, both in terms of total surface area and in actual quantity of wafers, there is still much life remaining in 200mm fabs, the capacity report concludes. IC production capacity on 200mm wafers is expected to increase every year



through 2021, growing at a CAGR of 1.1% in terms of total available silicon area. However, the share of the IC industry's monthly wafer capacity represented by 200mm wafers is forecast to drop from 28.4% in 2016 to 22.8% in 2021.

IC Insights believes there is still much life left in 200mm fabs because not all semiconductor devices are able to take advantage of the cost savings 300mm wafers can provide. Fabs running 200mm wafers will continue to be profitable for many more years for the fabrication of numerous types of ICs, such as specialty memories, display drivers, microcontrollers, and RF and analog products. In addition, 200mm fabs are also used for manufacturing MEMS-based "non-IC" products such as accelerometers, pressure sensors, and actuators, including acoustic-wave RF filtering devices and micro-mirror chips for digital projectors and displays, as well as power discrete semiconductors and some high-brightness LEDs. ◆

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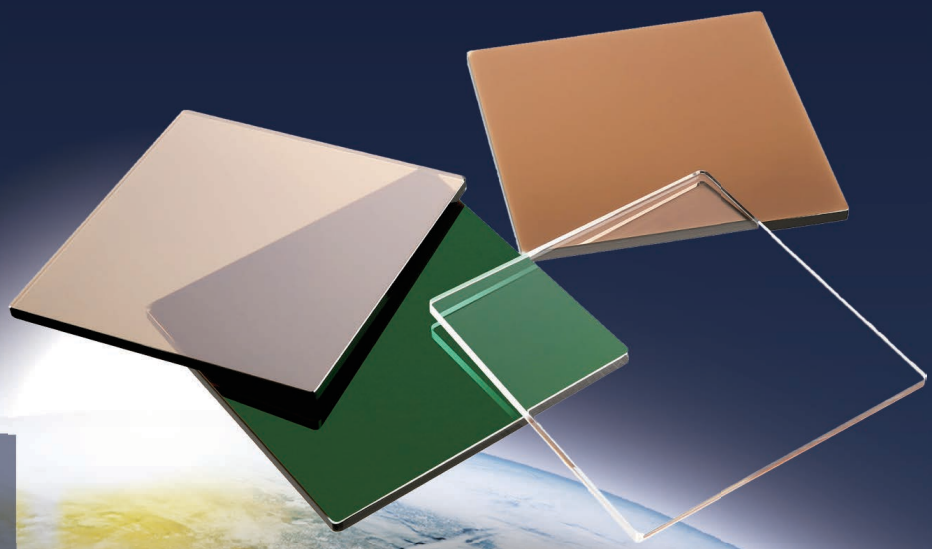

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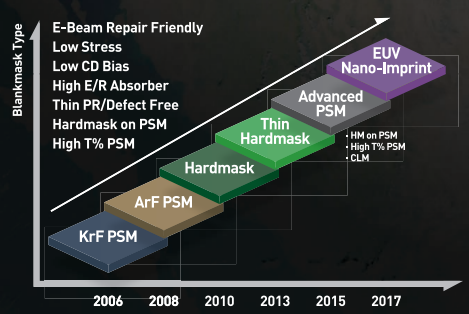

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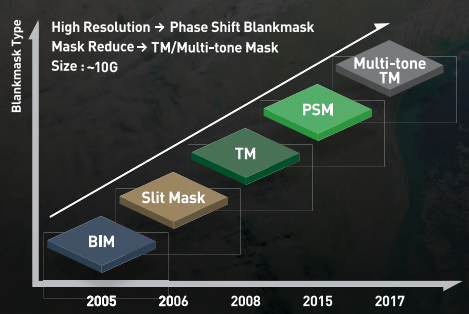

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